PG161-A00

TU106 6GB GDDR6, 192b, X16
DVI-D/DP + DP + HDMI

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19	IO: IFPA DP
20	IO: IFPB DP
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23	IO: IFPD DP
24	IO: NVHS Interface and Frame Lock
25	MISC1: Thermal, JTAG, GPIO,STEREO
26	MISC2: ROM, XTAL,STRAPS
27	PS: 1V8_AON
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30	PS: FBVDDQ
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32	PS: NVVDD Controller
33	PS: NVVDD Controller OVR3i
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35	PS: NVVDD Phase 3,5
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38	PS: Input, Filtering, and Monitoring
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43	SEQ: 5V, 1V8, NV3V3 ENABLE
44	SEQ: NV, PEX, FB ENABLE
45	SEQ: VOLTAGE MONITOR
46	SEQ: DISCHARGE
47	SEQ: MISC
48	LOGO LED
49	LED DRIVER & BOOST
50	FAN
51	PS: Pre-filter
52	MECH
53	PTC

V379-2.0 Change List (base on V375-2.1) :

Page	Description
6	change to GDDR5
7	change to GDDR5
8	change to GDDR5
9	change to GDDR5
11	change to GDDR5
12	change to GDDR5
13	change to GDDR5
14	change to GDDR5
25	Add GPIO10_FBVREF_SEL

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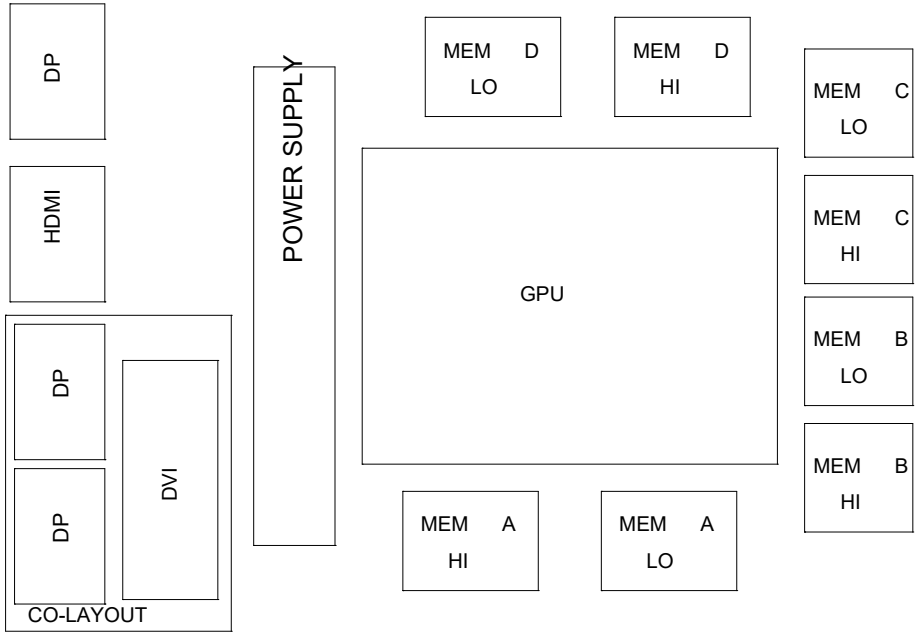
Page2: Block Diagram



Power Supply:

- Power Supply NVVDD-PH6
- Power Supply NVVDD-PH5
- Power Supply NVVDD-PH4
- Power Supply NVVDD-PH3
- Power Supply NVVDD-PH2
- Power Supply NVVDD-PH1
- Power Supply FBVDDQ-PH2
- Power Supply FBVDDQ-PH1
- Power Supply 5V
- PEX_VDD
- 1V8
- Fan
- DP_PWR

EXT_12V 2x4 PWR

PEX_12V Finger

3V3 Finger

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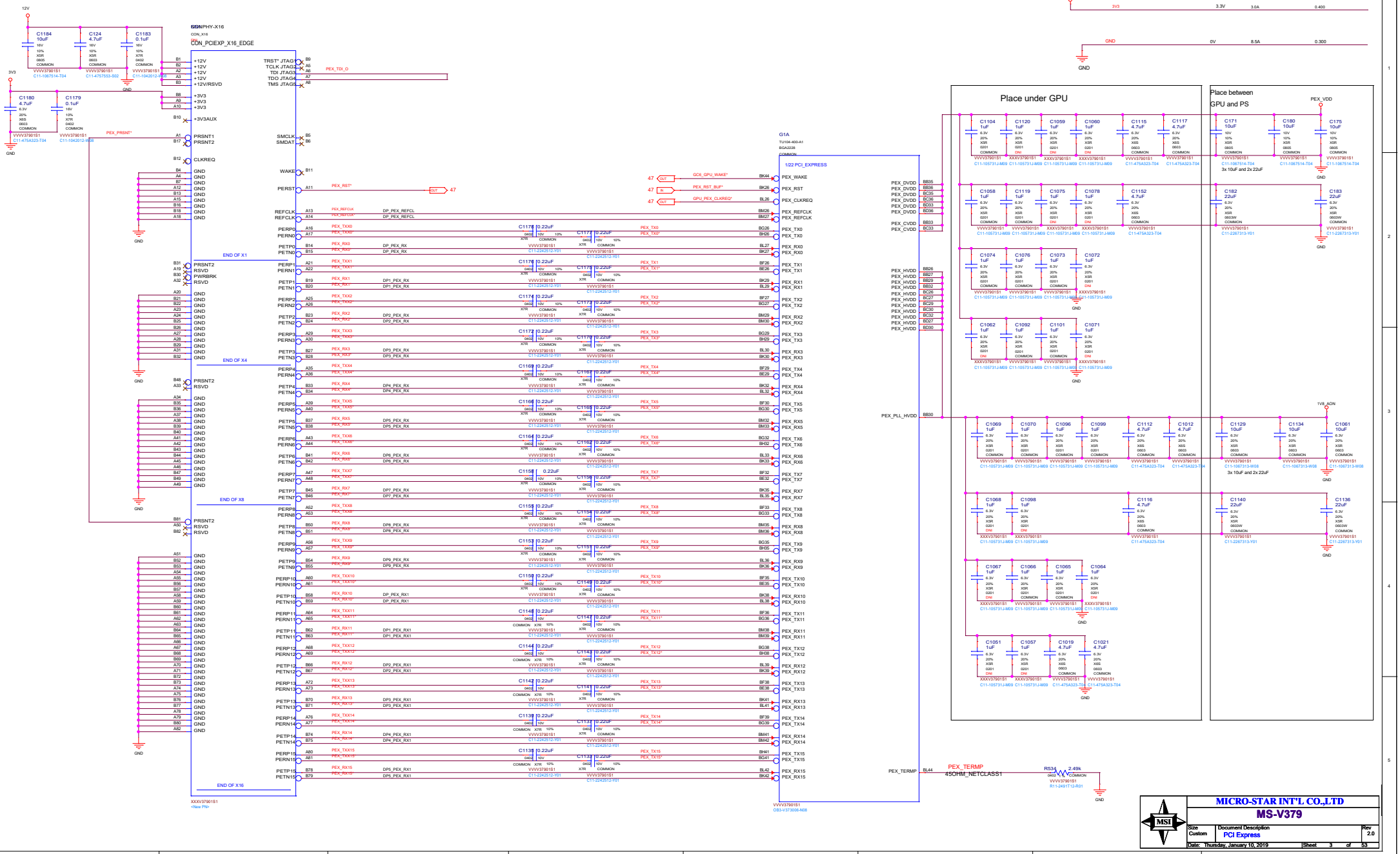
Page3: PCI Express



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	0.406
3V3	3.3V	3.0A	0.400
GND	0V	8.5A	0.300

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NO PEX GEN4 SUPPORT

DELETE RC TERMINATIONS

Page5: MEMORY: GPU Partition A/B

CMD	0_31	32_63
CMD0	CAS*	
CMD1	CKE*	
CMD2	RST*	
CMD3	RAS*	
CMD4	A1_A9	
CMD5	A0_A10	
CMD6	A12_RFU	
CMD7	ABI*	
CMD8	A6_A11	
CMD9	A7_A8	
CMD10	WE*	
CMD11	A5_BA1	
CMD12	A4_BA2	
CMD13	A2_BA0	
CMD14	A3_BA3	
CMD15	CS*	
CMD16		CAS*
CMD17		CKE*
CMD18		RST*
CMD19		RAS*
CMD20		A1_A9
CMD21		A0_A10
CMD22		A12_RFU
CMD23		ABI*
CMD24		A6_A11
CMD25		A7_A8
CMD26		WE*
CMD27		A5_BA1
CMD28		A4_BA2
CMD29		A2_BA0
CMD30		A3_BA3
CMD31		CS*

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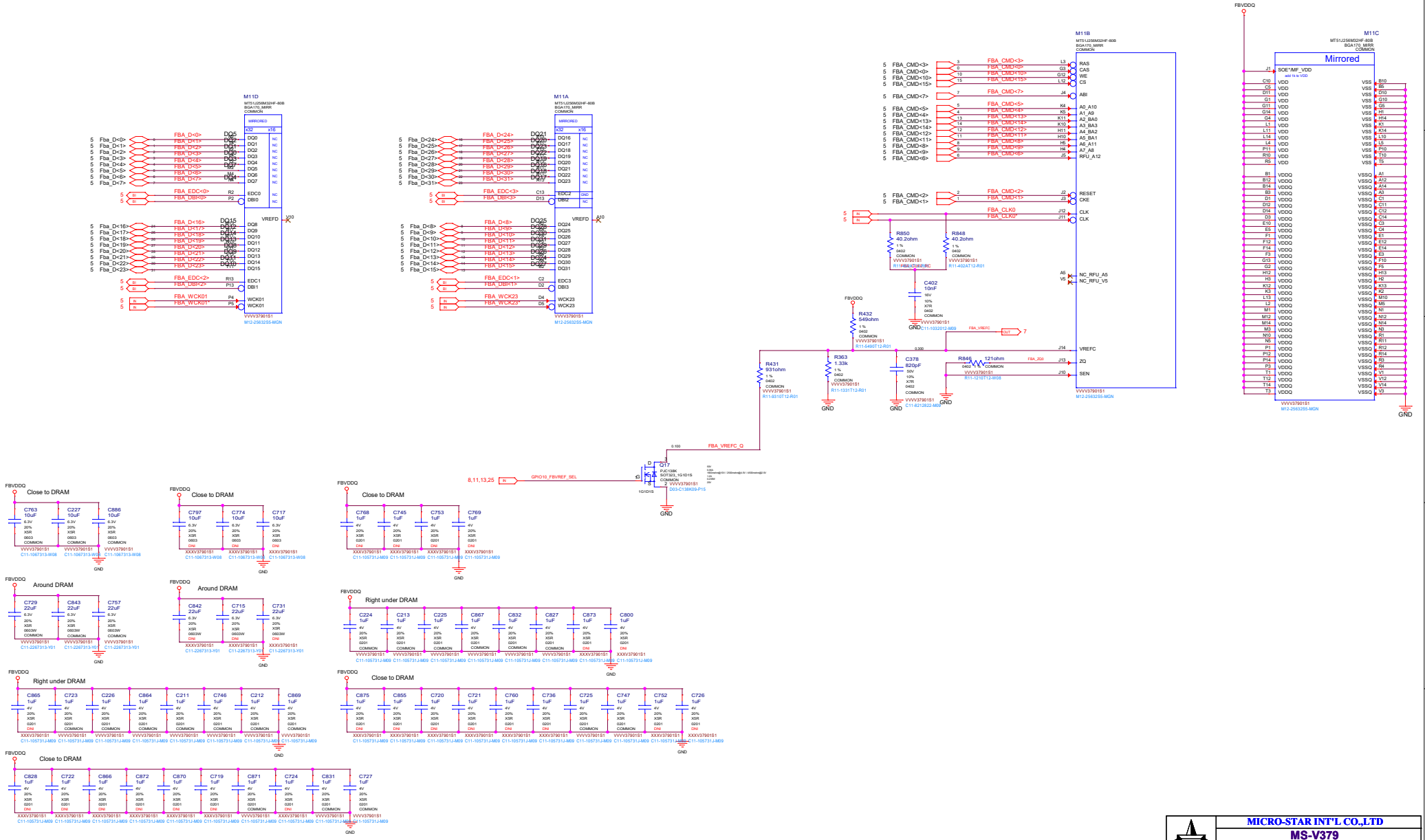
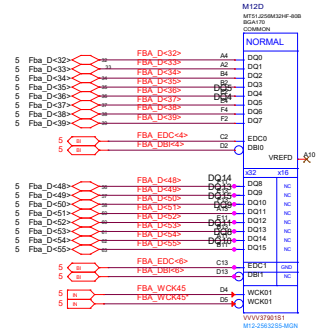
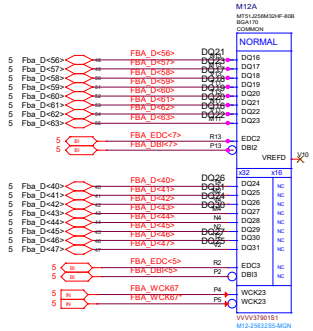
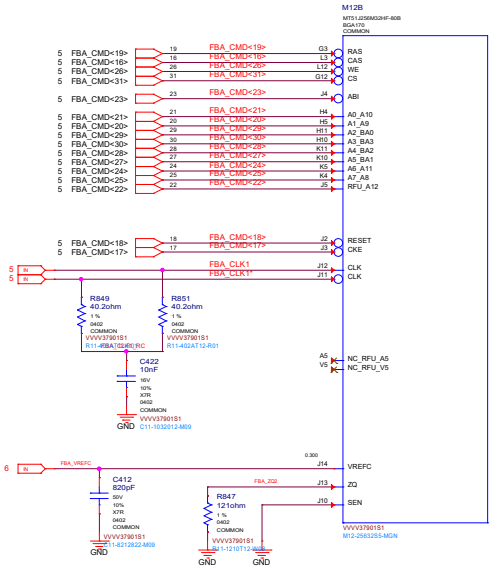
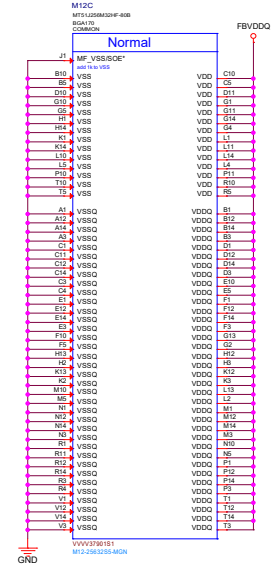
Page5: MEMORY: FBA Partition 31..0

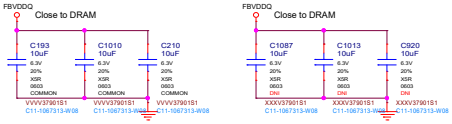












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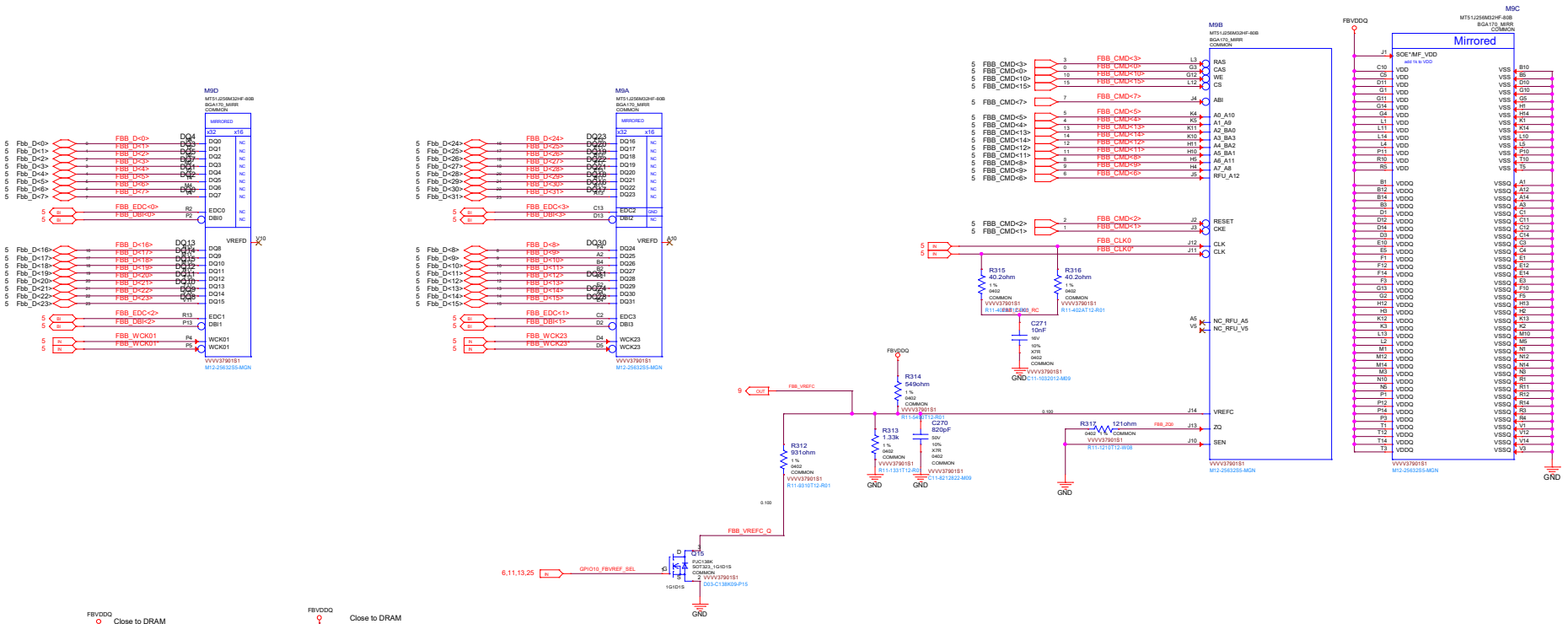
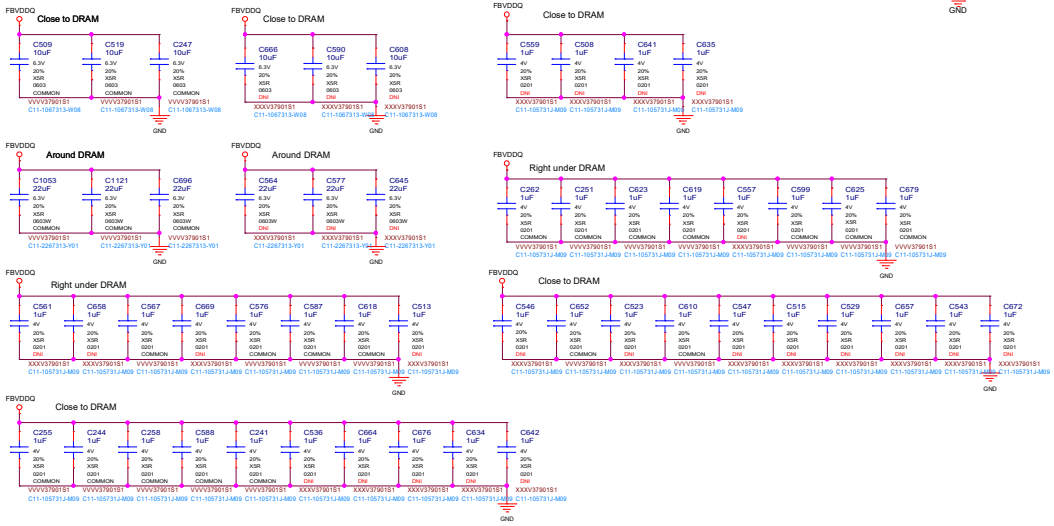
Page7: MEMORY: FBB Partition 31..0





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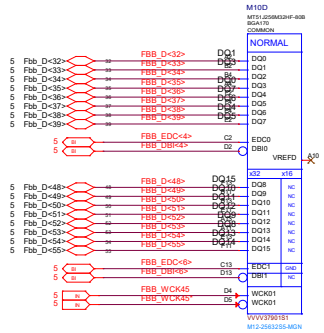

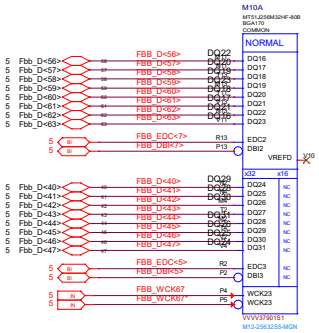

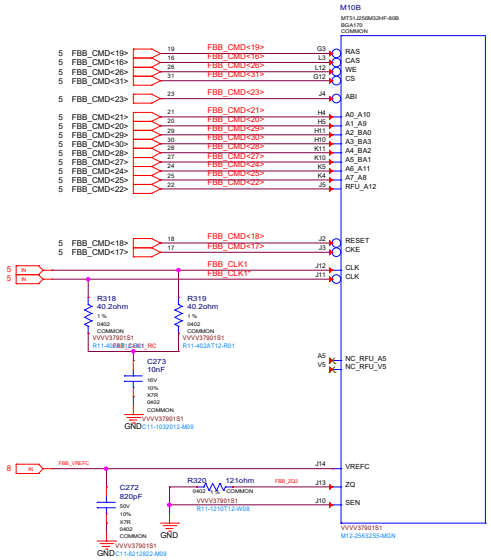

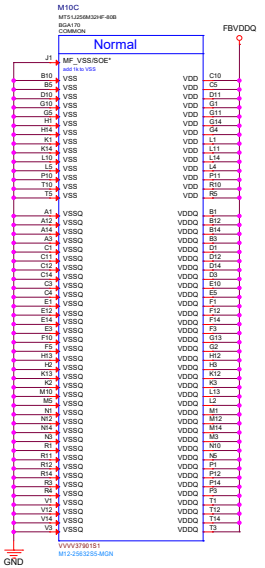

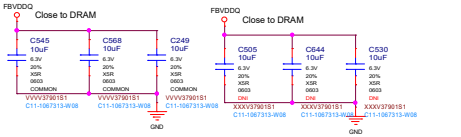

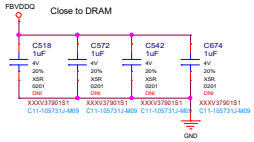

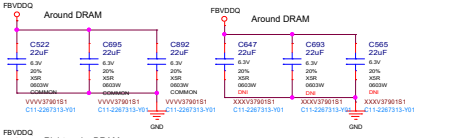

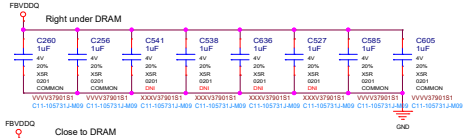

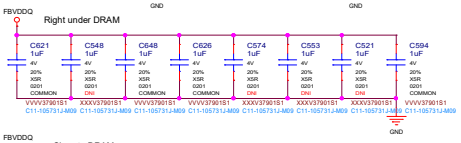

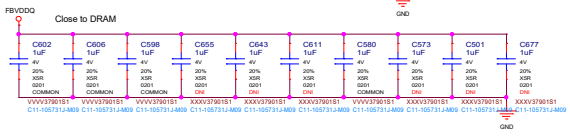

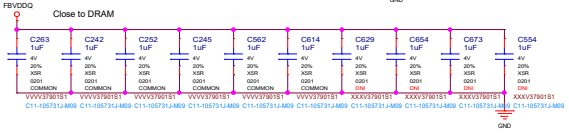

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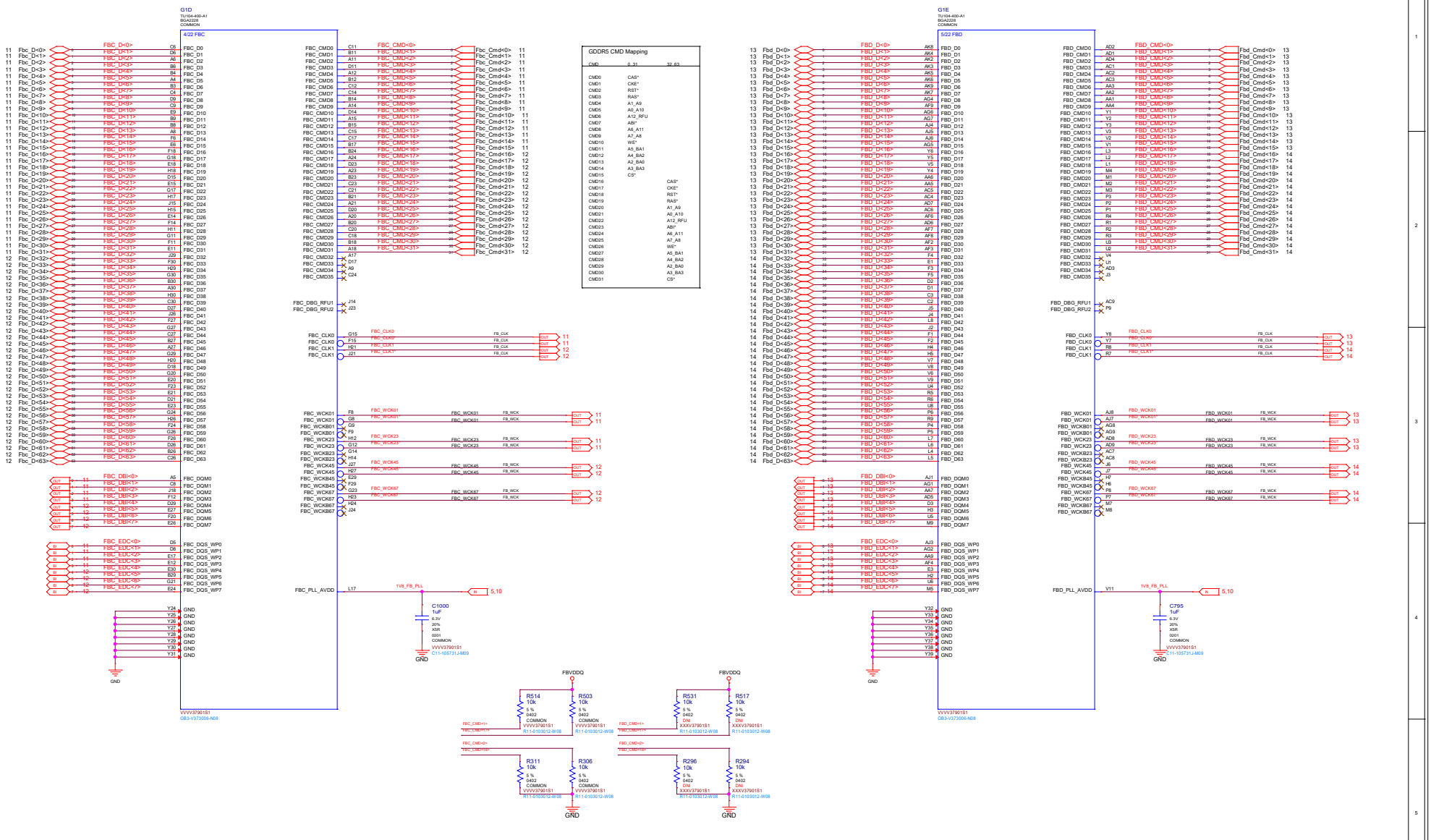
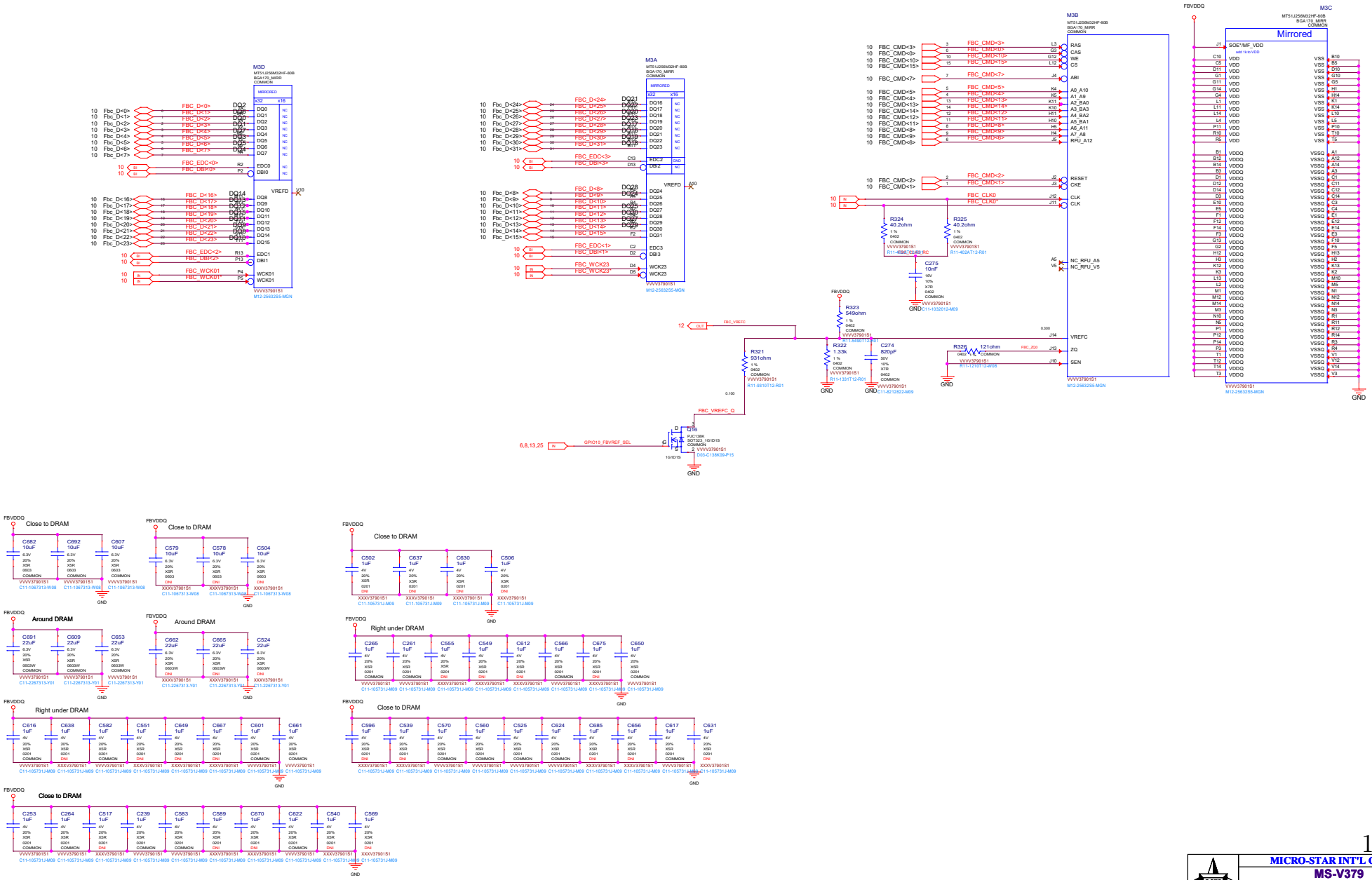
Page10: MEMORY: GPU Partition C/D





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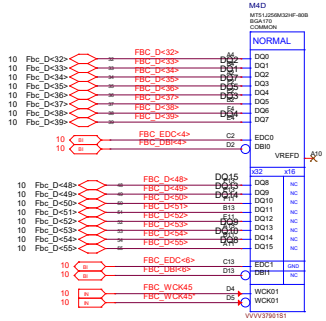
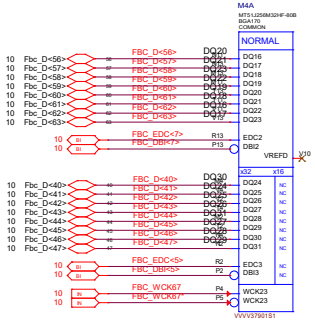
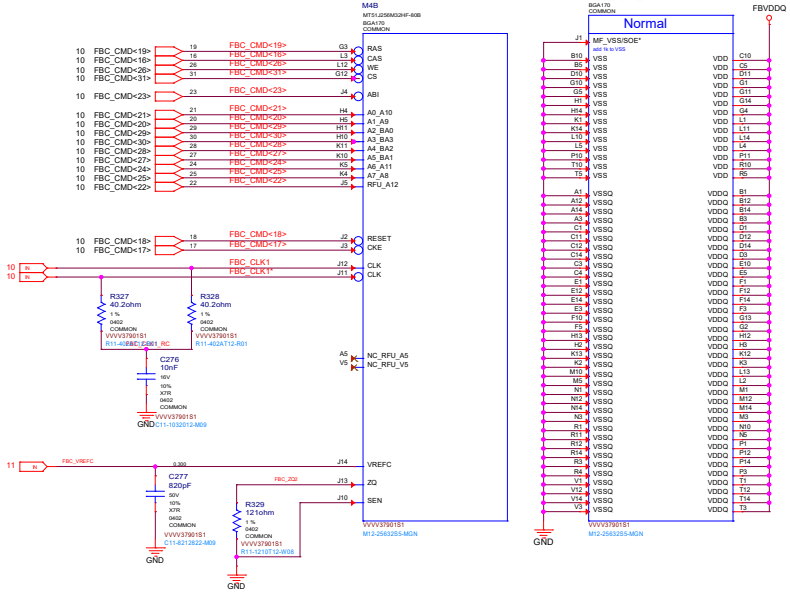
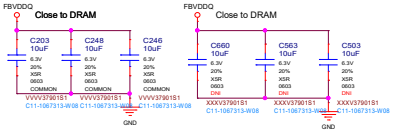
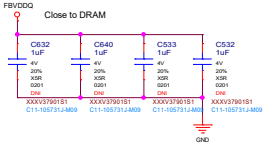
Page11: MEMORY: FBC Partition 63..32

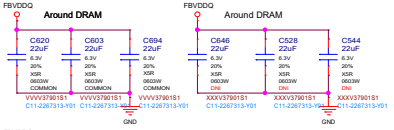


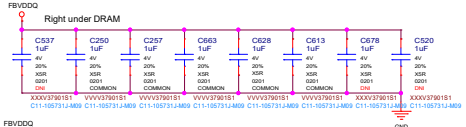


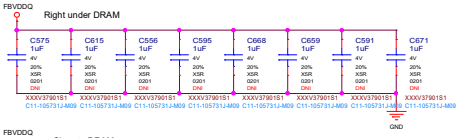


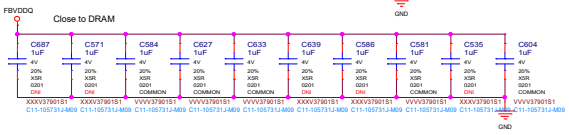












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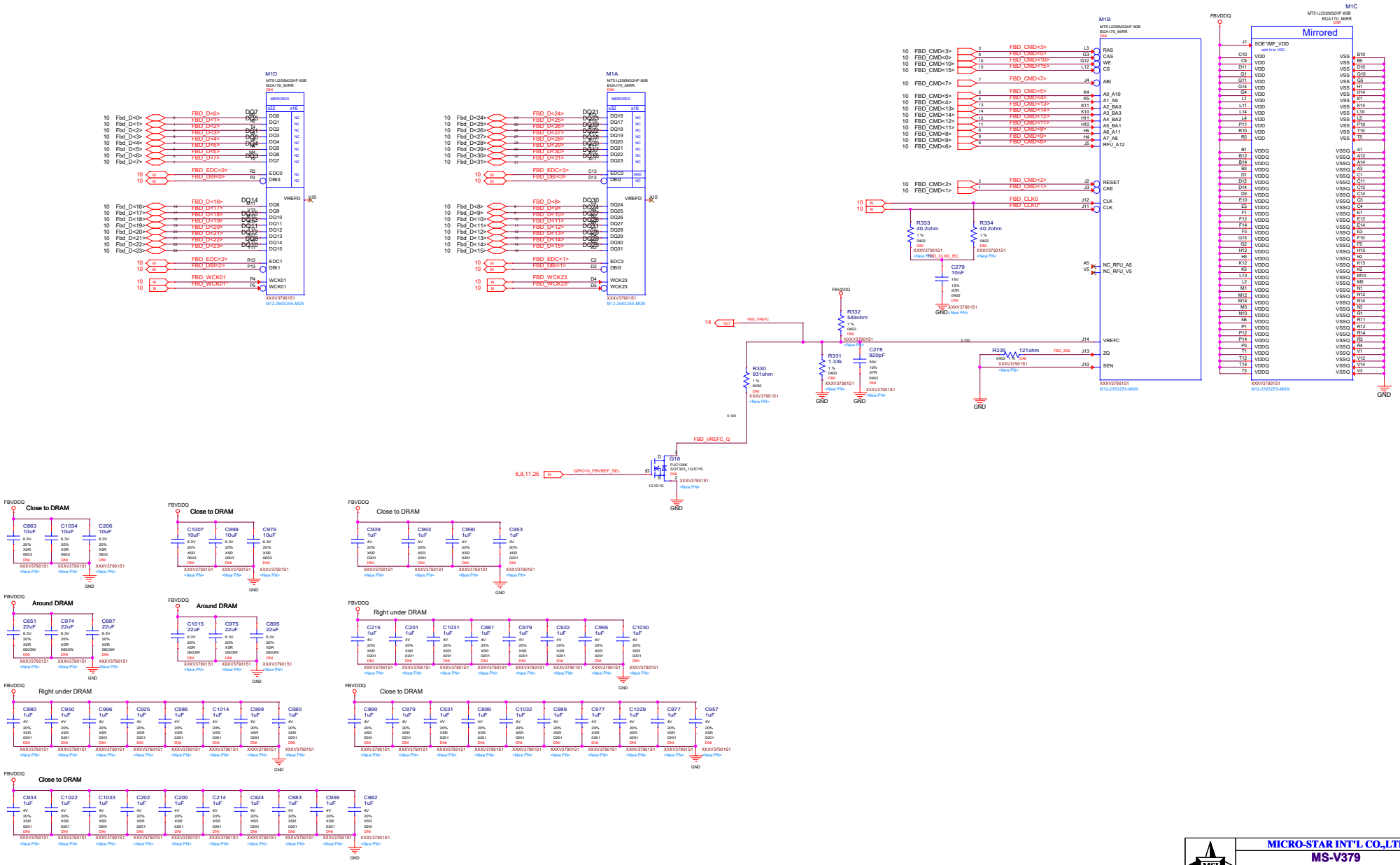
Page12: MEMORY: FBD Partition 31..0



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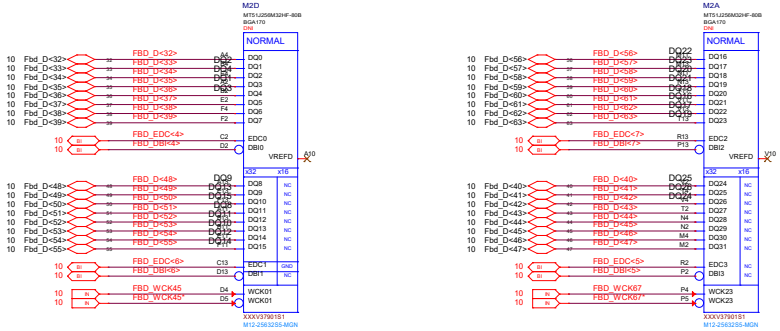
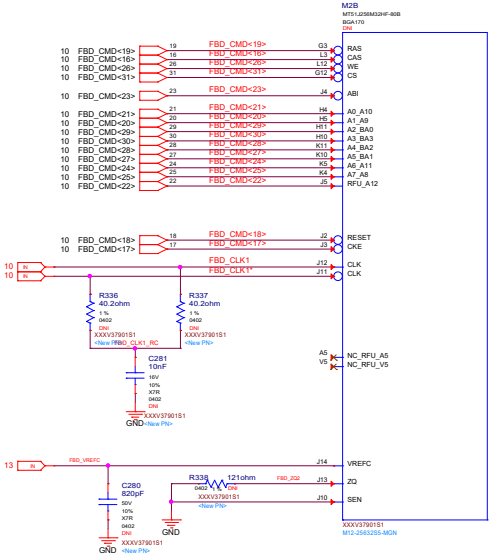
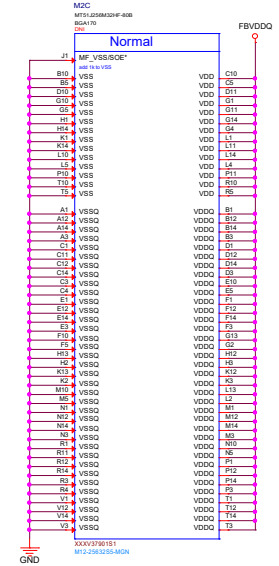
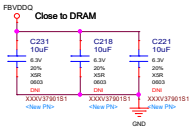
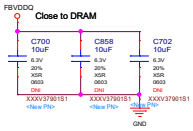
Page13: MEMORY: FBD Partition 63..32

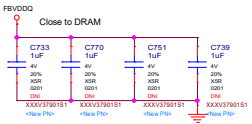


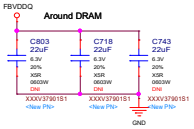


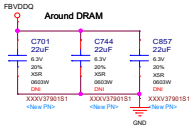


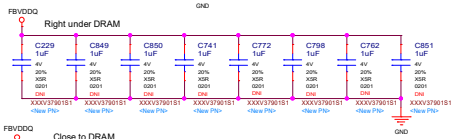


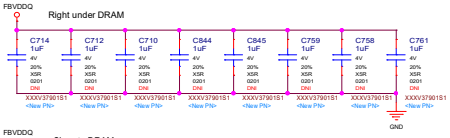


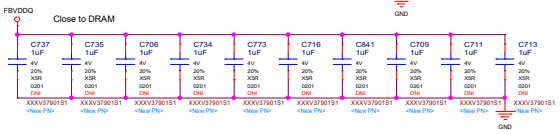


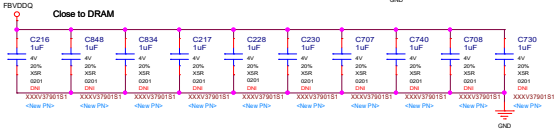












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MS-V379			
Size: Custom	Document Description: MEMORY_ FBD[63_32]		Rev: 2.0
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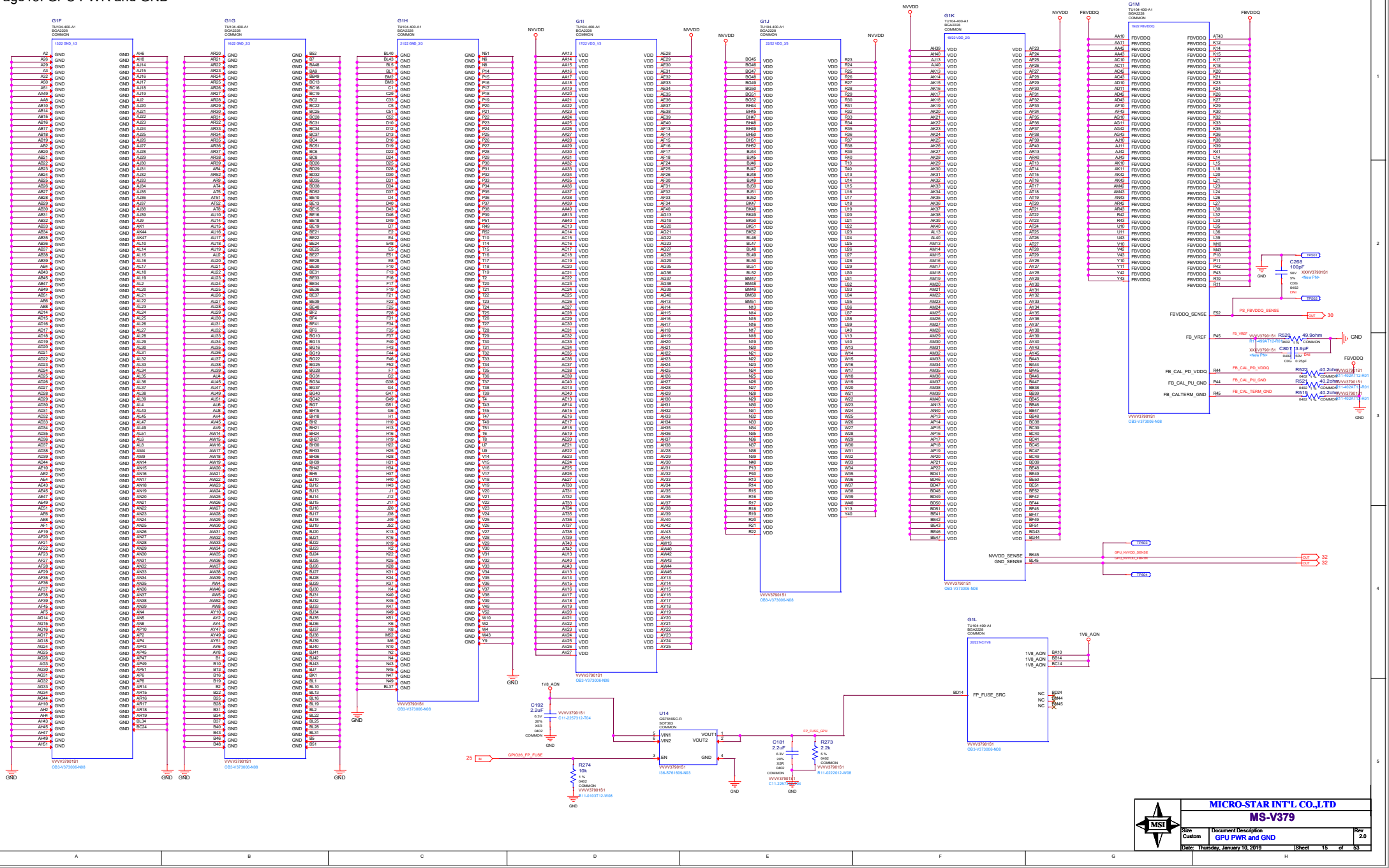
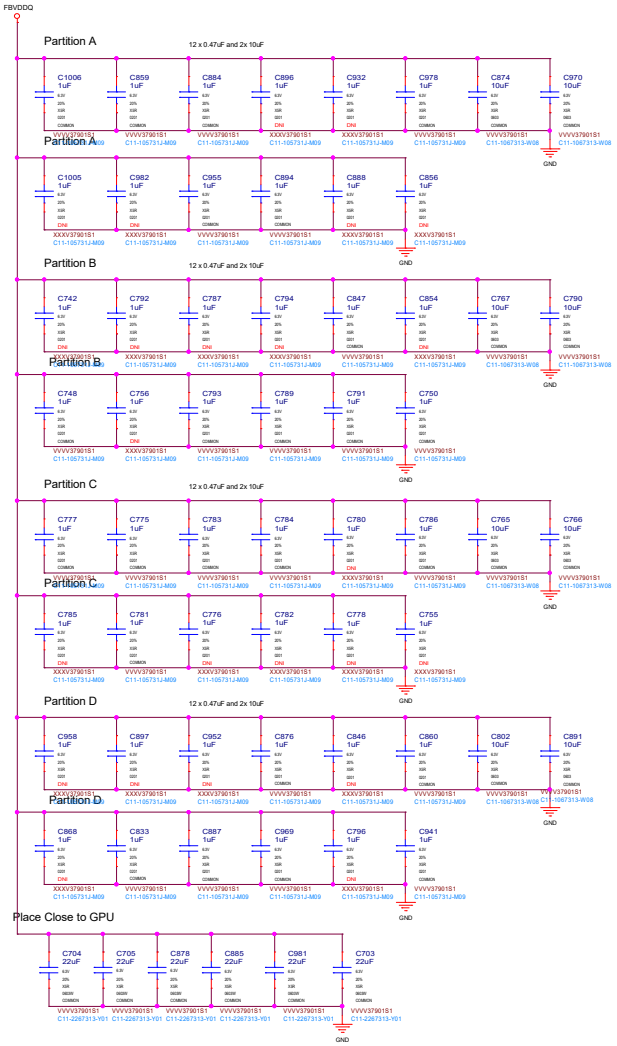
Page15: GPU PWR and GND

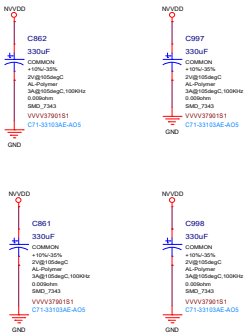


Page16: GPU Decoupling 1

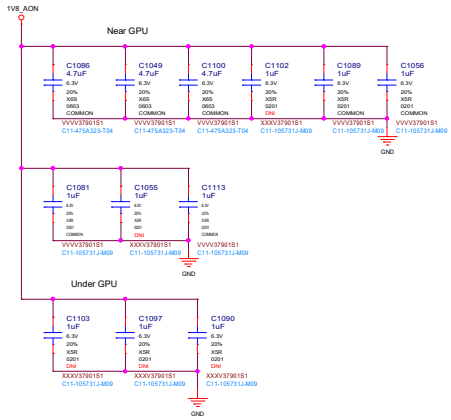
FBVDDQ



NVVDD



1V8_AON



MICRO-STAR INT'L CO.,LTD		
MS-V379		
Size: Custom	Document Description: GPU Decoupling 1	Rev: 2.0
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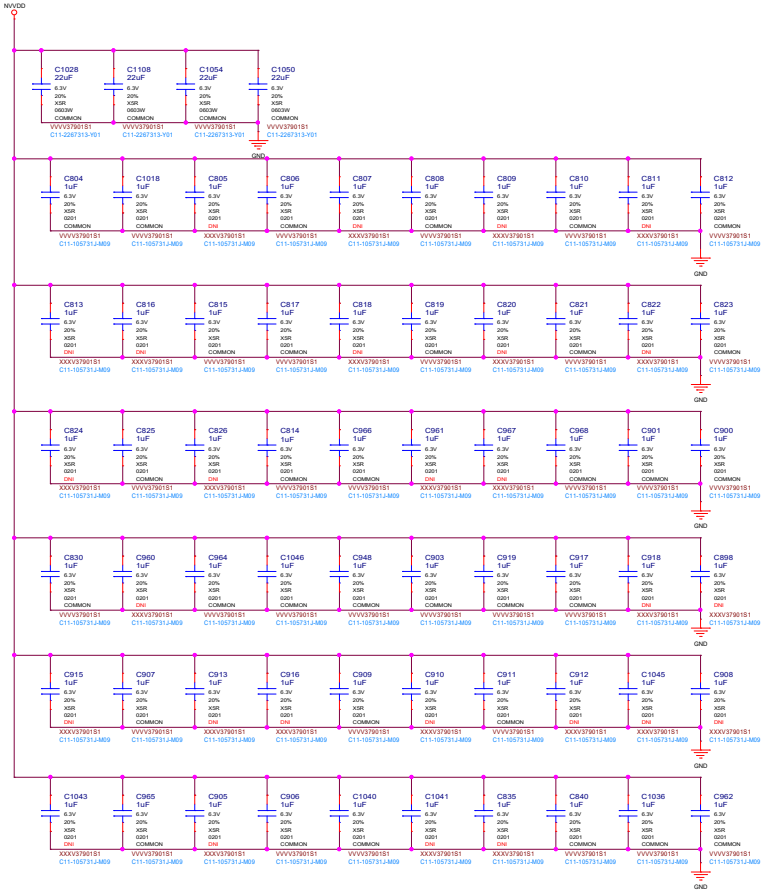
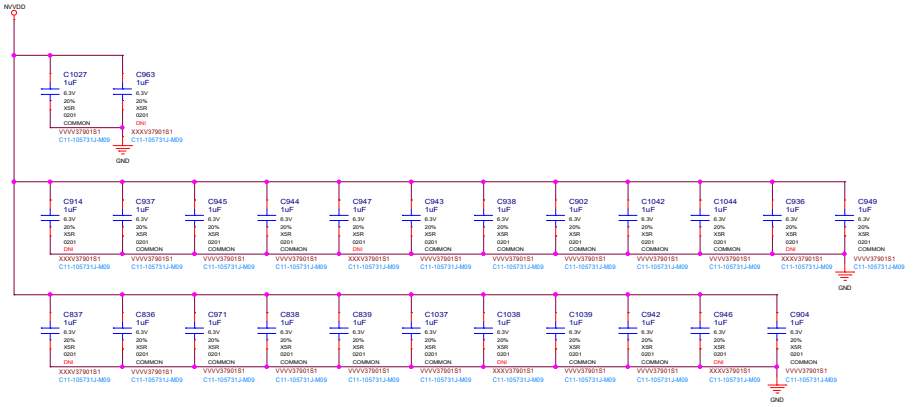
Page17: GPU Decoupling 2

NVVDD





MICRO-STAR INT'L CO.,LTD		
MS-V379		
Size: Custom	Document Description: GPU Decoupling 2	Rev: 2.0
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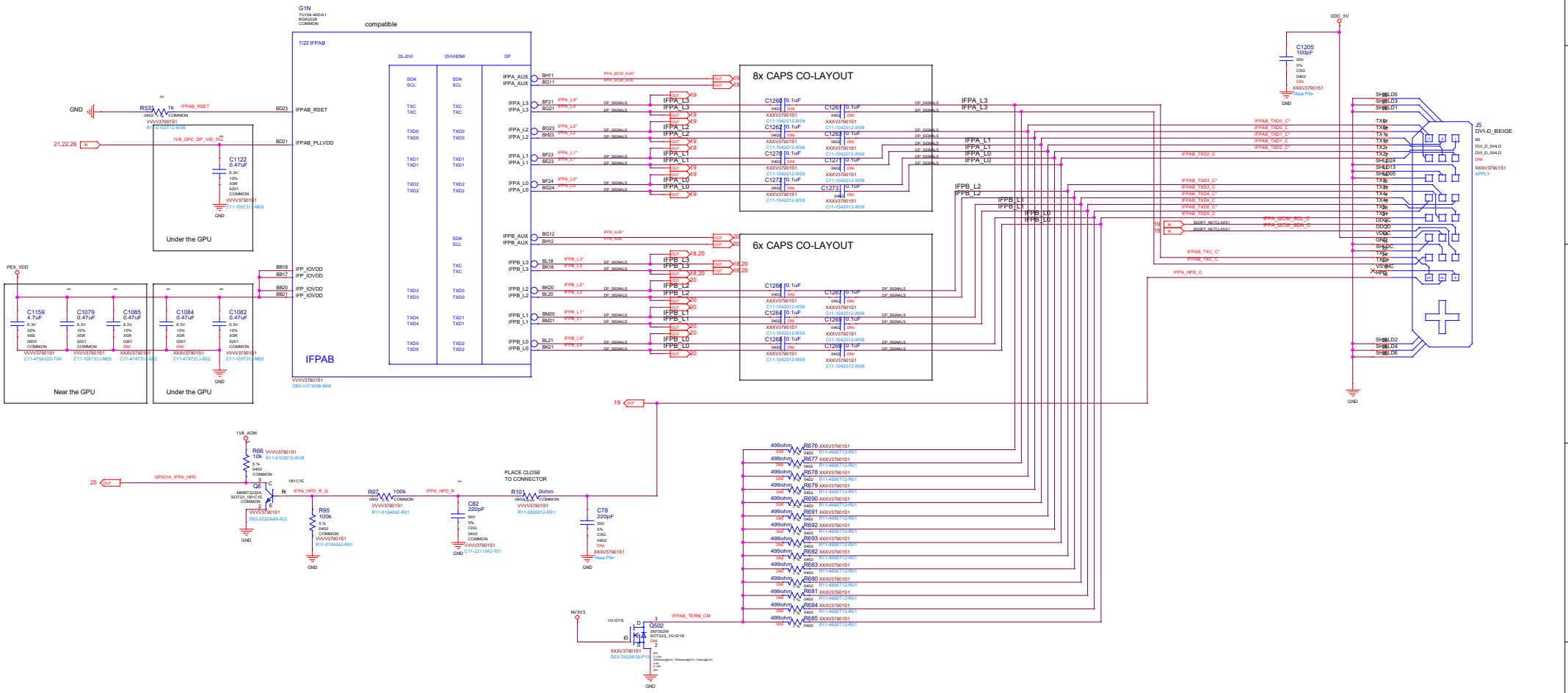
IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



MICRO-STAR INT'L CO.,LTD			
MS-V379			
Size: Custom	Document Description: IFPAB DVI-D-DL		Rev: 2.0
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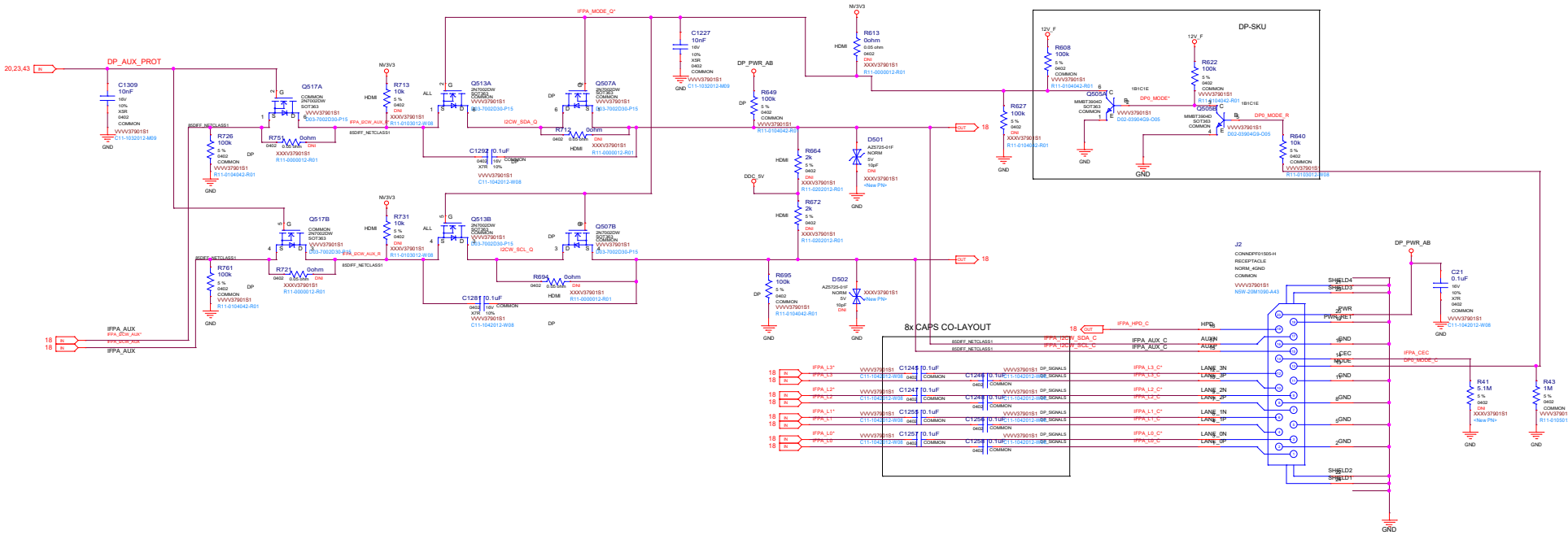

IFPA DP CO-LAYOUT WITH IFPAB DVI-D-DL

MICRO-STAR INT'L CO.,LTD		
MS-V379		
Size: Custom	Document Description: IFPA DP	Rev: 2.0
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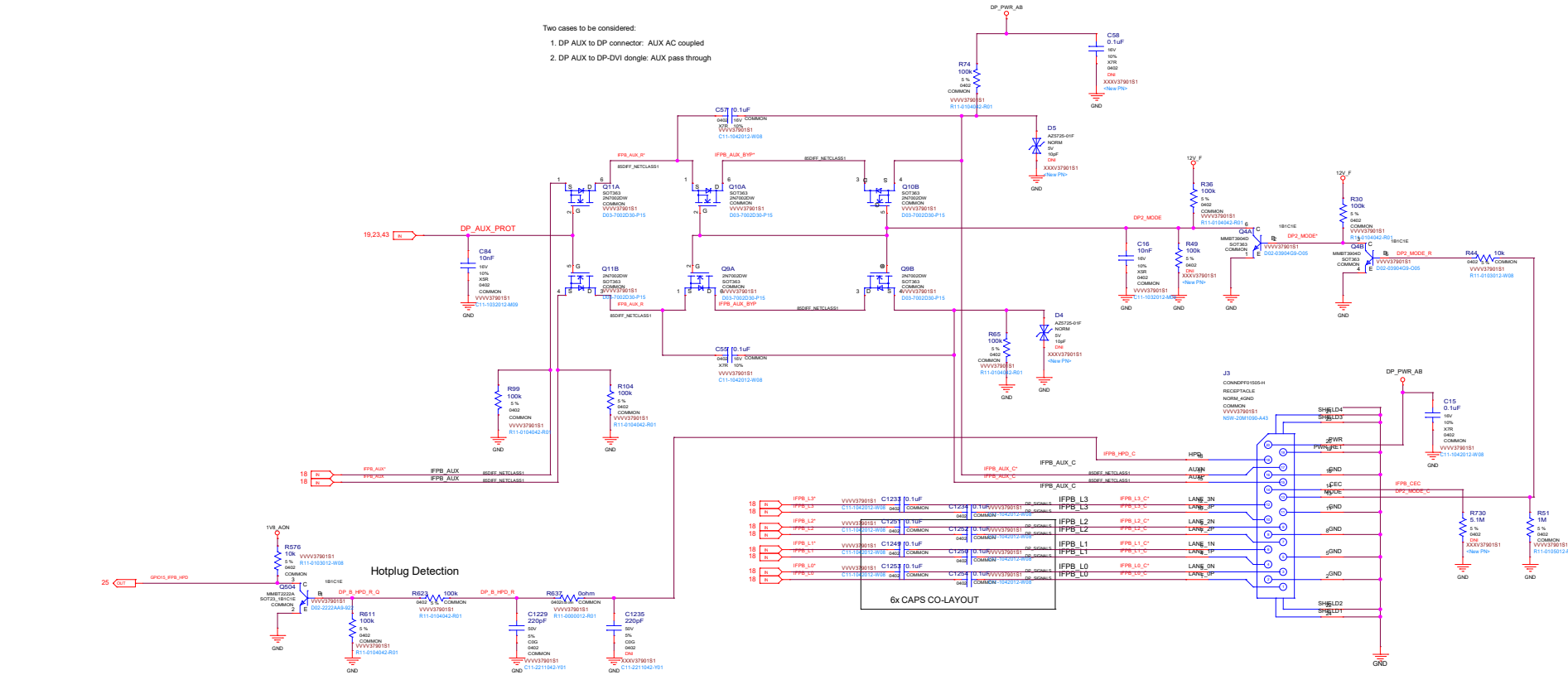
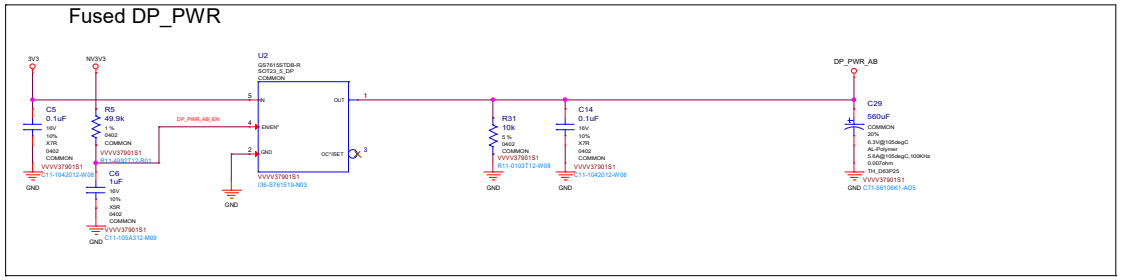
IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL





MICRO-STAR INT'L CO.,LTD		
MS-V379		
Size: Custom	Document Description: IFPB DP	Rev: 2.0
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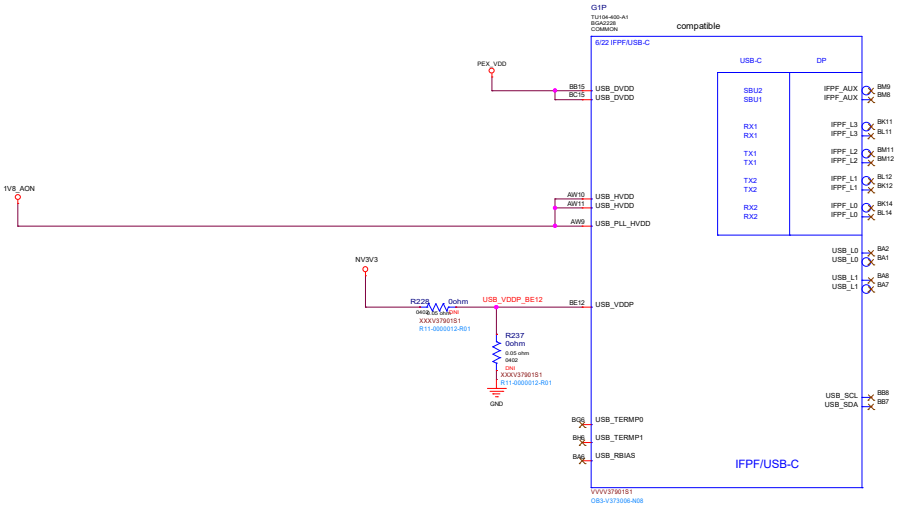
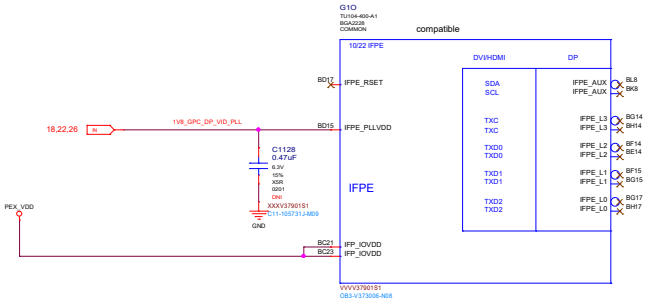


IFPF NC



IFPE NC

MICRO-STAR INT'L CO.,LTD

MS-V379

Size	Document Description	Rev
Custom	IFPE & IFPF USB-C NC	2.0

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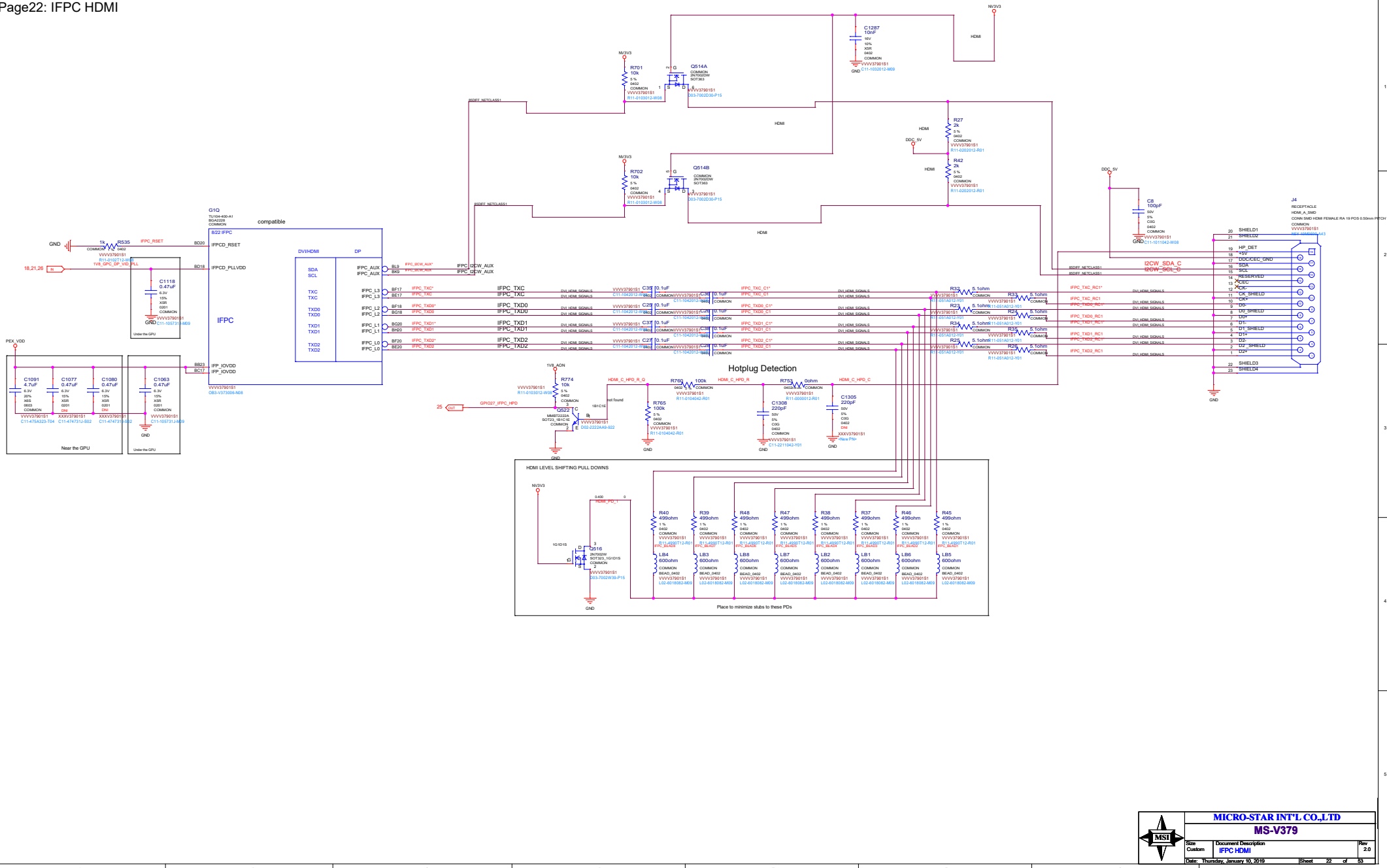
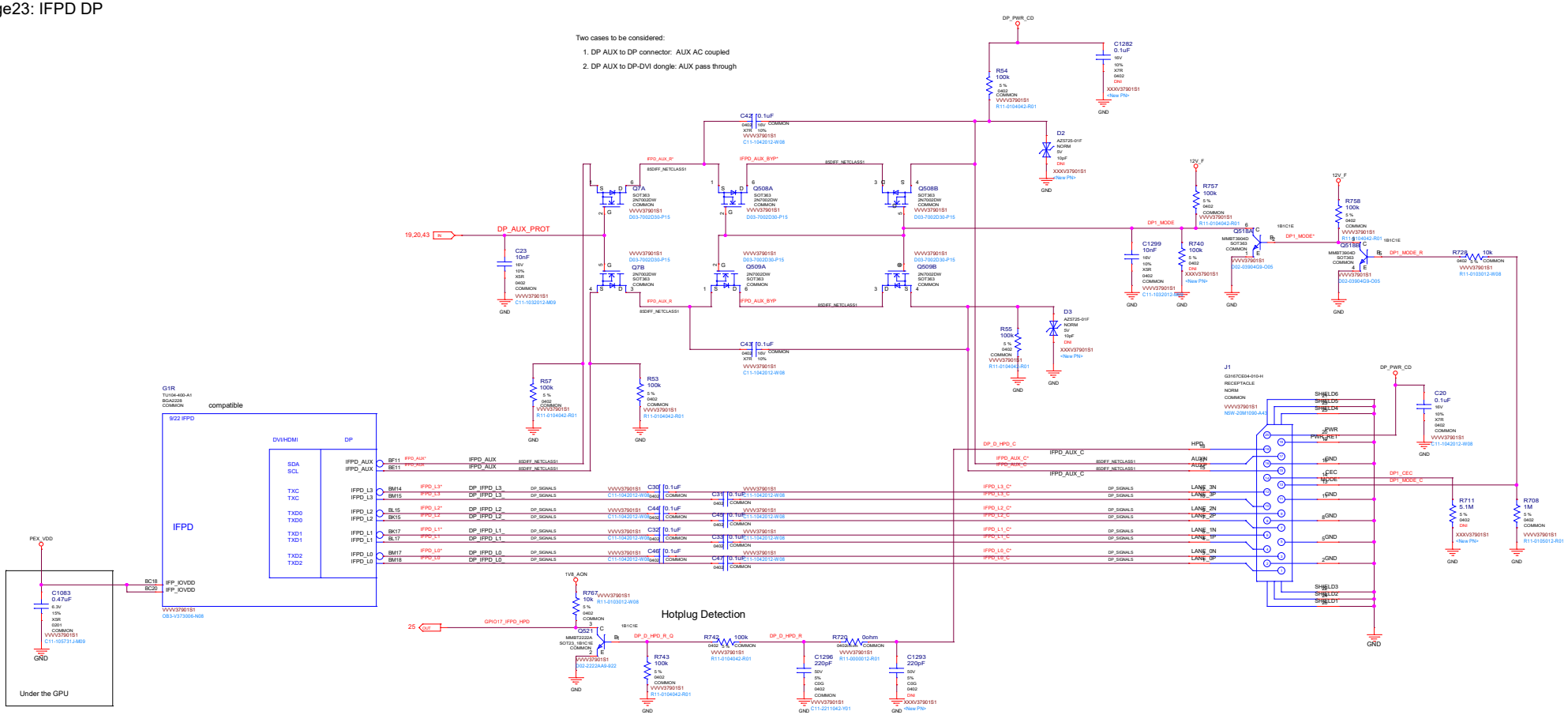
Page22: IFPC HDMI



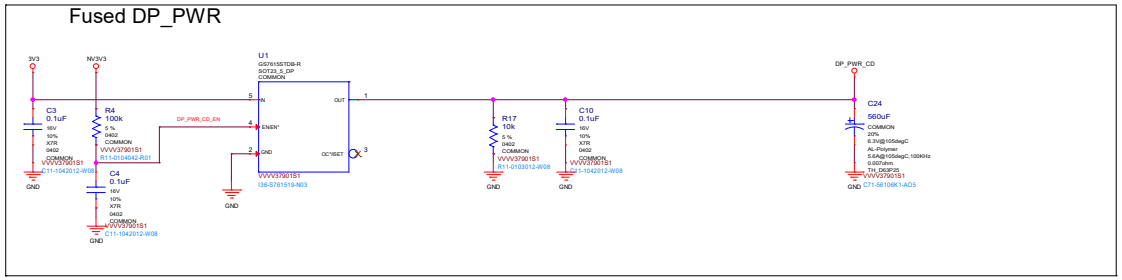
Page23: IFPD DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



Fused DP_PWR



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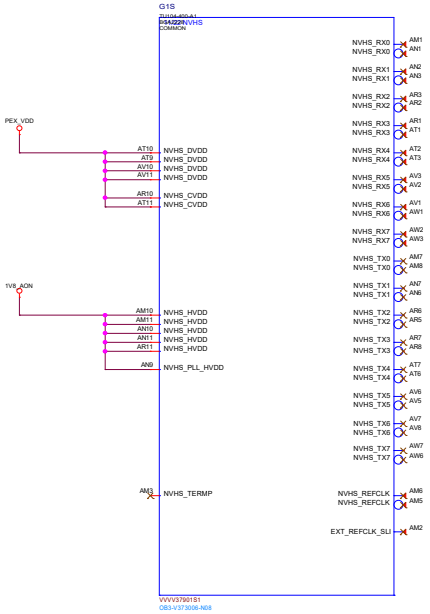
Page24: NVHS Interface and Frame Lock



19ci203

MSI	MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: NVHS Interface and Frame Lock	Rev: 2.0
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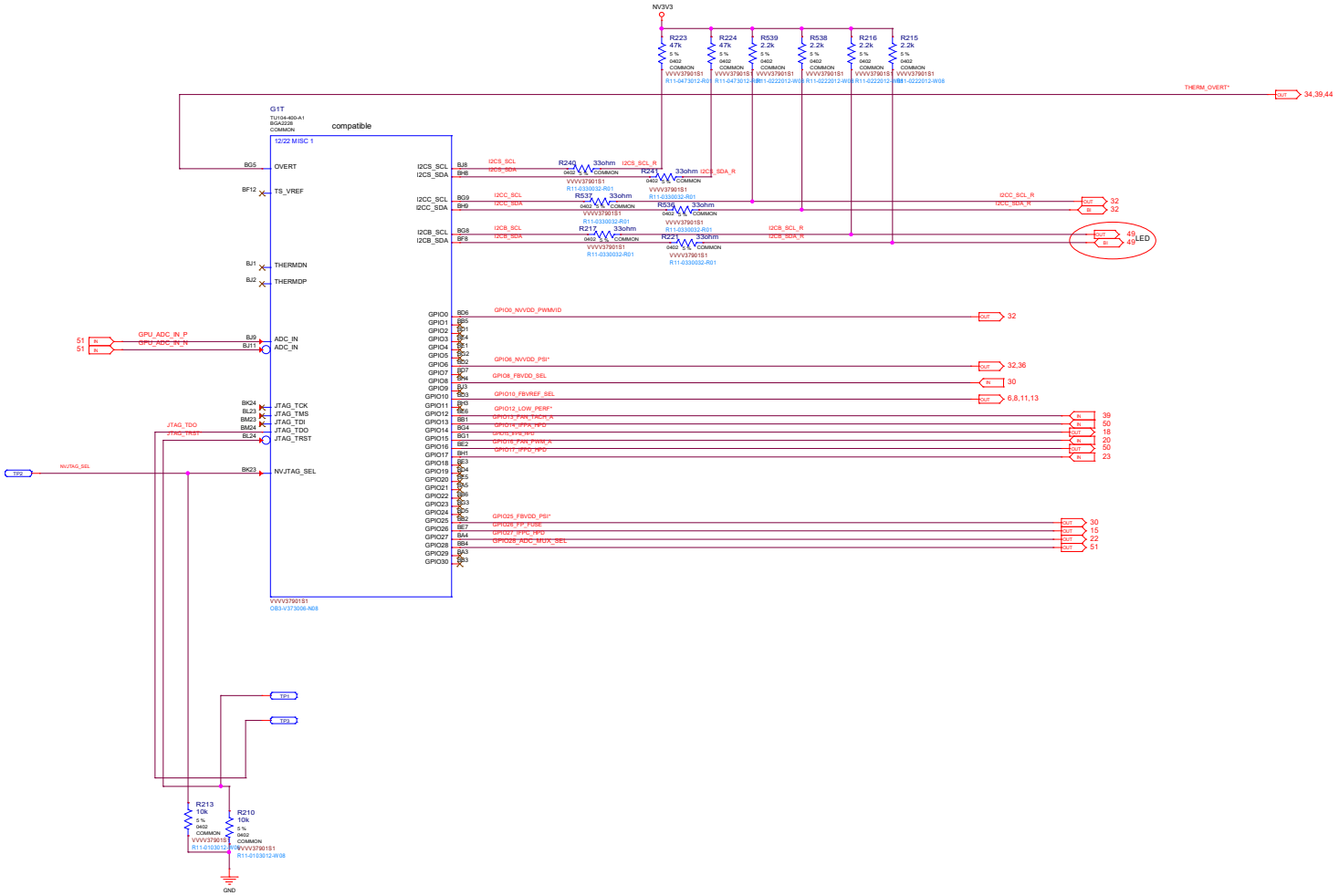
Page25: MISC1: Fan, Thermal, JTAG, GPIO



MICRO-STAR INT'L CO.,LTD	
MS-V379	
Size: Custom	Document Description: MISC1: Fan, Thermal, JTAG, GPIO
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Page26: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

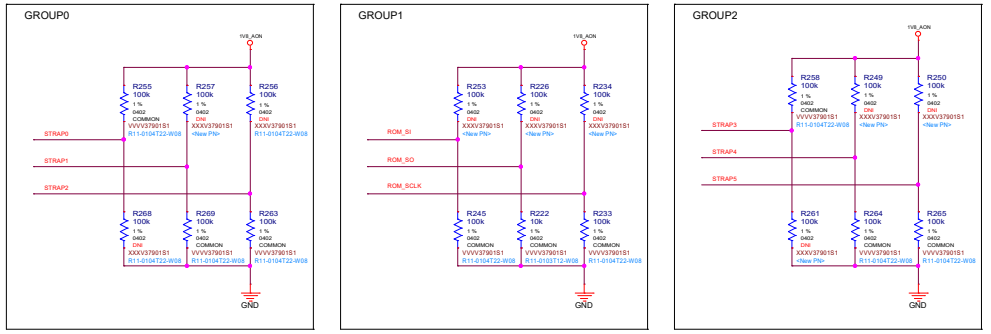
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

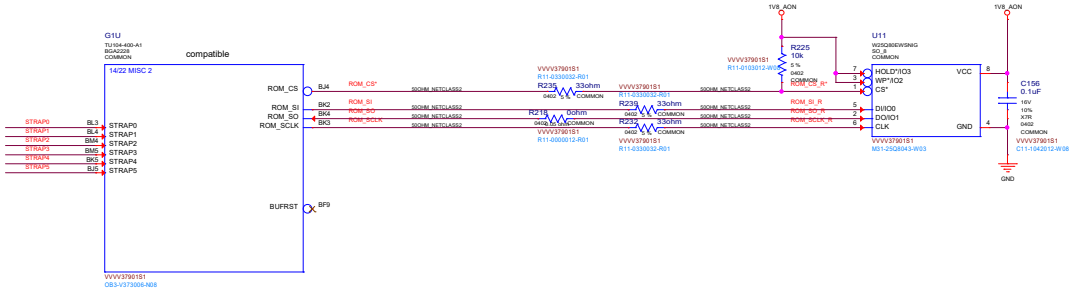
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

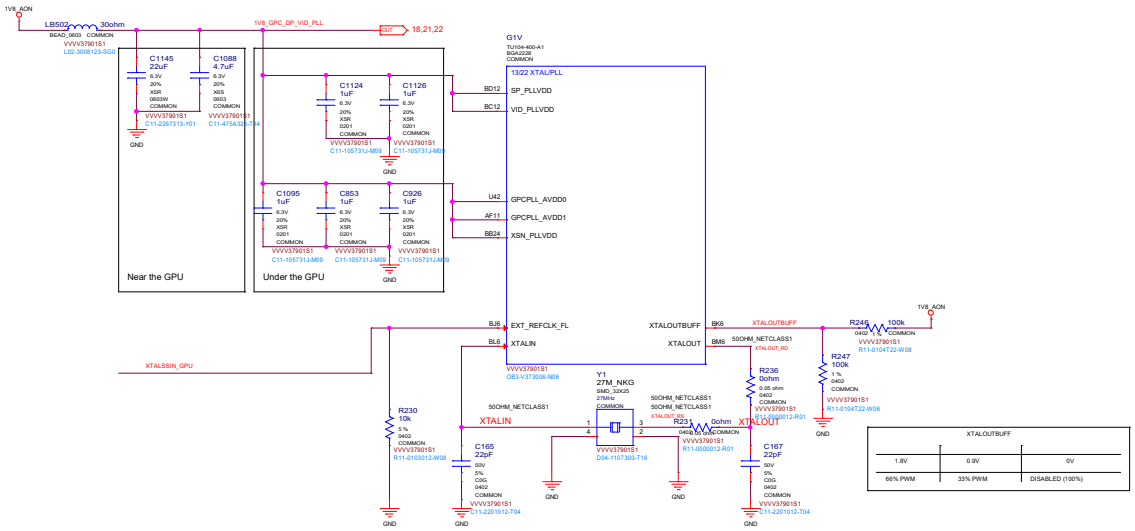
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE







MICRO-STAR INT'L CO.,LTD
MS-V379
Size: Custom
Document Description: MISC2: ROM, XTAL, Straps
Rev: 2.0
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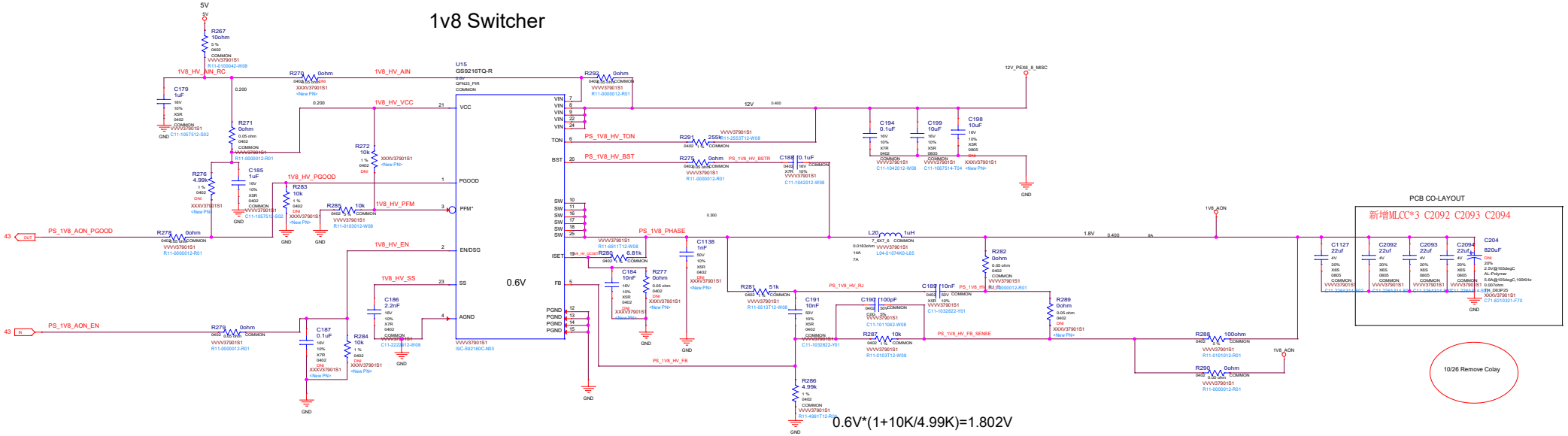
1v8 Switcher



MICRO-STAR INT'L CO.,LTD		
MS-V379		
Size: Custom	Document Description: PS: 1V8_AON	Rev: 2.0
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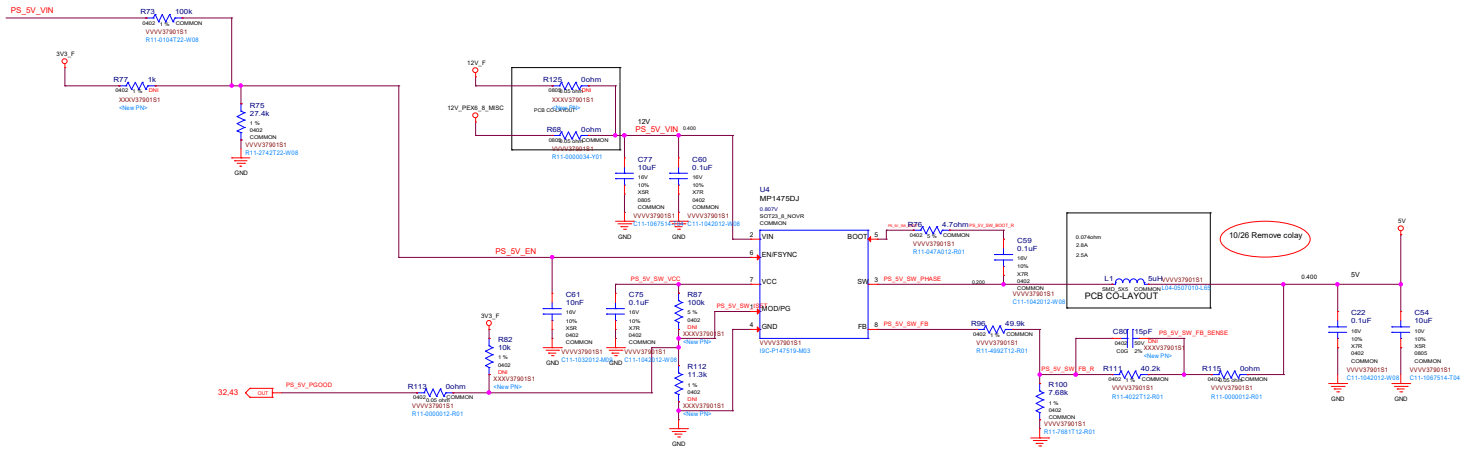

0.8V*(1+40.2K/7.68K)=4.9875V

MSI	MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: PS: 5V	Rev: 2.0
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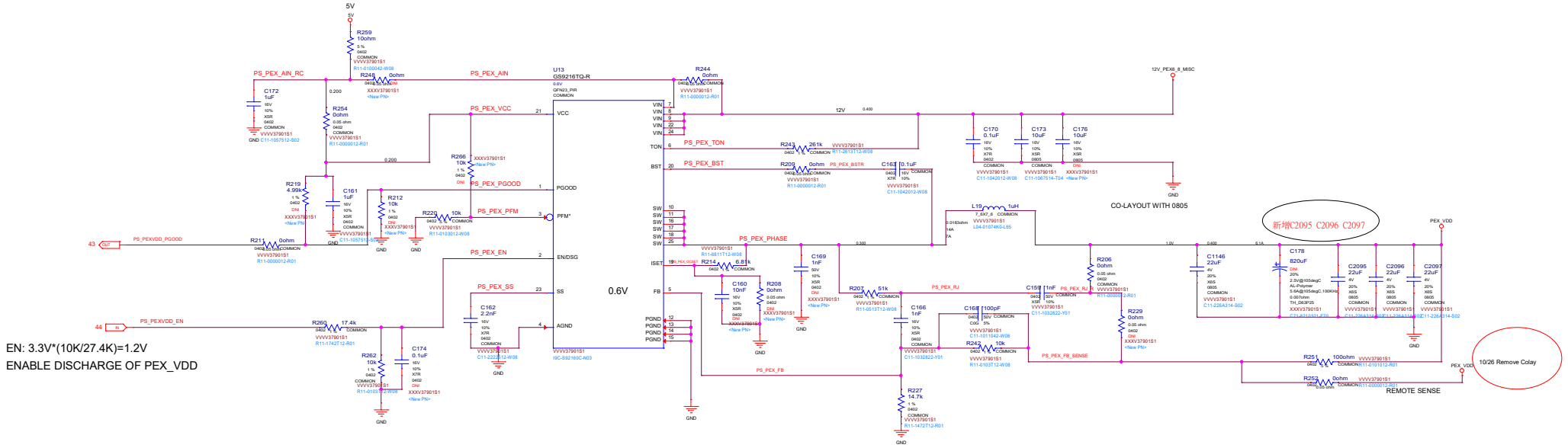
PEX Switcher



EN: 3.3V*(10K/27.4K)=1.2V

ENABLE DISCHARGE OF PEX_VDD

0.6V*(1+10K/14.7K)=1.008V

MICRO-STAR INT'L CO.,LTD		
MS-V379		
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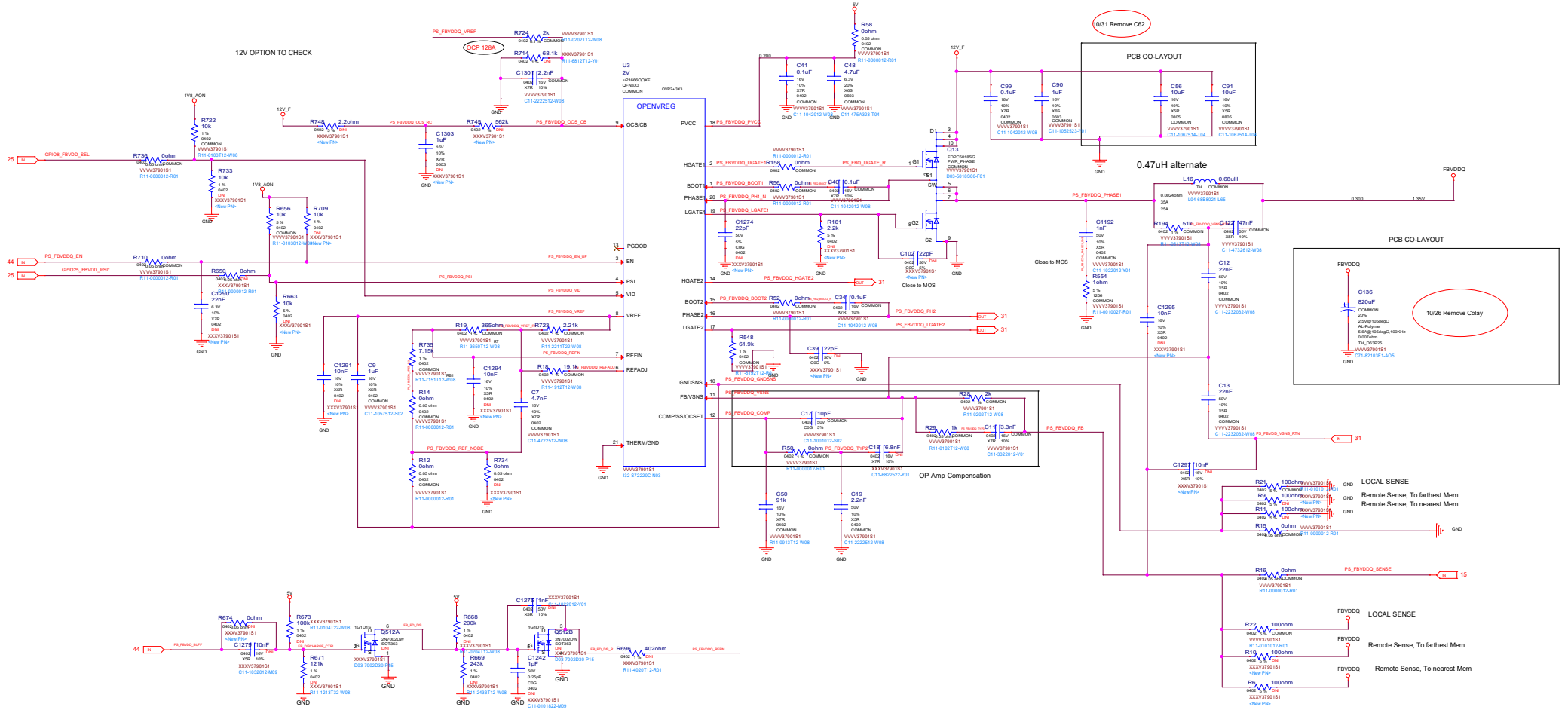

MICRO-STAR INT'L CO.,LTD			
MS-V379			
Size: Custom	Document Description: PS: FBVDDQ		Rev: 2.0
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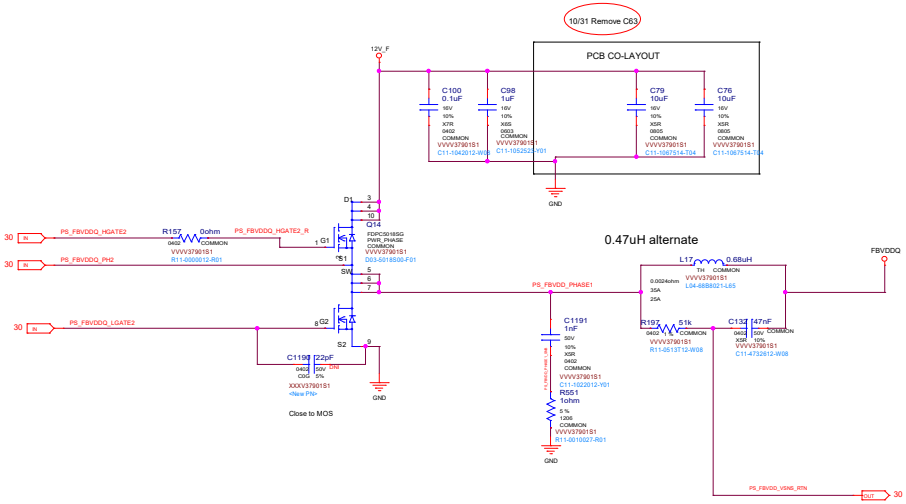

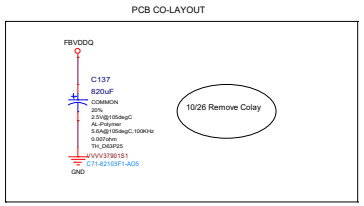

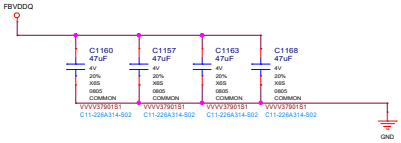

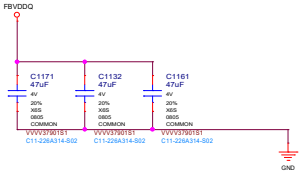

MSI	MICRO-STAR INT'L CO.,LTD	
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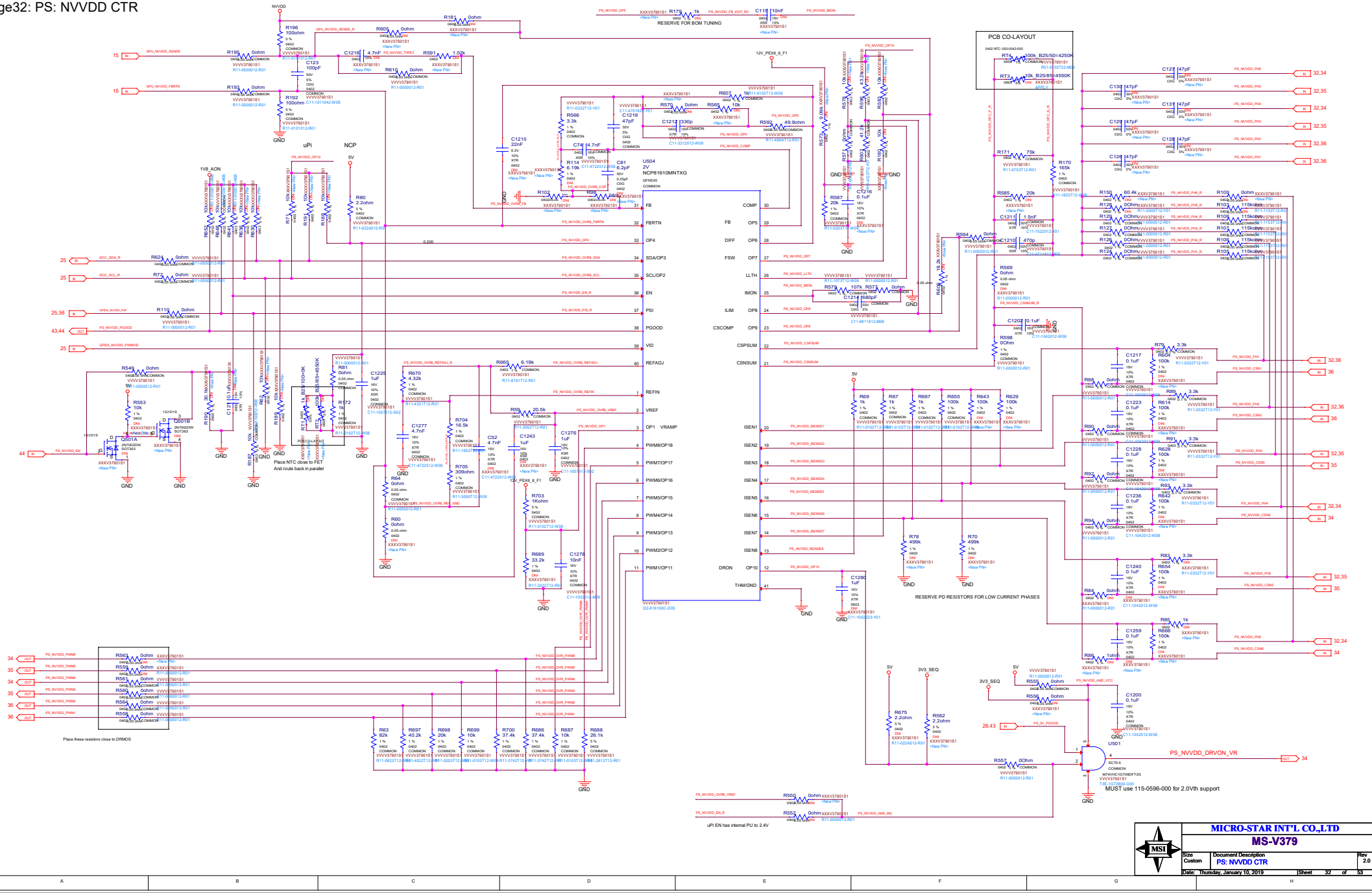
Page32: PS: NVVDD CTR



MICRO-STAR INT'L CO.,LTD	
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DROP OVR3i SOLUTION

19ci203

MSI	MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: PS: NVVDD CTR OVR3i	Rev: 2.0
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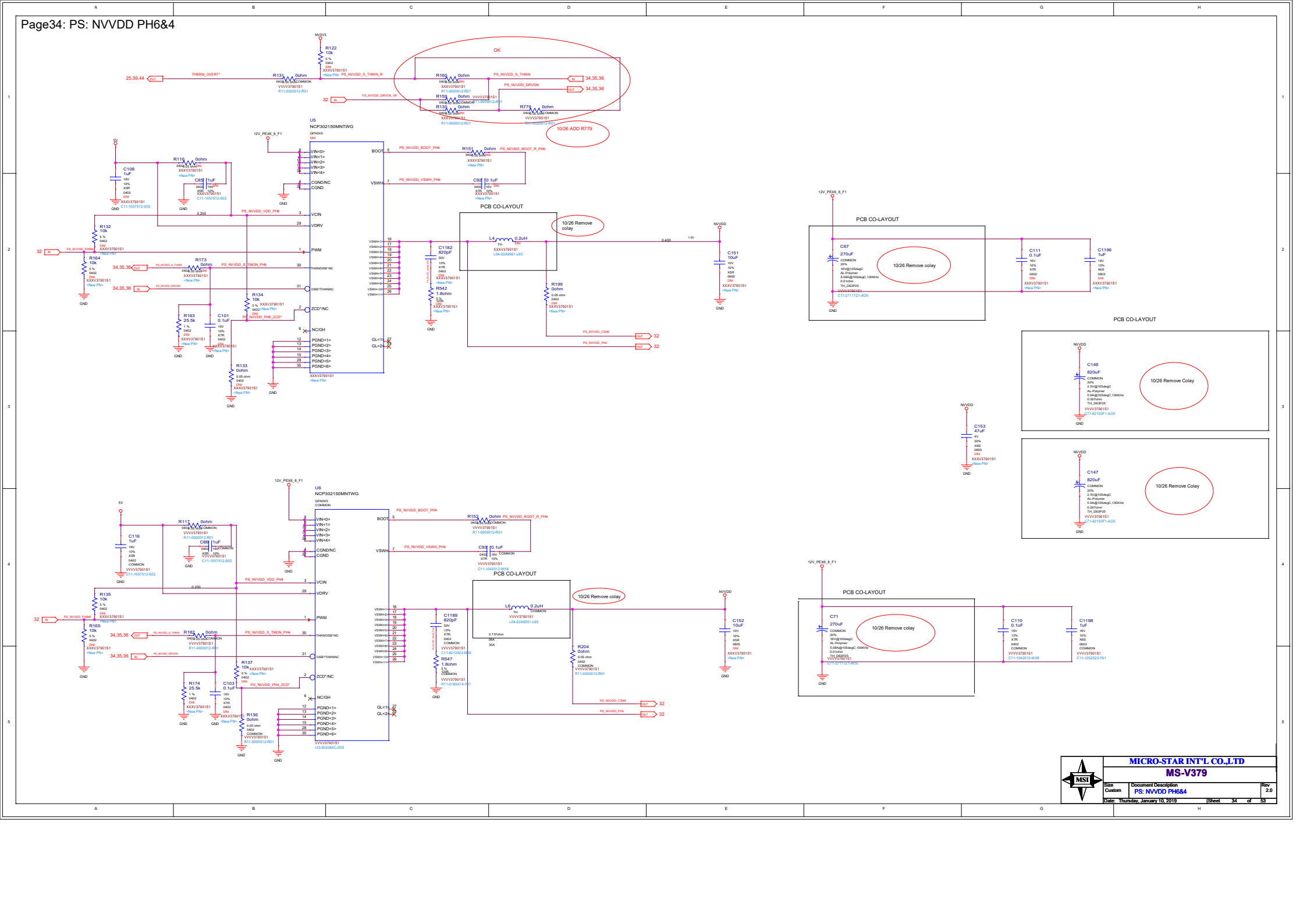
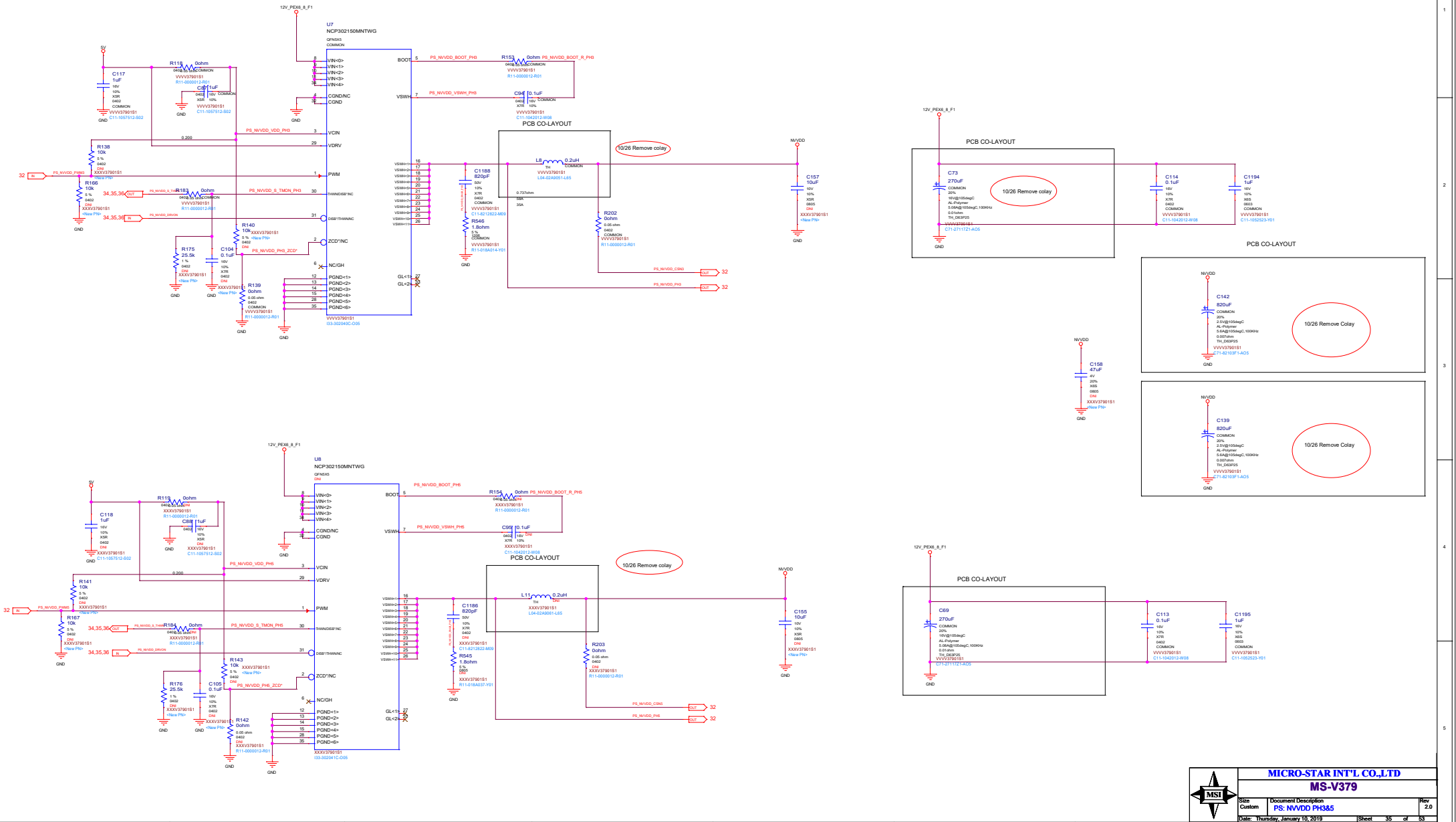
Page34: PS: NVVDD PH6&4




12V_PEX6_8_F1
U7
NCP302150MNTWG
QFNSX5
COMMON
PS_NVVDD_BOOT_PH3
PS_NVVDD_VSWH_PH3
PS_NVVDD_VDD_PH3
PS_NVVDD_PWM3
PS_NVVDD_S_TMON_PH3
PS_NVVDD_DRVON
PS_NVVDD_PH3_ZCD*
PCB CO-LAYOUT
10/26 Remove colay
L8
0.2uH
C157
10uF
NVVDD
U8
NCP302150MNTWG
PS_NVVDD_BOOT_PH5
PS_NVVDD_VSWH_PH5
PS_NVVDD_VDD_PH5
PS_NVVDD_PWM5
PS_NVVDD_S_TMON_PH5
PS_NVVDD_DRVON
PS_NVVDD_PH5_ZCD*
L11
0.2uH
C155
10uF
C73
270uF
C114
0.1uF
C1194
1uF
C142
820uF
C158
47uF
C139
820uF
C69
270uF
C113
0.1uF
C1195
1uF
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MS-V379
Size
Custom
Document Description
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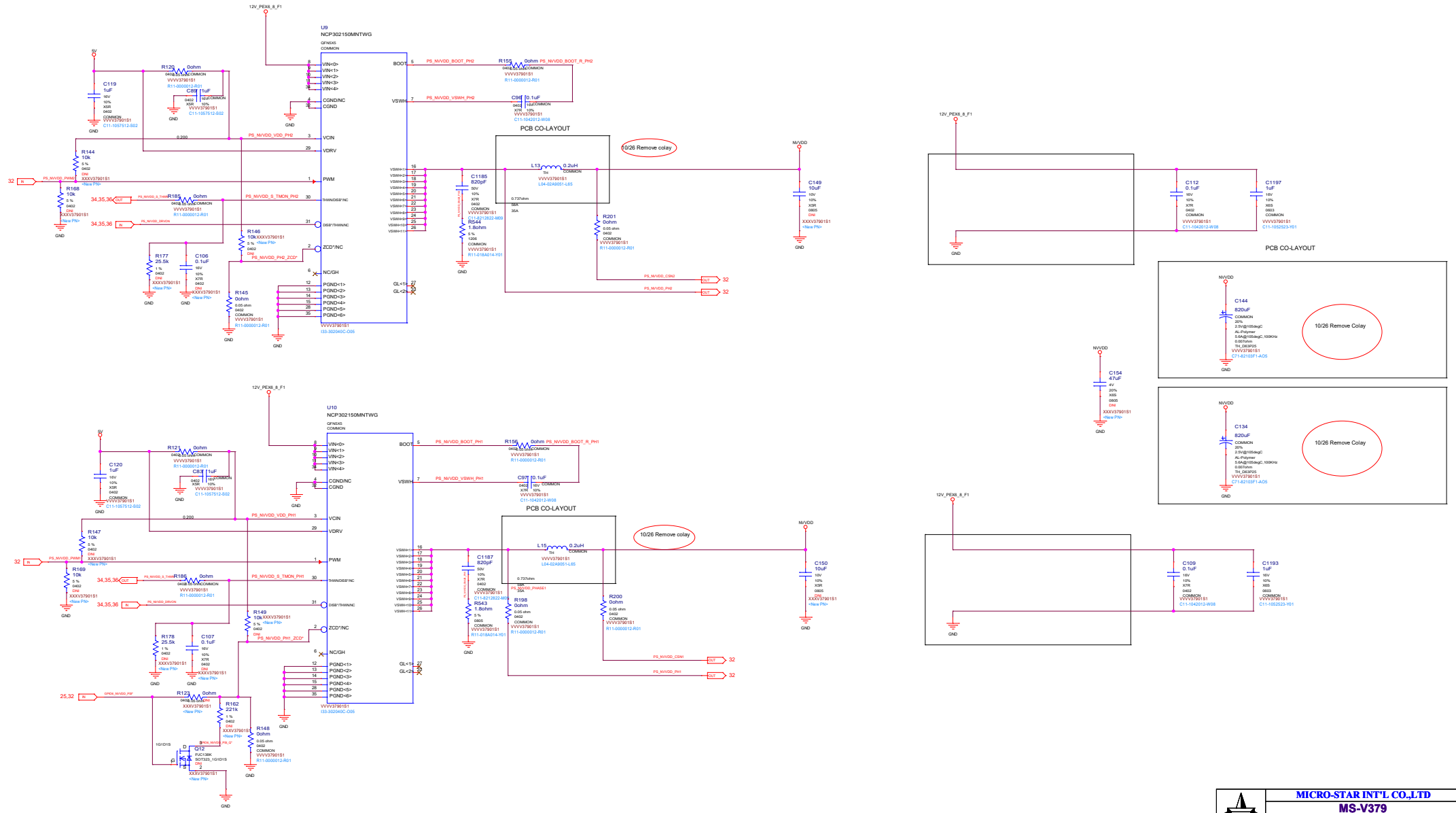
Page36: PS: NVVDD PH2&1



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MS-V379	
Size: Custom	Document Description: NVVDD PH2&1
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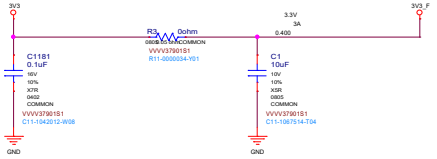
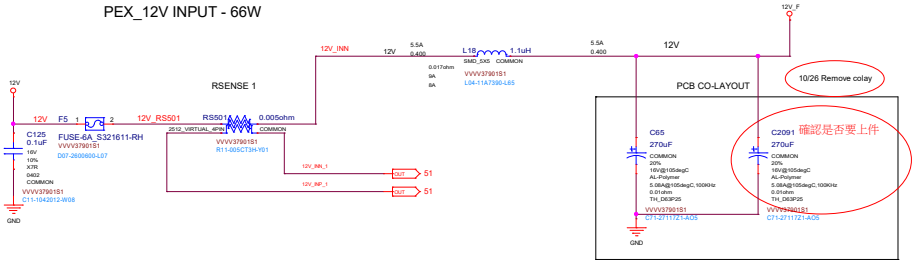
DELETE RAIL BALANCE CIRCUIT

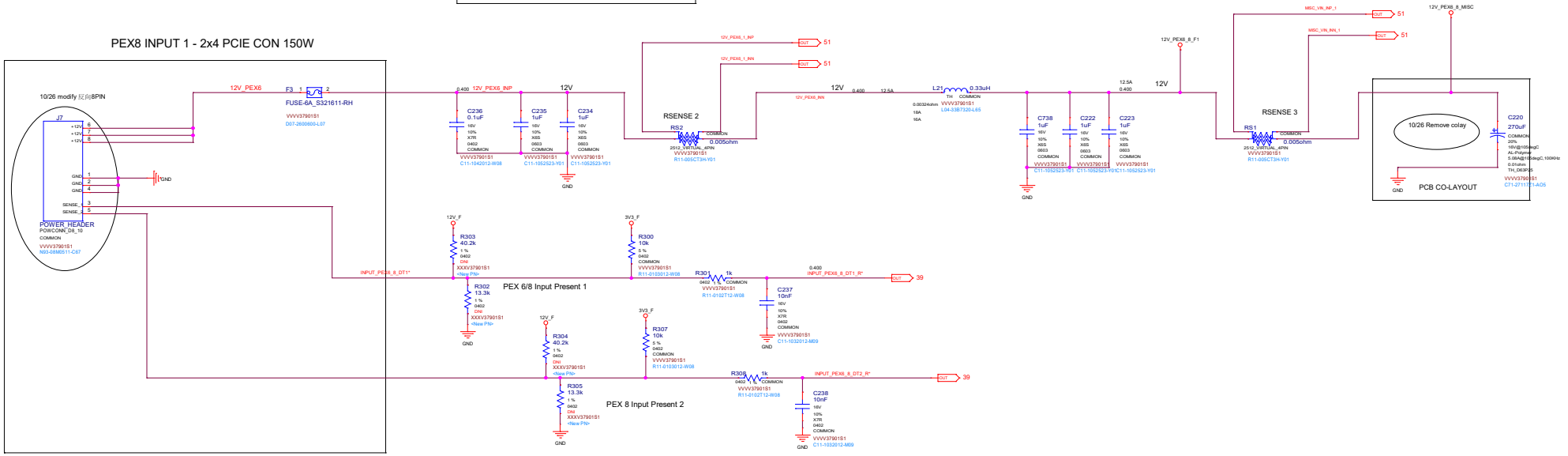
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX8 INPUT 1 - 2x4 PCIE CON 150W



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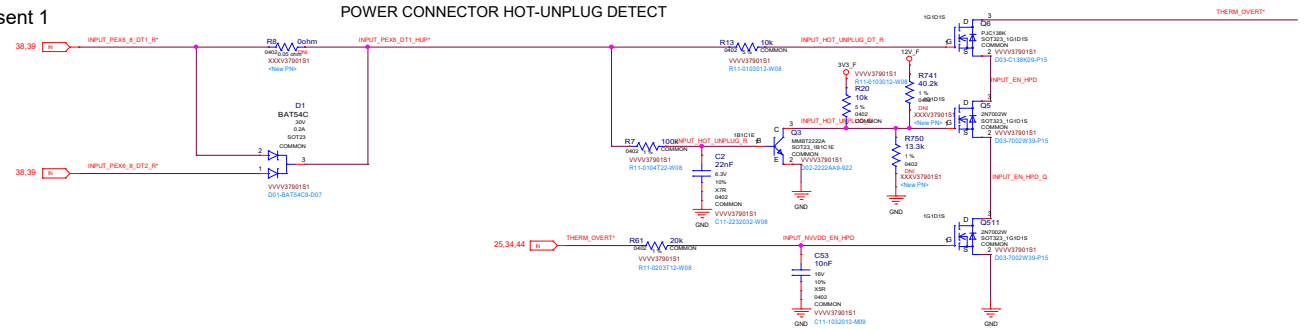
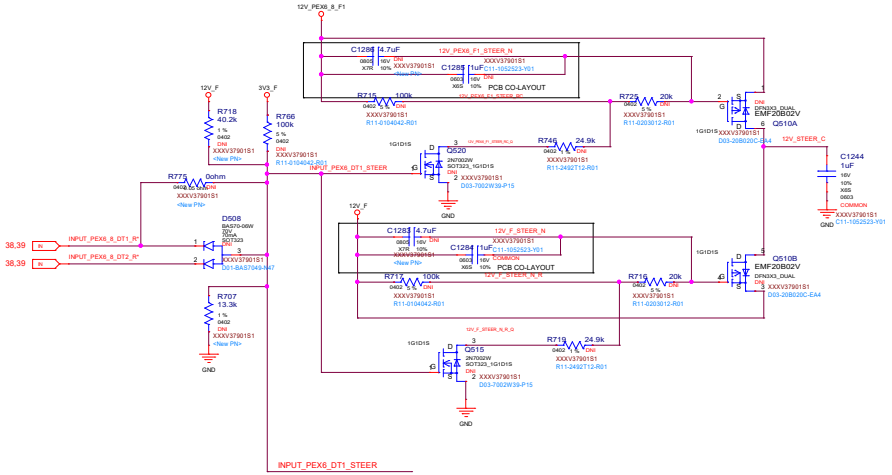
PEX Input Present 1

POWER CONNECTOR HOT-UNPLUG DETECT

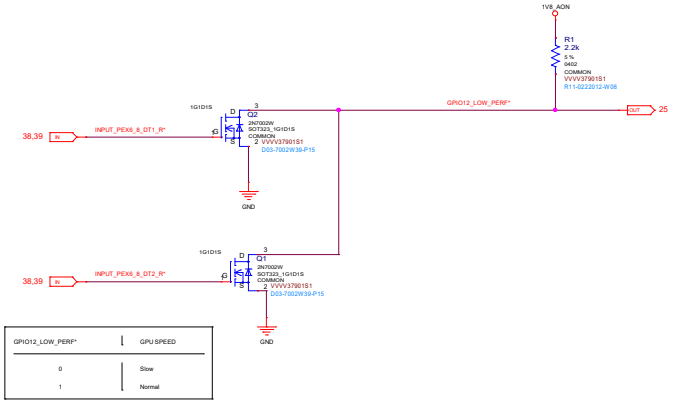


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



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Page40: BUCKBOOST

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Page41: PPC

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Page42: 12V & 3V3_A SWITCHER

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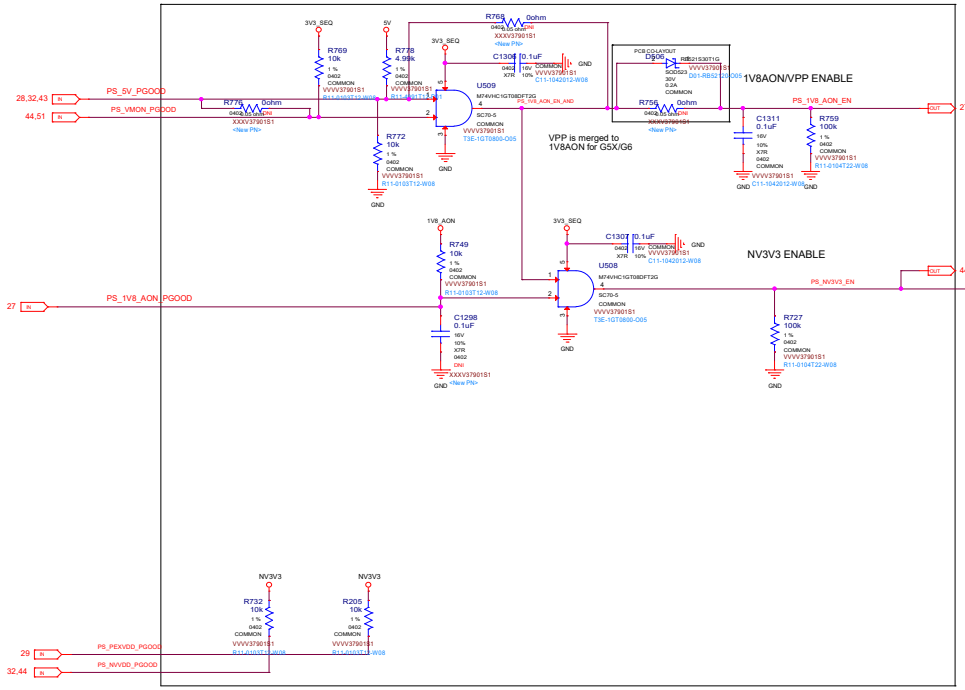
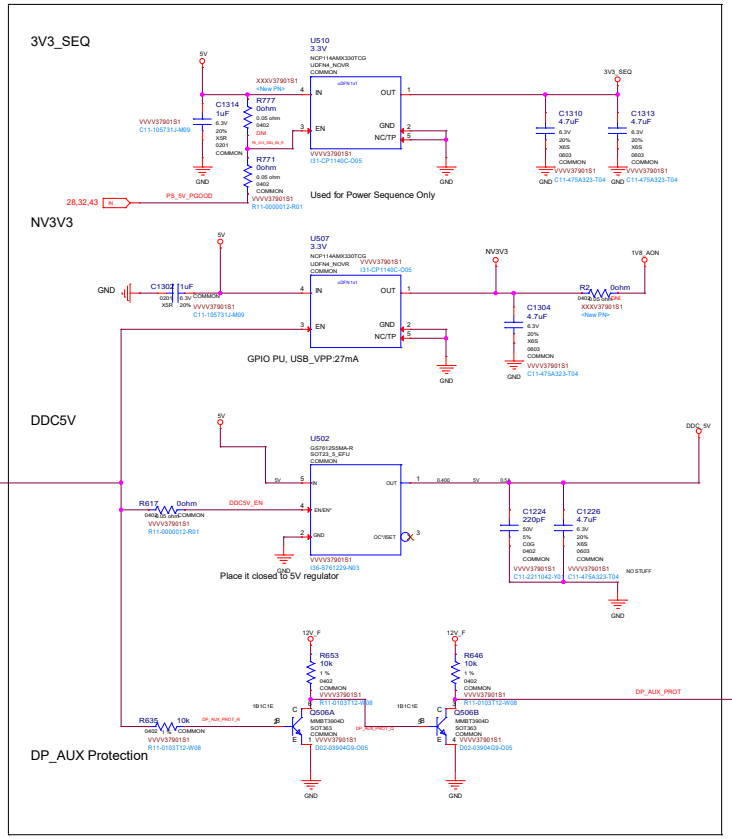
Page43: SEQ:5V,1V8,NV3V3 ENABLE





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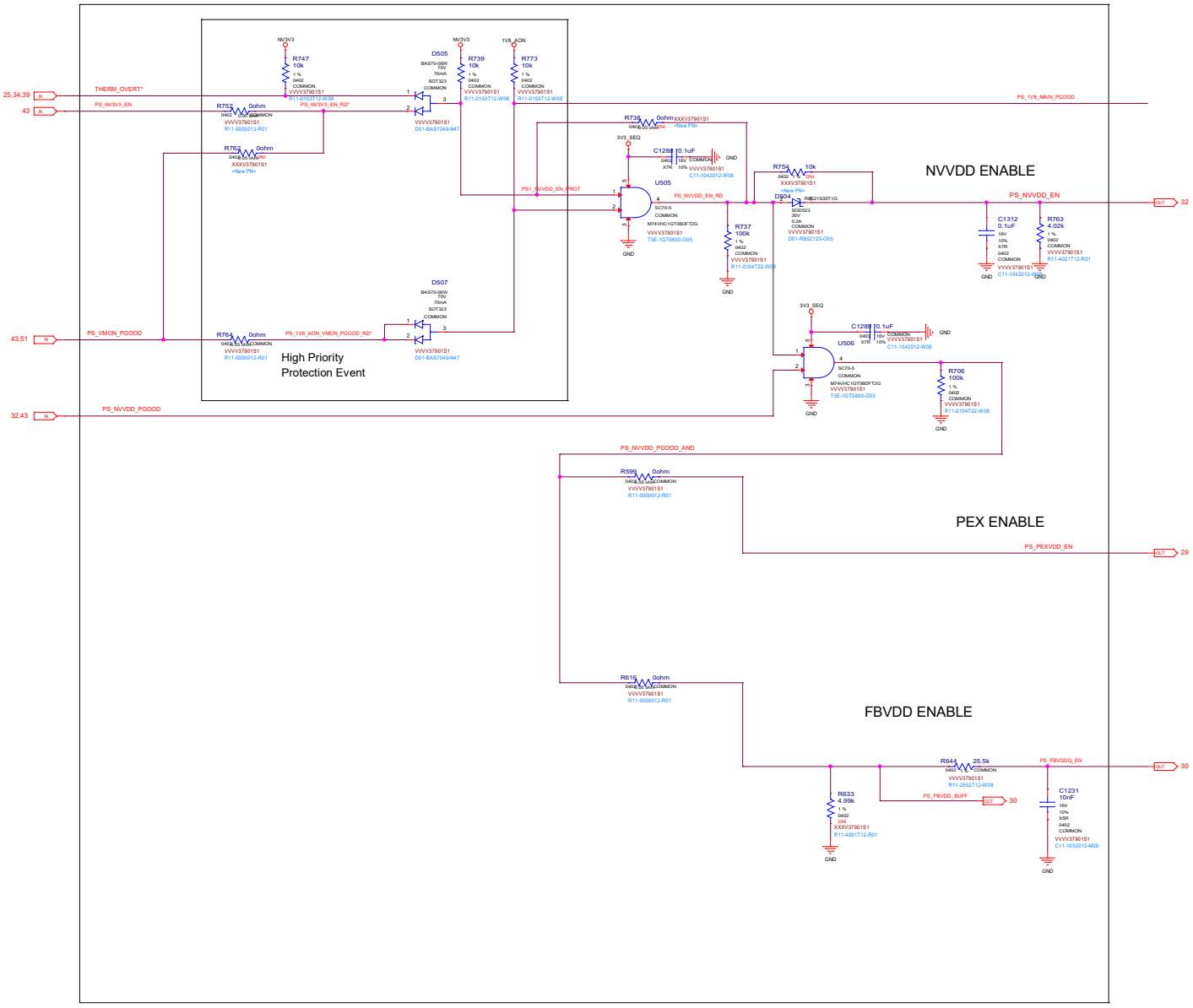
Page44: SEQ:NV,PEX,FB ENABLE



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Size: Custom	Document Description: SEQ:NV,PEX,FB ENABLE
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Page45: SEQUENCE:Voltage Monitor

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Page46: SEQUENCE:Discharge

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PEX_CLKREQ*

PU ON GPU SIDE

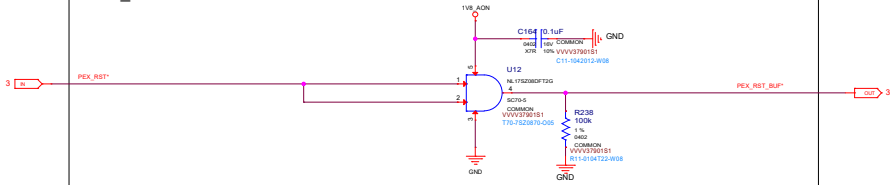
NC ON GOLD FINGER SIDE

GPU_WAKE*

PU ON GPU SIDE

NC ON GOLD FINGER SIDE

PEX_RST# LOGIC



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Page48: LOGO LED

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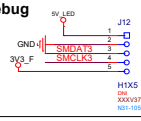
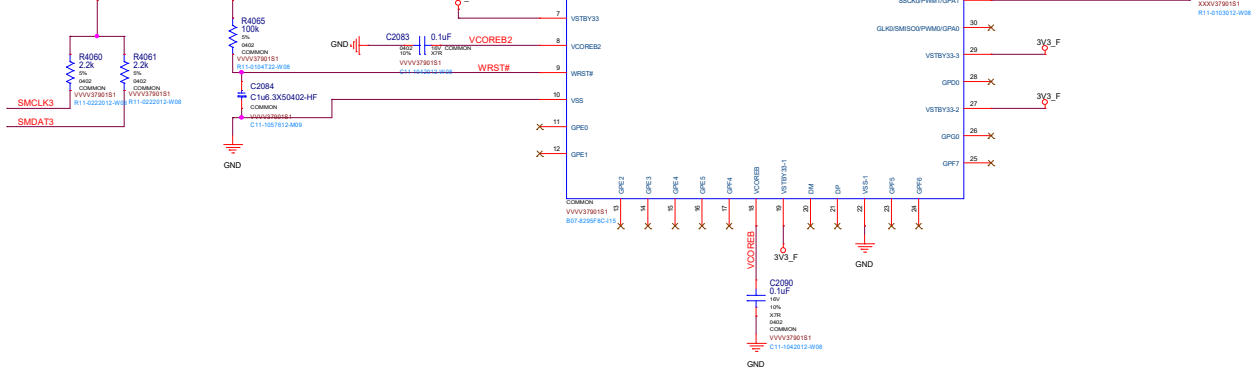
Page49: LED DRIVER & Boost

Firmware Programming

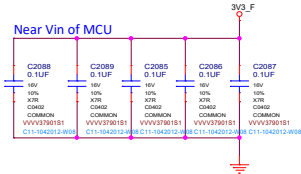
Debug



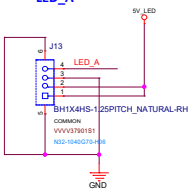
ADD LED



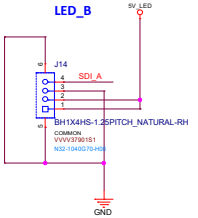
Near Vin of MCU



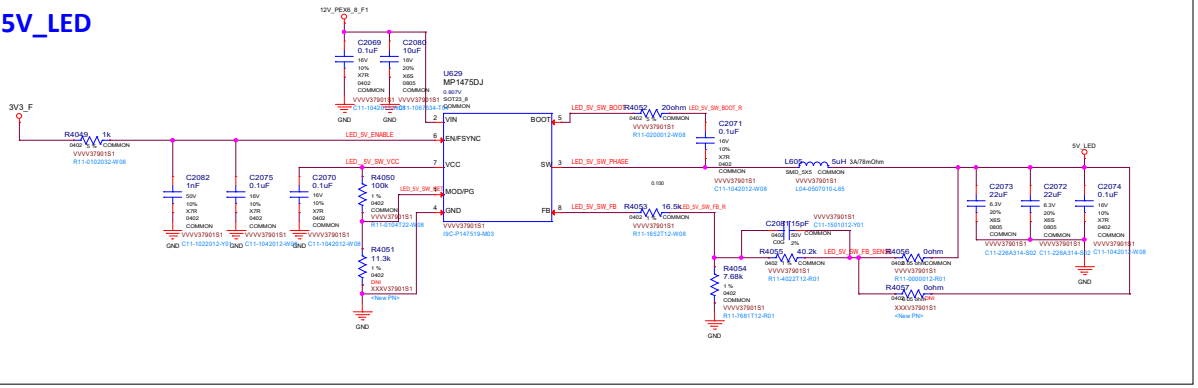
LED_A



LED_B



5V_LED



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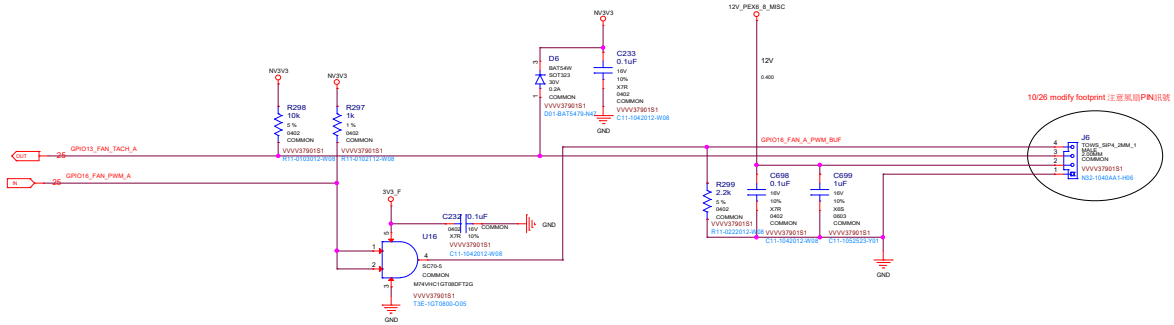
Page50: FAN



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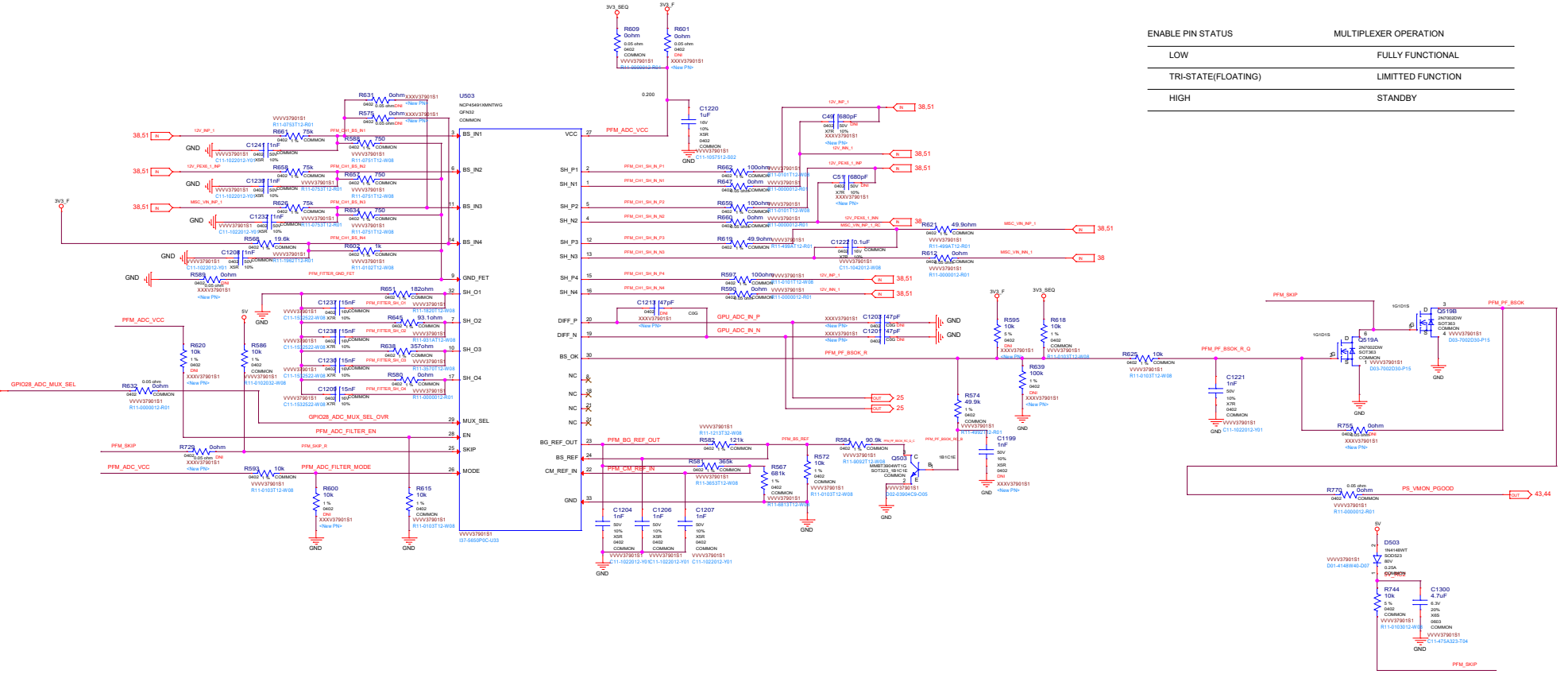
Page51: PWR SENSE

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY



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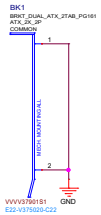
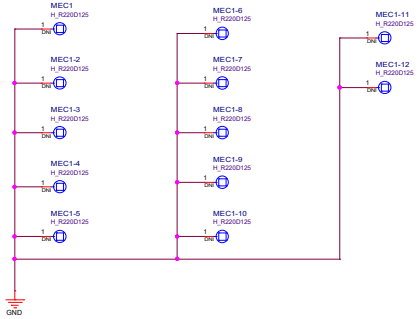
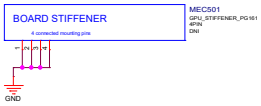
Bracket:



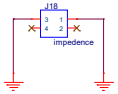
MOUNTING HOLES FOR HS:

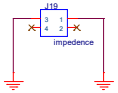


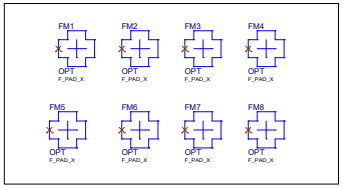
BACK STIFFENER:



Screw







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Page53: PTC

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