

PG161-A00

TU106 6GB GDDR6, 192b, X16
DVI-D/DP + DP + HDMI

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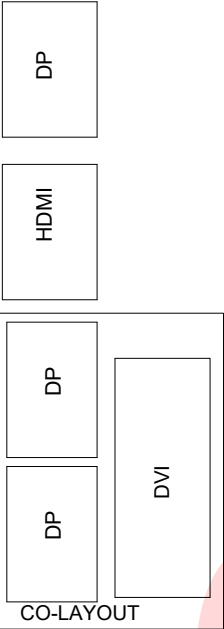
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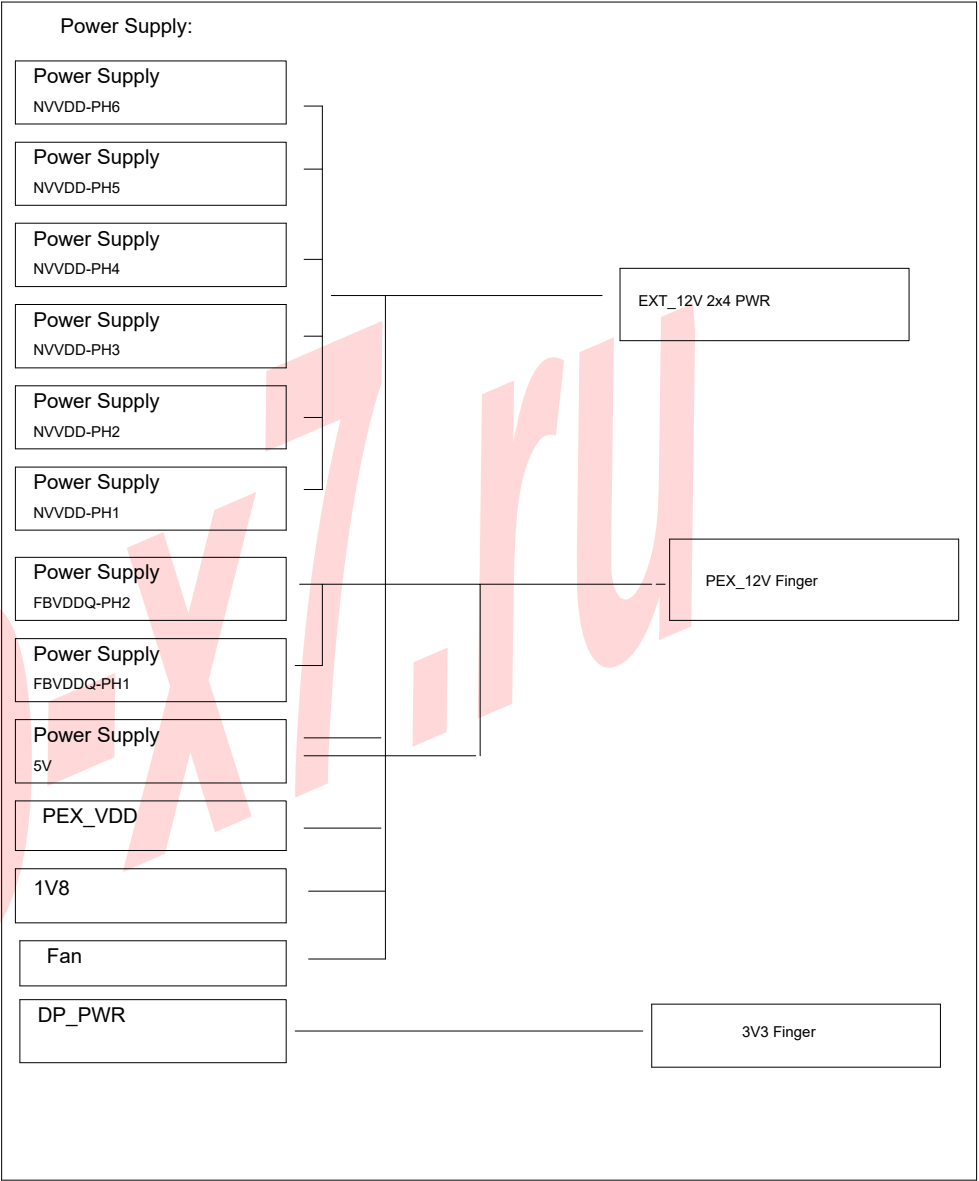
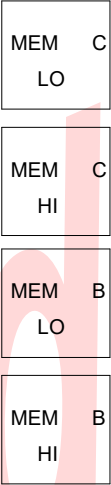
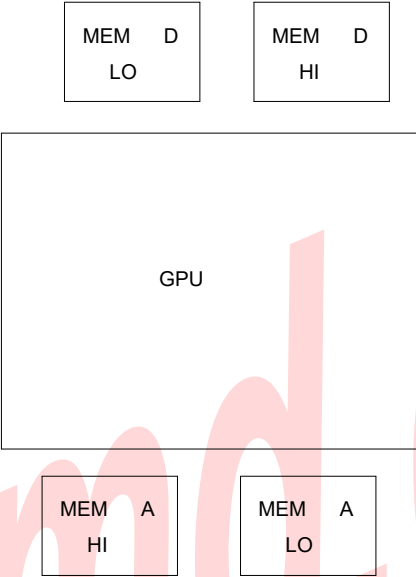
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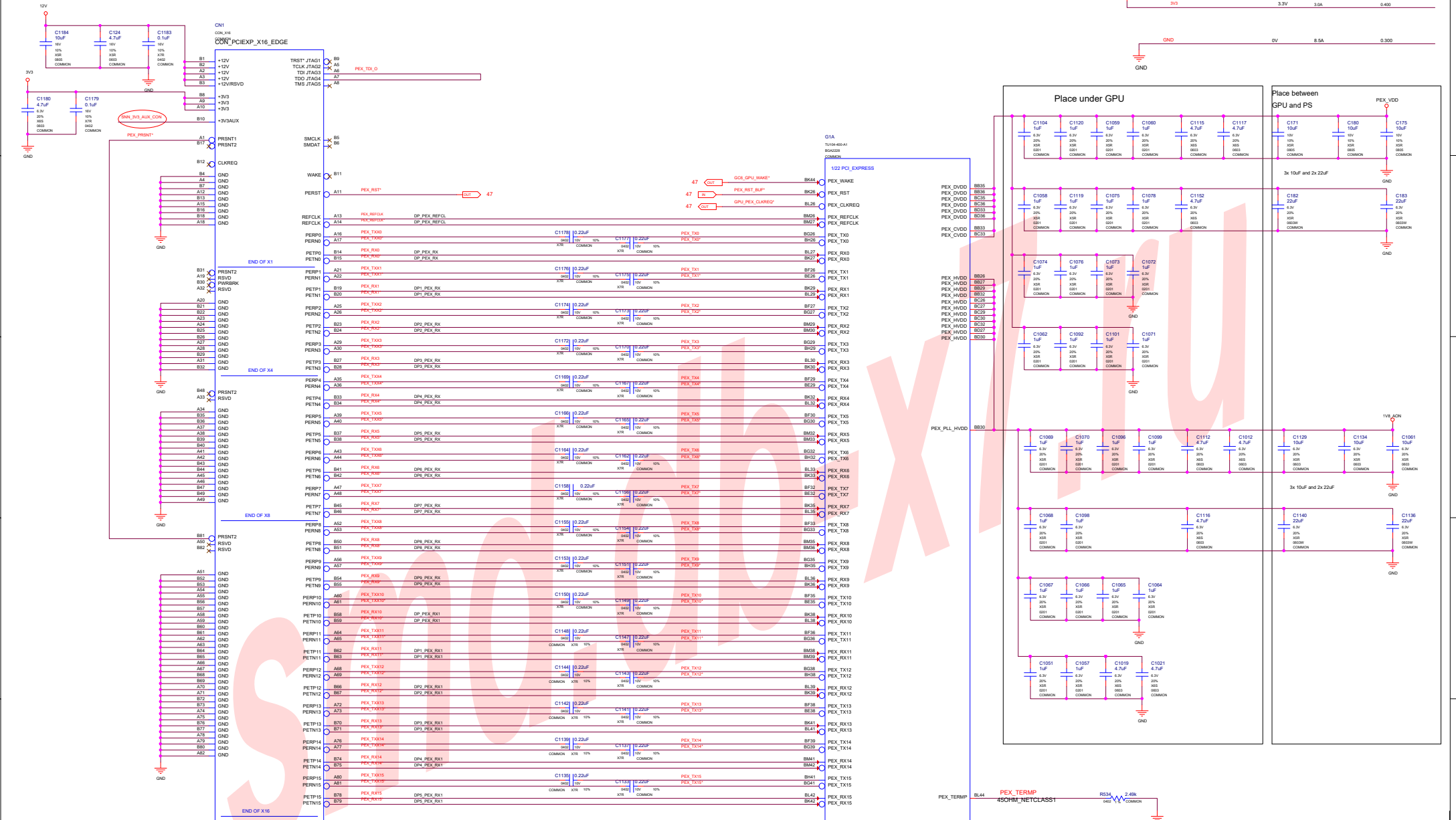
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POWER SUPPLY

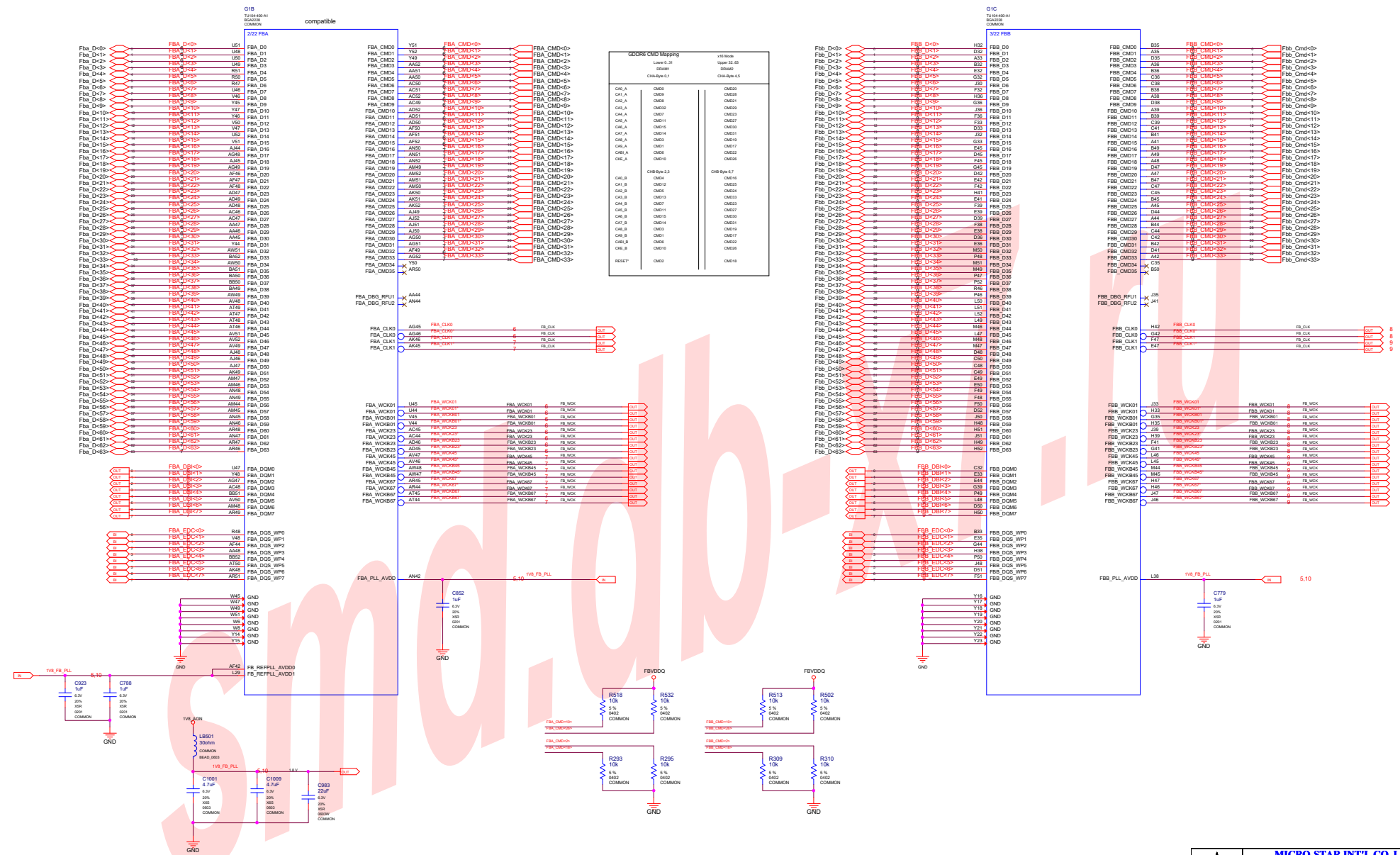


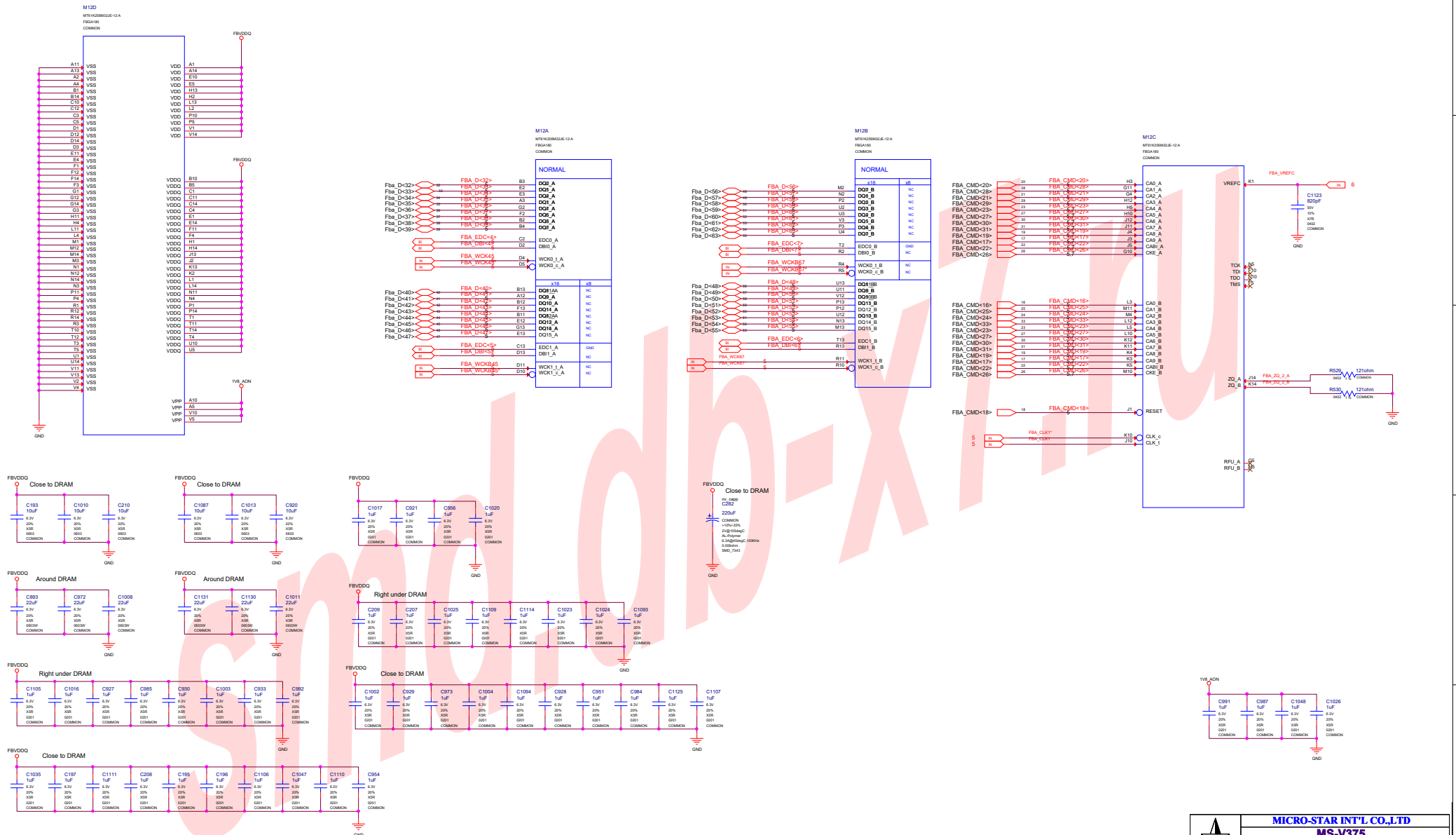


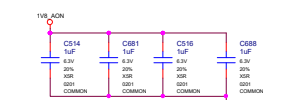
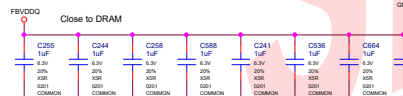
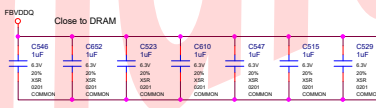
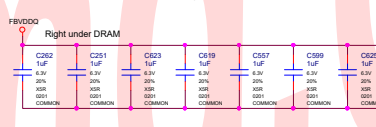
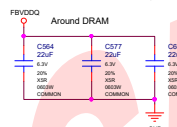
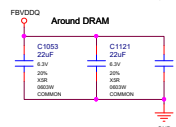
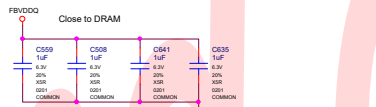
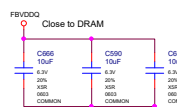
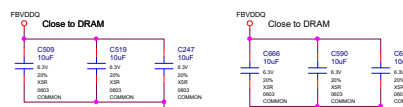
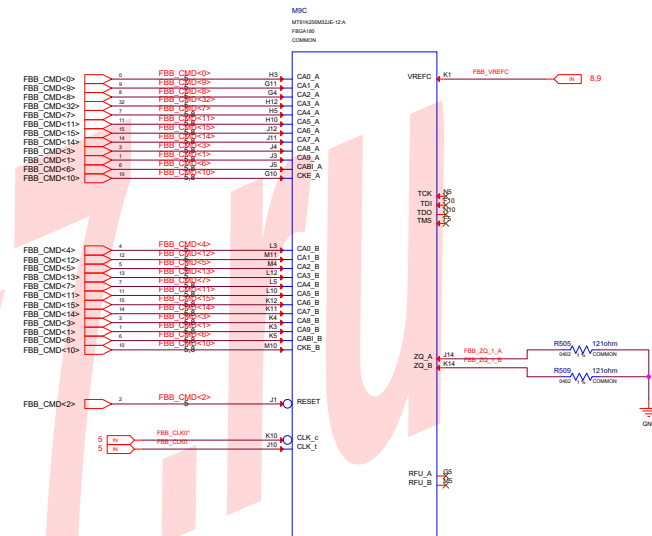
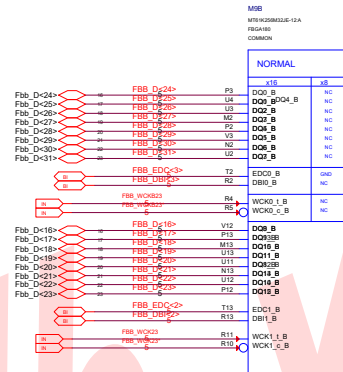
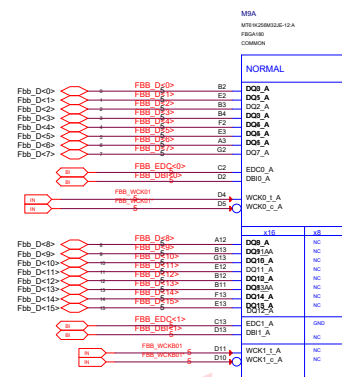
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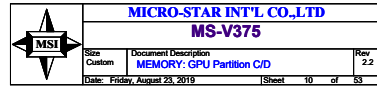
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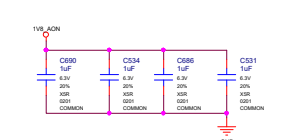
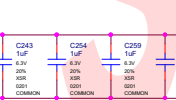
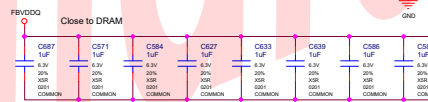
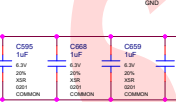
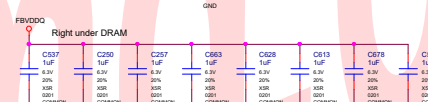
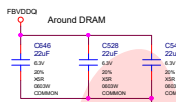
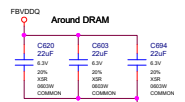
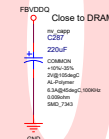
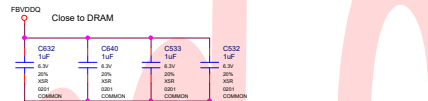
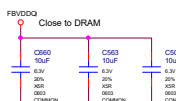
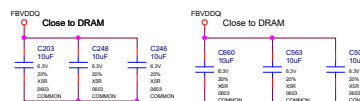
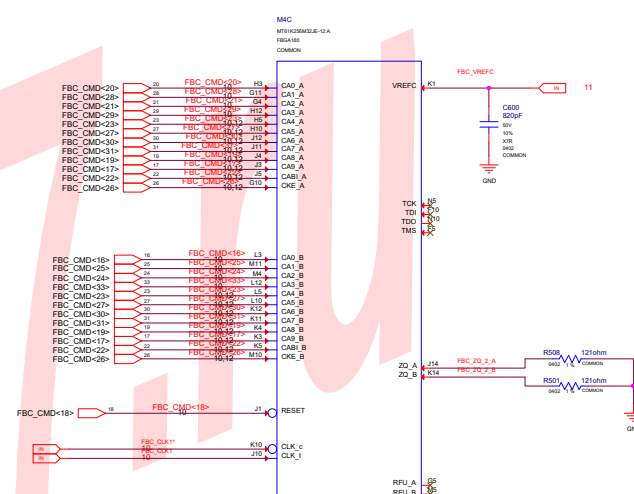
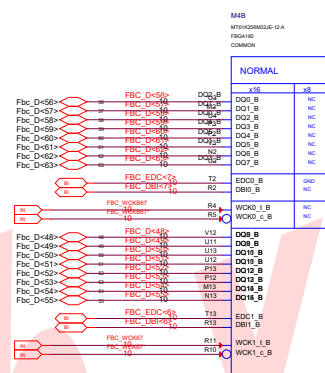
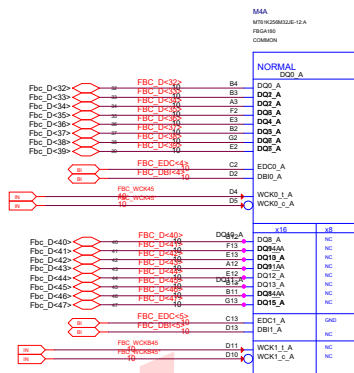
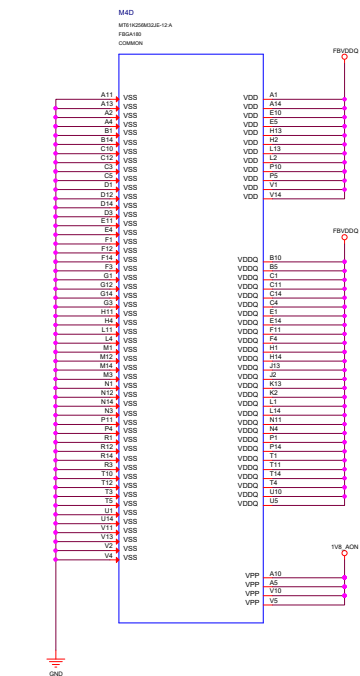
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	MS-V375		
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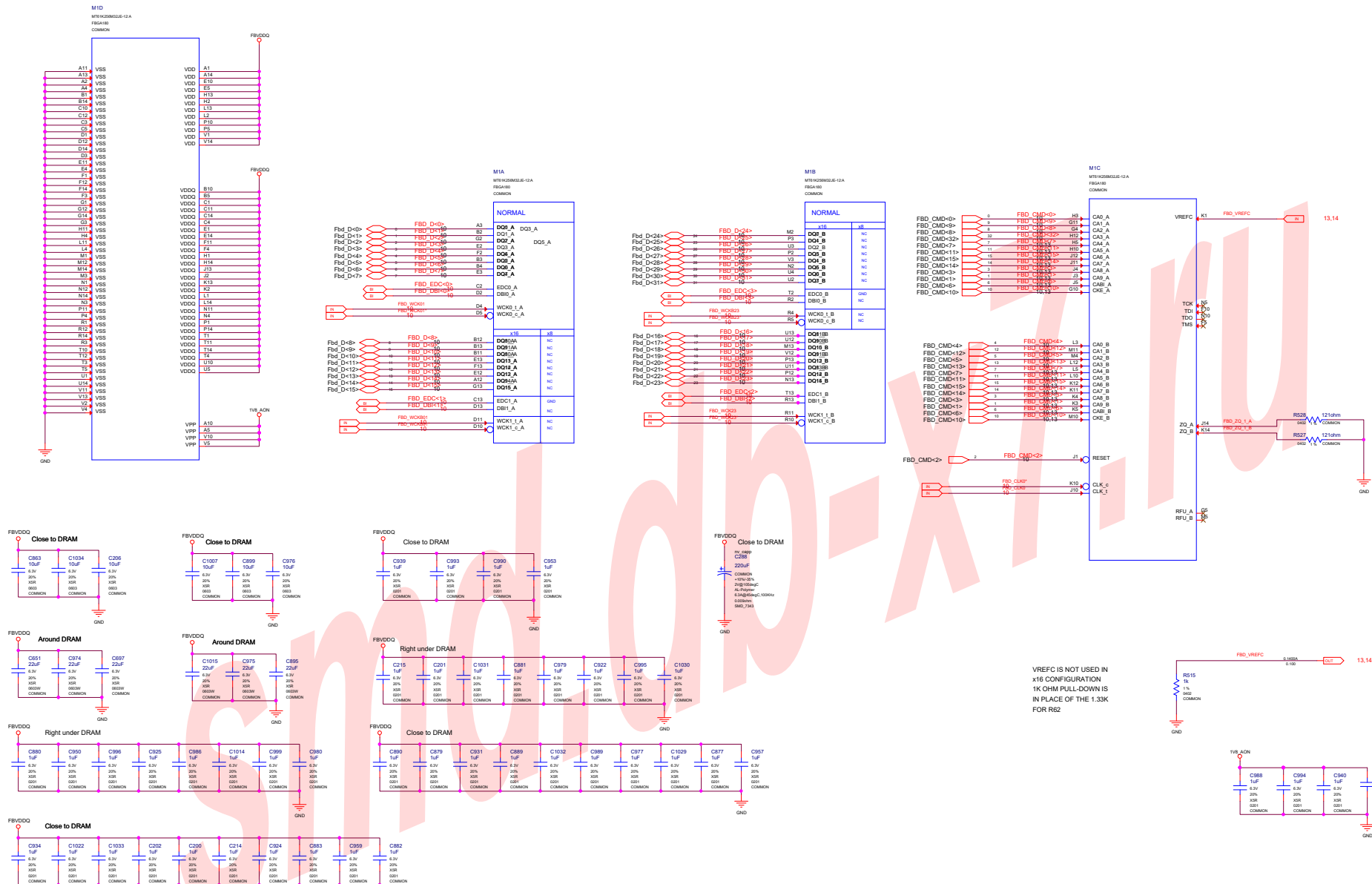


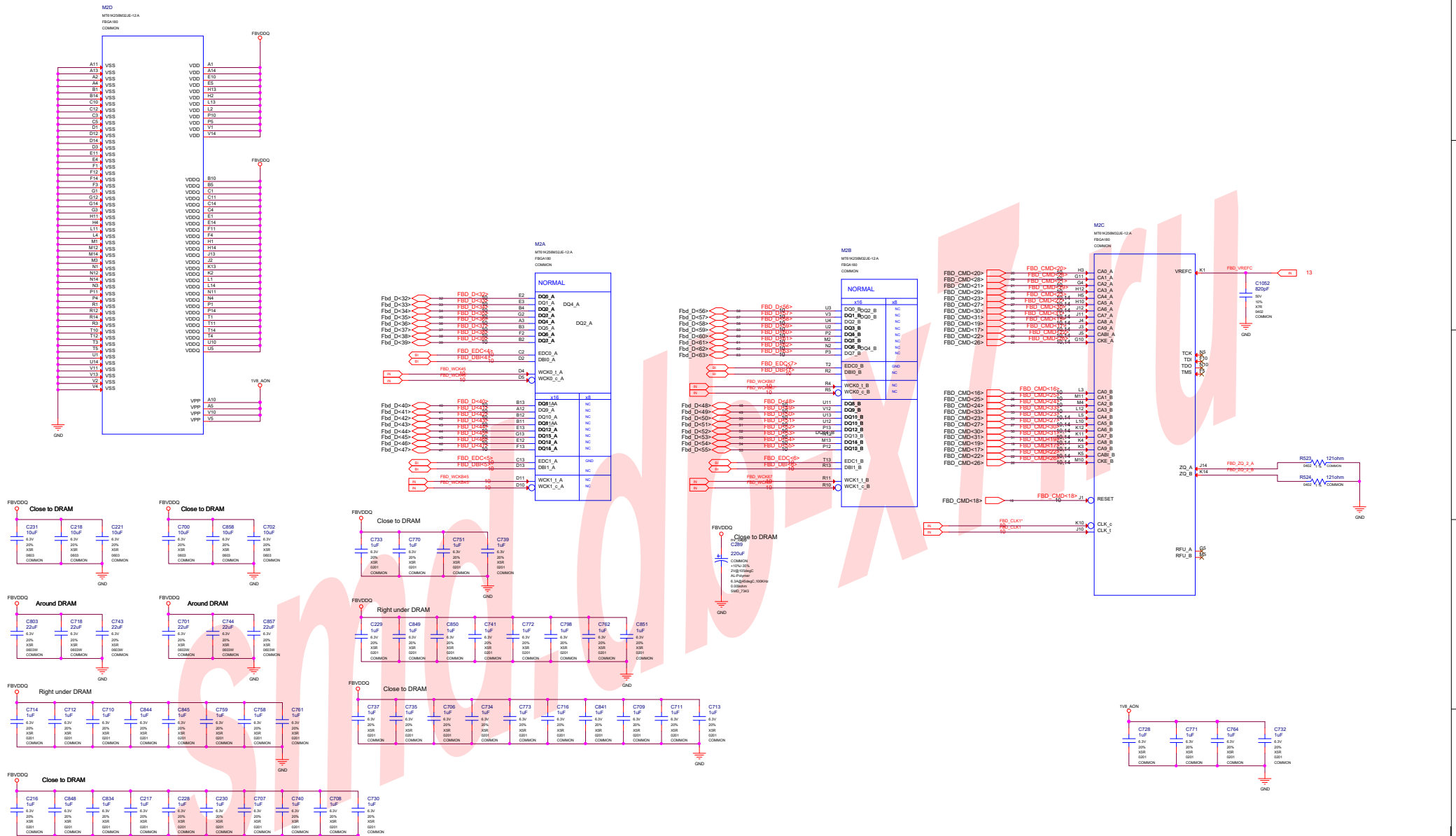




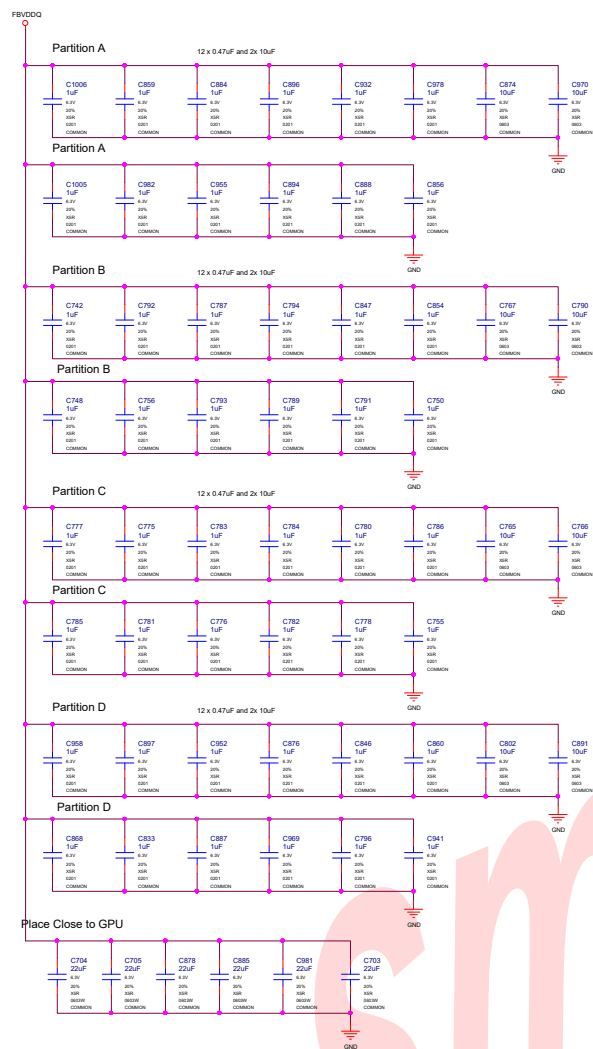




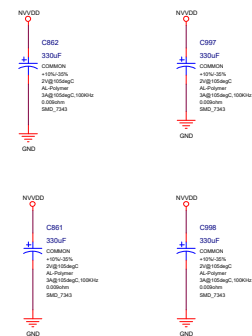




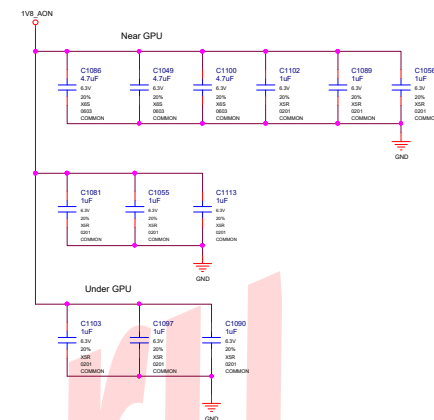
FBVDDQ



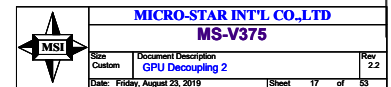
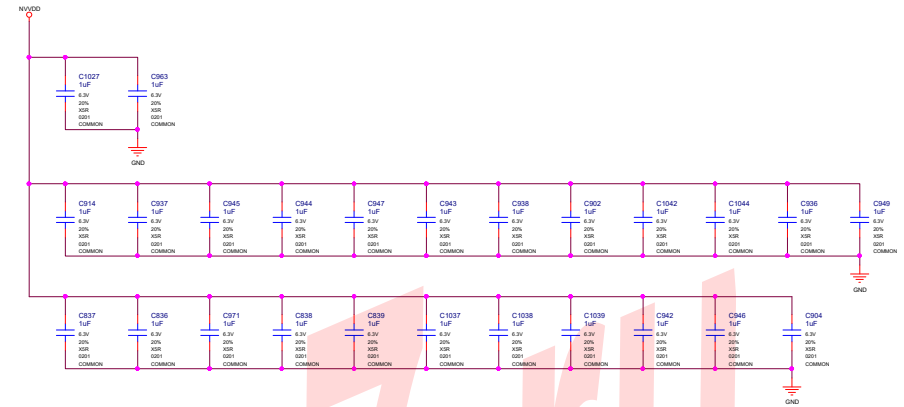
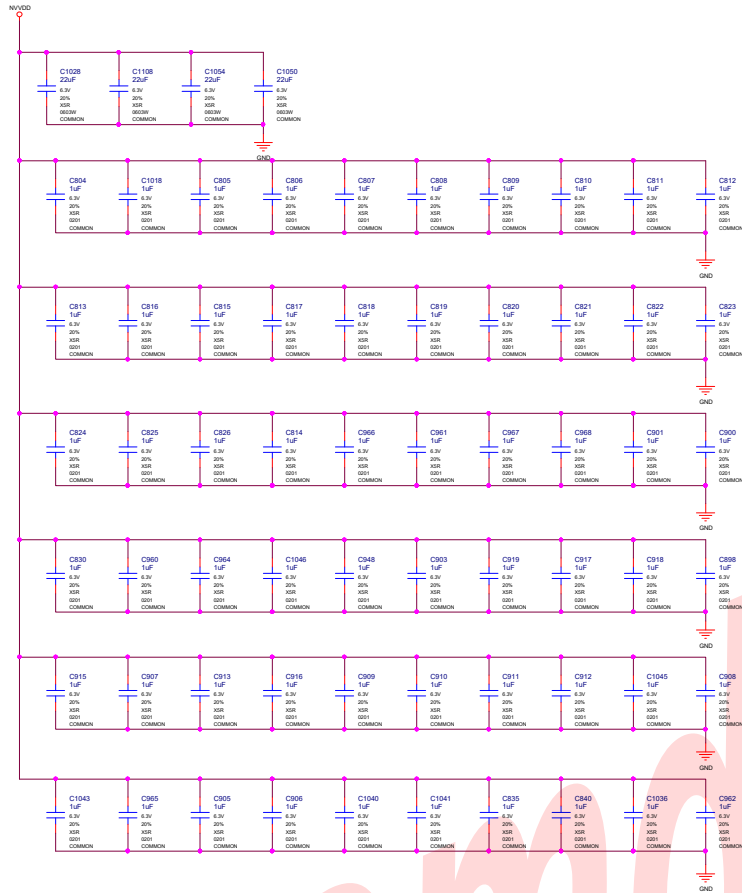
NVVDD



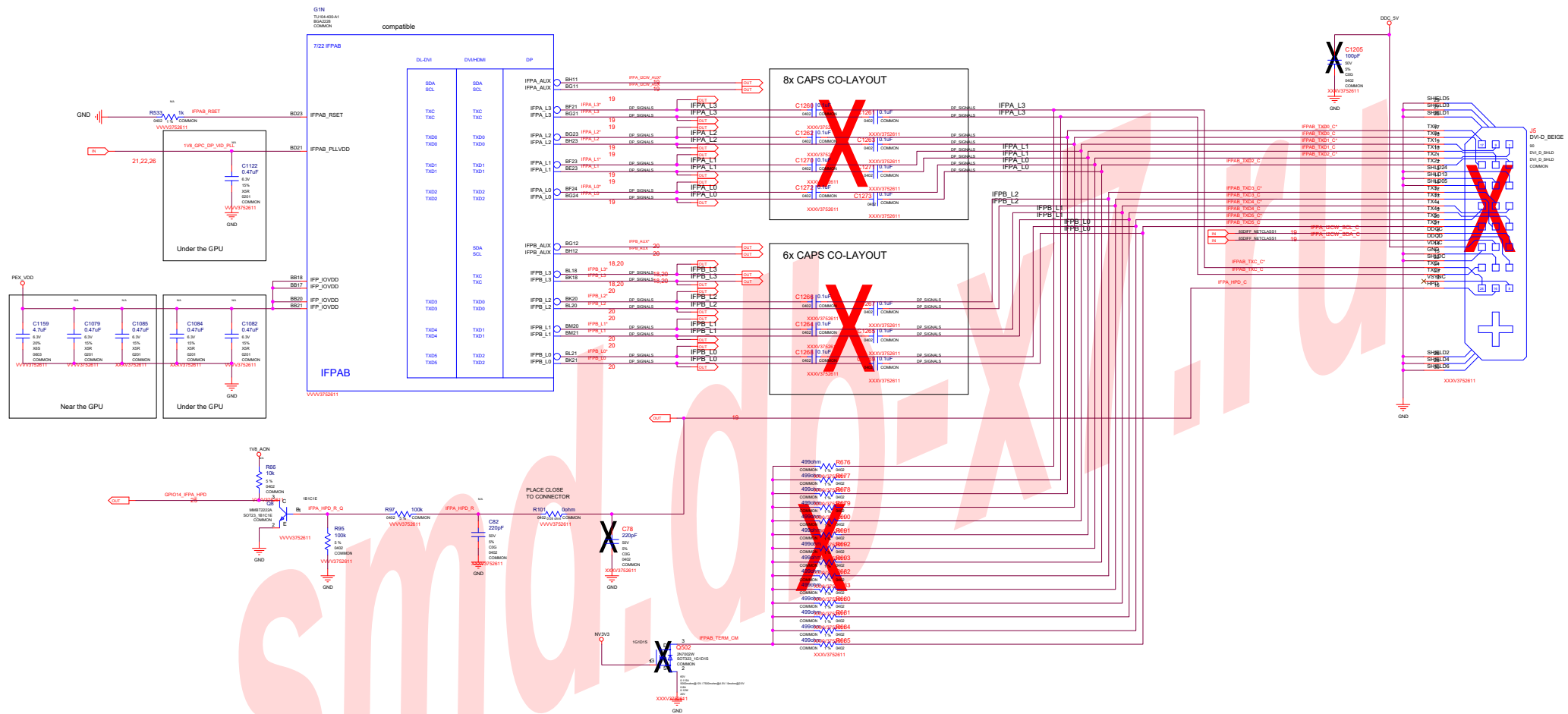
1V8_AON



NVVDD



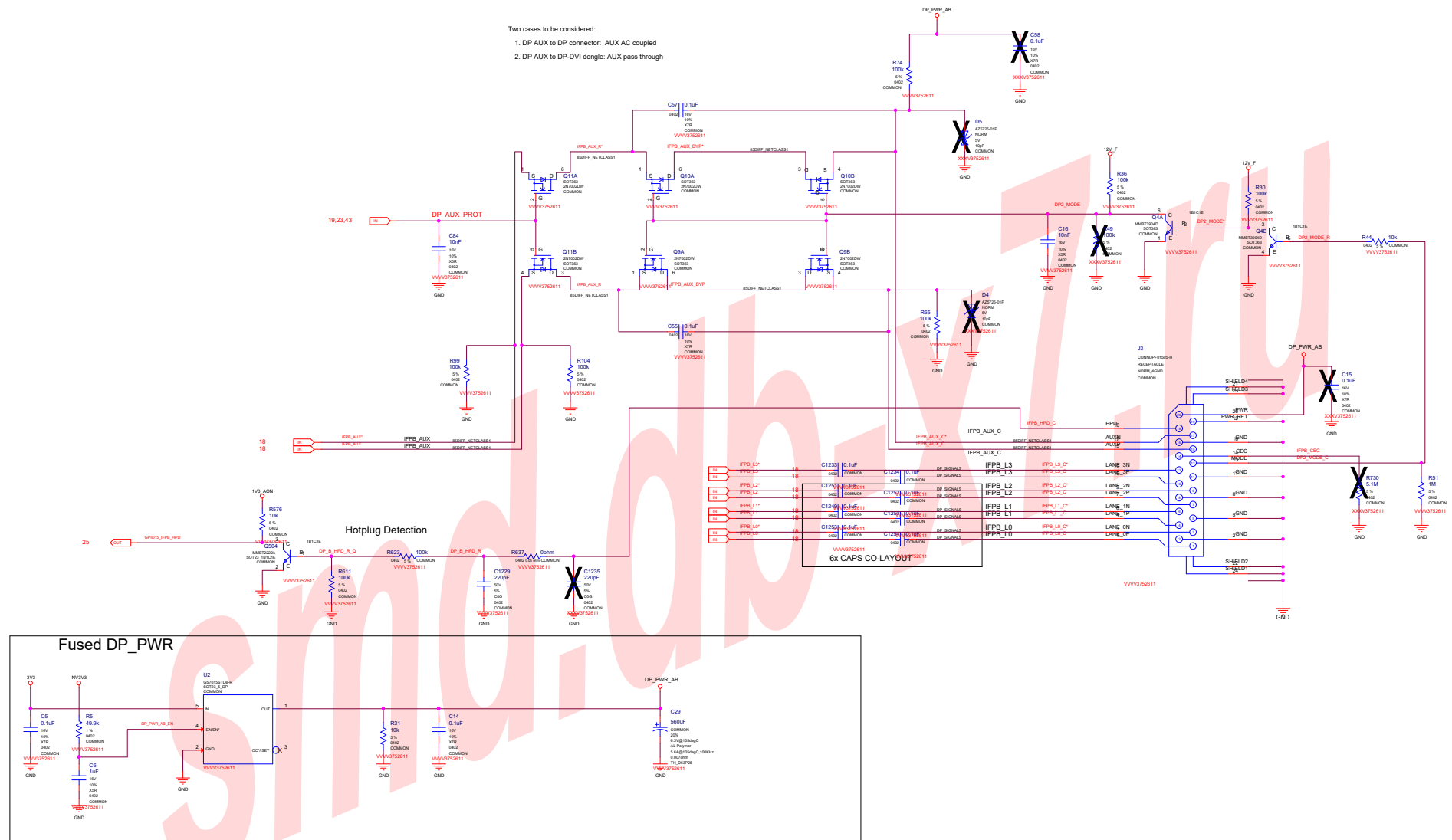
IFPAB DVI-D-DL CO-LAYOUT WITH 2x DP



IFPB DP CO-LAYOUT WITH IFPAB DVI-D-DL

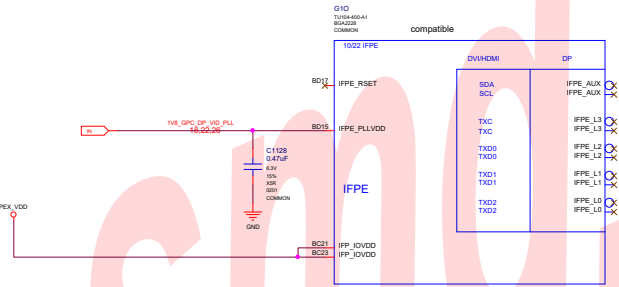
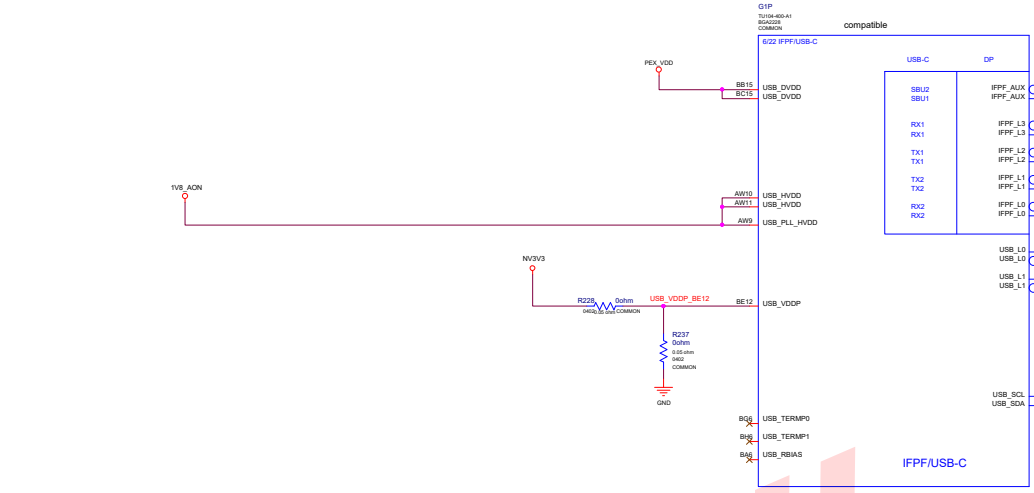
Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



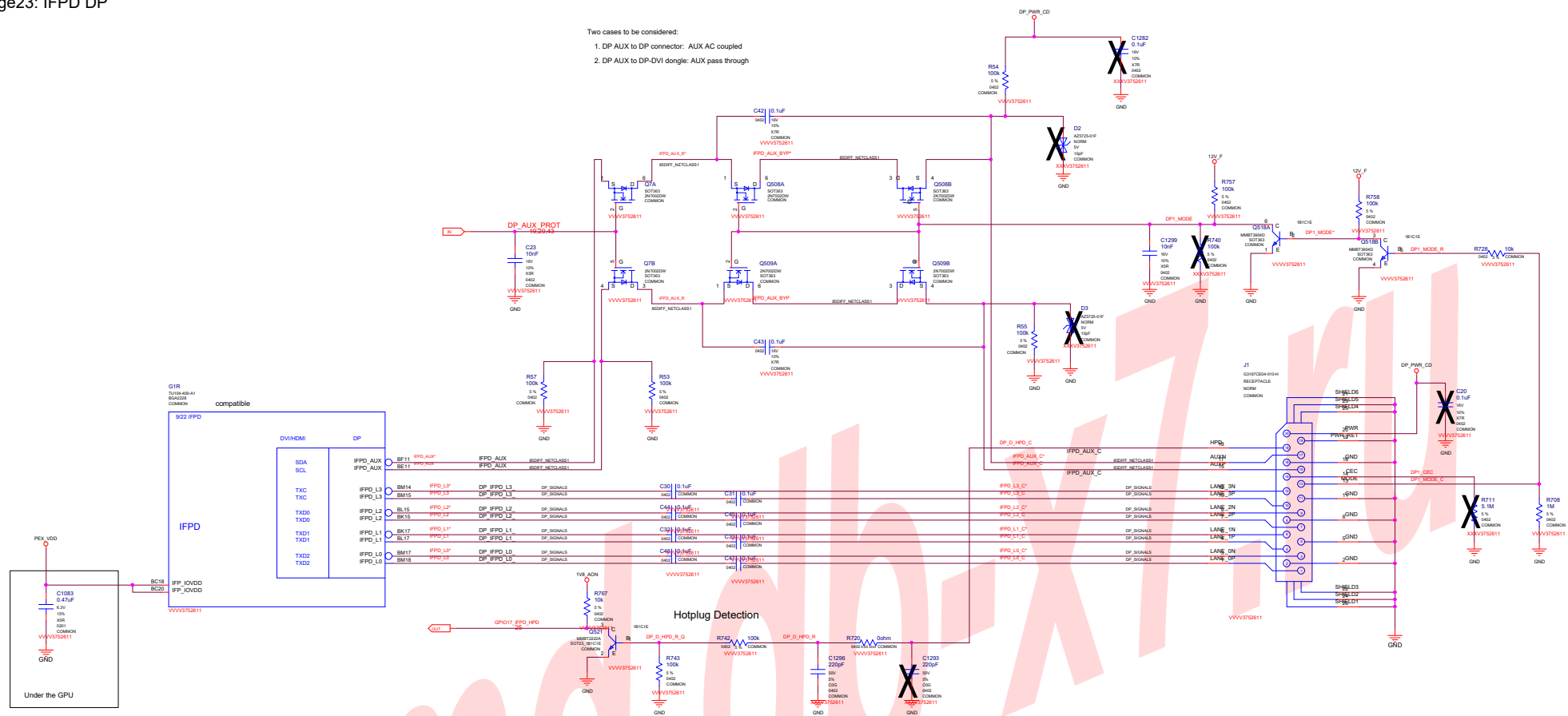
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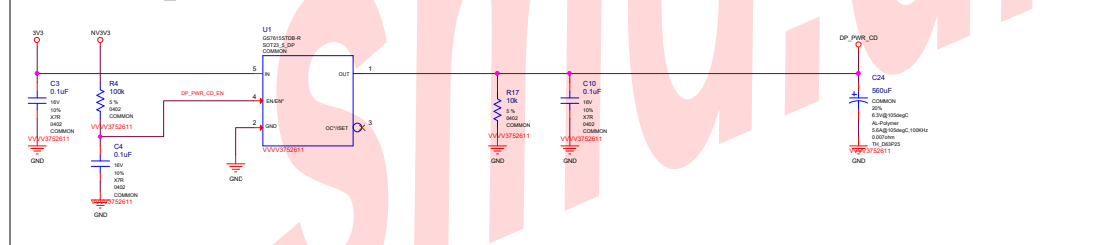


Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

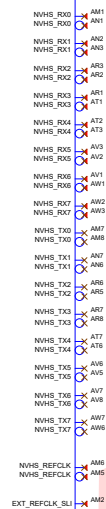


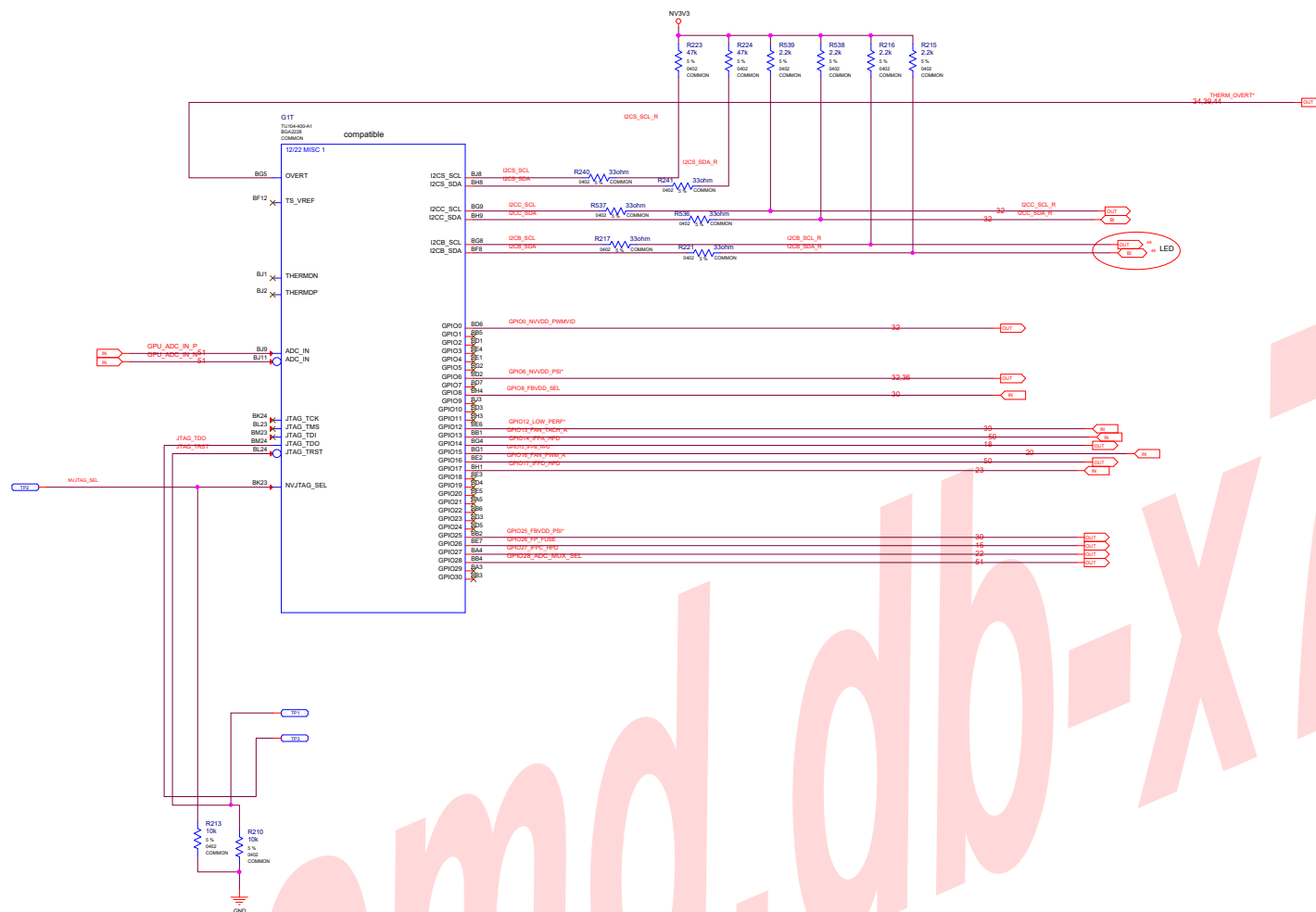
Fused DP_PWR



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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0].FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

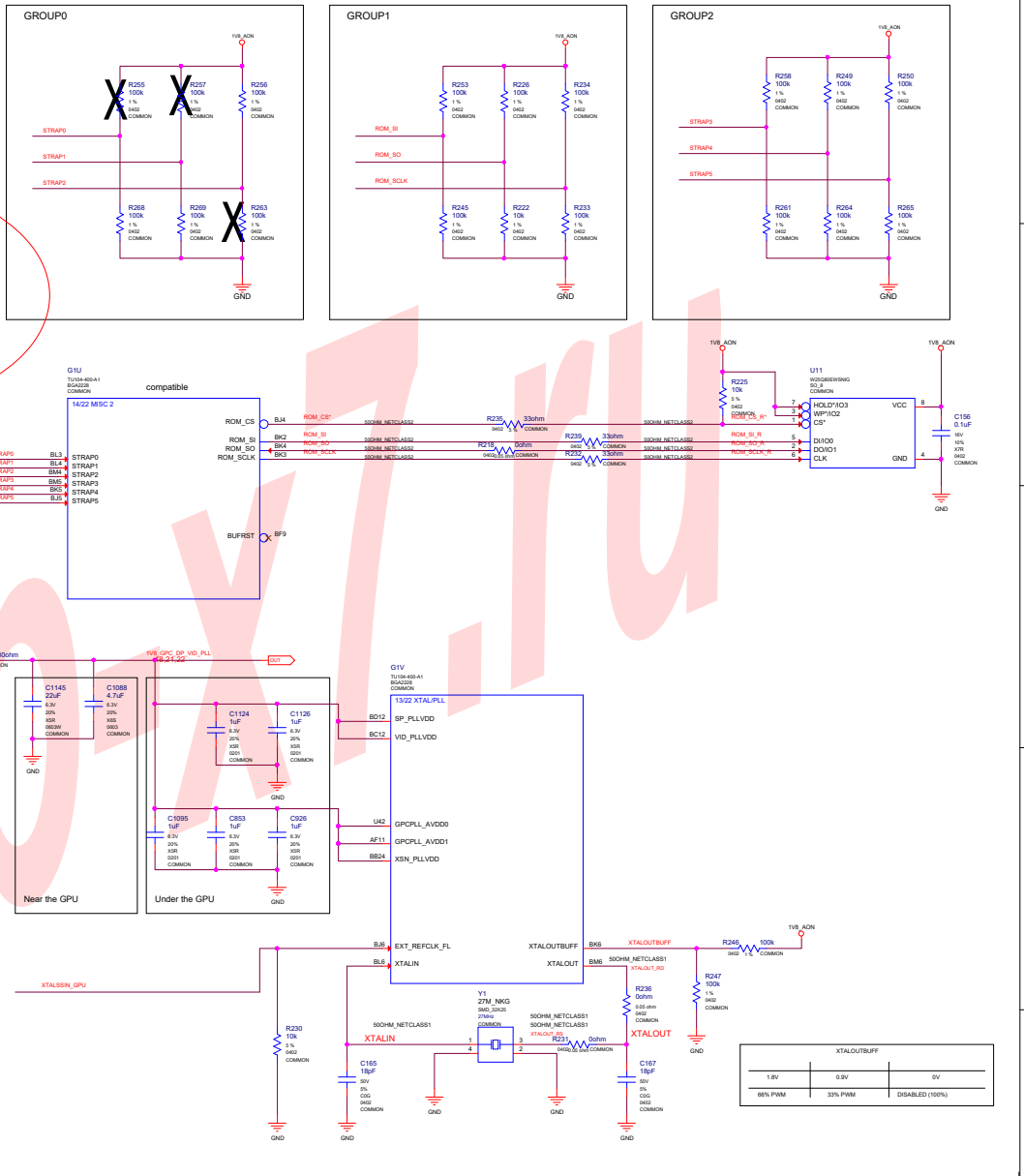
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

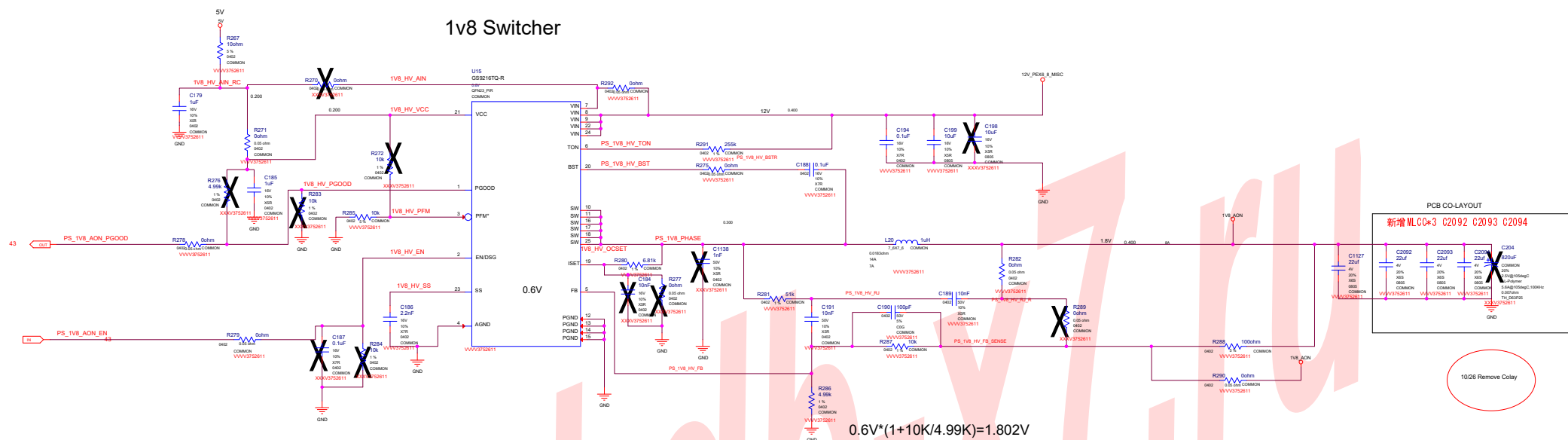
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

注意上件的MEM Straps



1v8 Switcher



PCB CO-LAYOUT

新增MLCC+3 C2092 C2093 C2094

C2092 22uF
4V
20%
X65
COMMON
VV3V752B11

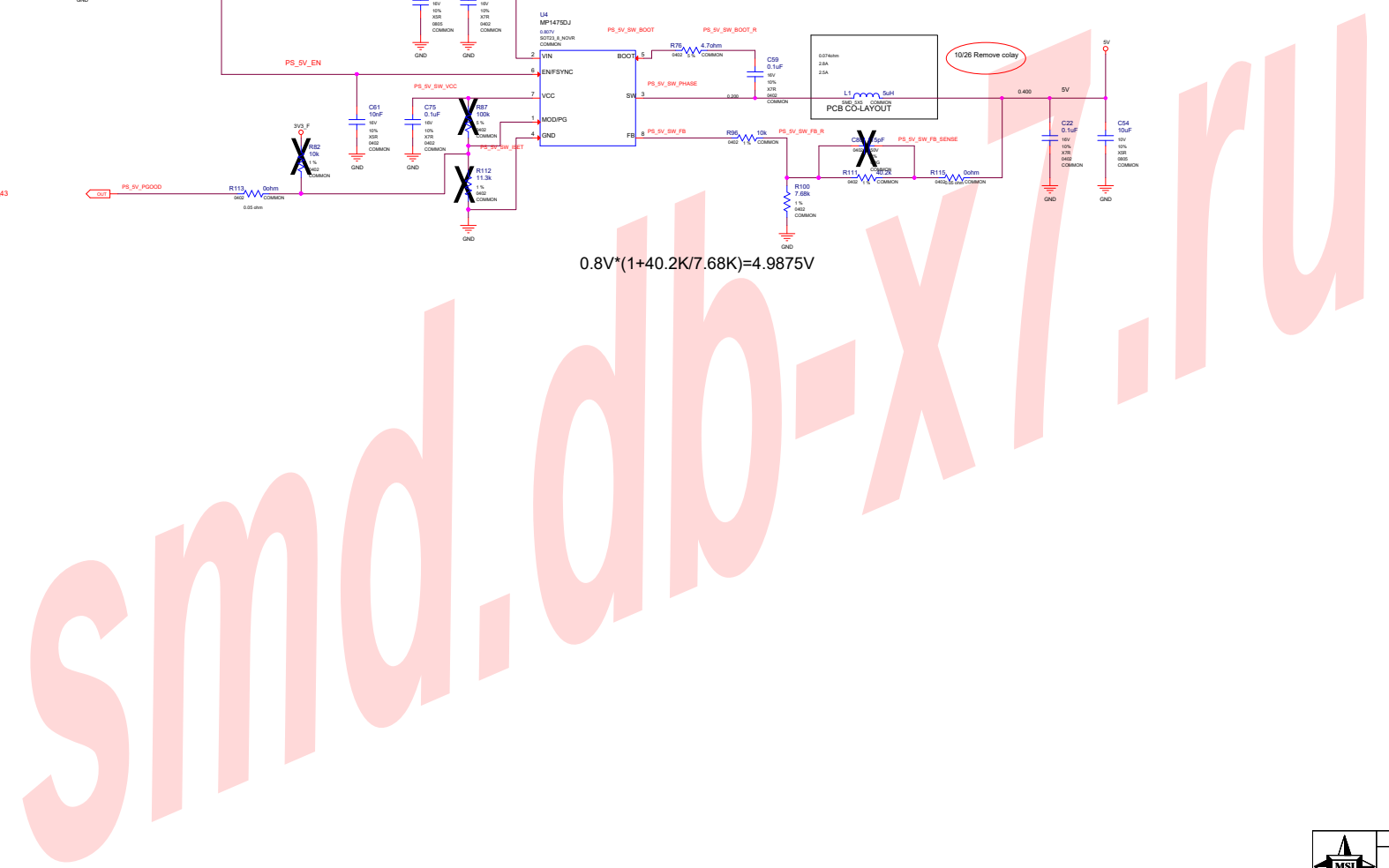
C2093 22uF
4V
20%
X65
COMMON
VV3V752B11

C2094 22uF
4V
20%
X65
COMMON
VV3V752B11

C204 520uF
5.0V1215050C
5.0V1215050C
5.6A@105°C@1000uA
5.000mm
70%DRUGS

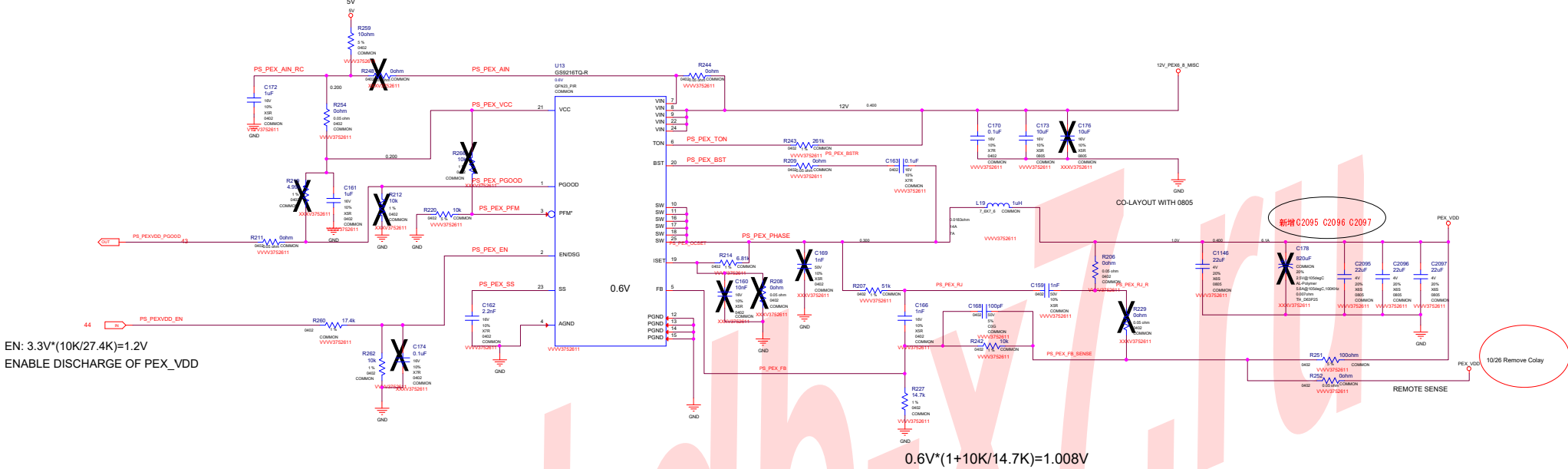
5.0V1215050C
GND

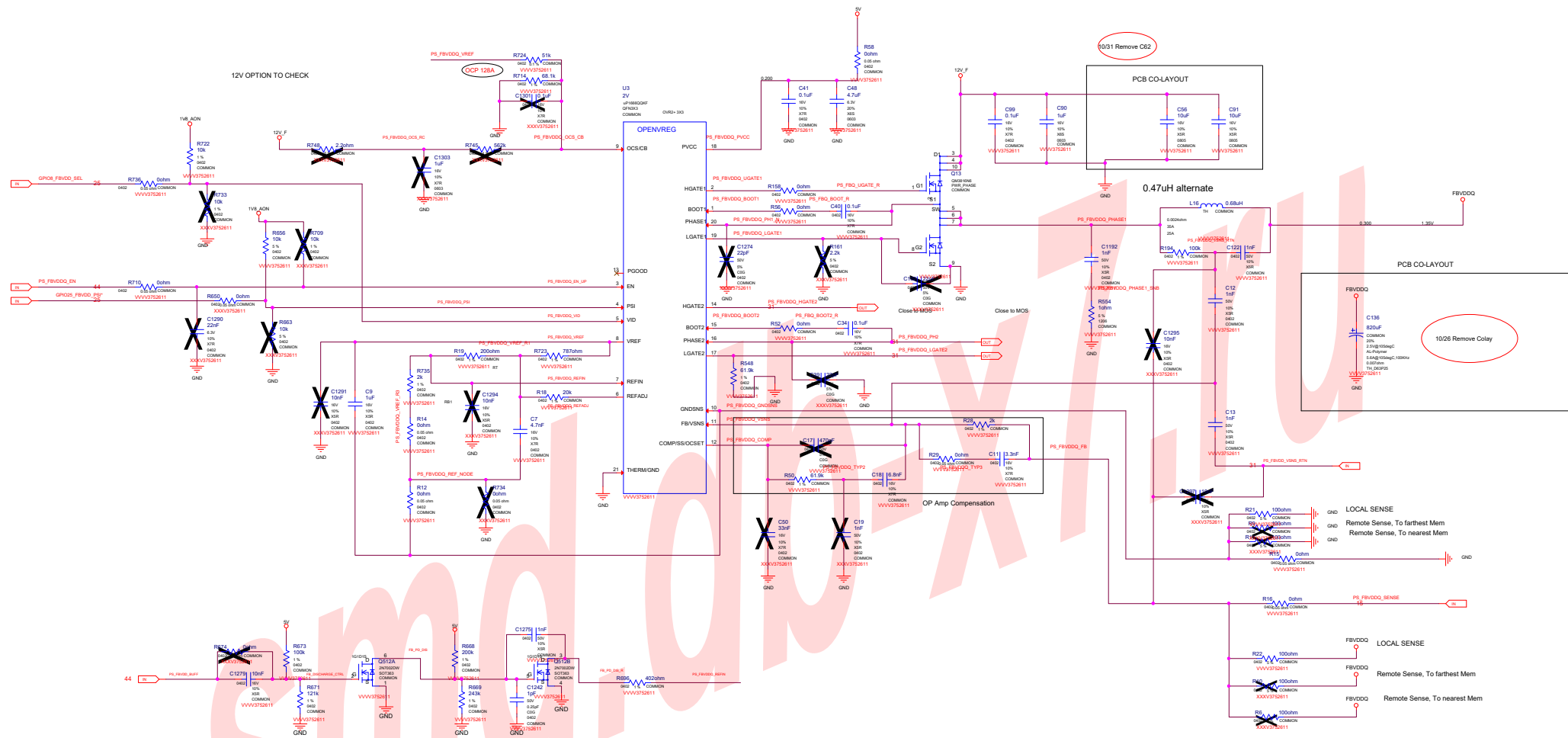
10/26 Remove Colan

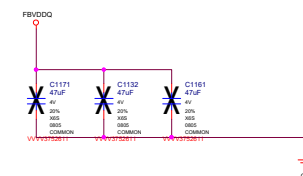
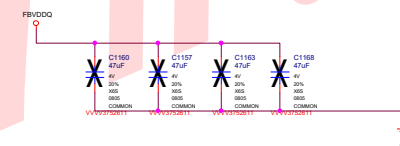
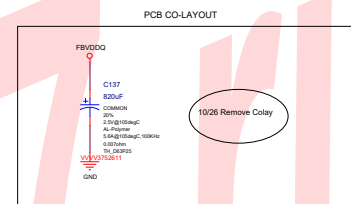
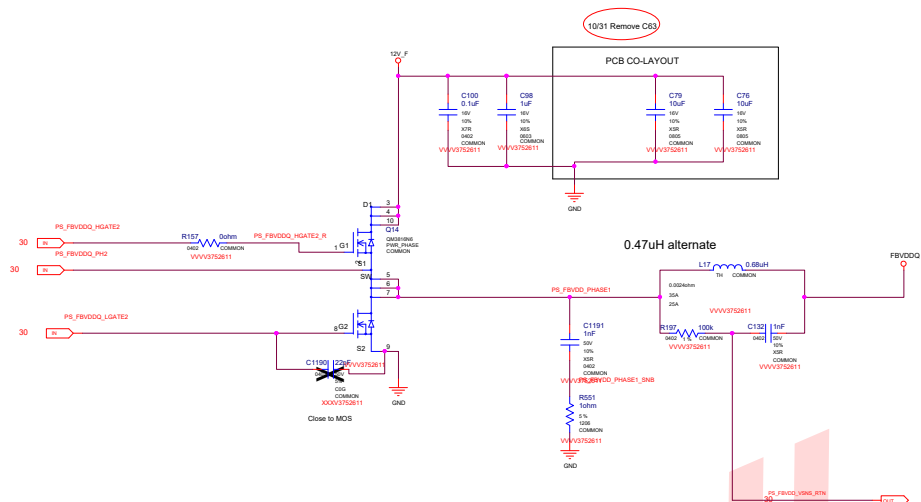


$$0.8V \cdot (1 + 40.2K / 7.68K) = 4.9875V$$

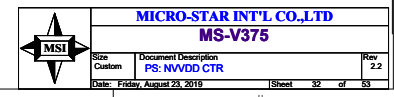
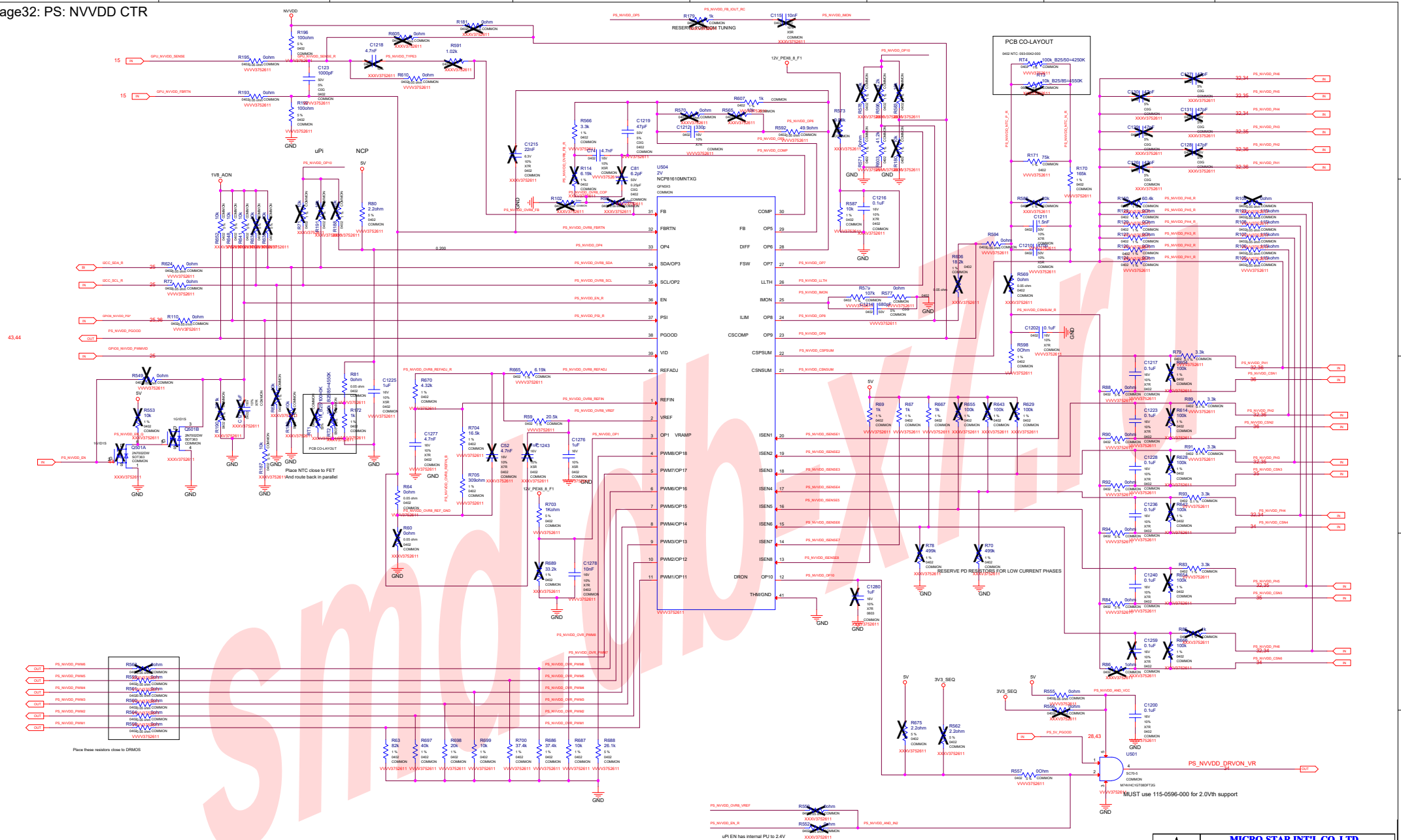
PEX Switcher







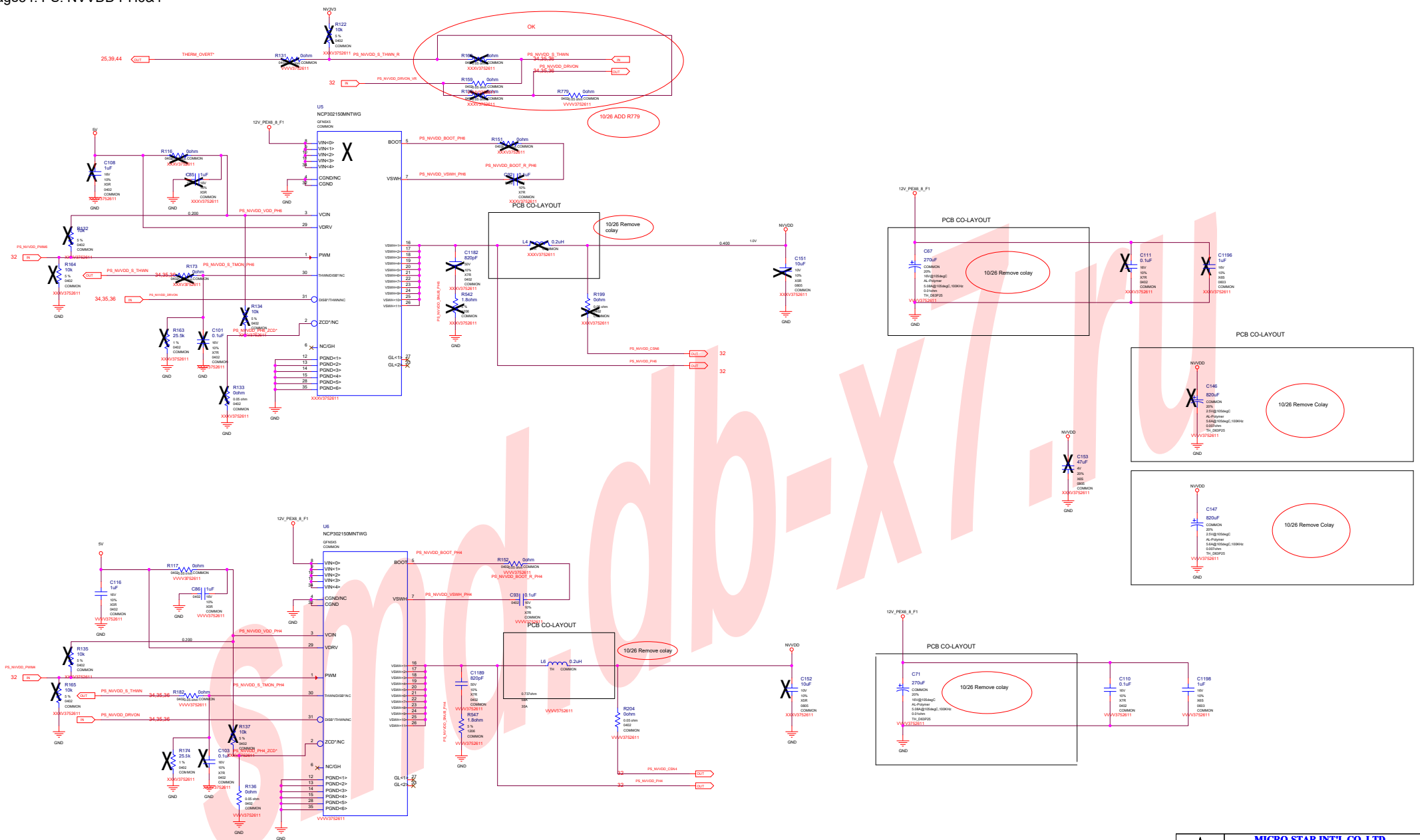
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MS-V375		
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Custom	PS: FBVDDQ PH2	2.2
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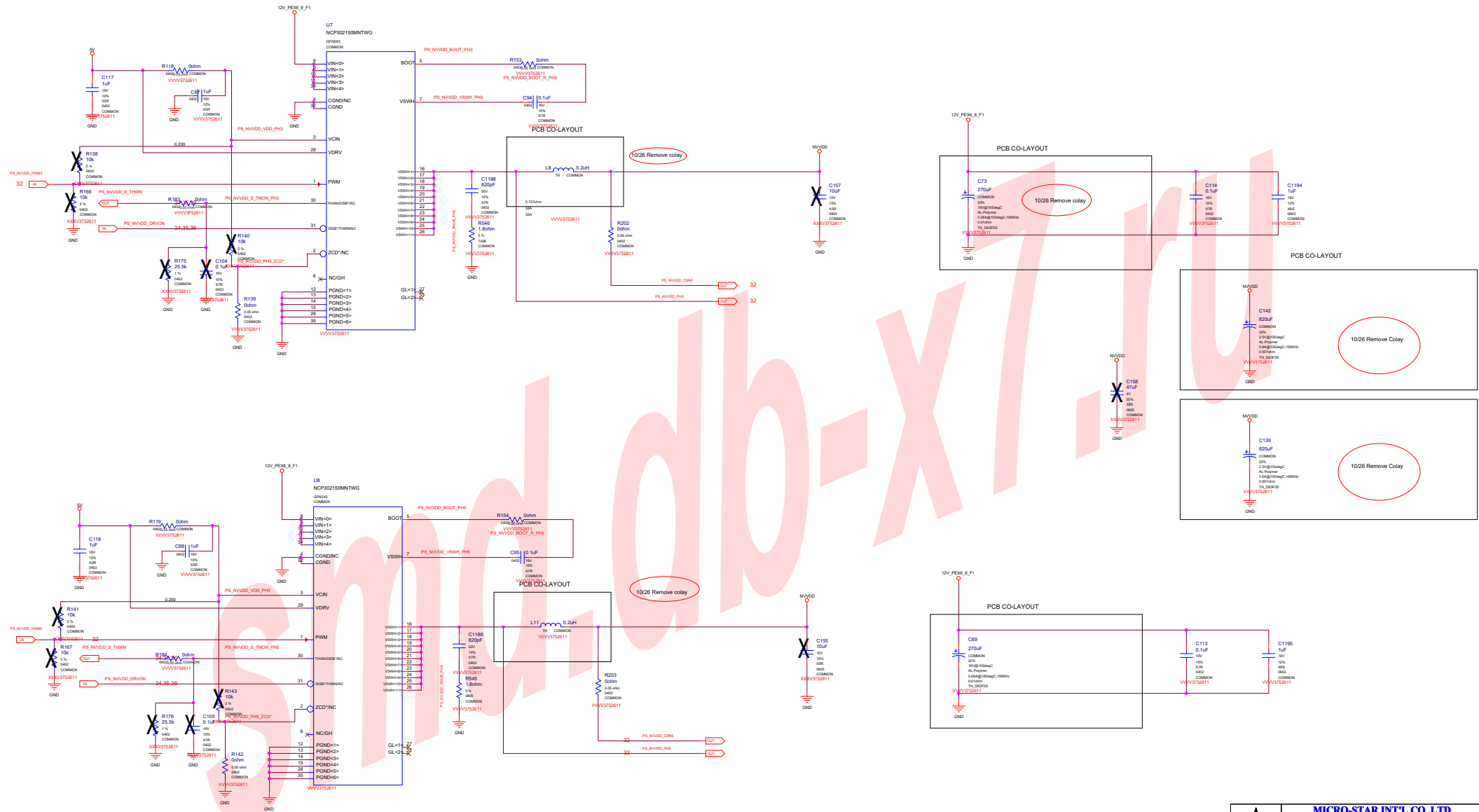


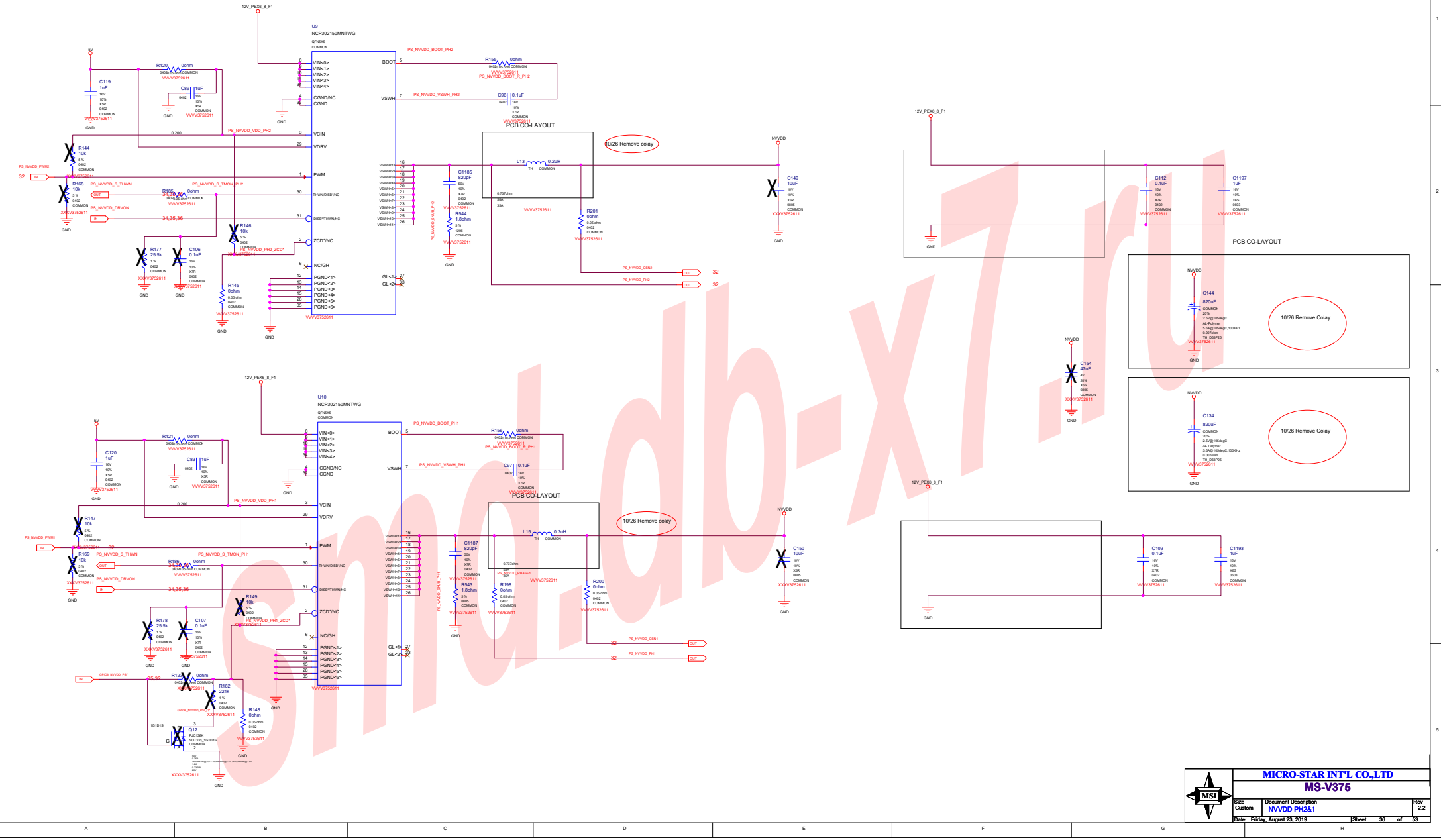
DROP OVR3i SOLUTION

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	Size	Document Description	Rev
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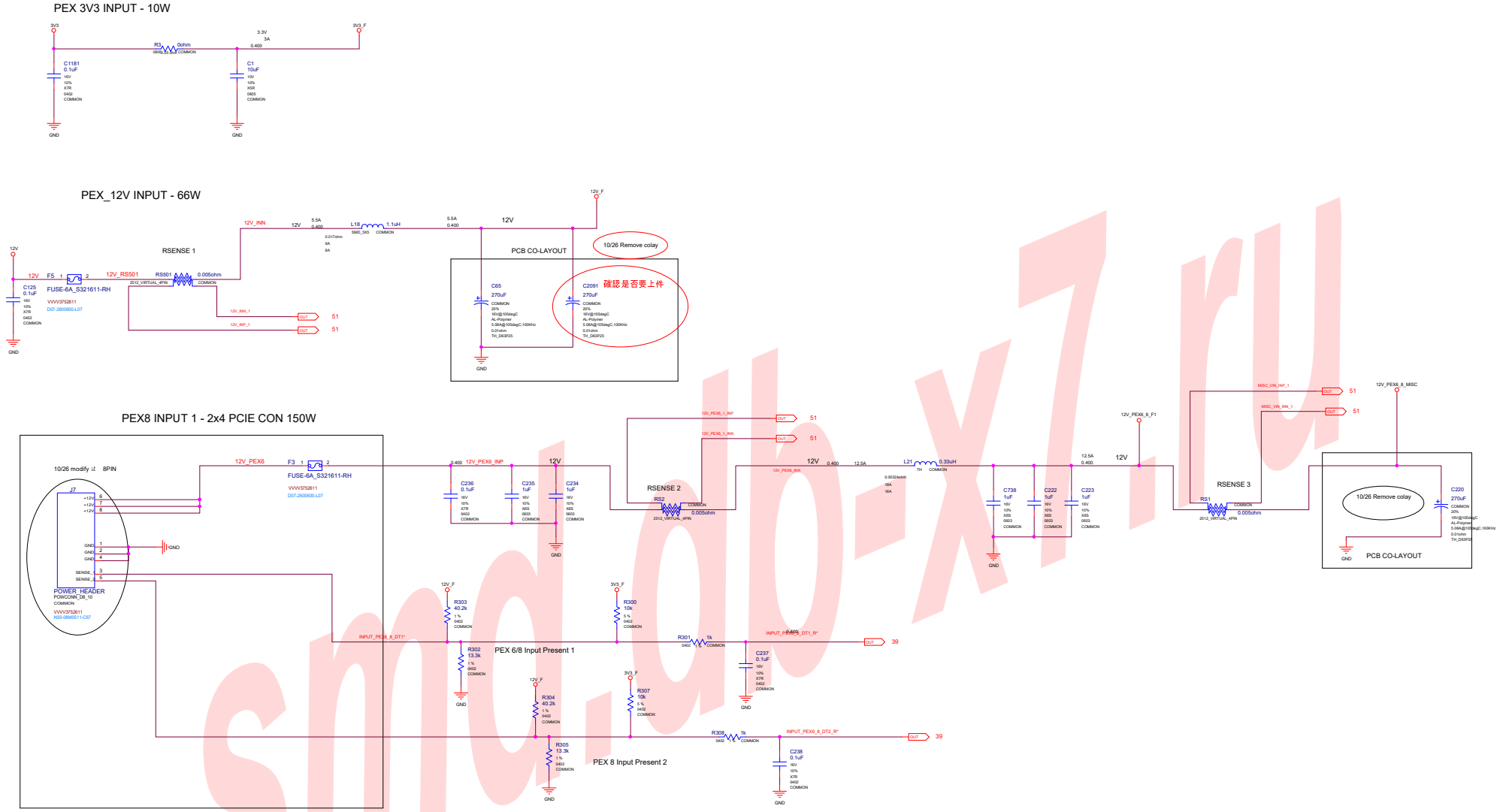




DELETE RAIL BALANCE CIRCUIT

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	MICRO-STAR INT'L CO.,LTD		
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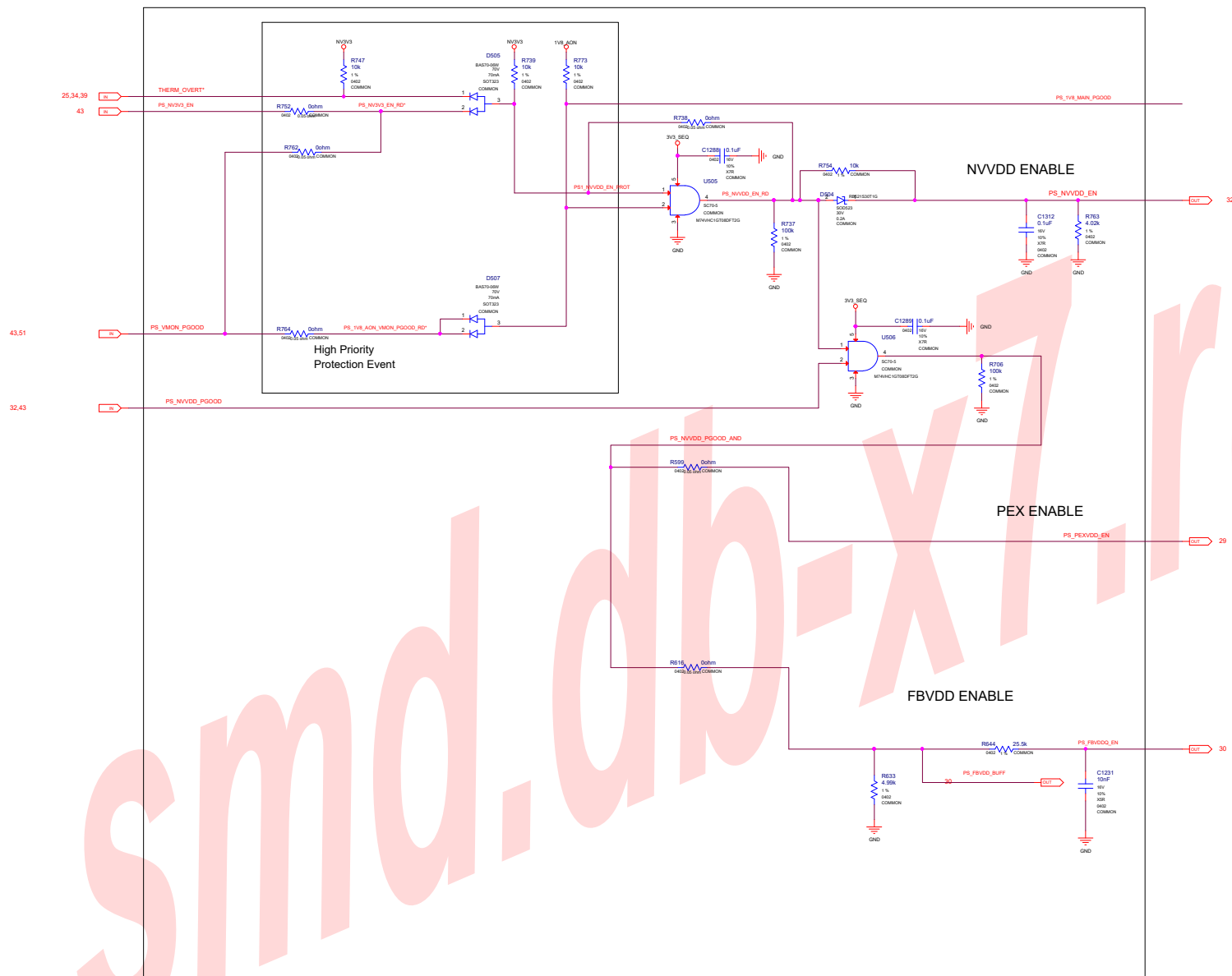
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	MICRO-STAR INT'L CO.,LTD		
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	Custom	12V & 3V3_A SWITCHER	2.2
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Size Custom	Document Description SEQ.NV_PEX,FB ENABLE	Rev 2.2
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	Size	Document Description	Rev
	Custom	SEQUENCE:Voltage Monitor	2.2
Date: Friday, August 23, 2019		Sheet 45 of 53	

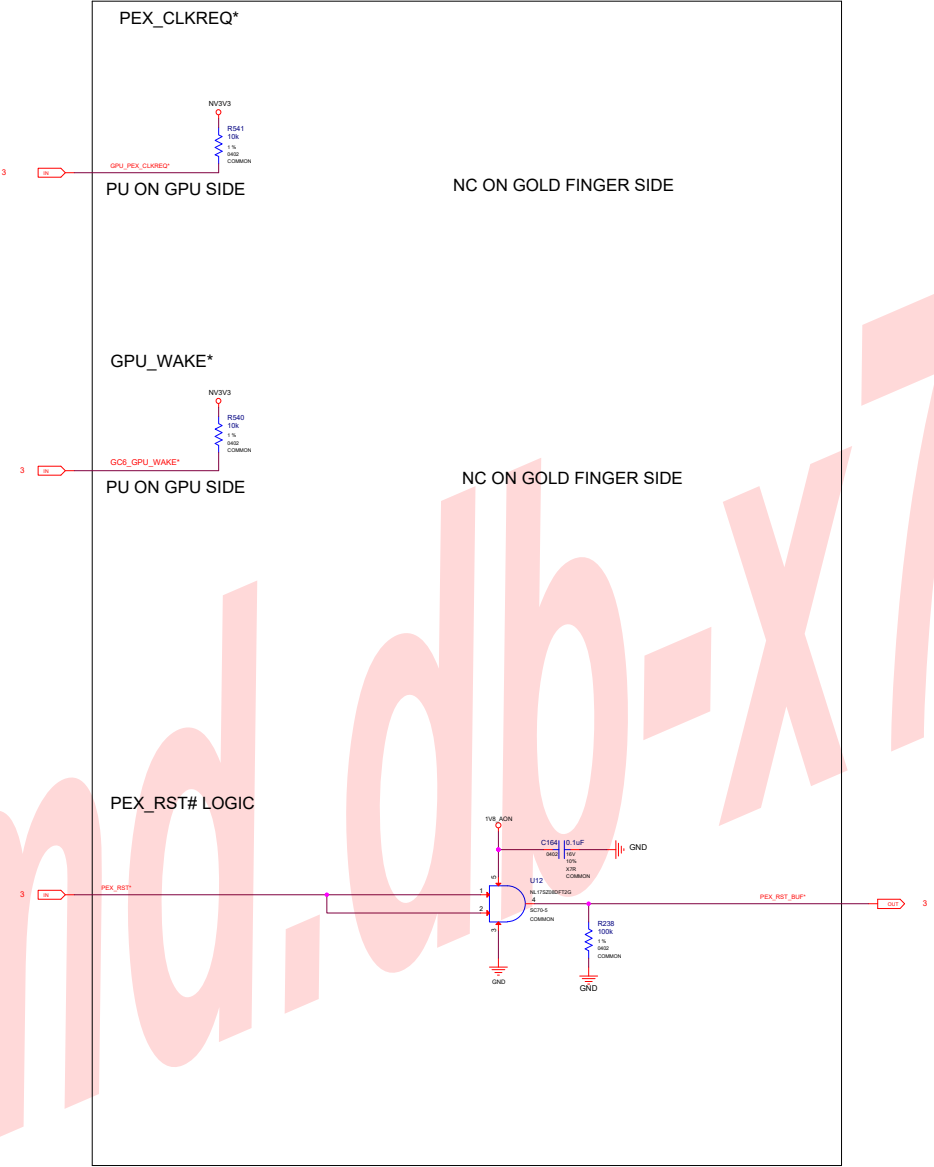
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Size	Document Description	Rev
Custom	SEQUENCE:Discharge	2.2
Date: Friday, August 23, 2019		Sheet 46 of 53

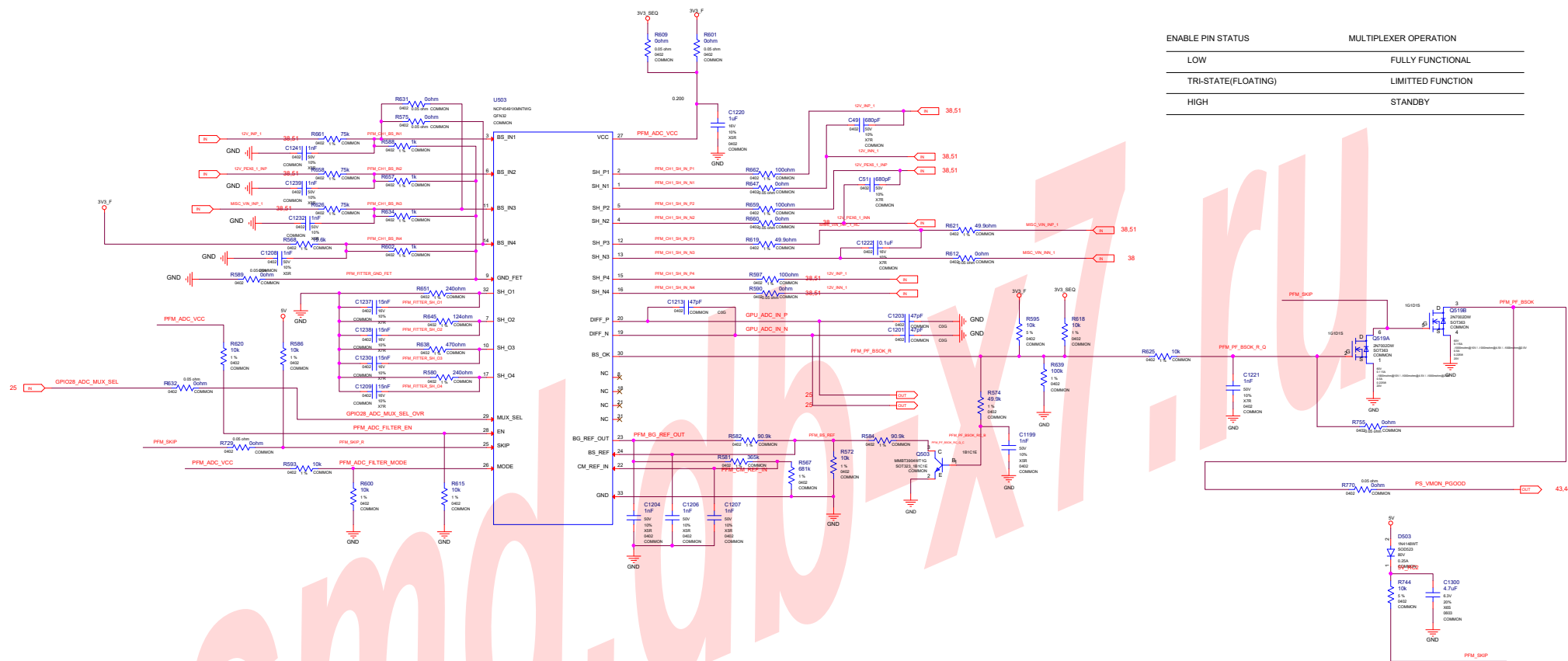


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	Size	Document Description	Rev
	Custom	LOGO LED	2.2
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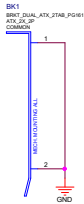
Size Custom	Document Description FAN	Rev 2.2
Date: Friday, August 23, 2019		Sheet 50 of 53



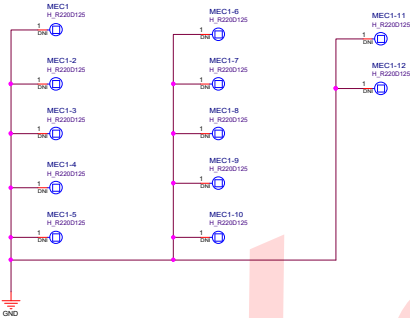
MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

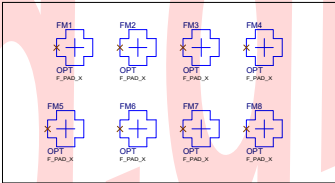
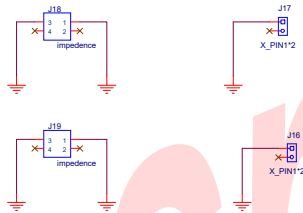
Bracket:



MOUNTING HOLES FOR HS:



BACK STIFFENER:



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	MS-V375		
	Size	Document Description	Rev
	Custom	PTC	2.2
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