

PG165-A00

TU116 6GB GDDR5, 192b, X32
DVI-D + DP + HDMI

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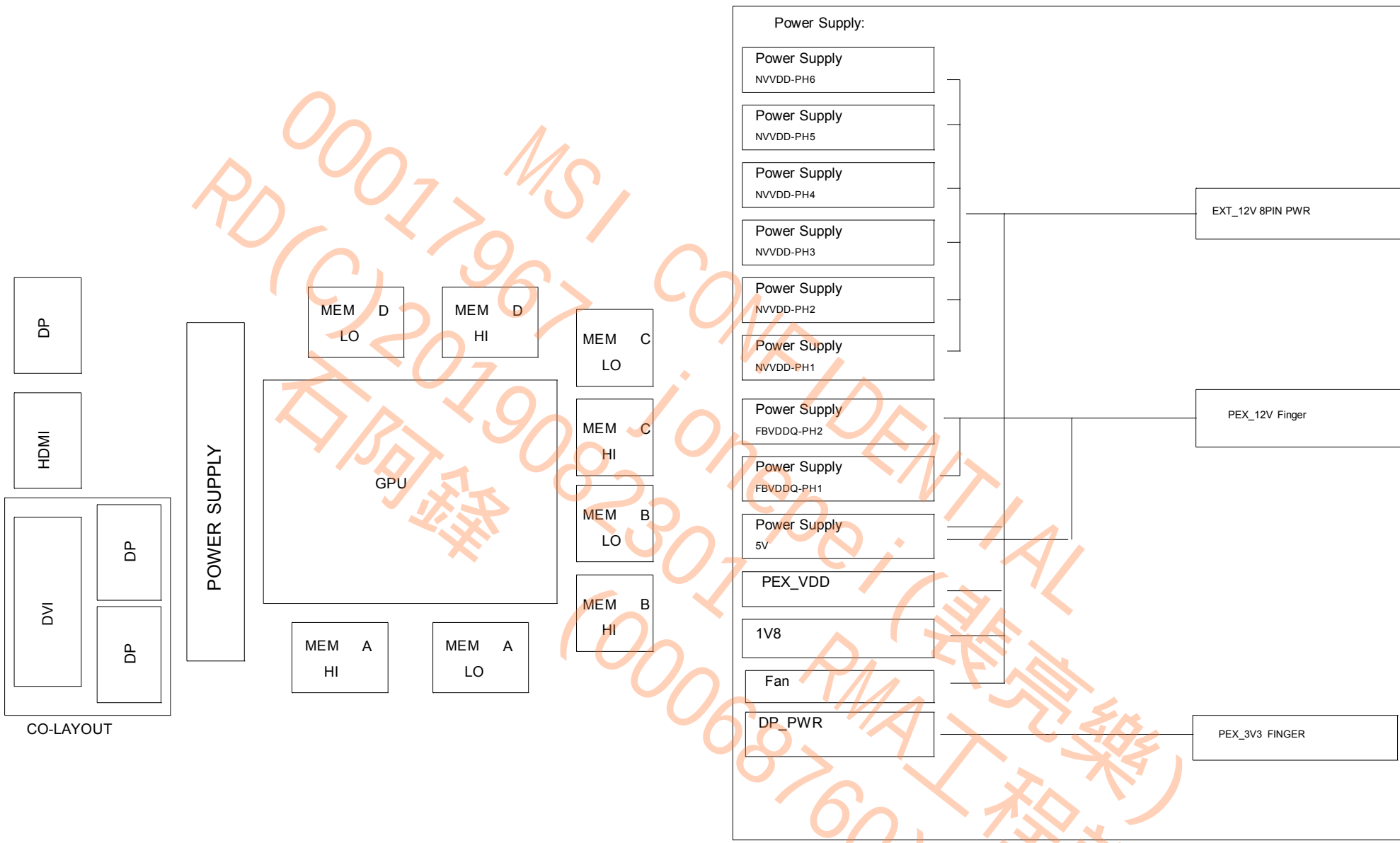
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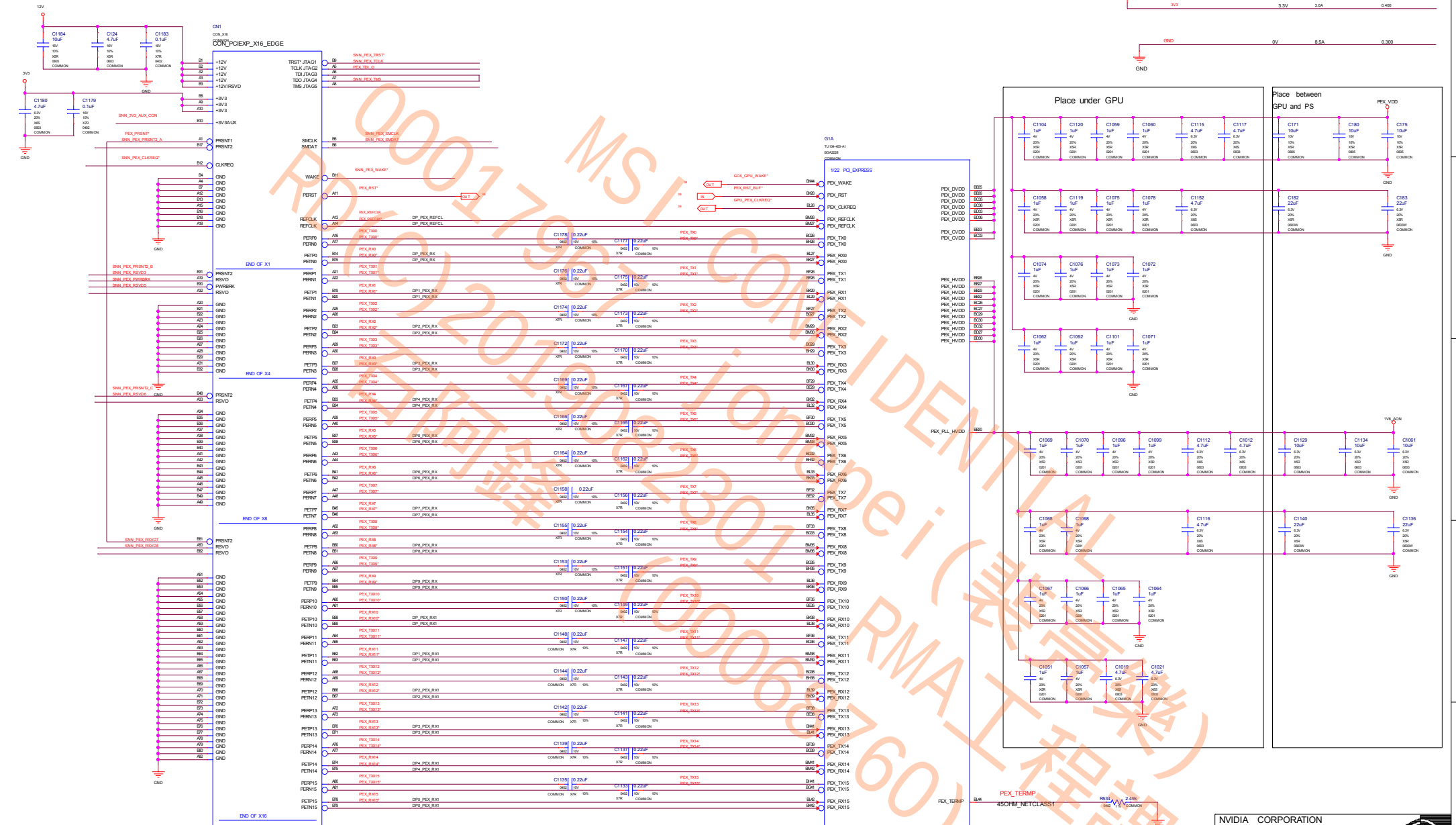
NV_PN	600-1G165-BASE-000		
PCB REV	PG165-A00	PRG#	1 OF 42
BOM REV	8	DATE	14-DEC-2018



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ASSEMBLY	ASSEMBLY DESCRIPTION
FIGURE DETAIL	Block Diagram

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCI Express

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[illegible]

AF49+CMD32, AQ52+CMD33 IN TU104
AF49+CMD33, AQ52+CMD32 IN GP104

G18

TU104-400-A1

BGA555

compatible

222 FBA

FBA_CMD00

FBA_CMD01

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FBA_CMD03

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FBA_CMD330

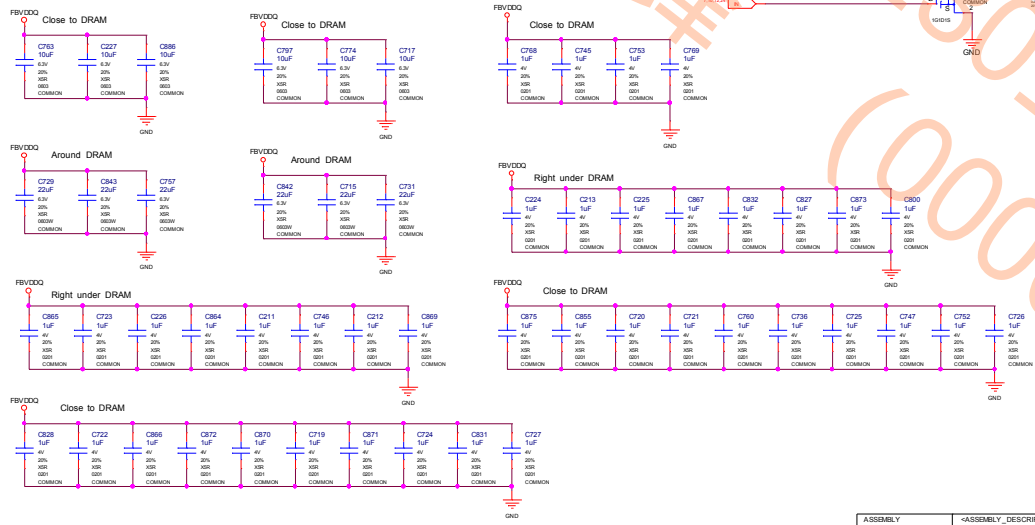
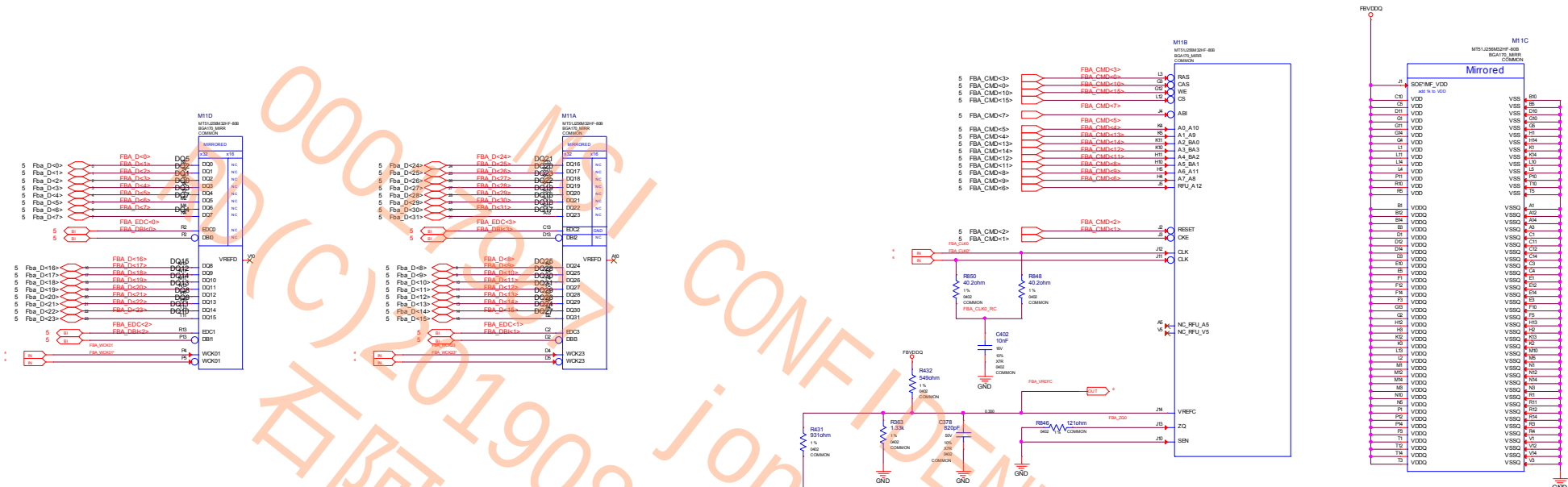
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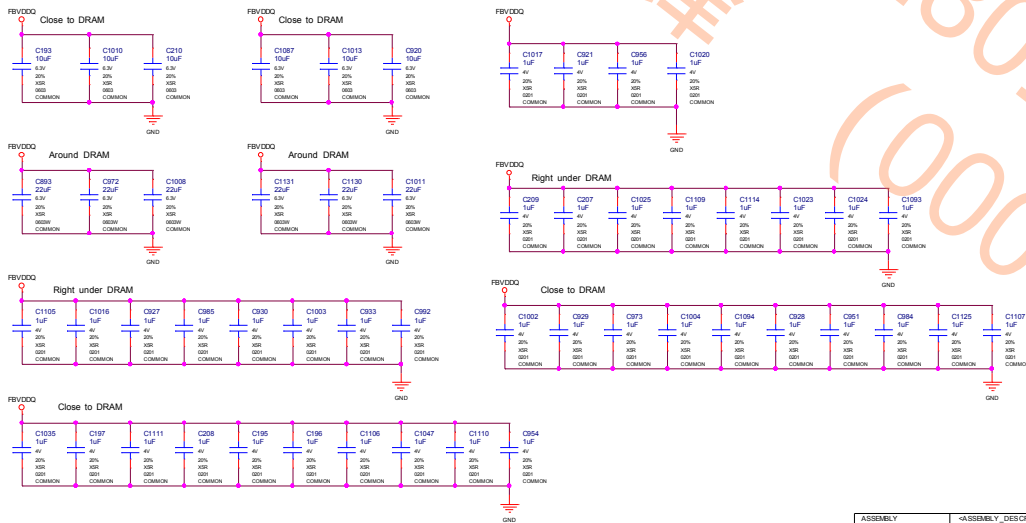
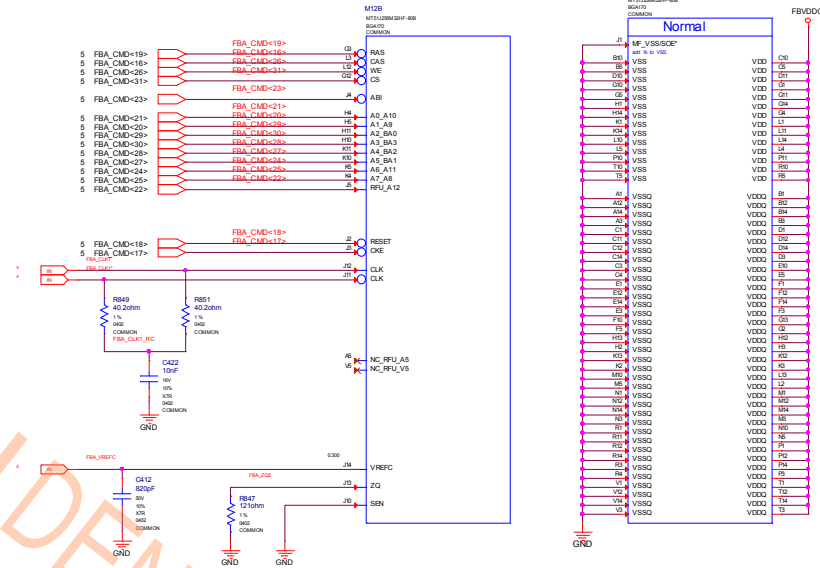
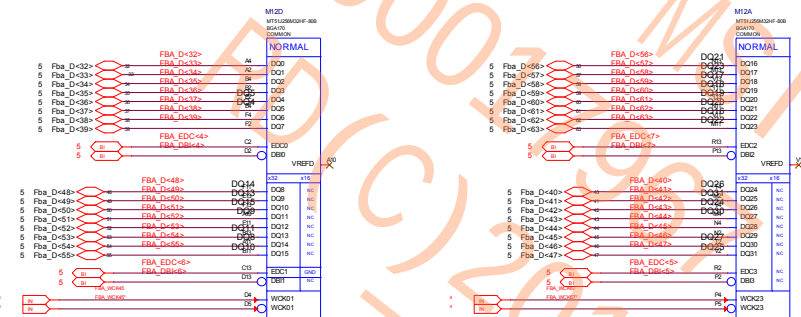


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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PCB DETAIL	MEMORY: FBA[31:0]





ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	MEMORY: FBA(63.32)

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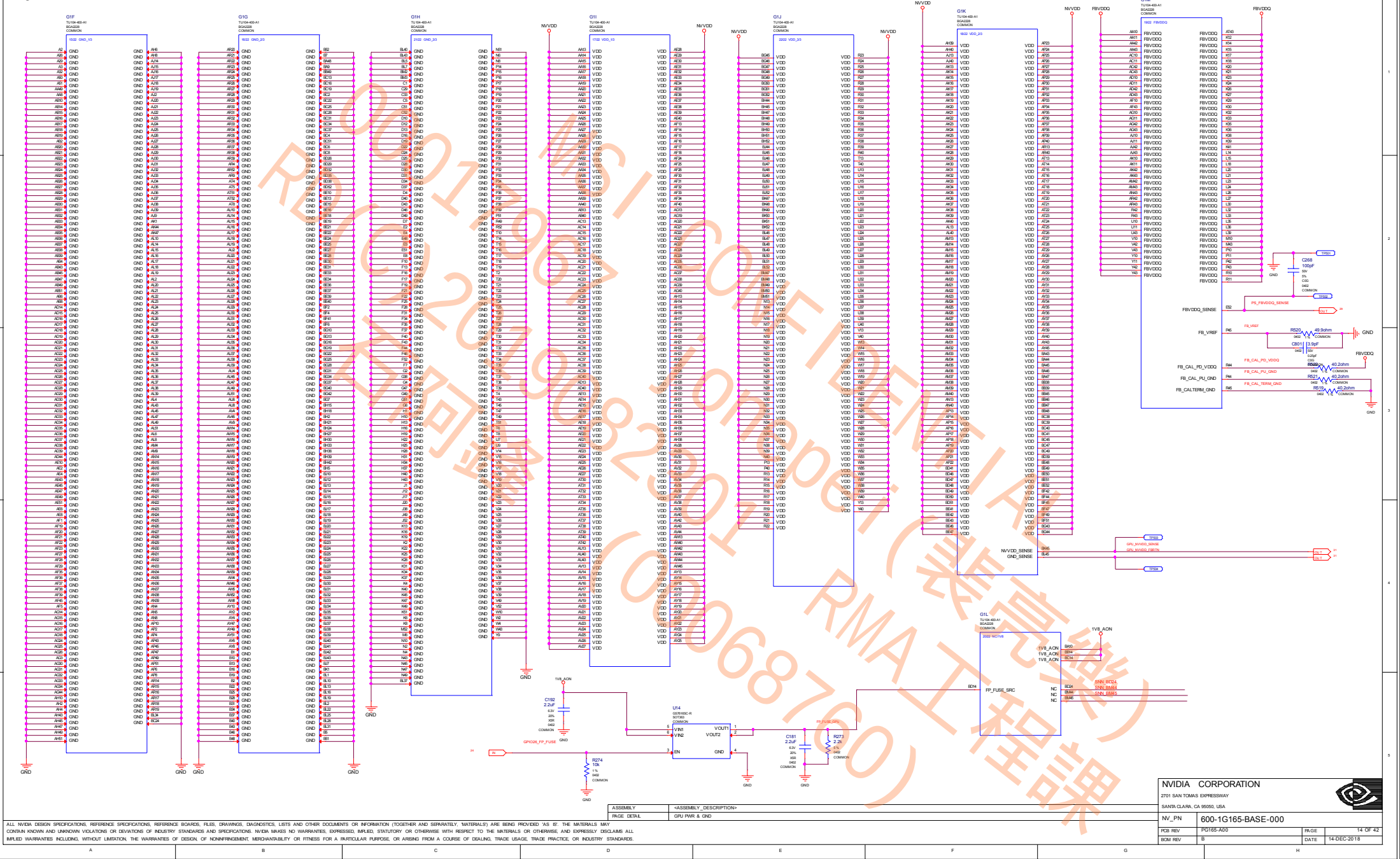


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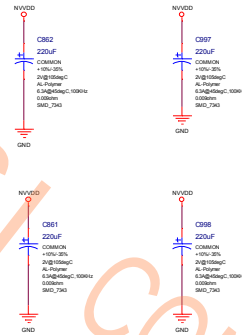


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LAMB ALL STANDARDS.		PCB REV PG165-A00 PRICE 14 OF 42 BOM REV B DATE 14/DEC-2018

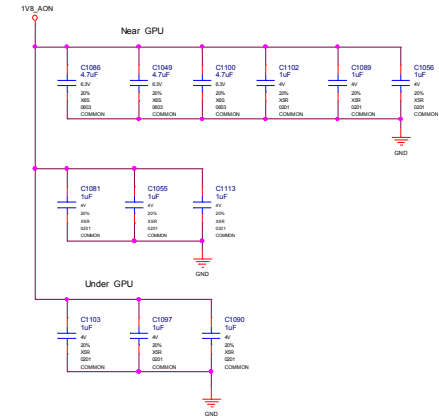
FBVDDQ



NVDD



1V8_AON



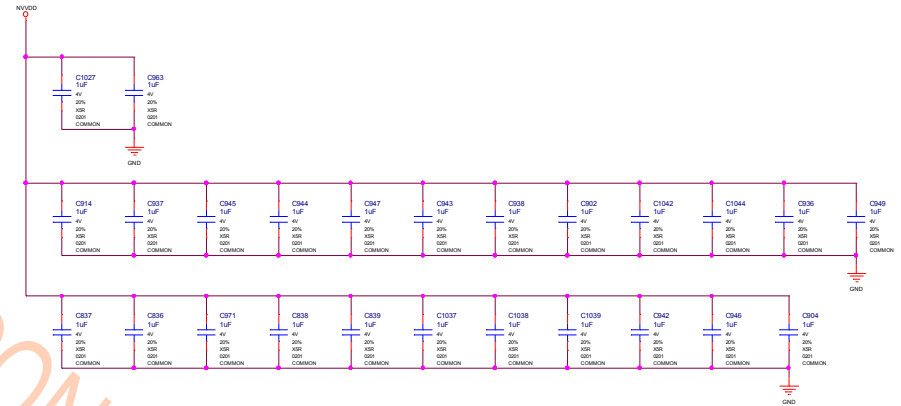
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ASSEMBLY	ASSEMBLY DESCRIPTION
FRIDGE DETAIL	GPU DECOUPLING 1

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NV_PN	600-1G165-BASE-000		
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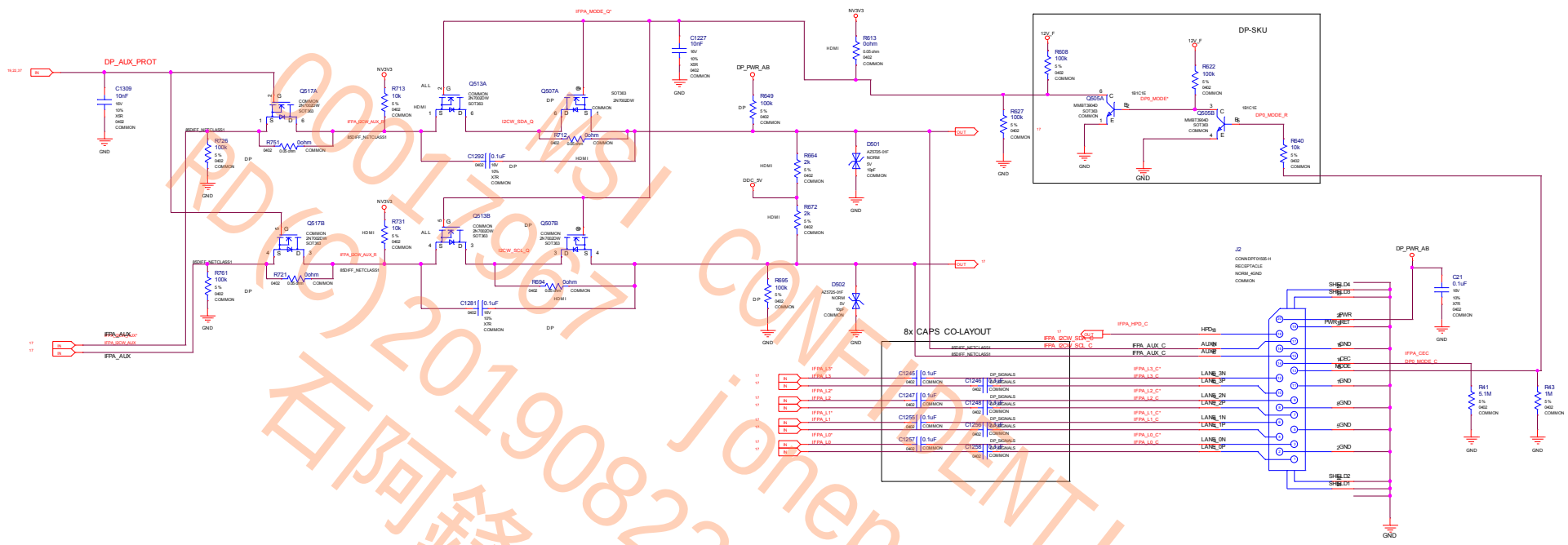


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PAGE DETAIL	GPU DECOUPLING 2



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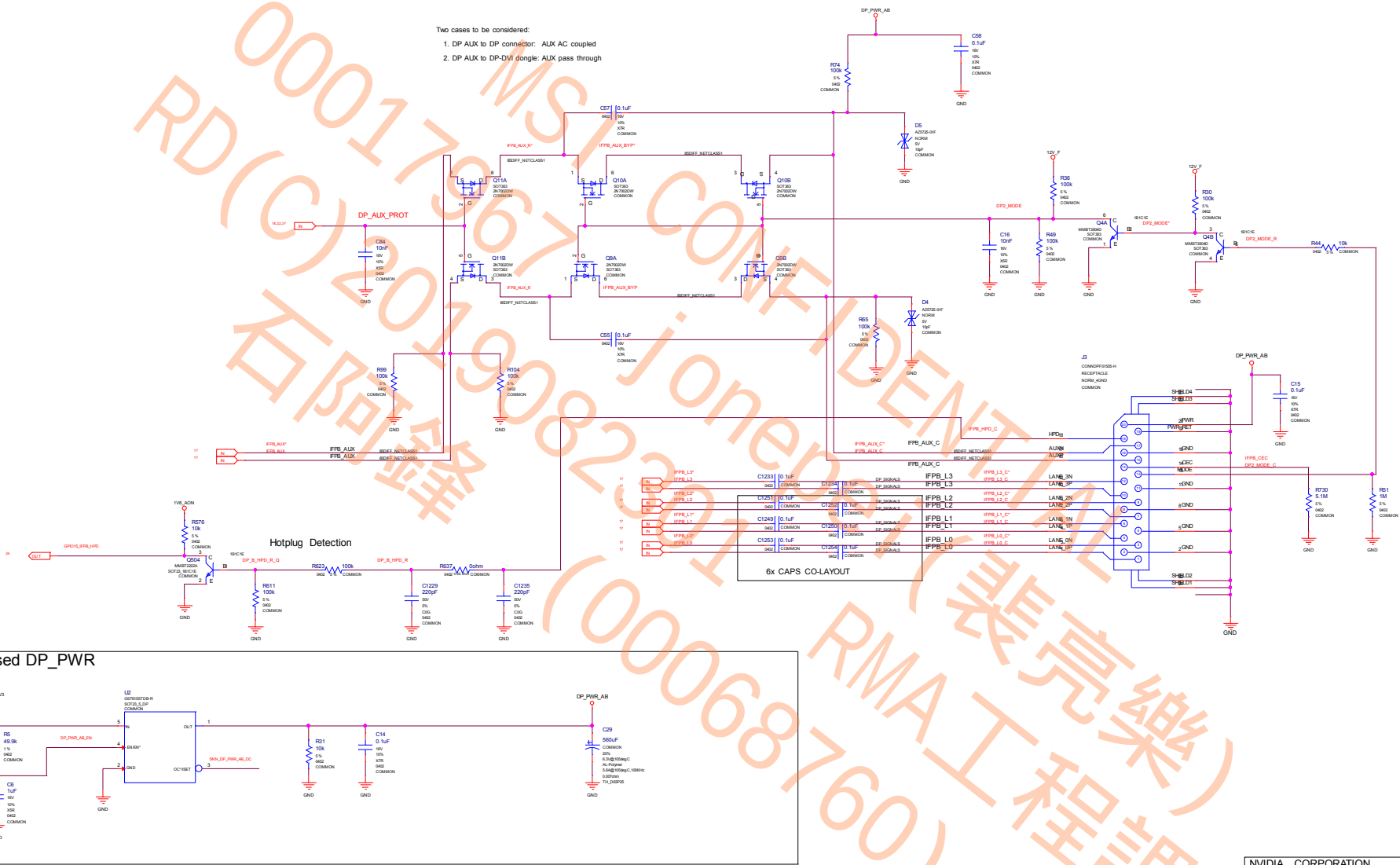
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DATE

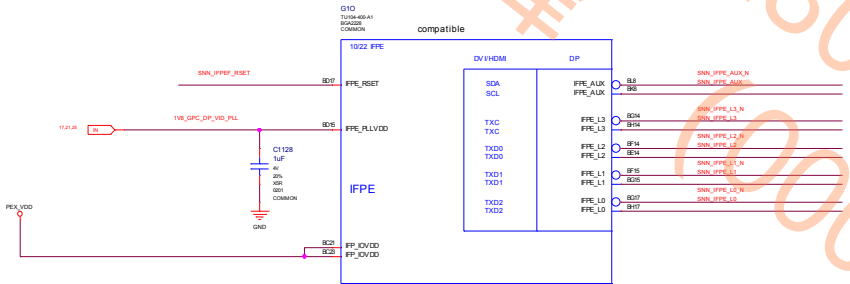
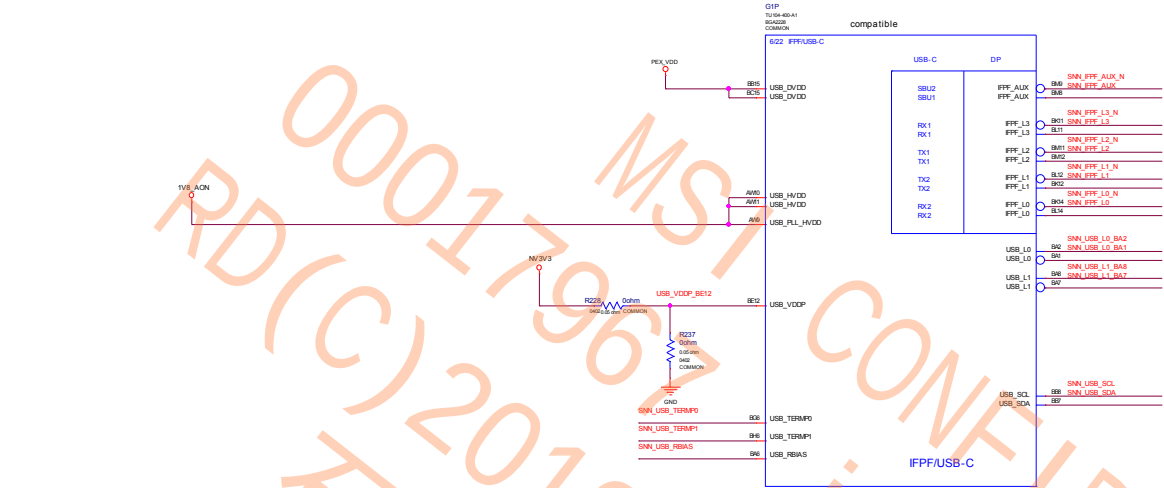
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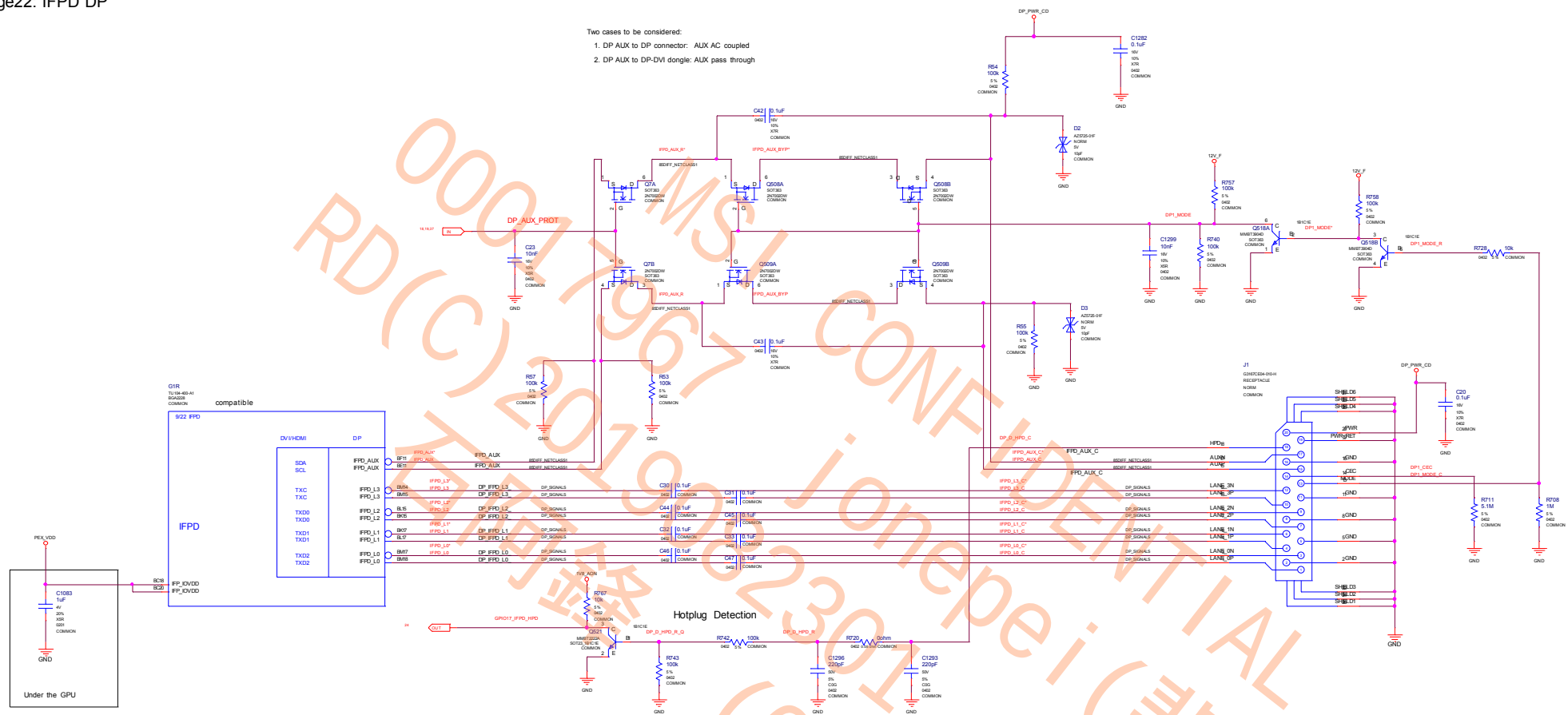
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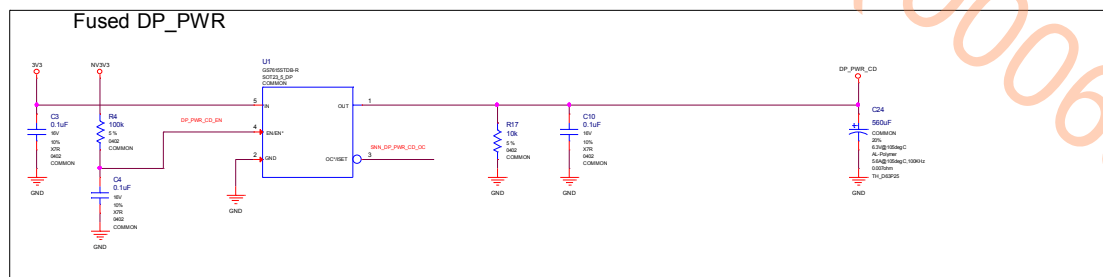
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Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



Fused DP_PWR



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFFD DP

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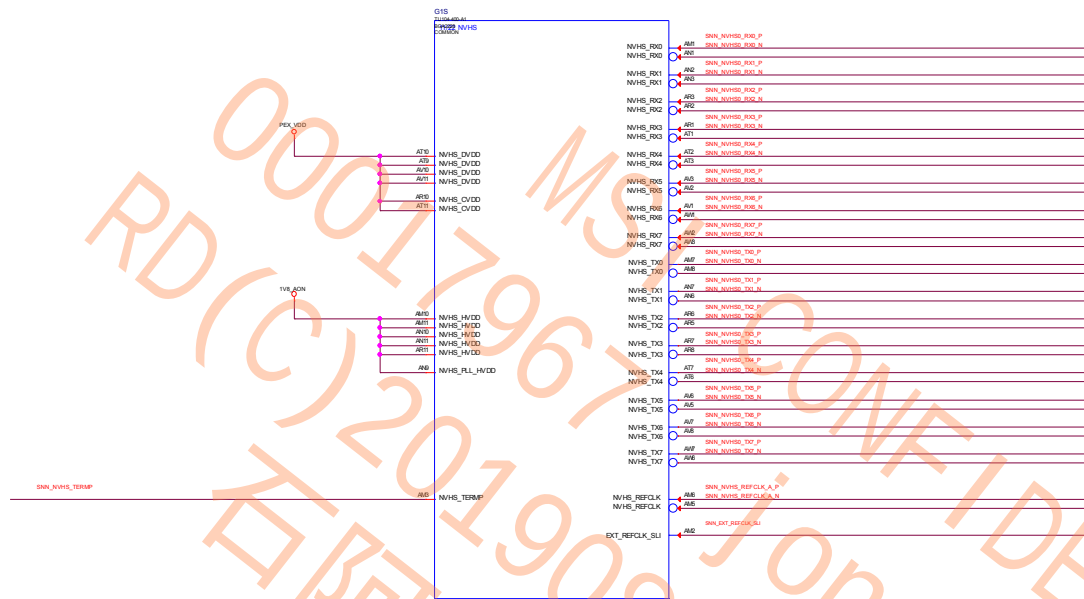
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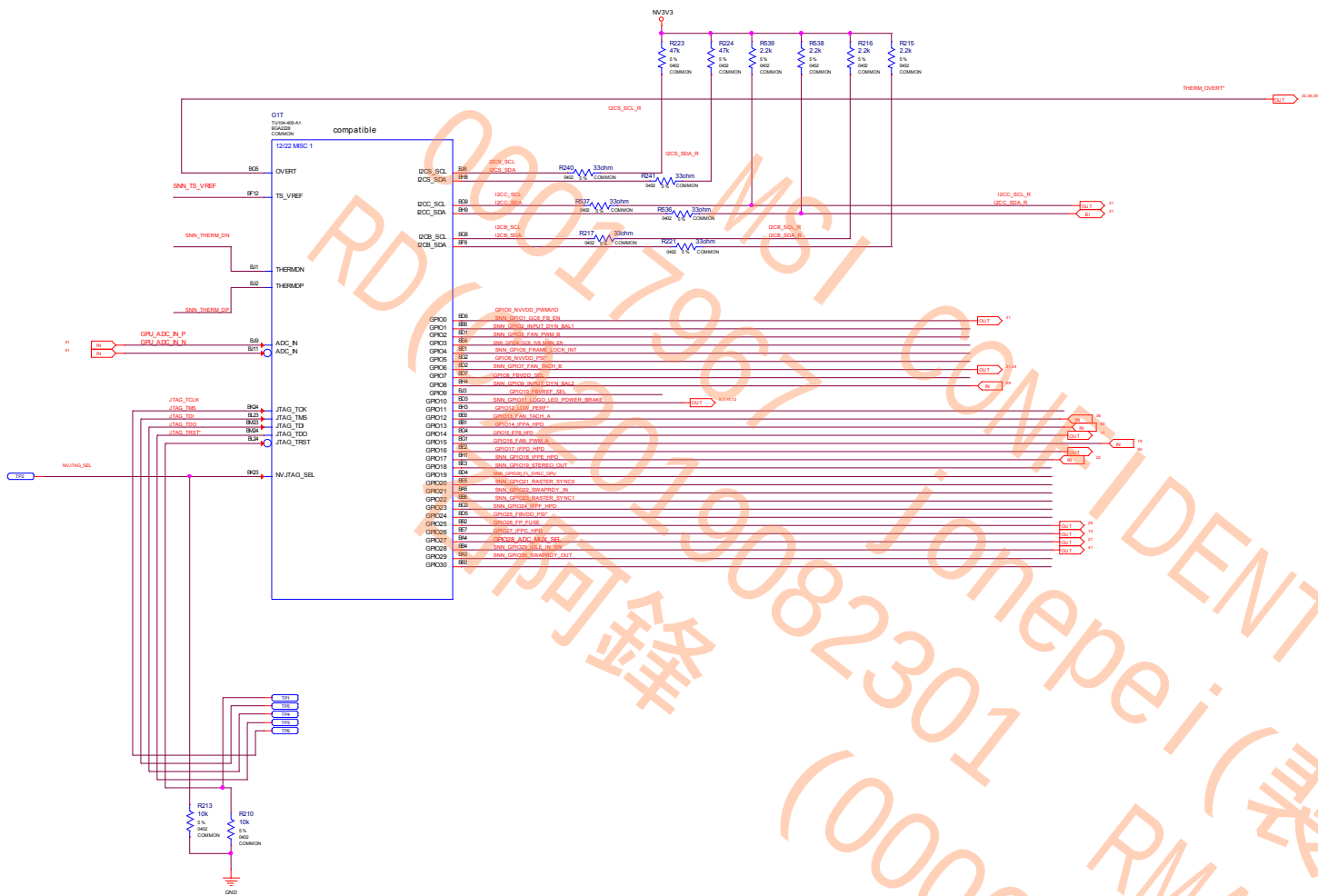
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PCB REV	PG165-A00
ROM REV	B
PRGE	24 OF 42
DATE	14-DEC-2018

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	0000
L	L	H	0001
L	H	L	0010
L	H	H	0011
H	H	L	0110
H	H	H	0111
L	L	M	0100

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	0000	Samsung 8Gb 256Mx32 K4G80325FC-HC25
L	L	H	0001	Micron 8Gb 256Mx32 MT51J256M32HF-80:B
L	H	L	0010	Hynix 8Gb 256Mx32 H5GC8H24AJR-R2C
L	H	H	0011	Hynix 8Gb 256Mx32 H5GQ8H24MJR-R4C
H	H	L	0110	
H	H	H	0111	
L	L	M	1000	
L	M	L	1001	

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]_FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

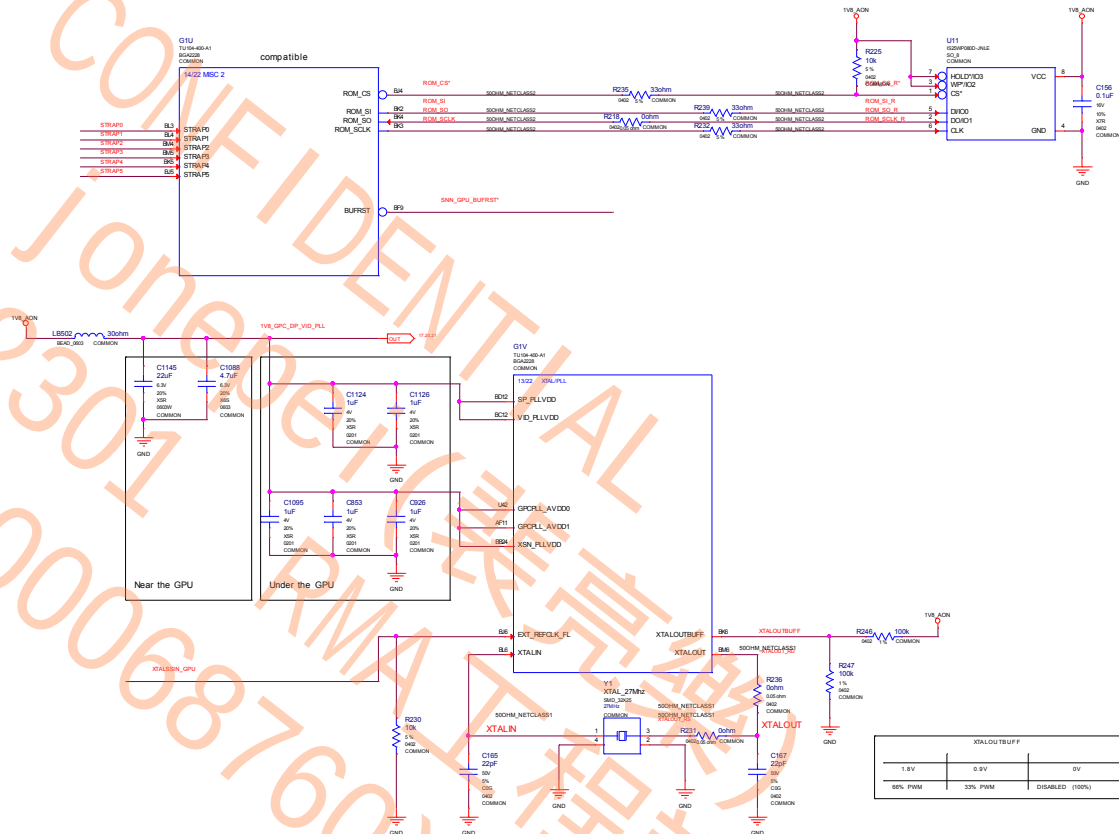
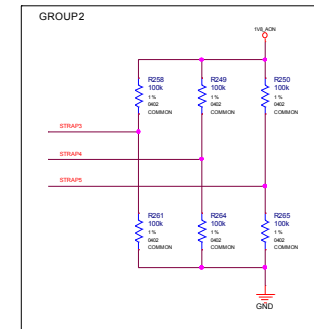
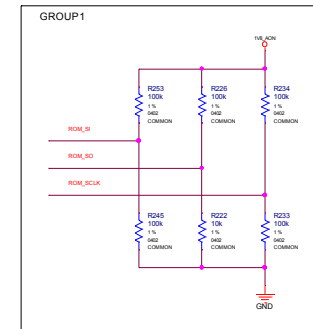
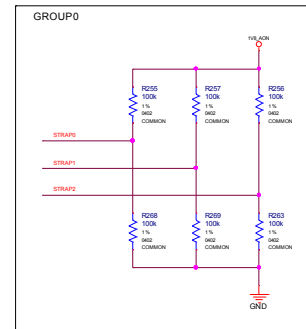
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



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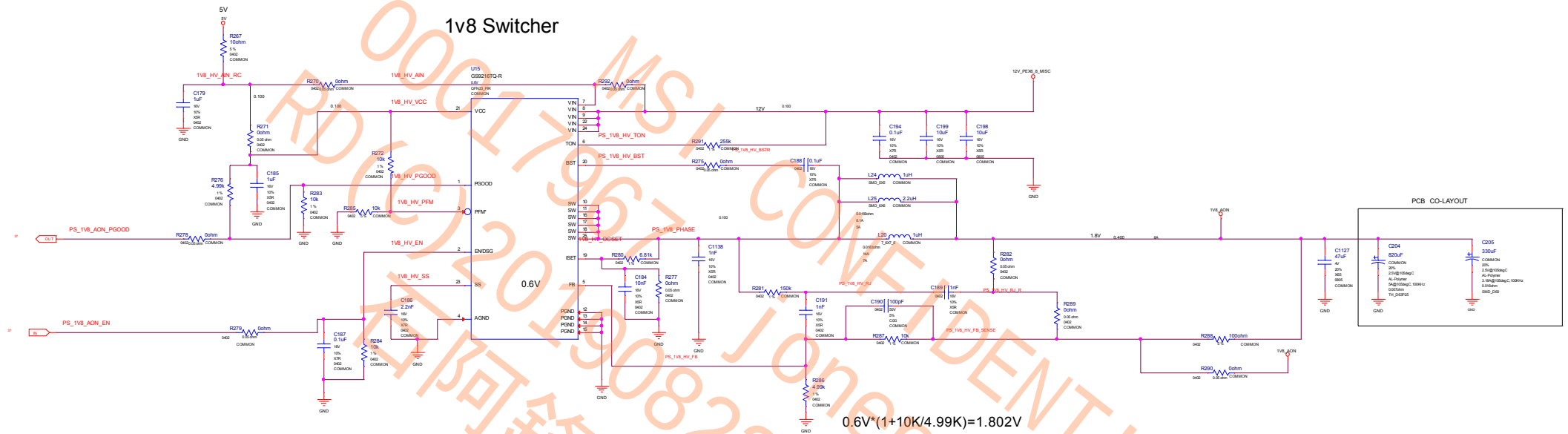


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PCB REV PG165-ADD
ROM REV B

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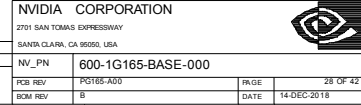


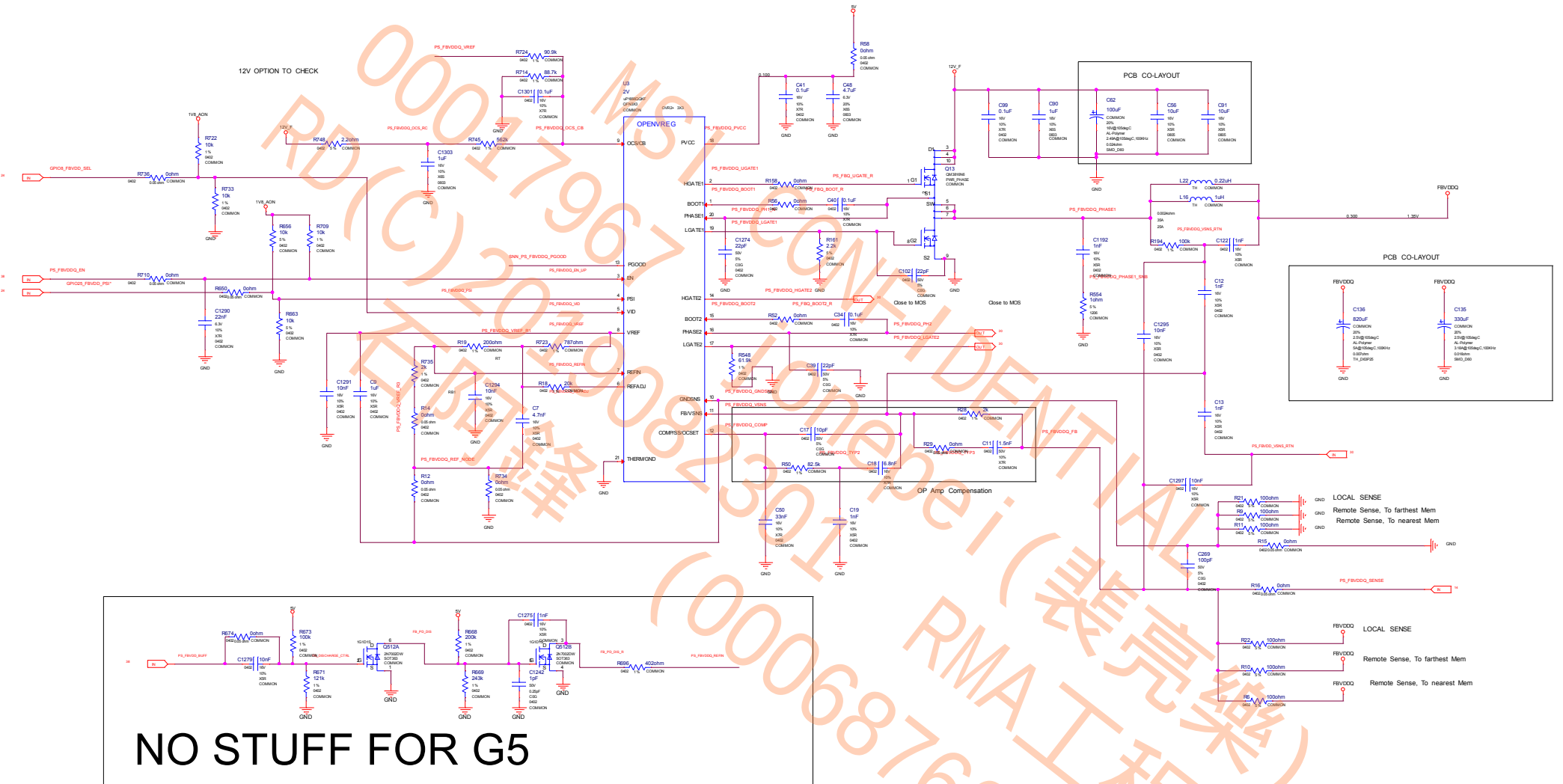
$$0.6V \cdot (1 + 10K/4.99K) = 1.802V$$

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RMAT (Bright) Engineering (760)

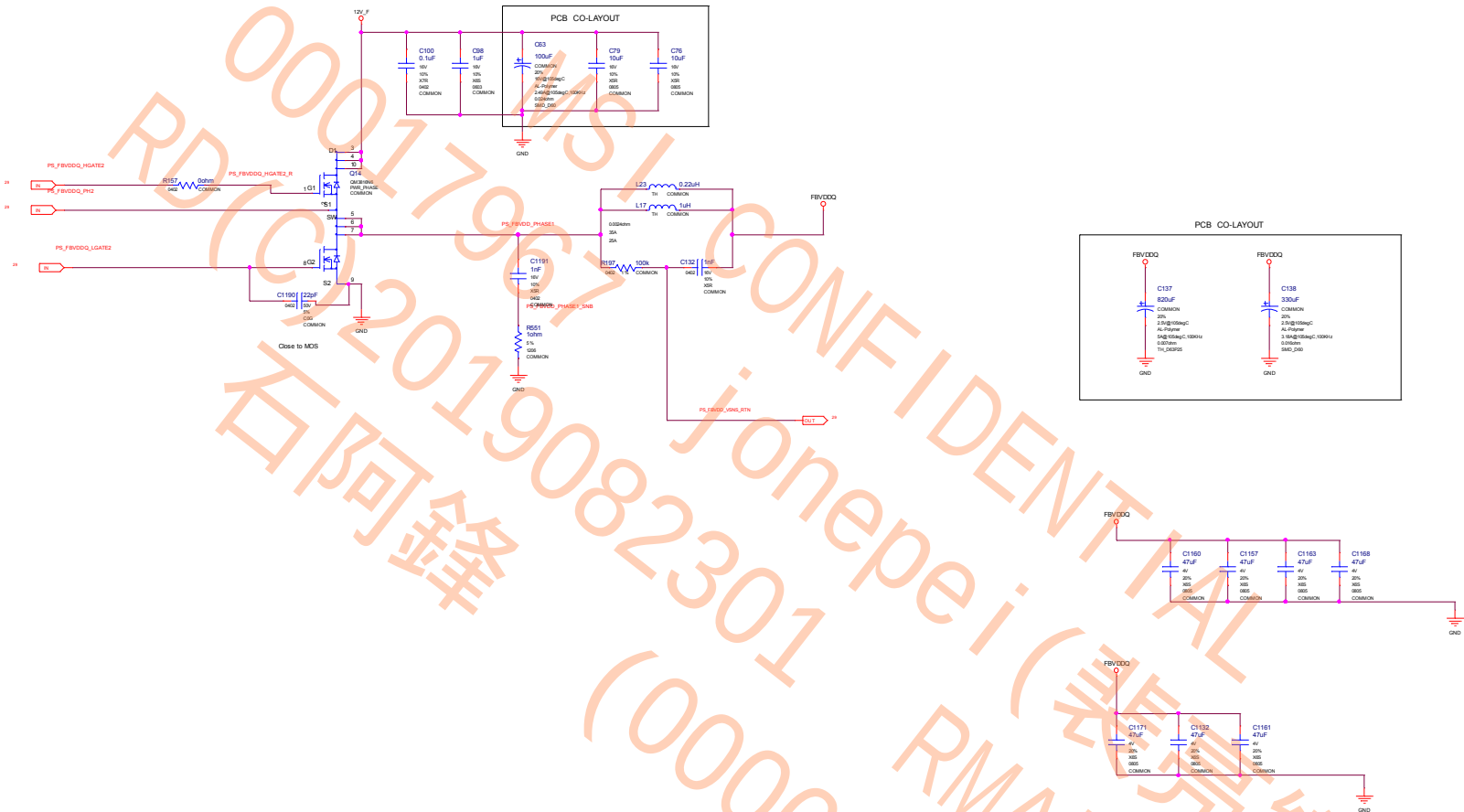




NO STUFF FOR G5

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PCB REV

PG165-A00

PCB REV

8

NV_PN

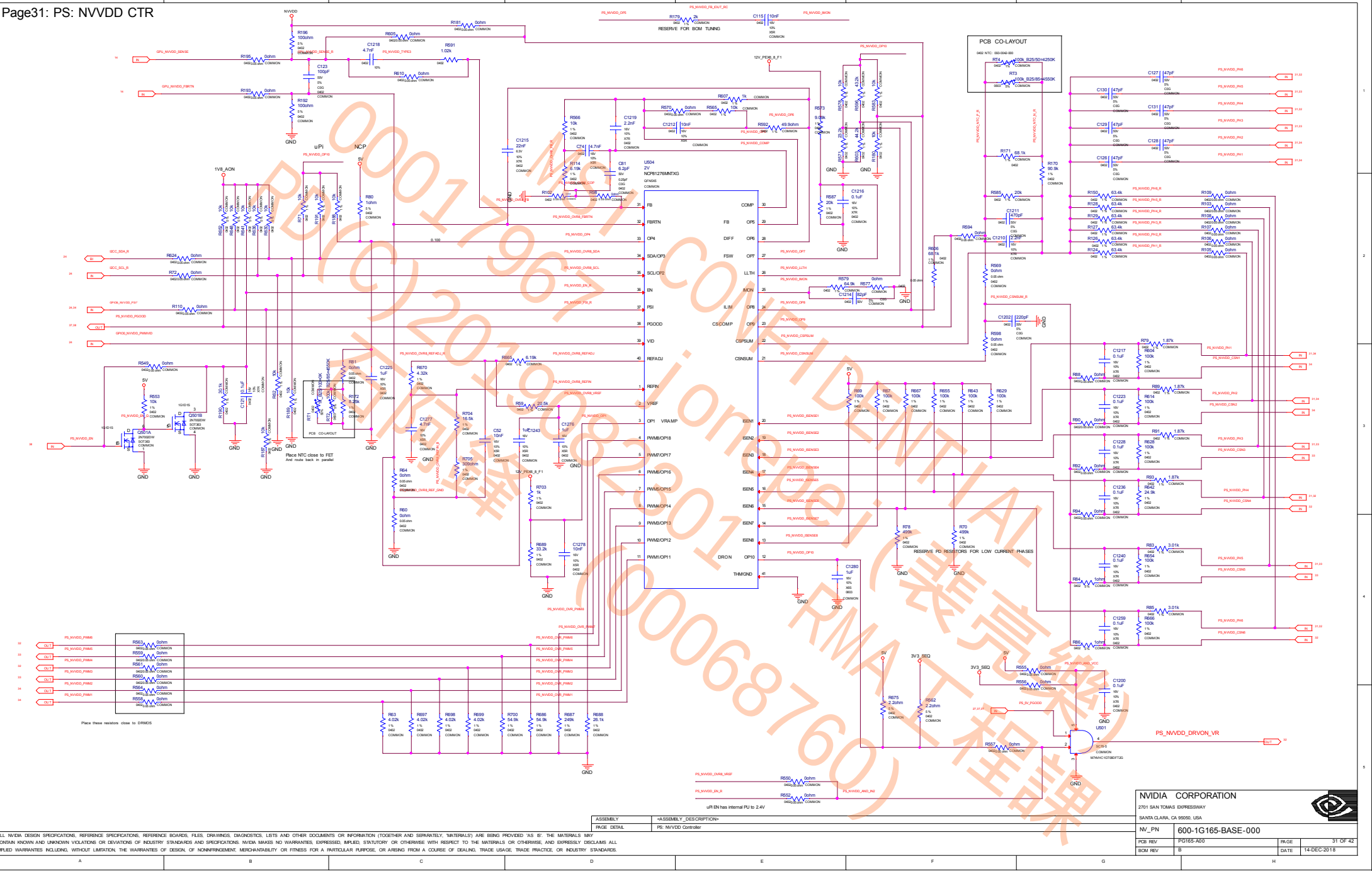
600-1G165-BASE-000

DATE

14-DEC-2018

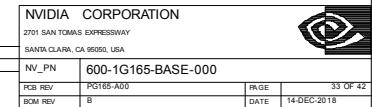
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A	B	C	D	E	F	G	H
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ASSEMBLY PAGE DETAIL	ASSEMBLY DESCRIPTION PS-NVVD Phase 3.5	SANTA CLARA, CA 95050, USA	
REV 35044MS ALL STANDARD		NV_PN 600-1G165-BASE-000	
		PCB REV P0165-A20	PAGE 33 OF 42
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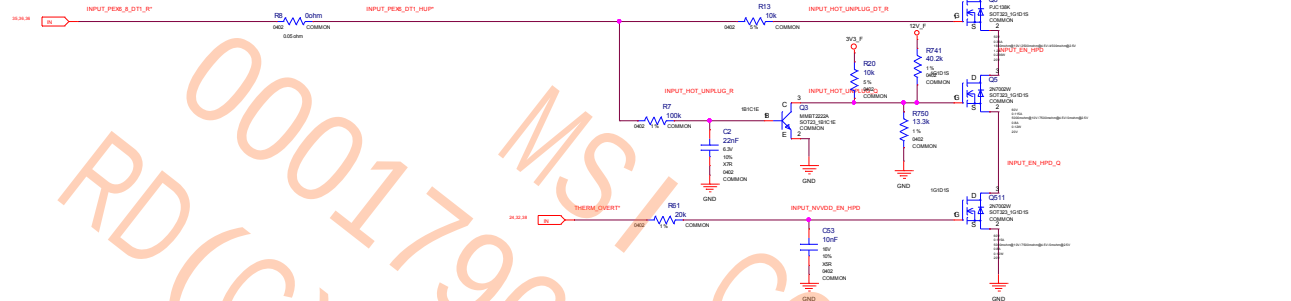


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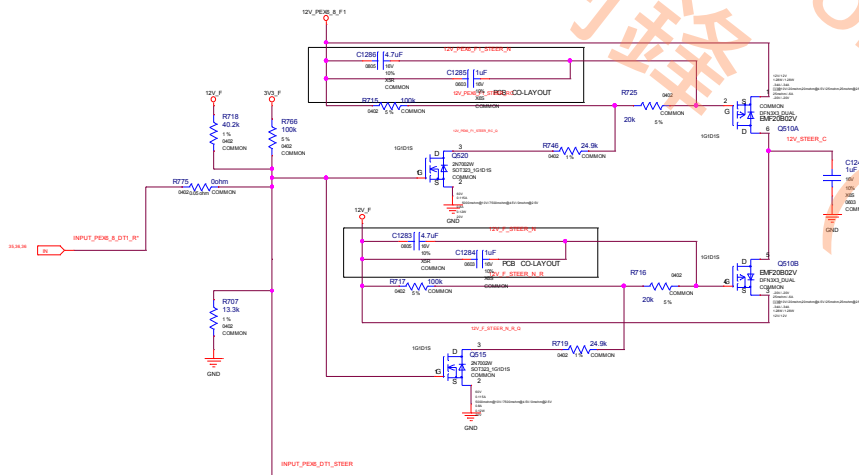
PEX Input Present 1

POWER CONNECTOR HOT-UNPLUG DETECT

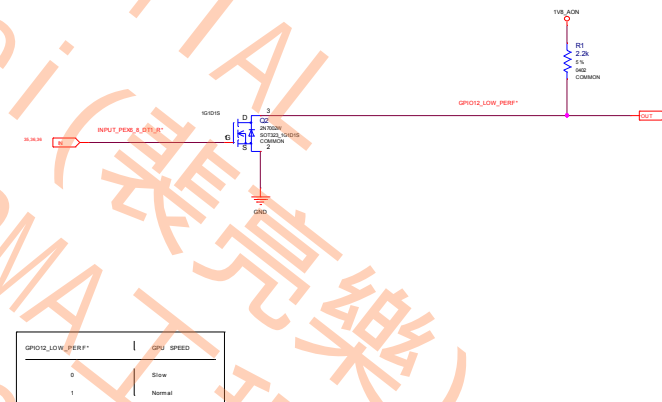


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



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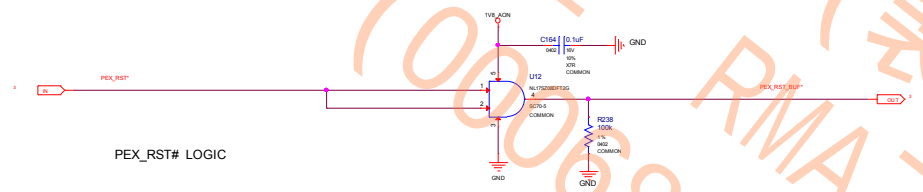
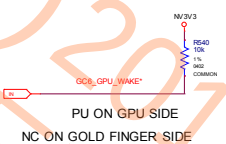


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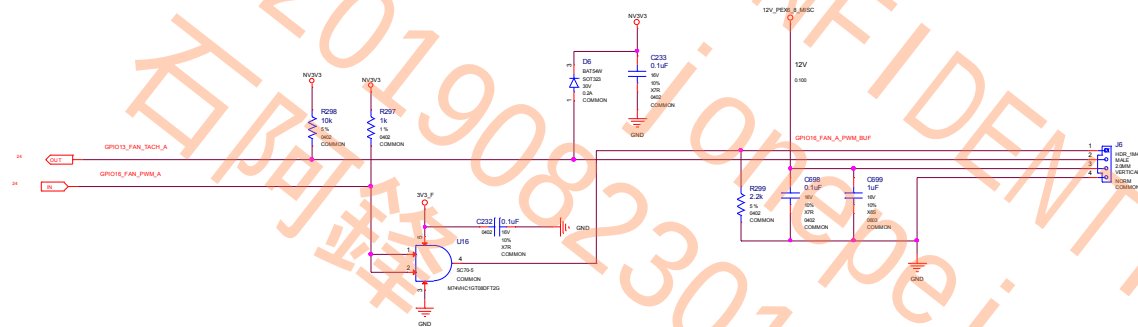
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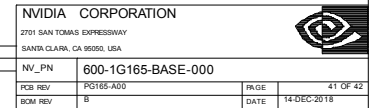
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PCB REV	PG165-A00	PRGE	39 OF 42
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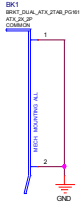
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ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	FAN

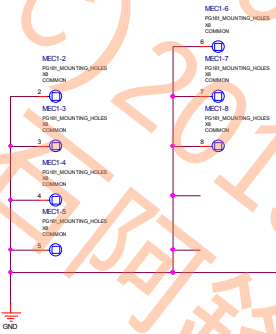
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NV_PN	600-1G165-BASE-000		
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Bracket:



MOUNTING HOLES FOR HS:



BACK STIFFENER:



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