

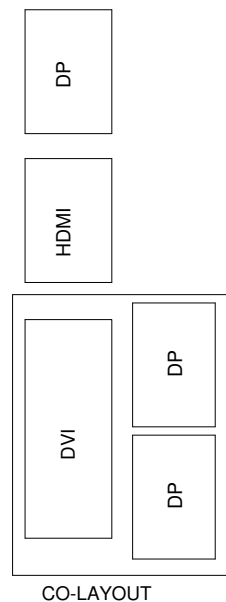
PG161-B00

TU106 8GB GDDR6, 192b, X16
DVI-D + DP + HDMI

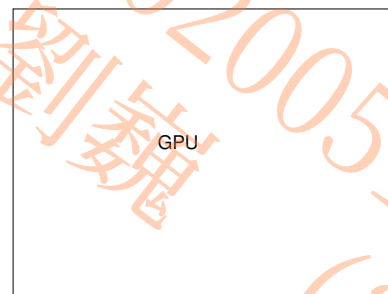
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POWER SUPPLY



MEM D
LO

MEM D
HI

MEM C
LO

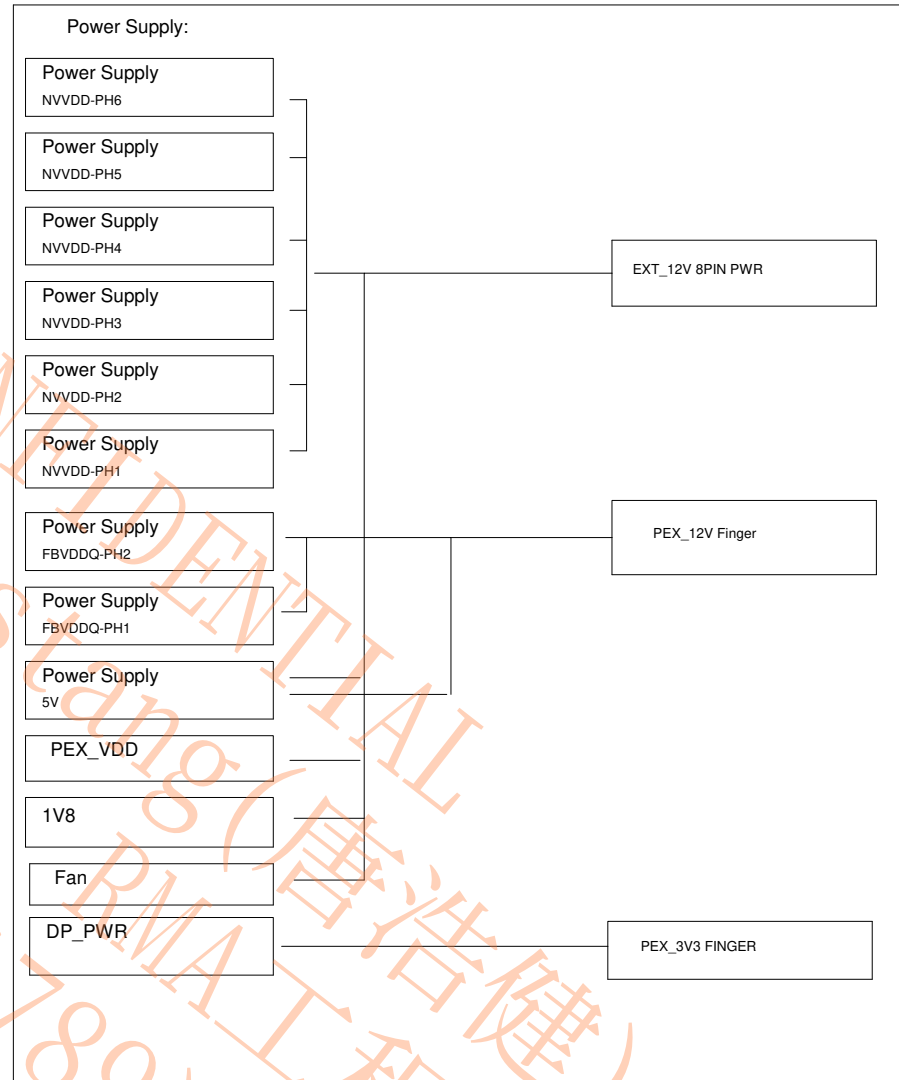
MEM C
HI

MEM B
LO

MEM B
HI

MEM A
HI

MEM A
LO

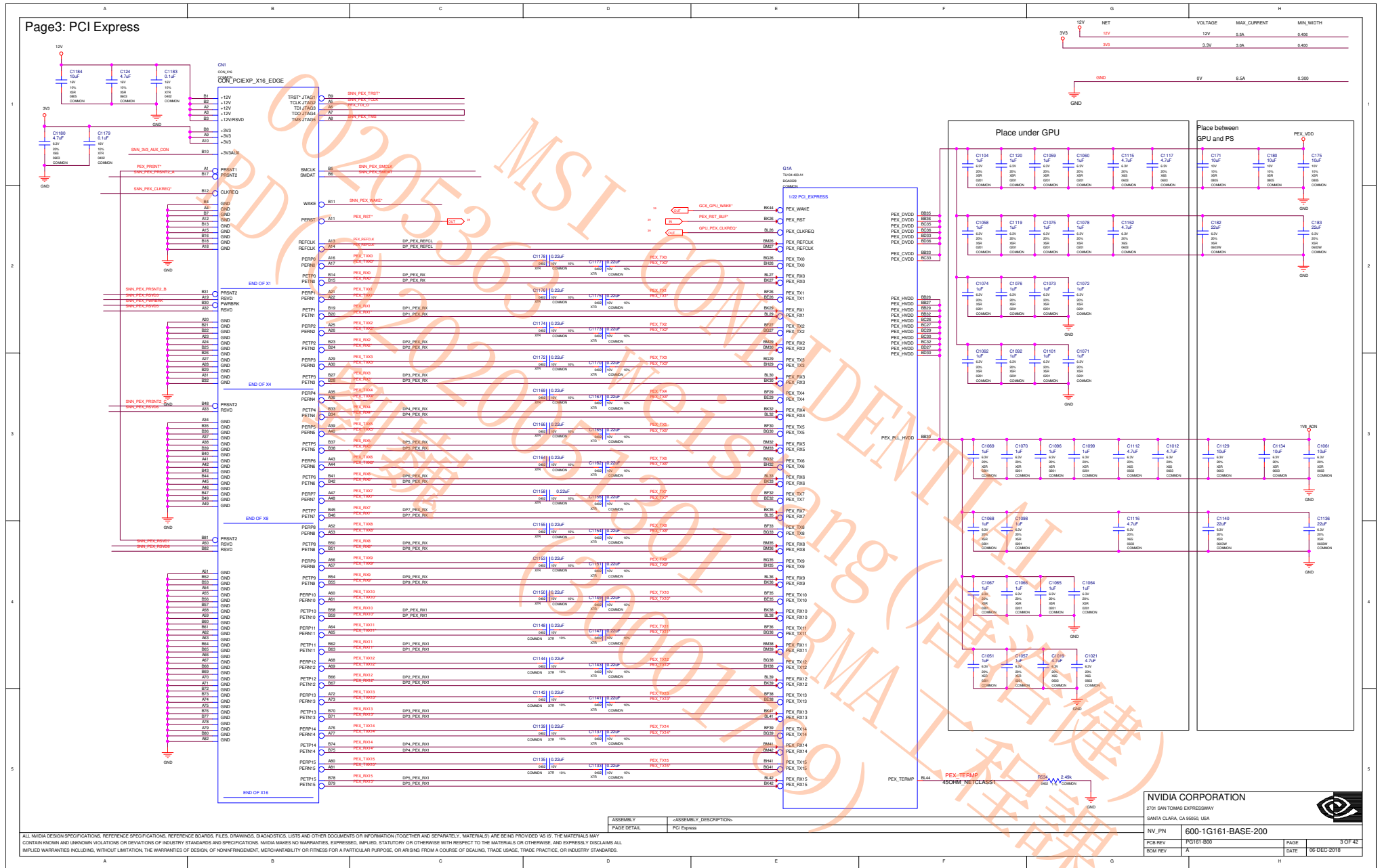


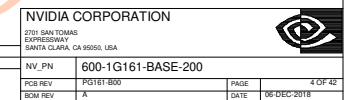
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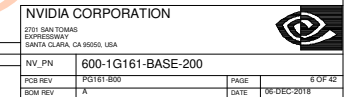
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PAGE DETAIL

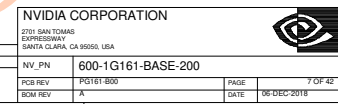
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Block Diagram

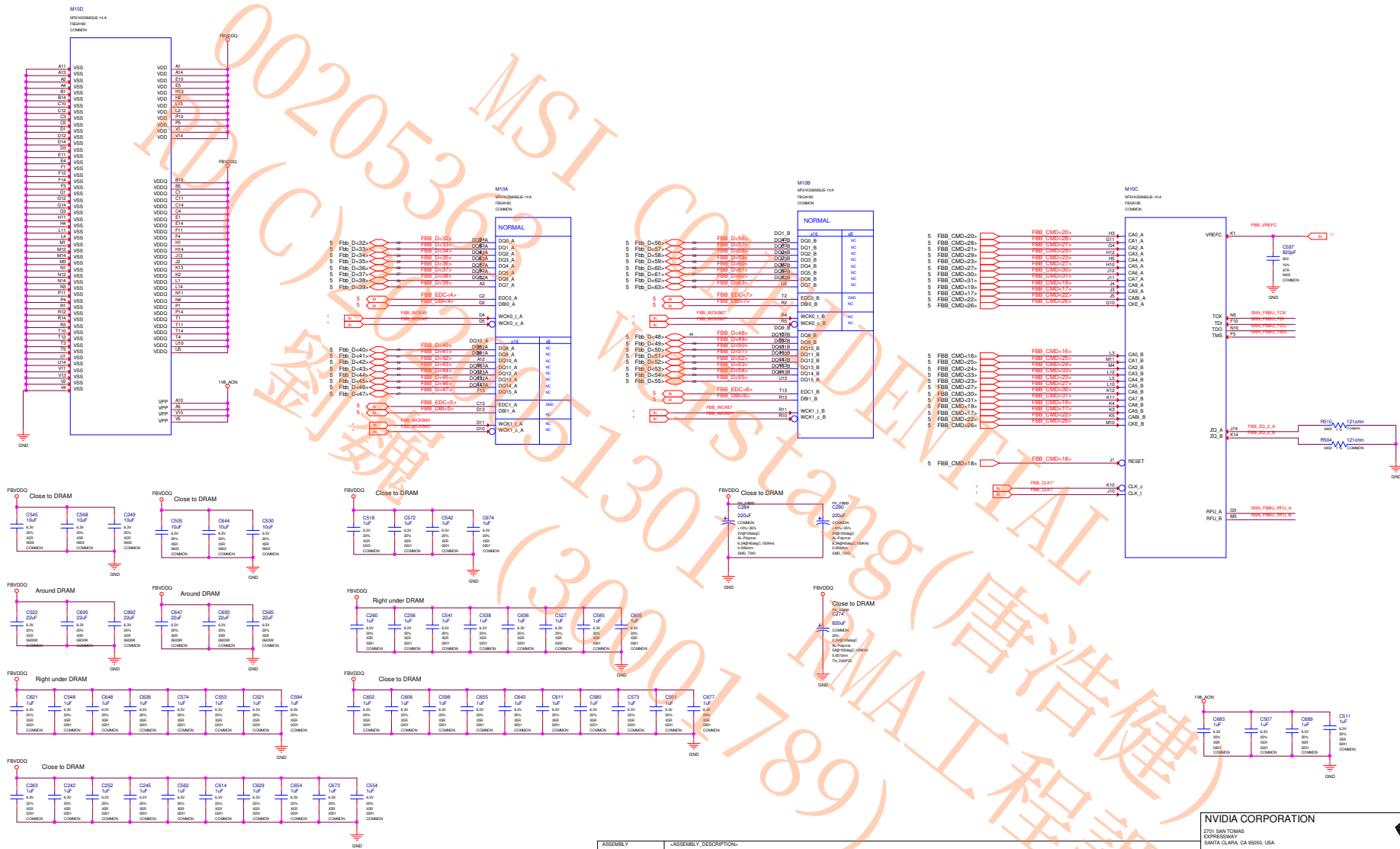
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NV_PN	600-1G161-BASE-200		
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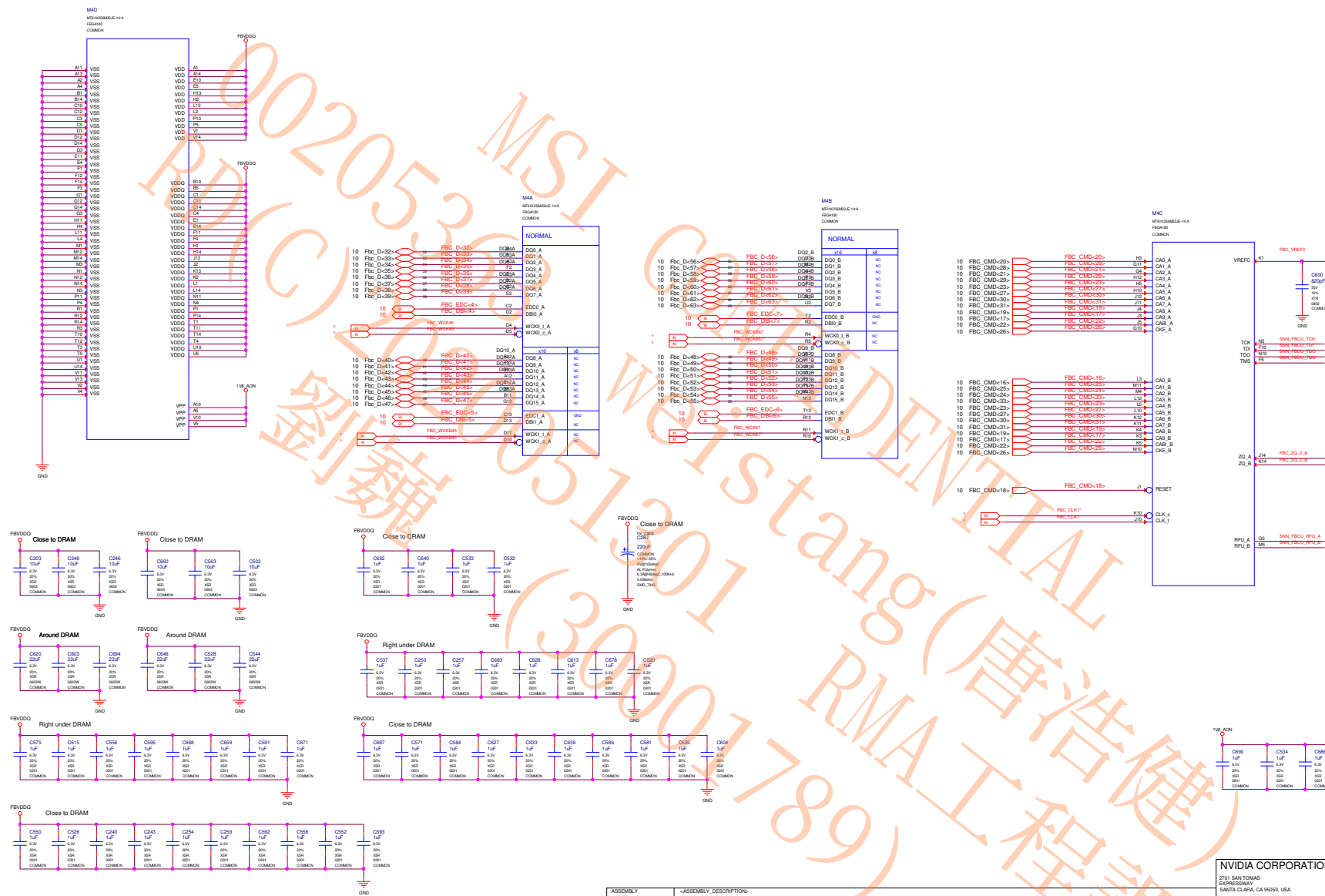




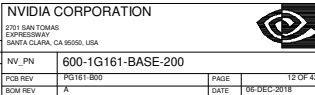


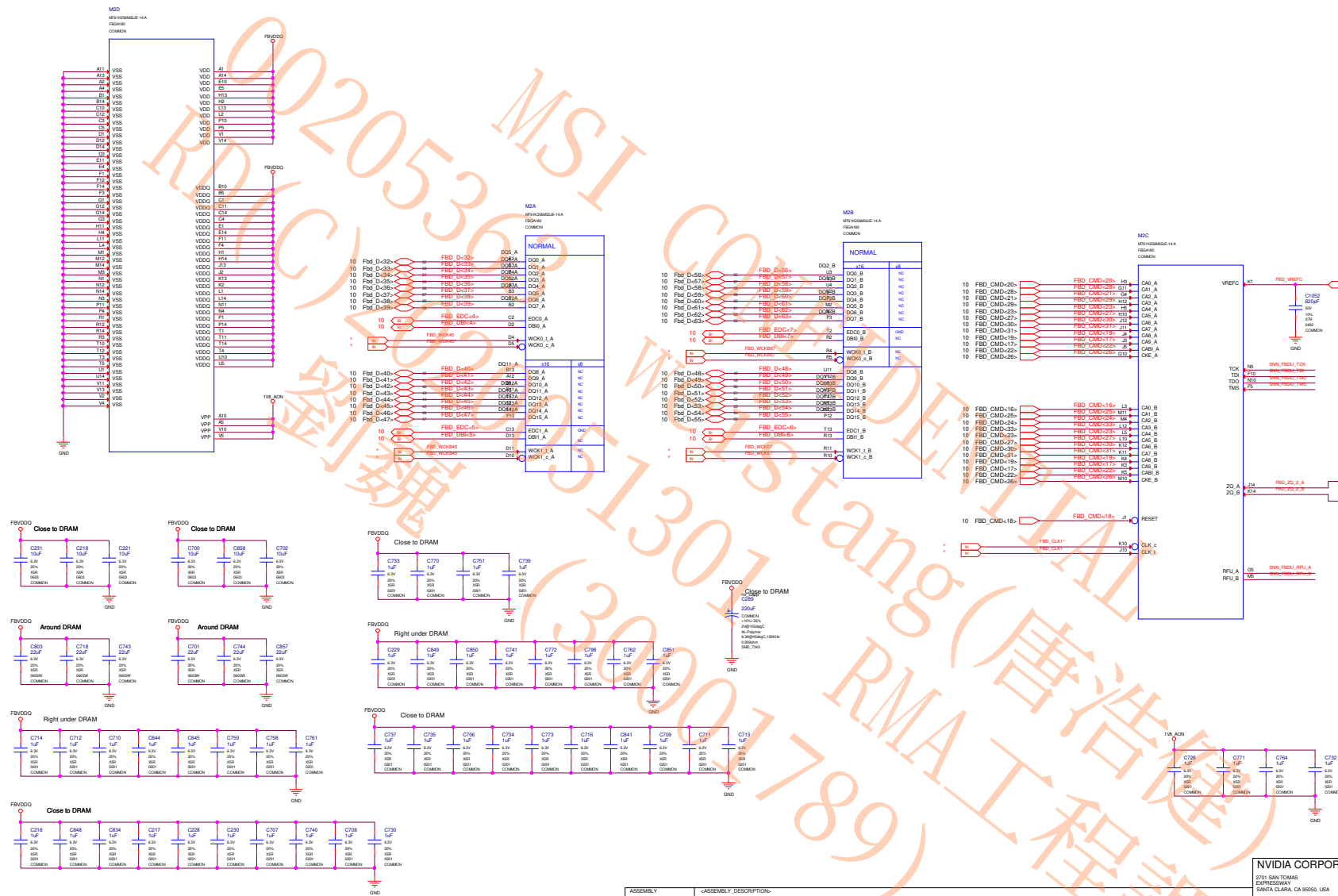


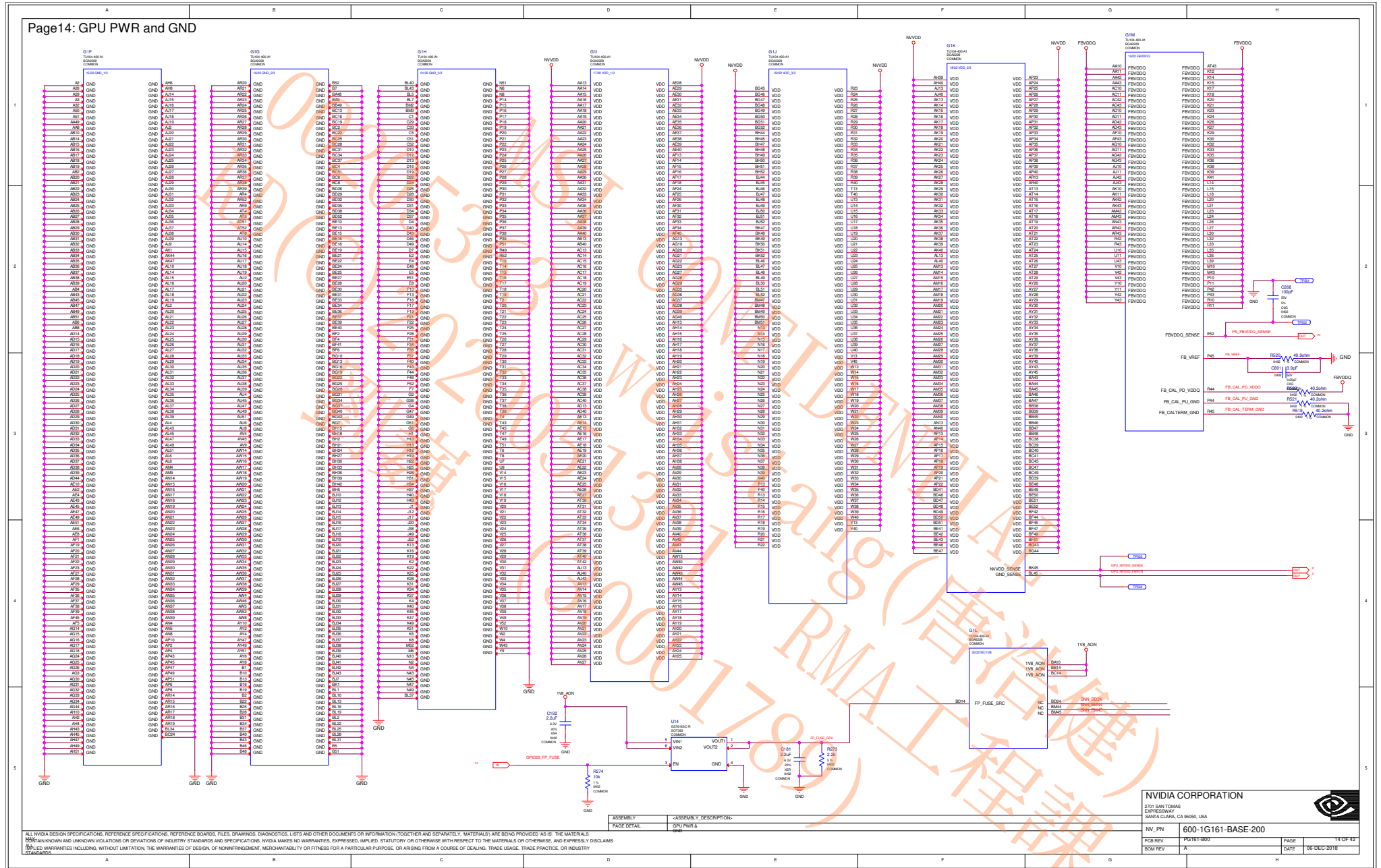




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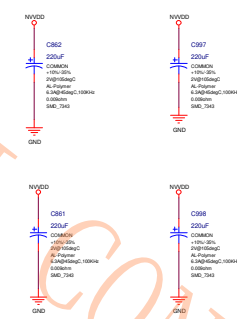




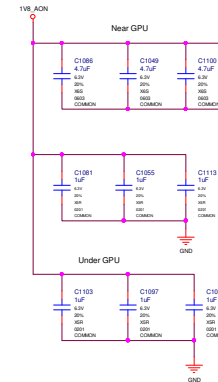
FBVDDQ



NVVD



1V8_AON



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	GPU DECOUPLING 1

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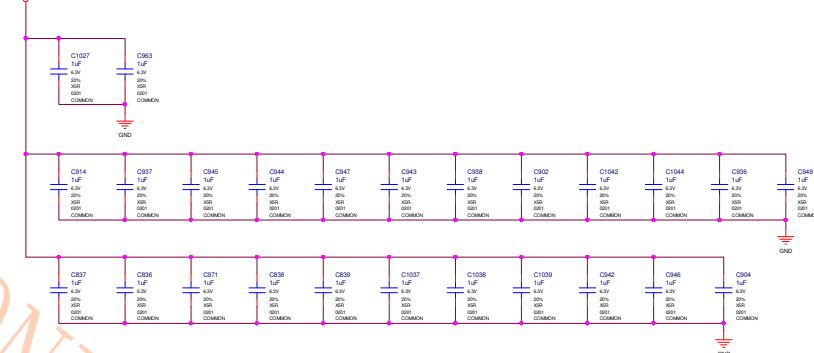
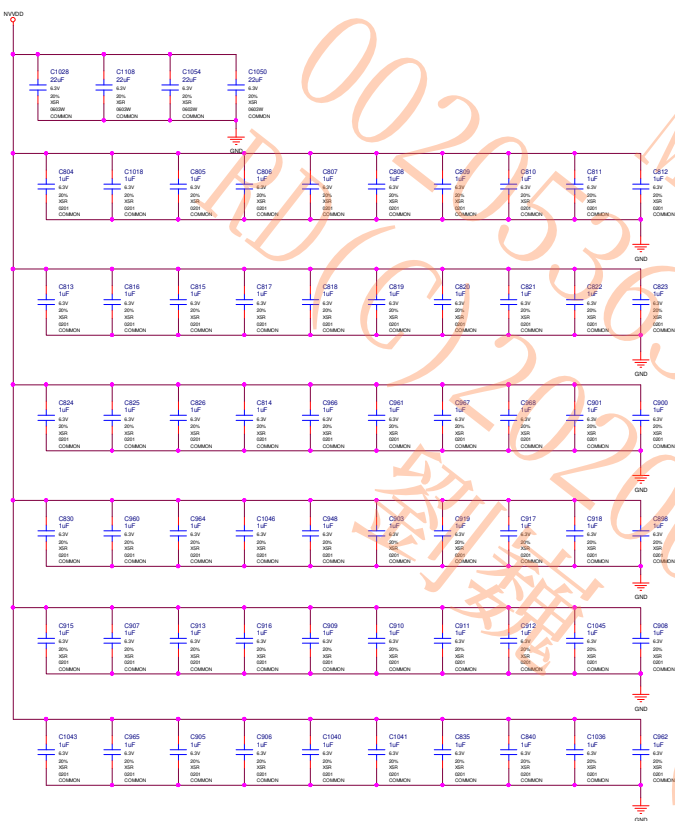
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PAGE DETAIL	GPU DECOUPLING 2

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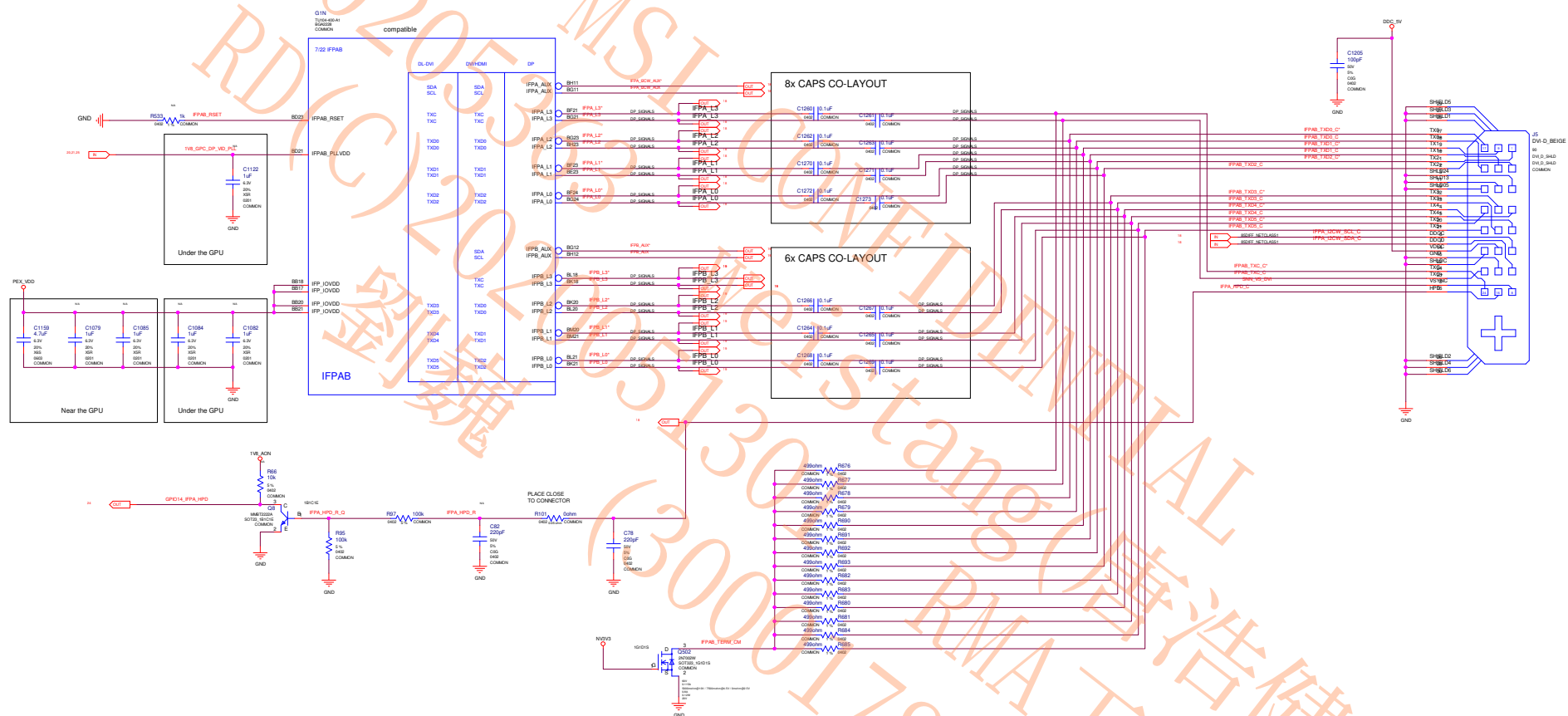


NV_PN	600-1G161-BASE-200
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PCB REV	1.0
BOM REV	A

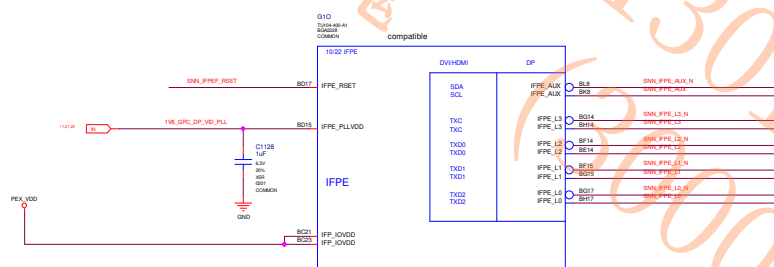
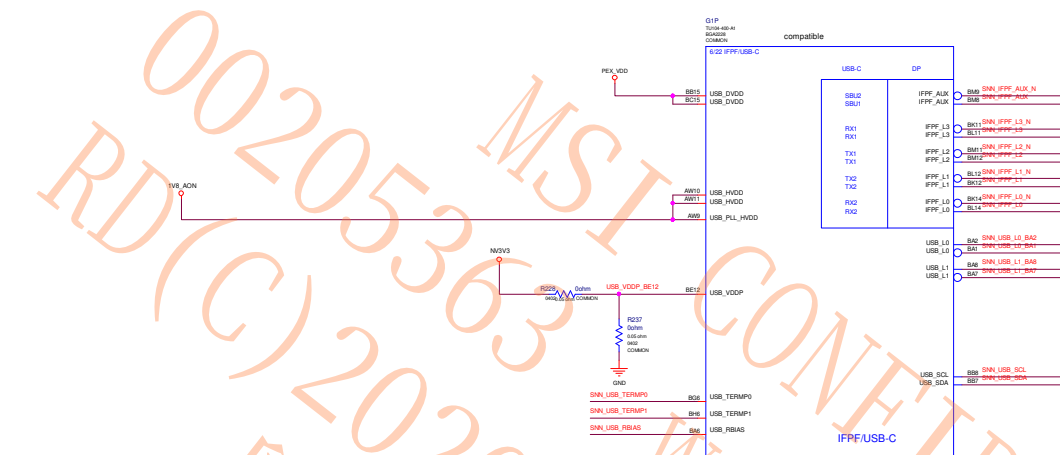
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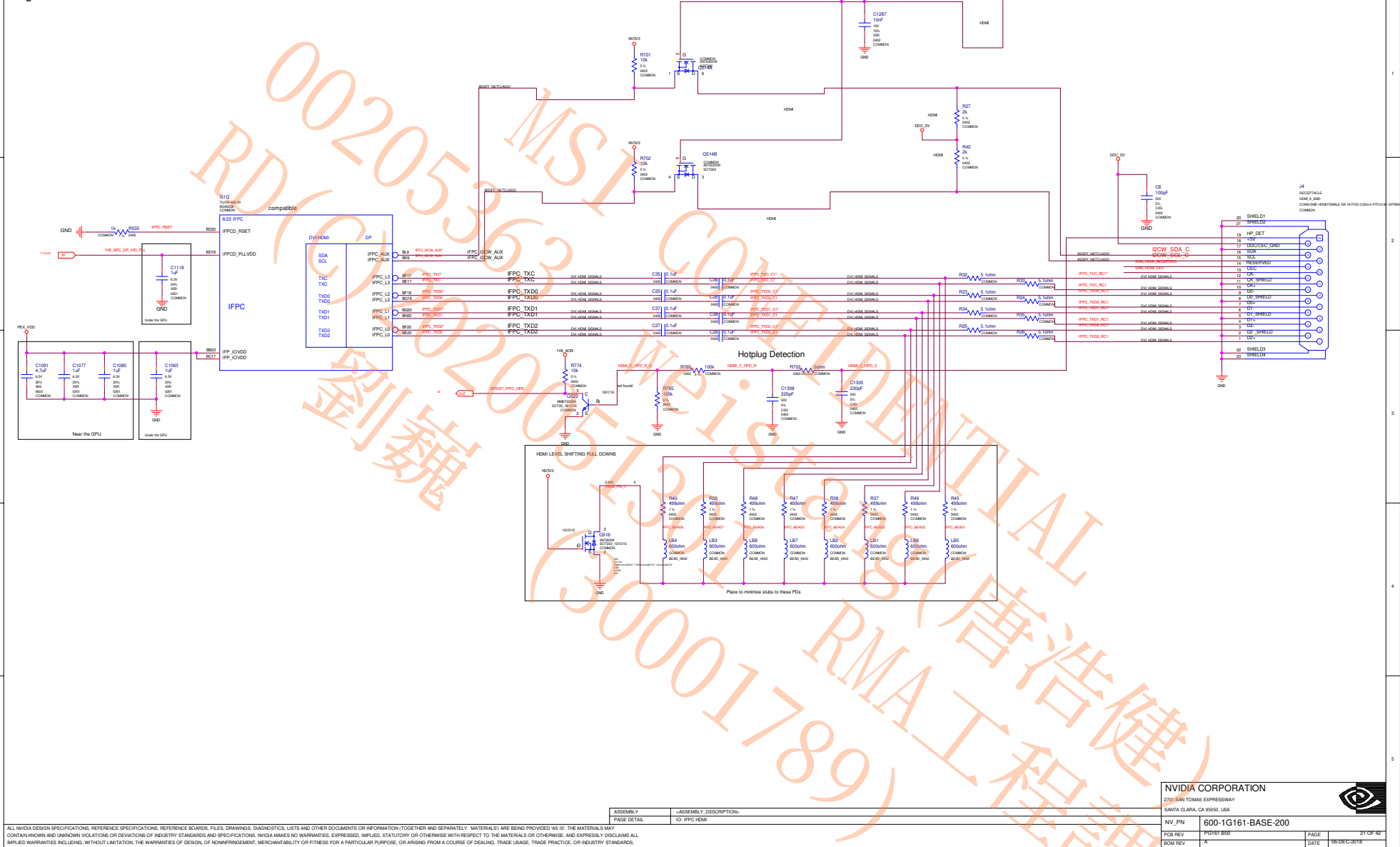


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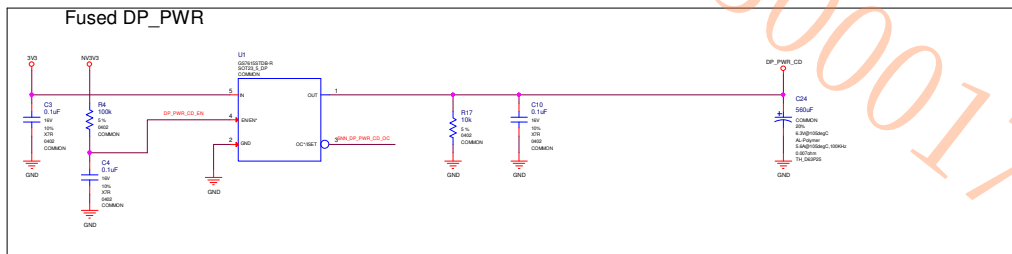
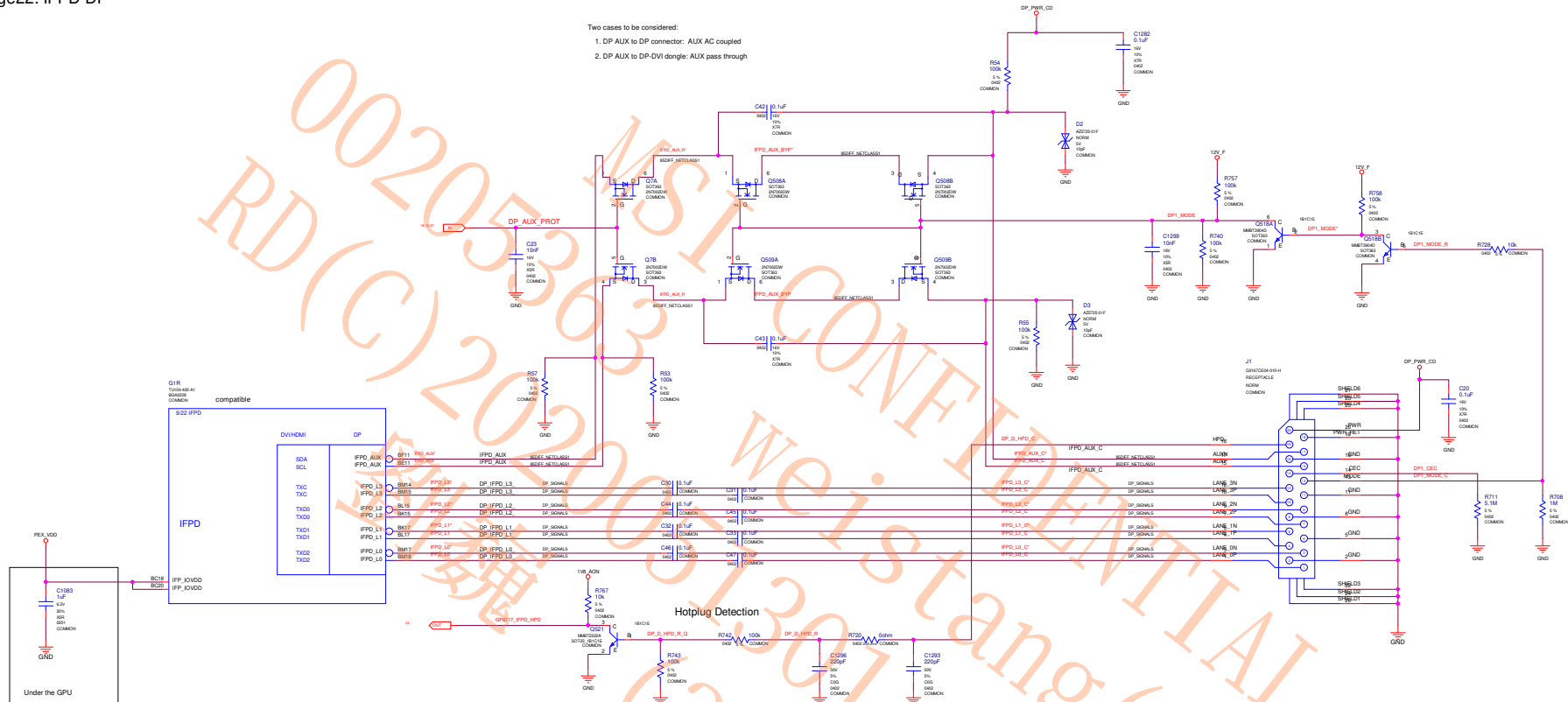
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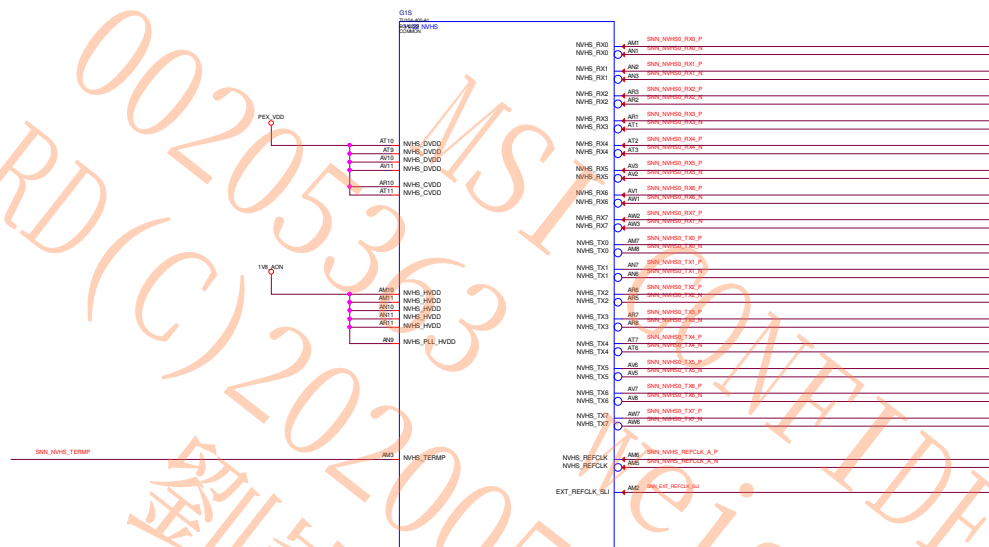
- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

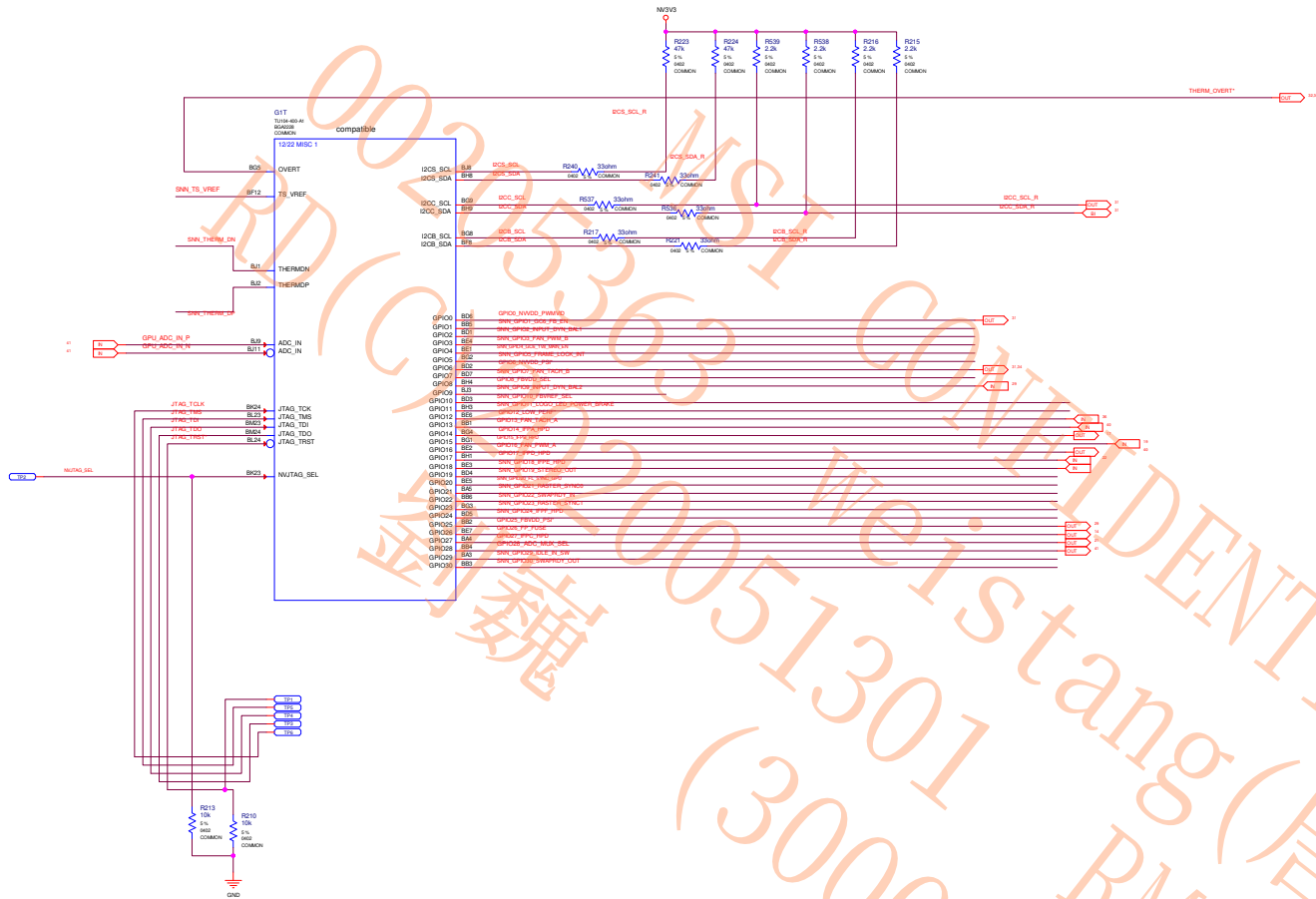


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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	IO: IFPD DP

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	MISC1: JTAG, GPIO, ADC, I2C, OVERT

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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

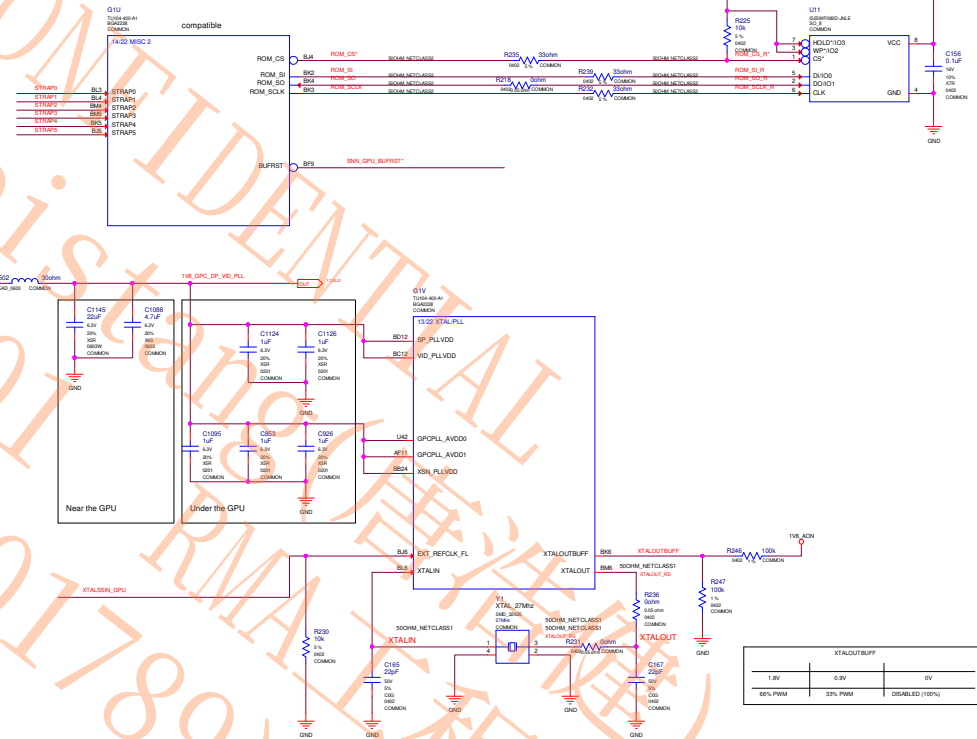
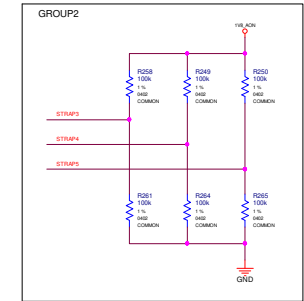
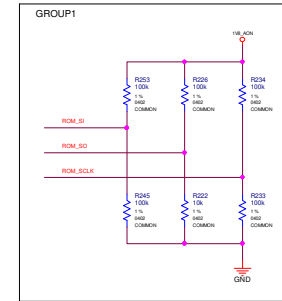
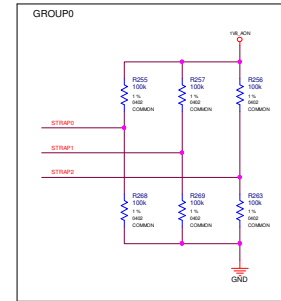
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

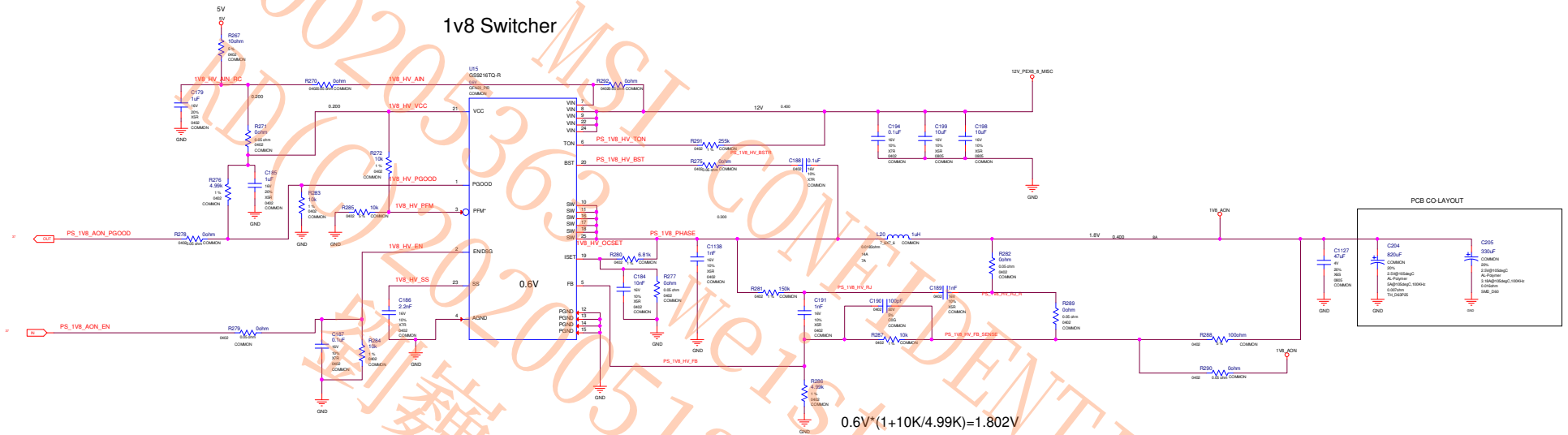
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE





ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PS: 1V8_AON

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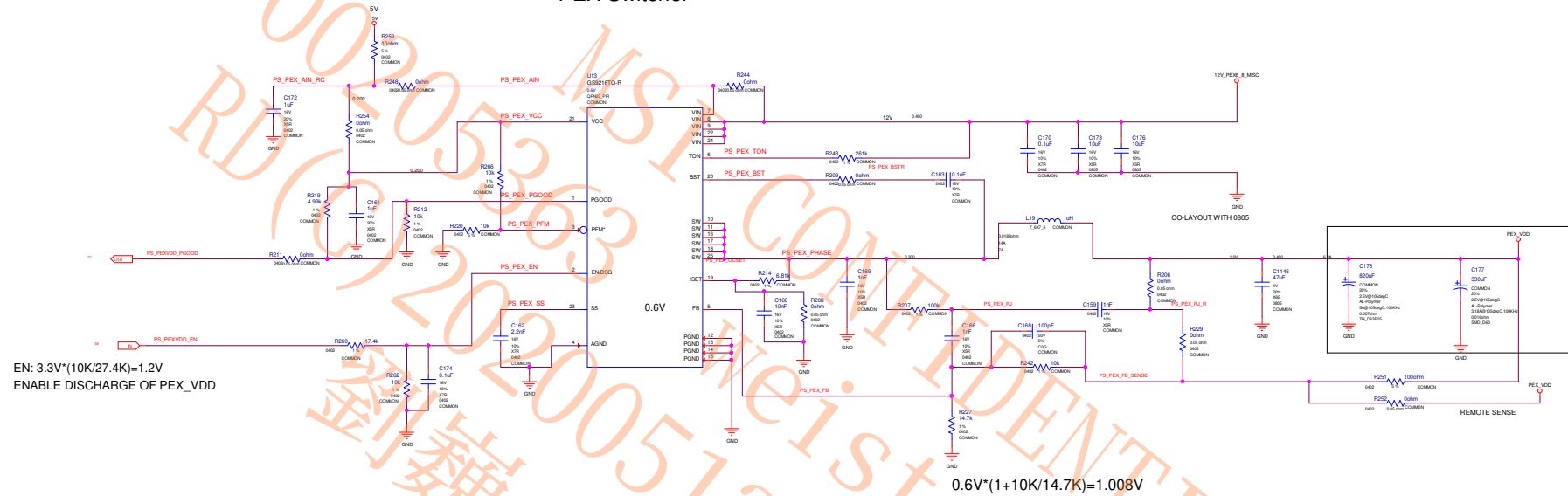
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PEX Switcher



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PAGE DETAIL PS: PEXVDD

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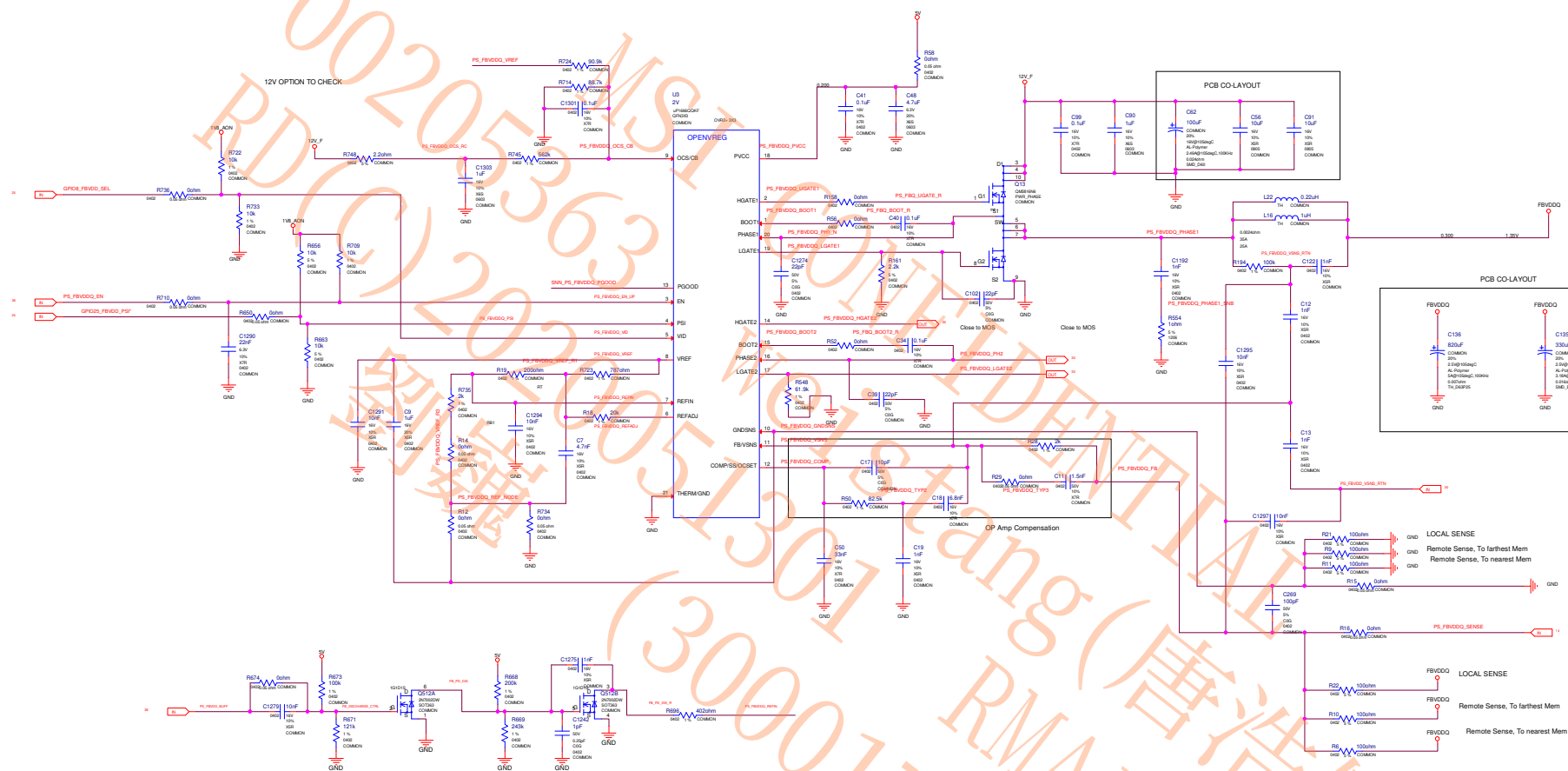
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDDQ

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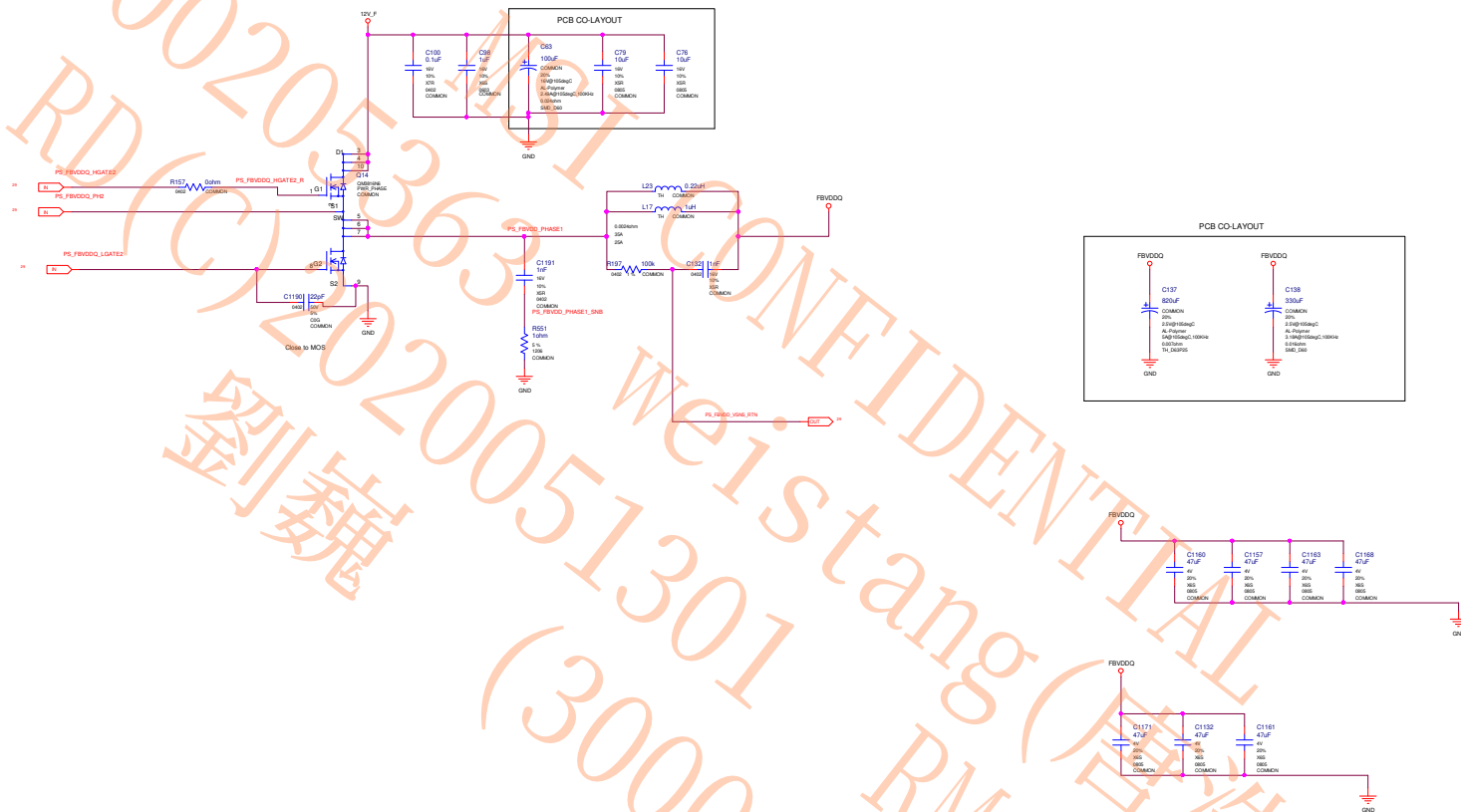
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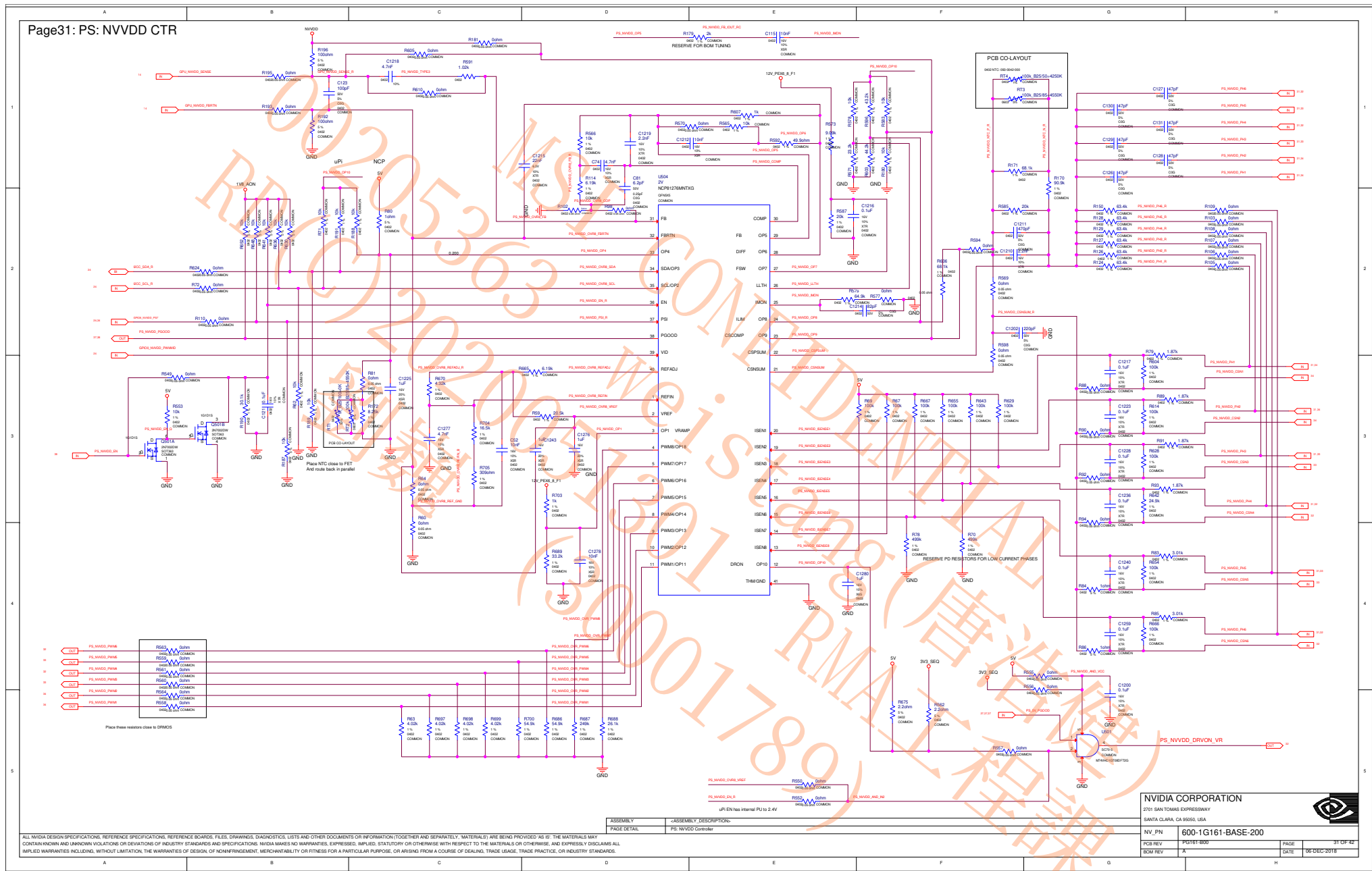
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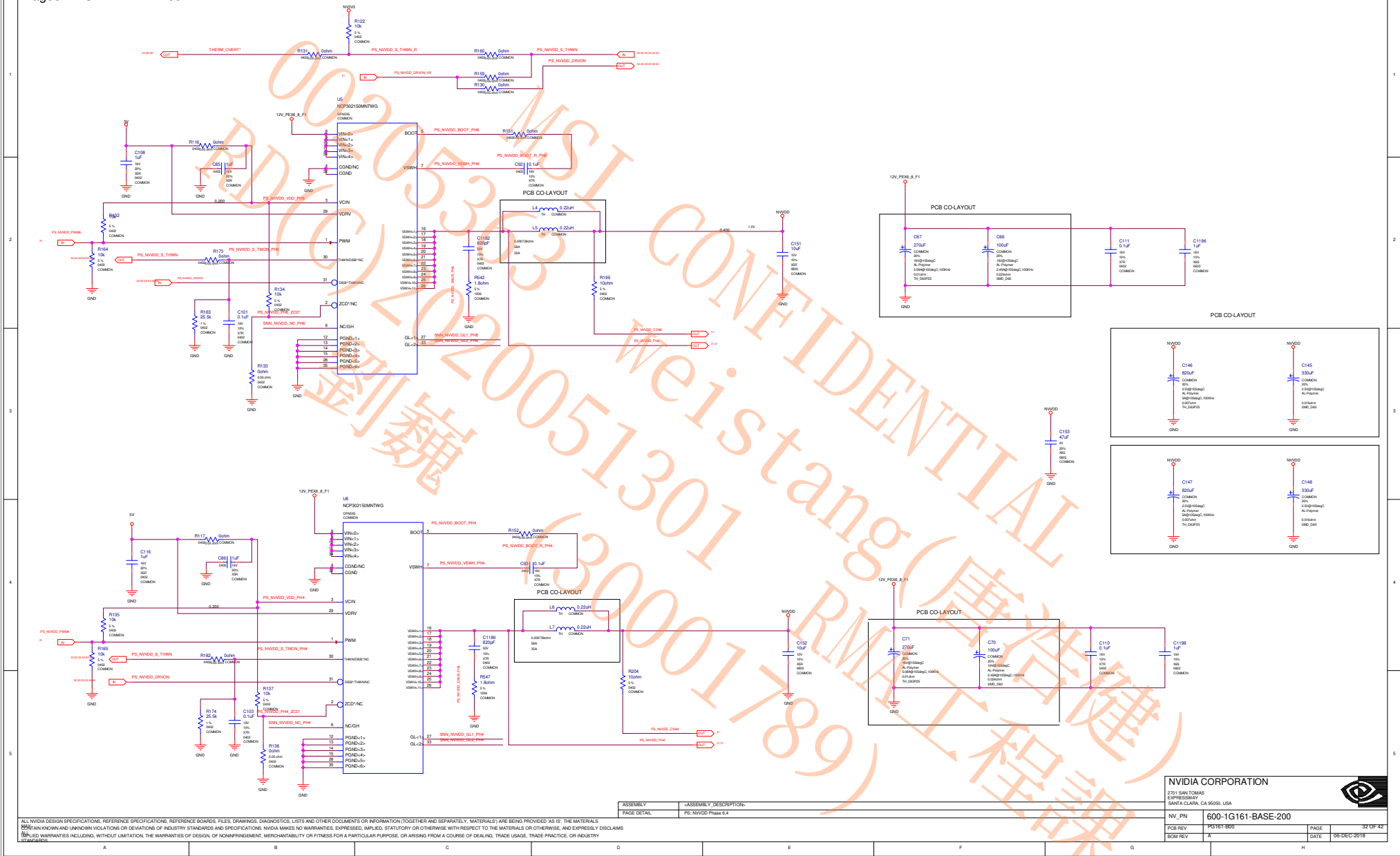
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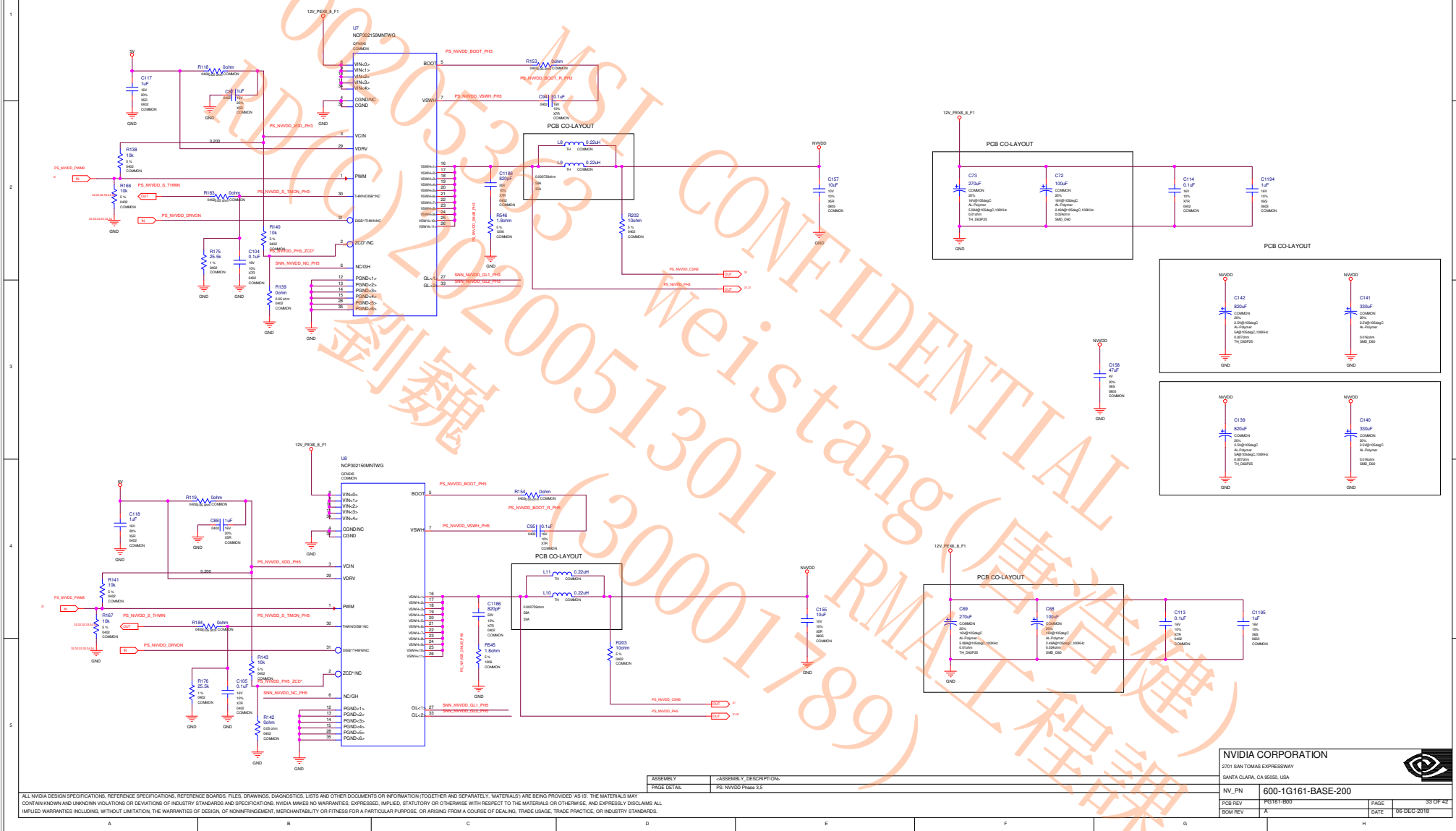
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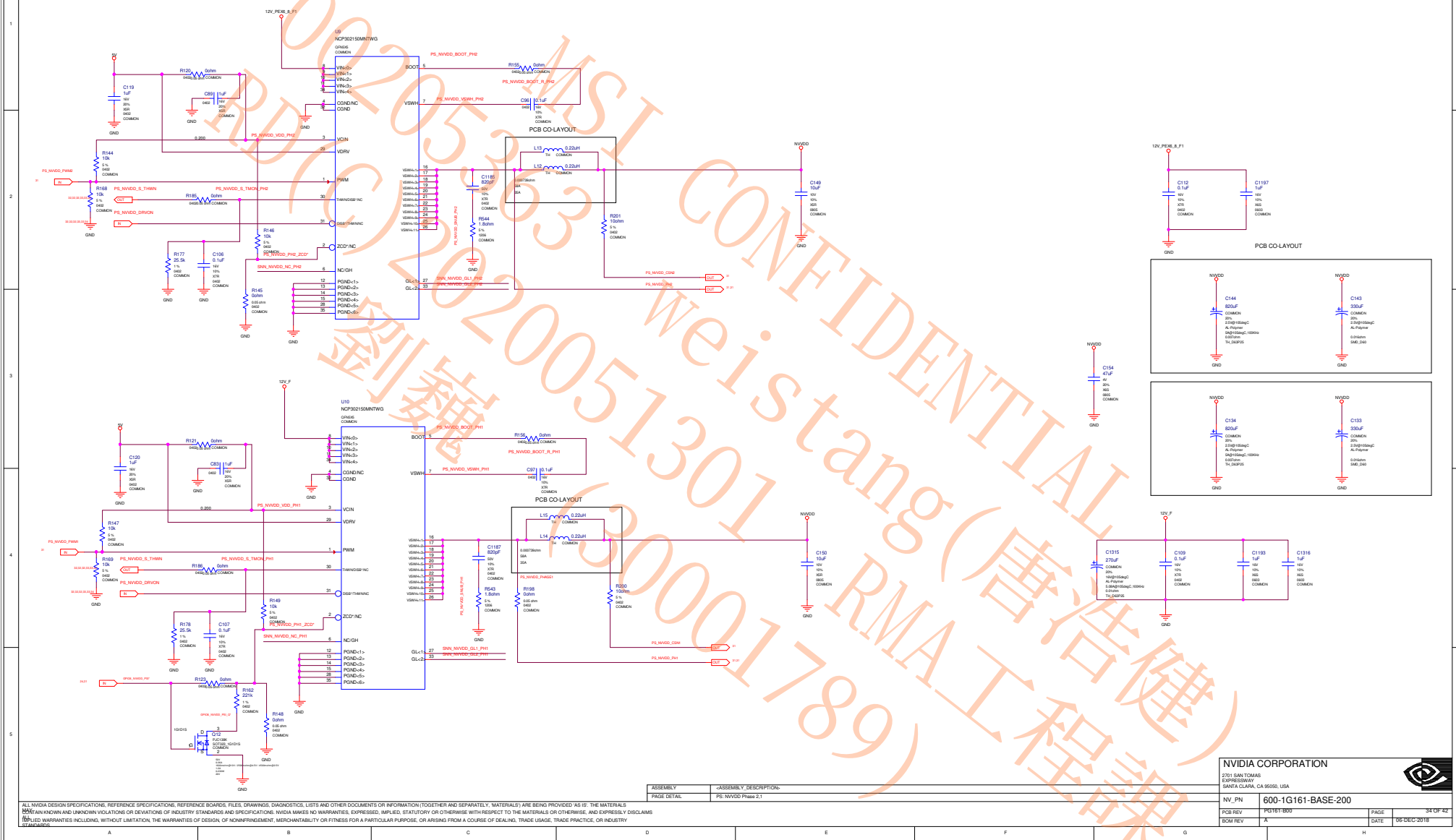


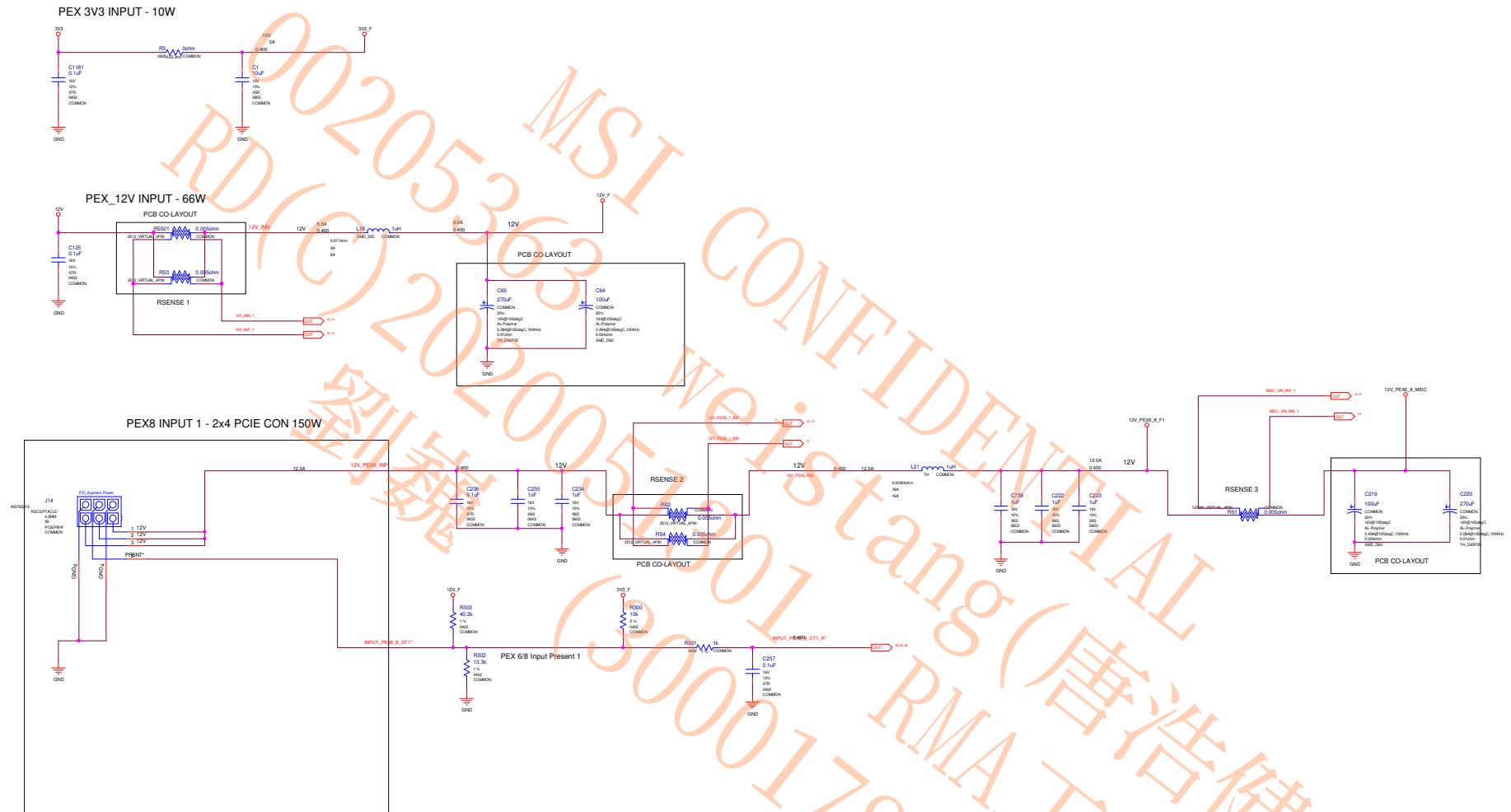
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PCB DETAIL PCB: P8000-PR2		NY_PN 600-1G161-BASE-200		PCB REV P0111-B00	
DATE 06 DEC 2018		PCB REV P0111-B00		DATE 06 DEC 2018	











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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	PS: PEX_INPUT, 12V_EXT_INPUT, FILTERING

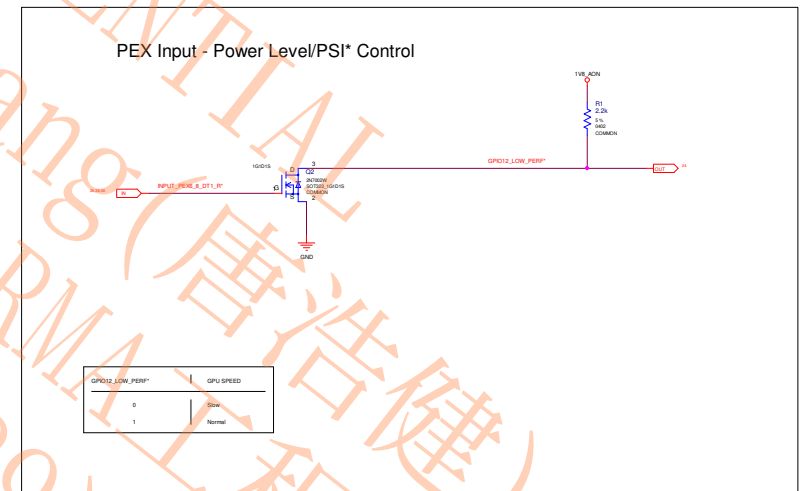
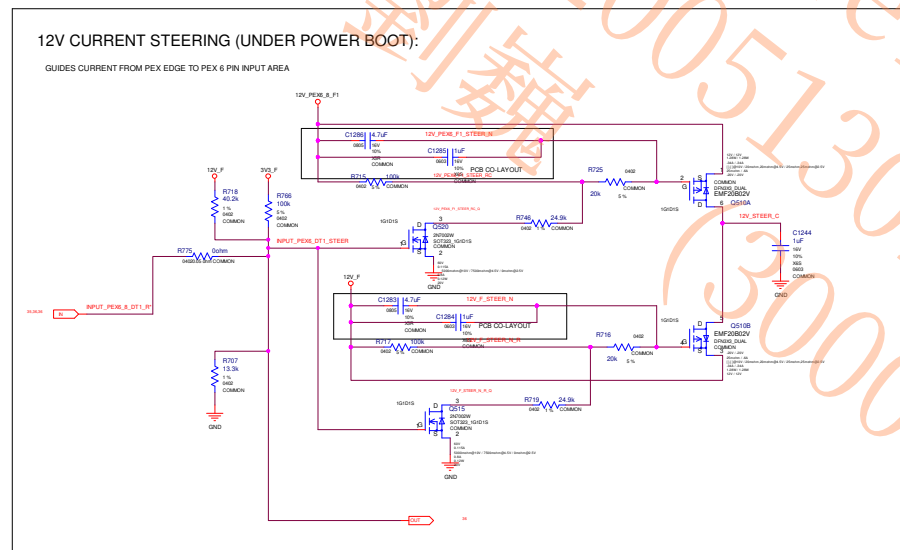
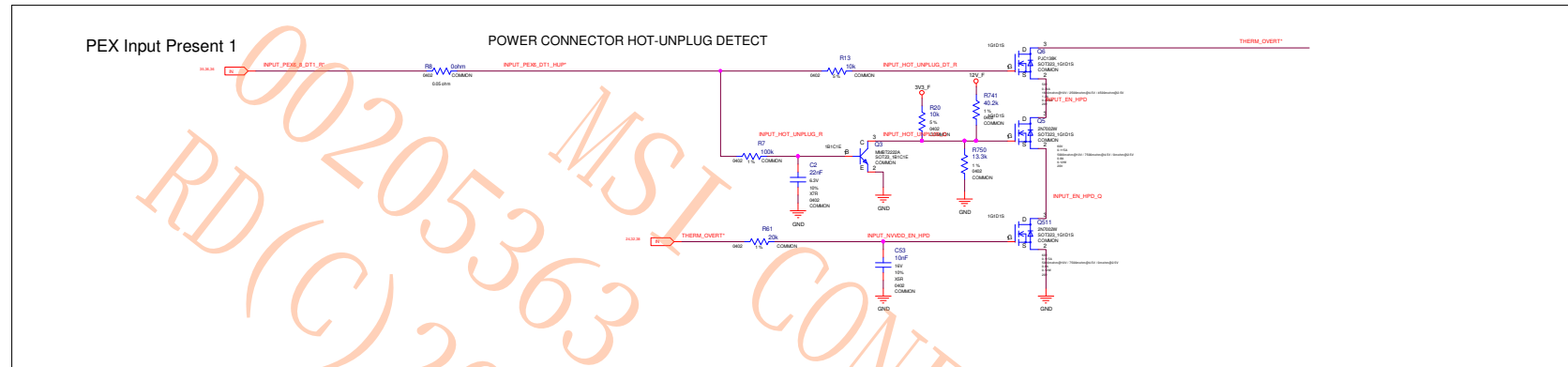
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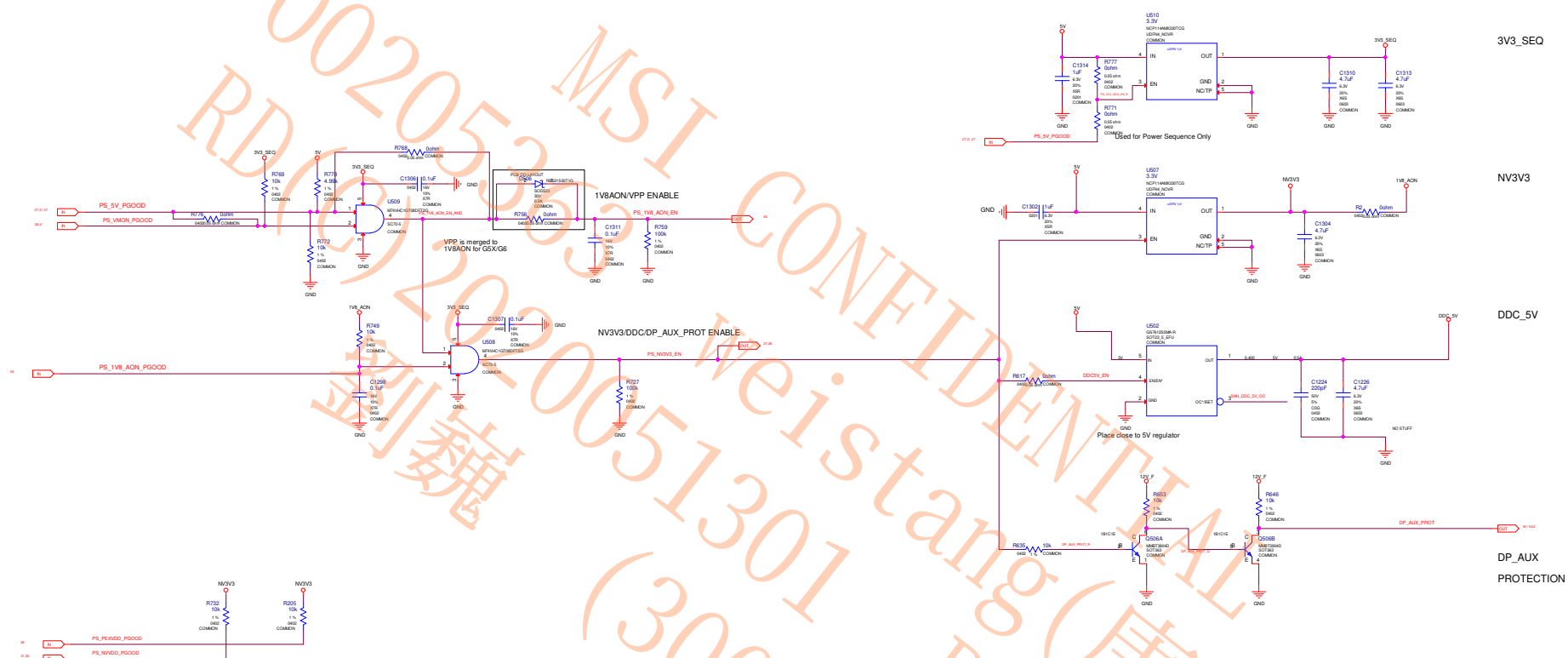
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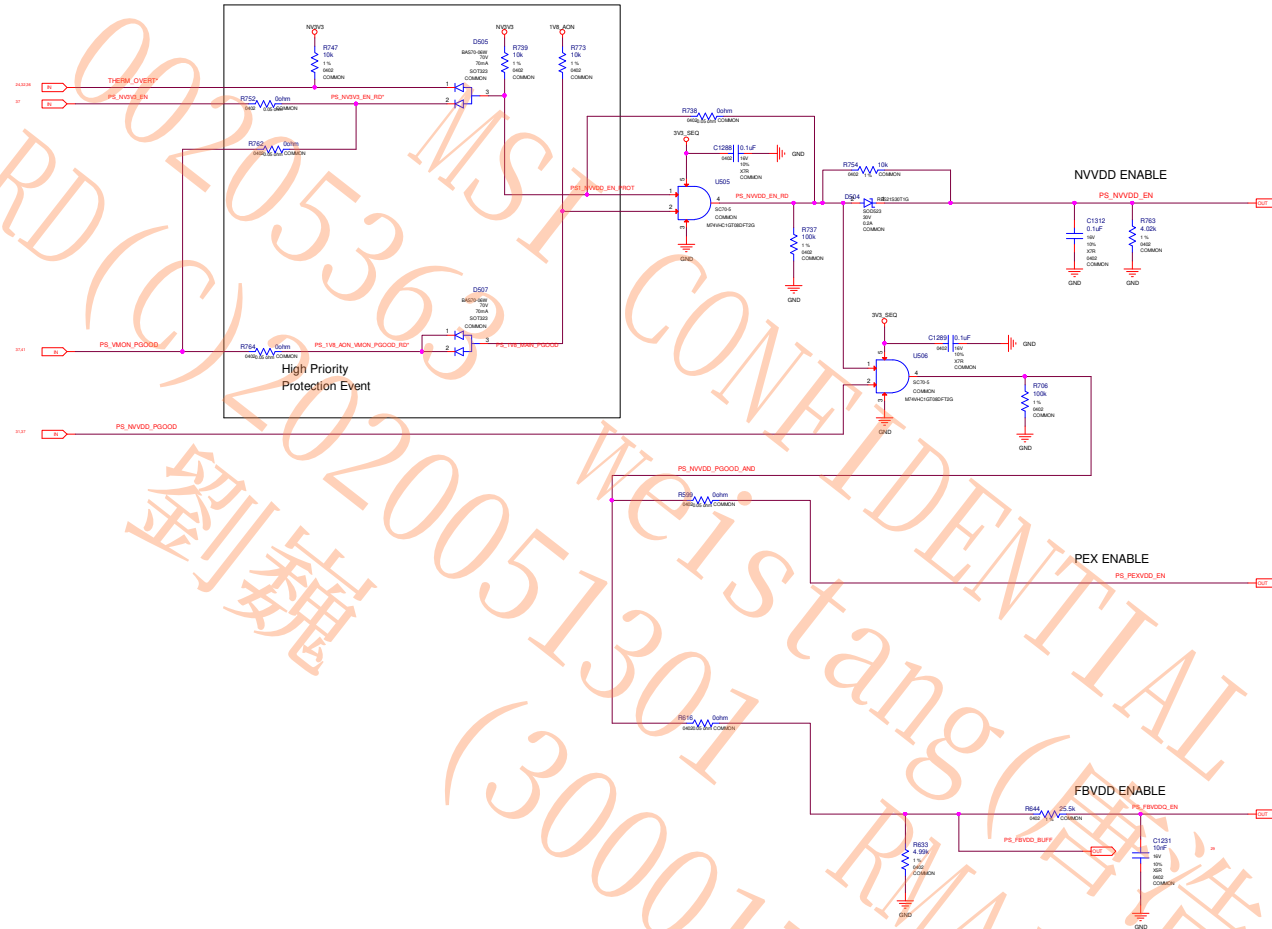
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Figure 1 shows a horizontal beam of total length L . The beam is divided into three segments of length H , $L/2$, and H from left to right. A pin support is located at the left end ($x=0$), and a roller support is located at the right end ($x=L$). A uniformly distributed load q is applied downwards over the entire length of the beam. The coordinate x is measured from the left end, and the vertical displacement w is measured downwards from the horizontal axis.



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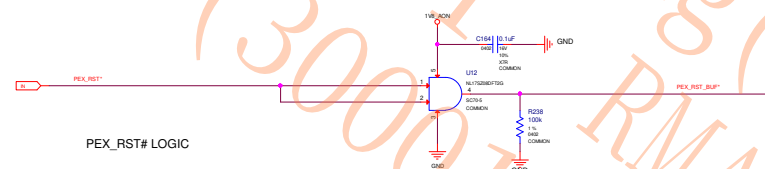
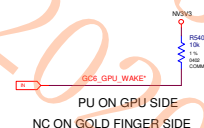
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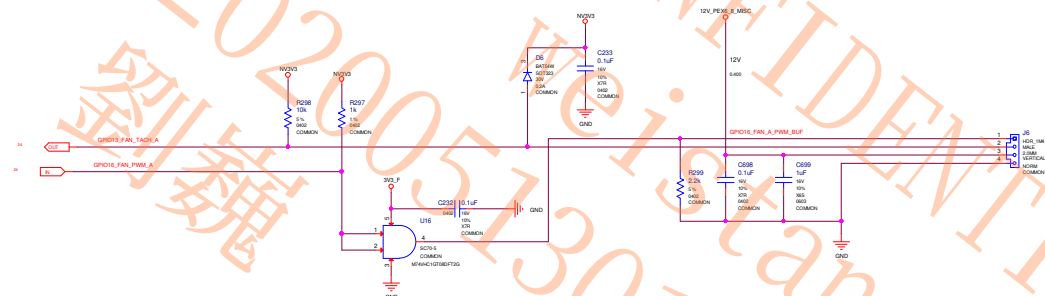




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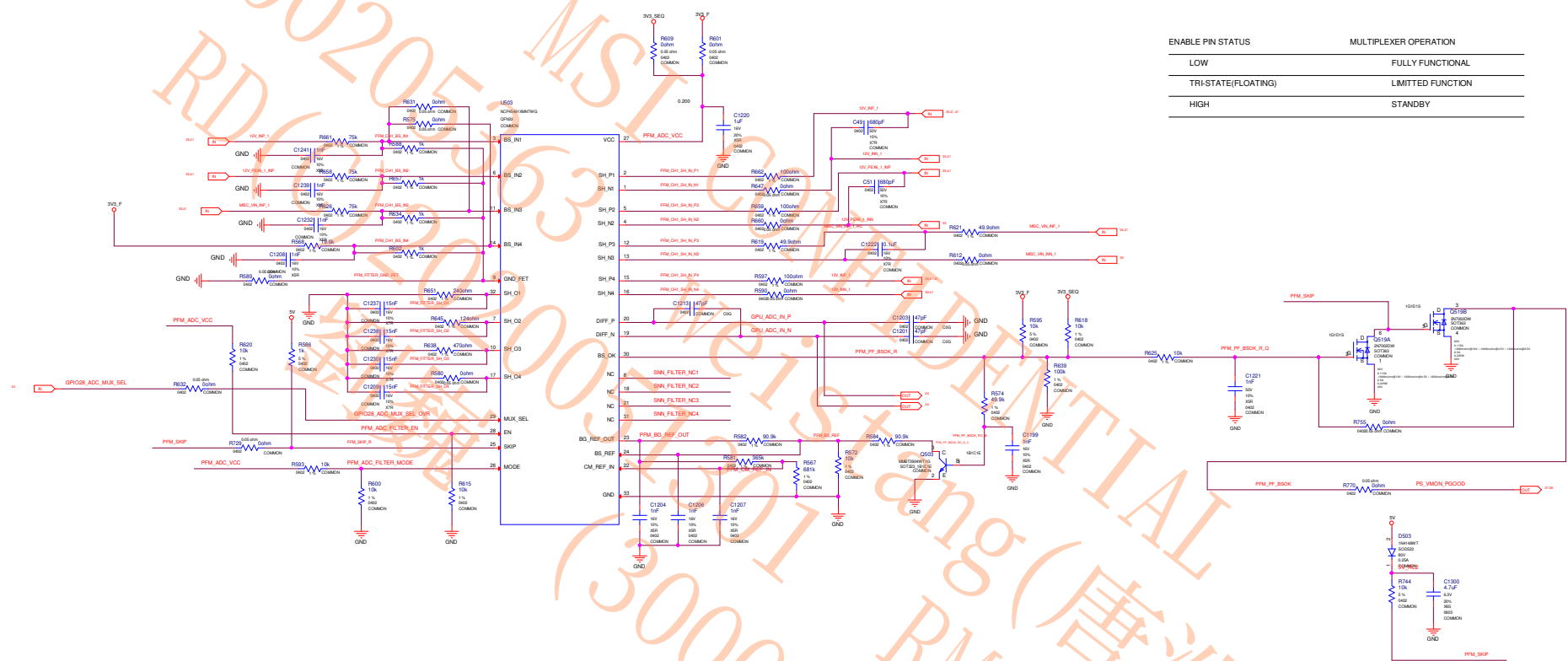


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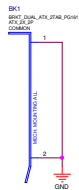


MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

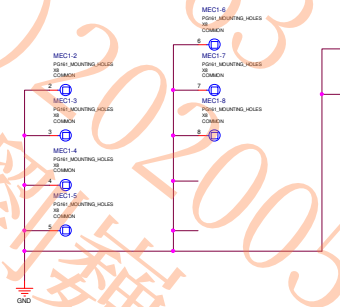
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LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY



Bracket:



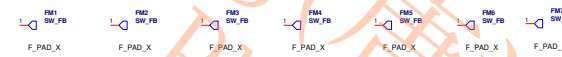
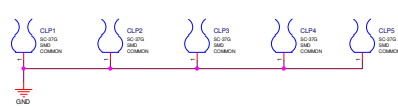
MOUNTING HOLES FOR HS:



BACK STIFFENER:



EMI Clip Options:



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