PG180-A02

256b GDDR6 x16
TALL DP + DP + DP + HDMI/DP + USB

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18	Change J4 footprint
19	Change J3 footprint
20	Remove DP co-layout
21	Remove JTAG & unused GPIO
32	Remove 0031_PS_ FBVDD CONTROLLER OVR3
34	NVVDD CONTROLLER change to MP2888A
35	DRMOS change to 10phases
36	DRMOS change to 10phases
37	Add NVVDD Output CAP
41	Remove INPUT SWITCH Rail Balance
44	J8 change to 8pin
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45	Add Hot Unplug Detect for J8
52	Add Remove LED & Fan Vin_12V option
53	Add MCU IT8295 for RGB LED

V372-3.1 change List

Base on V372-3.0，No changed

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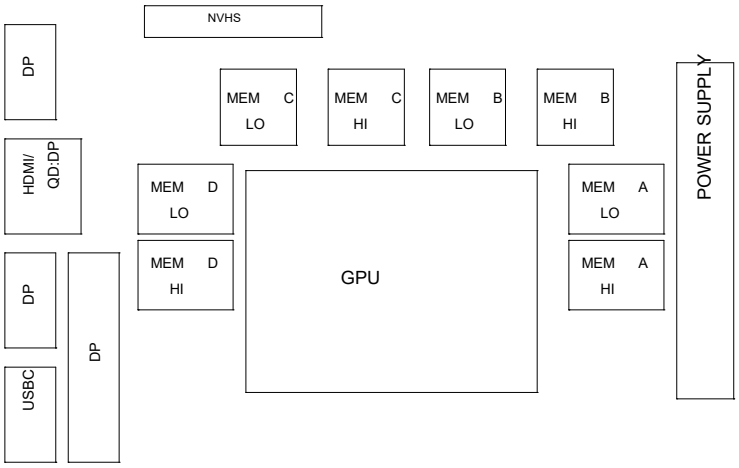

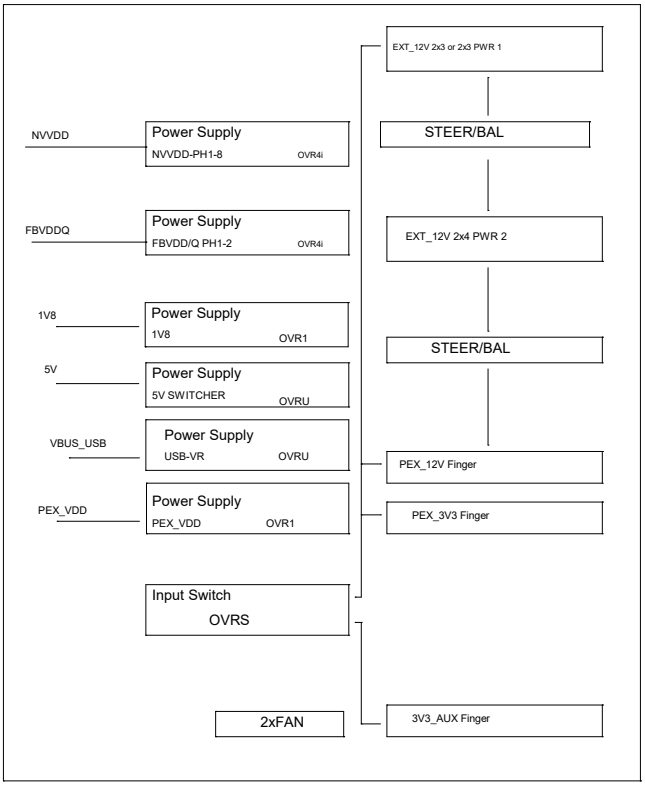

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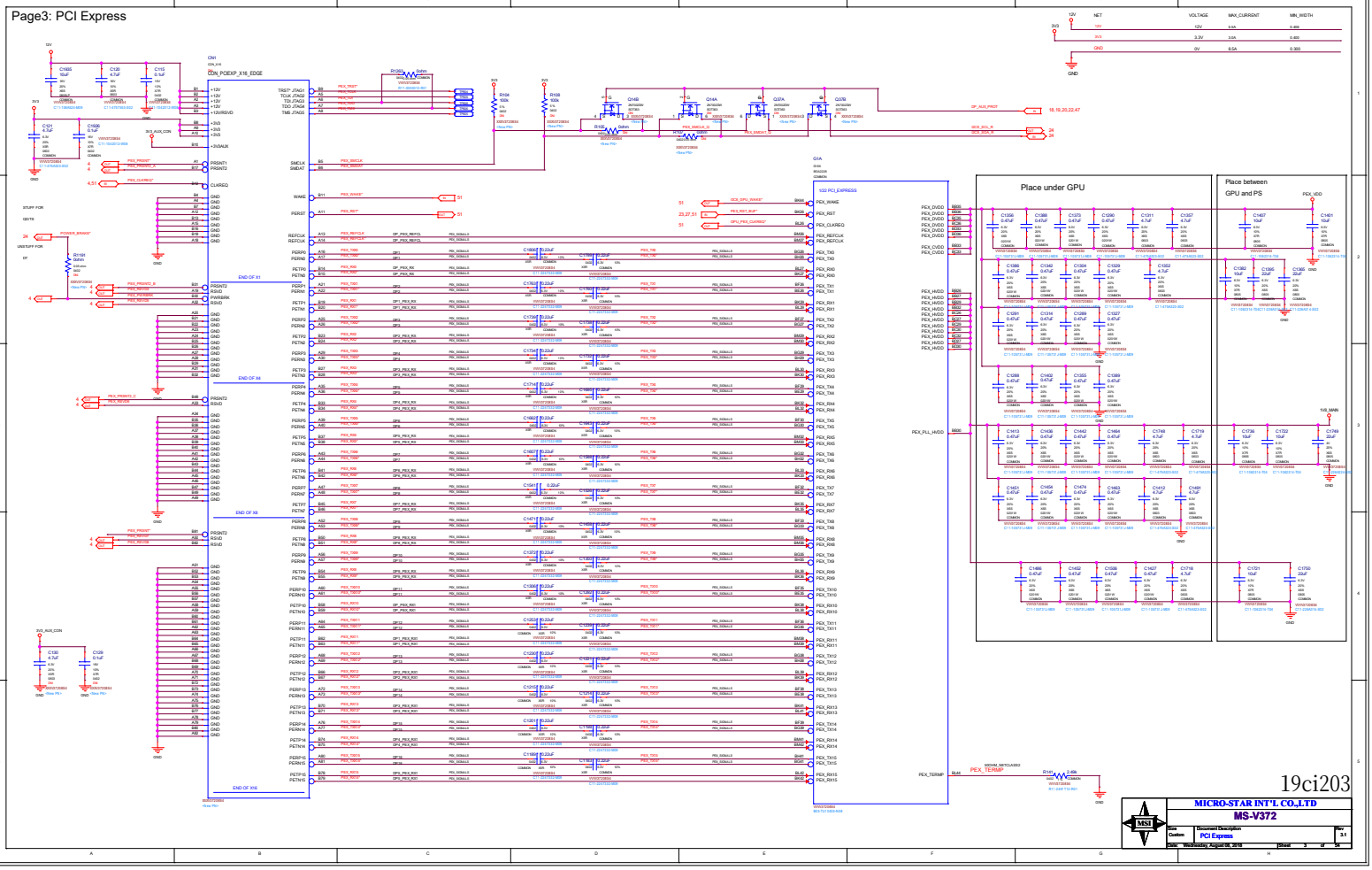
Page3: PCI Express
CN1
CON_PCIEXP_X16_EDGE
Place under GPU
Place between GPU and PS
U32 PCI_EXPRESS
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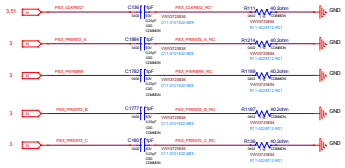
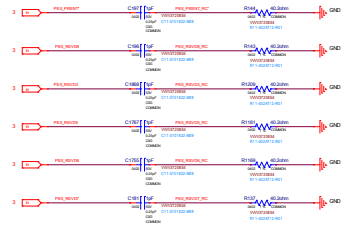
Page4: PCI Termination



PLACE CLOSE TO B81



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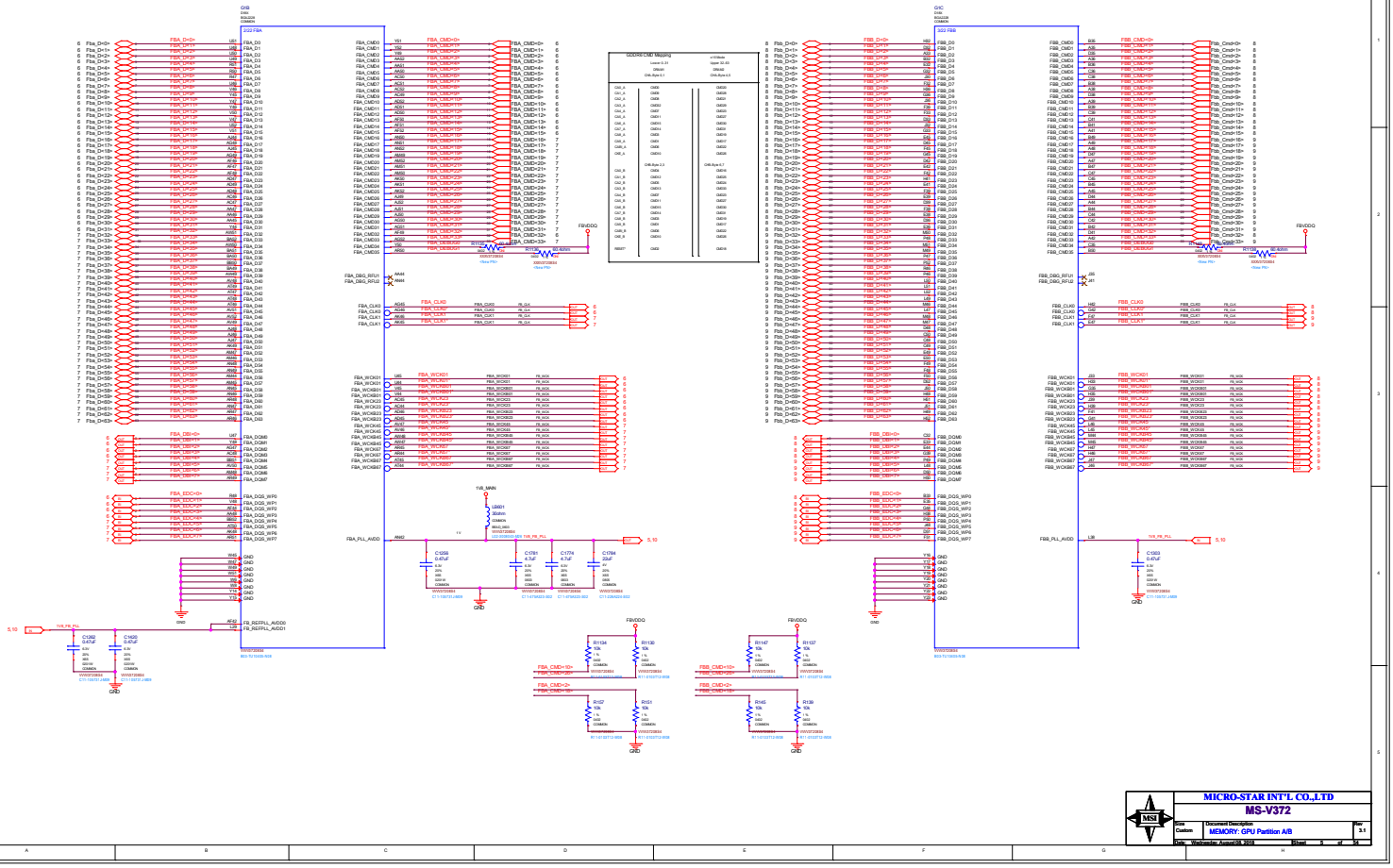
Page5: MEMORY: GPU Partition A/B



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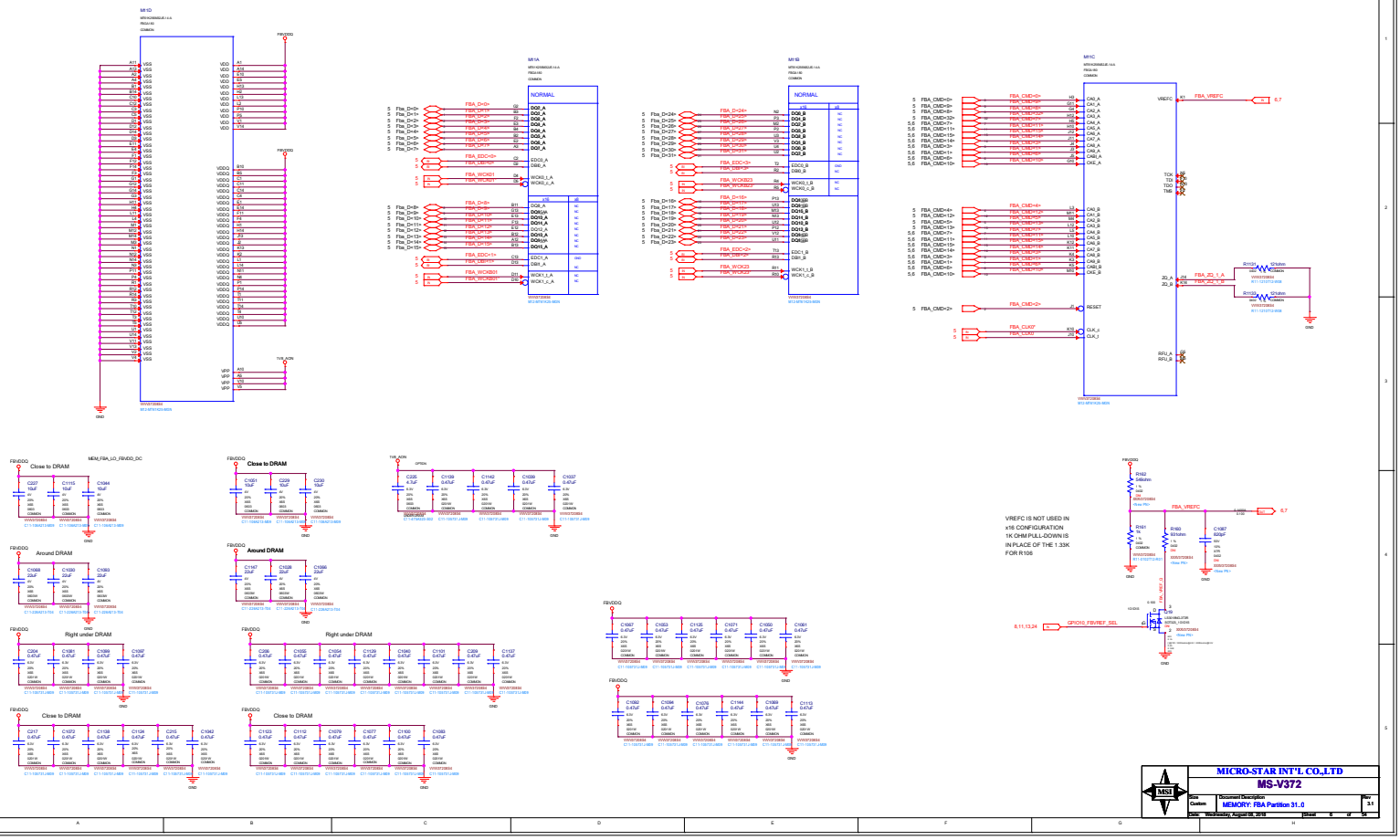
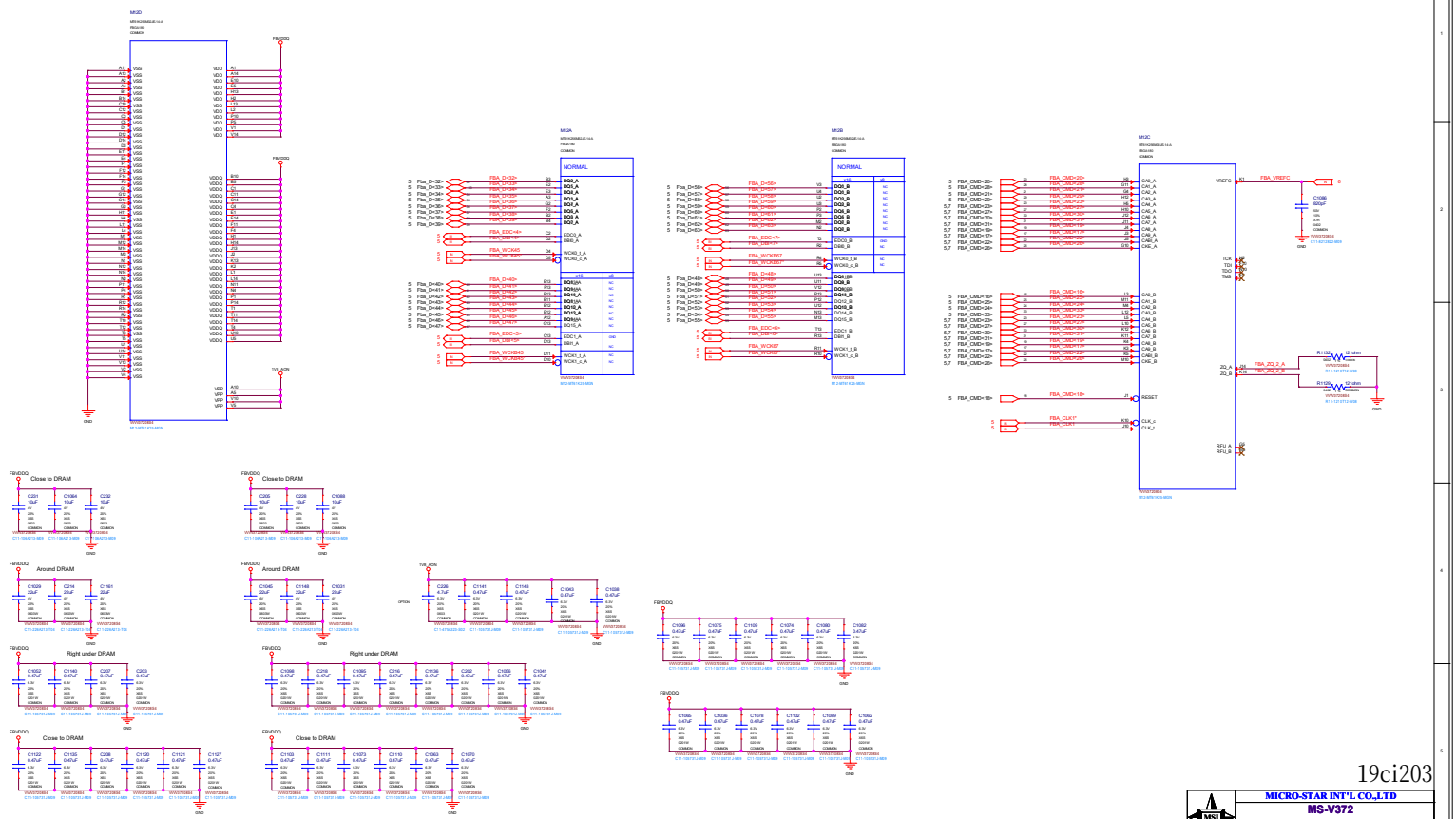
Page6: MEMORY: FBA Partition 31..0





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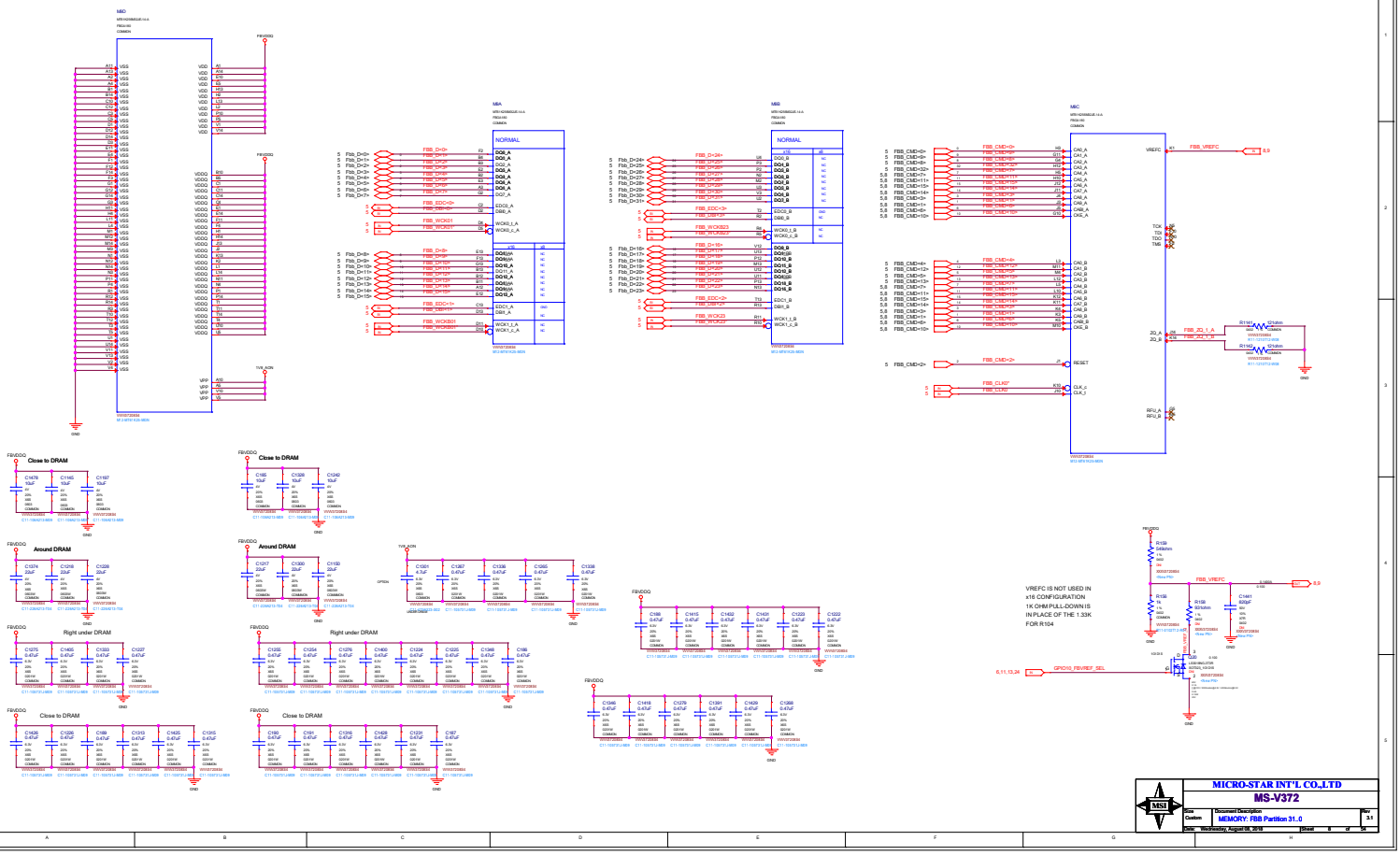
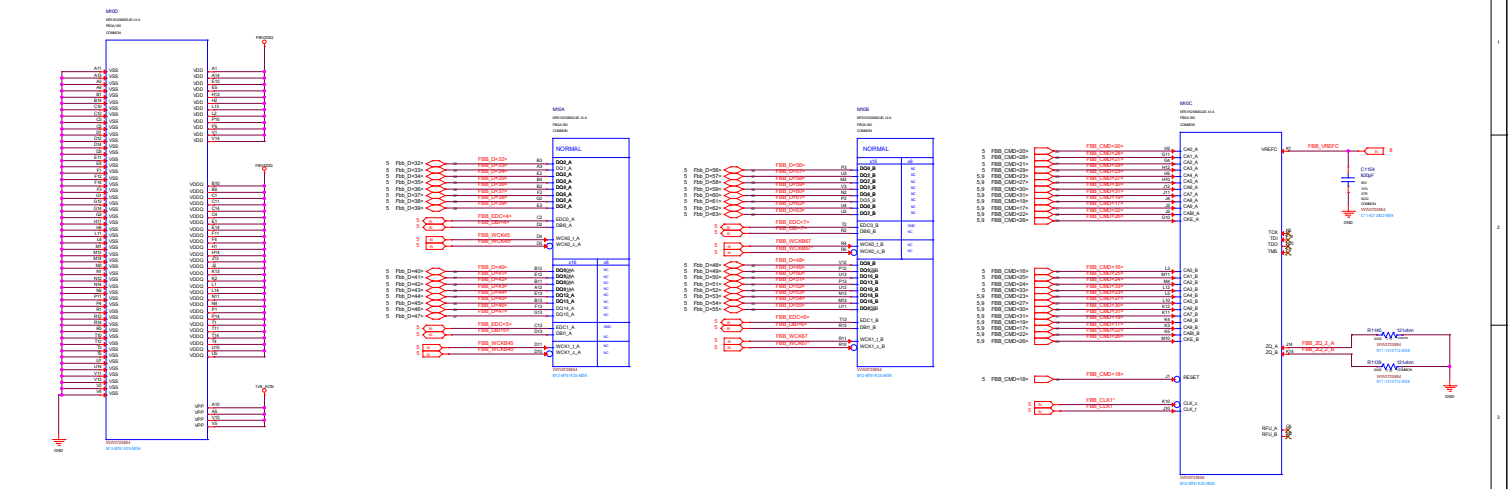
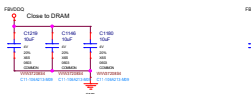
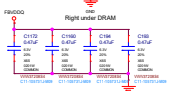
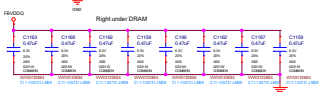
Page8: MEMORY: FBB Partition 31..0

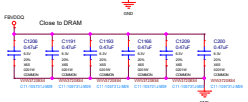


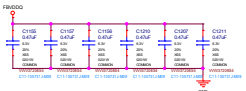












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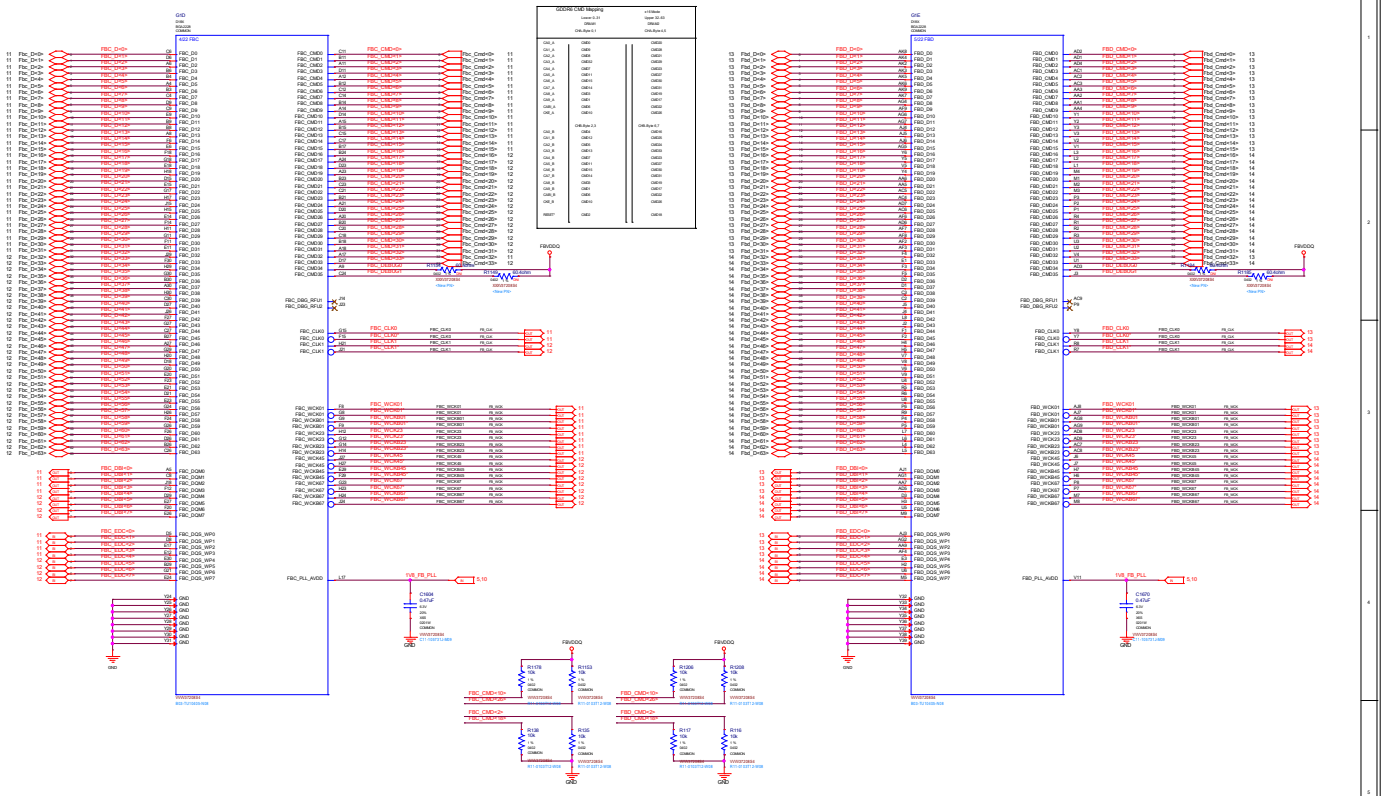

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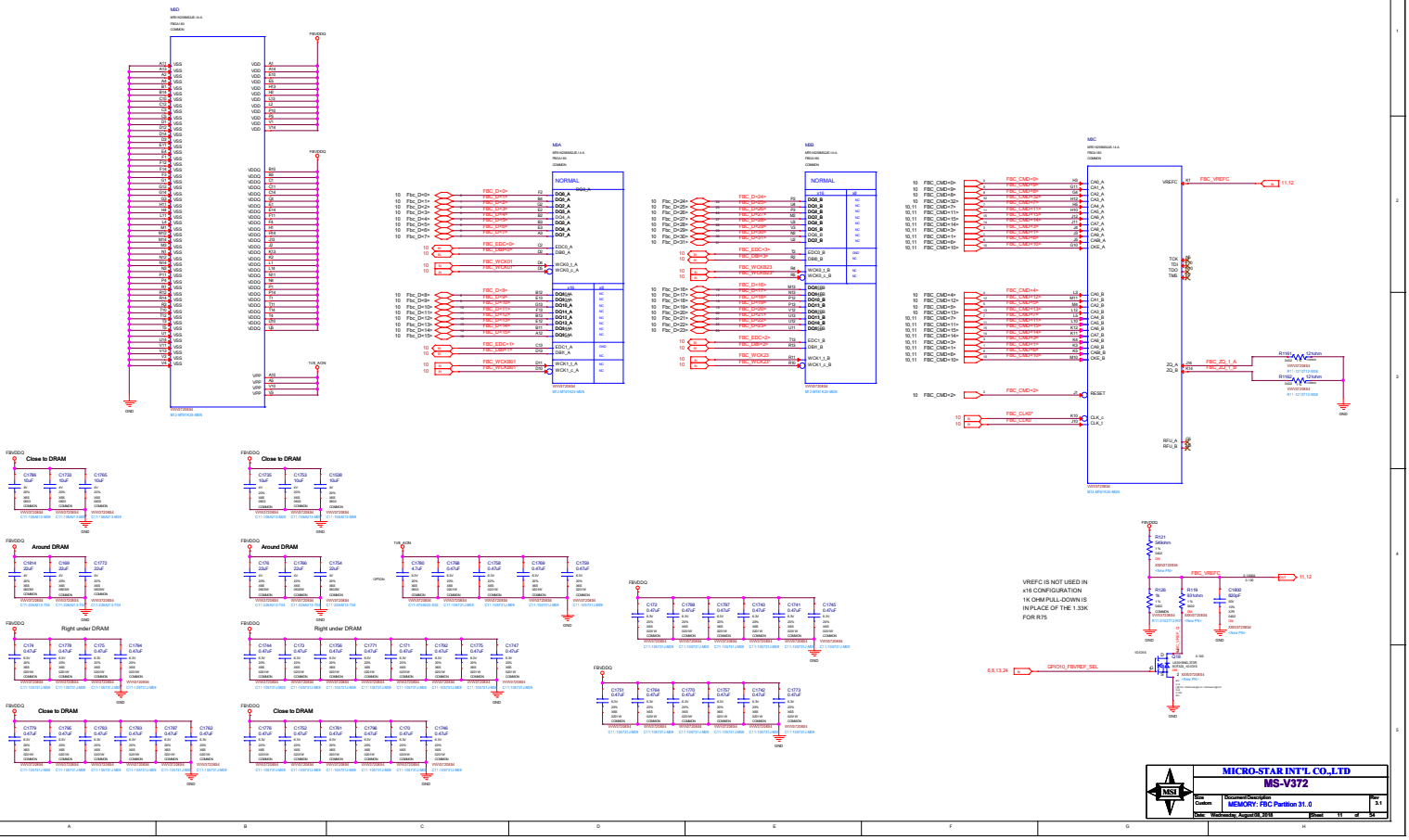
M6D
M6A
M6B
M6C
NORMAL
VREFC
RESET
TCK
TDI
TDO
TMS
RFU_A
RFU_B
Close to DRAM
Around DRAM
Right under DRAM
VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R75
GPIO10_FBVREF_SEL
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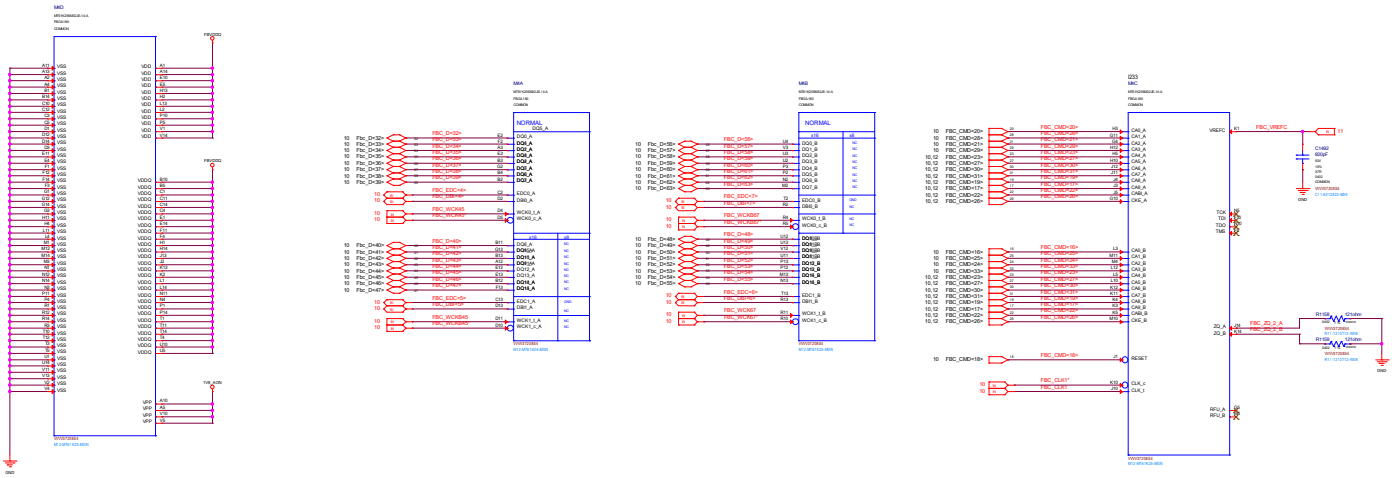

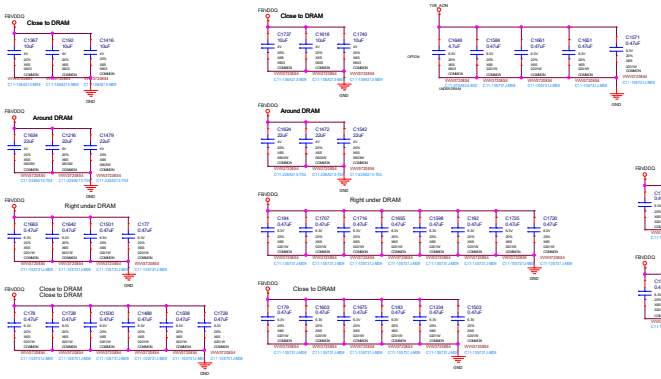

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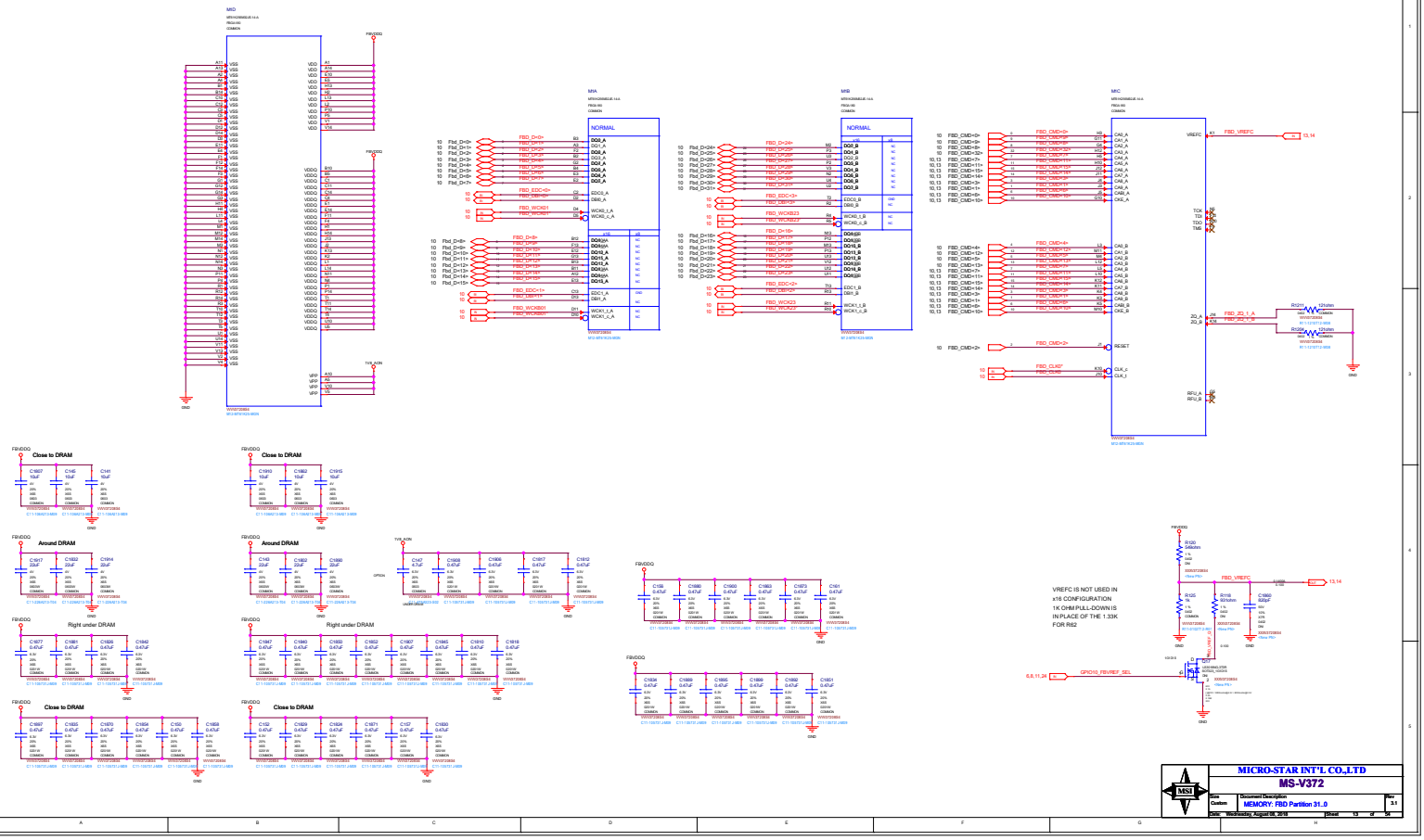

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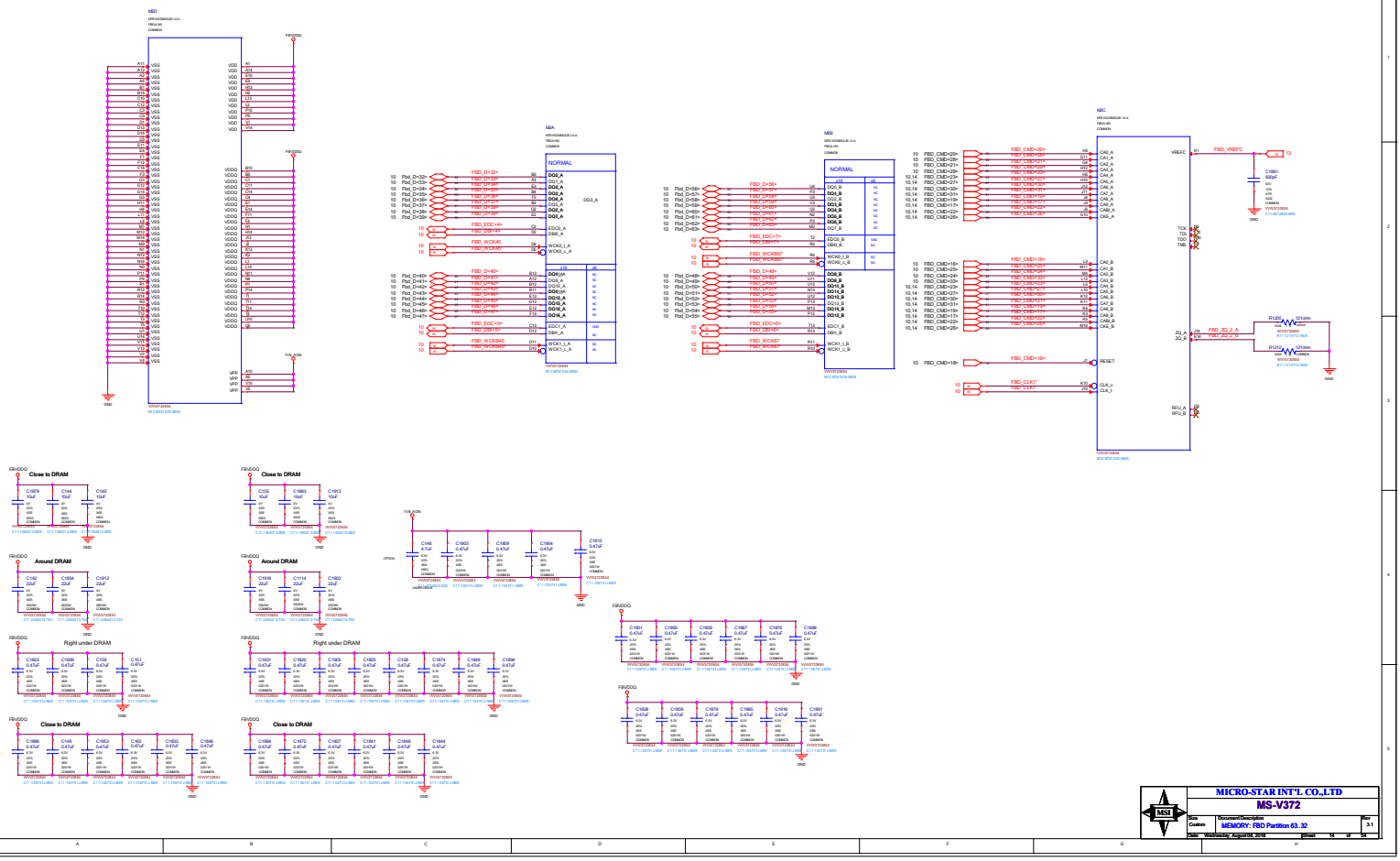

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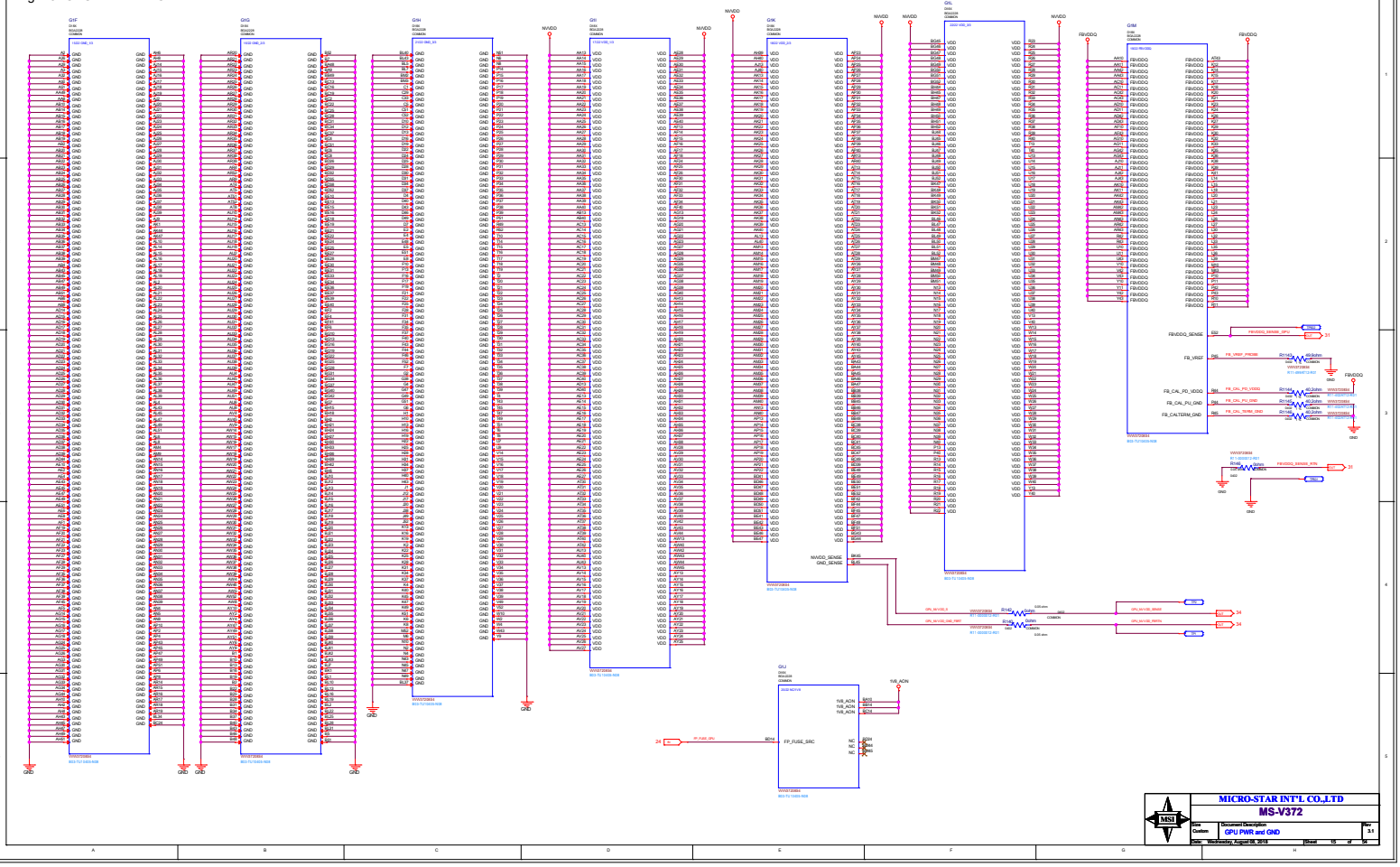
Page15: GPU PWR and GND
GND
NVVDD
FBVDDQ
FBVDDQ_SENSE
FB_VREF
FB_CAL_PD_VDDQ
FB_CAL_PU_GND
FB_CALTERM_GND
NVVDD_SENSE
GND_SENSE
FP_FUSE_SRC
1V8_AON
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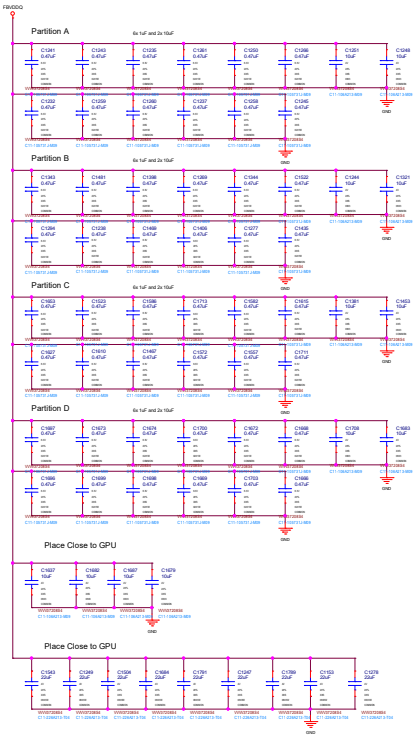
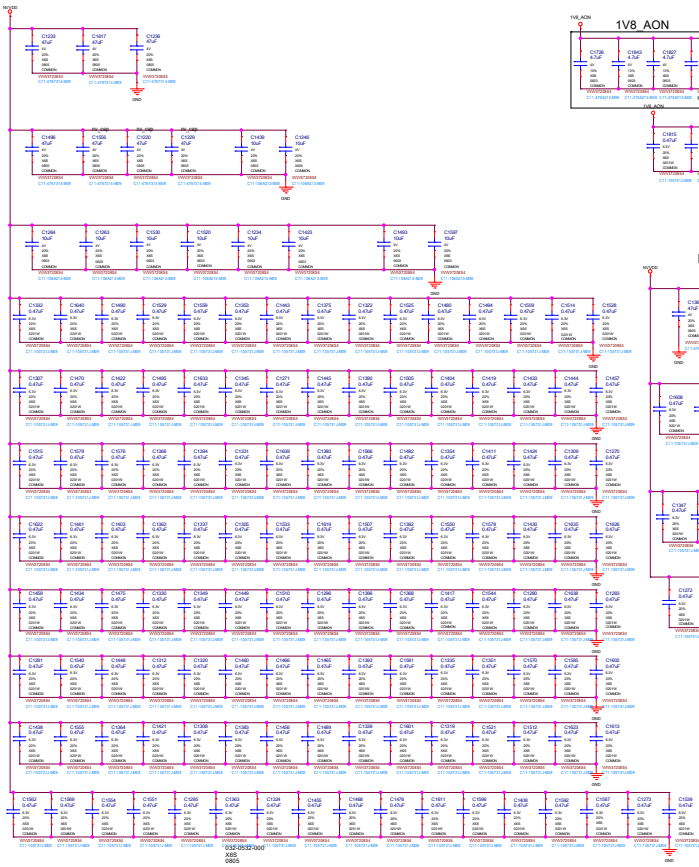
Page16: GPU Decoupling

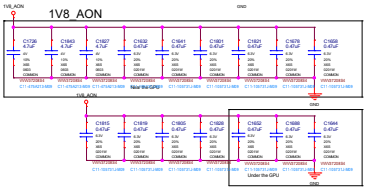
FBVDDQ



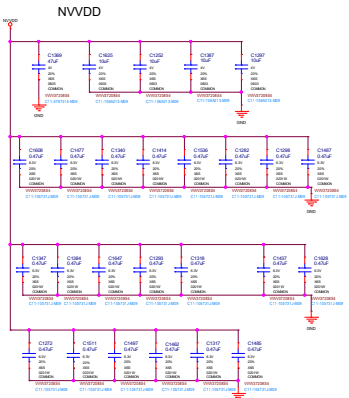
NVVDD



1V8_AON



NVVDD



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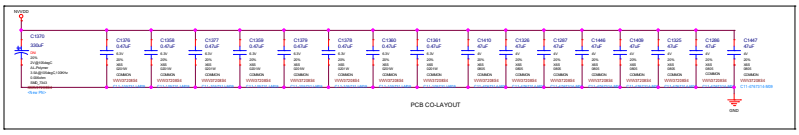
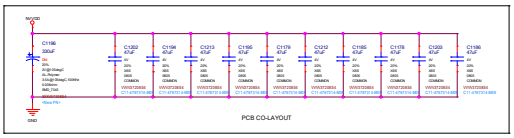
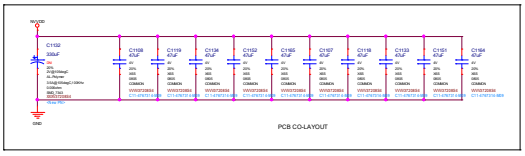
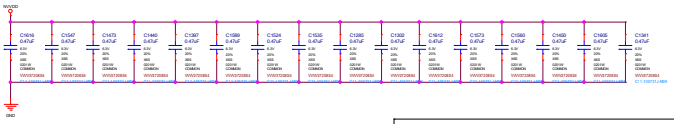
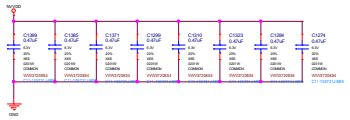
Page17: GPU Decoupling

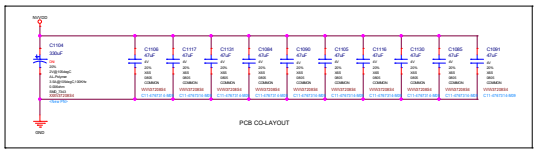


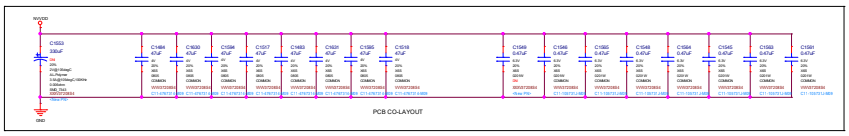












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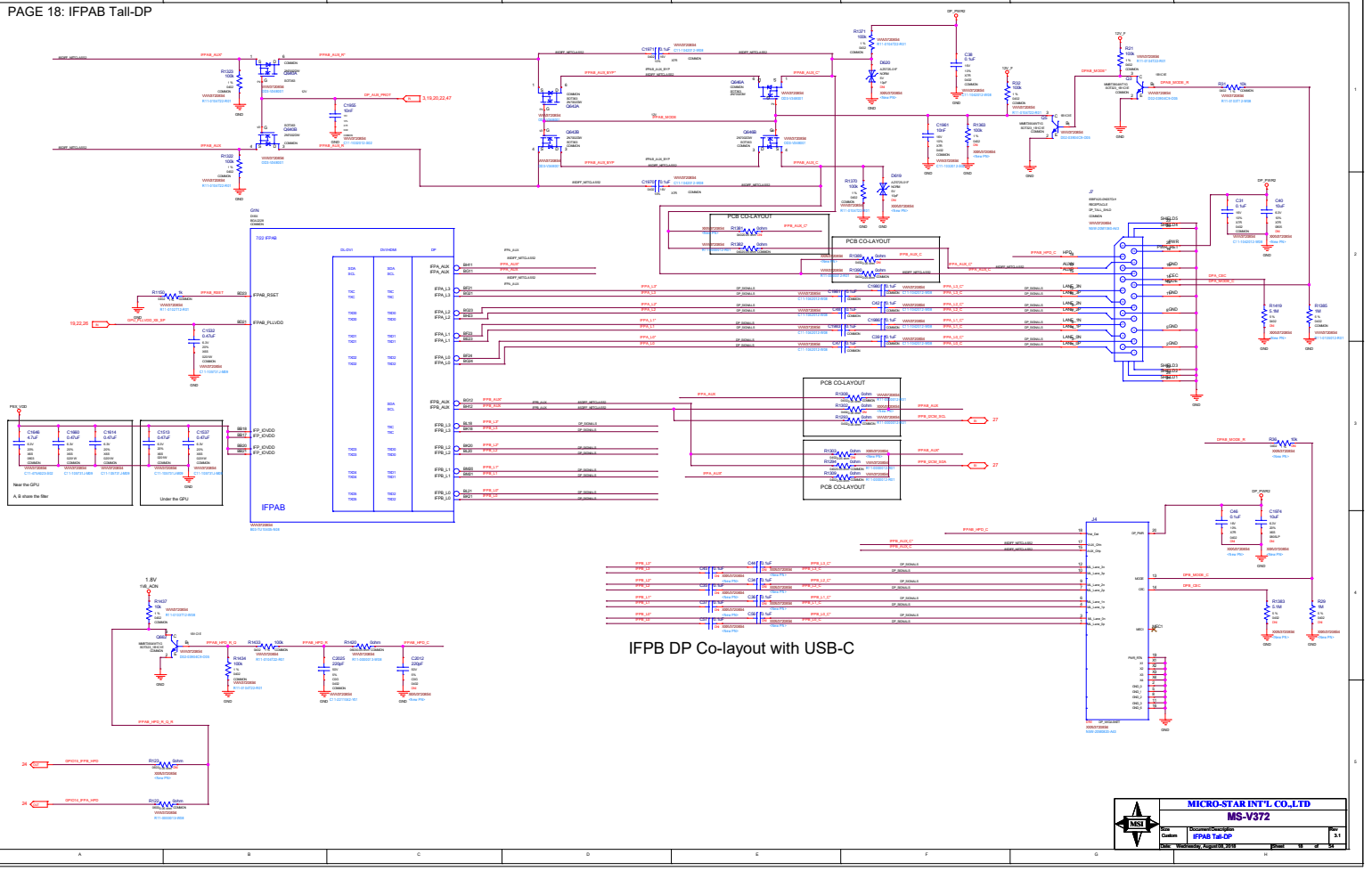
PAGE 18: IFPAB Tall-DP



IFPB DP Co-layout with USB-C

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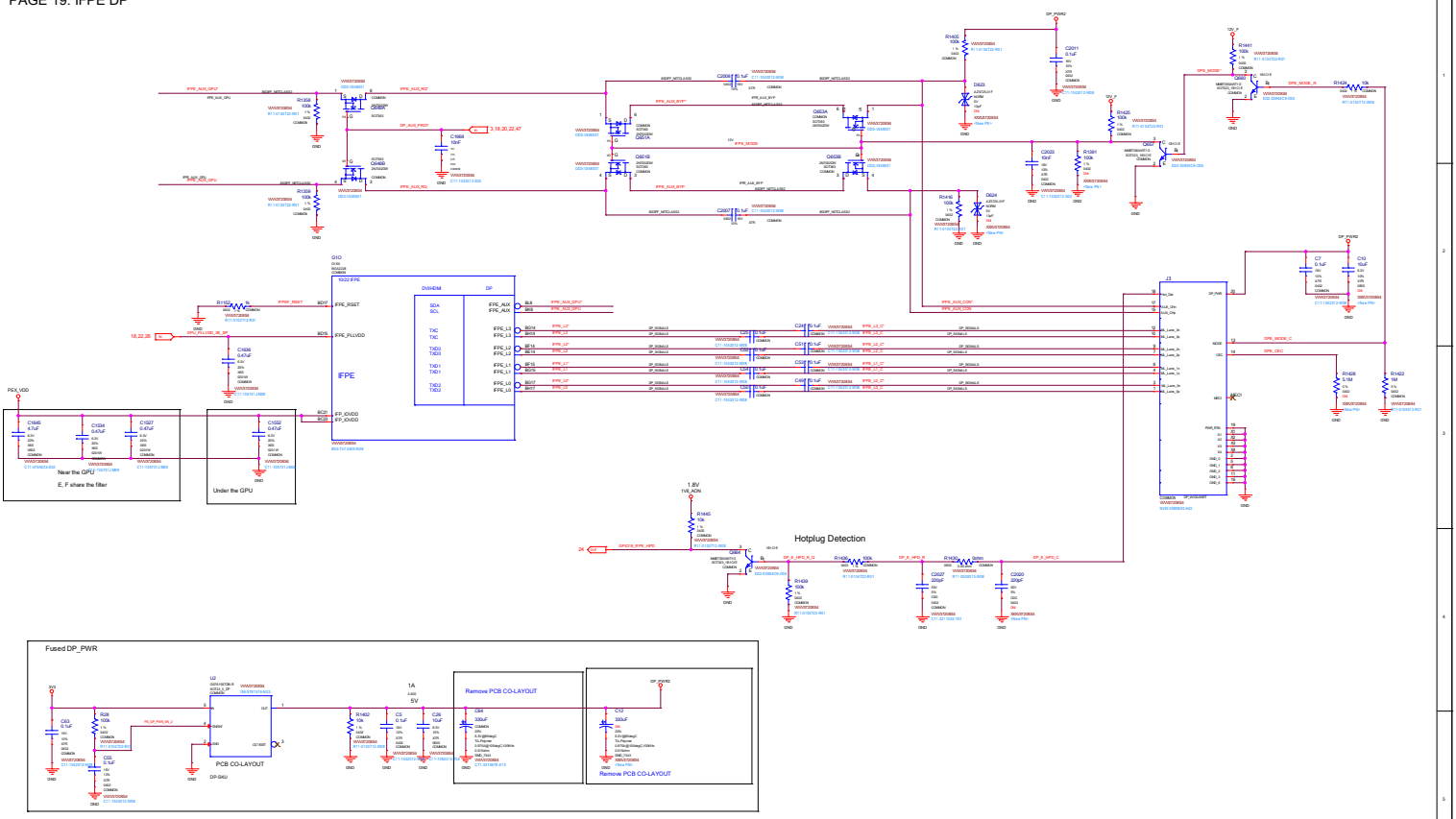
PAGE 19: IFPE DP



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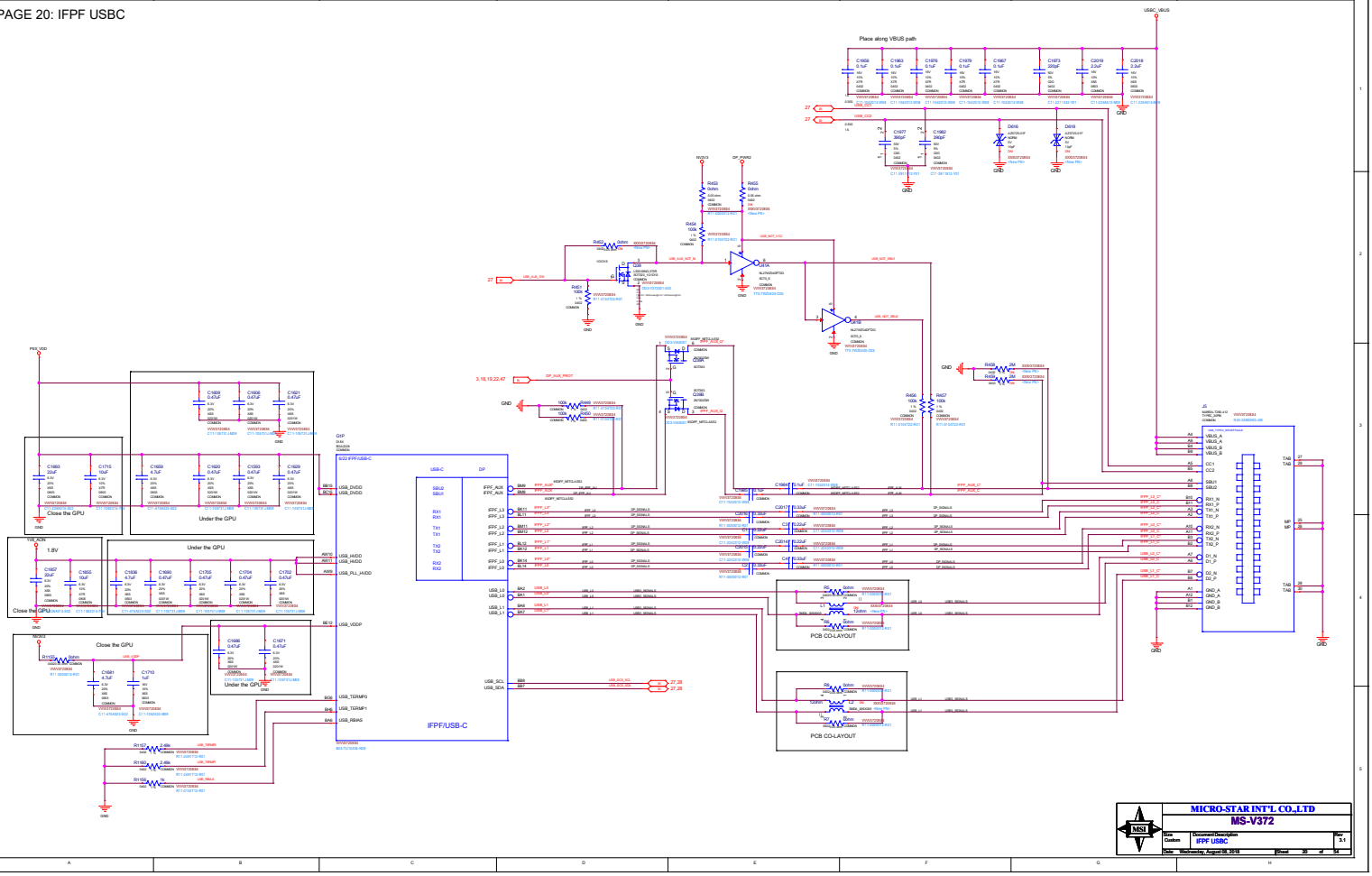
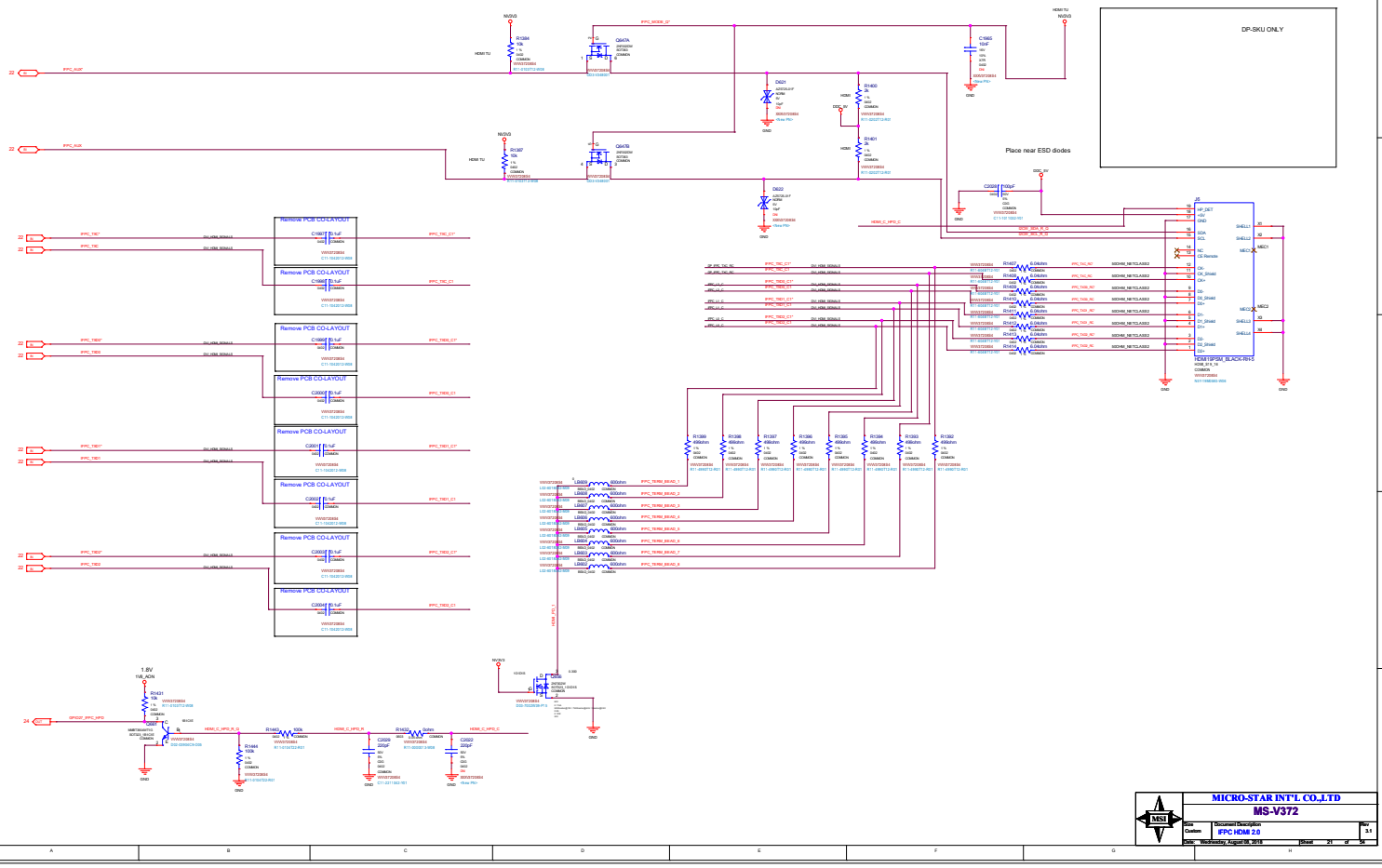
PAGE 20: IFPF USBC



PAGE 21:IFPC HDMI 2.0



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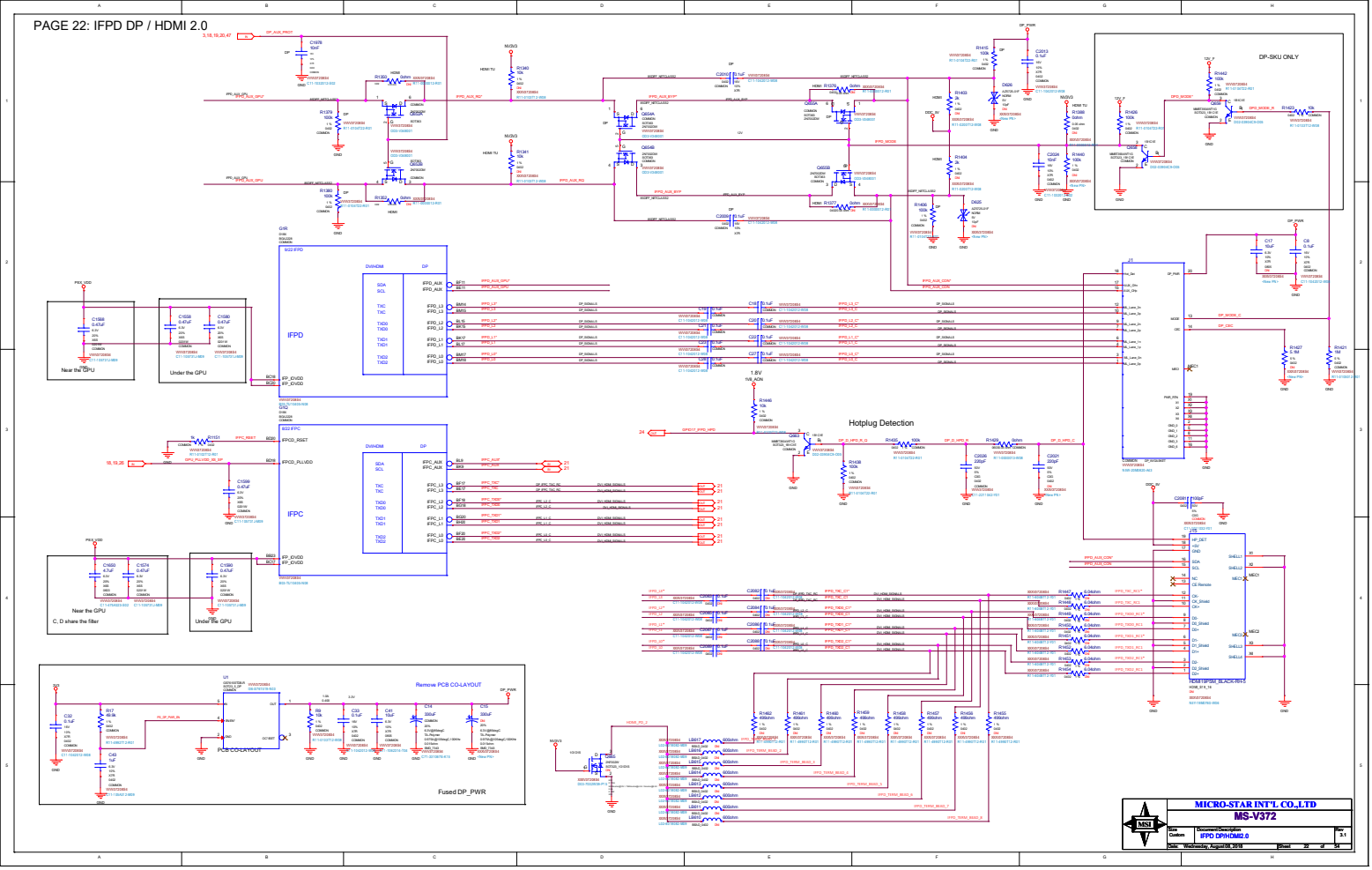
PAGE 22: IFPD DP / HDMI 2.0
DP-SKU ONLY
IFPD
IFPC
Hotplug Detection
Near the GPU
Under the GPU
C, D share the filter
Remove PCB CO-LAYOUT
PCB CO-LAYOUT
Fused DP_PWR
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IFPD DP/HDMI2.0
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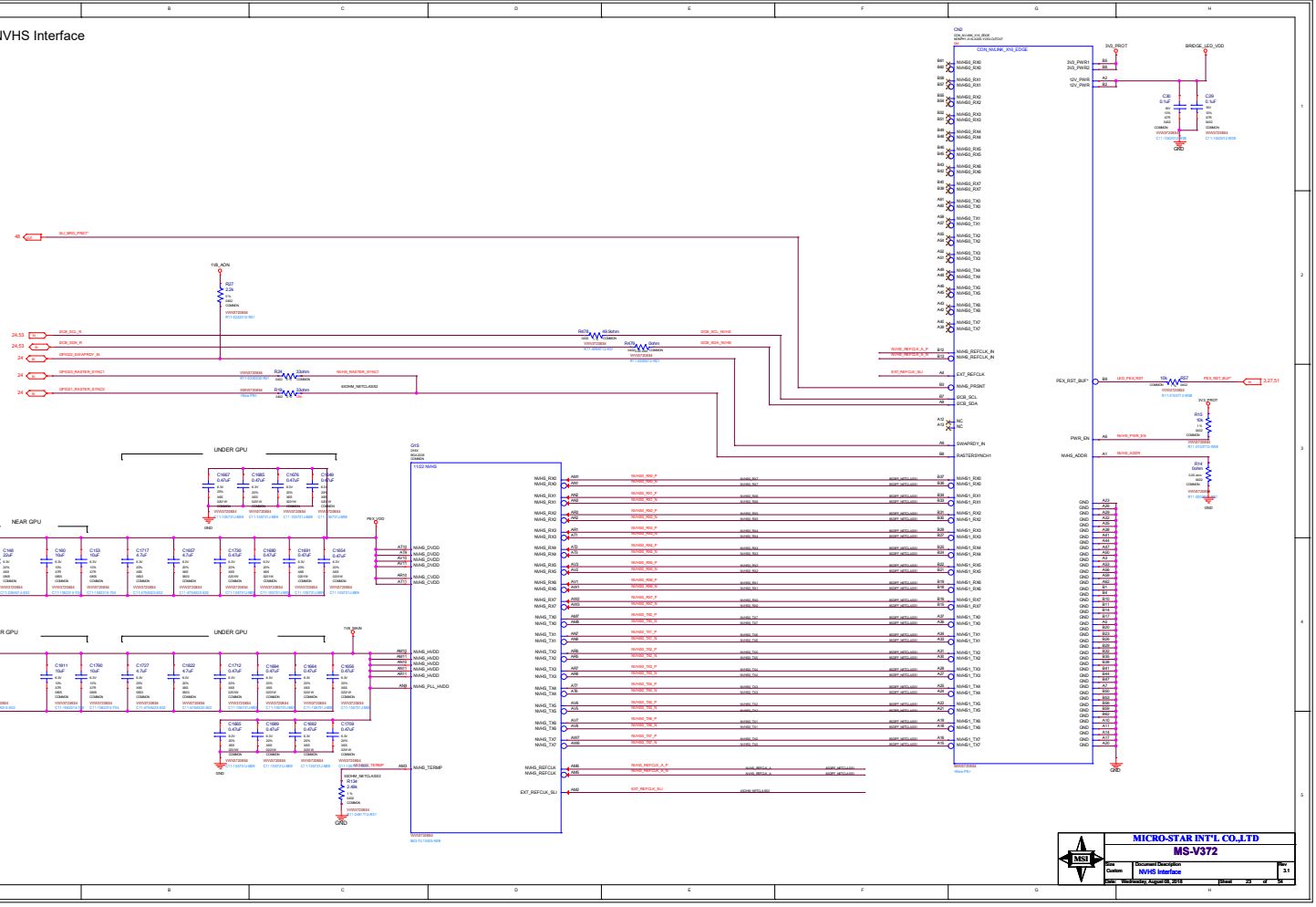
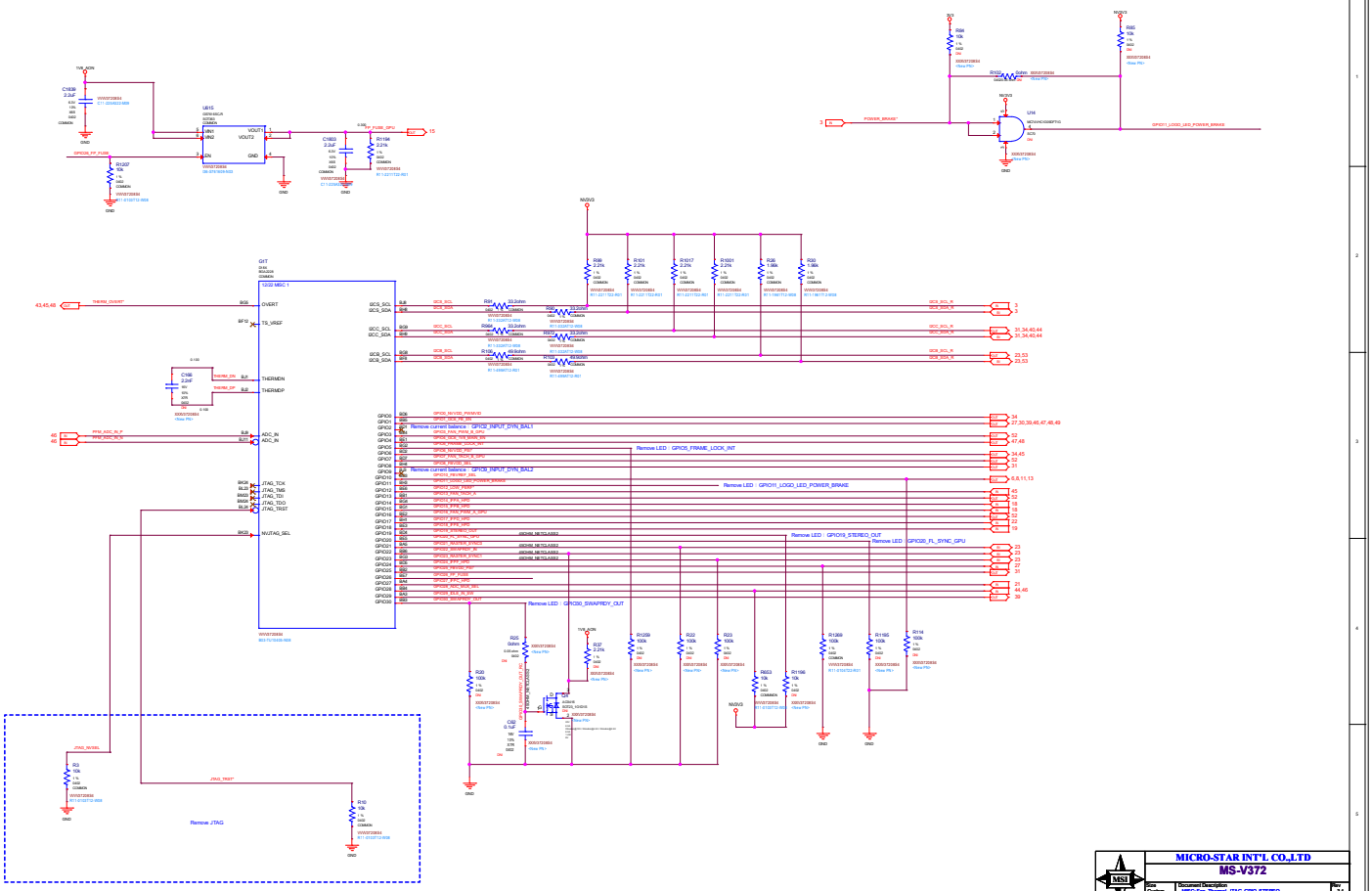
PAGE 23: NVHS Interface



PAGE 24: MISC: Fan, Thermal, JTAG, GPIO, STEREO



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PAGE 25: MISC: ROM, Straps

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

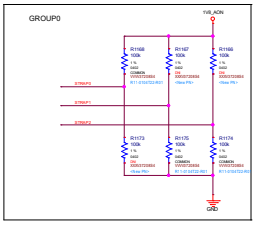
Default

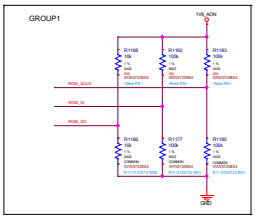
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

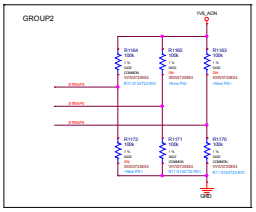
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

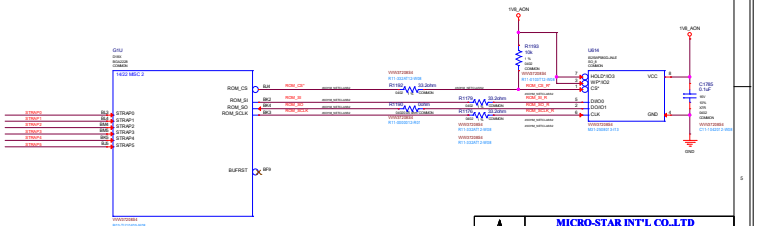
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE









MICRO-STAR INT'L CO.,LTD		
MS-V372		
Size: Custom	Document Description: MISC: ROM, Straps	Rev: 3.1
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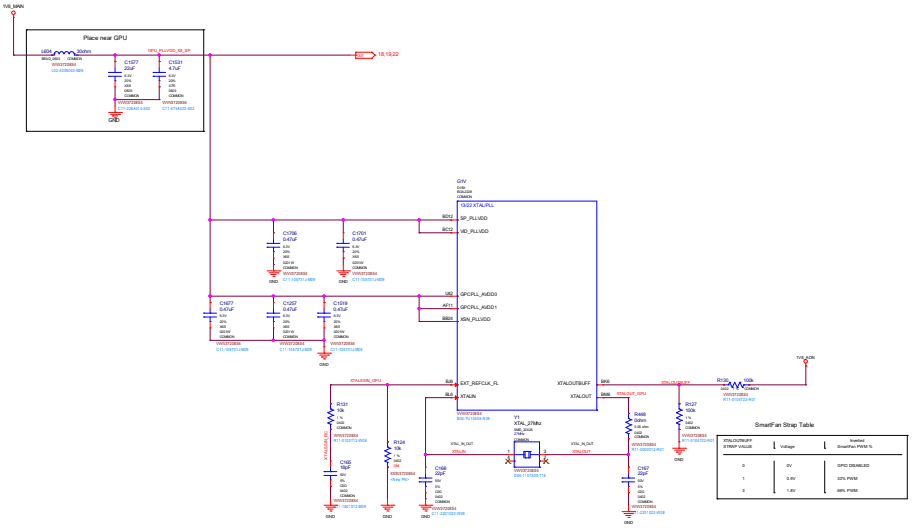
PAGE 26: MISC: XTAL. PLL



MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: MISC: XTAL PLL
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PAGE 27: MISC: USB PPC

PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN

UART RXD DEBUG PORT

PCB CO-LAYOUT

Place it closed to 5V regulator

MICRO-STAR INT'L CO.,LTD		
MS-V372		
Size: Custom	Document Description: MISC: USB PPC	Rev: 3.1
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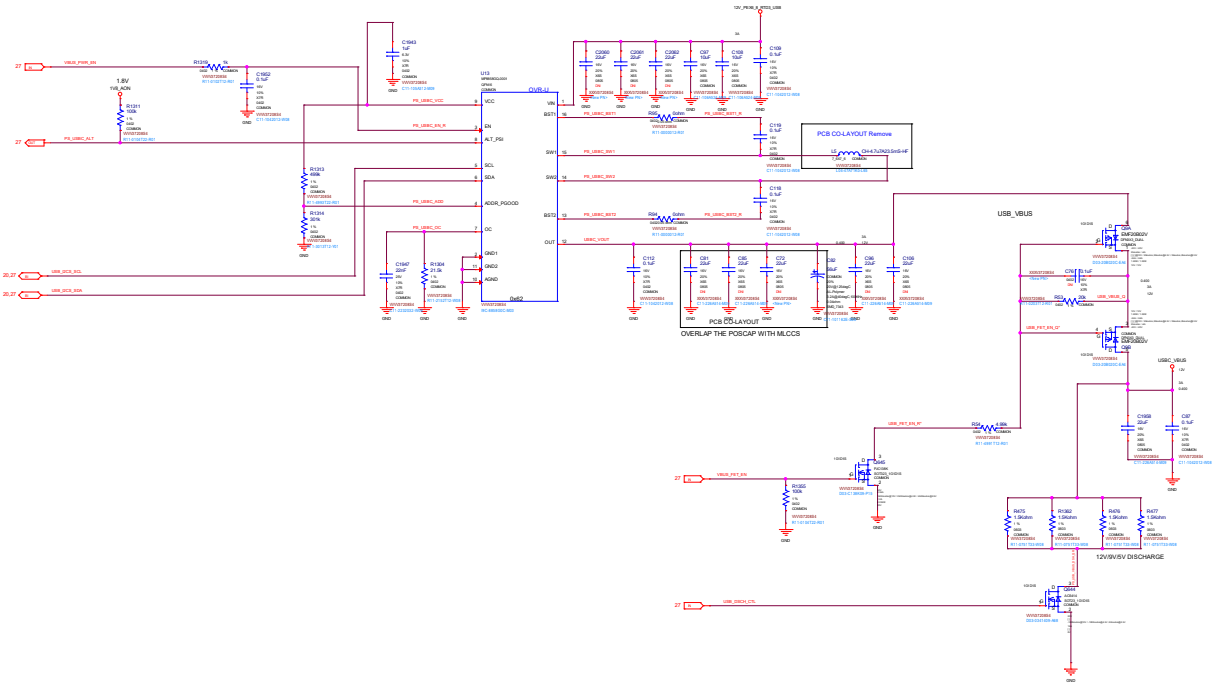
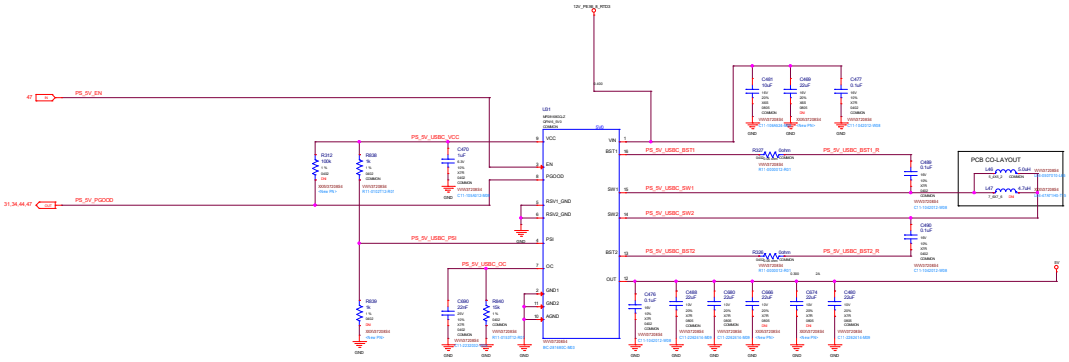


MICRO-STAR INT'L CO.,LTD	
MS-V372	
Size: Custom	Document Description: PS: USB VR
Rev: 3.1	
Date: Wednesday, August 09, 2018	Sheet 28 of 54

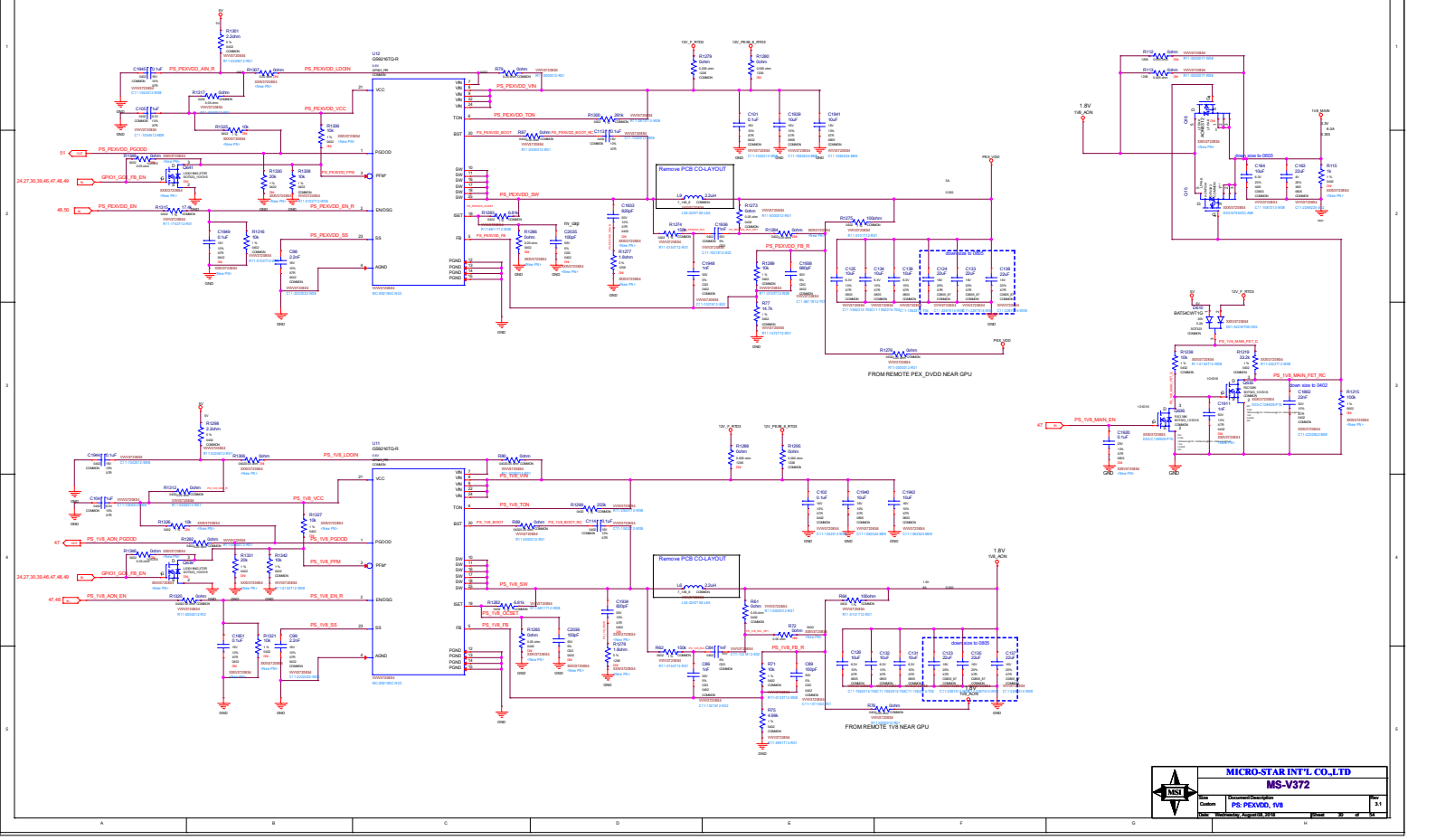
PAGE 29: PS: 5V, 5V_BACKUP



Remove U32 (RT7296FGJ8F)

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V372	
Size: Custom	Document Description: PS: 5V, 5V_BACKUP	Rev: 3.1
Date: Wednesday, August 08, 2018	Sheet 29 of 54	

PAGE 30: PS: PEXVDD, 1V8



MICRO-STAR INT'L CO.,LTD	
MS-V372	
Size: Custom	Document Description: PS: PEXVDD, 1V8
Rev: 3.1	
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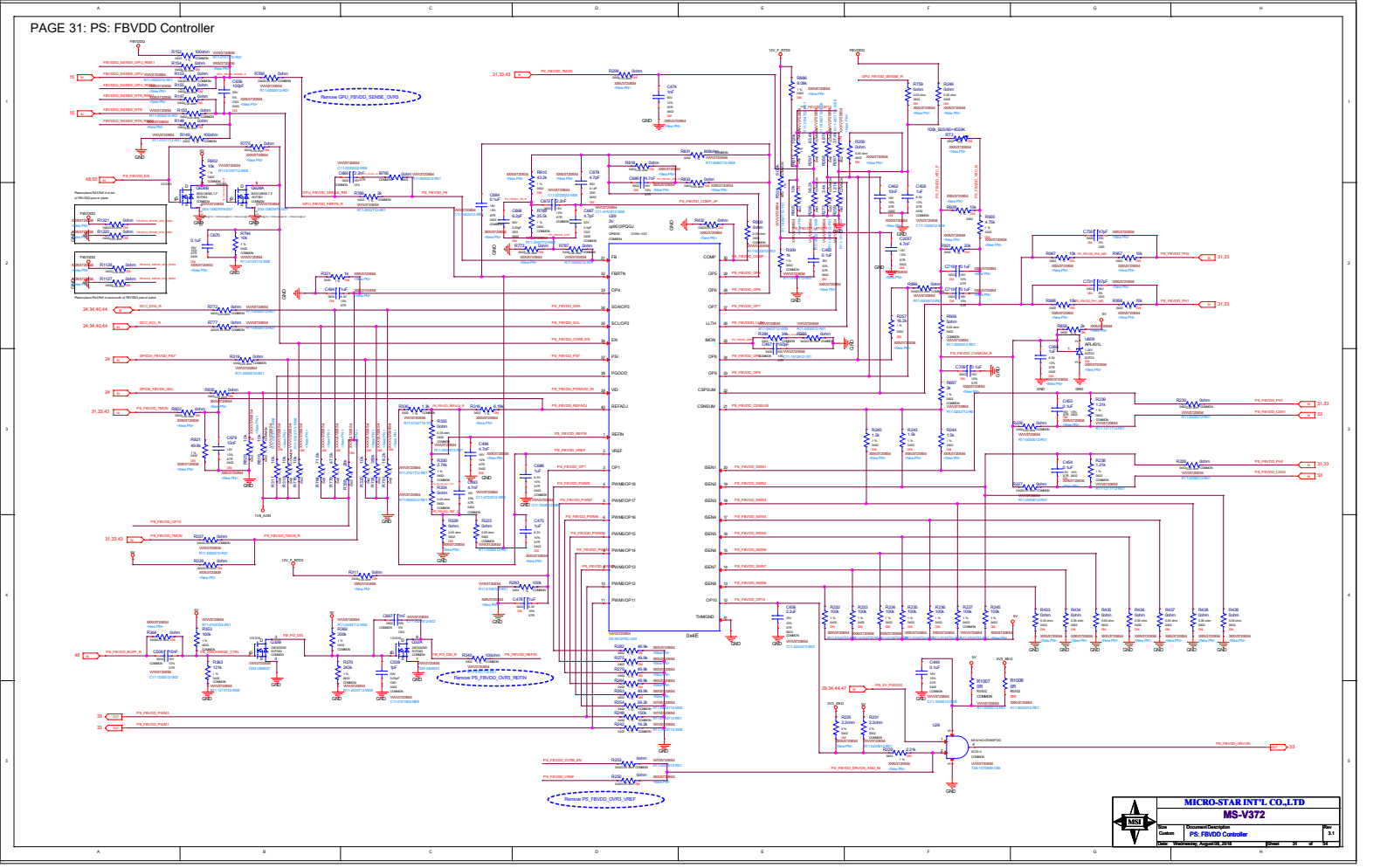
PAGE 31: PS: FBVDD Controller



PAGE 32: PS: FBVDD Controller OVR3

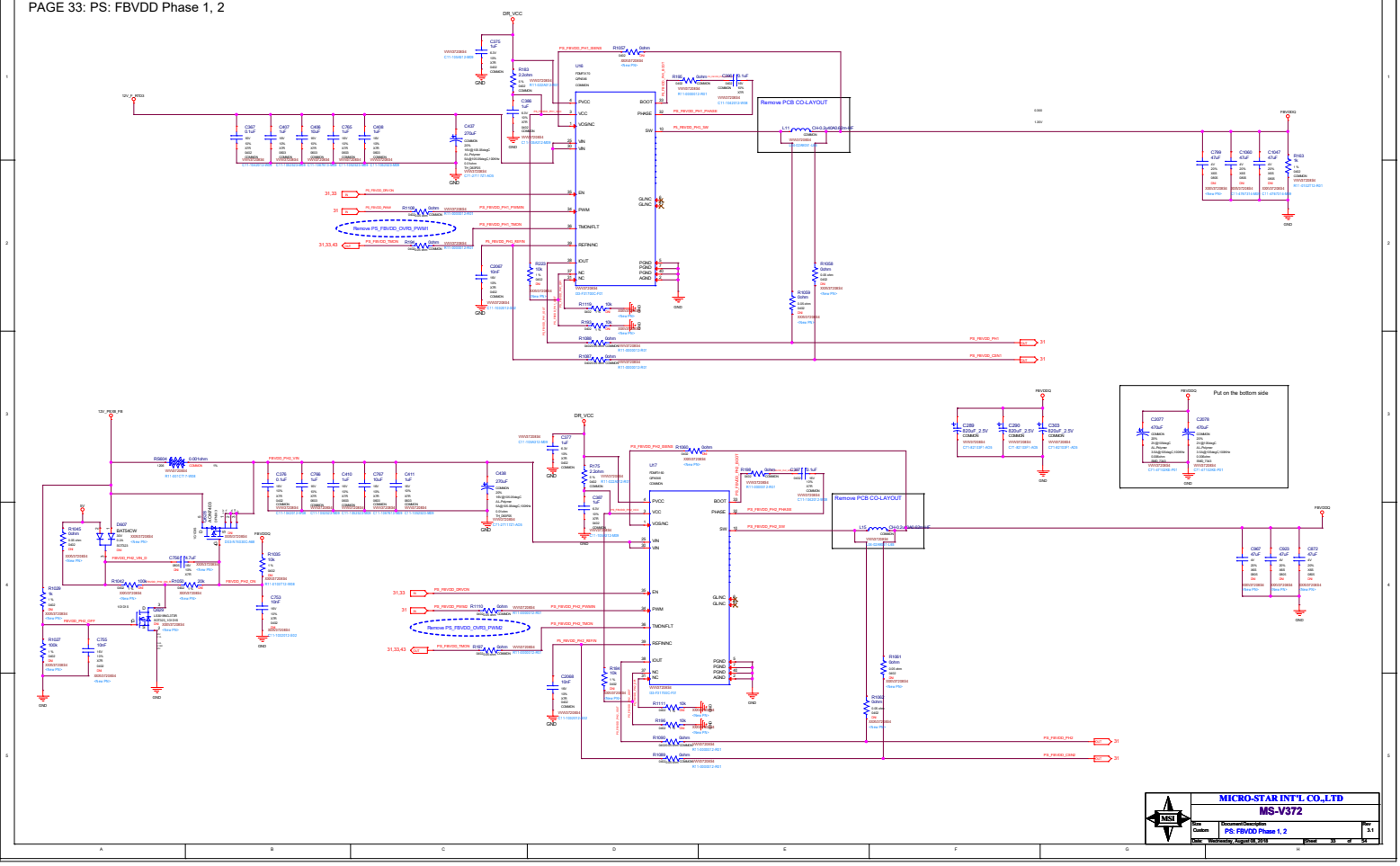
MICRO-STAR INT'L CO.,LTD

MS-V372

Size: Custom | Document Description: PS: FBVDD Controller OVR3 (X) | Rev: 3.1

Date: Wednesday, August 08, 2018 | Sheet 32 of 34

PAGE 33: PS: FBVDD Phase 1, 2



MICRO-STAR INT'L CO.,LTD	
MS-V372	
Size: Custom	Document Description: PS: FBVDD Phase 1, 2
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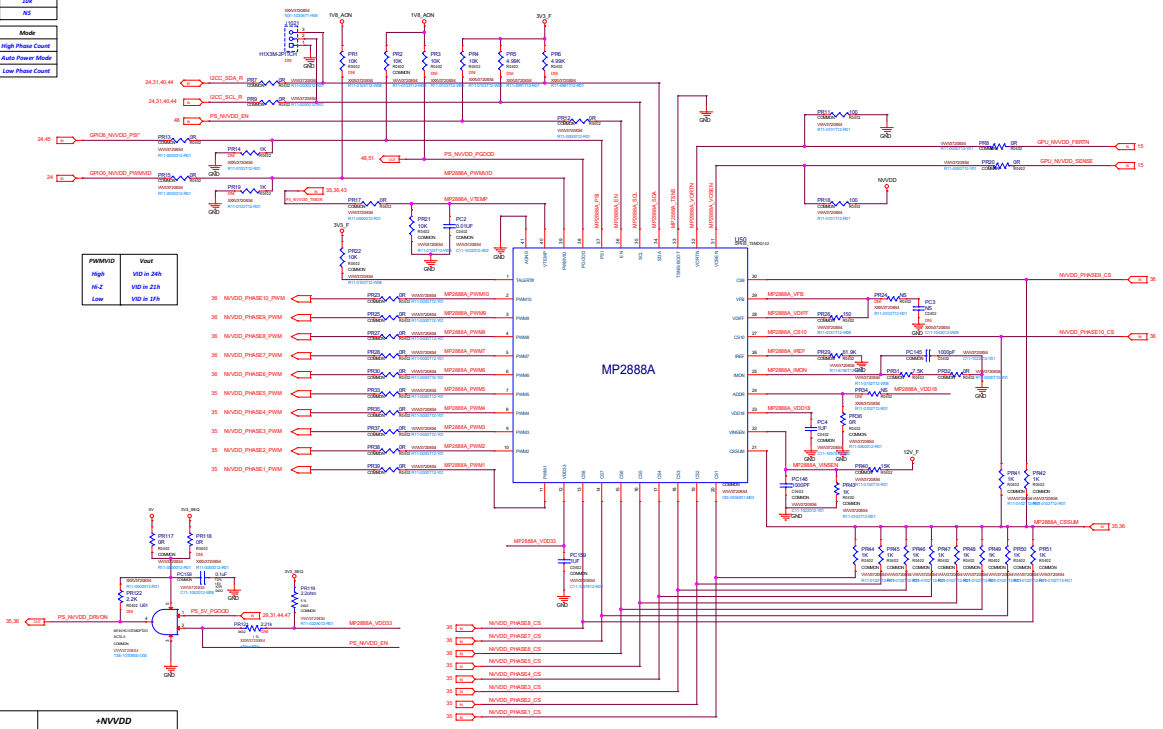
Date: Wednesday, August 08, 2018	Sheet 33 of 54

EN Type	R3
Open Drain	10k
Push Pull	NS

PSI	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count

PWMVID	Vout
High	VID in 24h
Hi-Z	VID in 21h
Low	VID in 1Fh



	+NVVDD
TDC	200A
IccMax	330A
Vboot	0.8V
Load Line	0mohm

PMBus Address	Setting Point(V)	R_{upper} (kΩ) 1%	R_{lower} (kΩ) 1%
20h	0	0	0
21h	0.031	3.32	0.059
22h	0.057	3.32	0.11
23h	0.084	3.32	0.162
24h	0.116	3.32	0.226
25h	0.156	3.32	0.316
26h	0.205	3.32	0.43
27h	0.266	3.32	0.576
28h	0.340	3.32	0.768
29h	0.430	3.32	1.05
2Ah	0.540	3.32	1.43
2Bh	0.675	3.32	2
2Ch	0.844	3.32	2.94
2Dh	1.048	3.32	4.64
2Eh	1.301	3.32	8.66
2Fh	1.500	3.32	16.5

MICRO-STAR INT'L CO.,LTD
MS-V372
Size: Custom | Document Description: PS: NVVDD - MP2888A | Rev: 3.1
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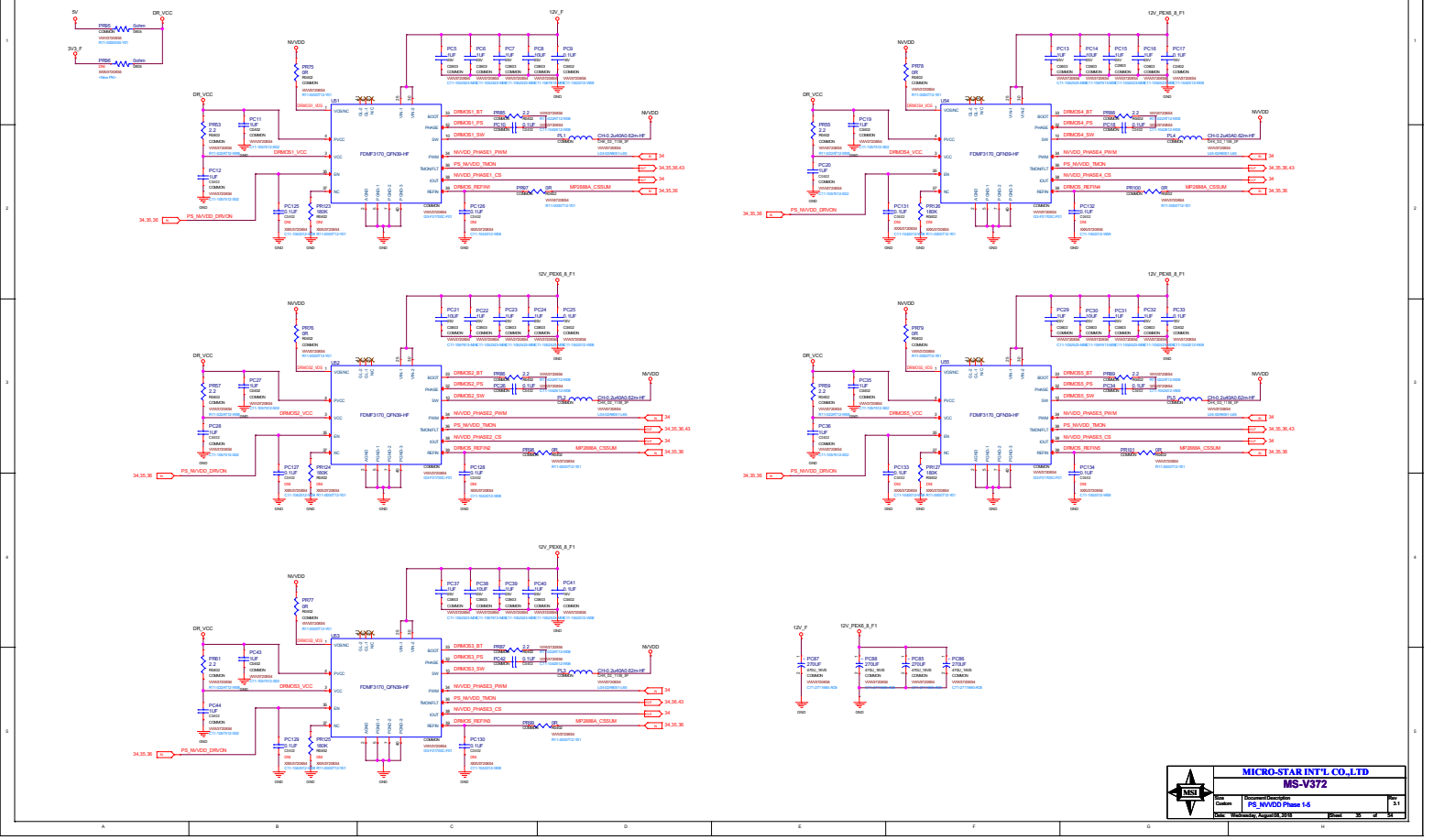
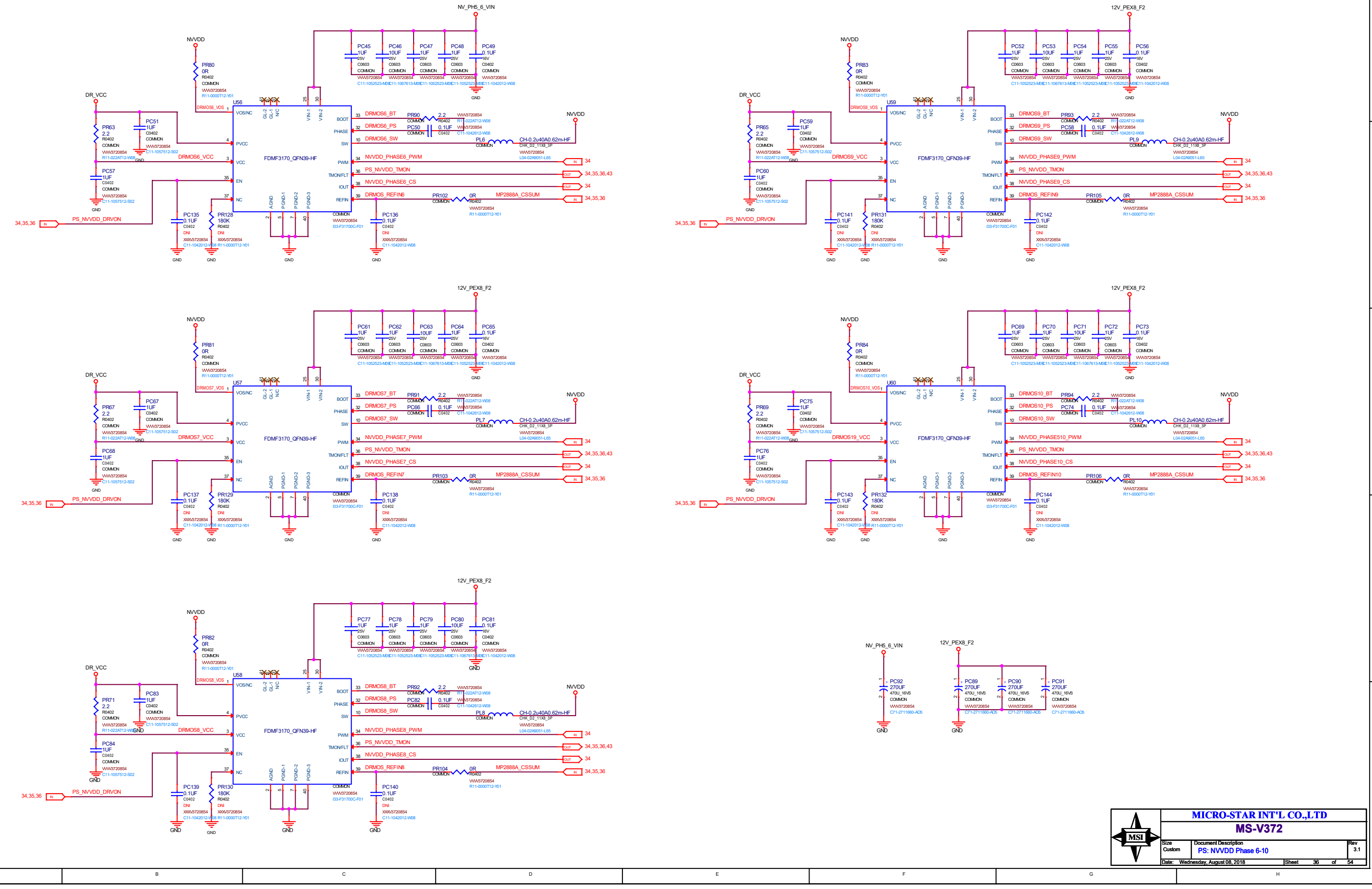
Page35: PS: NVVDD Phase 1-5



MICRO-STAR INT'L CO.,LTD	
MS-V372	
Size: Custom	Document Description: PS_NVDD Phase 1-5
Date: Wednesday, August 08, 2018	Sheet 35 of 54

Page36: PS: NVVDD Phase 6-10



NVVDD Output CAP

MICRO-STAR INT'L CO.,LTD		
MS-V372		
Size: Custom	Document Description: PS: NVVDD Output CAP	Rev: 3.1
Date: Wednesday, August 08, 2018	Sheet 37 of 54	

PAGE 38: PS:NVVDD (X)

MICRO-STAR INT'L CO.,LTD

MS-V372

Size: Custom | Document Description: PS:NVVDD (X) | Rev: 3.1

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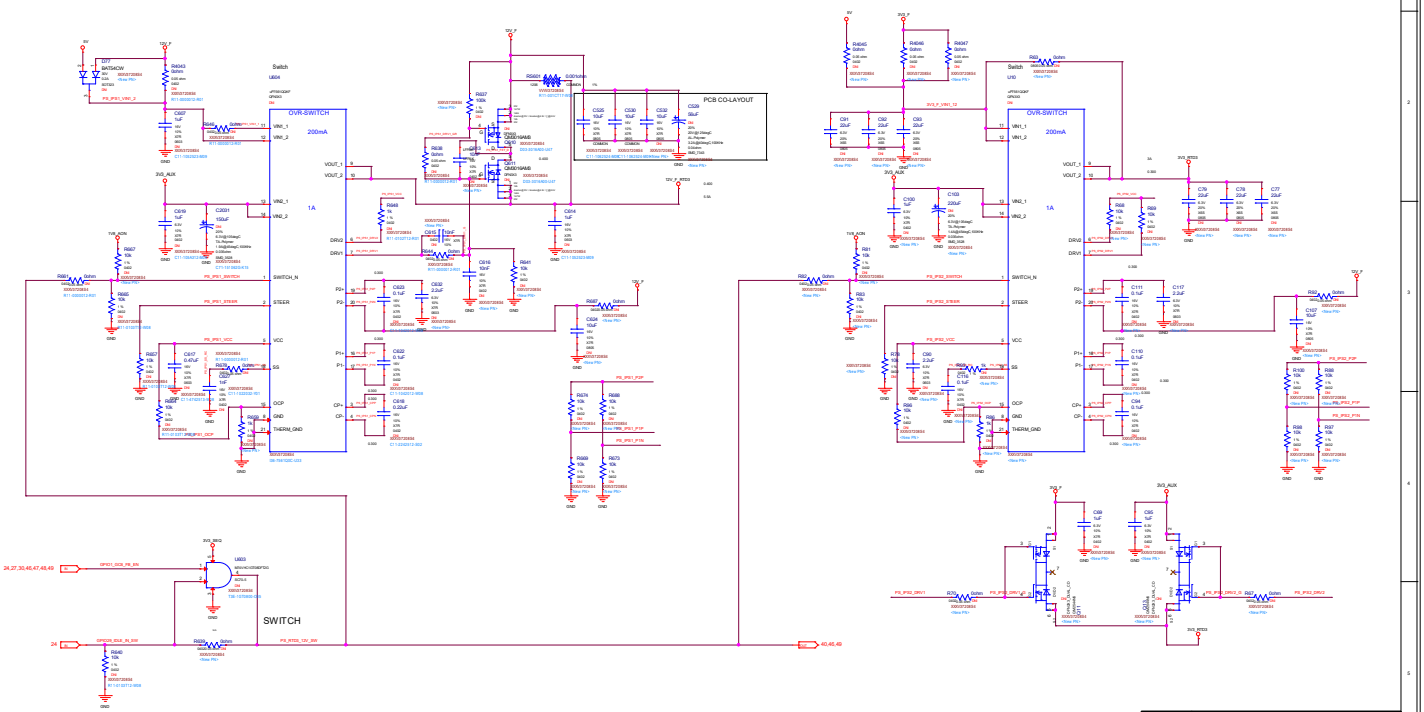
AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



MICRO-STAR INT'L CO.,LTD		
MS-V372		
Size: Custom	Document Description: PS: INPUT SWITCH RTD3	Rev: 3.1
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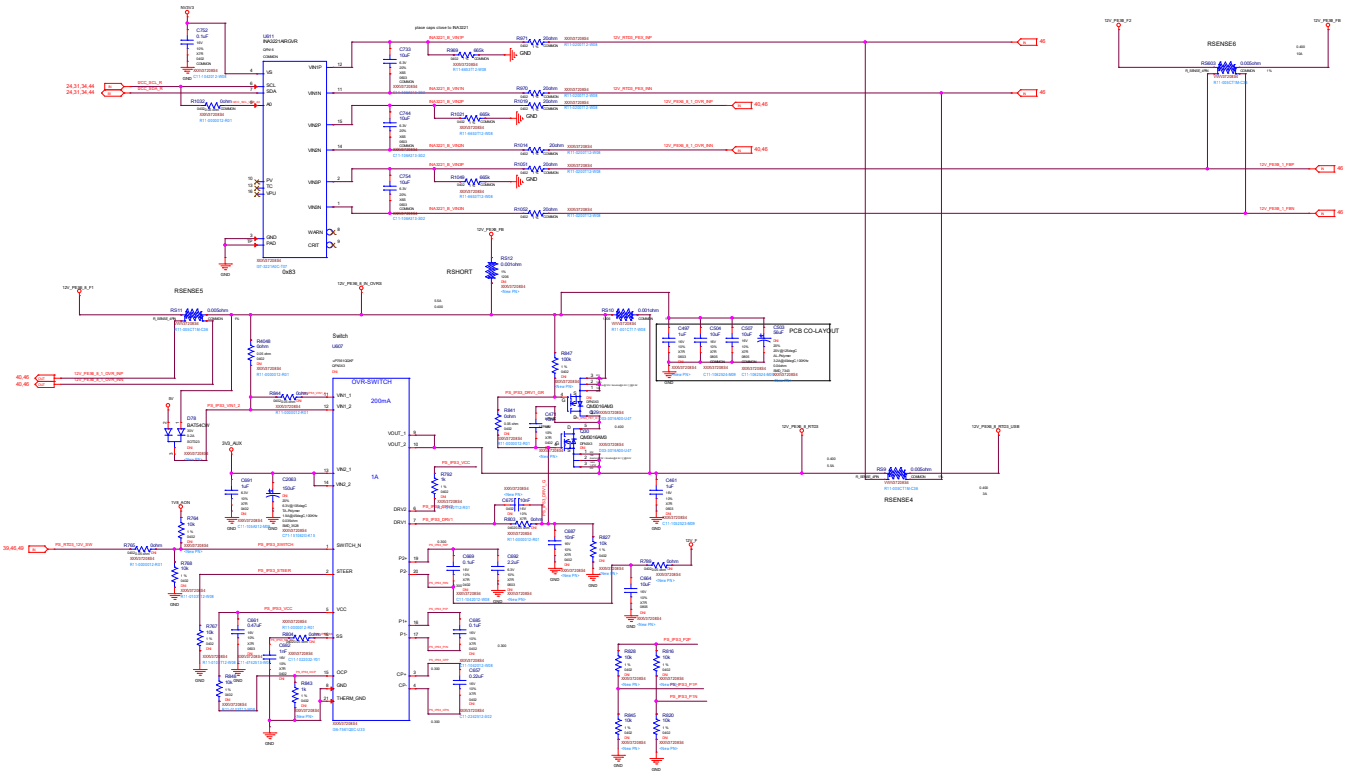
PAGE 40: PS: INPUT SWITCH RTD3 USB



MICRO-STAR INT'L CO.,LTD	
MS-V372	
Size: Custom	Document Description: PS: INPUT SWITCH RTD3 USB
Rev: 3.1	
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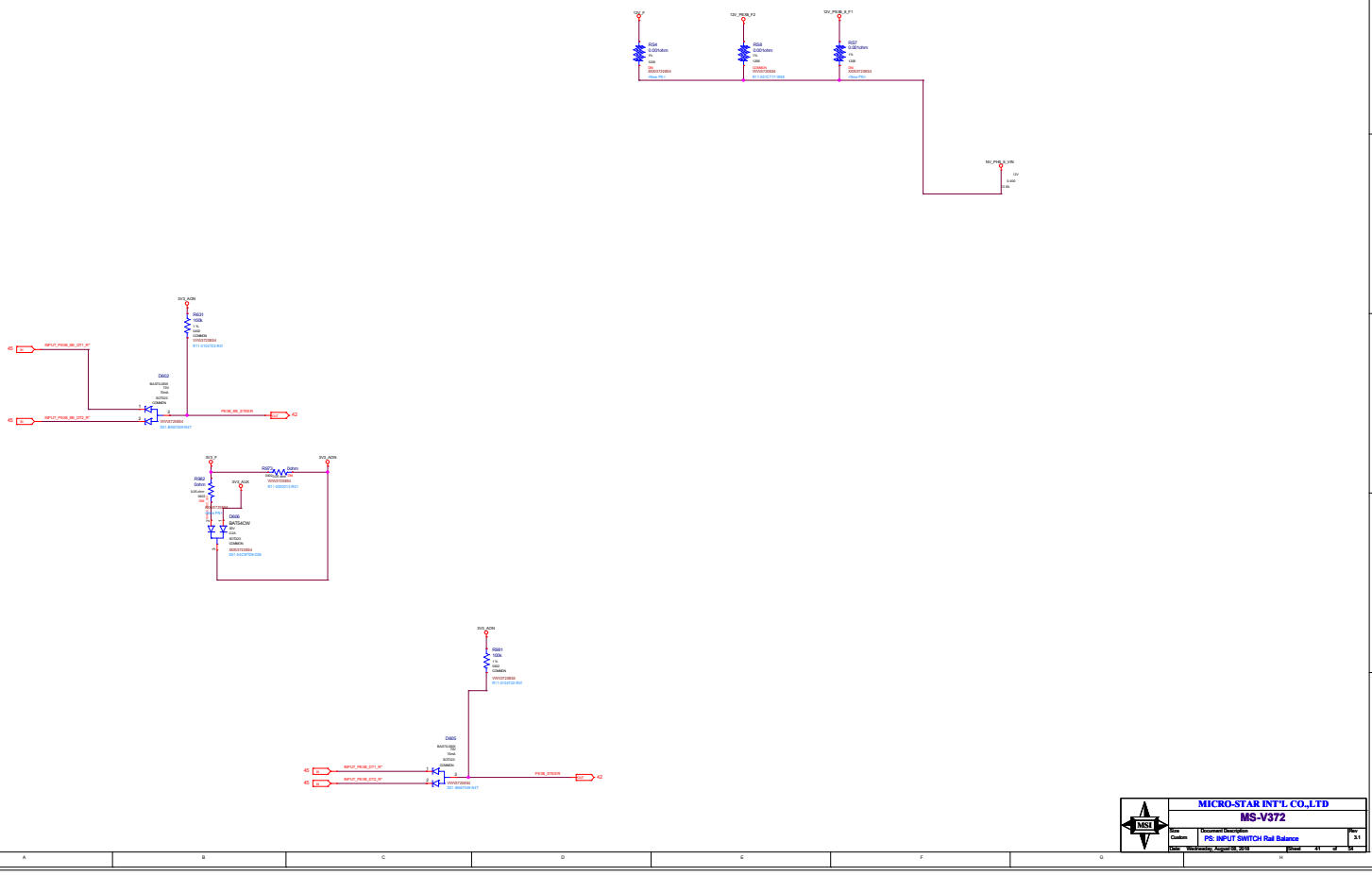
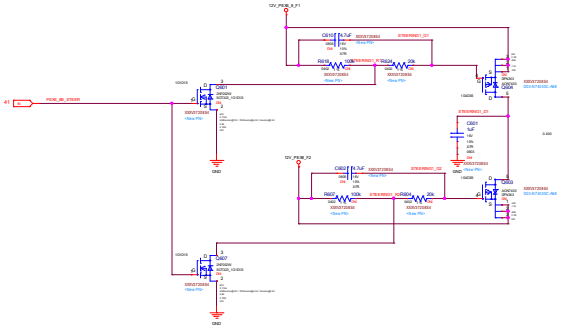
PAGE 41: PS: INPUT SWITCH Rail Balance



MICRO-STAR INT'L CO.,LTD	
MS-V372	
Size: Custom	Document Description: PS: INPUT SWITCH Rail Balance
Rev: 3.1	
Date: Wednesday, August 08, 2018	Sheet 41 of 54

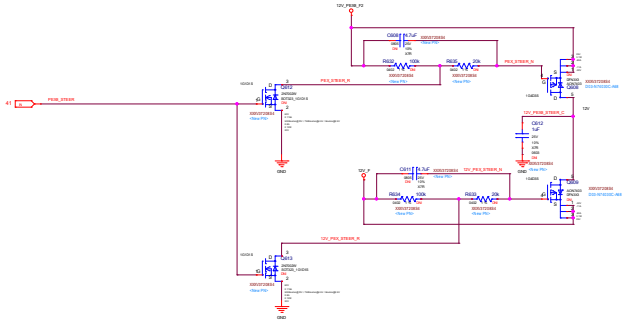
12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



MICRO-STAR INT'L CO.,LTD		
MS-V372		
Size: Custom	Document Description: PS: 12V CURRENT STEERING	Rev: 3.1
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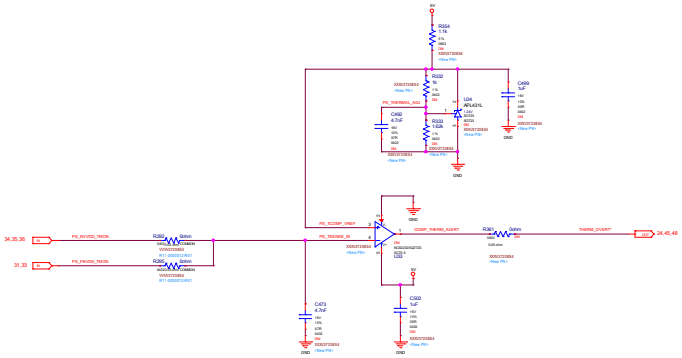

MICRO-STAR INT'L CO.,LTD			
MS-V372			
Size: Custom	Document Description: PS: VR THERMAL PROTECTION		Rev: 3.1
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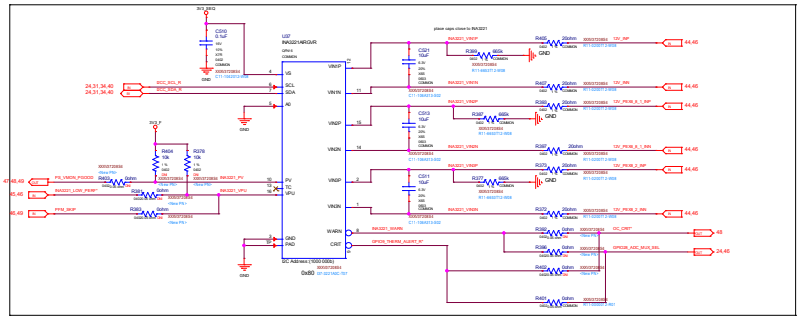
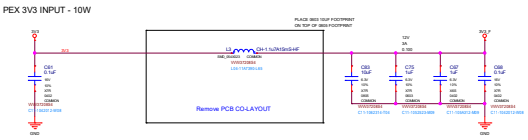
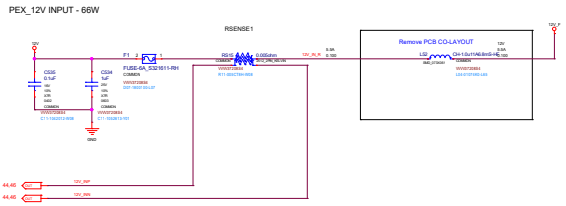
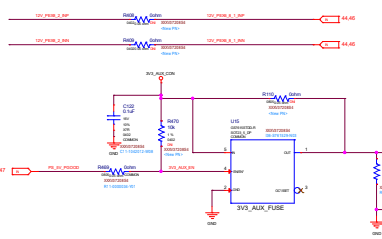
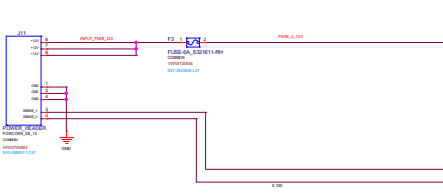
PAGE 44: PS: Inputs, Filtering, and Monitoring











MICRO-STAR INT'L CO.,LTD	
MS-V372	
Size: Custom	Document Description: PS: Inputs, Filtering, and Monitoring
Rev: 3.1	
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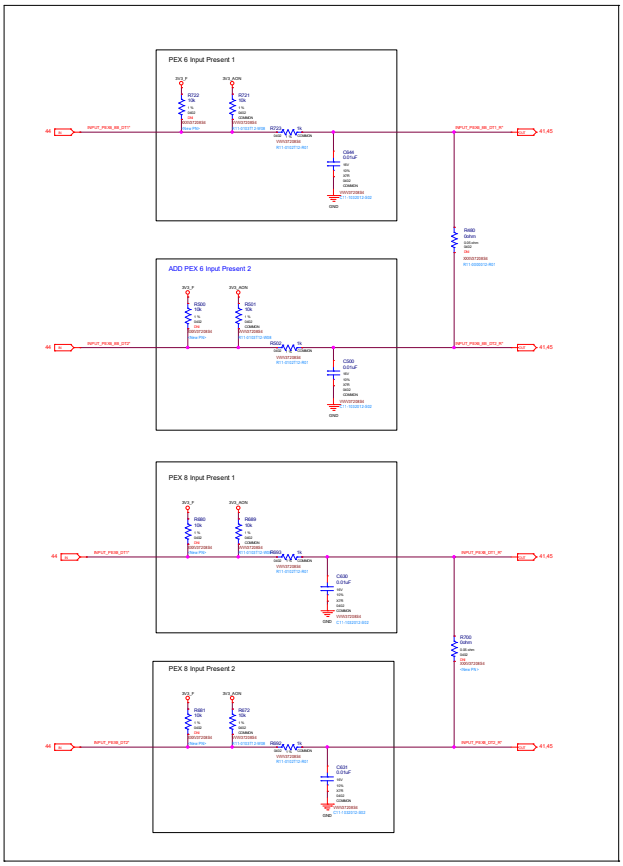
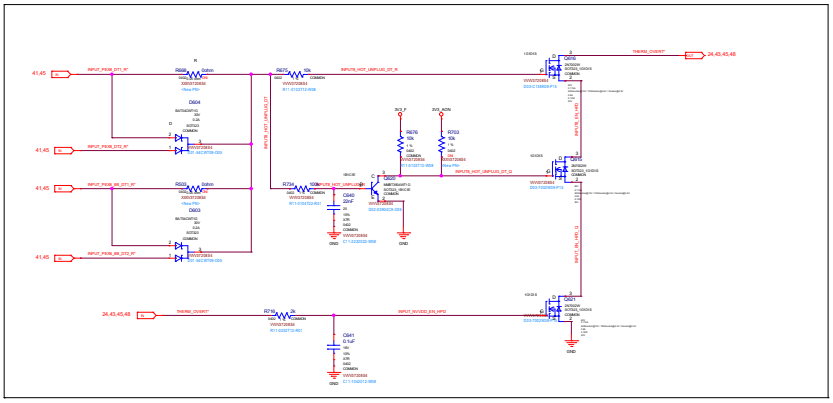
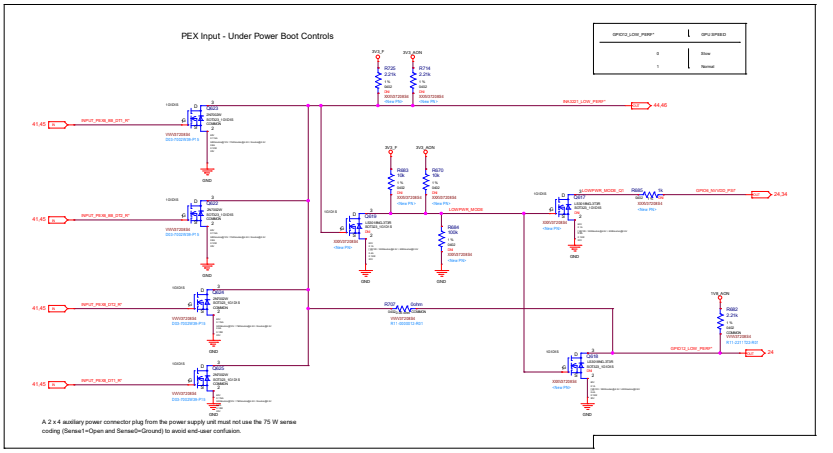
PAGE 45: PS: Current Steering, Hot Unplug Detect







MICRO-STAR INT'L CO.,LTD
MS-V372
Size: Custom
Document Description: PS: Current Steering, Hot Unplug Detect
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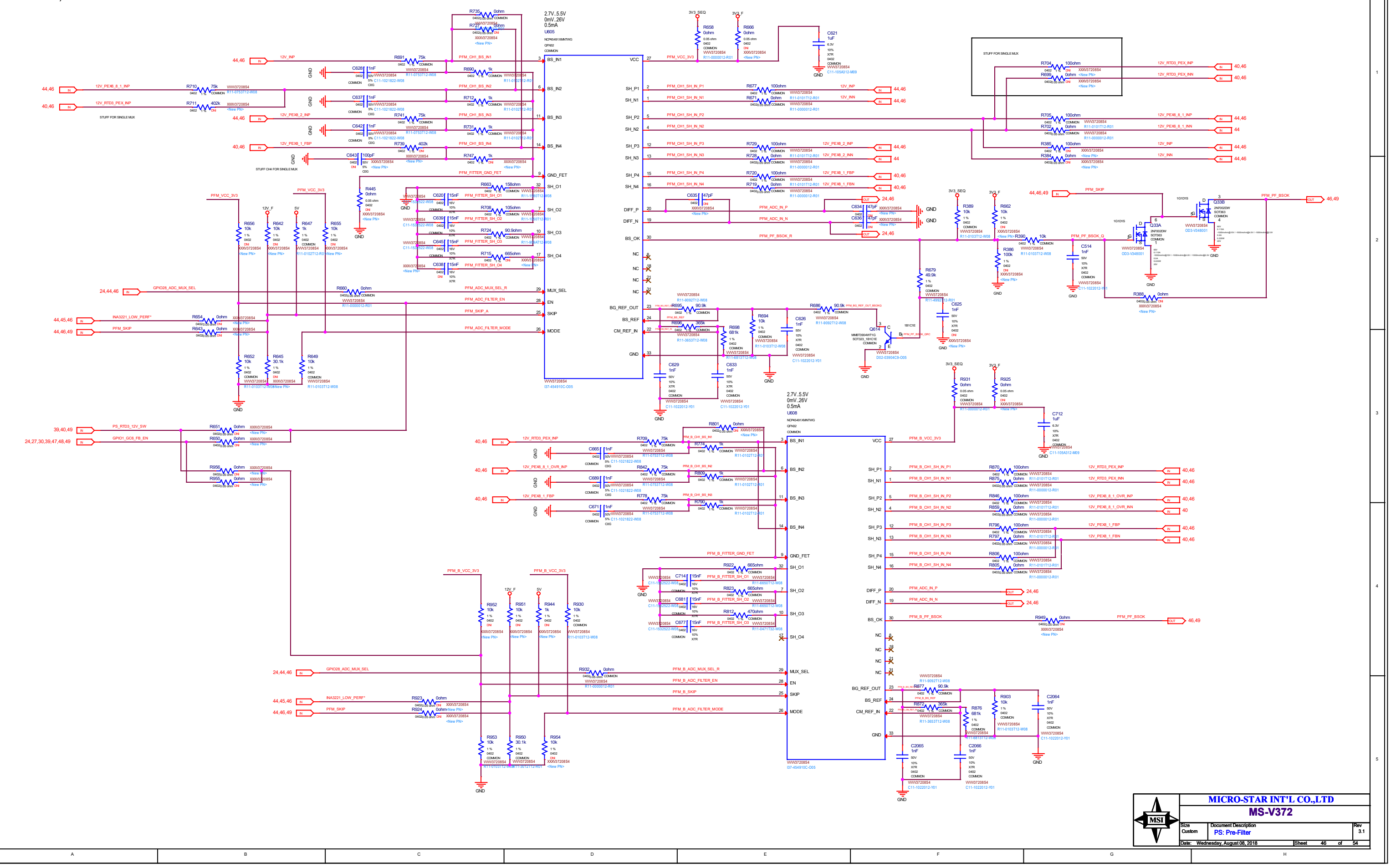
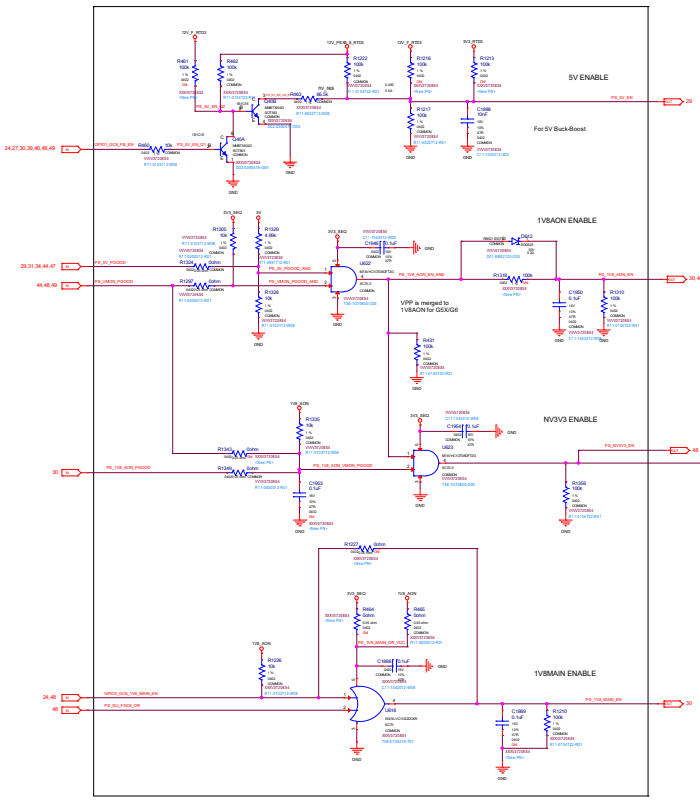
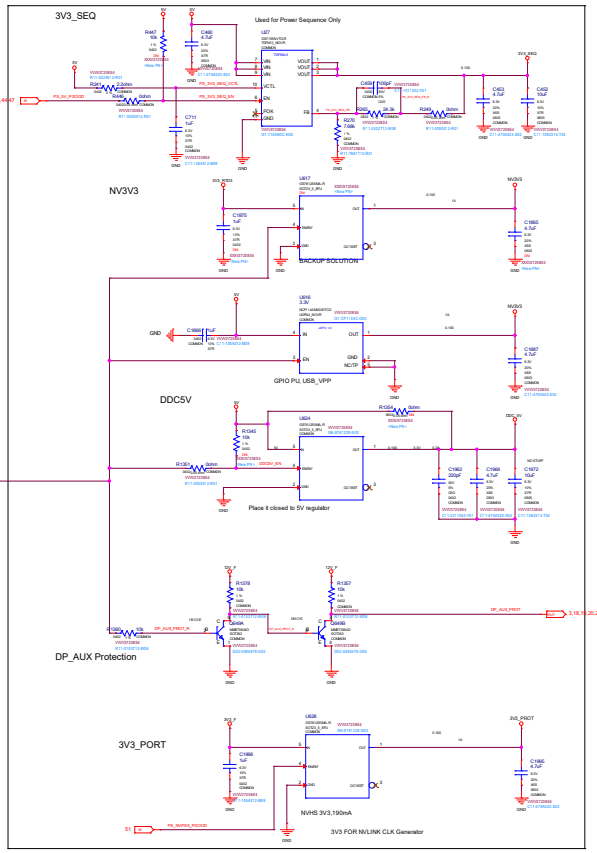
PAGE46; PS: Pre-Filter



PAGE 47: SEQUENCE:5V,1V8,NV3V3 ENABLE





MICRO-STAR INT'L CO.,LTD	
MS-V372	
Size: Custom	Document Description: SEQUENCE:5V,1V8,NV3V3 ENABLE
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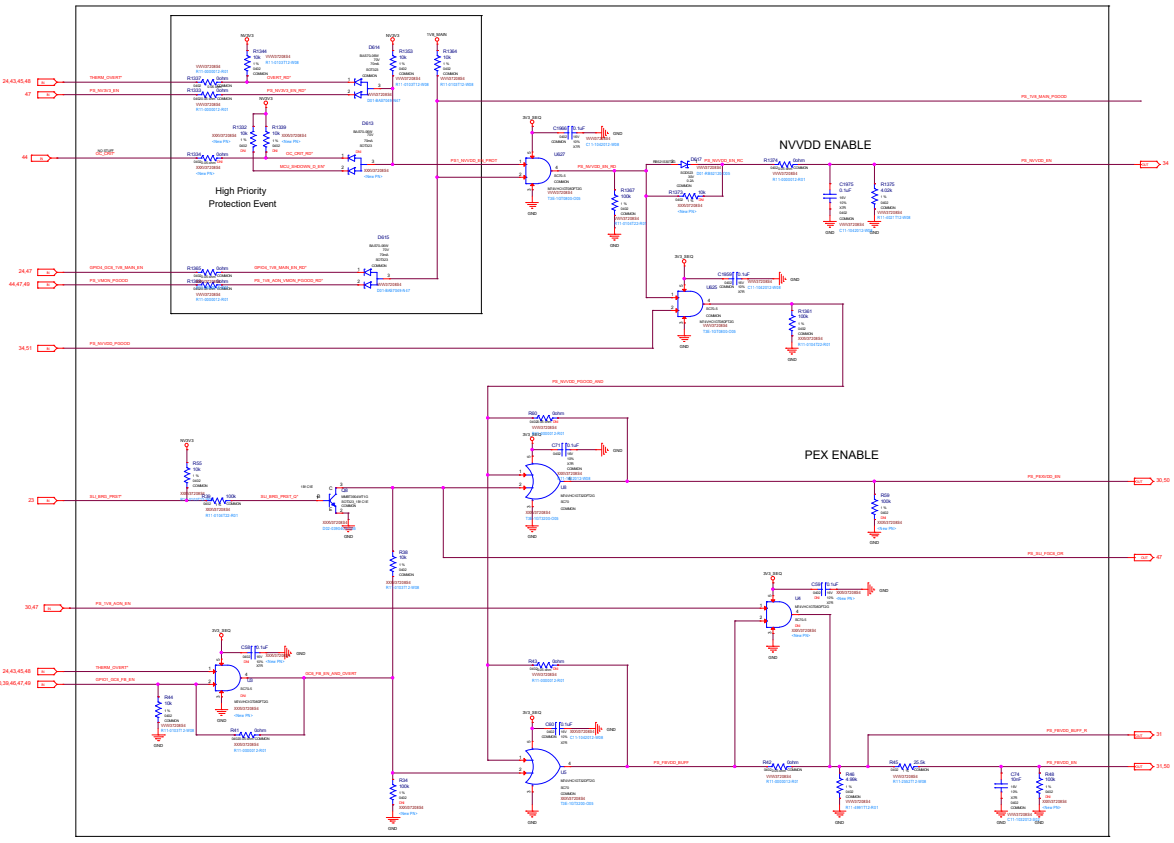
PAGE 48: SEQUENCE:NV,PEX,FB ENABLE



MICRO-STAR INT'L CO.,LTD			
MS-V372			
Size: Custom	Document Description: SEQUENCE:NV,PEX,FB ENABLE		Rev: 3.1
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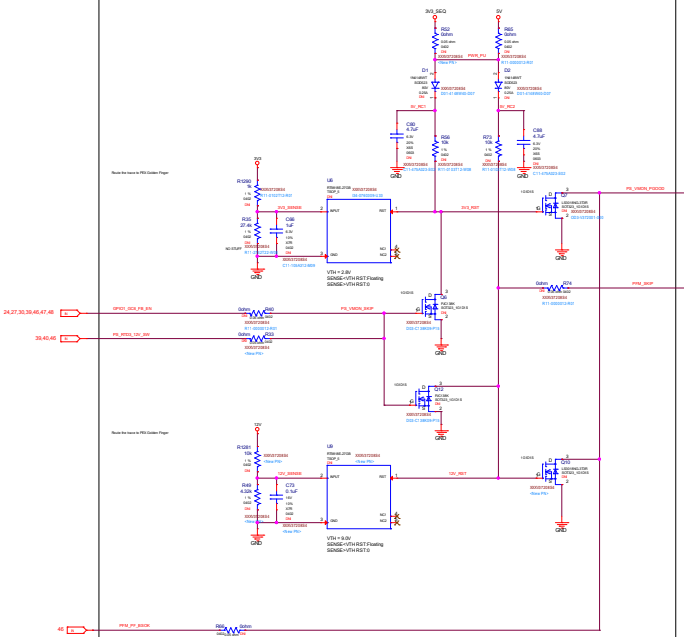
PCIE Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H):once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

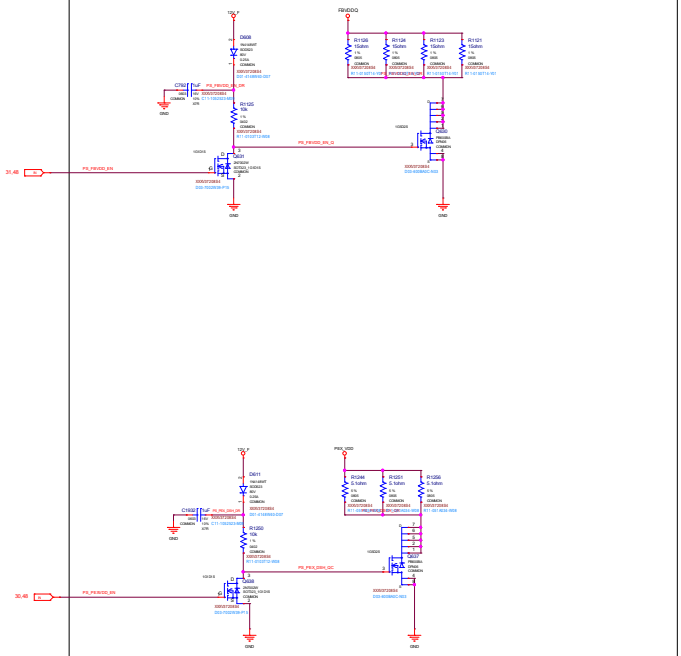
Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX

and All Input 12Vs

PAGE 50: SEQUENCE:DISCHARGE



MICRO-STAR INT'L CO.,LTD	
MS-V372	
Size: Custom	Document Description: SEQUENCE:DISCHARGE
Rev: 3.1	
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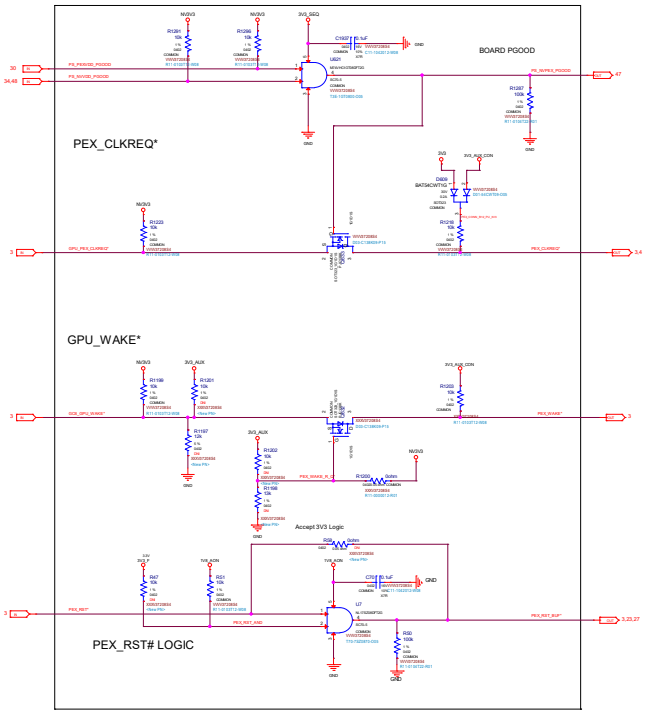

MICRO-STAR INT'L CO.,LTD	
MS-V372	
Size: Custom	Document Description: SEQUENCE-MISC
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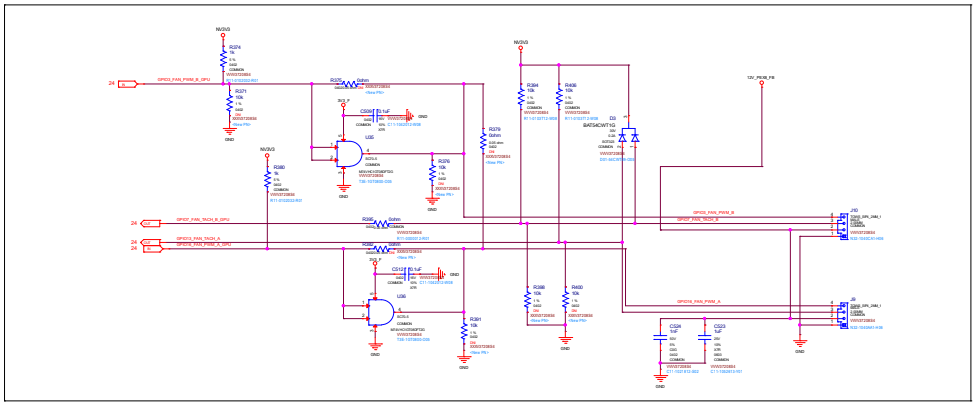
PAGE 52: LED & FAN HEADERS

Remove LED



Remove LED BOOST

MICRO-STAR INT'L CO.,LTD		
MS-V372		
Size: Custom	Document Description: LED & FAN HEADERS	Rev: 3.1
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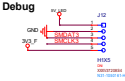
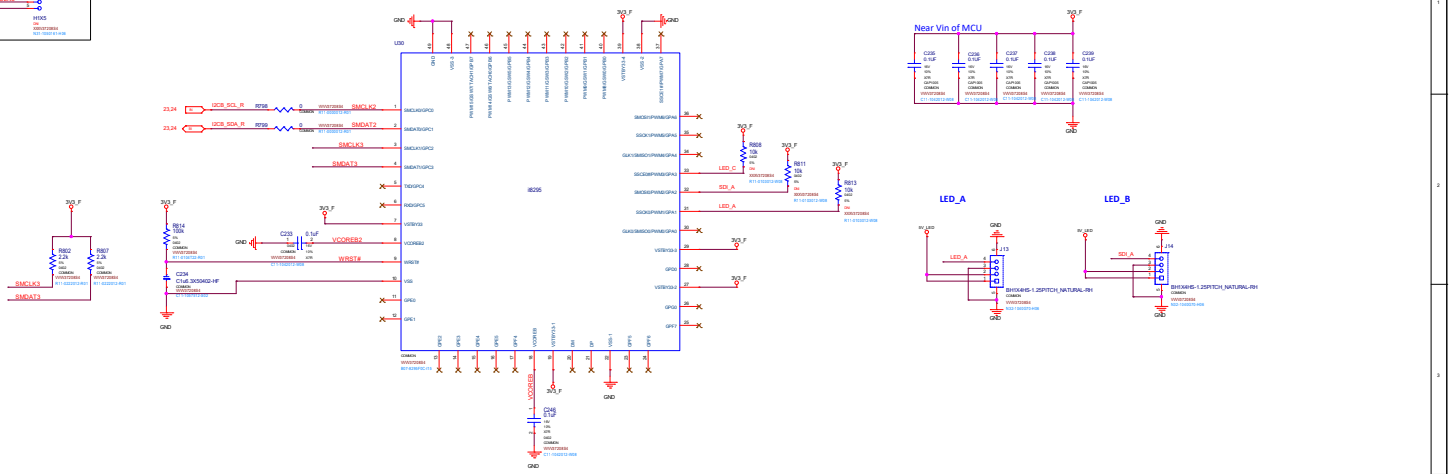
Page53: LED_CONTROLLER_IT8295

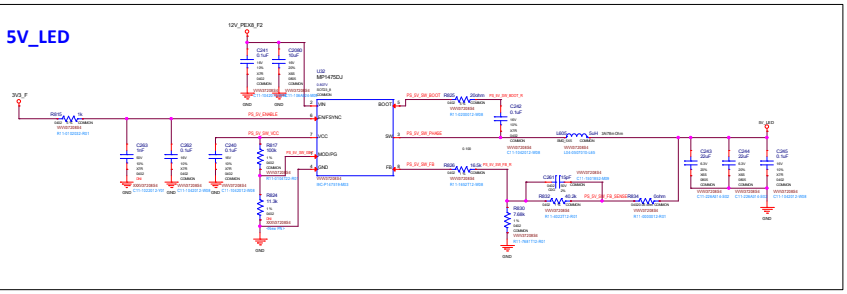
Firmware Programming

Debug





5V_LED



MICRO-STAR INT'L CO.,LTD		
MS-V372		
Size: Custom	Document Description: LED CONTROLLER_IT8295	Rev: 3.1
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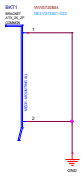
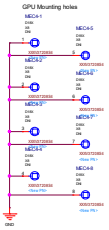
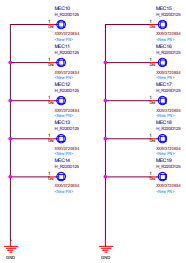
Brackets:



Screw



Mechanical Holes Symbol



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