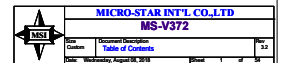
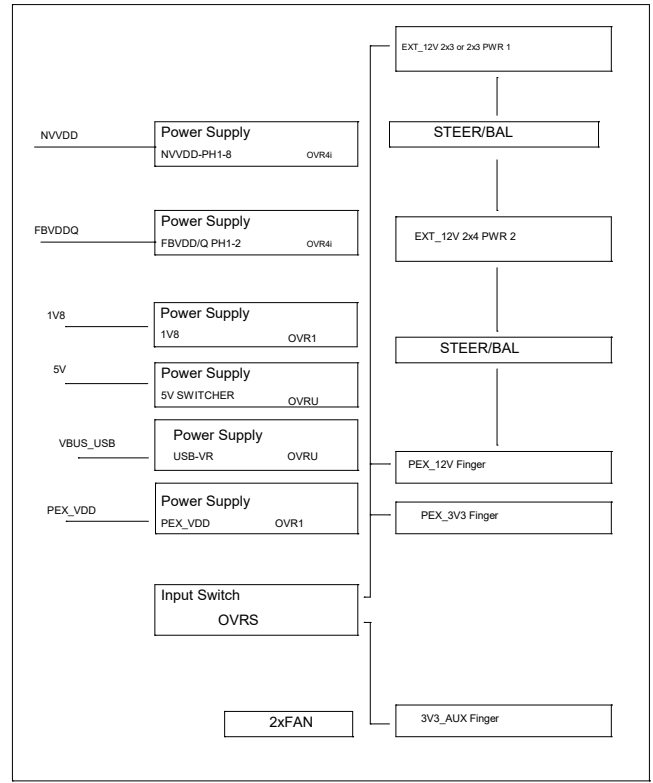
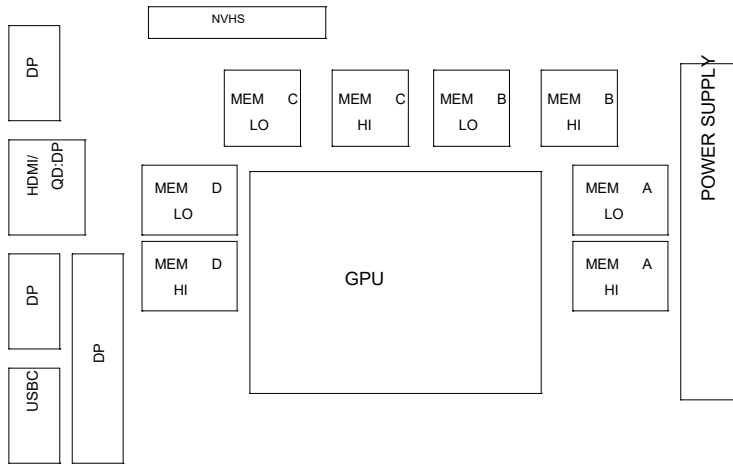
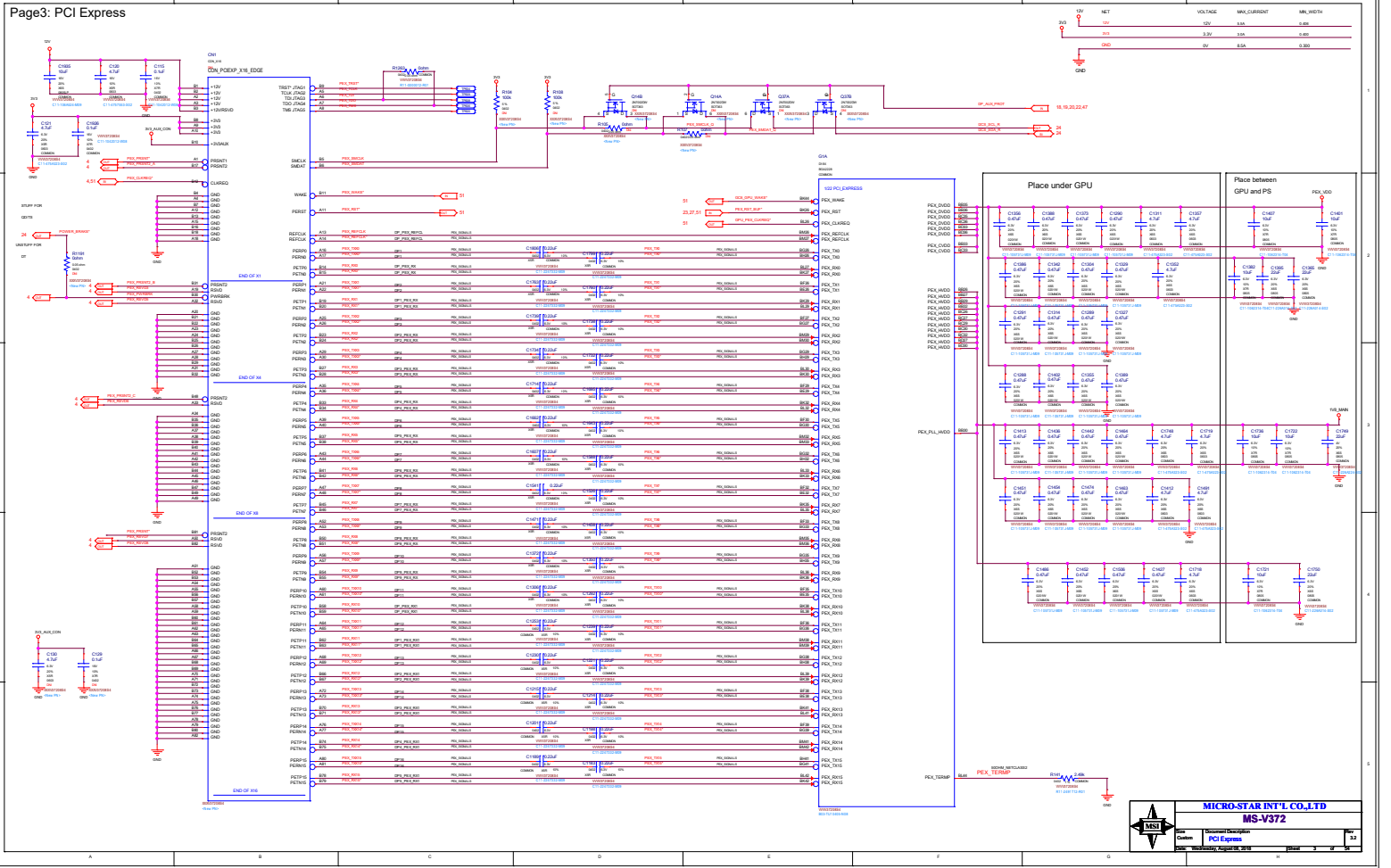


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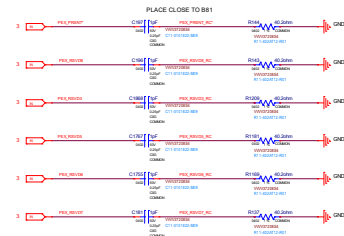
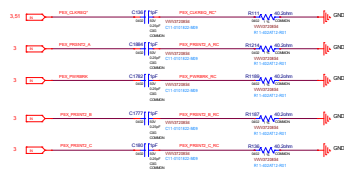
Page	Description	Page	Description	Page	Description
1	Table of Contents	41	PS: INPUT SWITCH RAIL BALANCE	V372-3.0	change List
2	Block Diagram	42	PS: 12V CURRENT STEERING	18	Change J4 footprint
3	PCI Express	43	PS: VR THERMAL PROTECTION	19	Change J3 footprint
4	PCI Termination	44	PS: INPUTS, FILTERING AND MONITORING	20	Remove DP co-layout
5	MEMORY: GPU Partition A/B	45	PS: CURRENT STEERING,HOT UNPLUG DETECT	21	Remove JTAG & unused GPIO
6	MEMORY: FBA Partition 31..0	46	PS: PRE-FILTER	32	Remove 0031_PS_ FBVDD CONTROLLER OVR3
7	MEMORY: FBA Partition 63..32	47	SEQUENCE: 5V, 1V8, NV3V3 ENABLE	34	NVVDV CONTROLLER change to MP2888A
8	MEMORY: FBB Partition 31..0	48	SEQUENCE: NV, PEX, FB ENABLE	35	DRMOS change to 10phases
9	MEMORY: FBB Partition 63..32	49	SEQUENCE: PCIE VOLTAGE MONITOR	36	DRMOS change to 10phases
10	MEMORY: GPU Partition C/D	50	SEQUENCE: DISCHARGE	37	Add NVVDV Output CAP
11	MEMORY: FBC Partition 31..0	51	SEQUENCE: MISC	41	Remove INPUT SWITCH Rail Balance
12	MEMORY: FBC Partition 63..32	52	LED & FAN HEADERS	44	J8 change to 8pin
13	MEMORY: FBD Partition 31..0	53	LED 2		Add Fuse F1~F3
14	MEMORY: FBD Partition 63..32	54	Mechanical: Bracket/Thermal Solution		Change 12V input choke footprint
15	GPU PWR and GND			45	Add Hot Unplug Detect for J8
16	GPU Decoupling			52	Add Remove LED & Fan Vin_12V option
17	GPU DECOUPLING			53	Add MCU IT8295 for RGB LED
18	IFPAB TALL-DP				
19	IFPE DP			V372-3.1	change List
20	IFPF USBC				Base on V372-3.0 · No changed
21	IFPC HDMI 2.0/DP				
22	IFPD DP			V372-3.2	change List
23	NVHS INTERFACE				Base on V372-3.0 · No changed
24	MISC: FAN,THERMAL,JTAG,GPIO,STEREO				
25	MISC3: ROM, STRAPS				
26	MISC: XTAL, PLL				
27	MISC: USB PPC				
28	PS: USB VR				
29	PS: 5V, 5V BACKUP				
30	PS: PEXVDD, 1V8				
31	PS: FBVDD CONTROLLER				
32	PS: FBVDD CONTROLLER OVR3				
33	PS: FBVDD PHASE 1, 2				
34	PS: NVVDV CONTROLLER OVR8				
35	PS: NVVDV Phase 1, 2				
36	PS: NVVDV Phase 3, 4				
37	PS: NVVDV Phase 5, 6				
38	PS: NVVDV Phase 7, 8				
39	PS: INPUT SWITCH RTD3				
40	PS: INPUT SWITCH RTD3 USB				

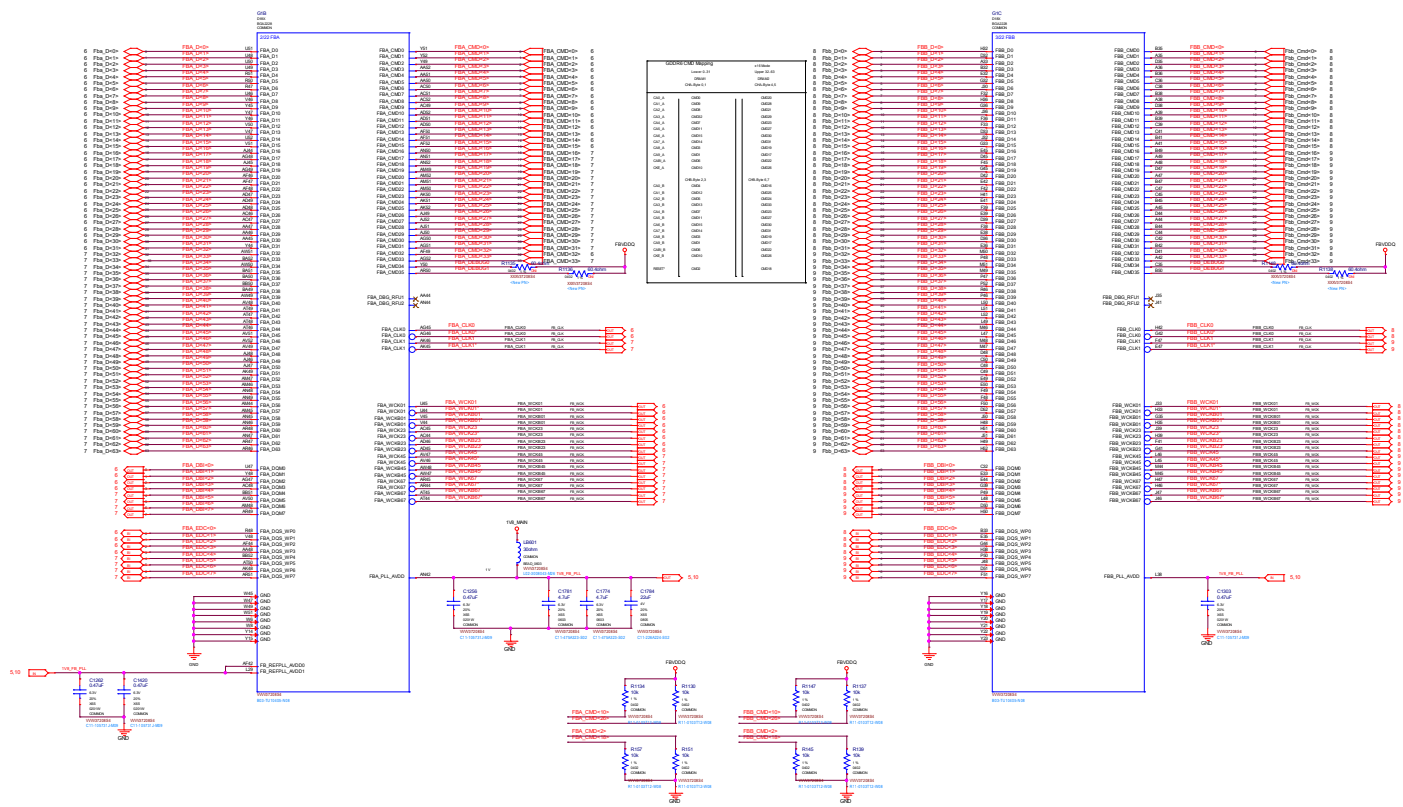


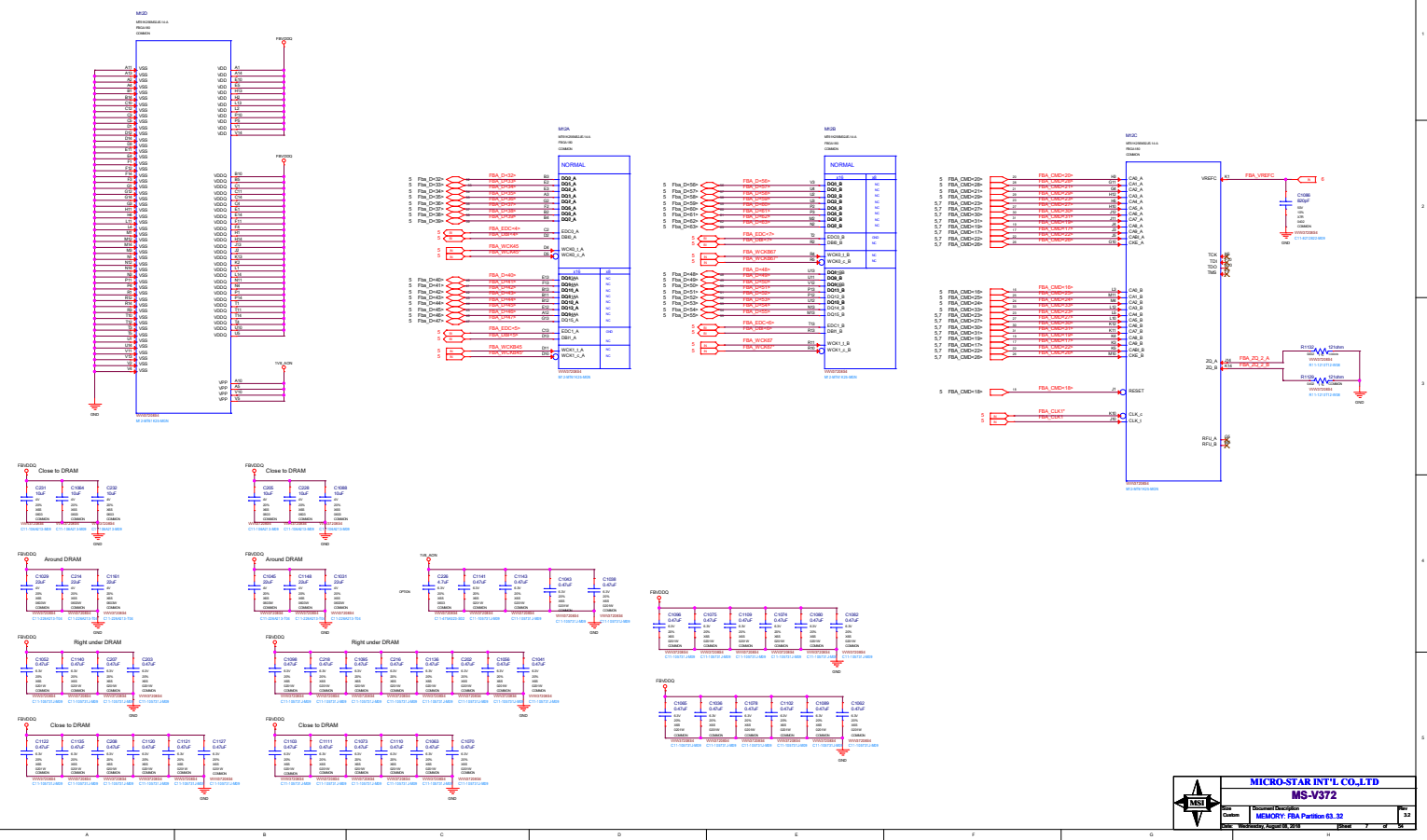




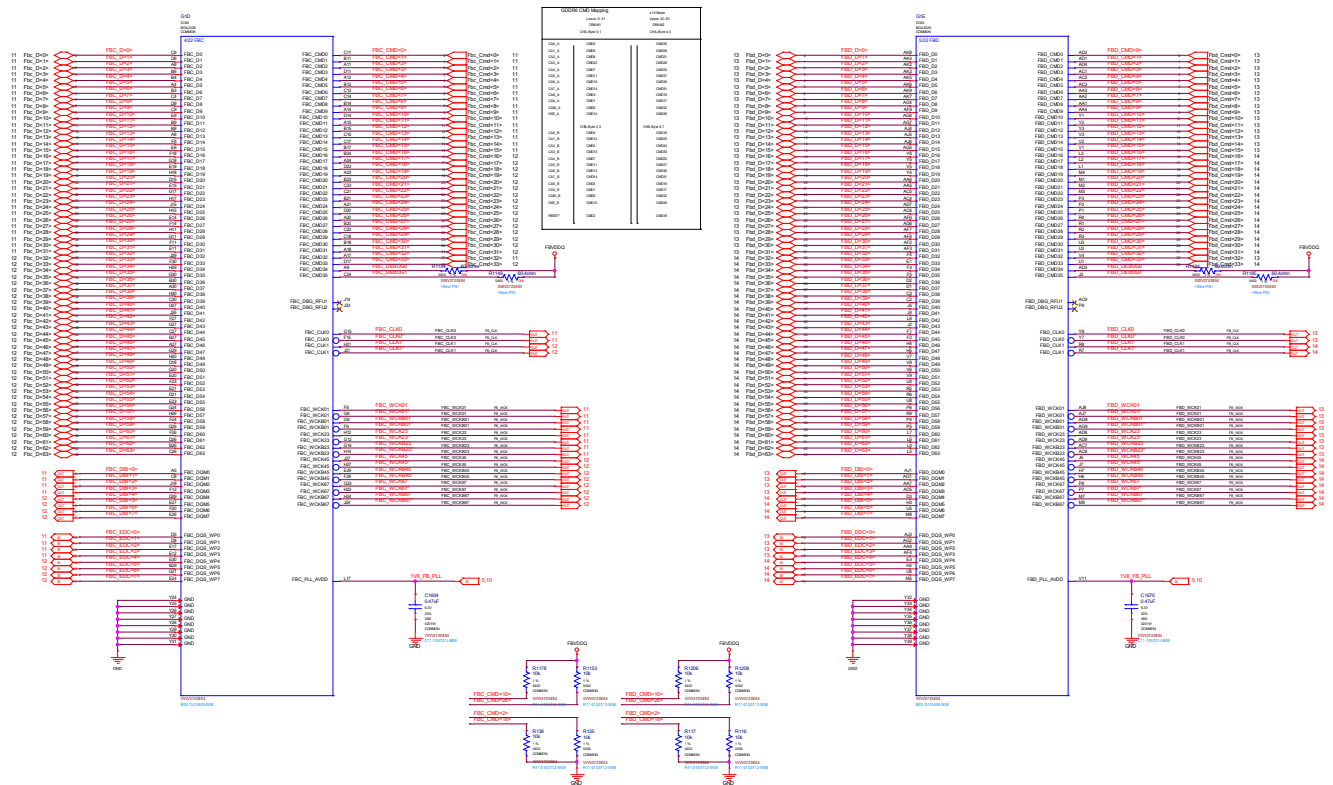
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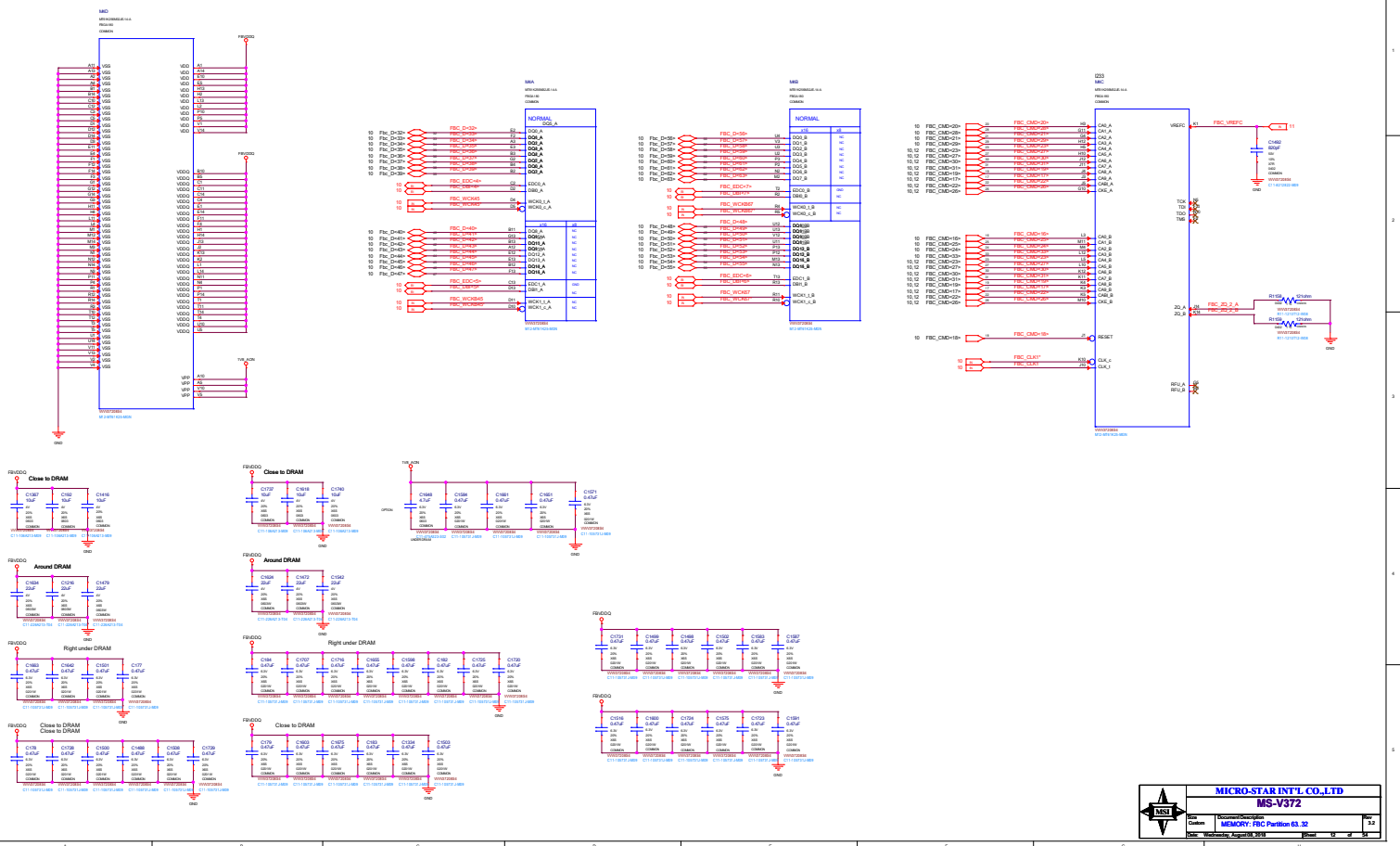


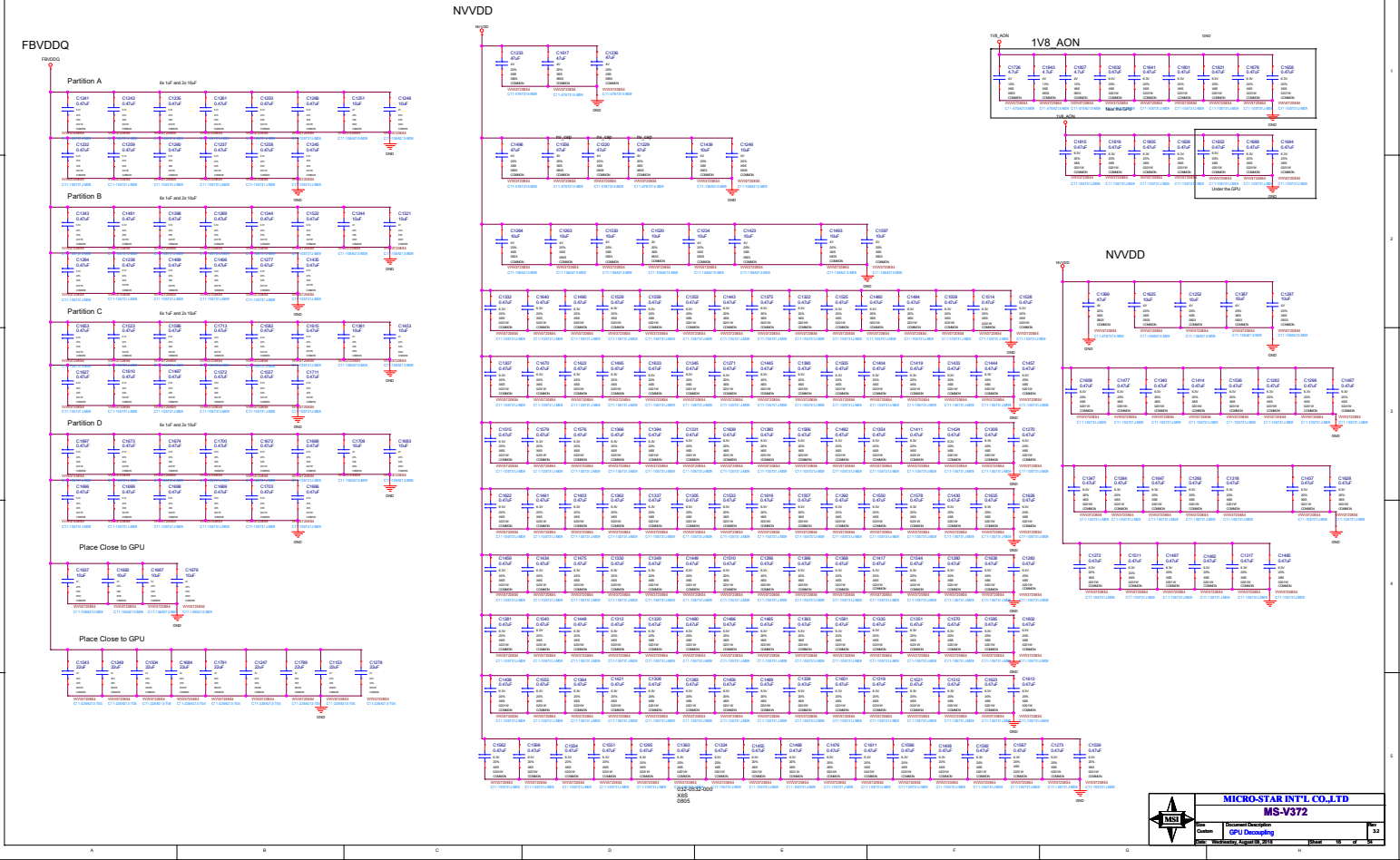


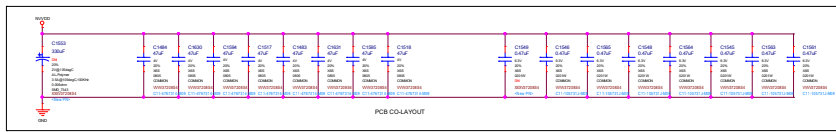
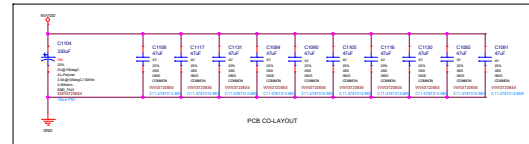
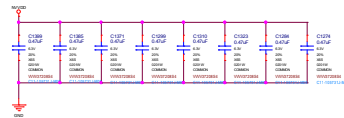
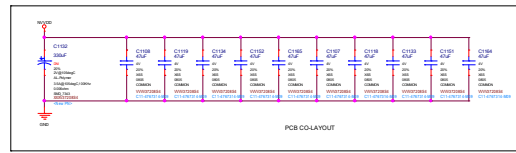
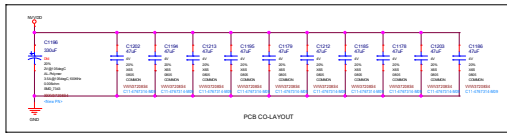
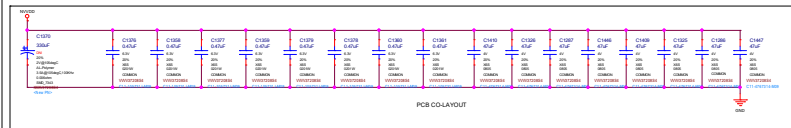


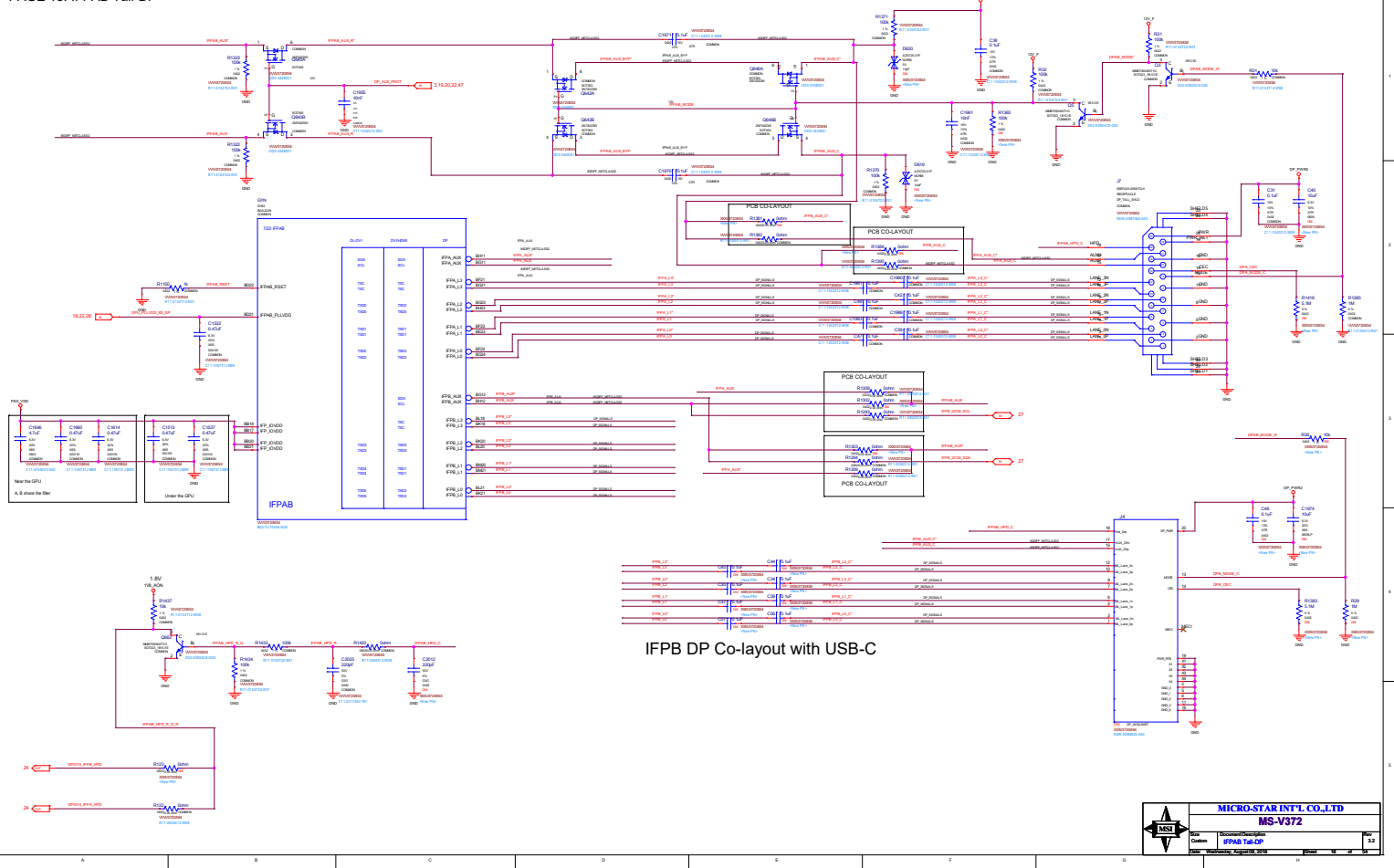
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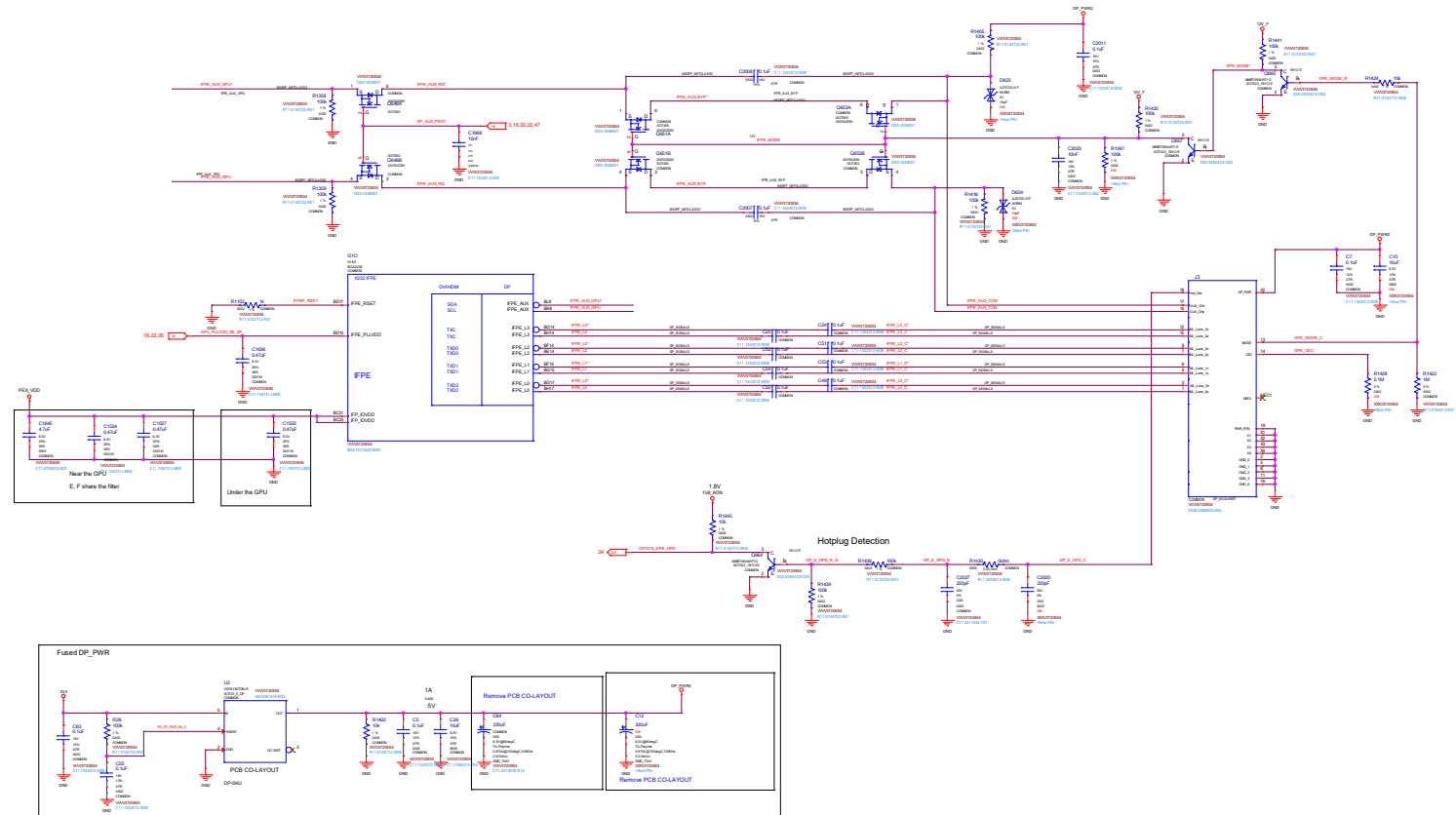


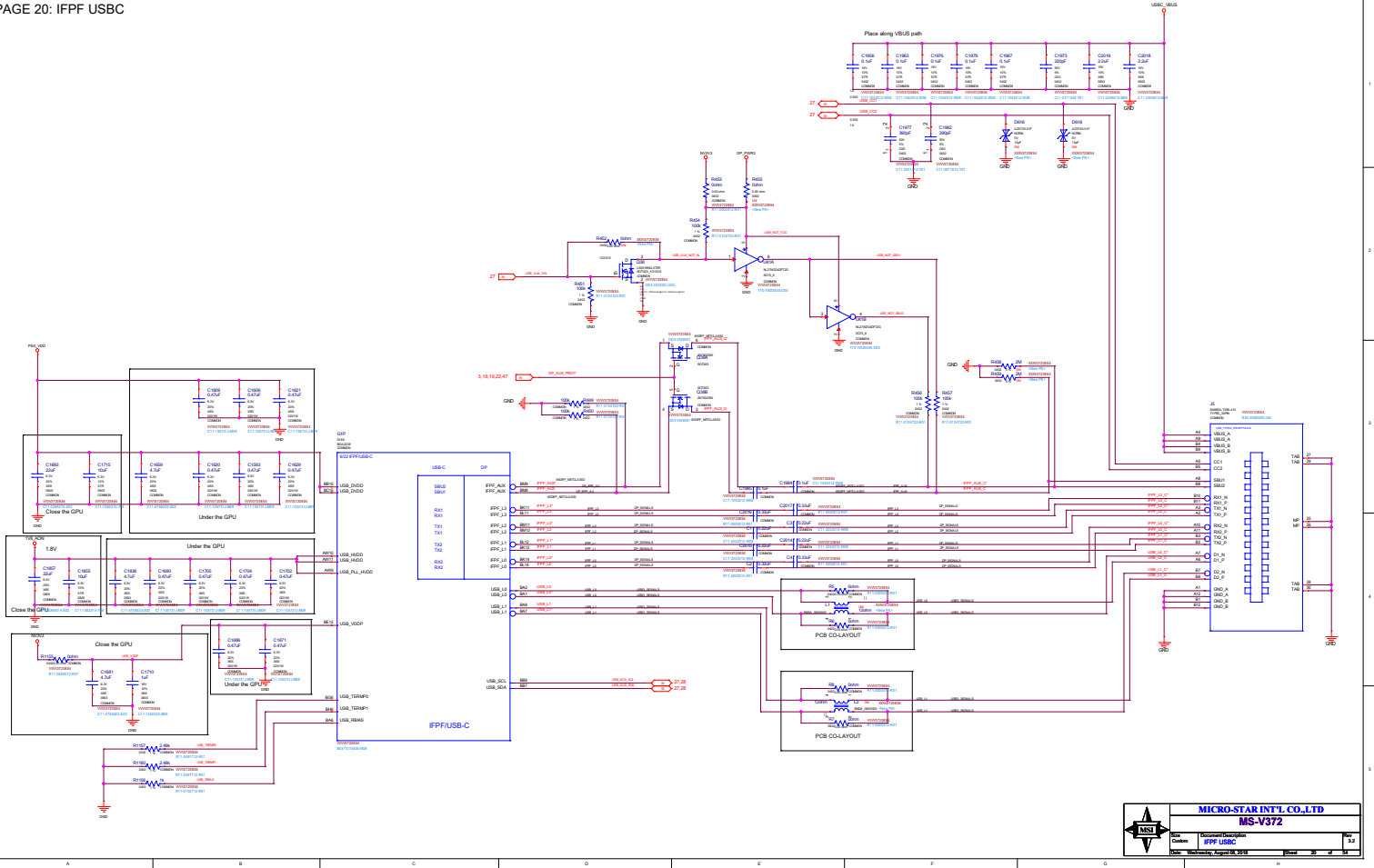




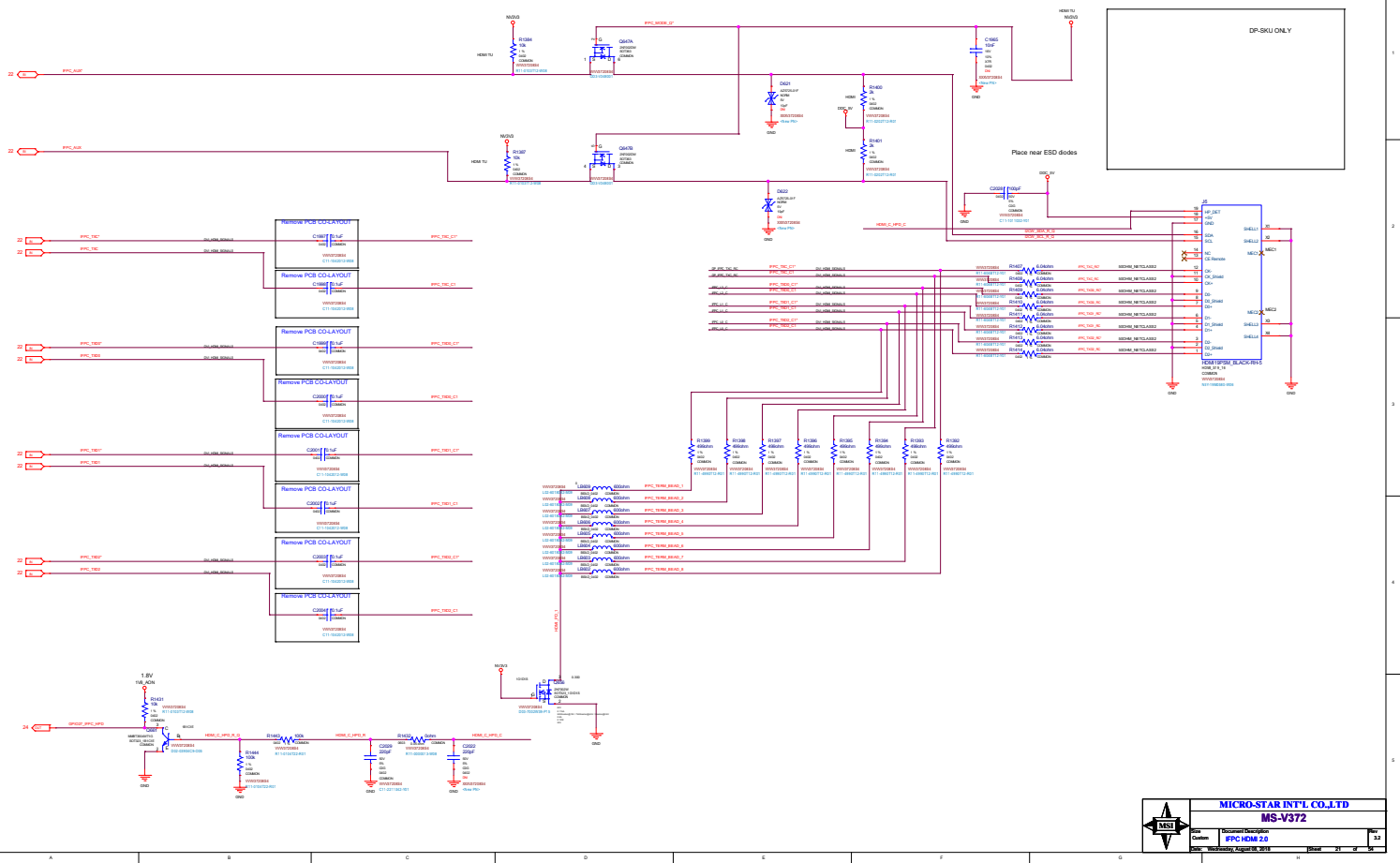




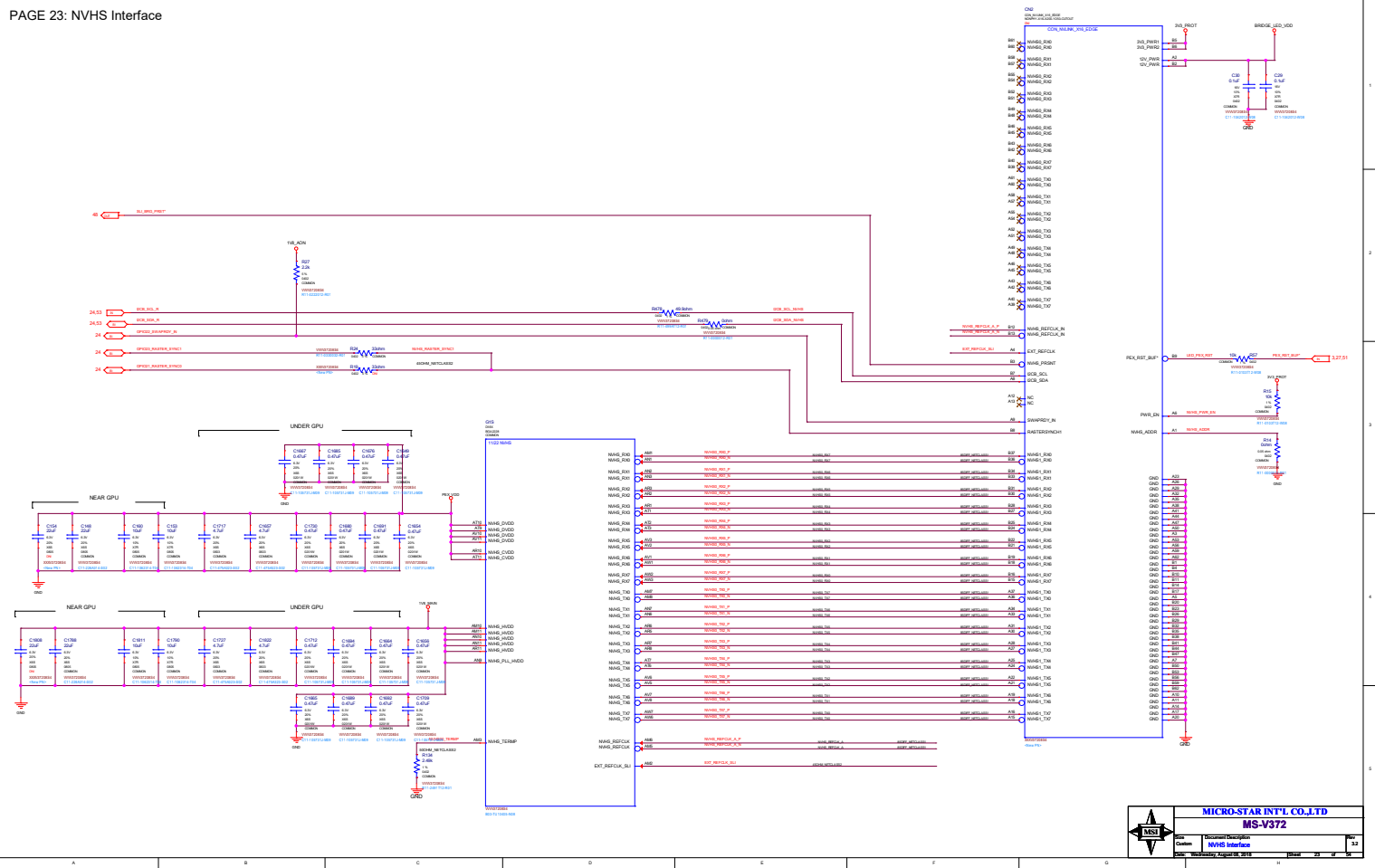


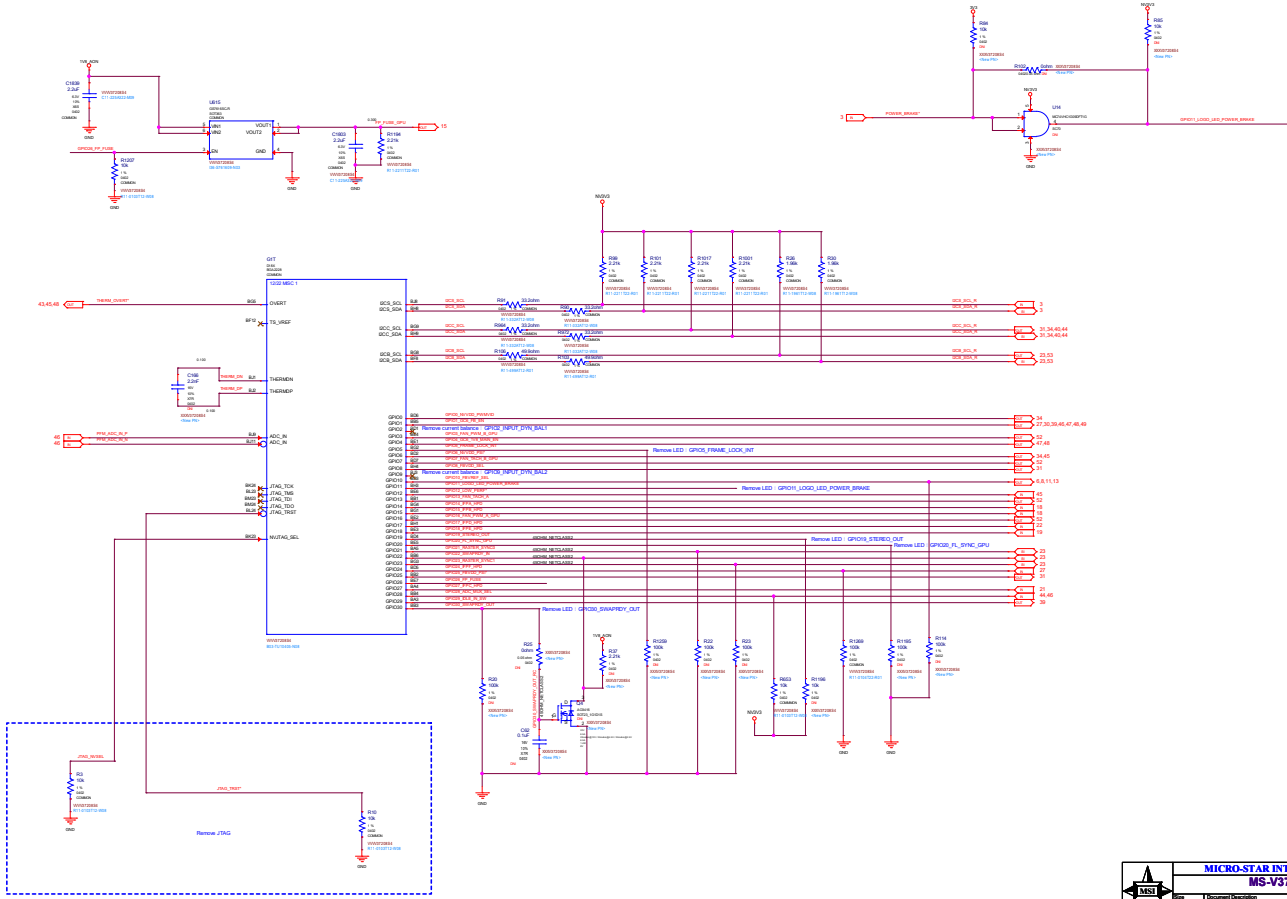


MICRO-STAR INT'L CO., LTD	
MS-V372	
Part No.	IFPF USBC
Rev.	1.0
Issue Date	2023/08/08









H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

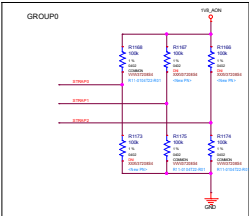
DEFAULT

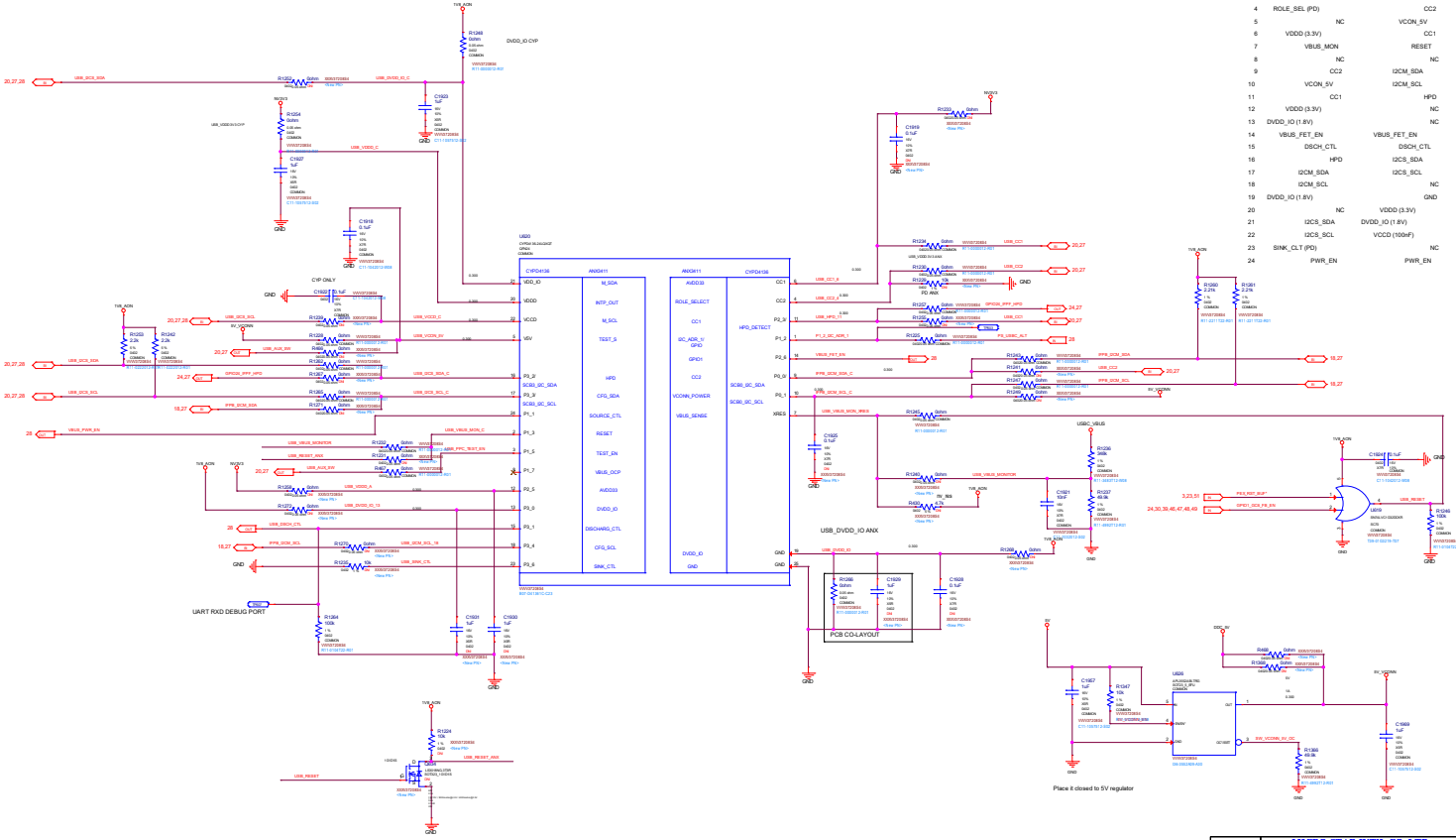
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Default

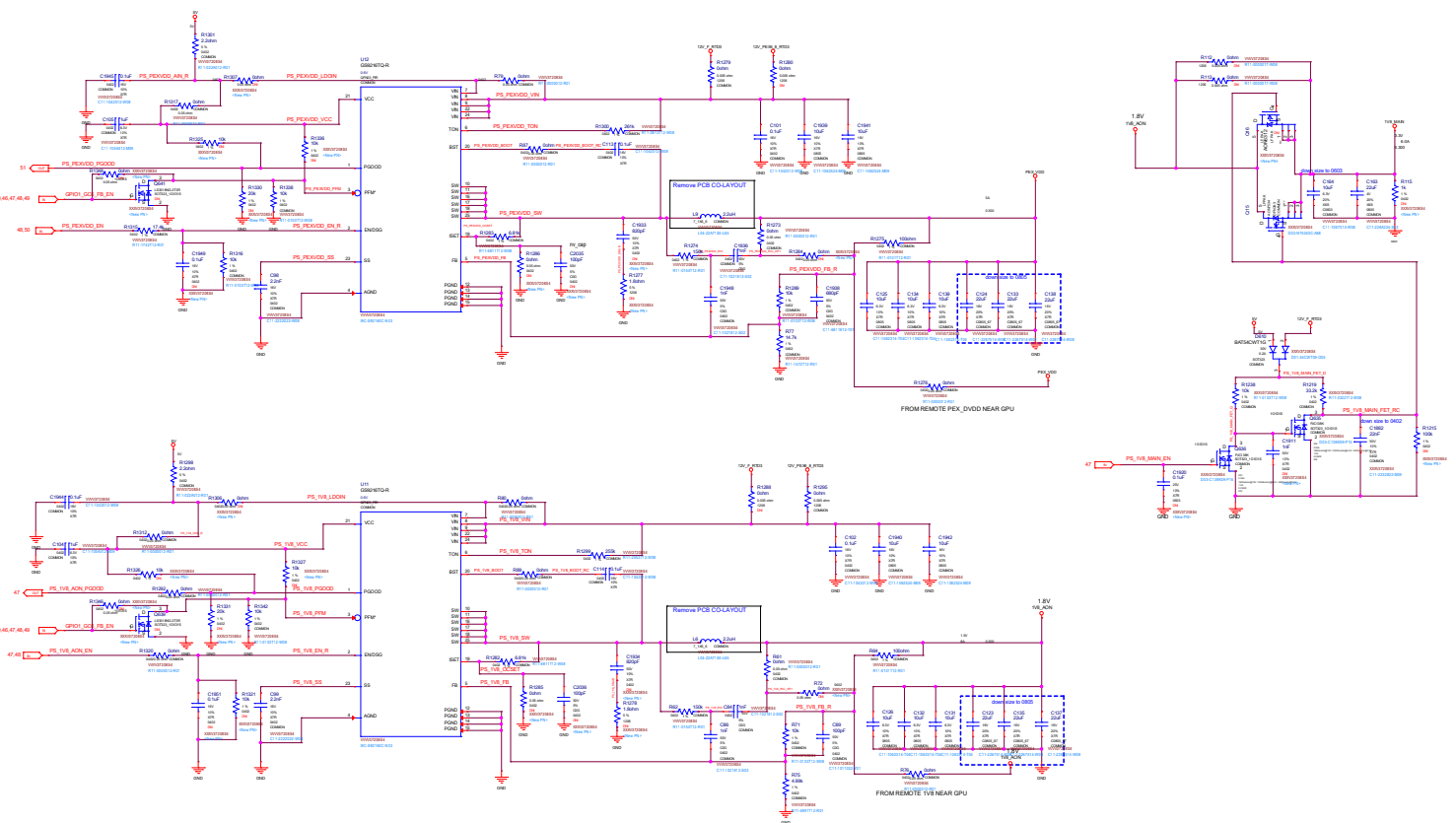
RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung

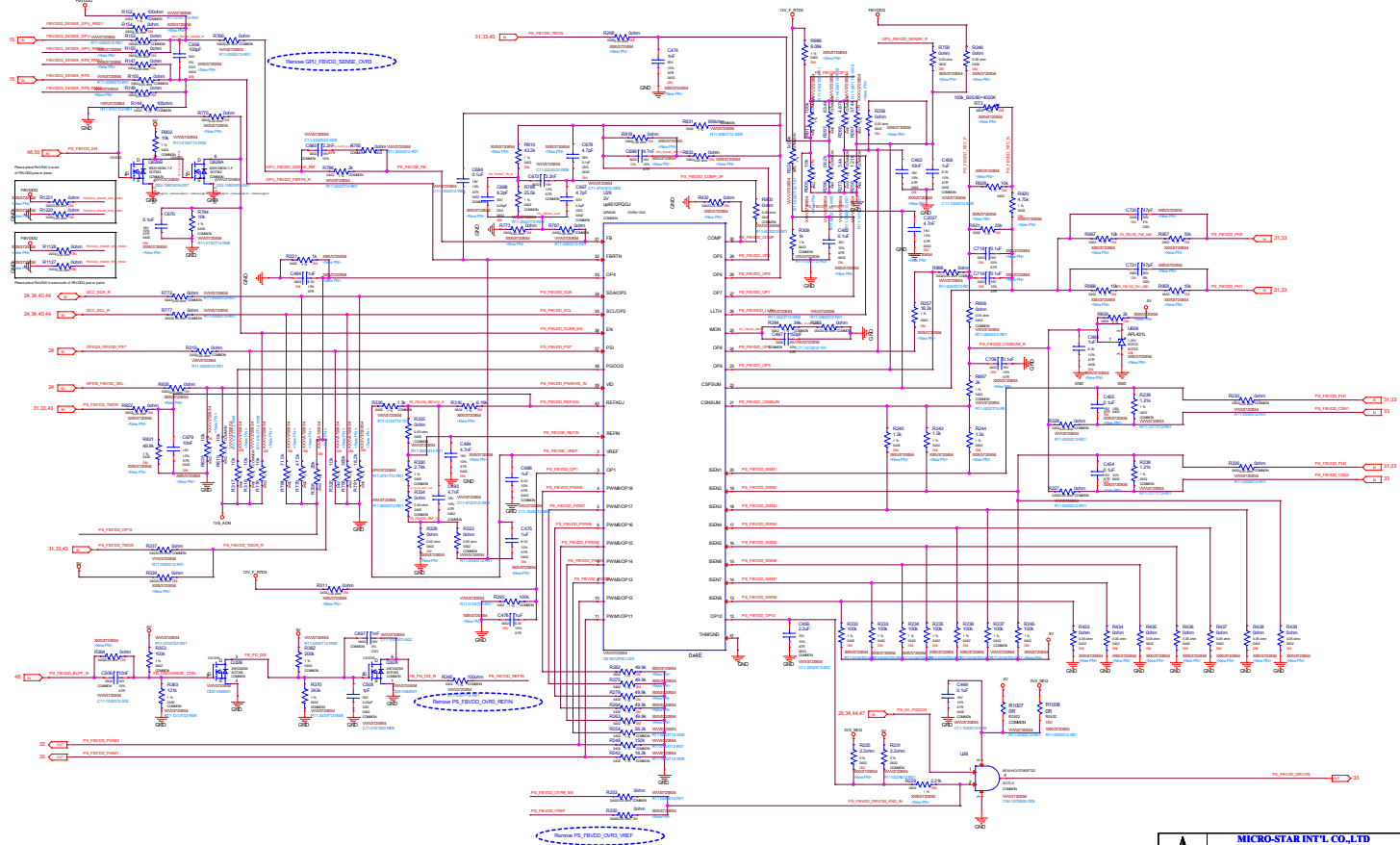




PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3		NC
4	ROLE_SEL_P0	CC2
5	NC	VCOM_SV
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	DCM_SDA
10	VCOM_SV	DCM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DISCH_CTL	DISCH_CTL
16	HPD	DCS_SDA
17	DCM_SDA	DCS_SCL
18	DCM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	DCS_SDA	DVDD_IO (1.8V)
22	DCS_SCL	VDDD (100mV)
23	SNK_CLT_P0	NC
24	PWR_EN	PWR_EN

**MICRO-STAR INT'L CO., LTD**
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MICRO-STAR INT'L CO., LTD

MS-V372

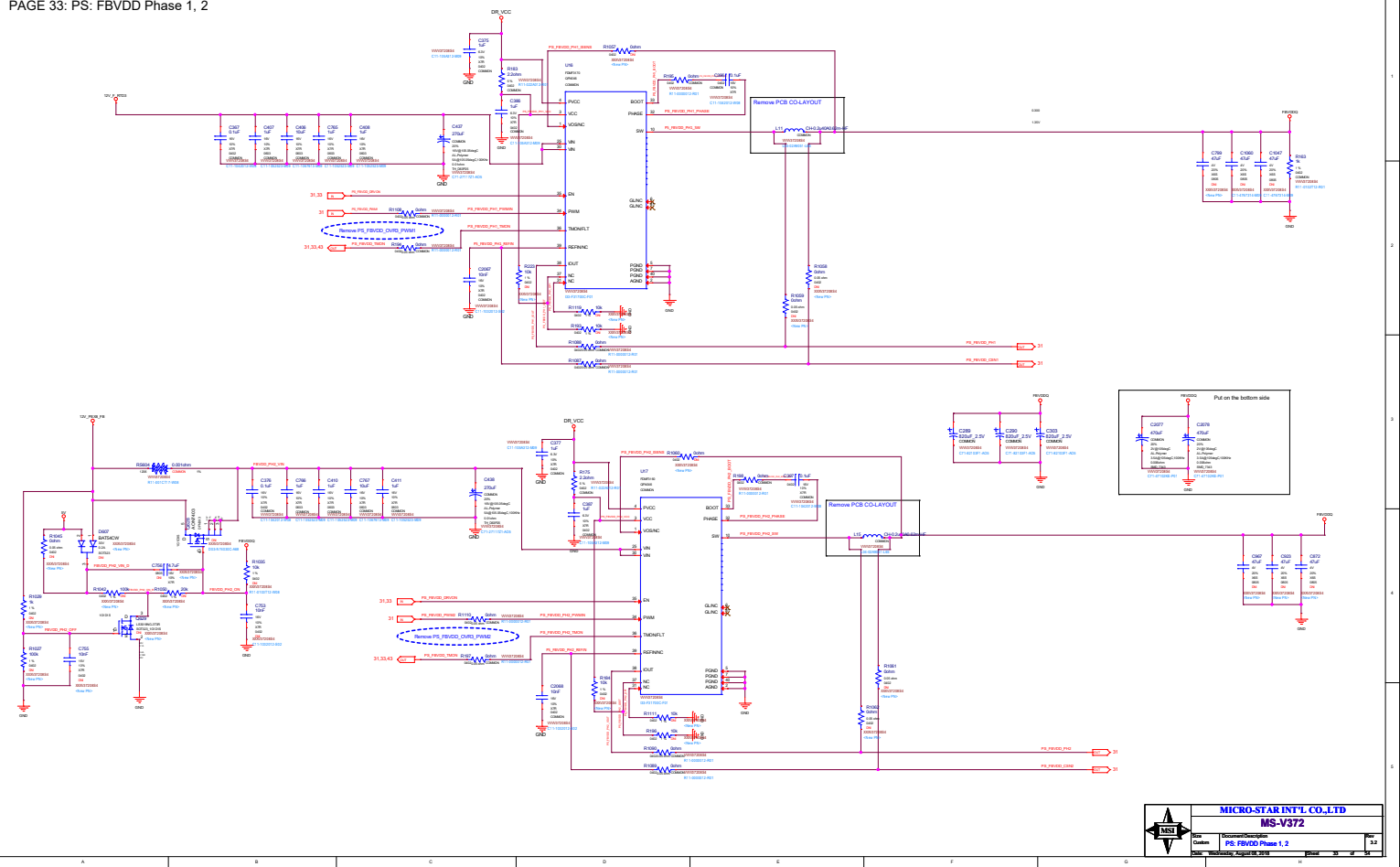
Version: 1.0

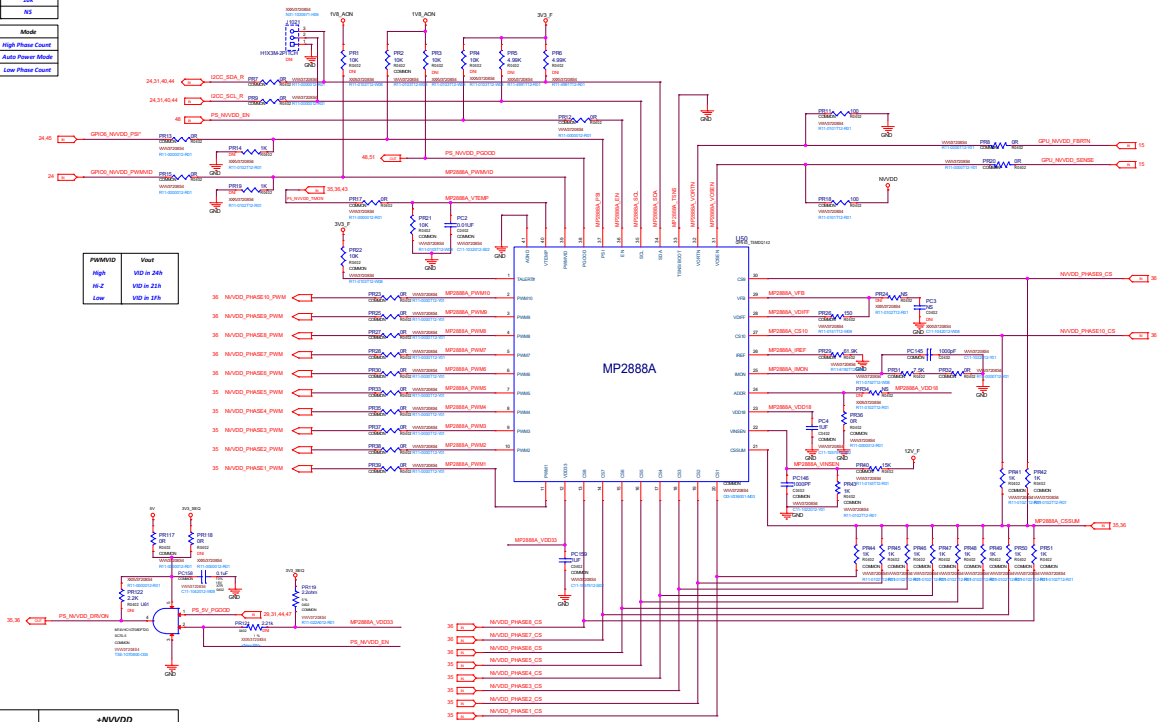
Created: 2018-08-01

By: [Redacted]

Check: [Redacted]

Scale: 1:1

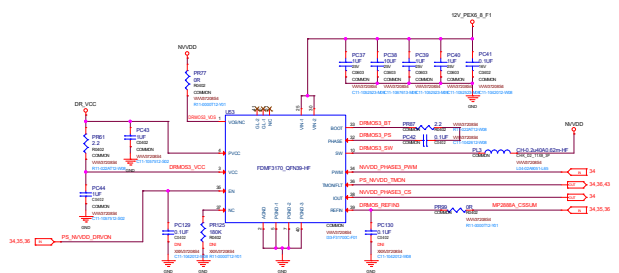
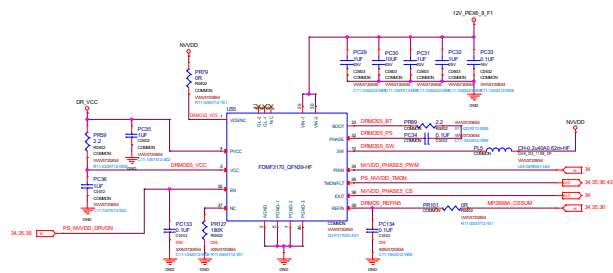
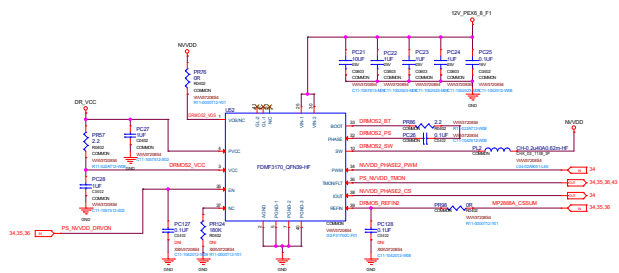
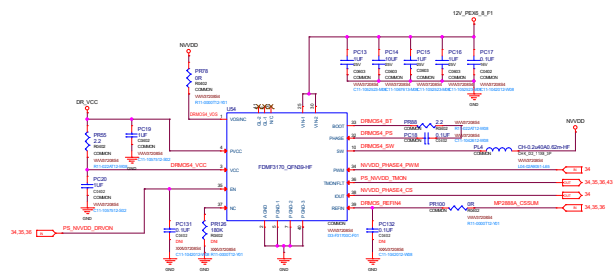
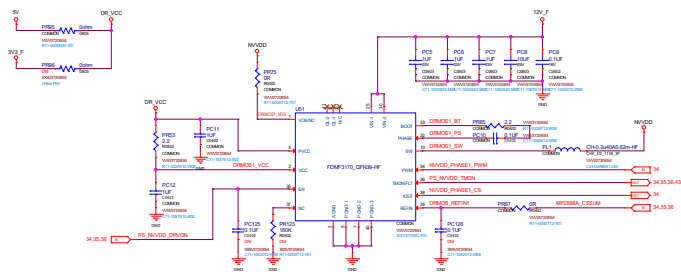


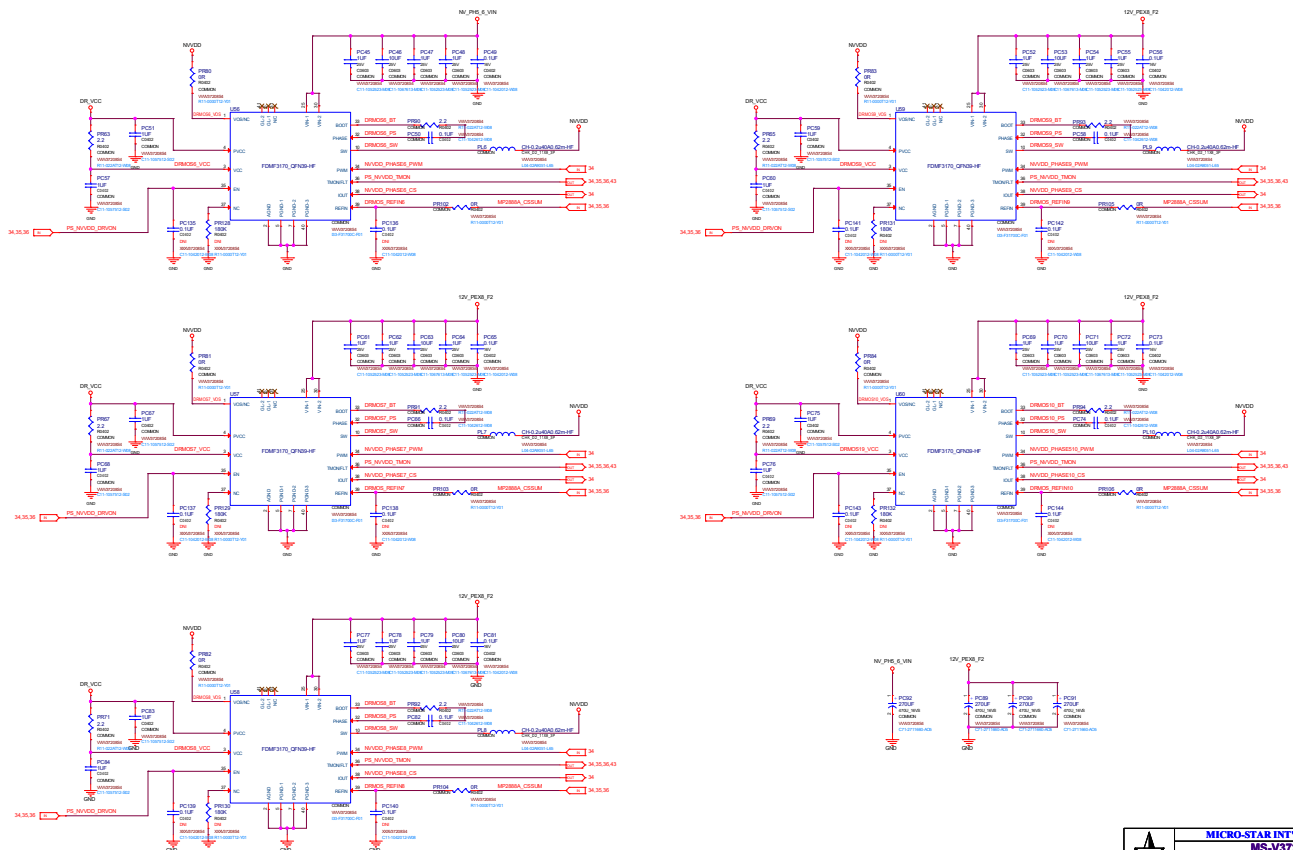


	+NVVDD
TDC	200A
IccMax	330A
Vboot	0.8V
Load Line	0mohm

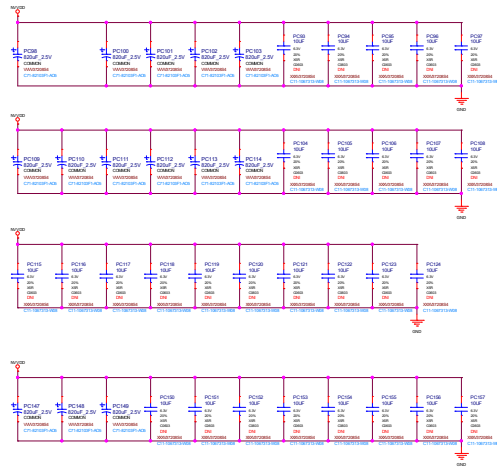
FWBss Address	Setting Point(V)	R _{avg} (Ω) 1%	R _{avg} (Ω) 1%
20th	0	-	0
21th	0.031	3.32	0.050
22th	0.057	3.32	0.11
23th	0.084	3.32	0.17
24th	0.116	3.32	0.226
25th	0.156	3.32	0.316
26th	0.205	3.32	0.43
27th	0.266	3.32	0.576
28th	0.340	3.32	0.768
29th	0.430	3.32	1.03
24th	0.540	3.32	1.43
26th	0.675	3.32	2
20th	0.848	3.32	2.84
21th	1.044	3.32	4.64
22th	1.301	3.32	8.66
23th	1.600	3.32	16.5







NVVDD Output CAP



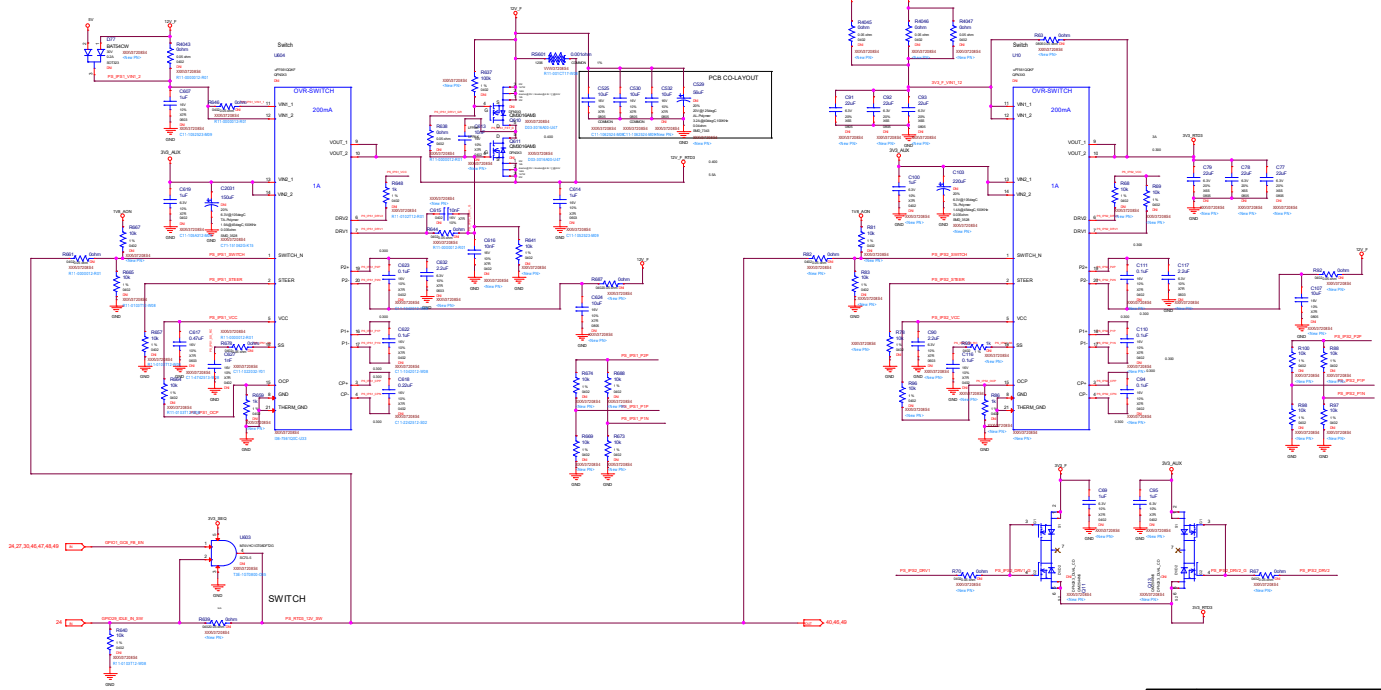
	MICRO-STAR INT'L CO., LTD	
	MS-V372	
	Rev:	Revised: November 2018
	Drawn:	PS:NVVDD (X)
	Date:	Wednesday August 29, 2018
		Sheet 38 of 50

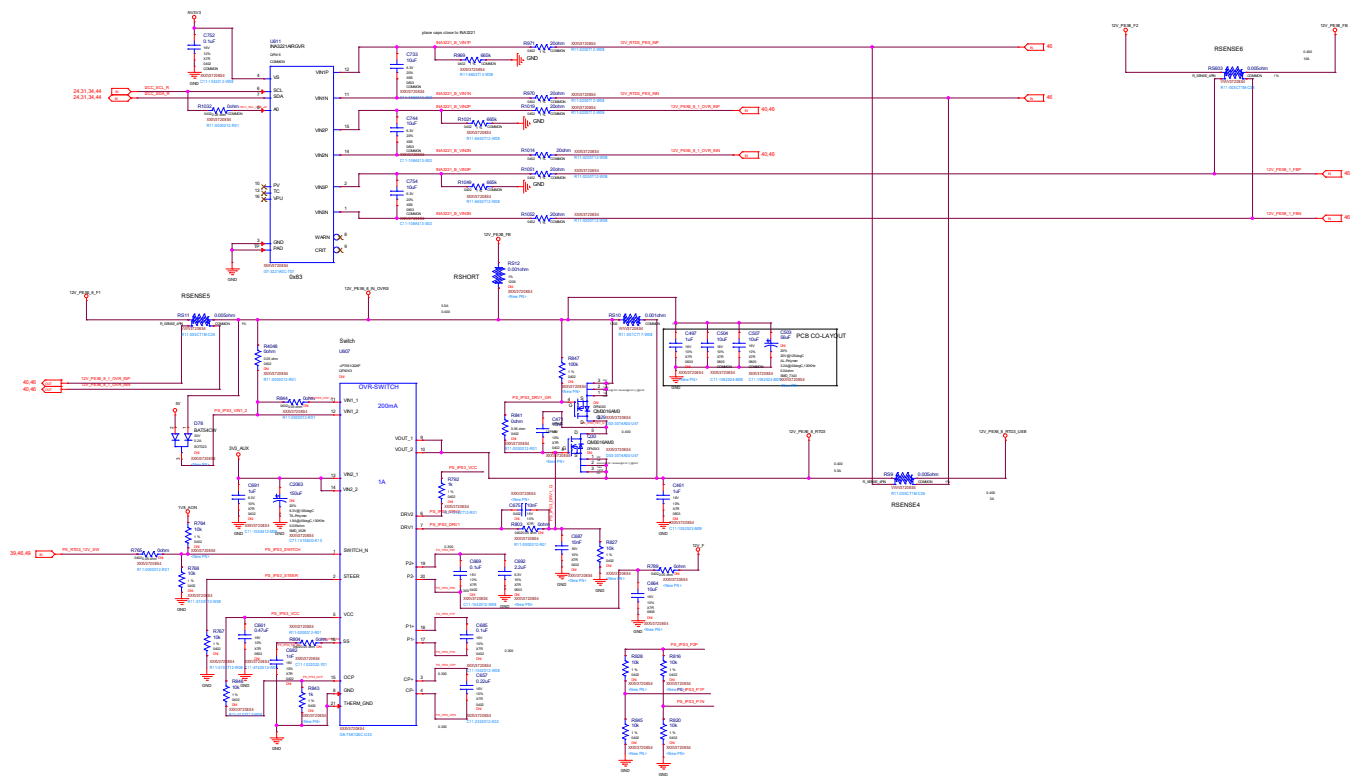
AND GATE LOGIC FOR P-BOARD

GPI01	GPI029	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

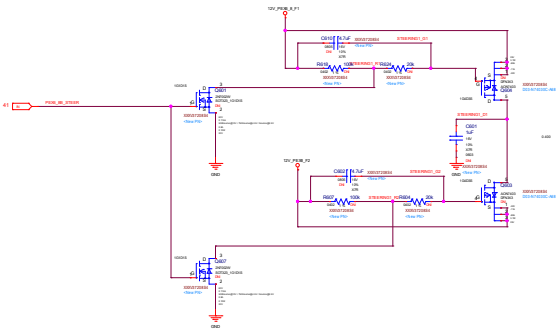
AND GATE LOGIC FOR P-BOARD

GPI01	GPI029	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

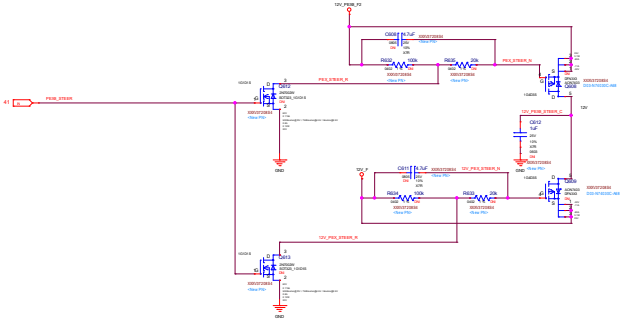


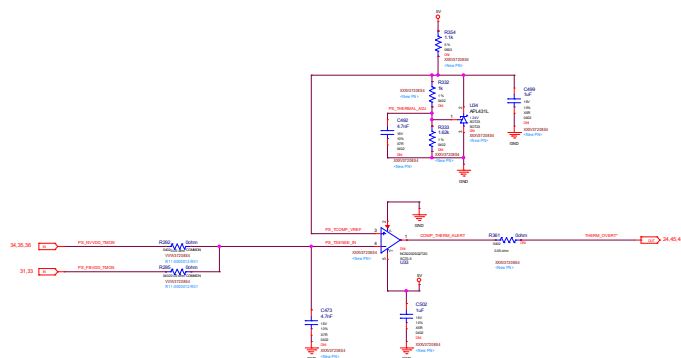


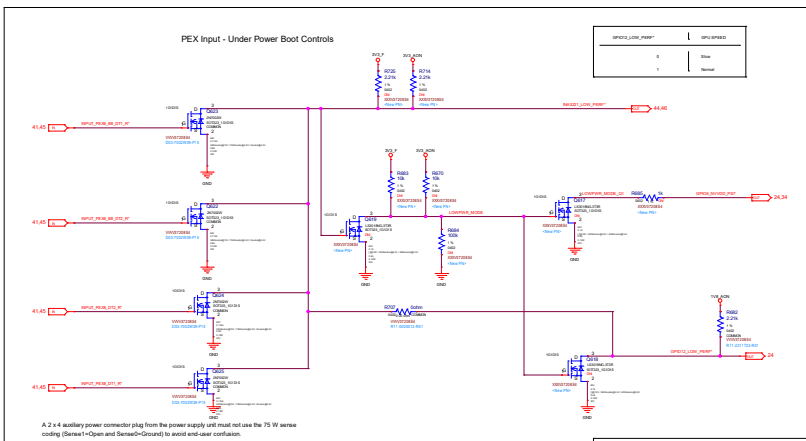
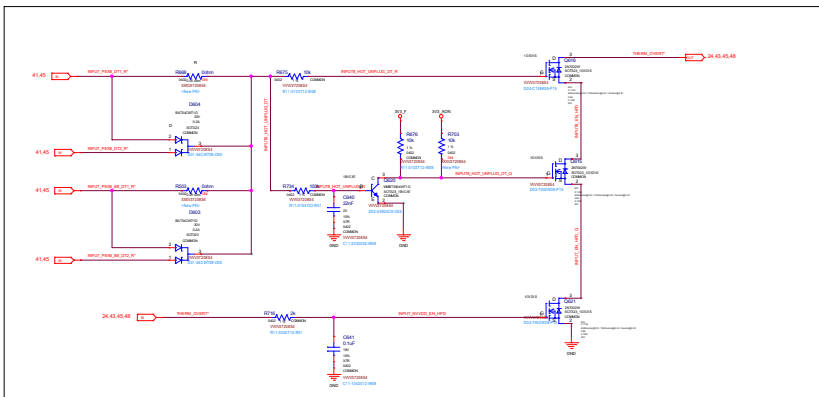
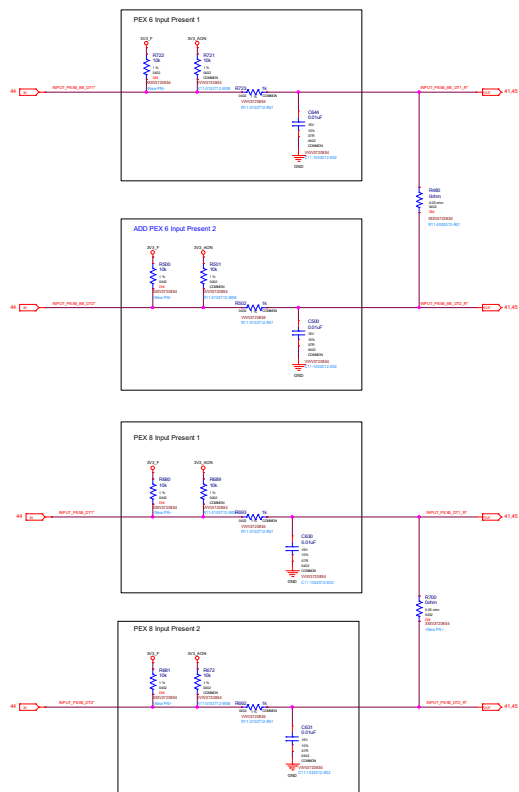
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



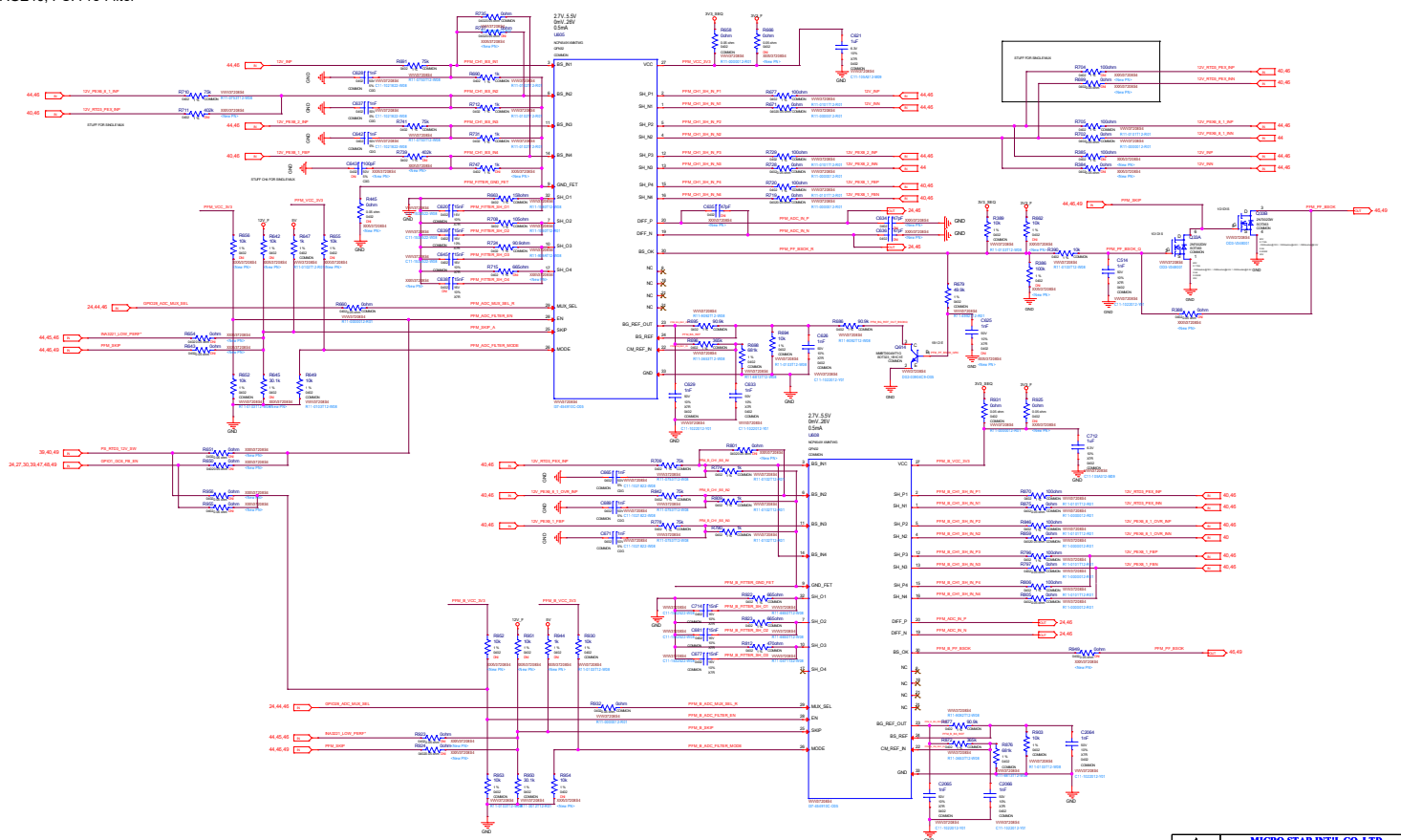
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

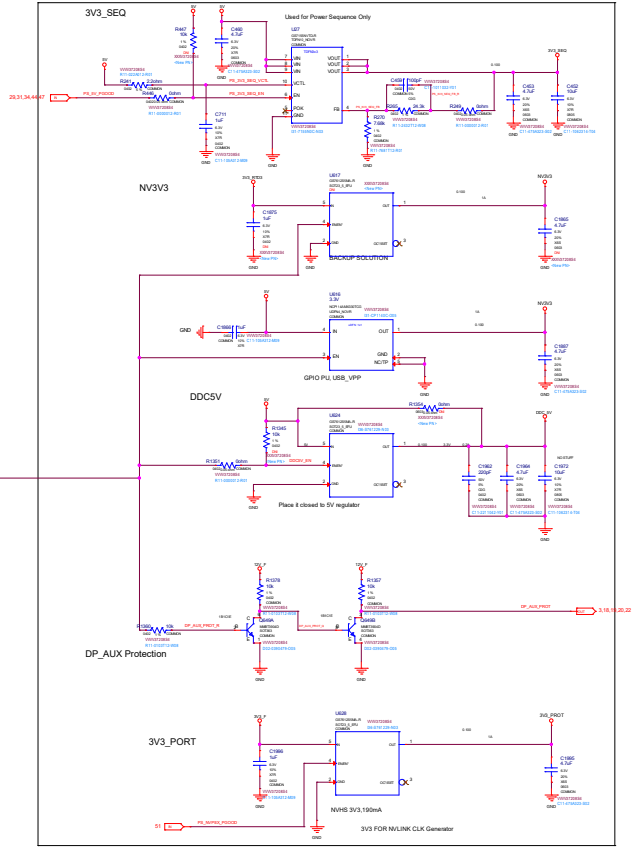
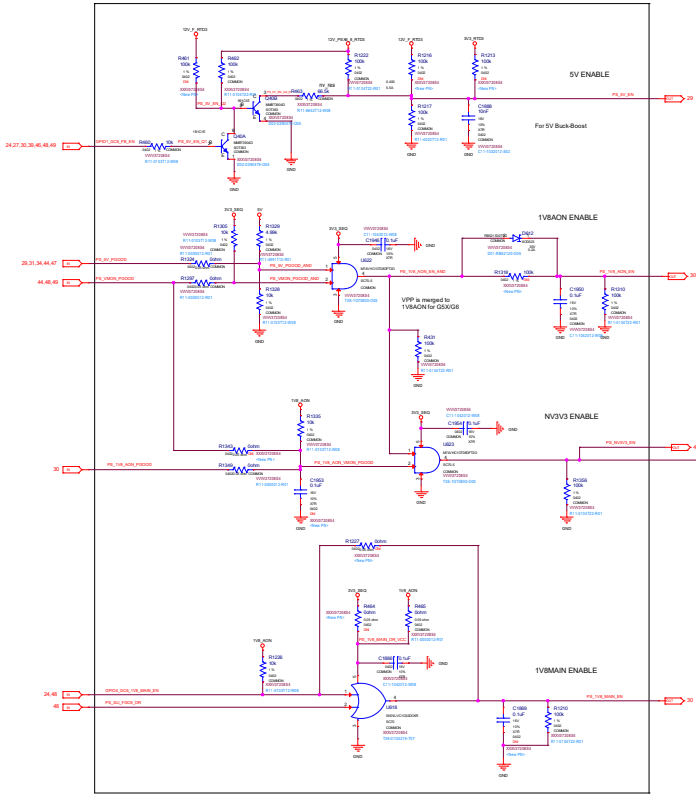


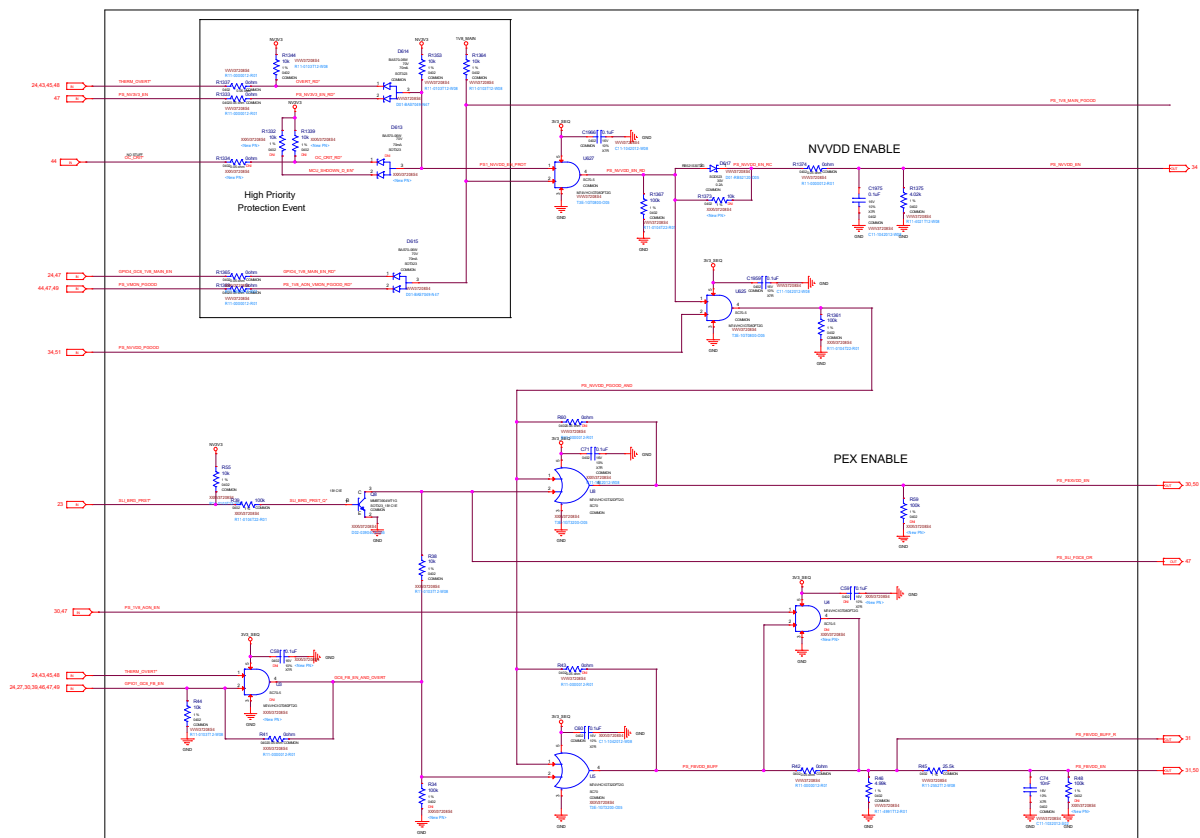




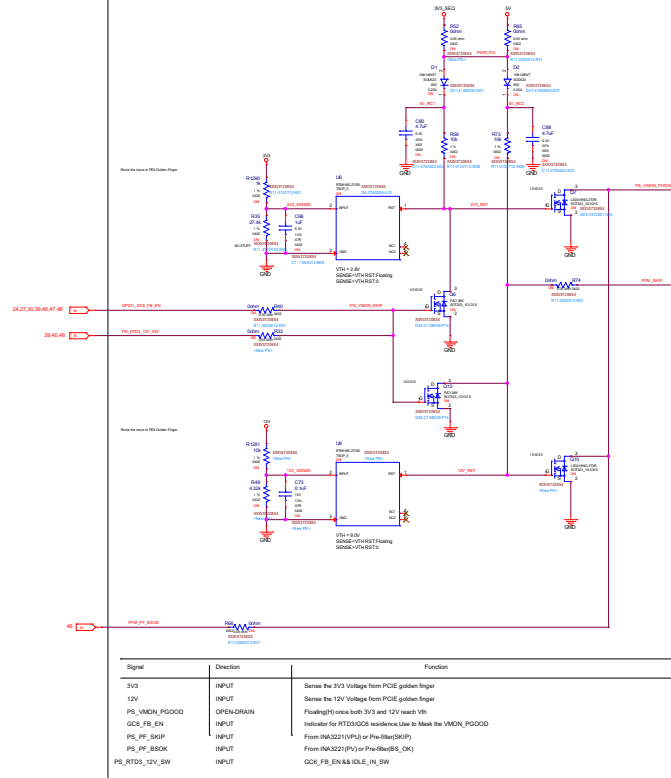
A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W series coding (Sense1+Open and Sense2+Ground) to avoid end-user confusion.







PCIE Voltage Monitor

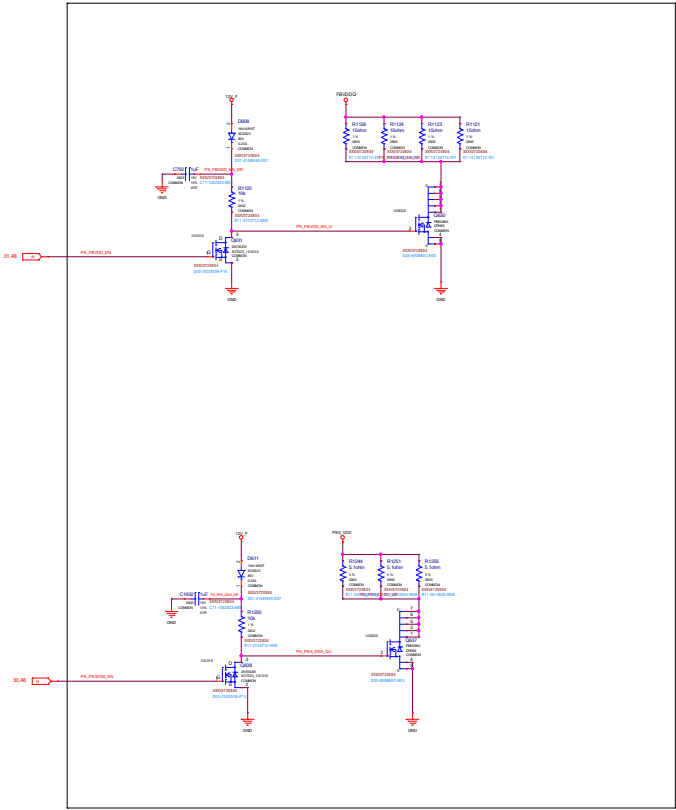


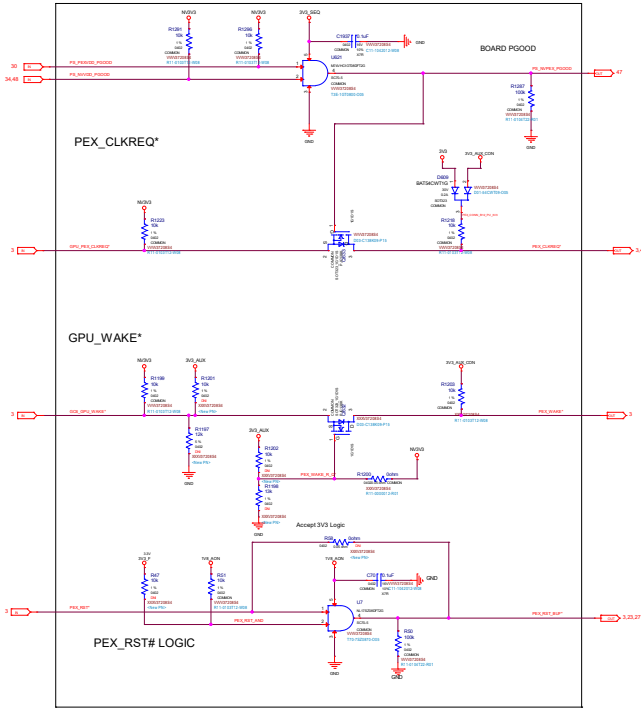
BOM Configuration

OPTIONS	PEX12V_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q105 NO STUFF D15	Pre-Filter NO STUFF U12 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

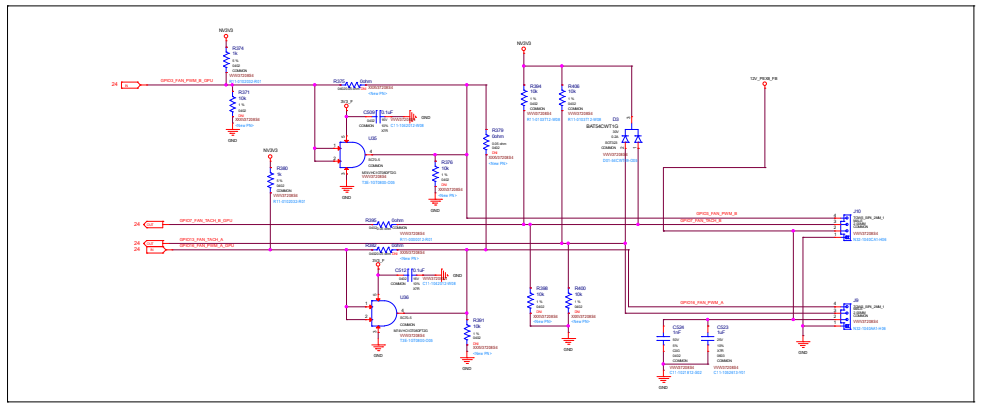
Power Supply
INA3221:3V3_SEQ
Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:
Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs



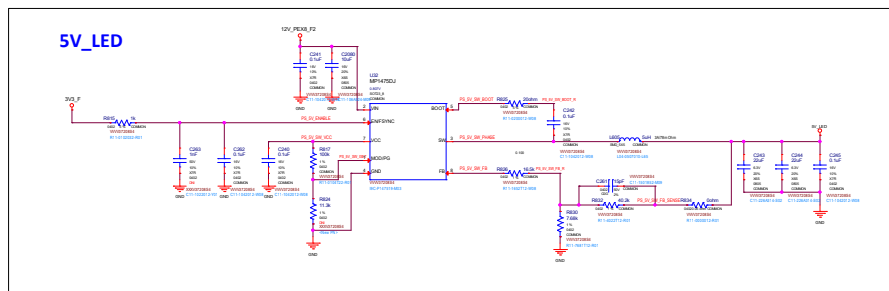
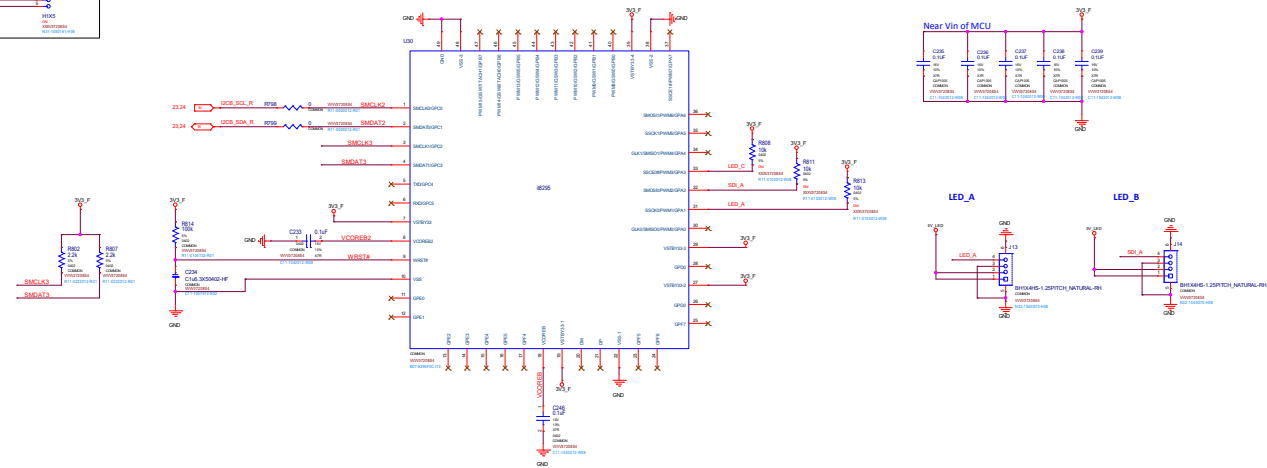
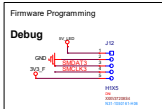


Remove LED

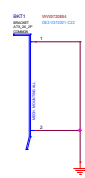


Remove LED BOOST

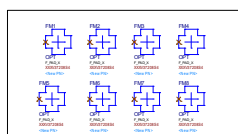
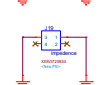
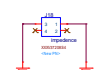




Brackets:



Screw



Mechanical Holes Symbol

