

PG180-A02

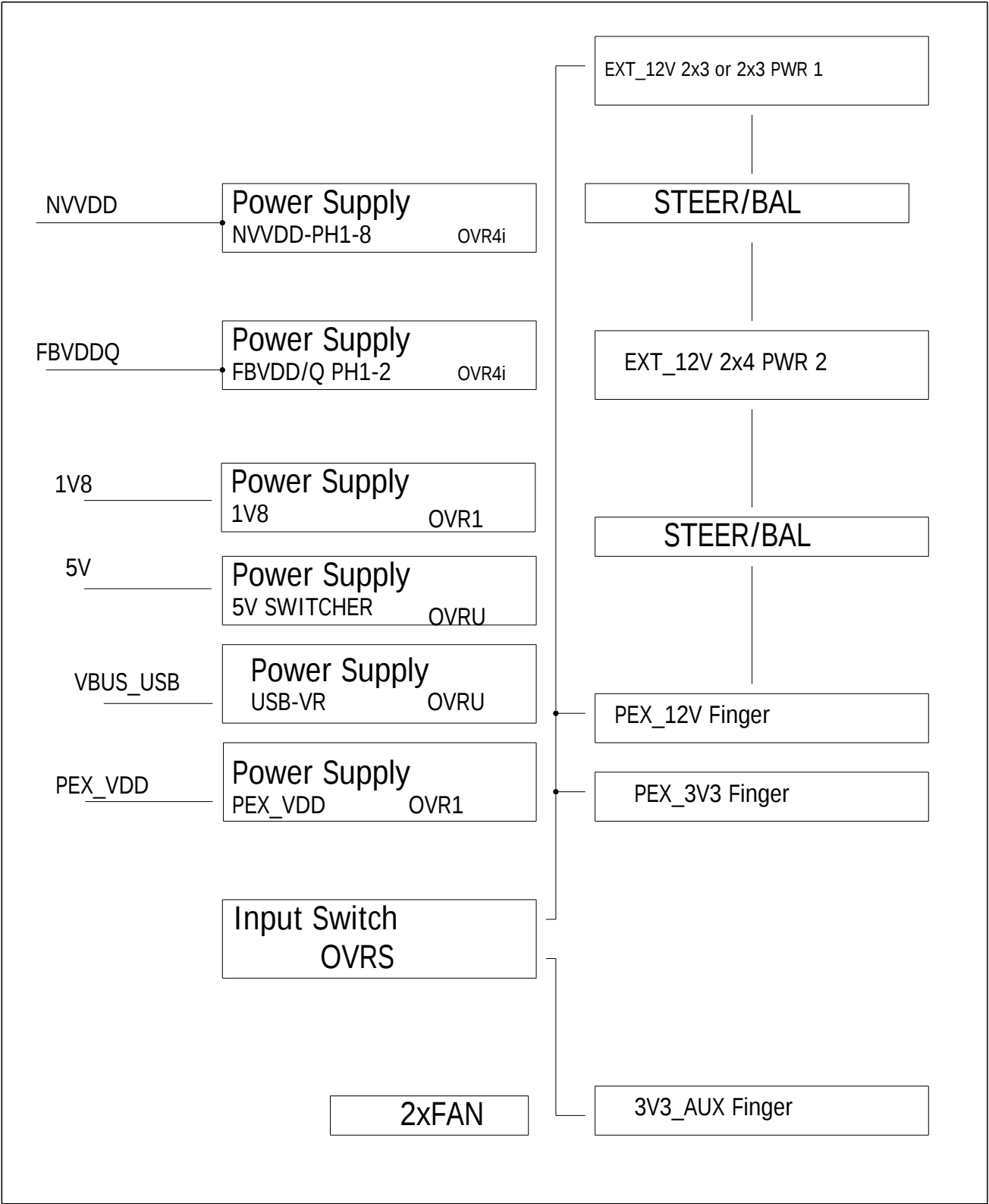
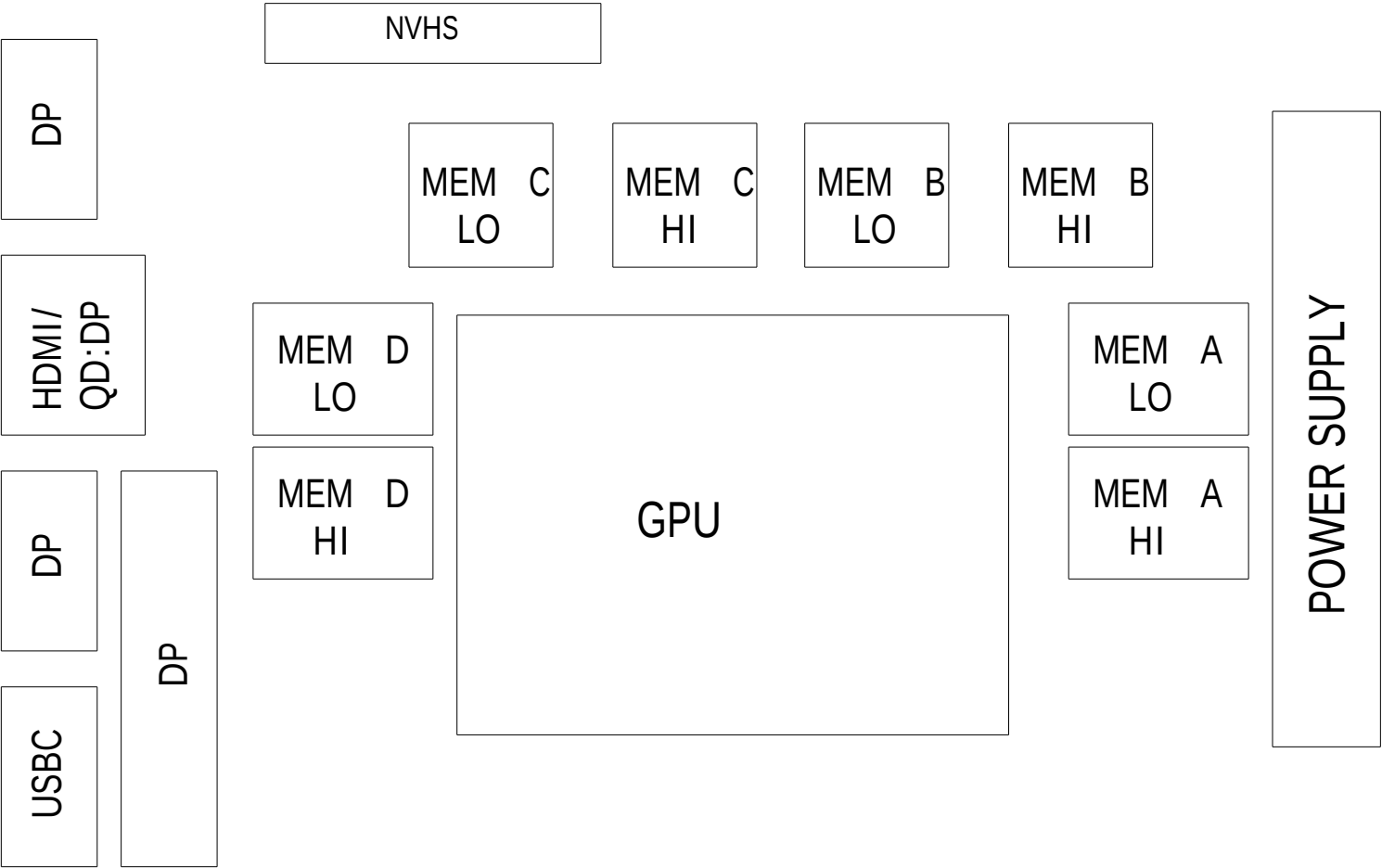
256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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Page2: Block Diagram

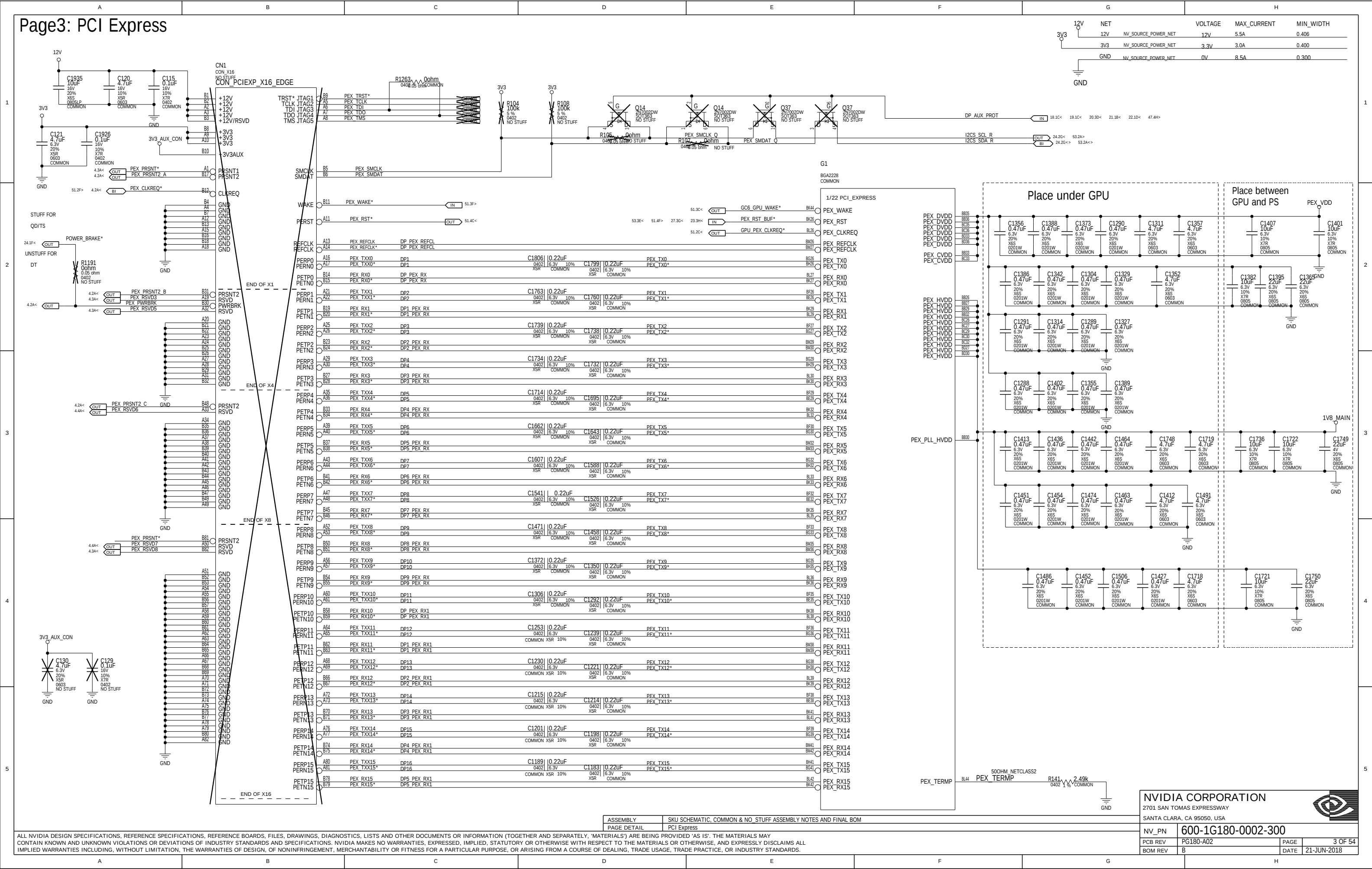


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ASSEMBLY	SKU SCHEMATIC, COMMON & NO. STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	Block Diagram

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Page3: PCI Express



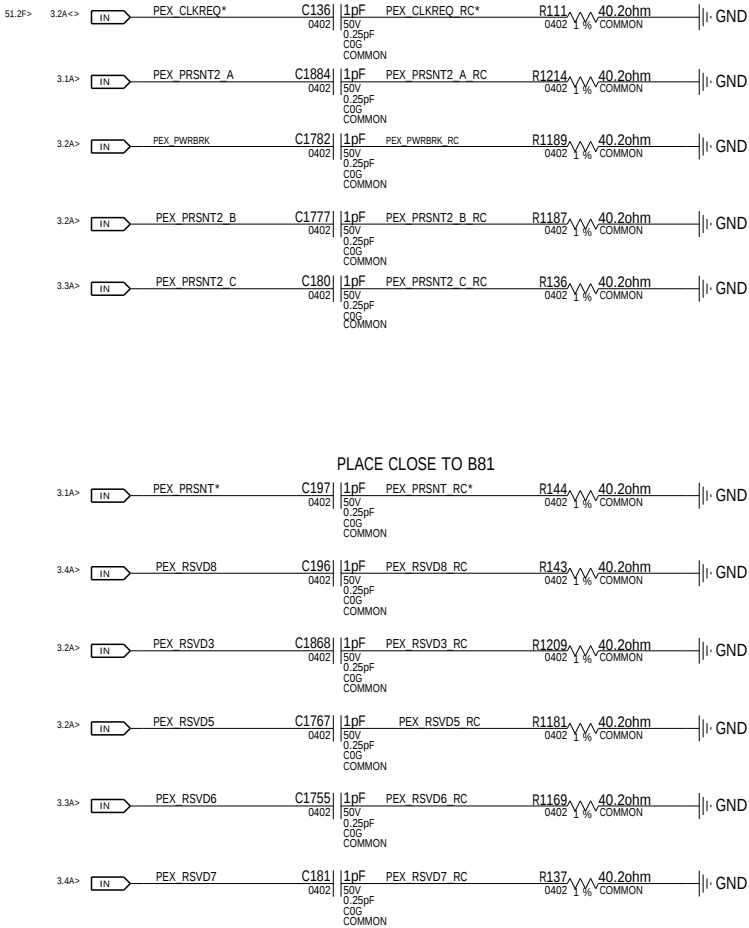
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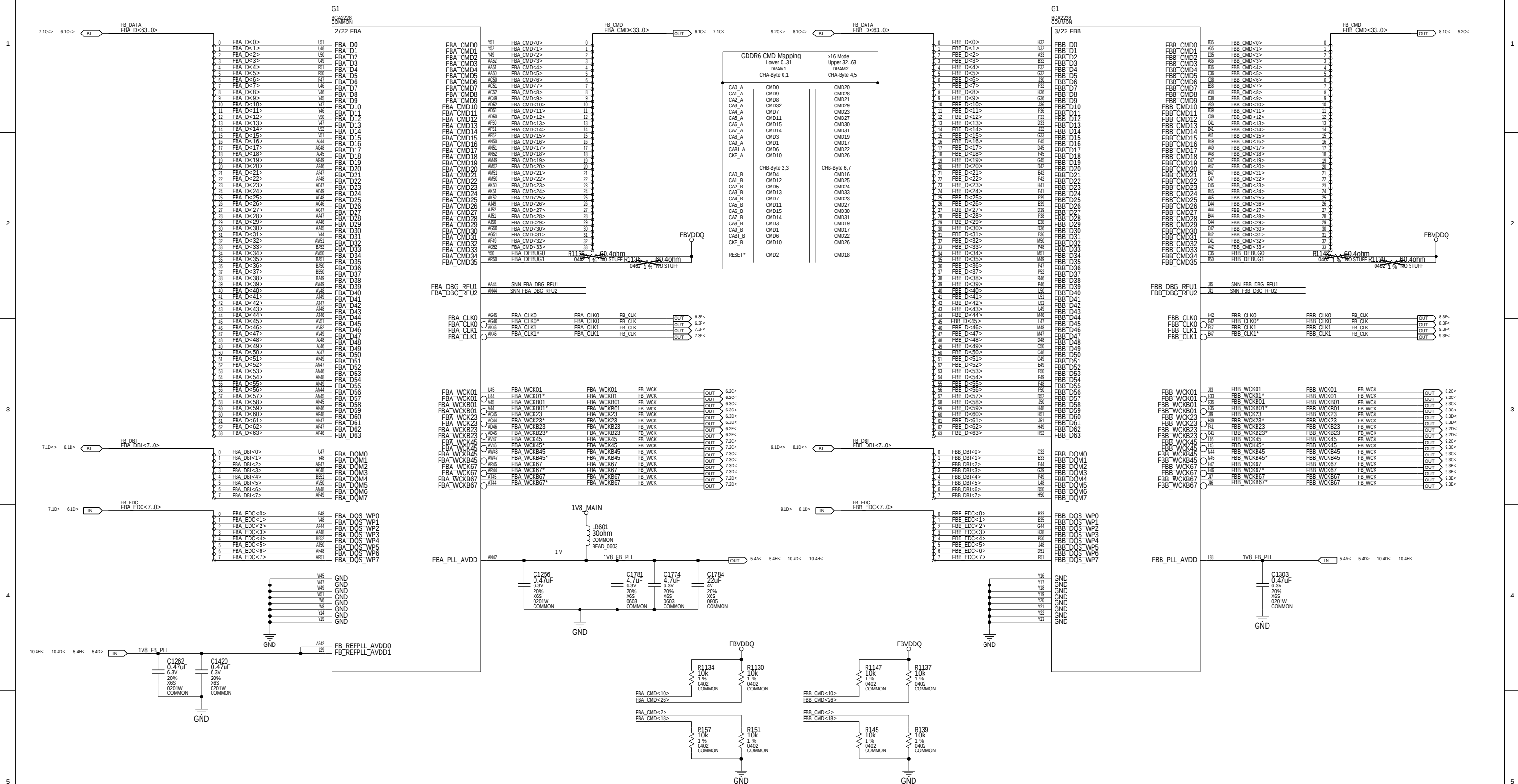


Page4: PCI Termination



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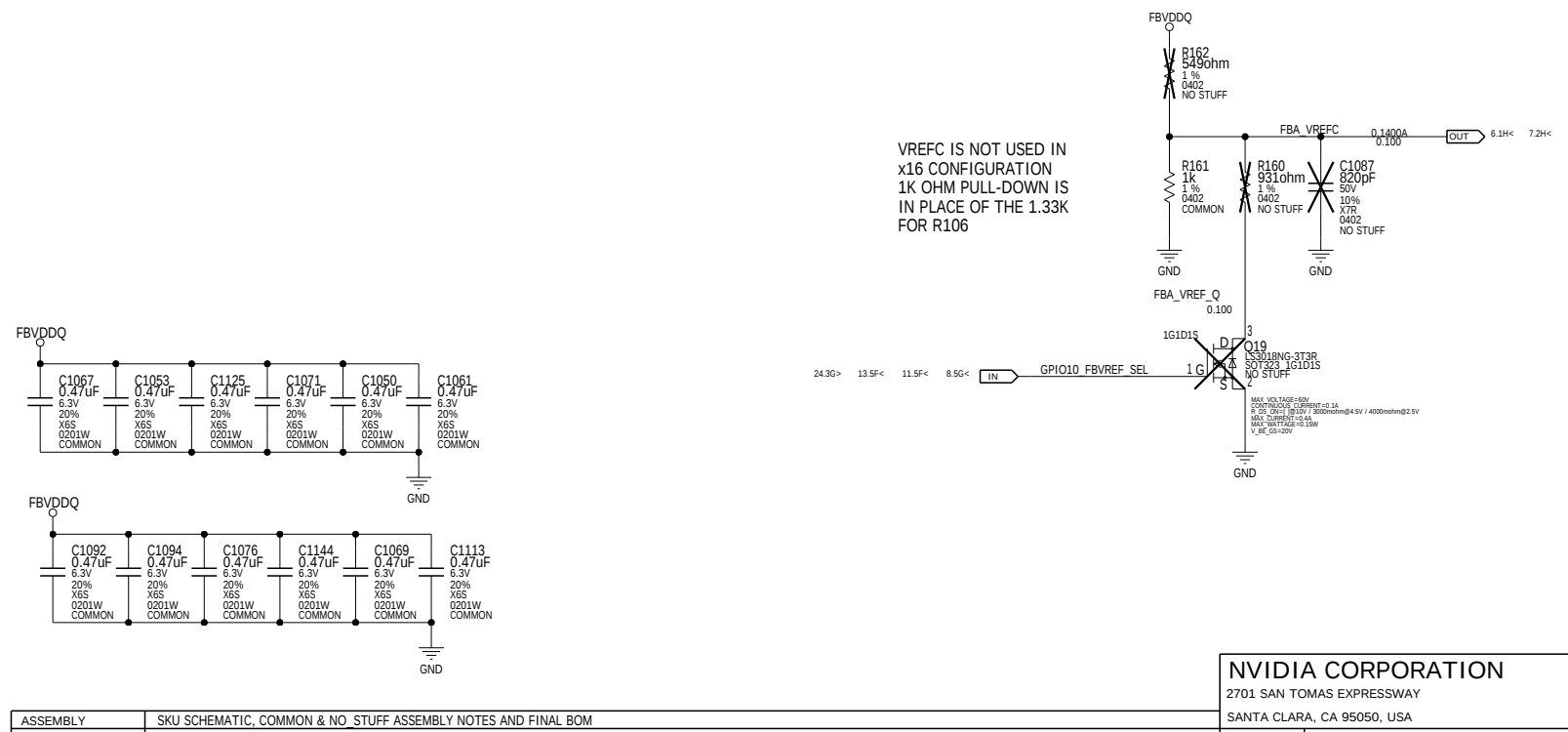
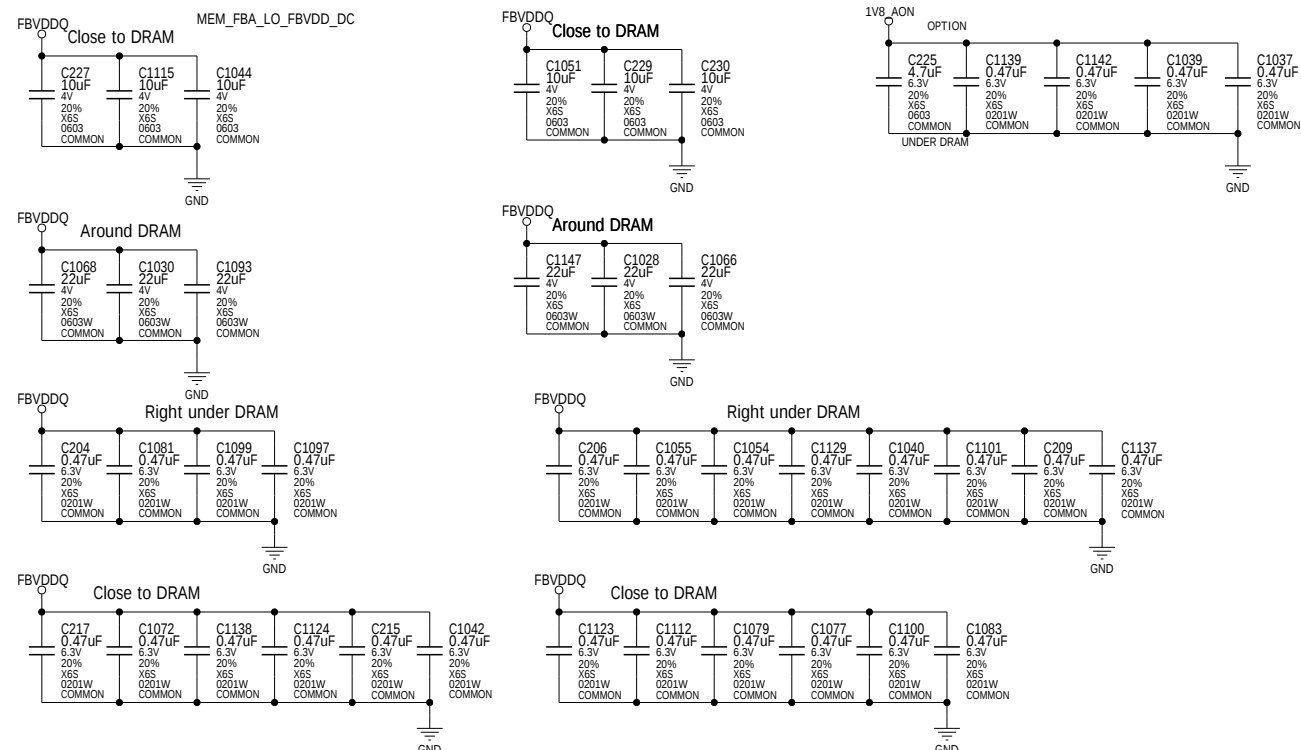
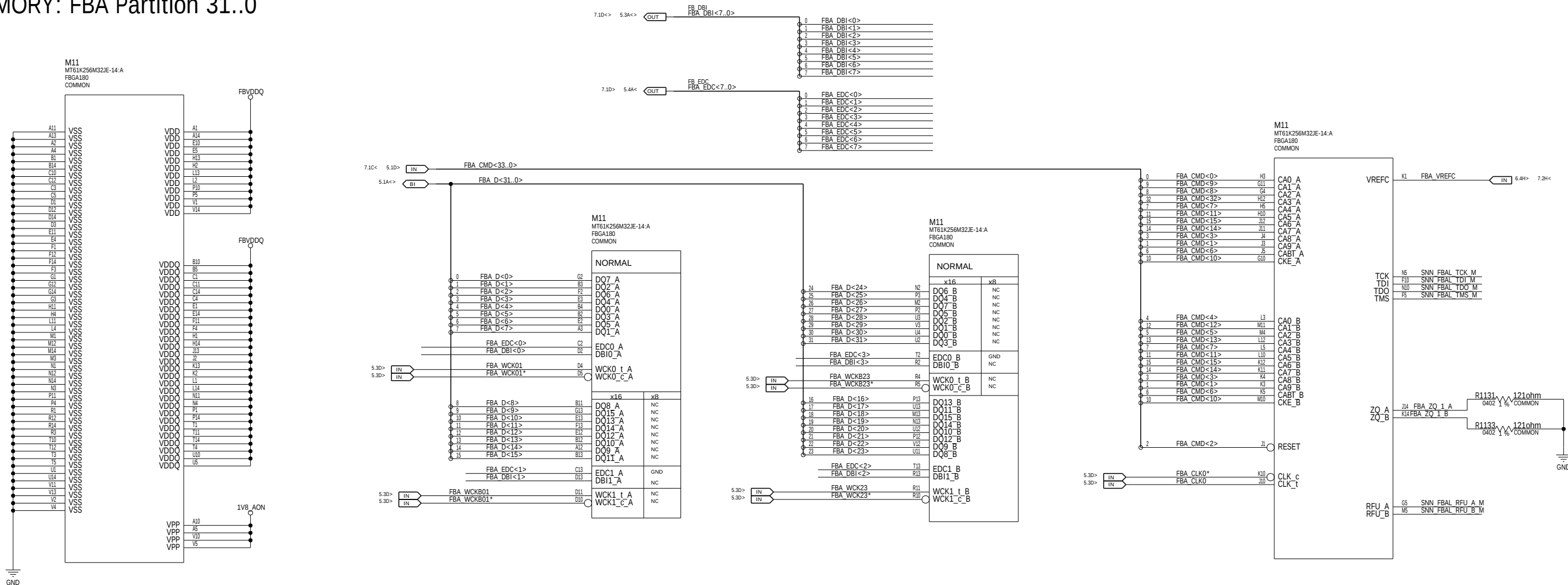
Page5: MEMORY: GPU Partition A/B



Page6: MEMORY: FBA Partition 31..0

5

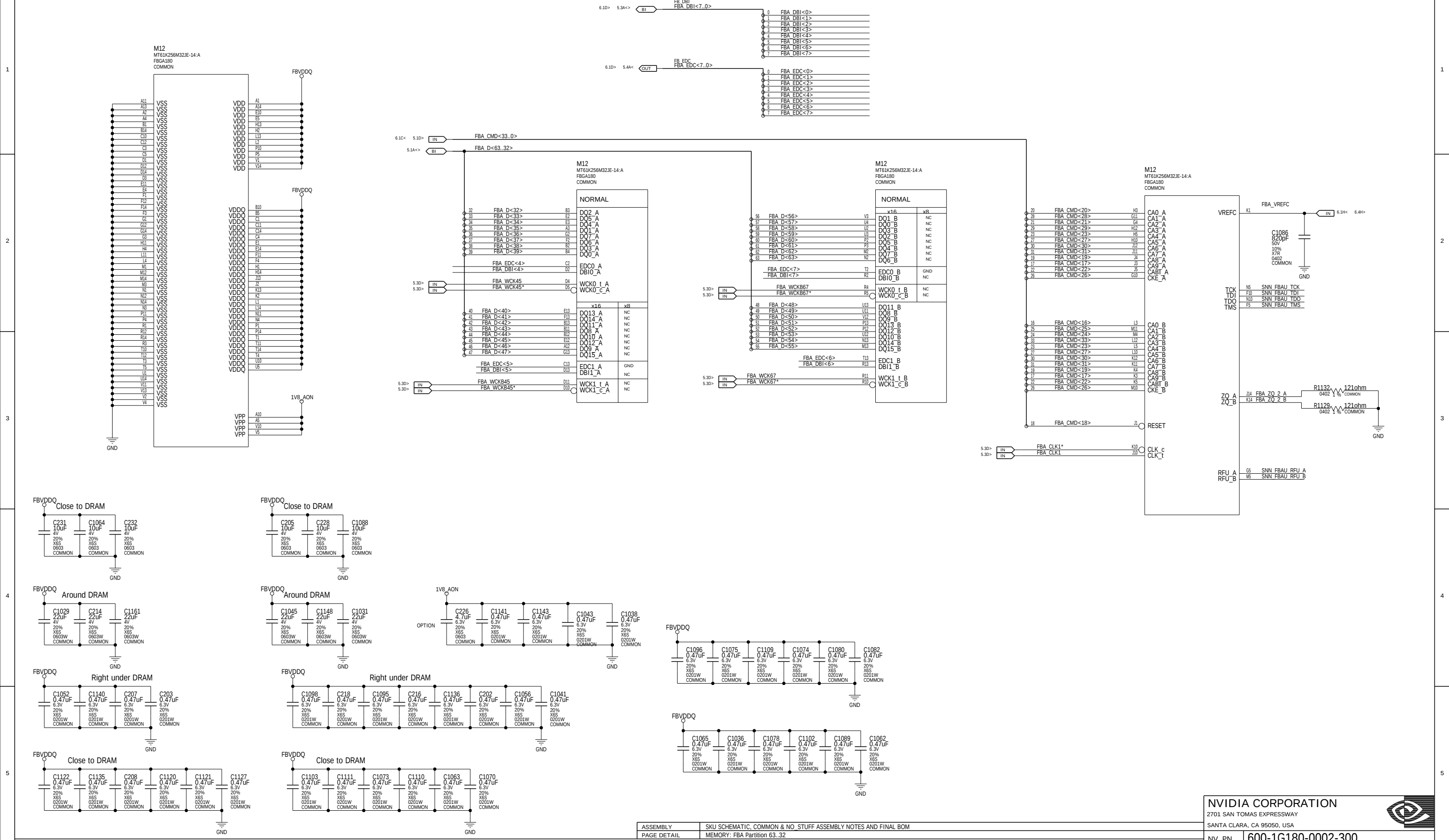
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ASSEMBLY		SKU SCHEMATIC, COMMON & NO. STUFF ASSEMBLY NOTES AND FINAL BOM		SANTA CLARA, CA 95050, USA			
PAGE DETAIL		MEMORY: FBA Partition 31..0		NV_PN 600-1G180-0002-300			
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Page7: MEMORY: FBA Partition 63..32



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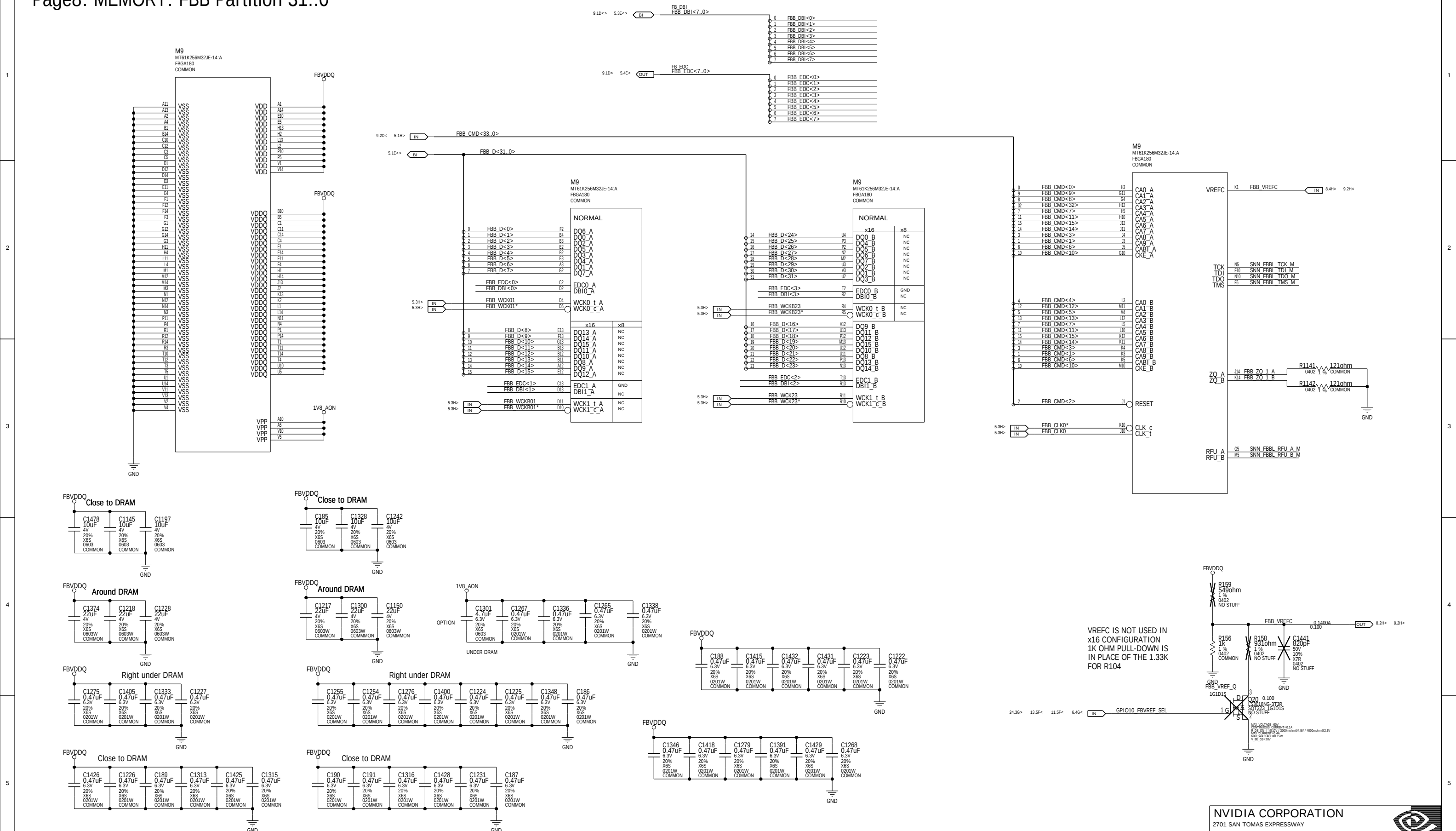
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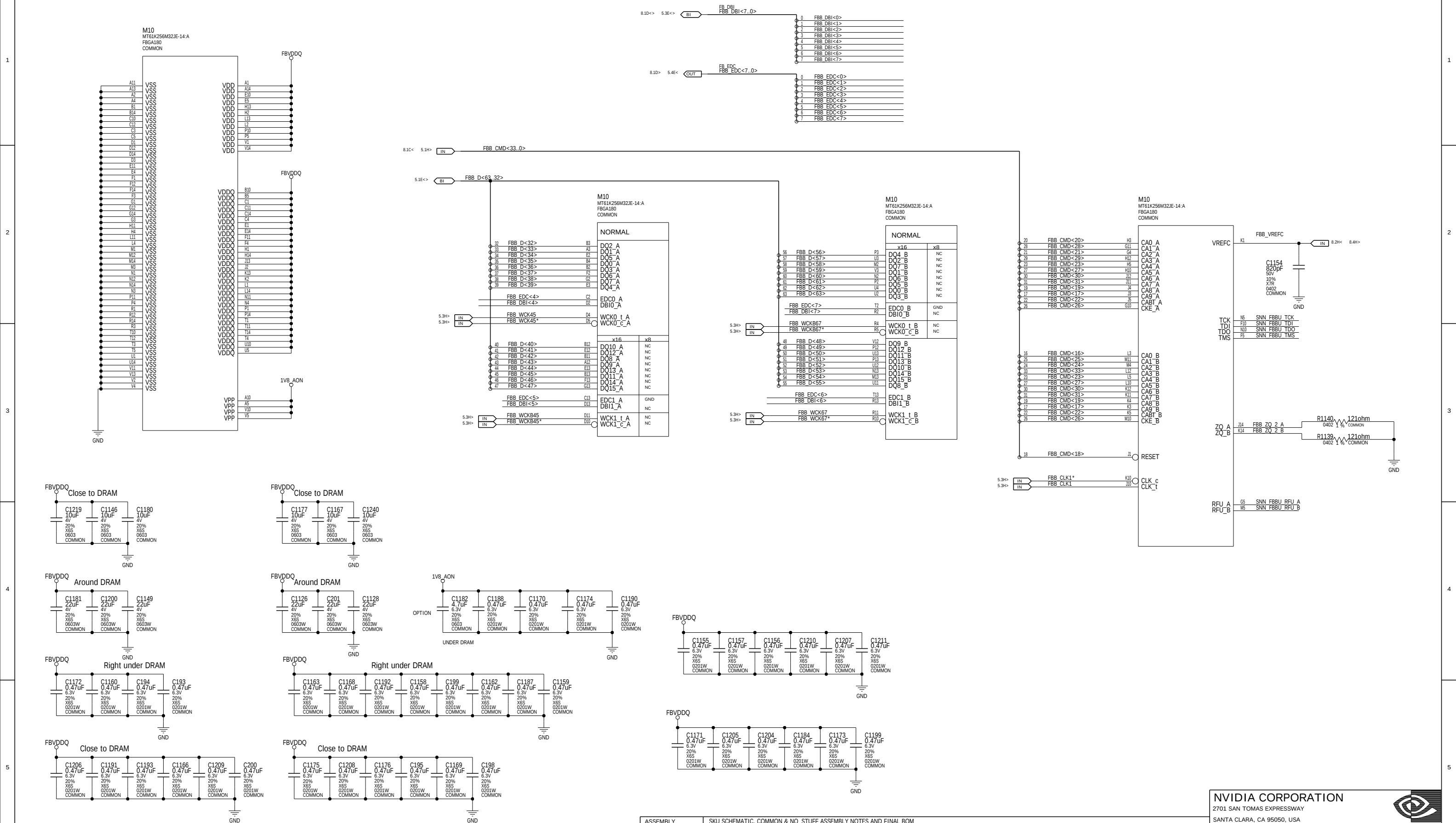
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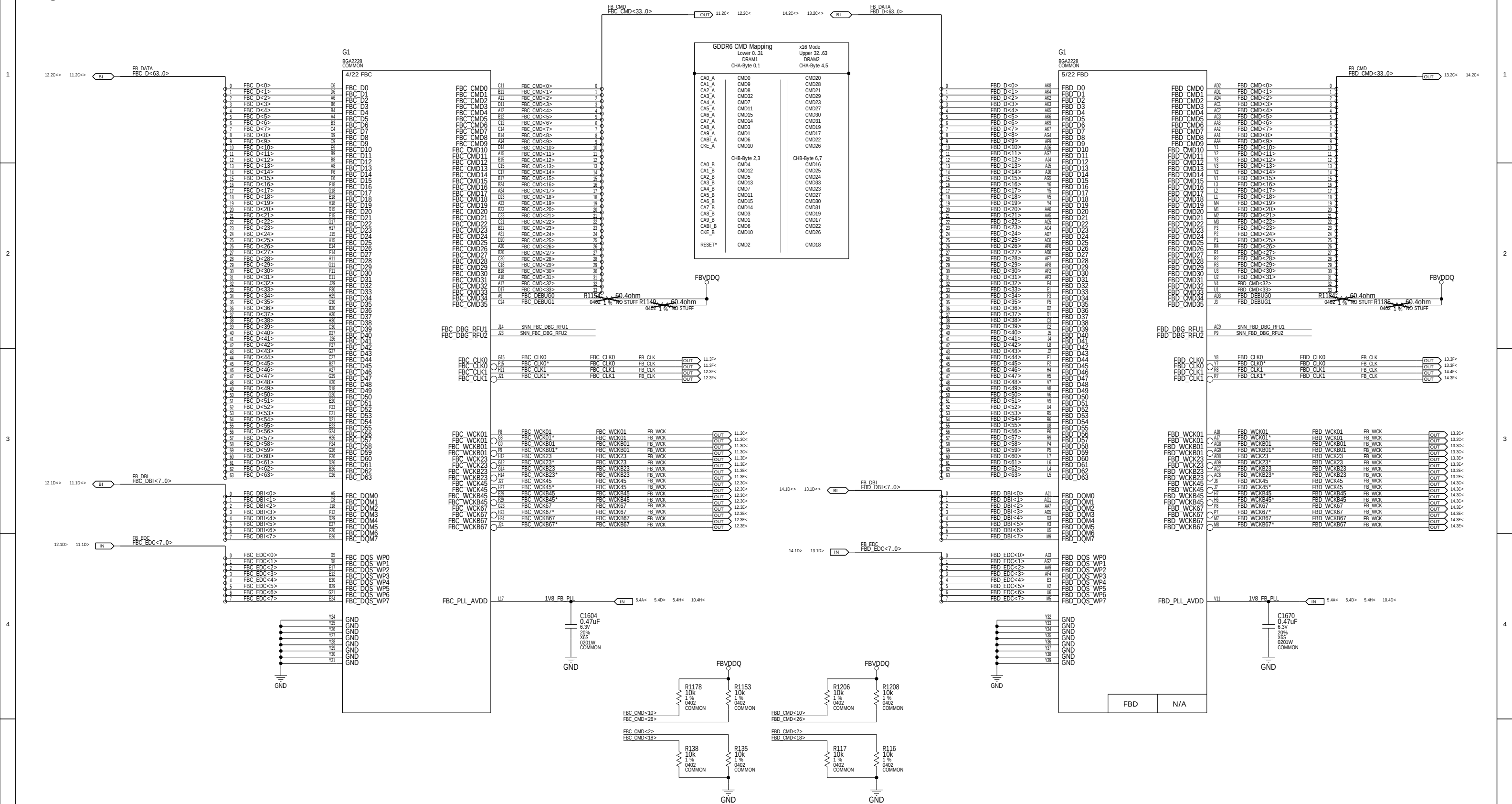
Page8: MEMORY: FBB Partition 31..0

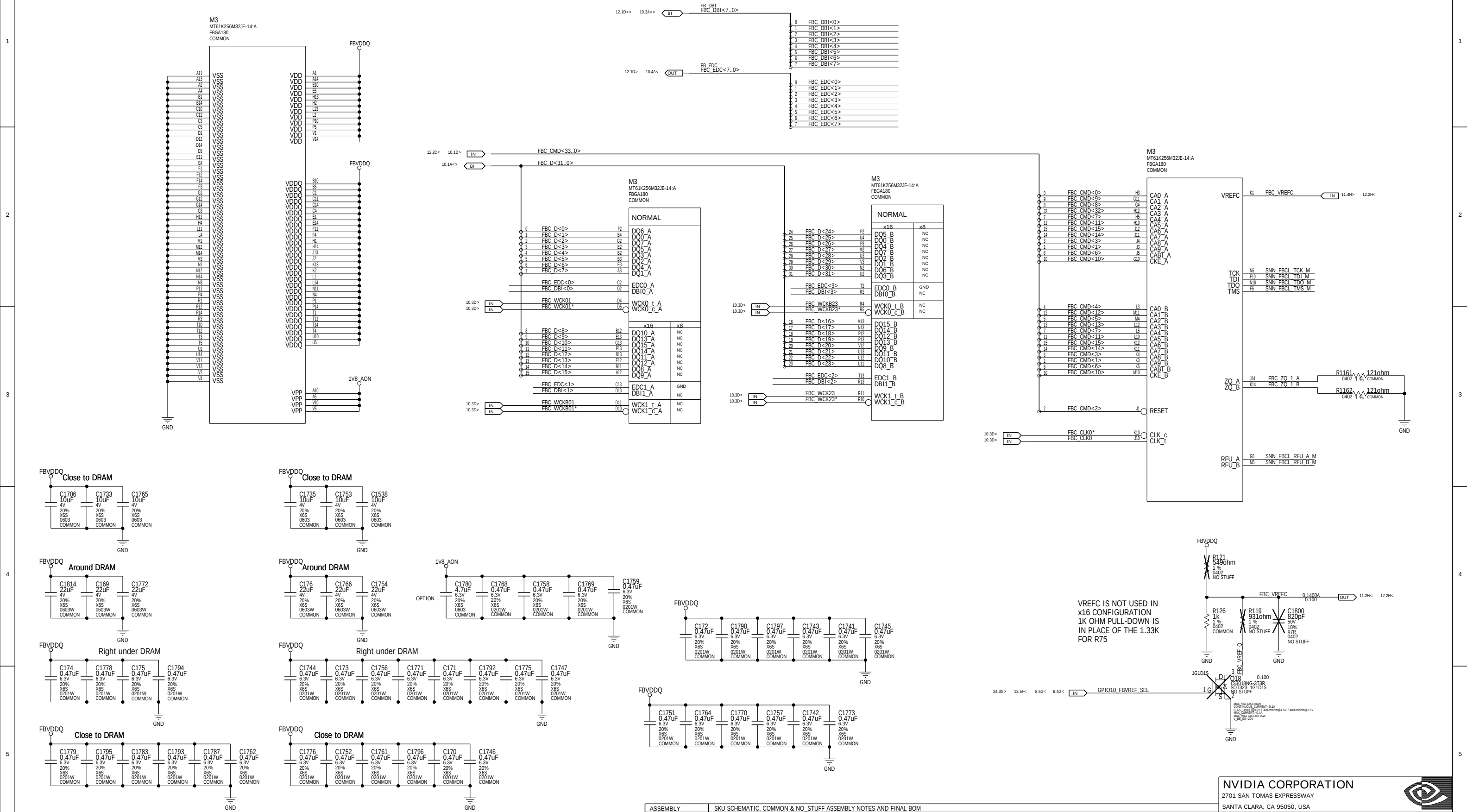


Page9: MEMORY: FBB Partition 63..32



Page10: MEMORY: GPU Partition C/D





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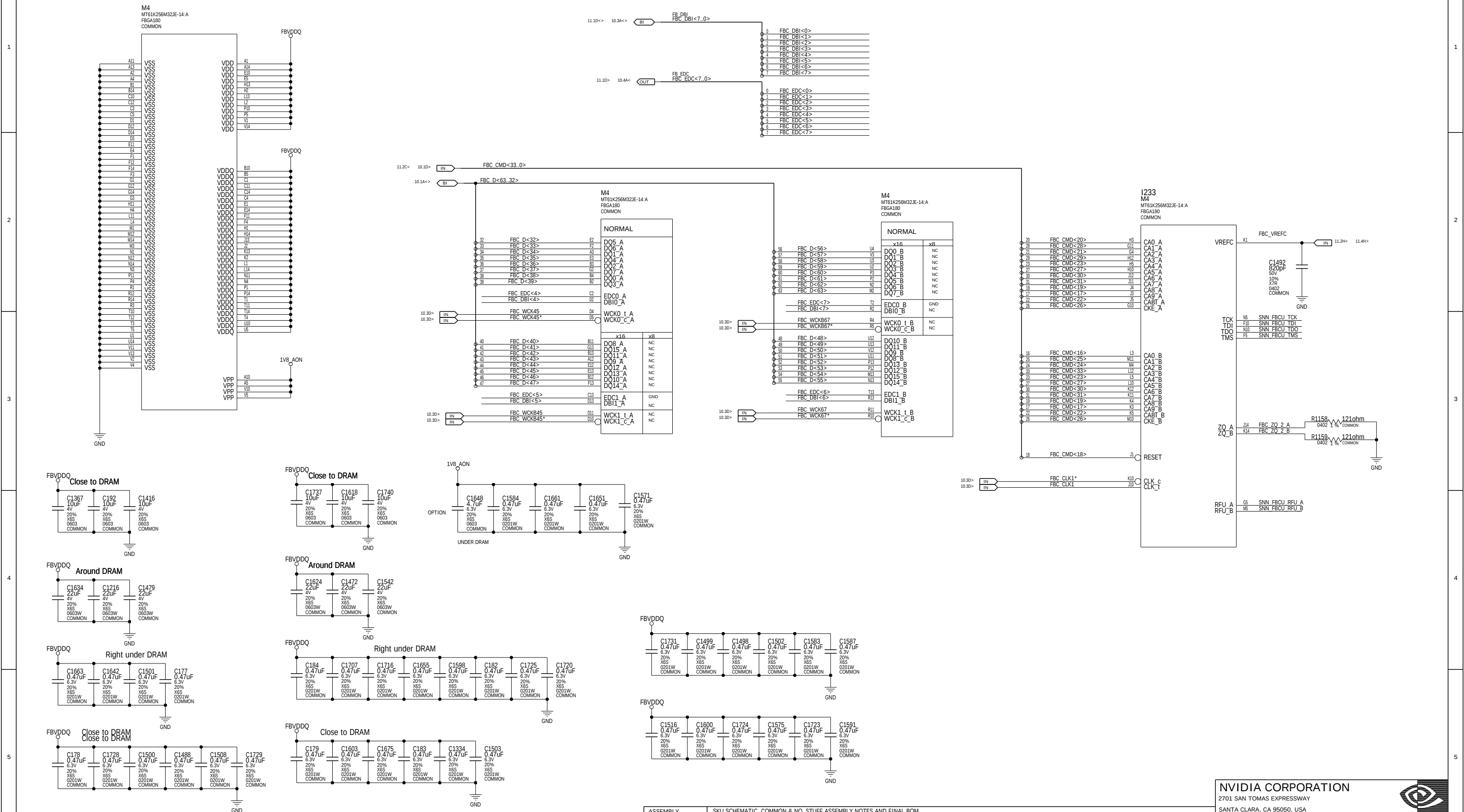
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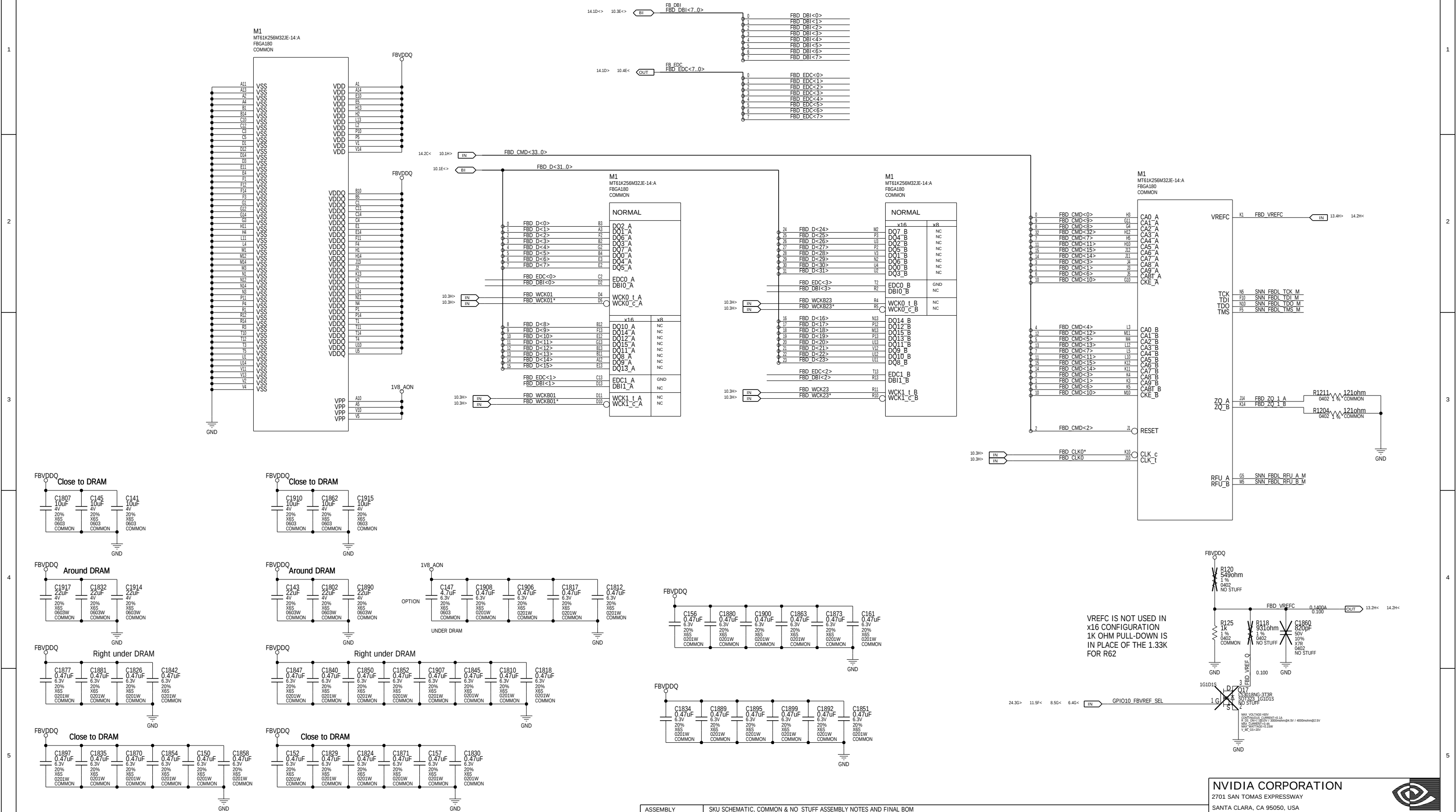
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Page12: MEMORY: FBC Partition 63..32



Page13: MEMORY: FBD Partition 31..0



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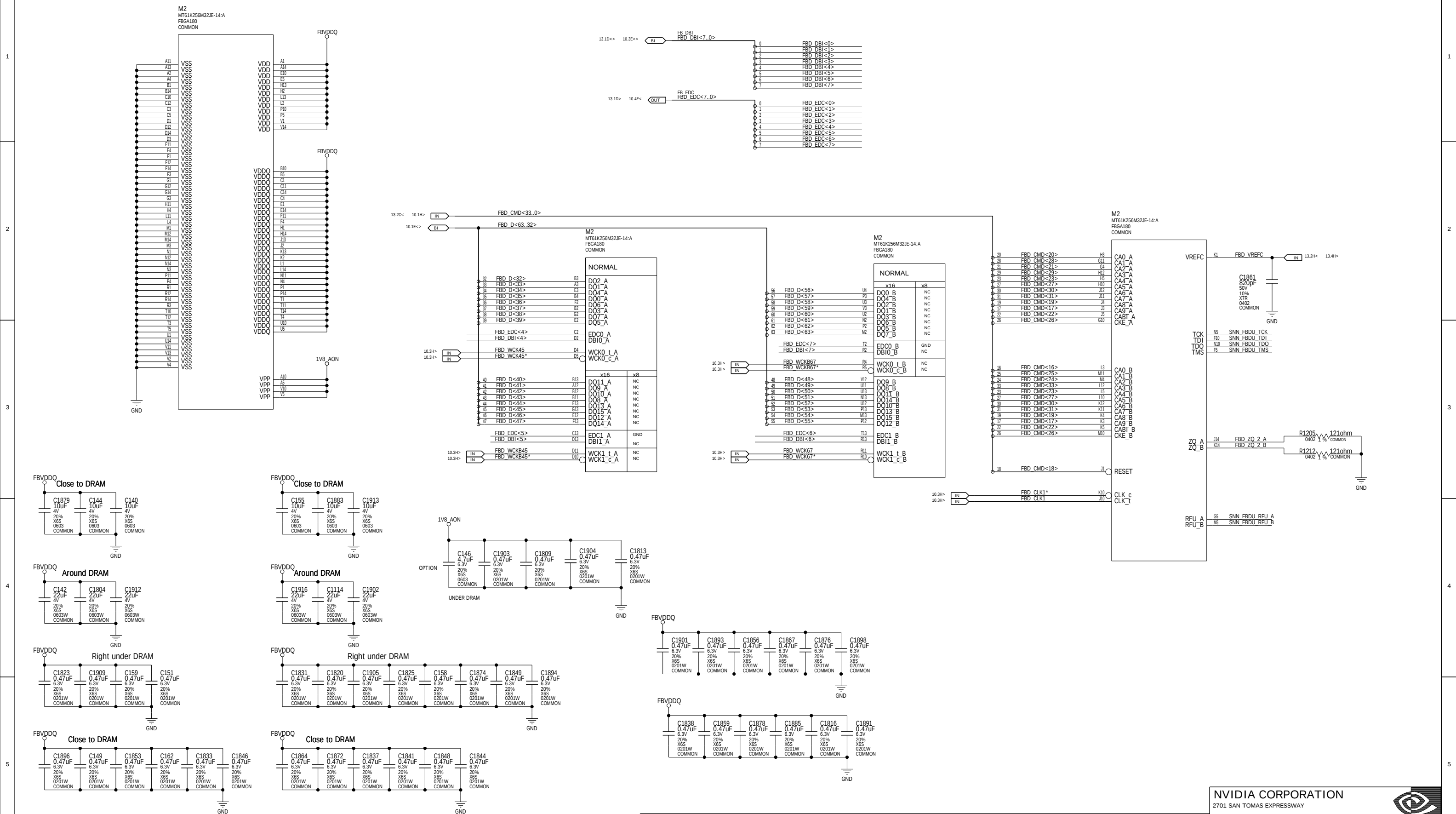
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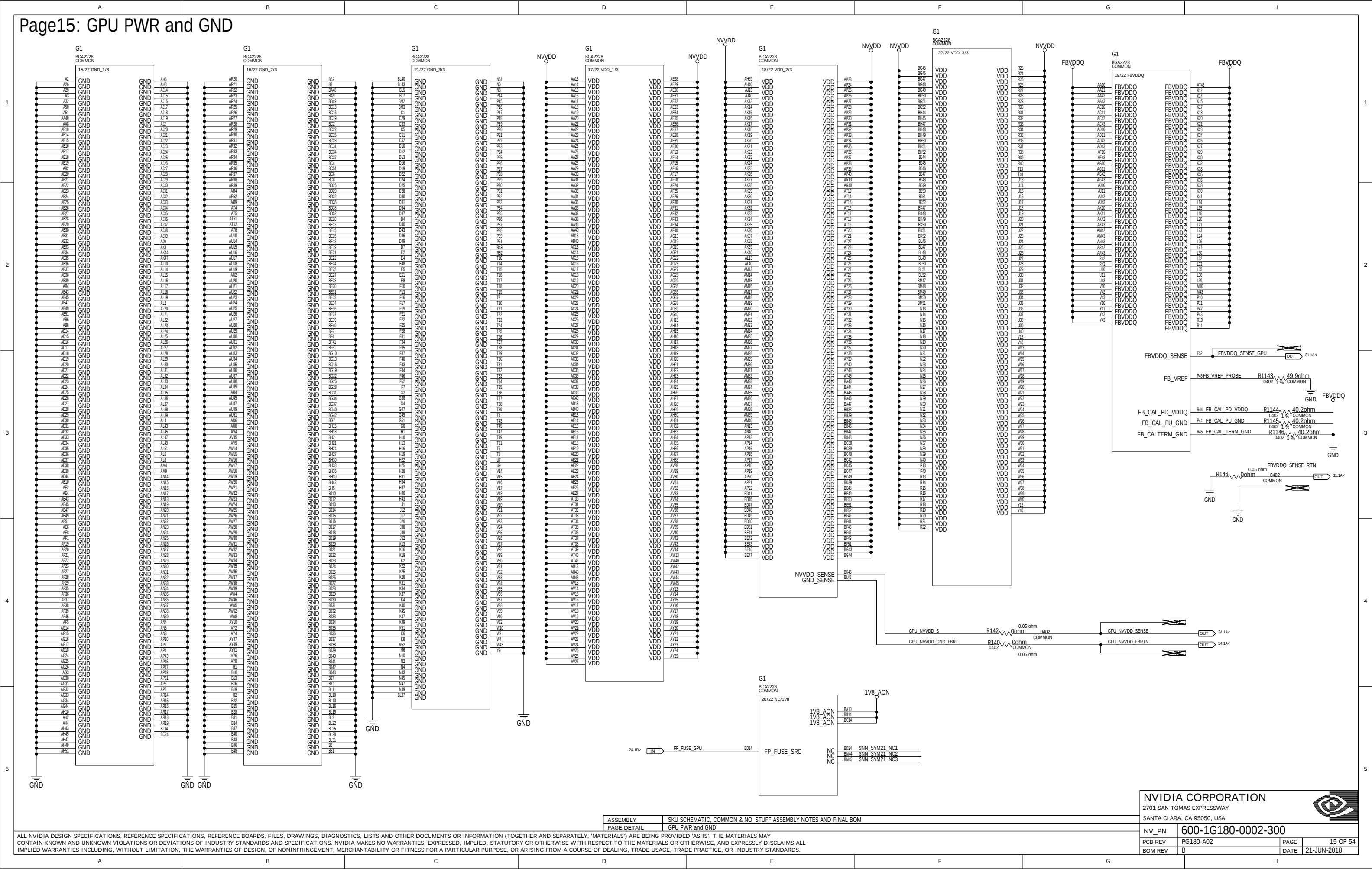
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Page14: MEMORY: FBD Partition 63..32



Page15: GPU PWR and GND

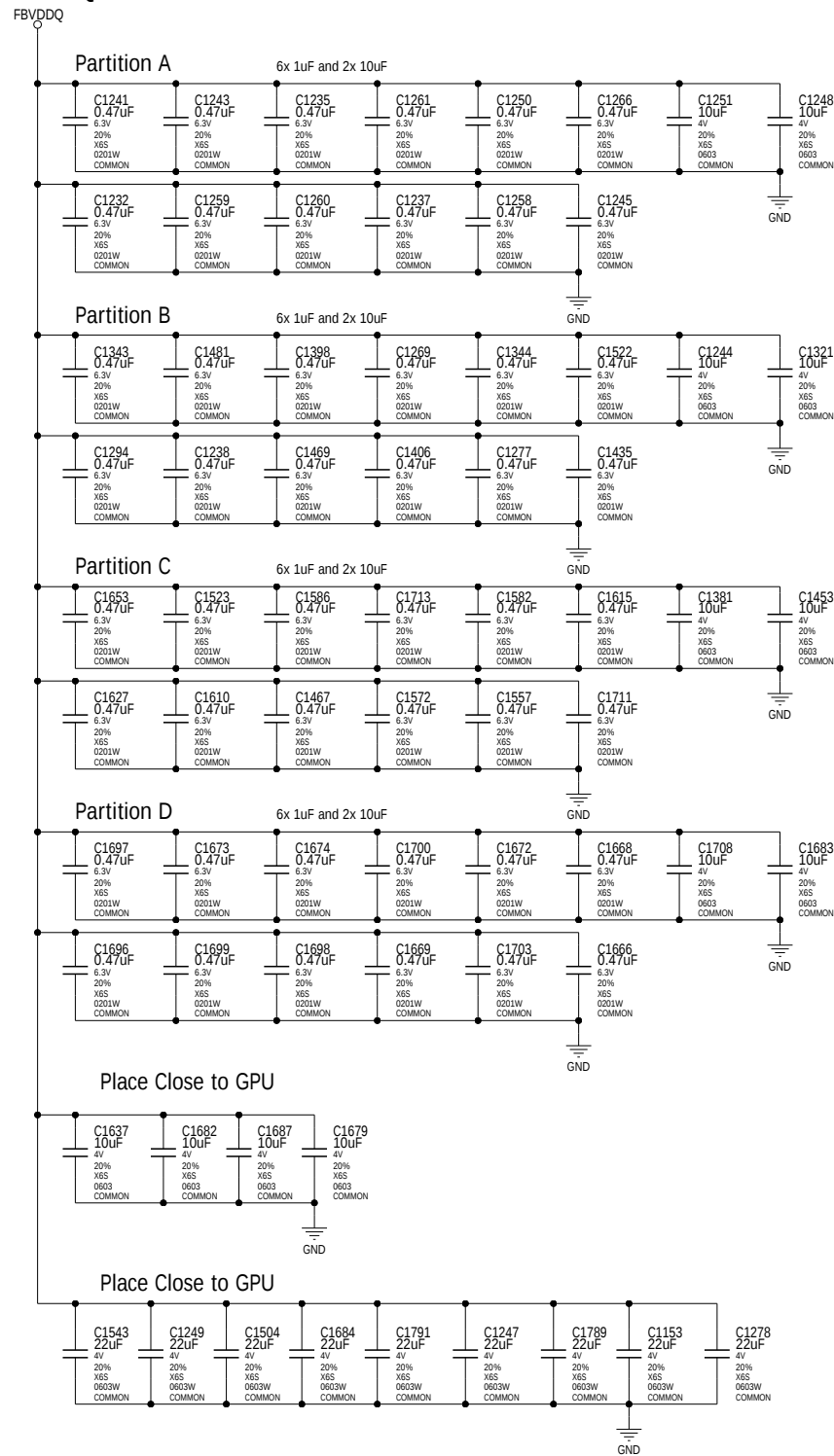


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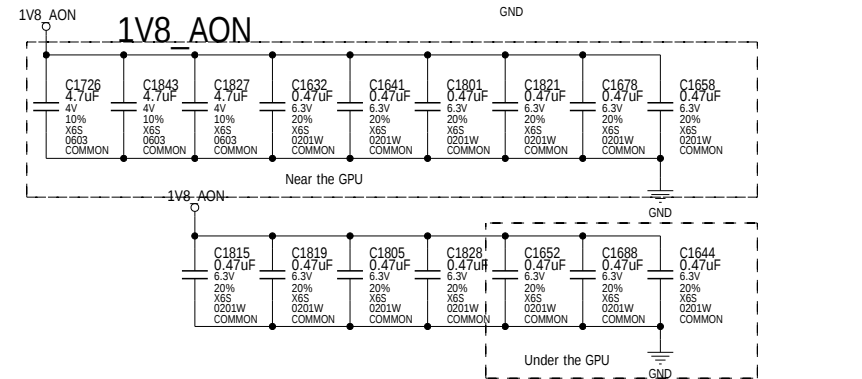
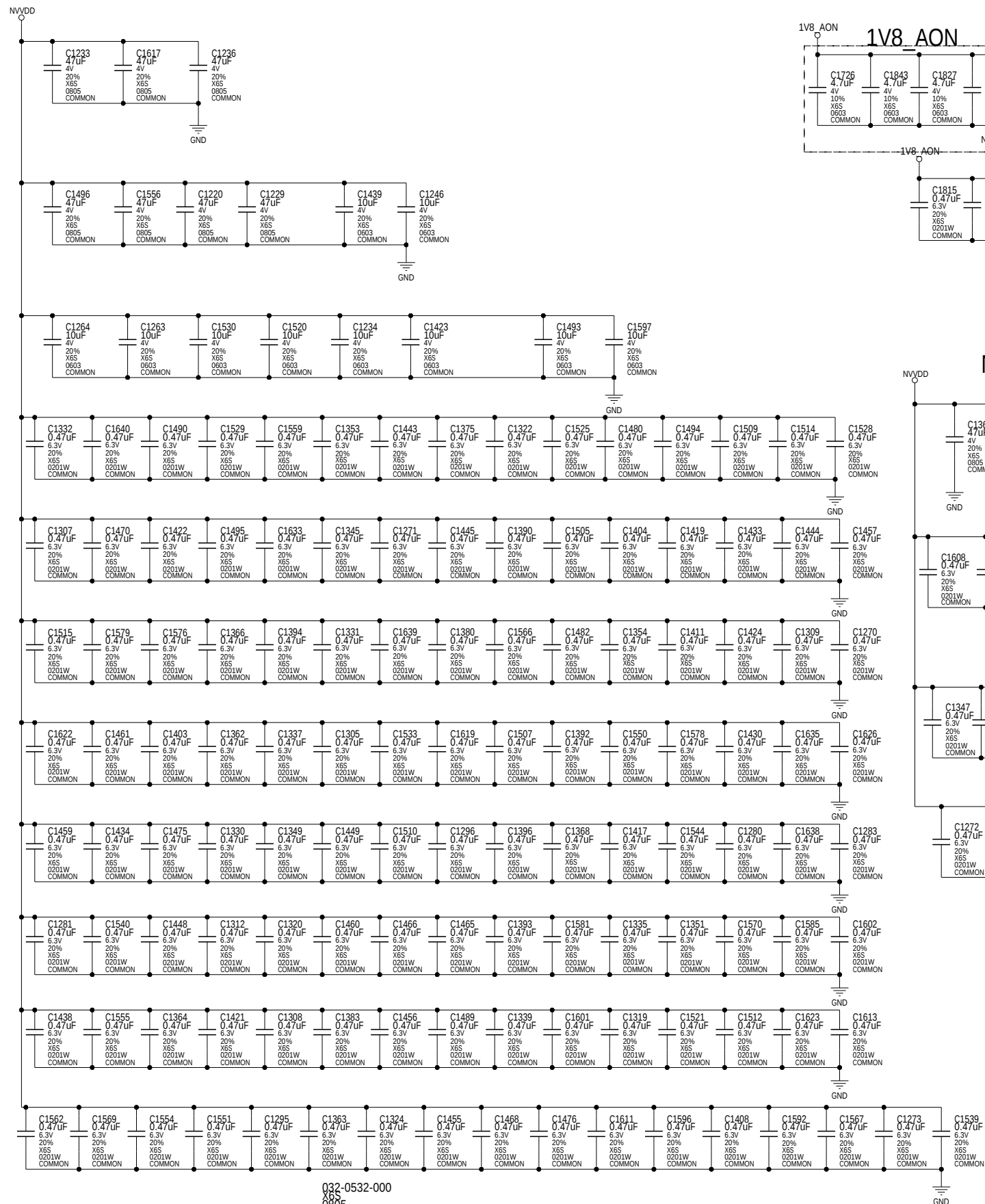
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PAGE DETAIL	GPU PWR and GND

Page16: GPU Decoupling

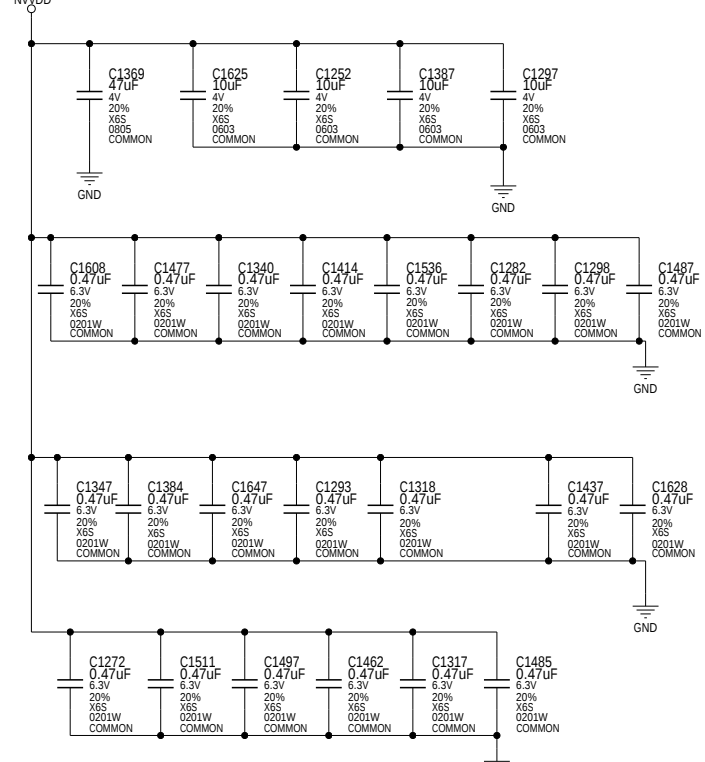
FBVDDQ



NVVDD



NVVDD



032-0532-000
X6S
090E

ASSEMBLY	SKU SCHEMATIC, COMMON & NO STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	GPU Decoupling

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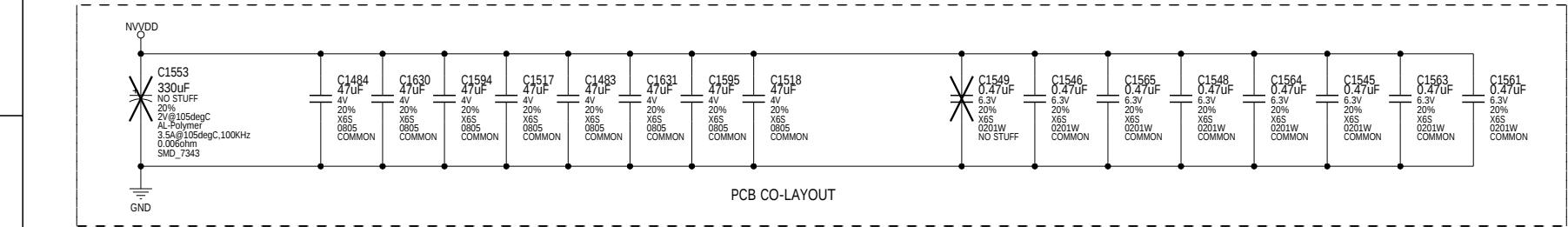
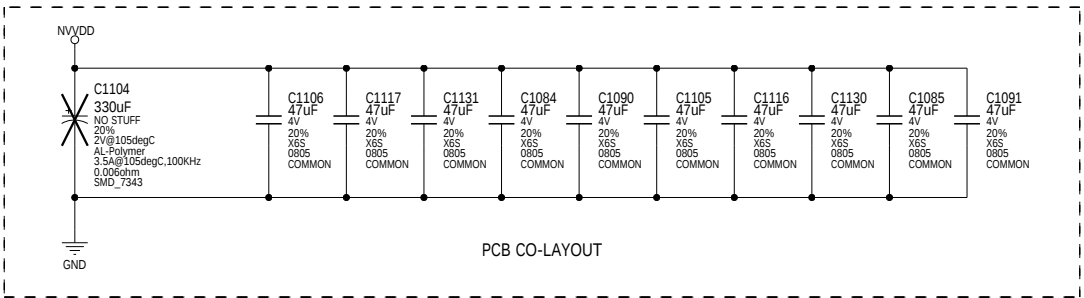
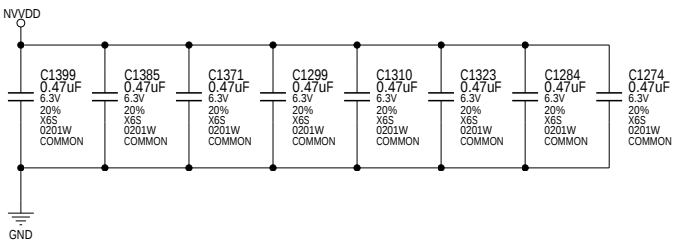
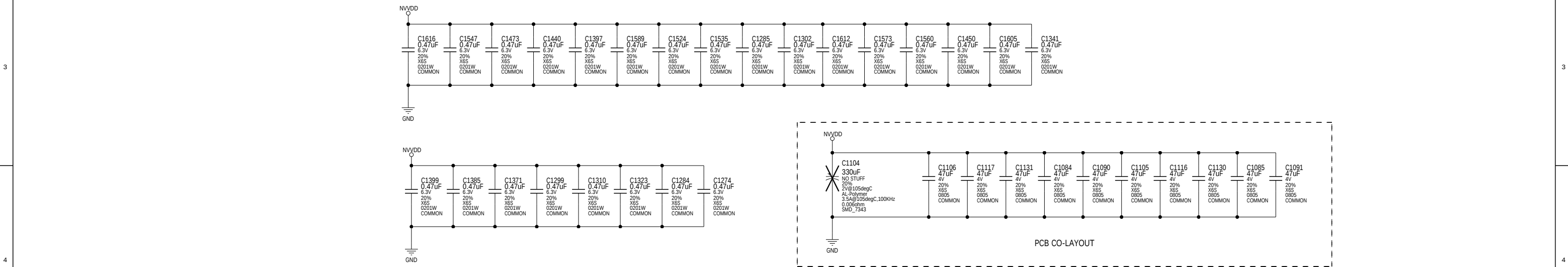
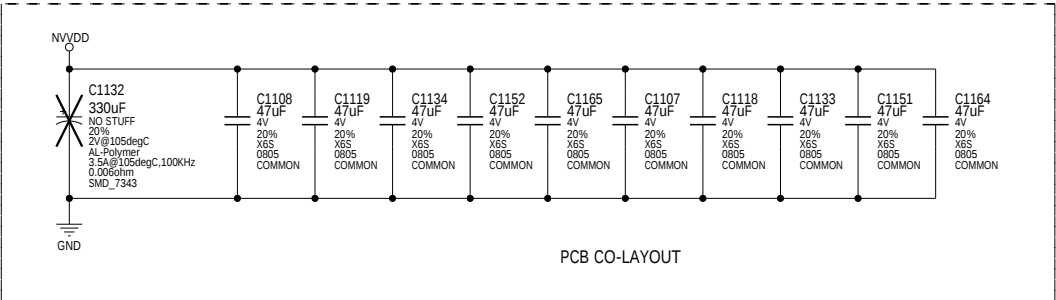
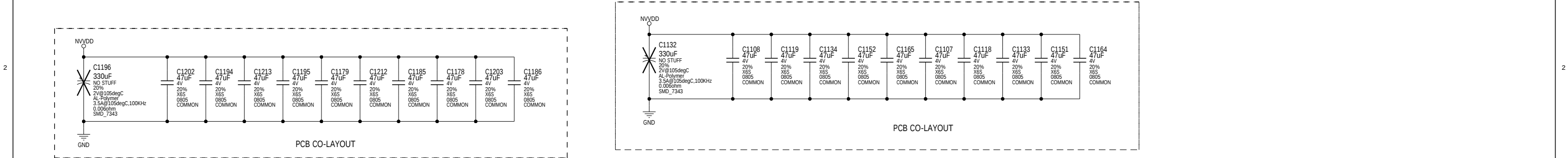
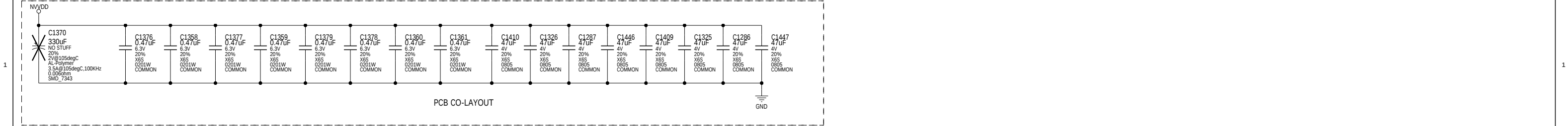
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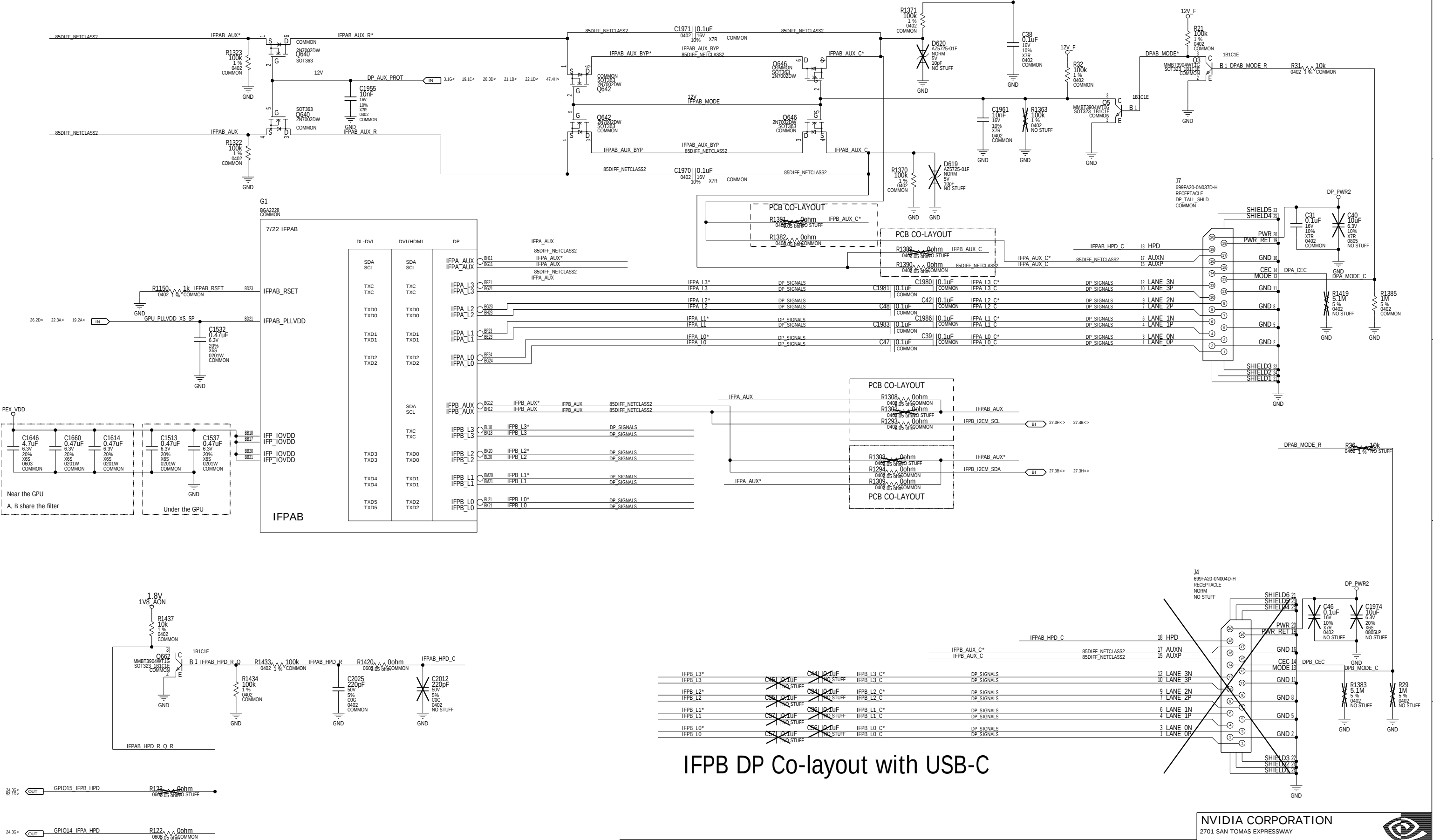
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Page17: GPU Decoupling



PAGE 18: IFPAB Tail-DP

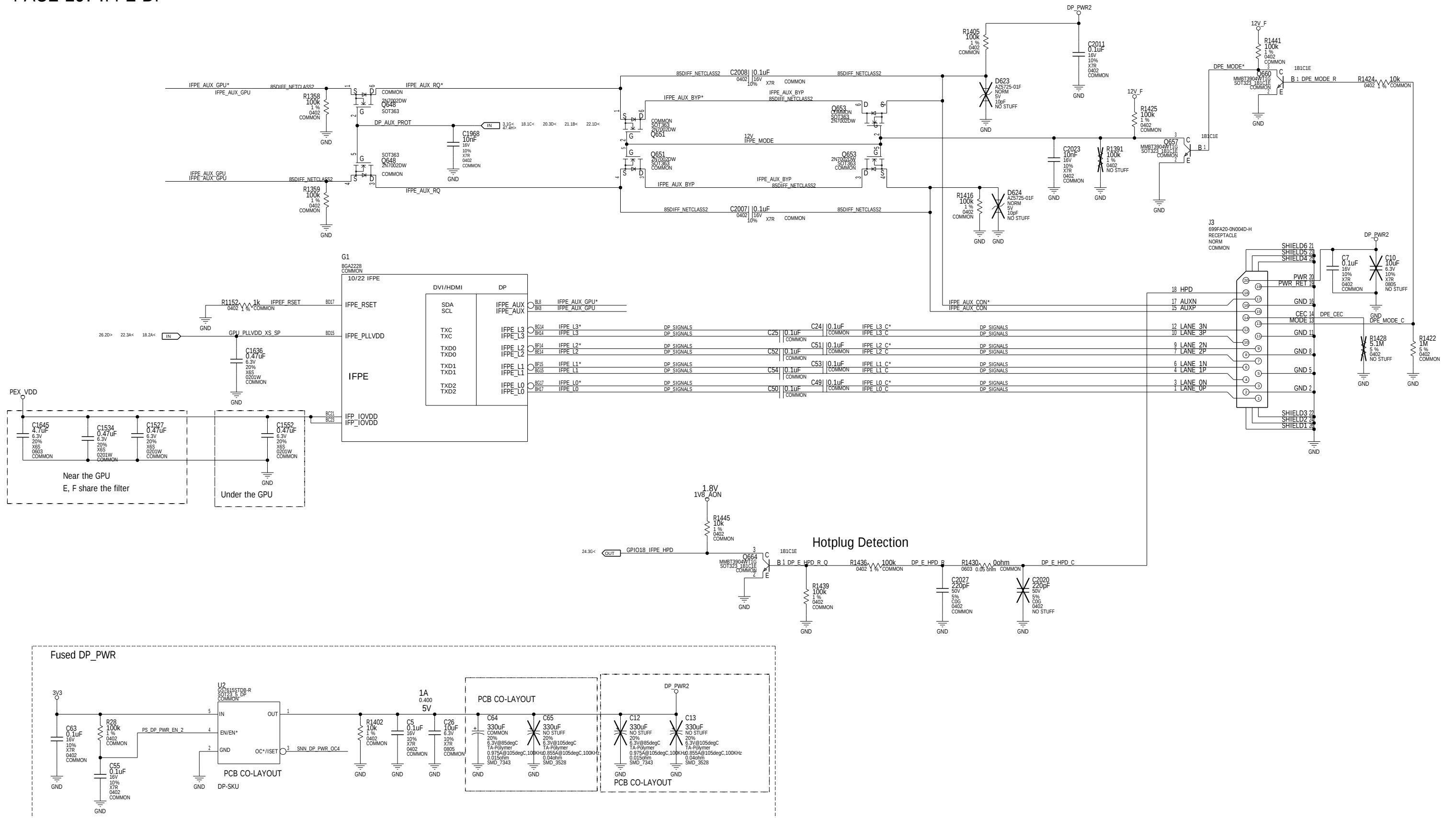


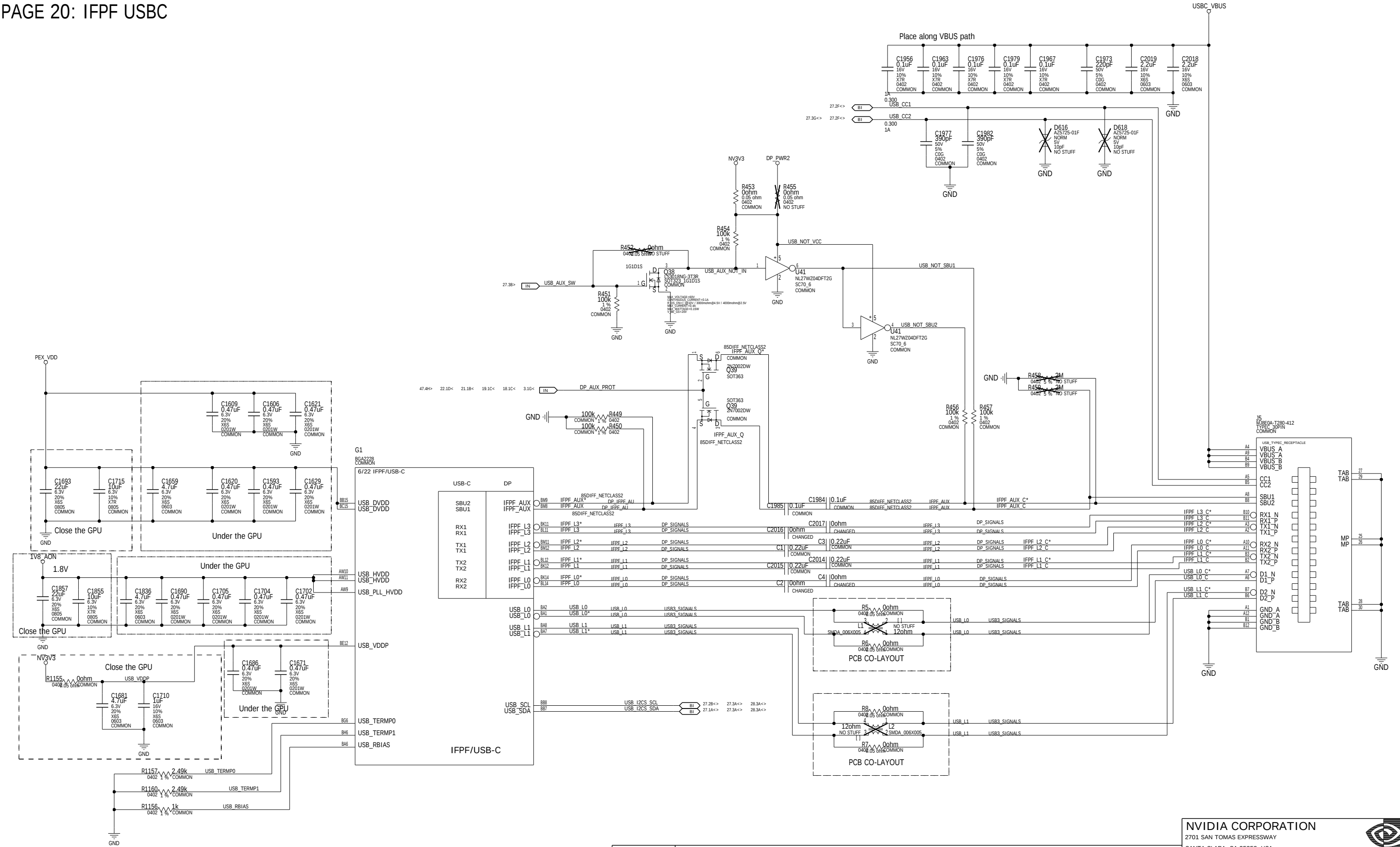
IFPB DP Co-layout with USB-C

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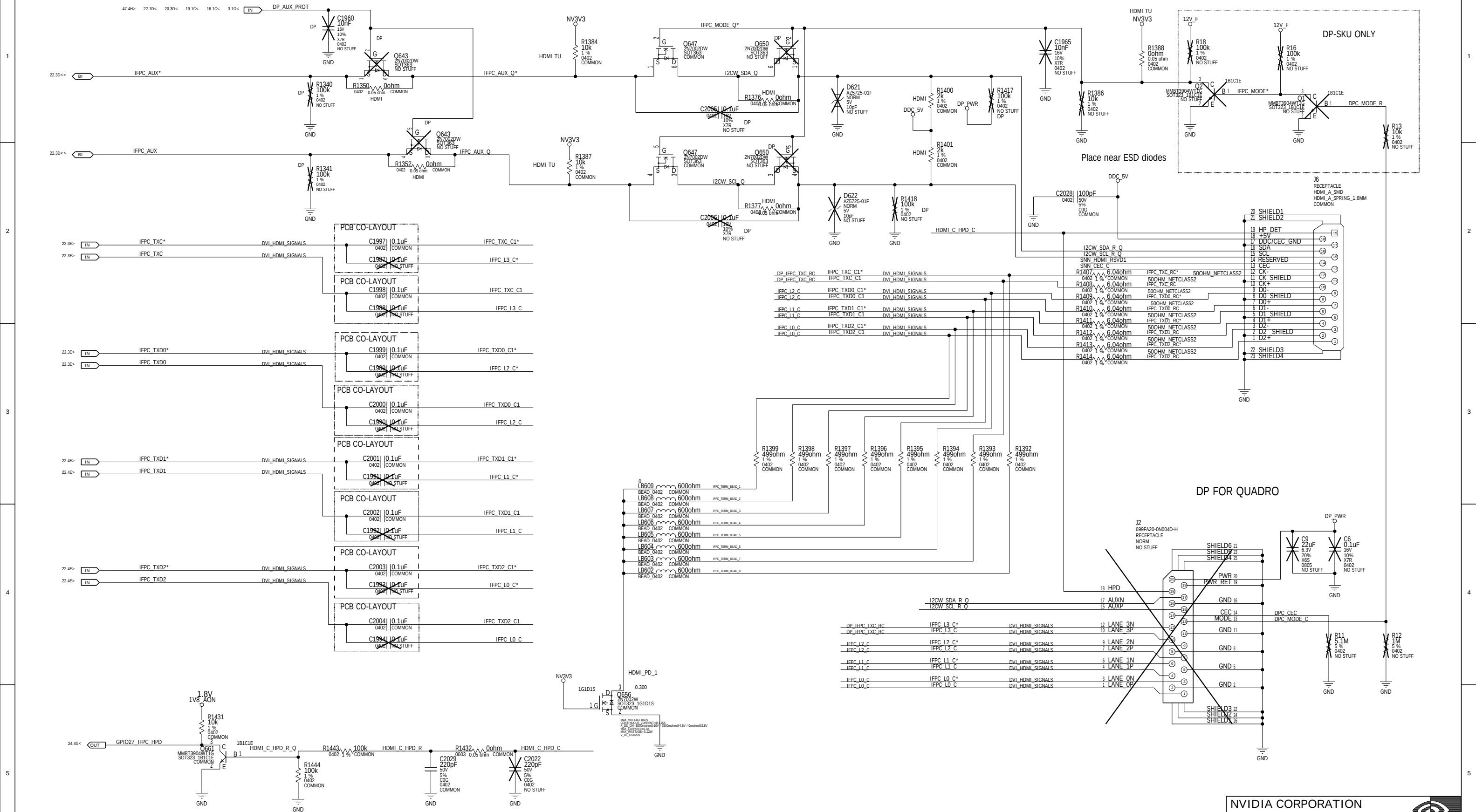
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PAGE 19: IFPE DP



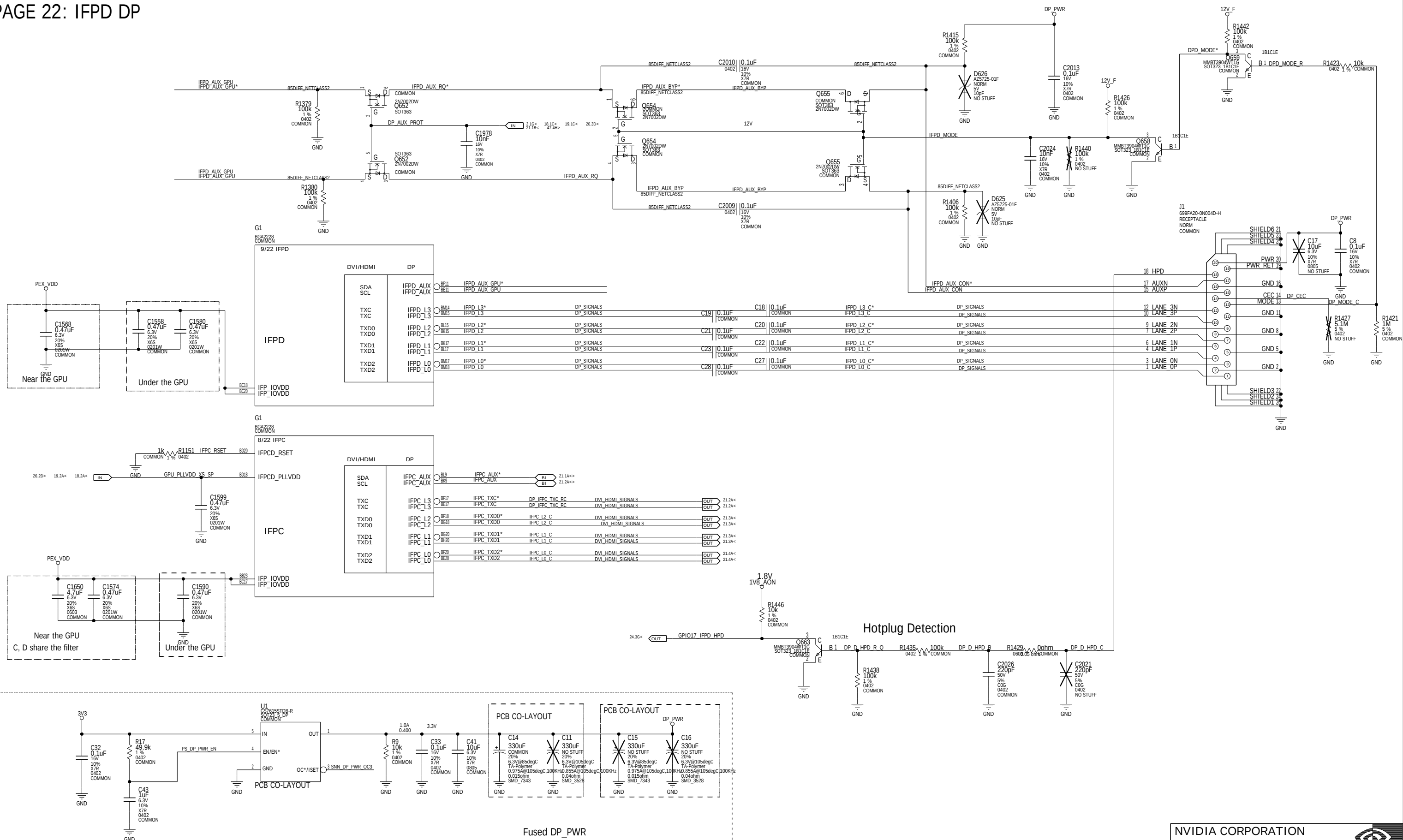


PAGE 21:IFPC HDMI 2.0/DP

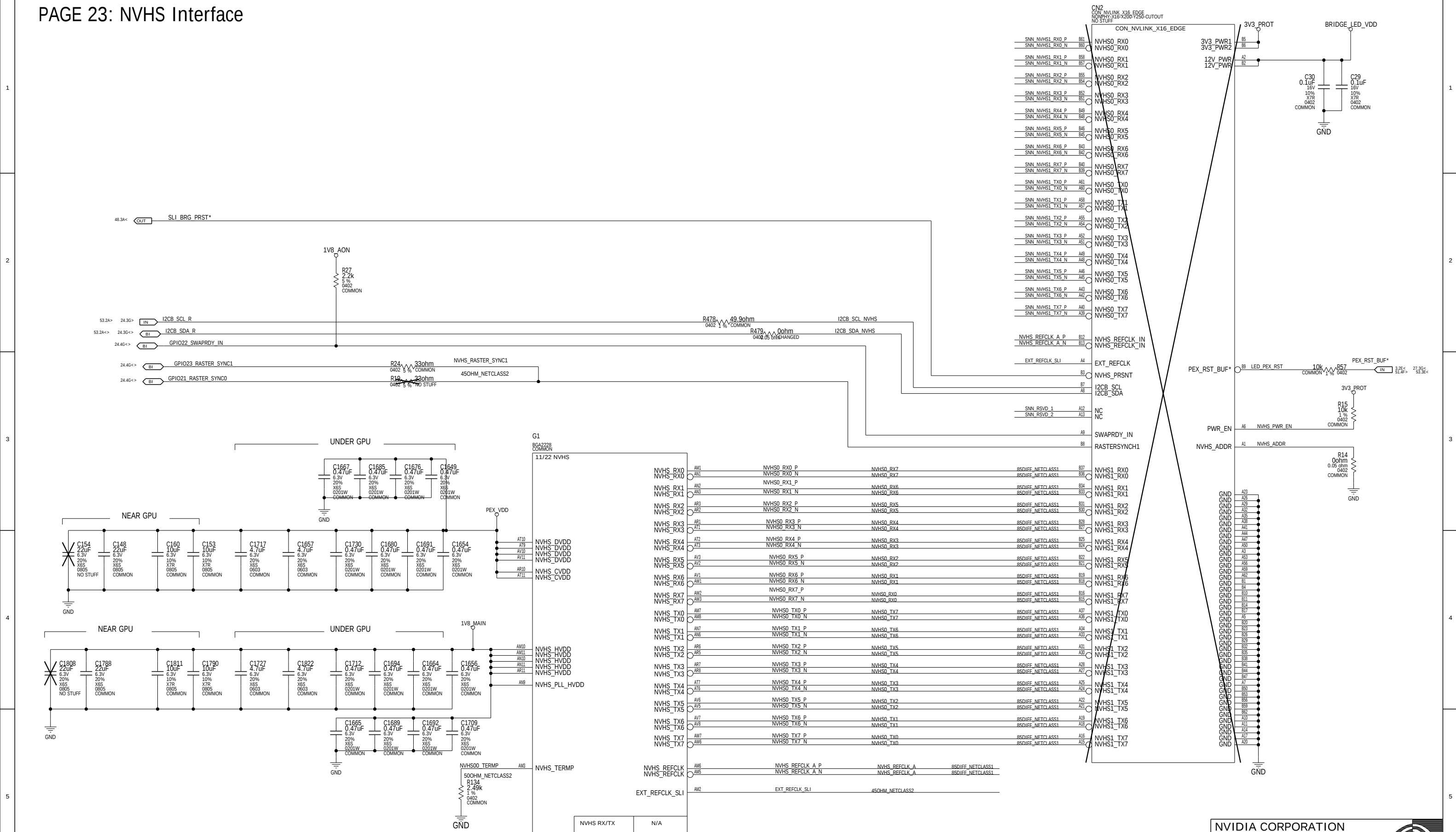


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PAGE 22: IFPD DP



PAGE 23: NVHS Interface

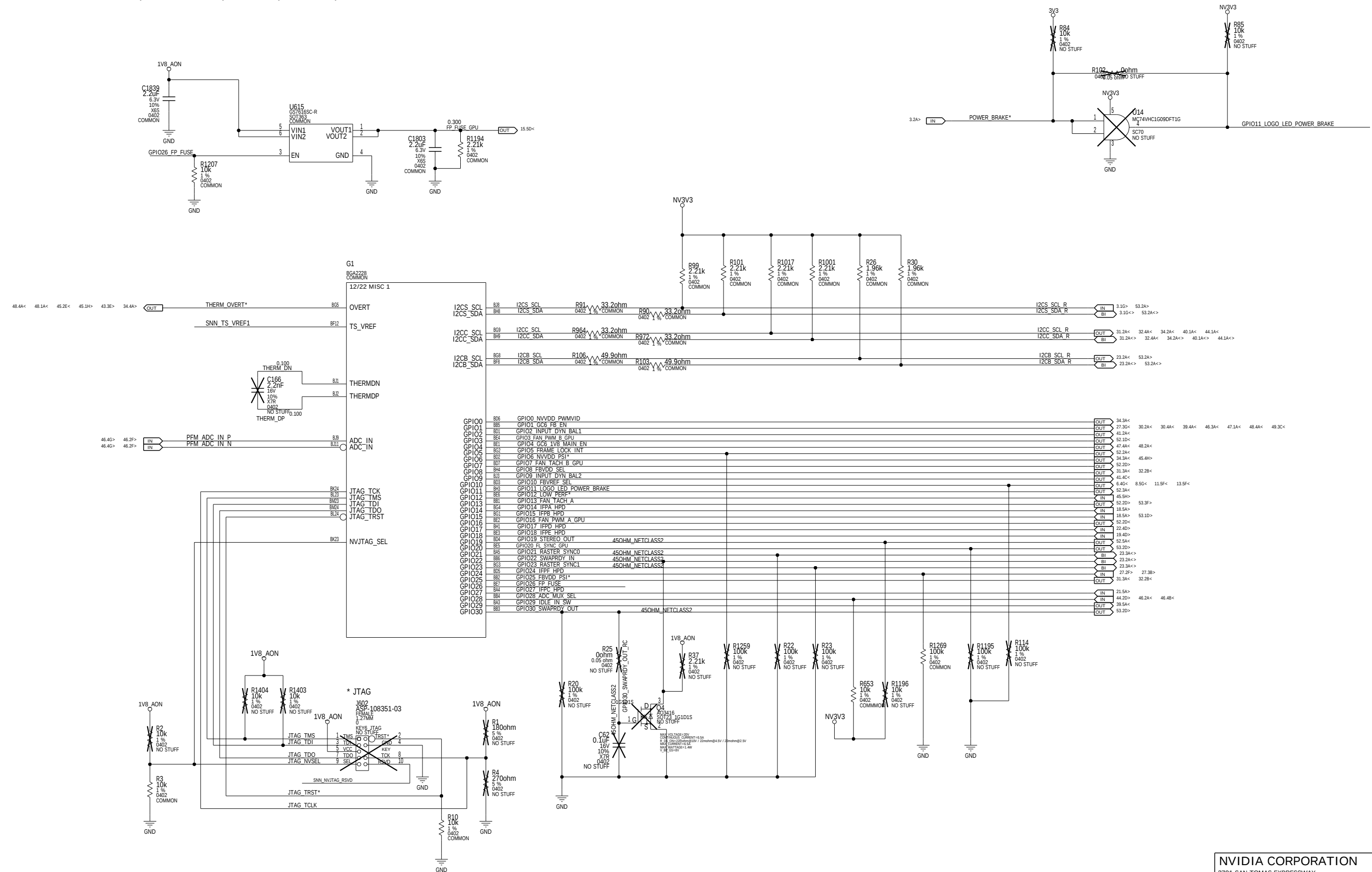


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PAGE DETAIL	NVHS INTERFACE

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PAGE 24: MISC: Fan, Thermal, JTAG, GPIO, STEREO



ASSEMBLY	SKU SCHEMATIC, COMMON & NO_STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	MISC: FAN,THERMAL,JTAG,GPIO,STEREO

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PAGE 25: MISC: ROM, Straps

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

DEFAULT

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Hynix
00111	16Gb	256-bit	Samsung
01000	16Gb	256-bit	Micron

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
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L	L	H	0	0	0	1
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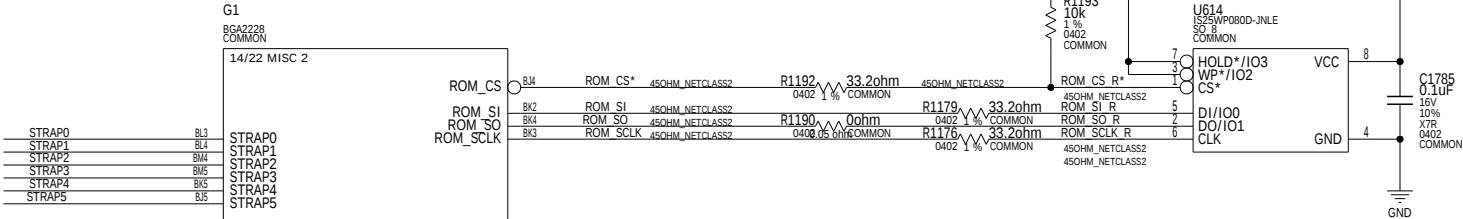
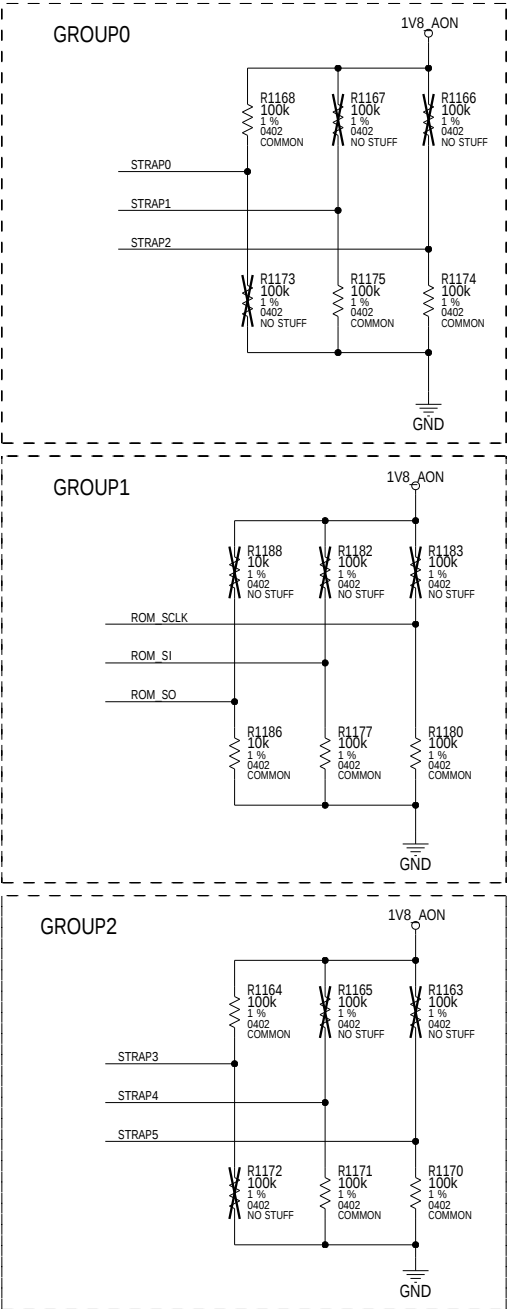
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

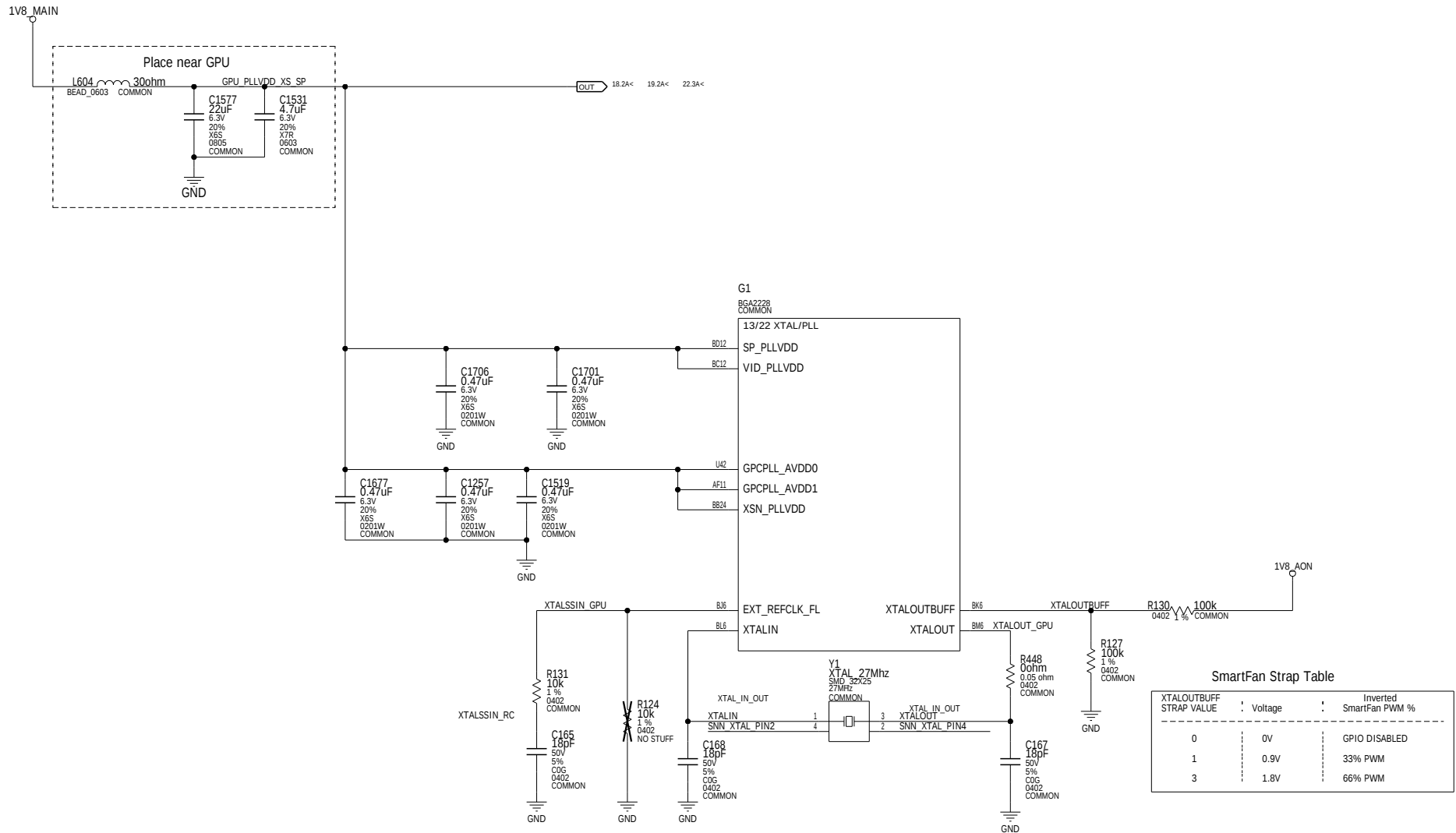
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
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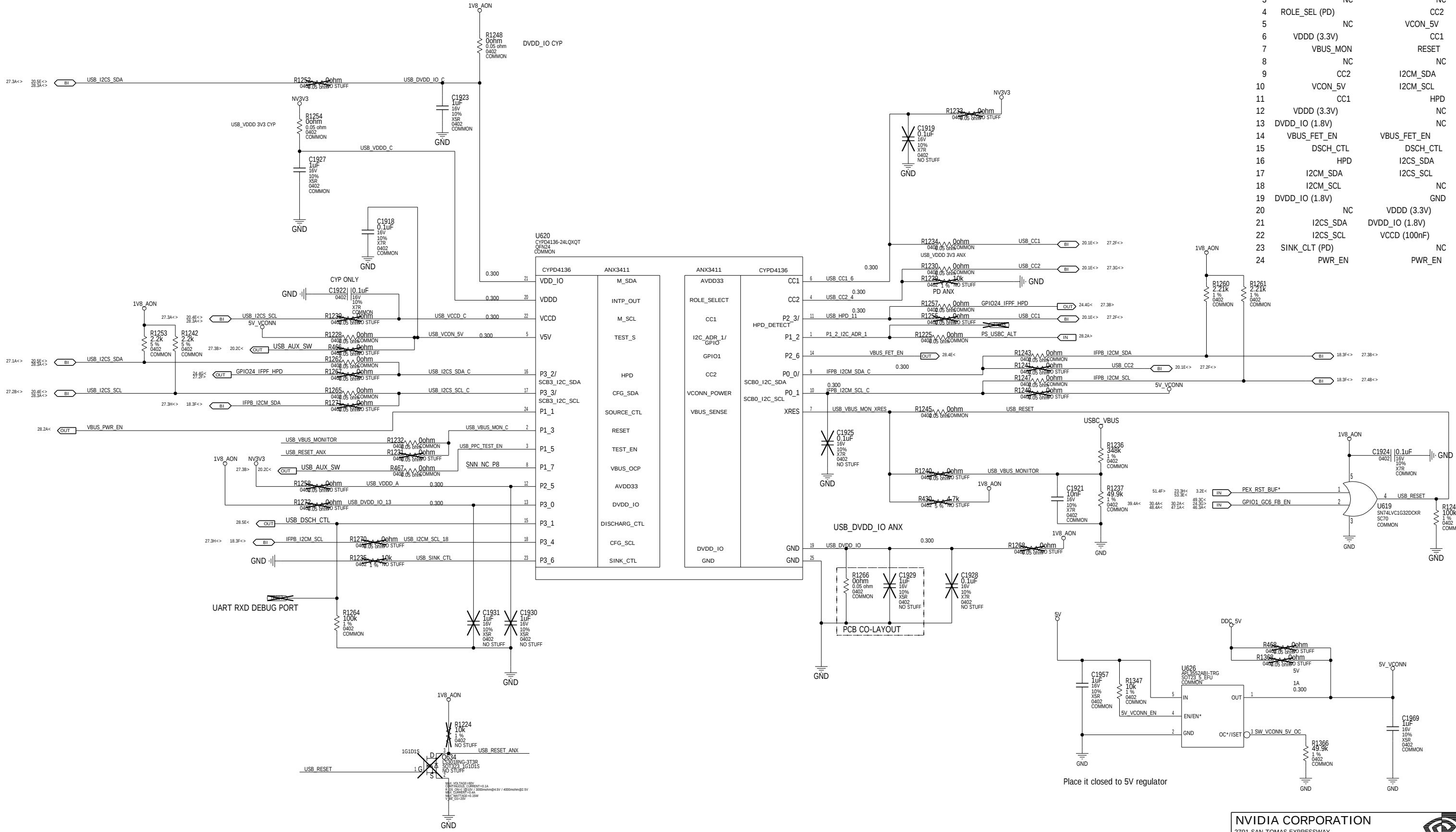


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PAGE 27: MISC: USB PPC



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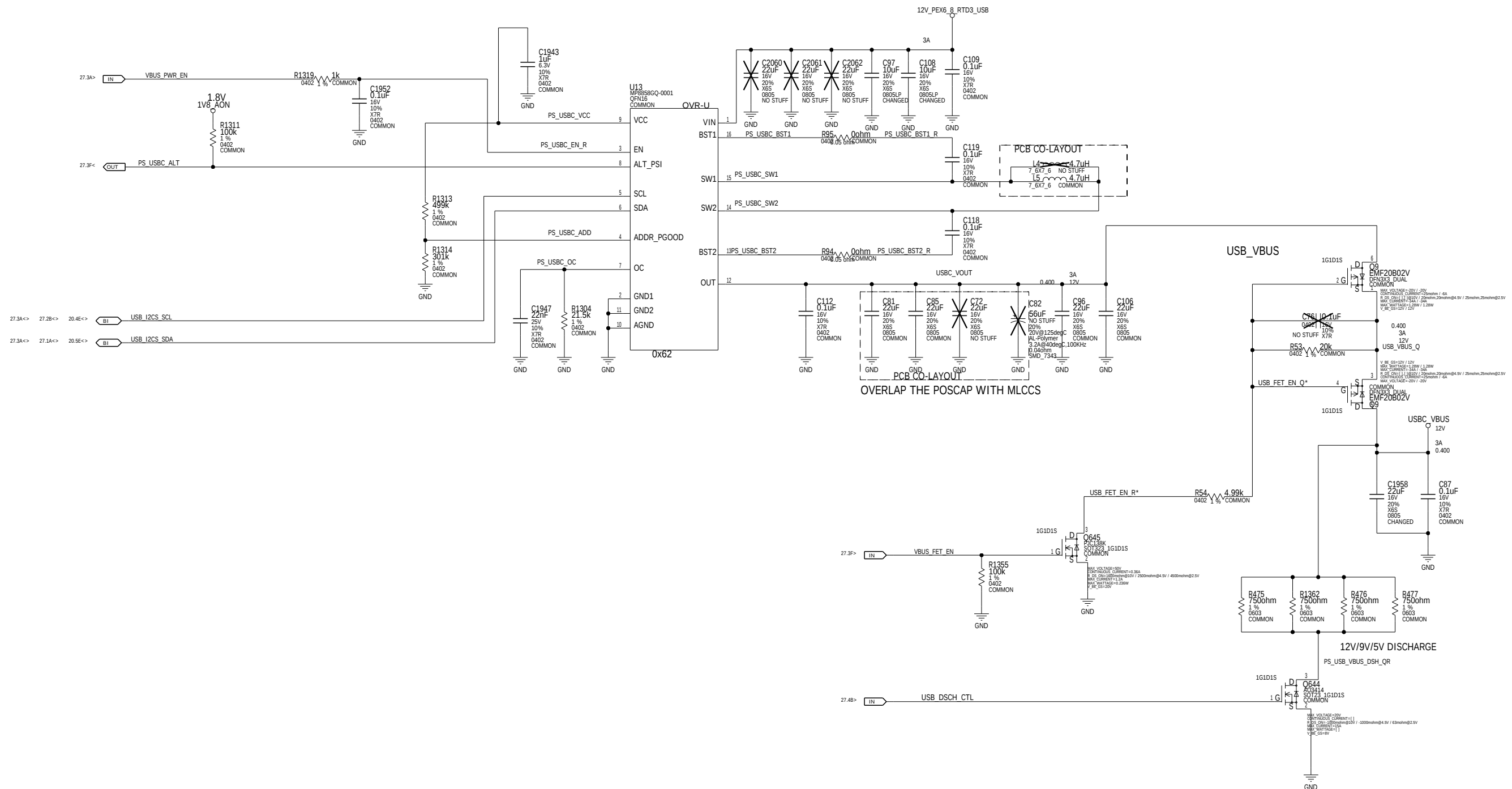
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PAGE DETAIL	PS: USB VR

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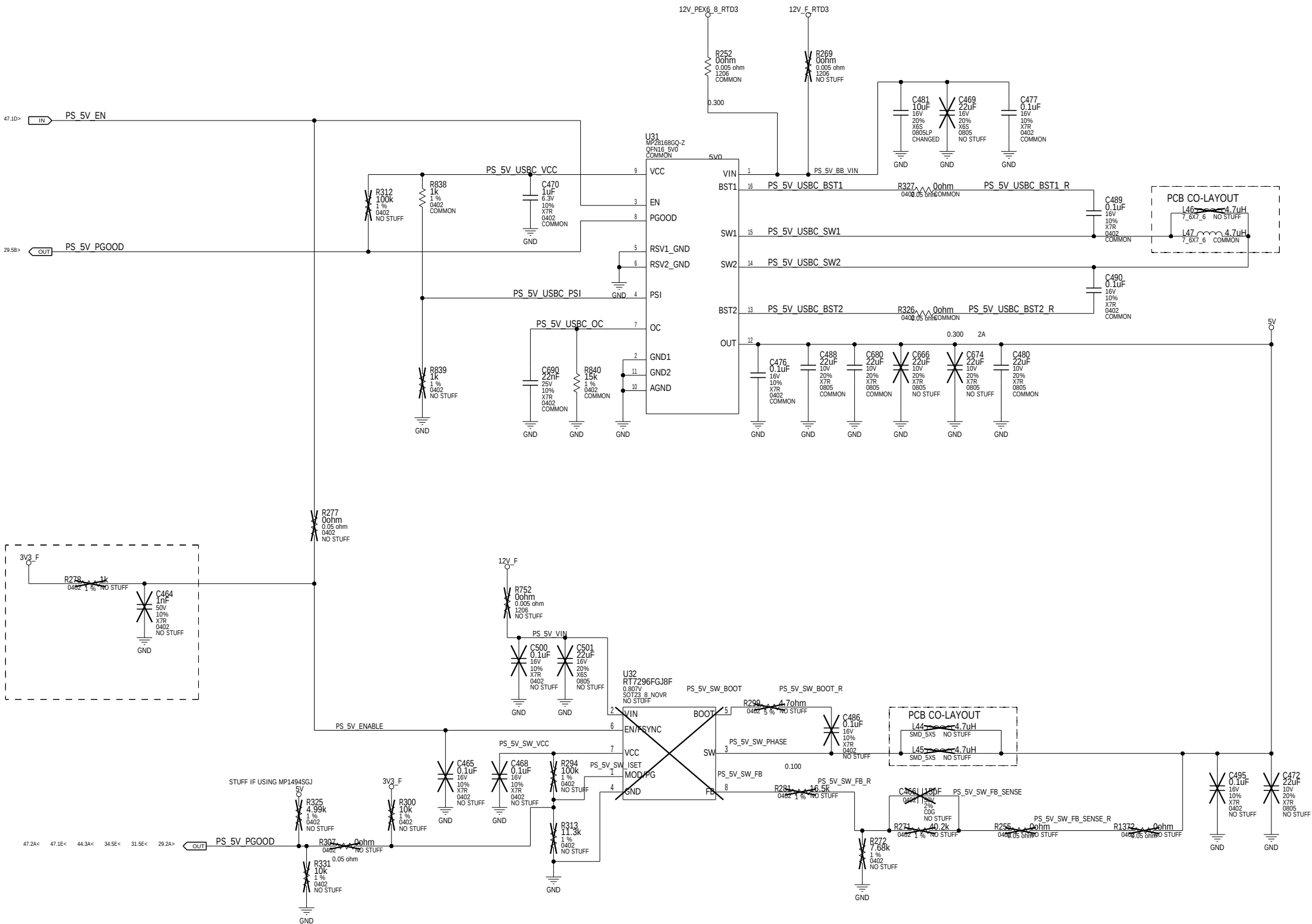
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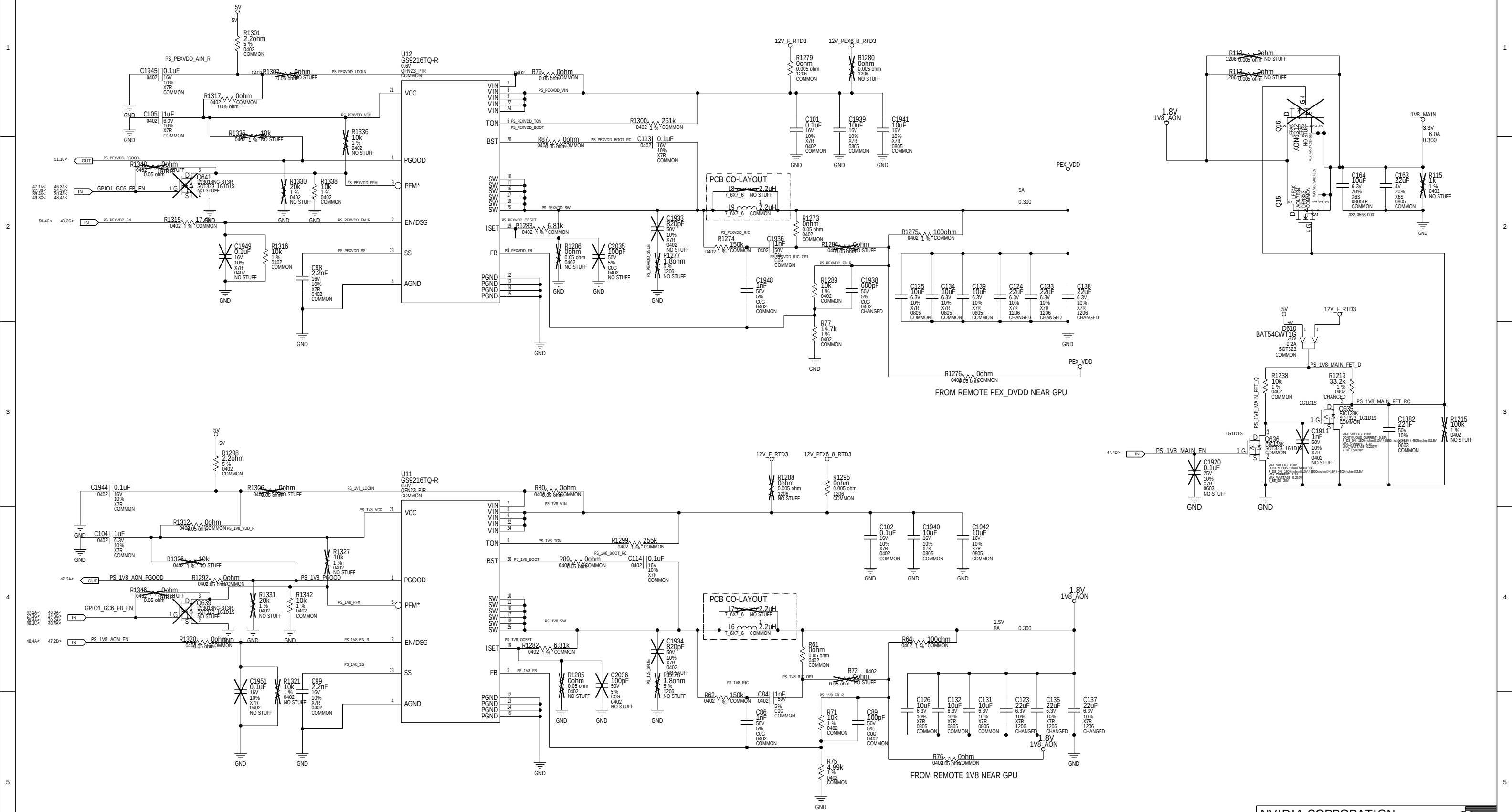
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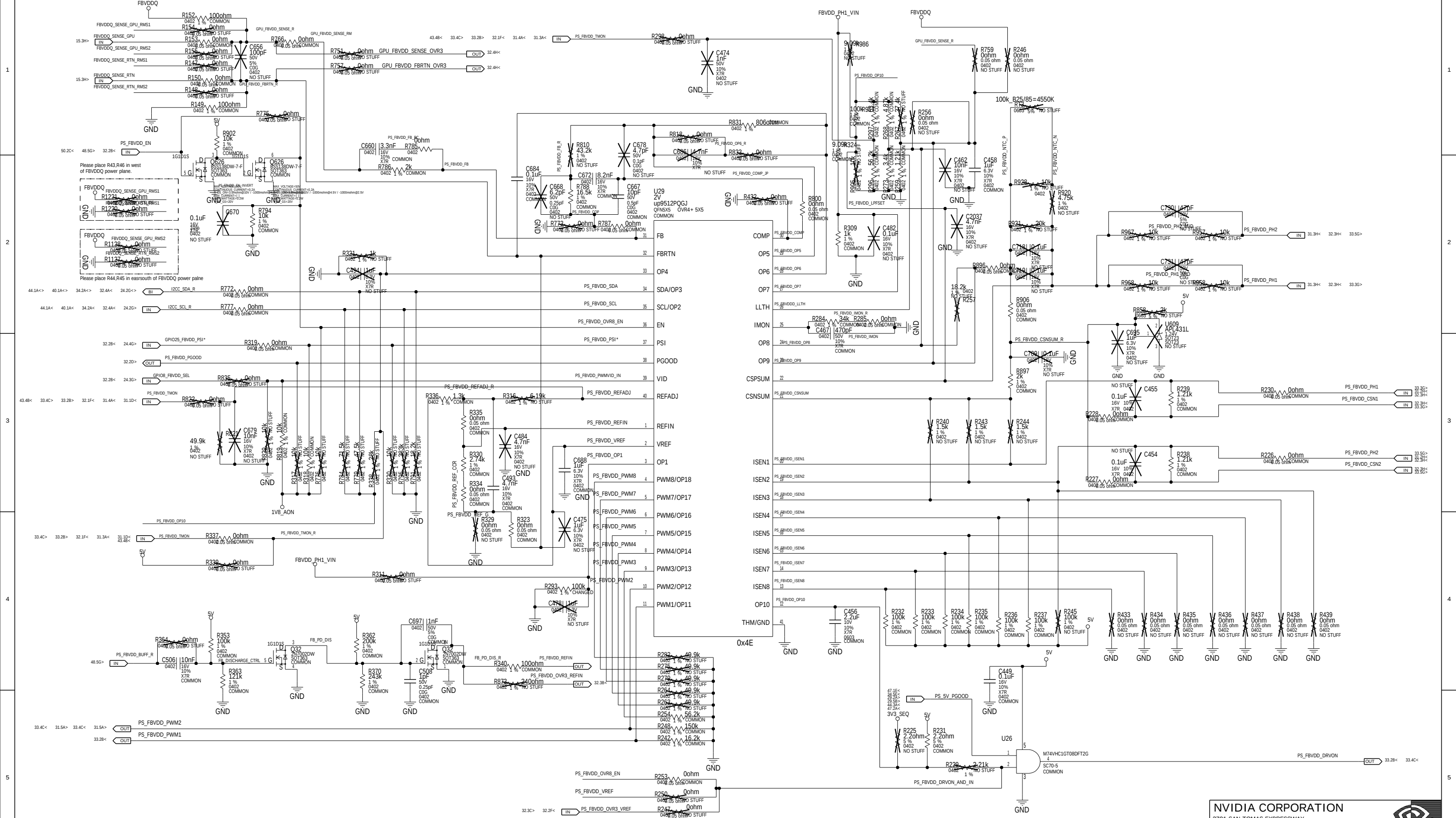
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PAGE 31: PS: FBVDD Controller



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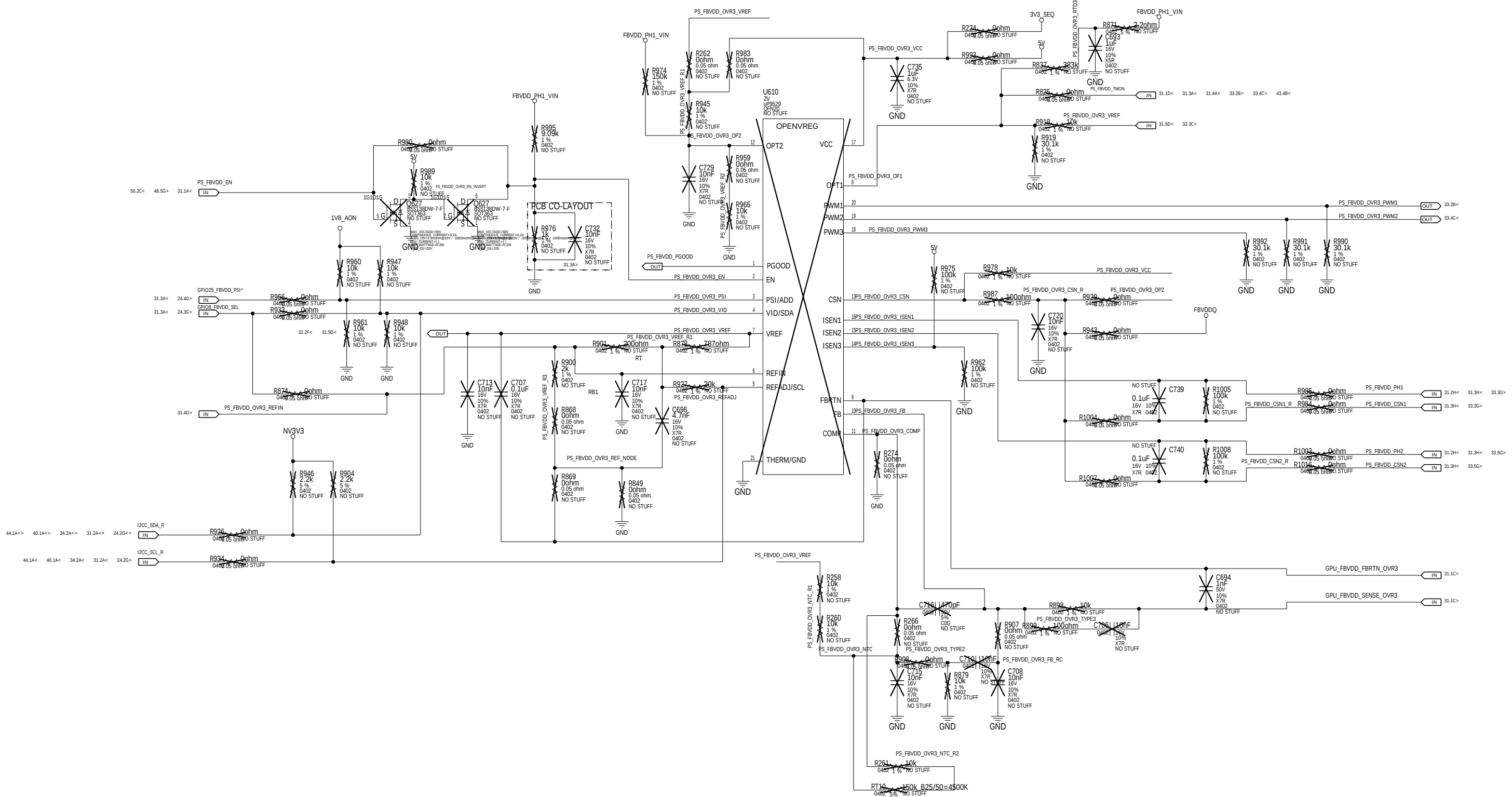


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PAGE 32: PS: FBVDD Controller OVR3



ASSEMBLY	SKU SCHEMATIC, COMMON & NO STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	PS: FBVDD CONTROLLER OVR3

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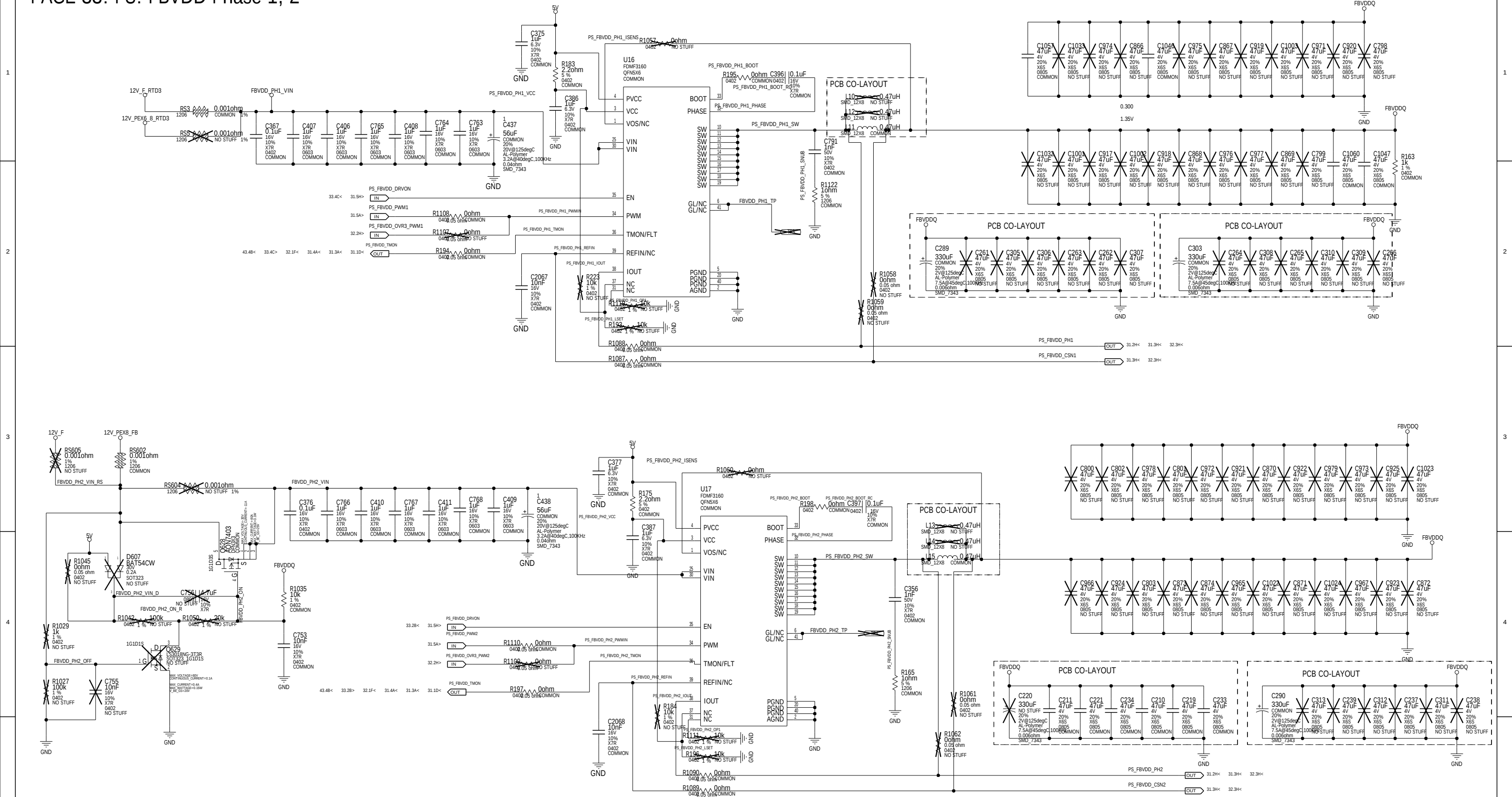
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PAGE 33: PS: FBVDD Phase 1, 2



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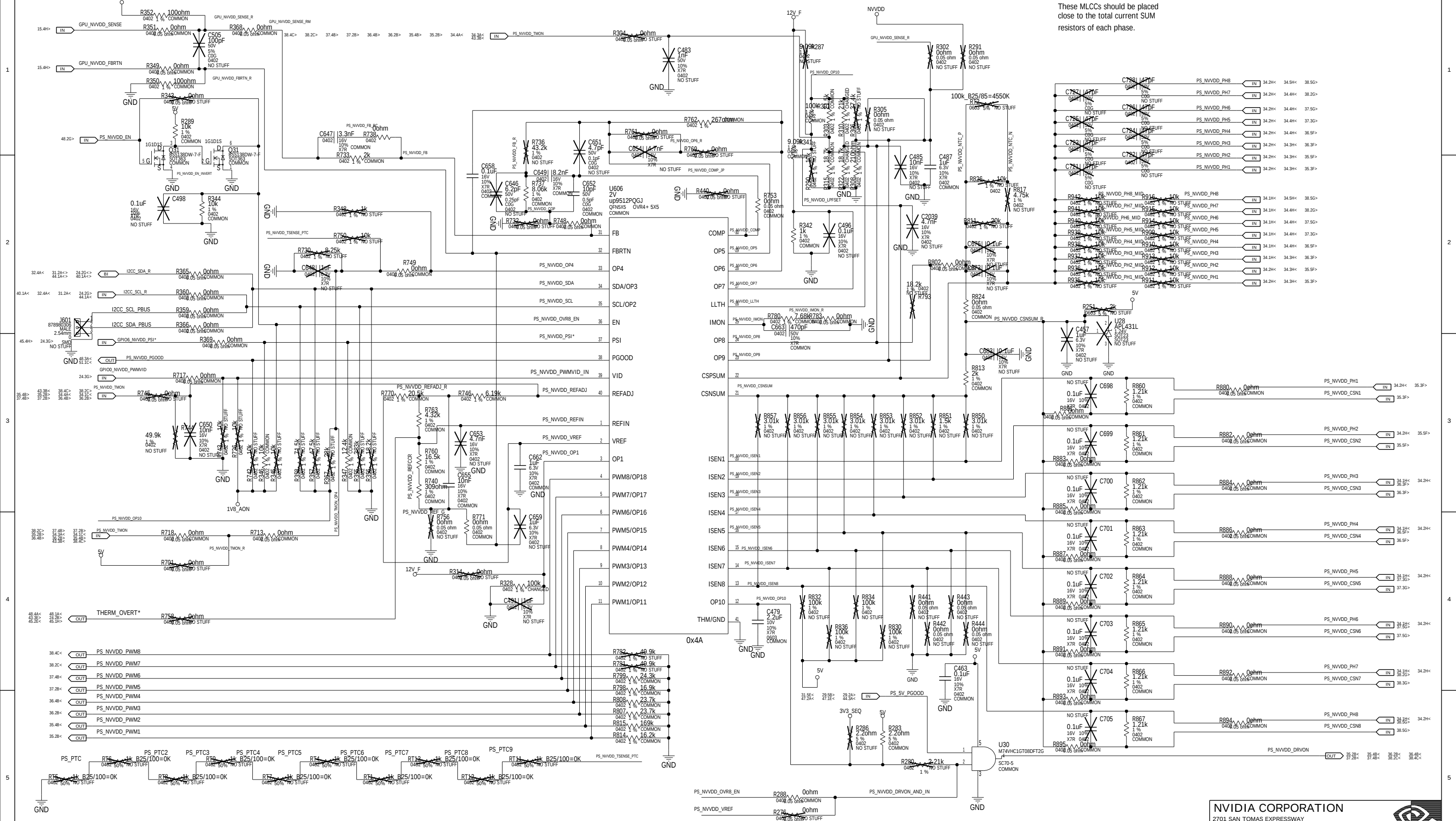
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ASSEMBLY	SKU SCHEMATIC, COMMON & NO STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	PS: FBVDD PHASE 1, 2

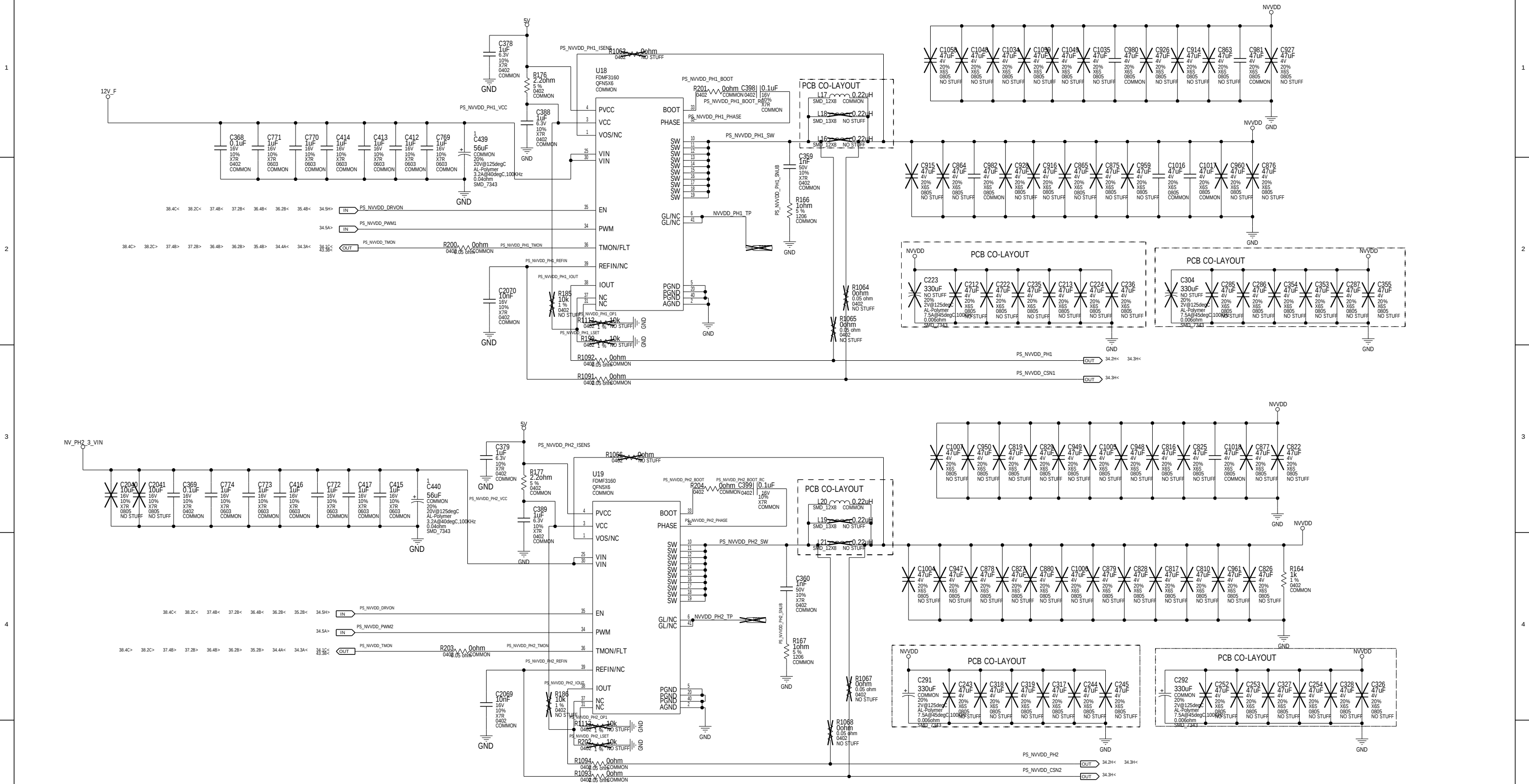
PAGE 34: PS: NVDD Controller OVR8



These MLCCs should be placed close to the total current SUM resistors of each phase.

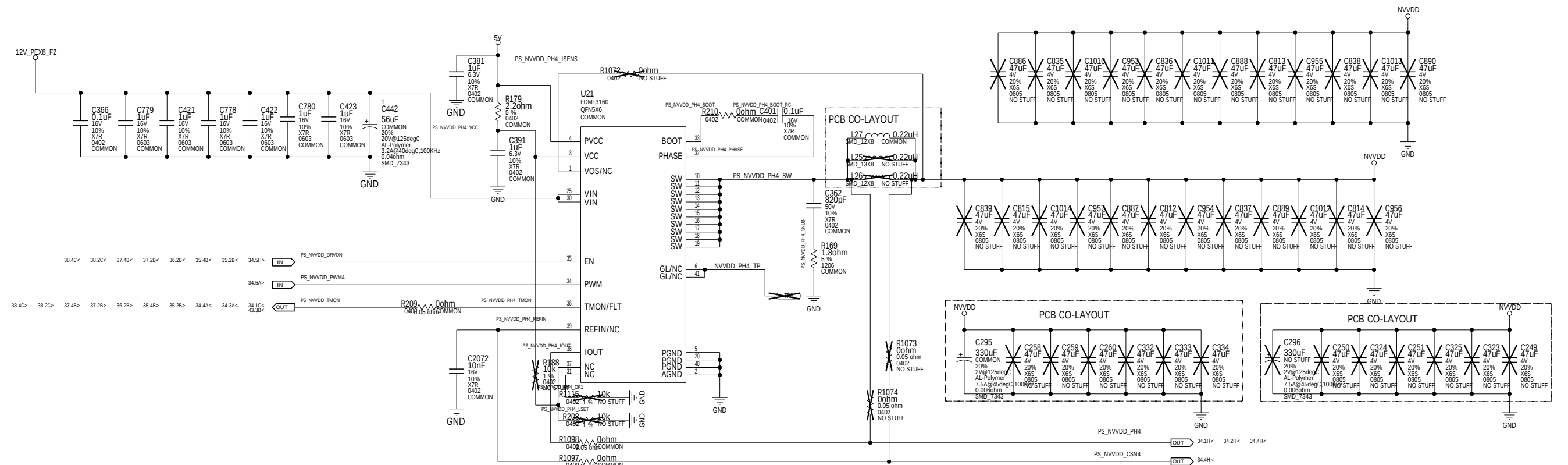
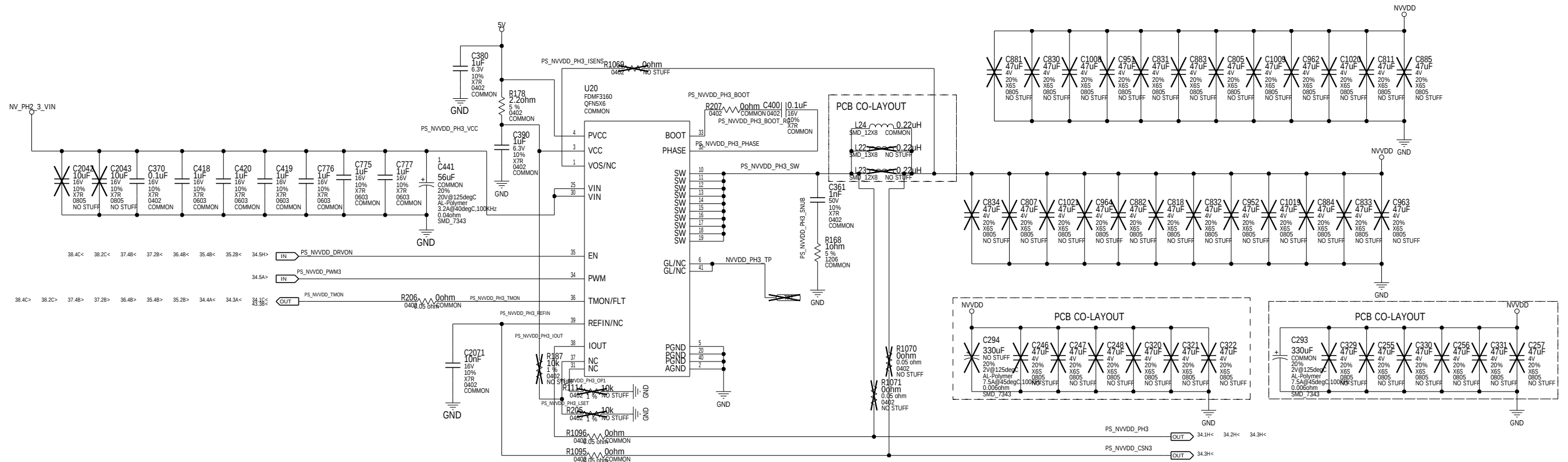
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PAGE 36: PS: NVVDD Phase 3, 4



ASSEMBLY	SKU SCHEMATIC, COMMON & NO STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	PS: NVDD Phase 3, 4

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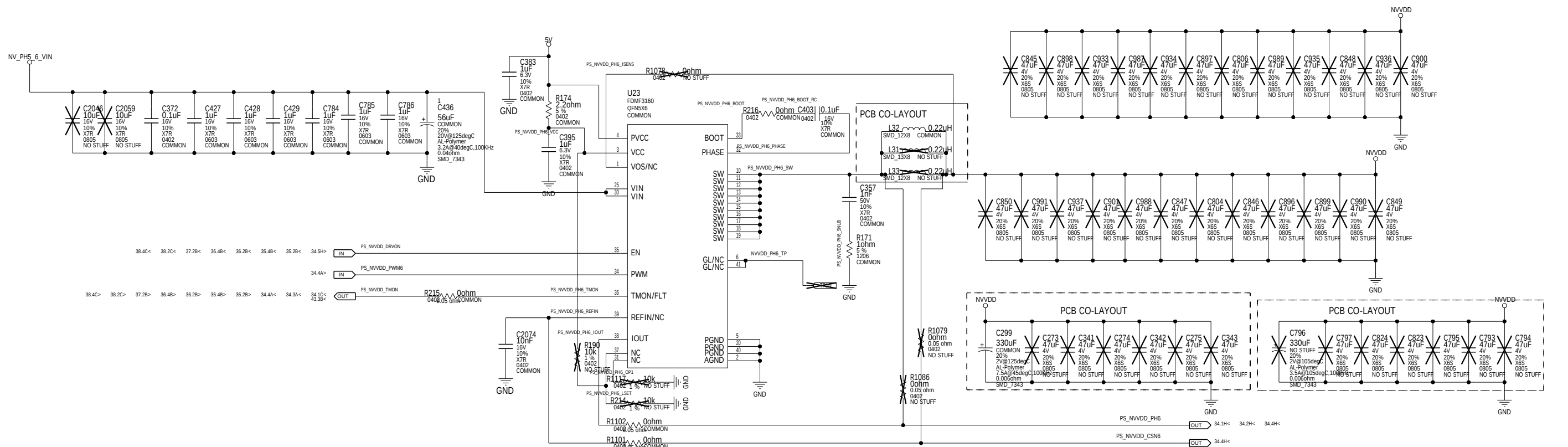
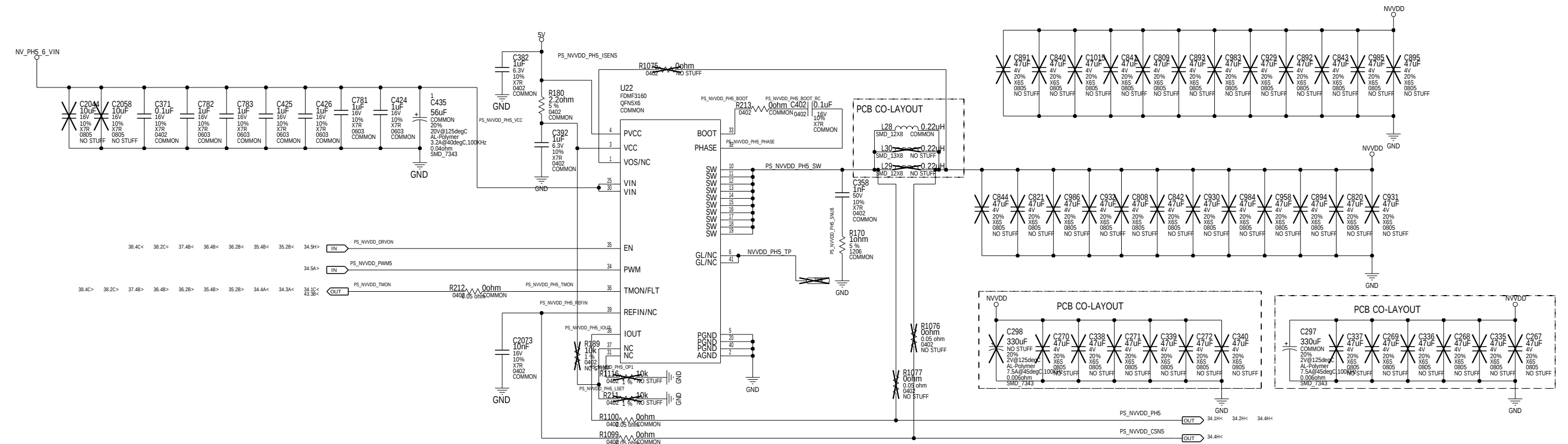
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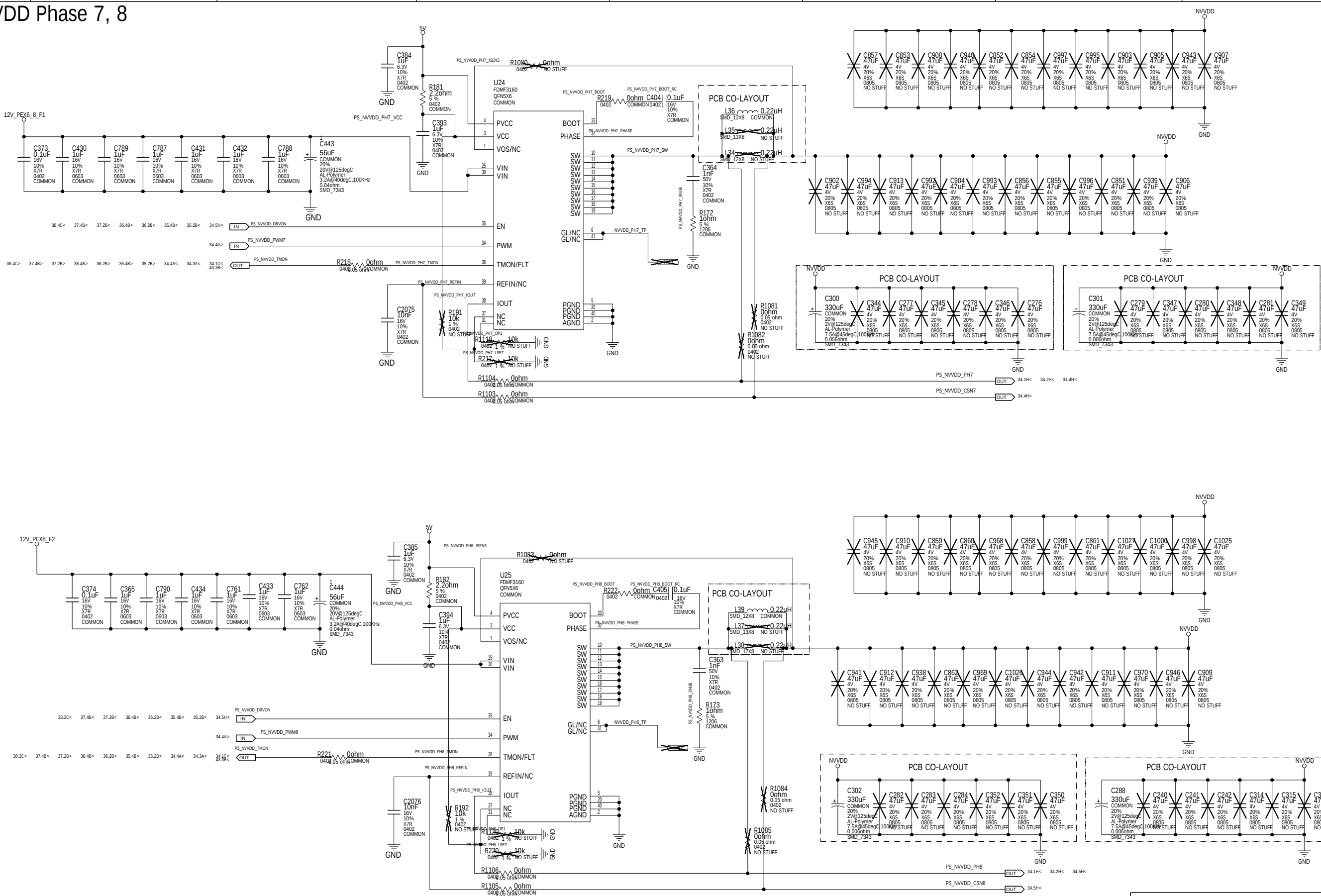


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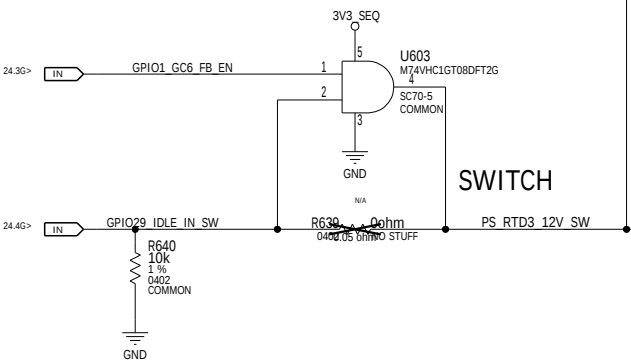
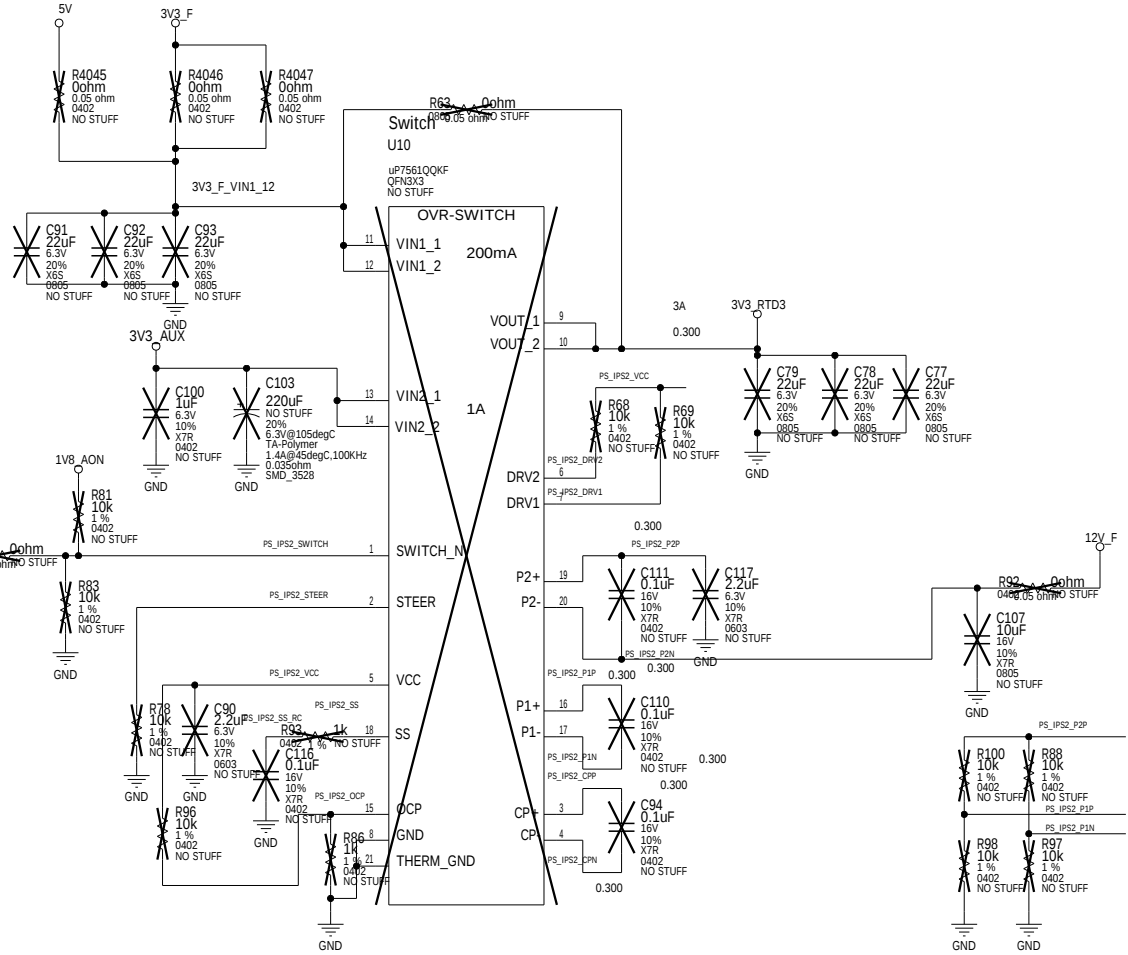
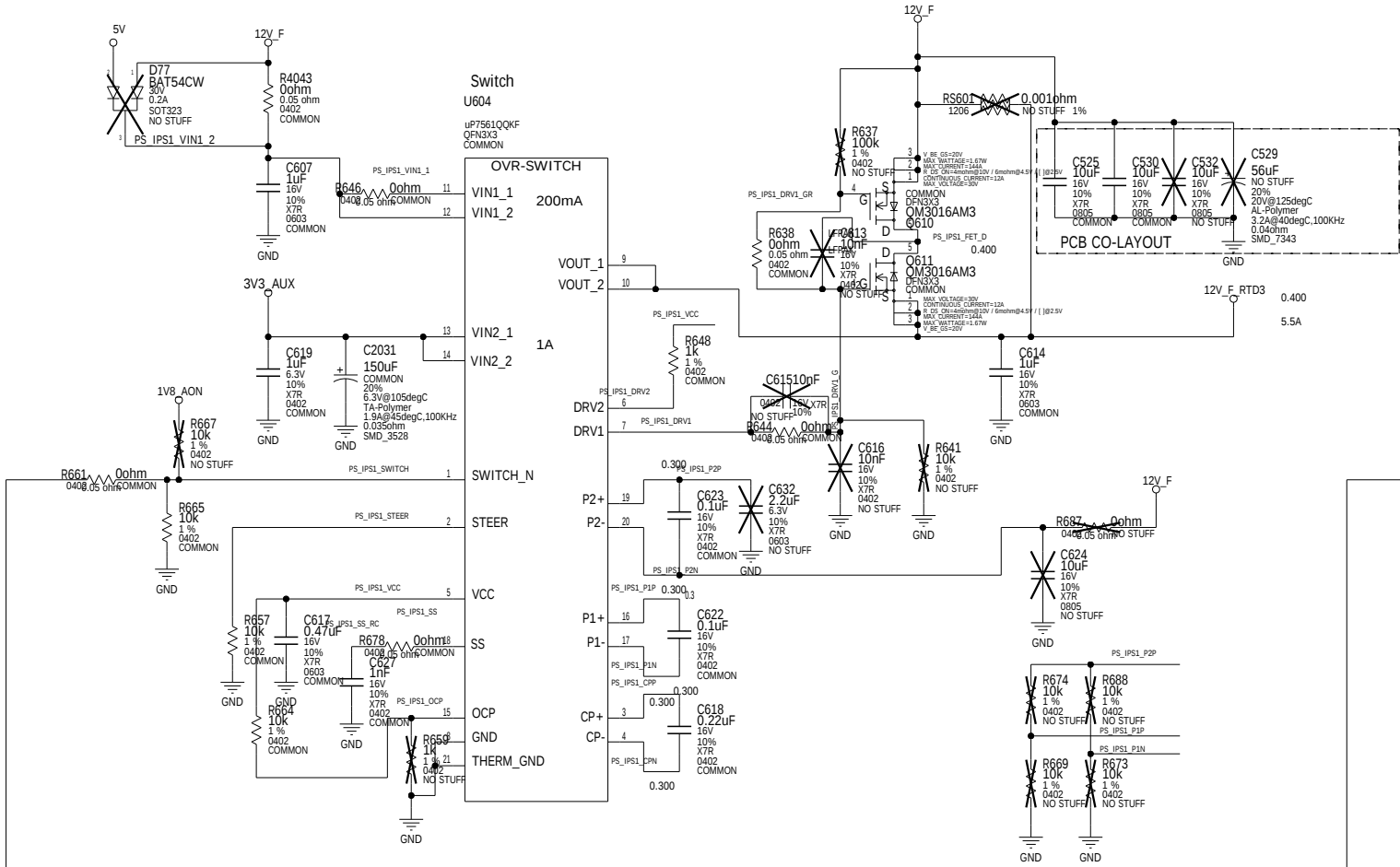
PAGE 38: PS:NVVDD Phase 7, 8



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AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

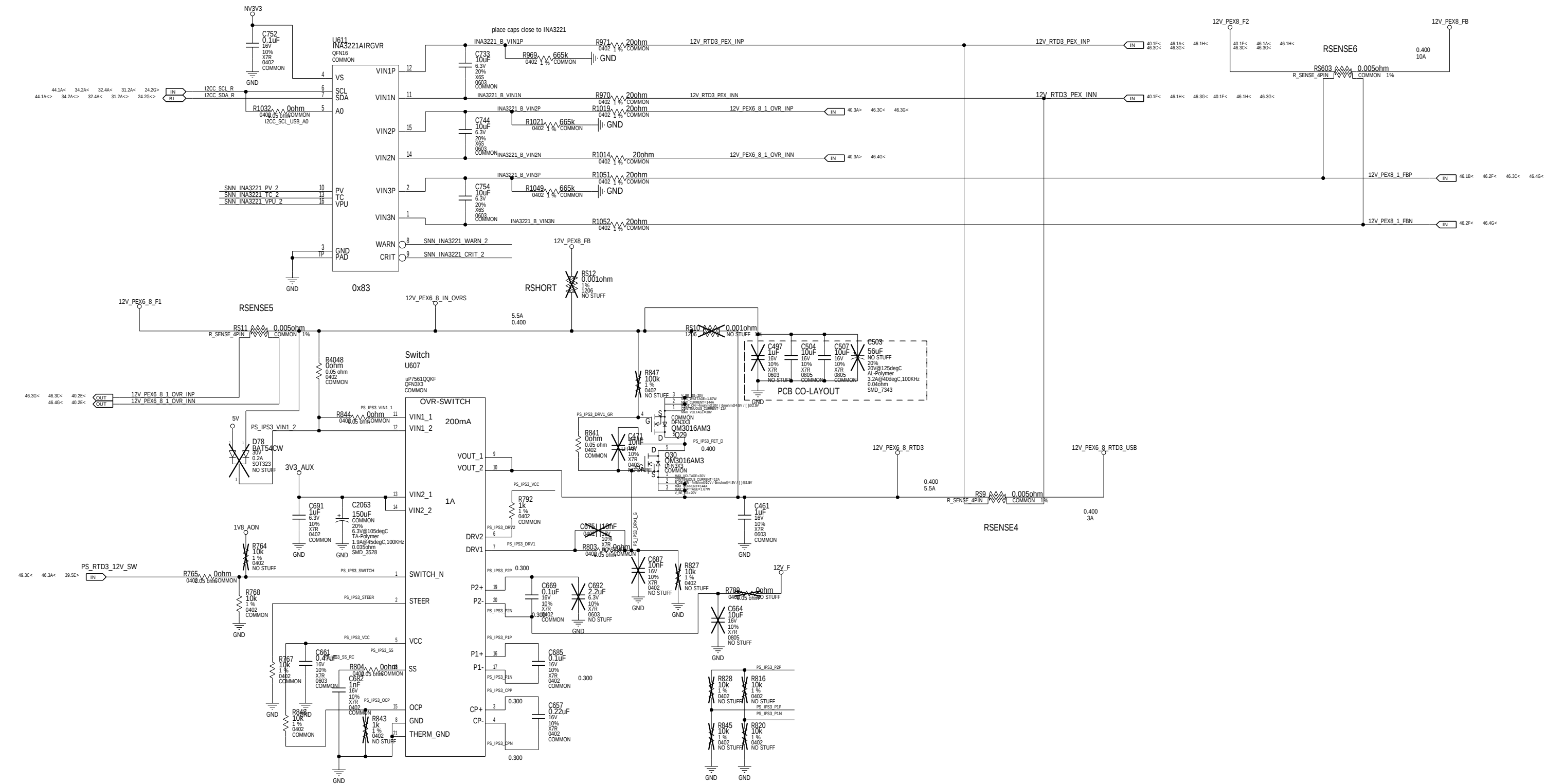


49.3C< 48.4A< 47.1A< 46.3A< 30.4A< 30.2A< 27.3C< 24.3C< IN

OUT 40.4A< 46.3A< 49.3C<

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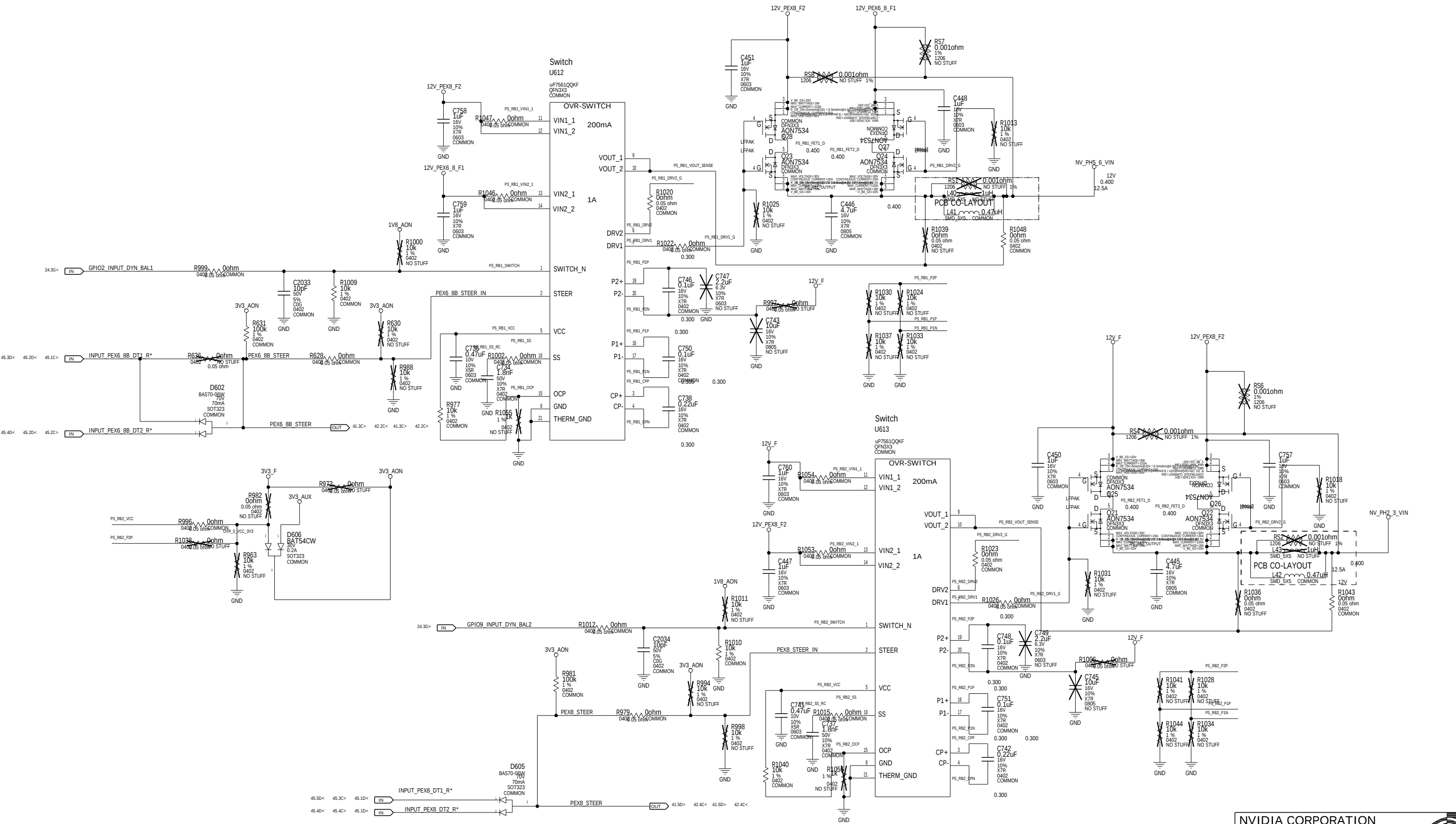
PAGE 40: PS: INPUT SWITCH RTD3 USB



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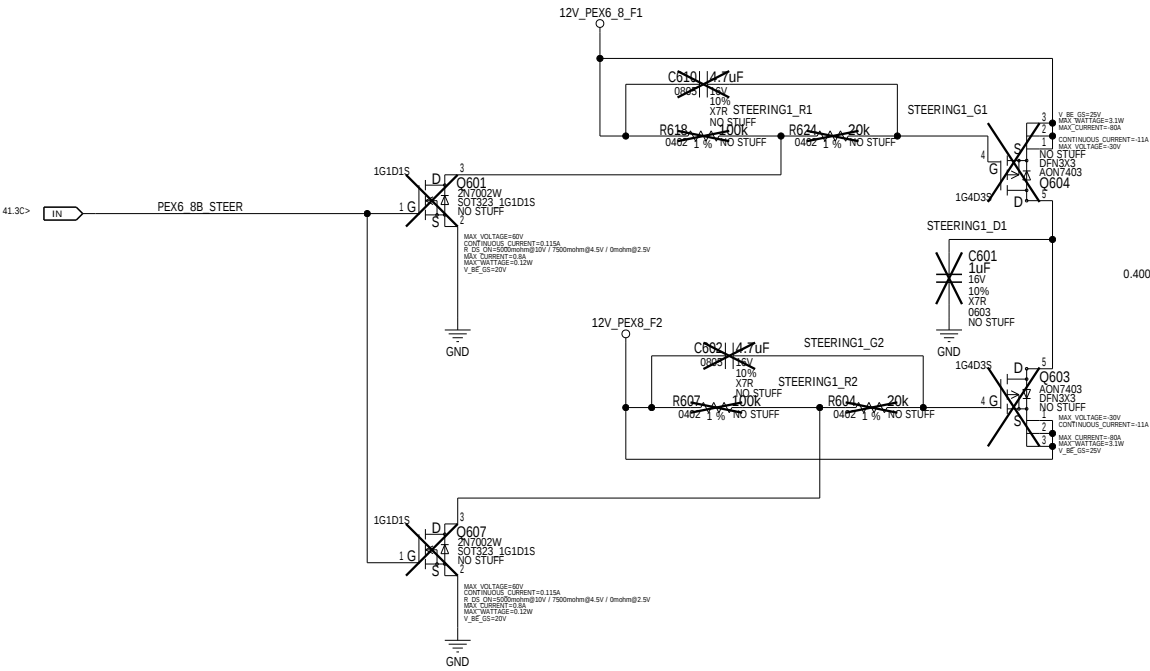
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PAGE 41: PS: INPUT SWITCH Rail Balance

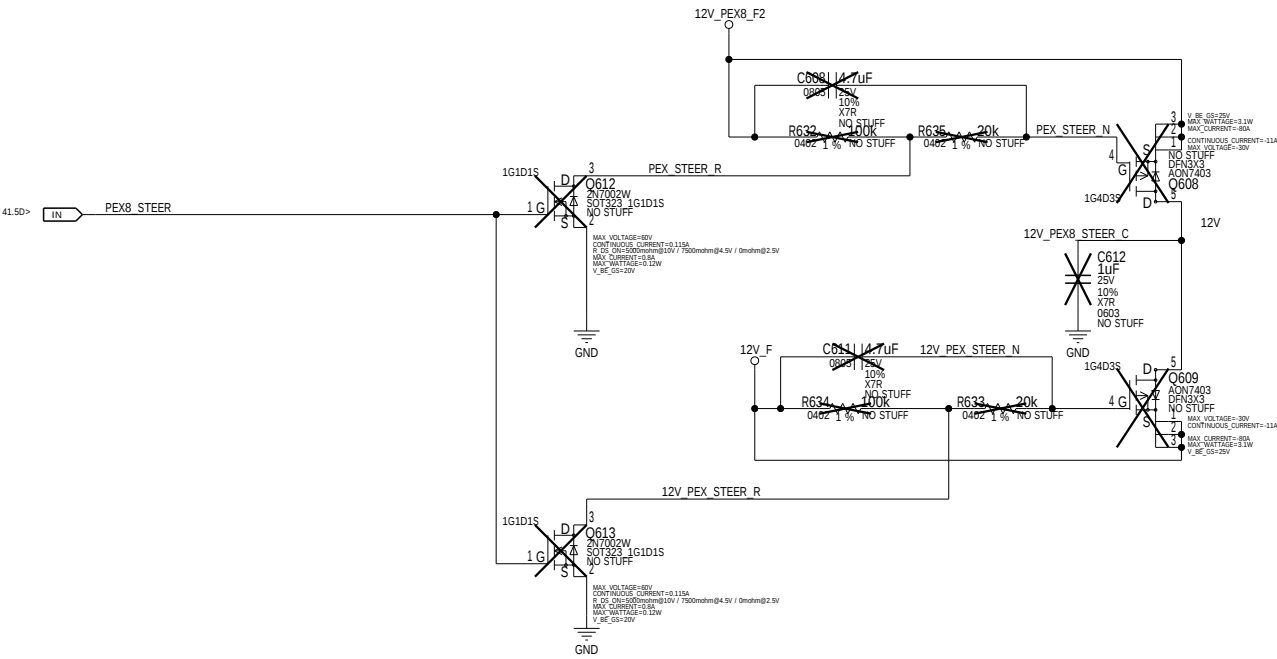


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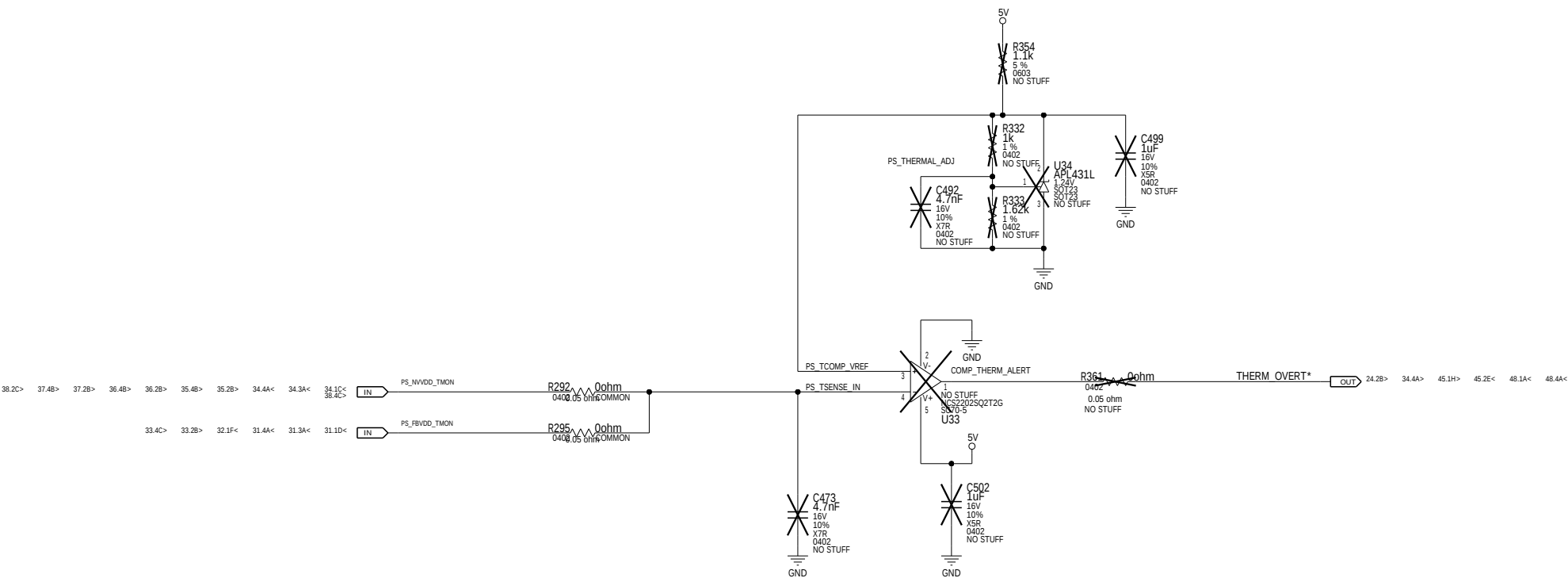
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

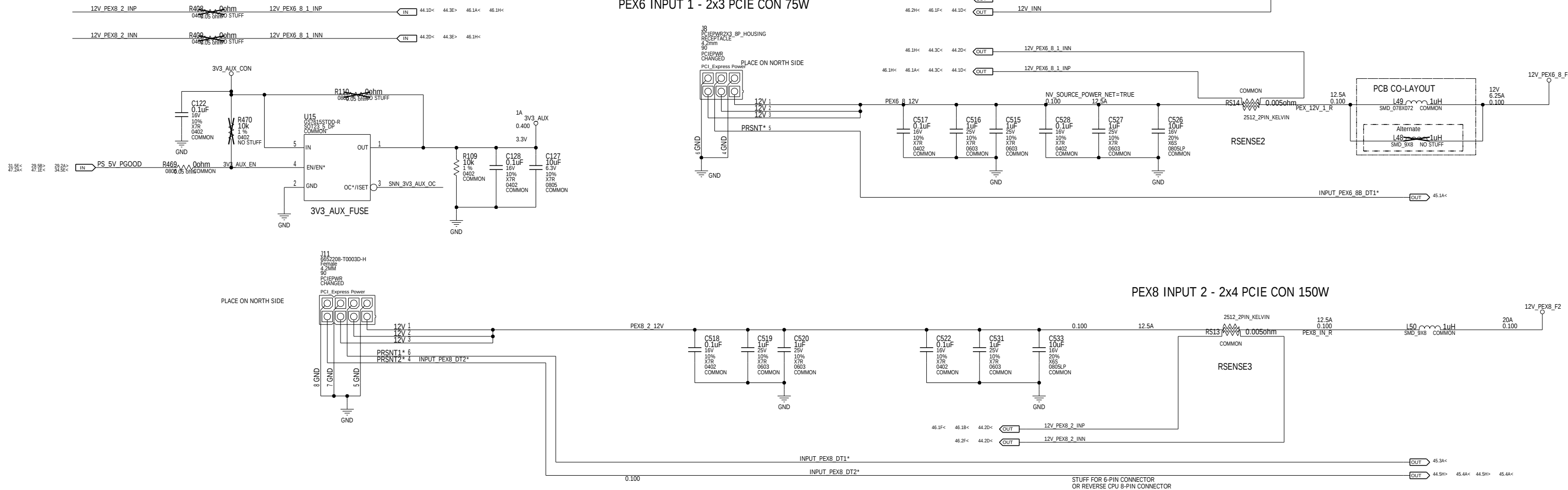
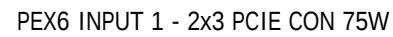
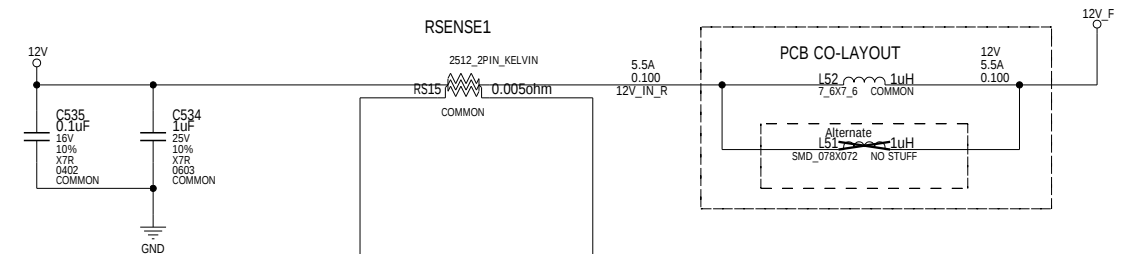
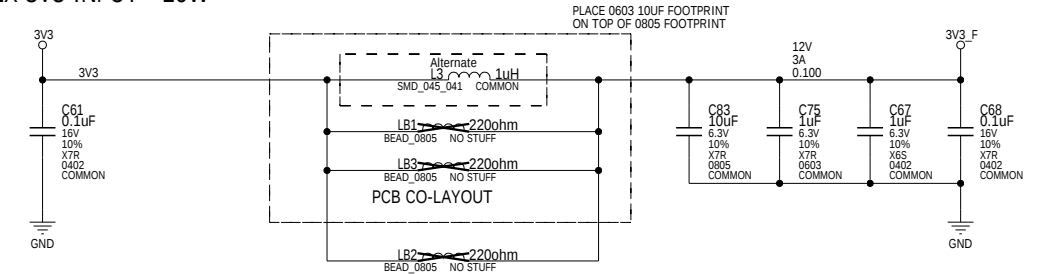
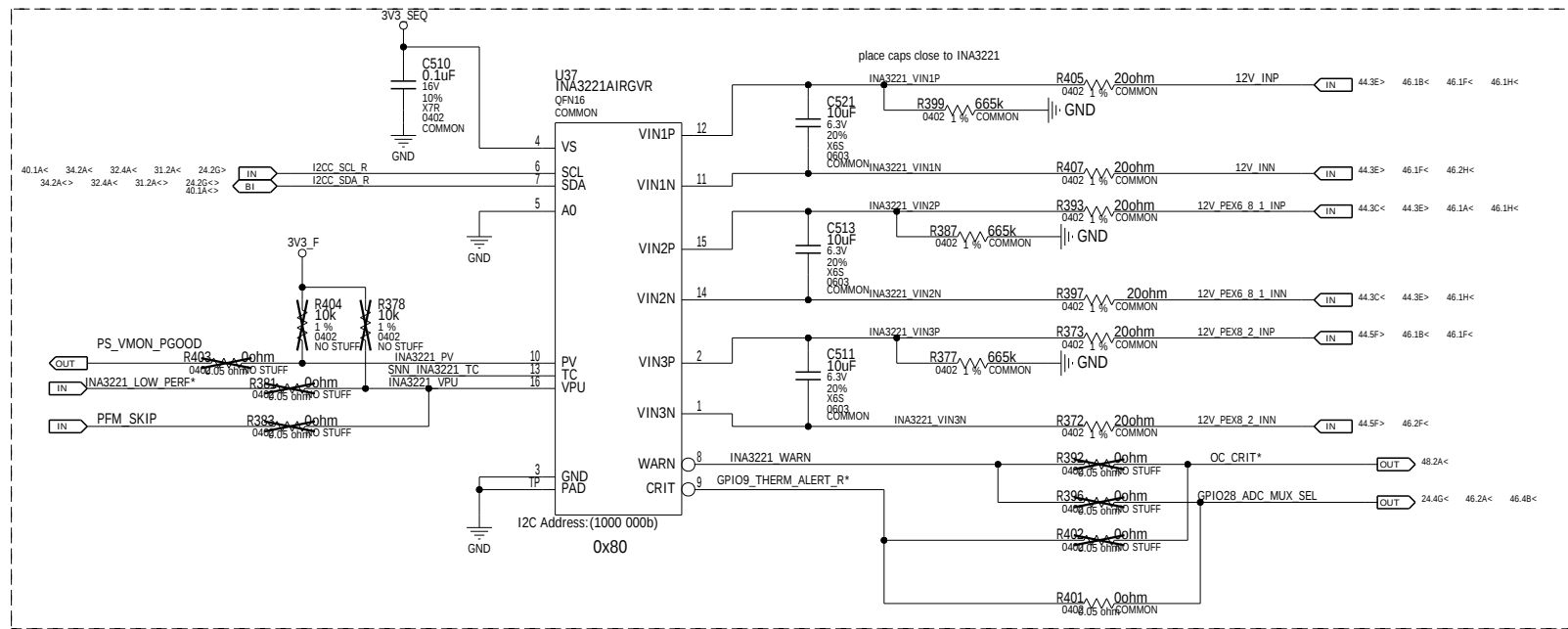


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PAGE 44: PS: Inputs, Filtering, and Monitoring



ASSEMBLY	SKU SCHEMATIC, COMMON & NO STUFF ASSEMBLY NOTES AND FINAL BOM
PAGE DETAIL	PS: INPUTS, FILTERING AND MONITORING

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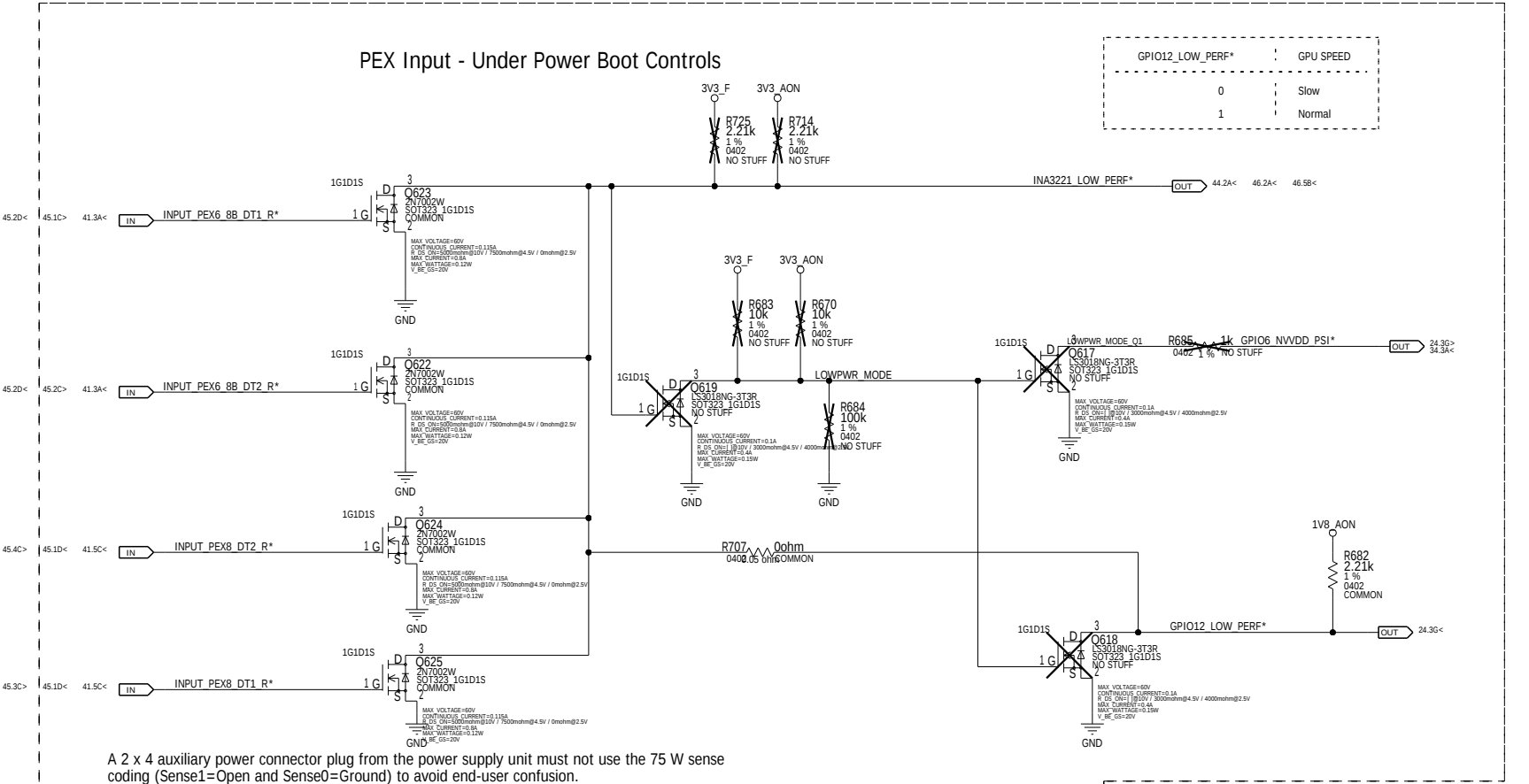
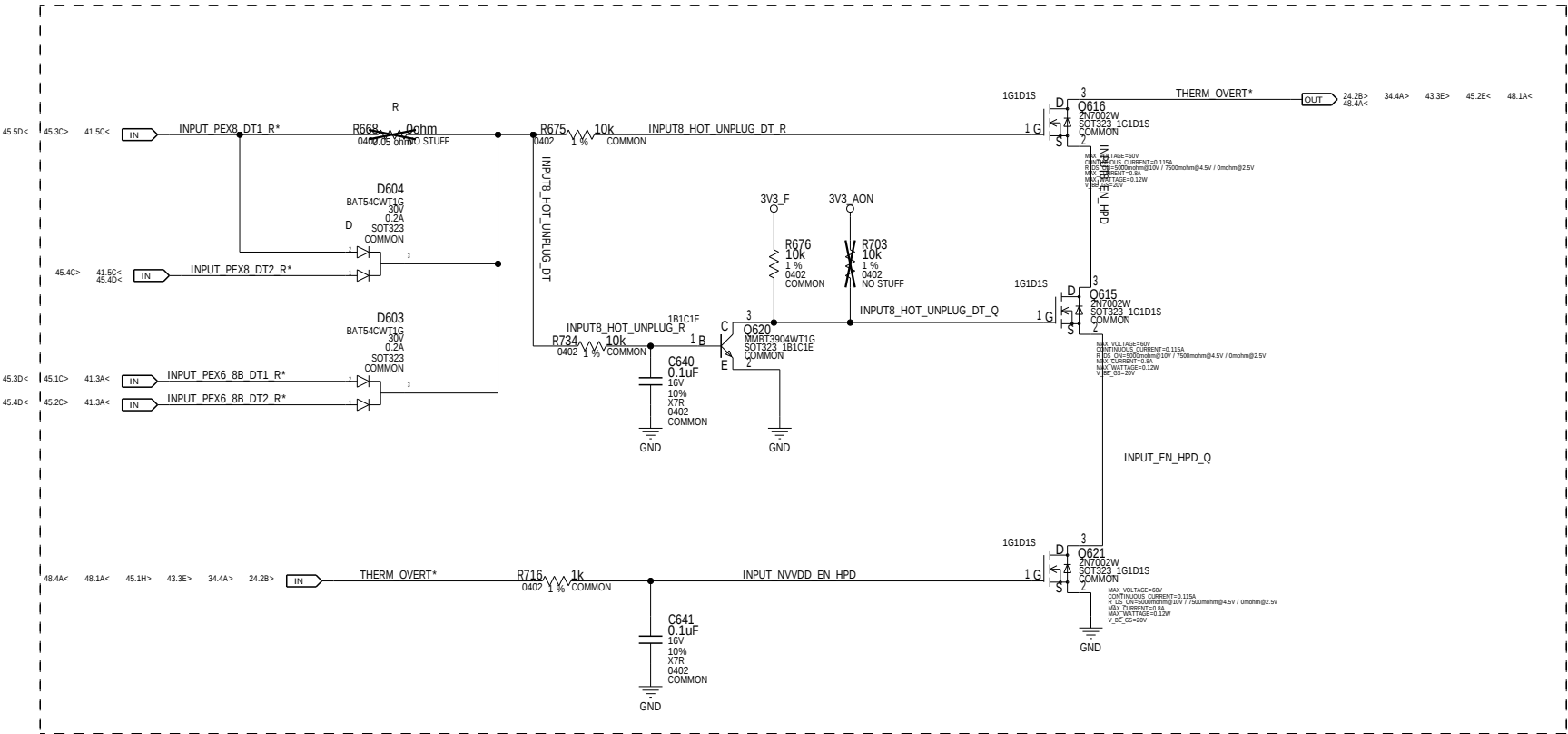
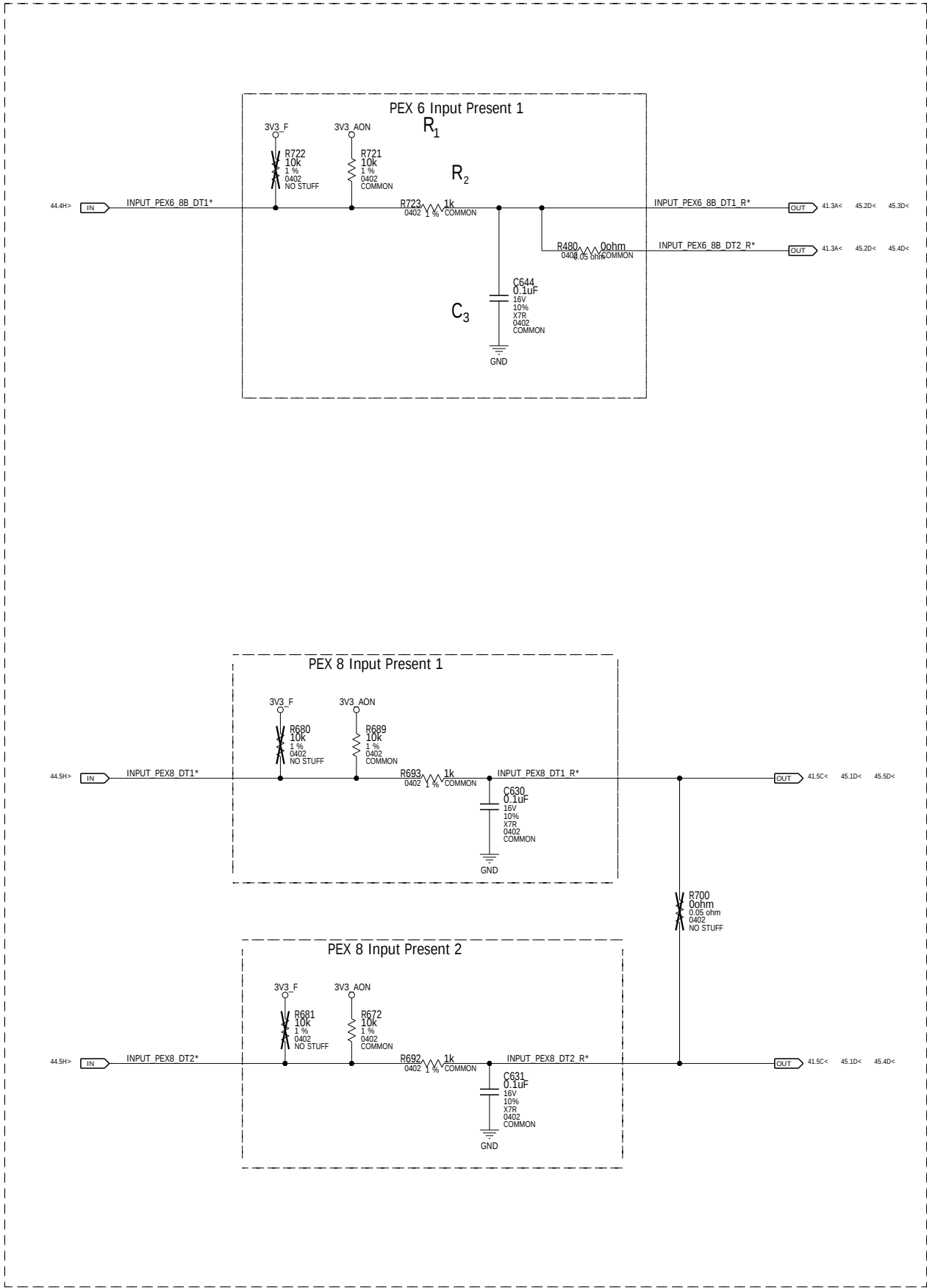
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PAGE 45: PS: Current Steering, Hot Unplug Detect



A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

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NV_PN 600-1G180-0002-300

PCB REV PG180-A02

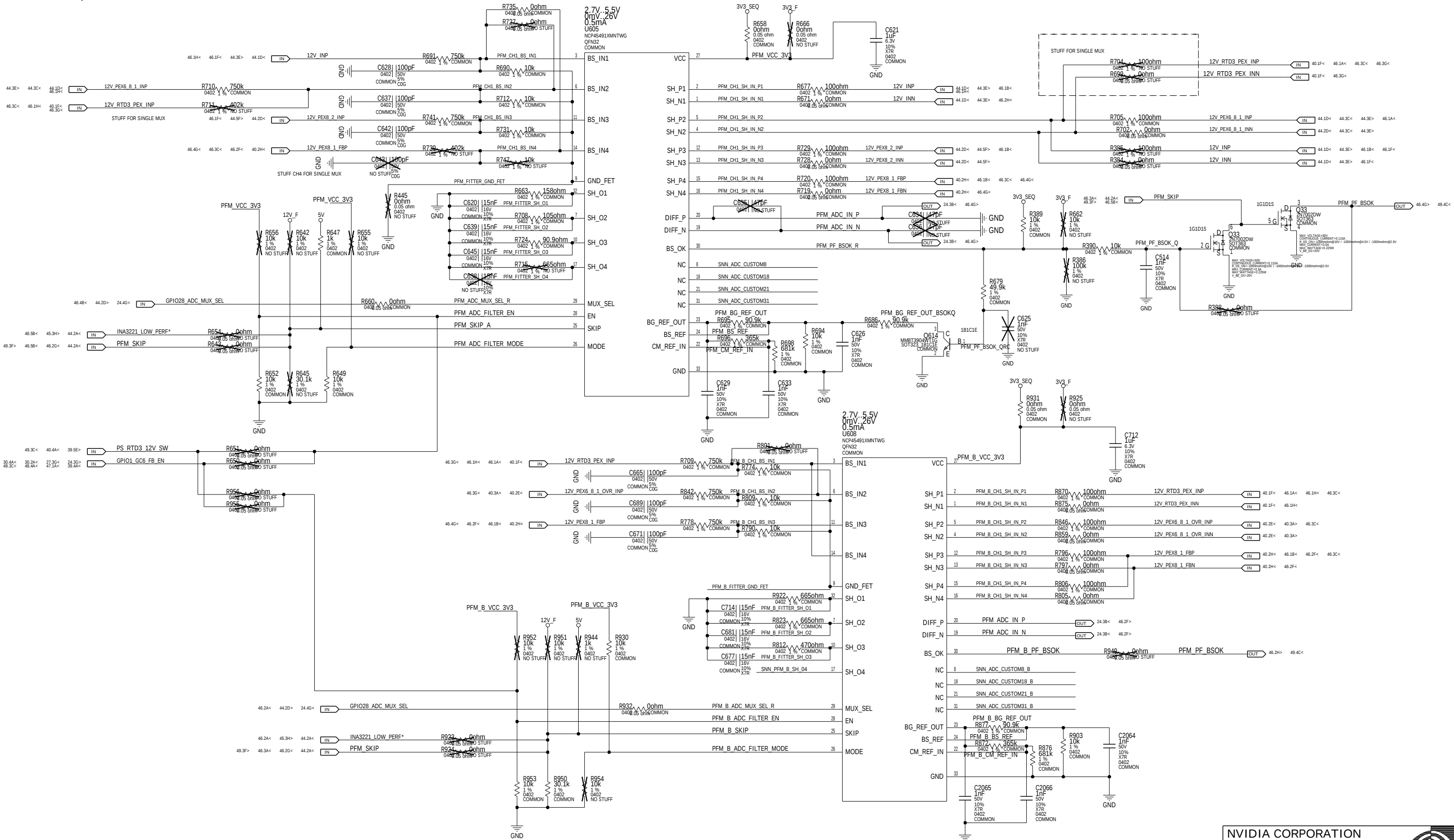
BOM REV B

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DATE 21-JUN-2018

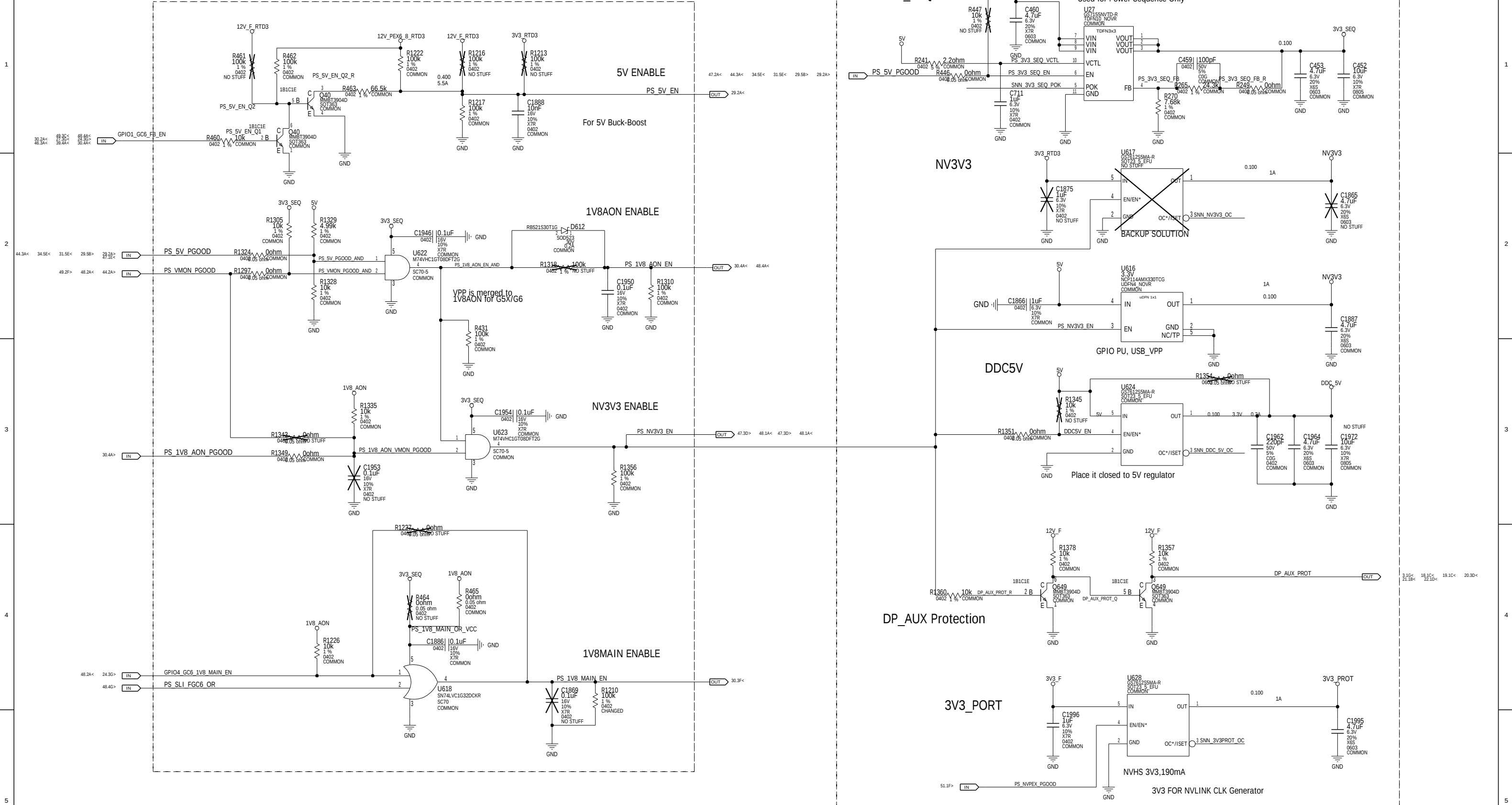
PAGE46; PS: Pre-Filter

STUFF IF USING 2XMUX



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PAGE 47: SEQUENCE:5V,1V8,NV3V3 ENABLE



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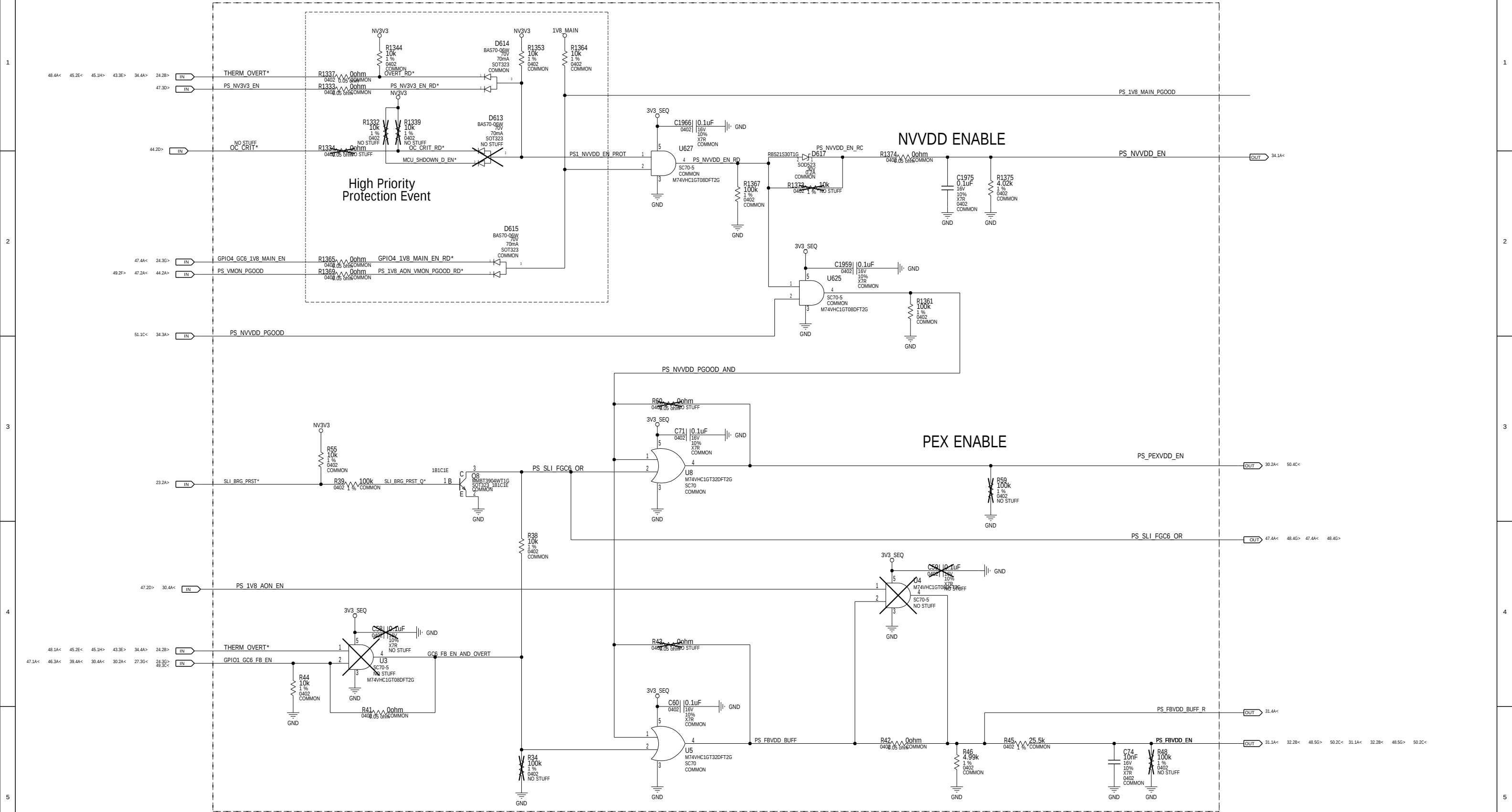
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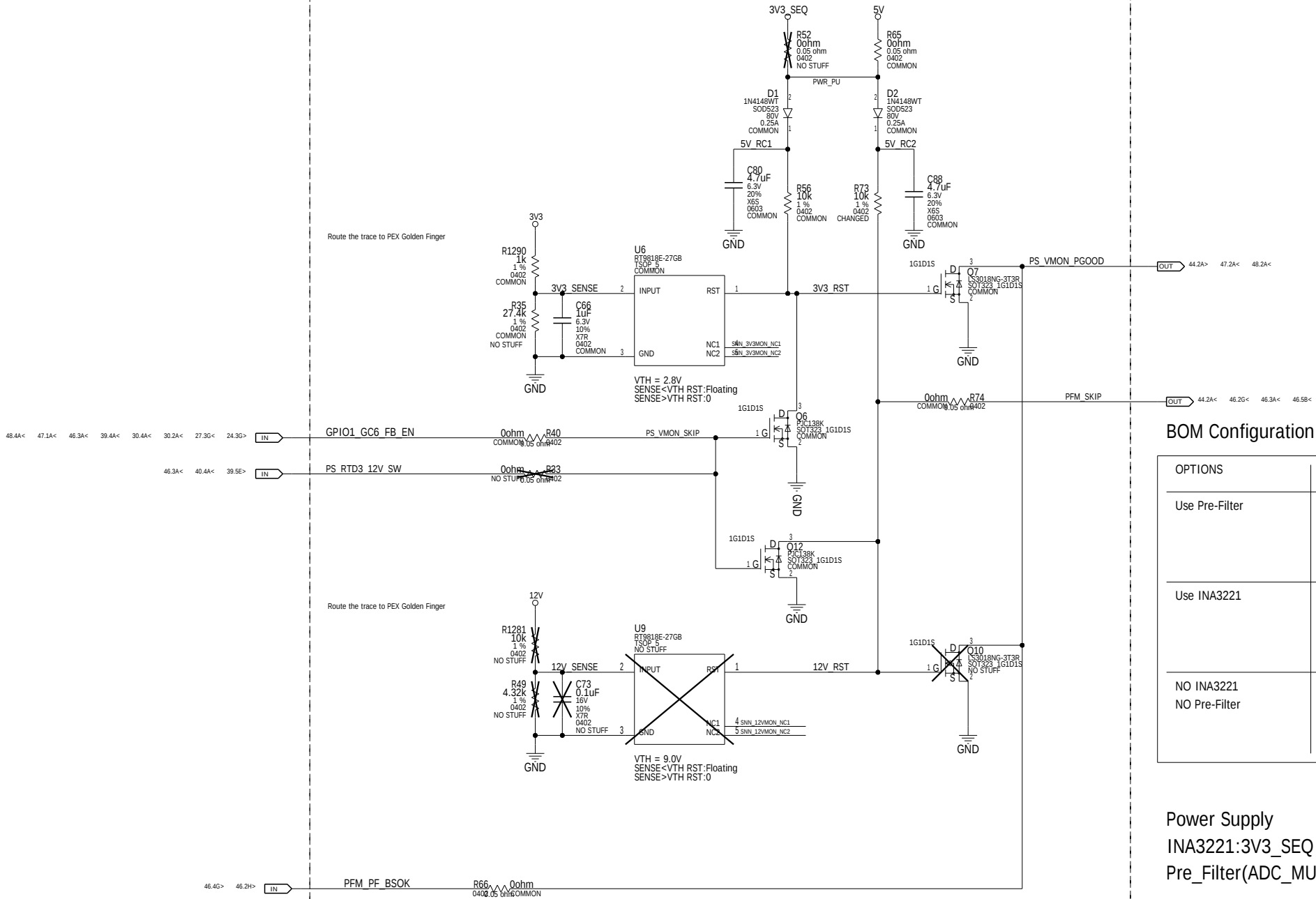
PCB REV	PG180-A02	PAGE	47 OF 54
BOM REV	B	DATE	21-JUN-2018

PAGE 48: SEQUENCE:NV,PEX,FB ENABLE



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PCIE Voltage Monitor



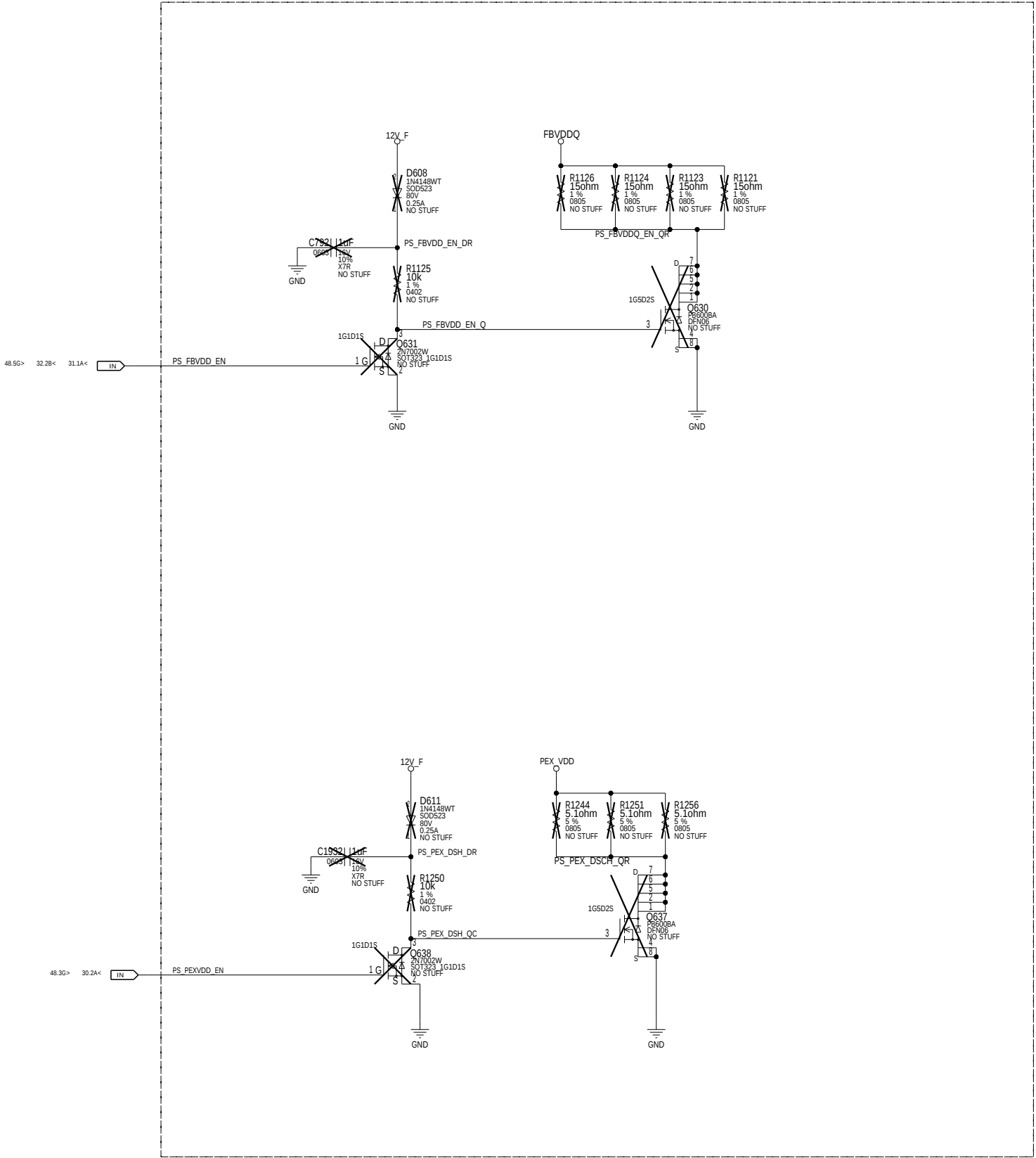
Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

BOM Configuration

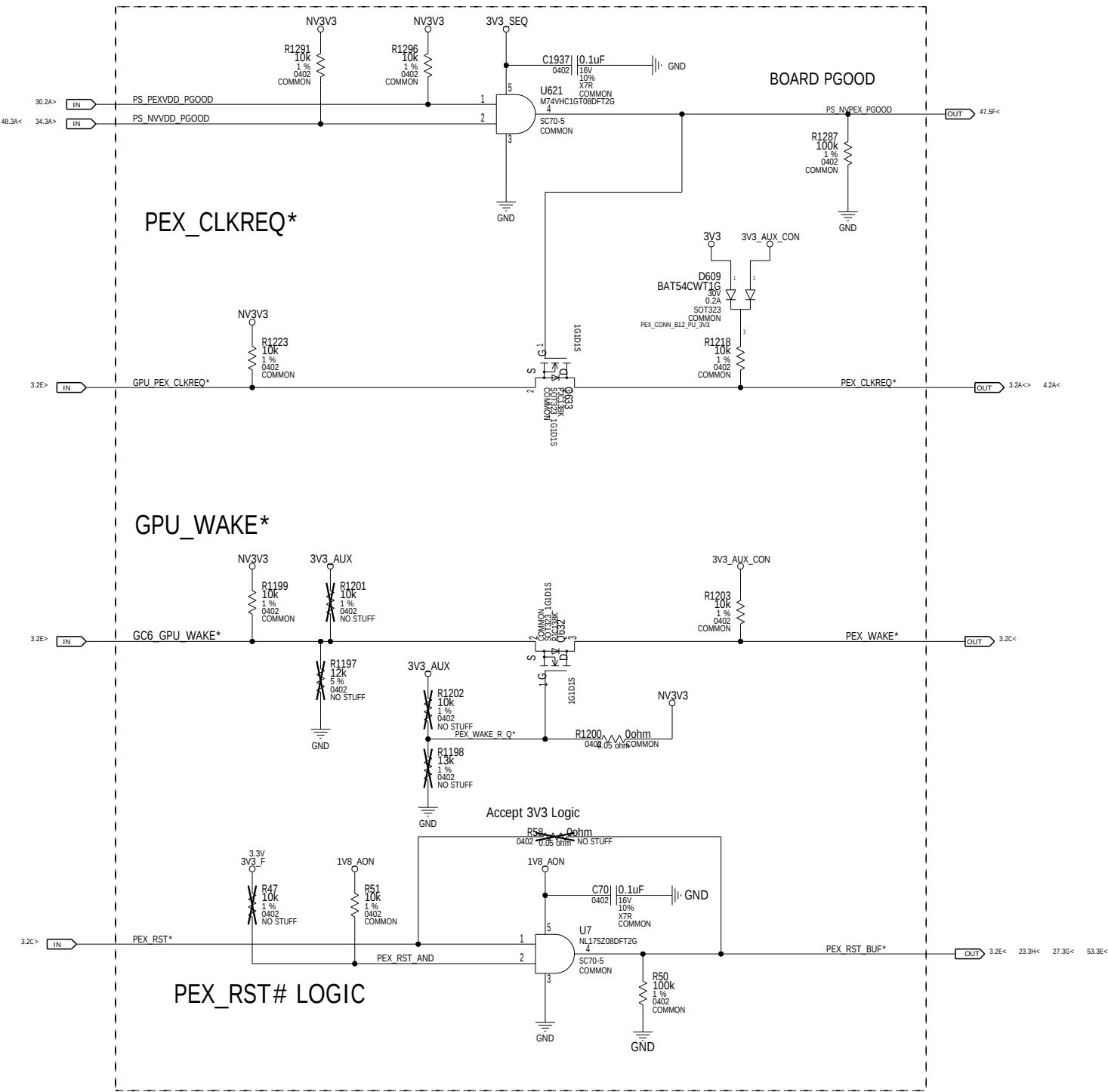
OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply
INA3221:3V3_SEQ
Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:
Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs

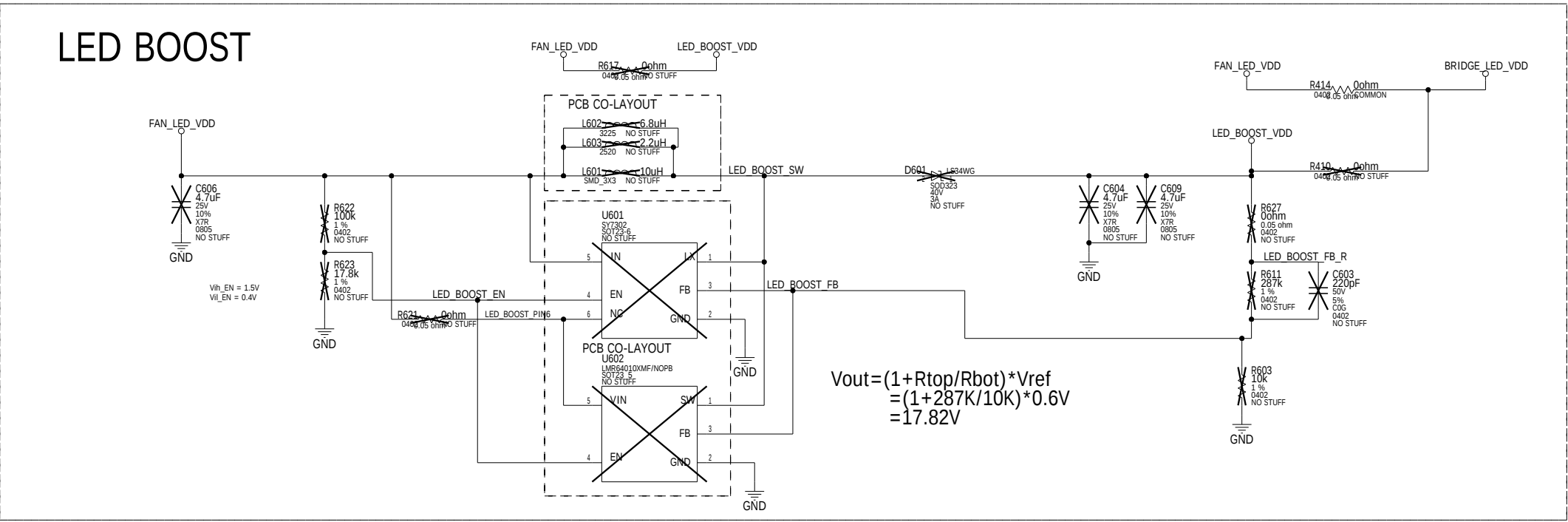
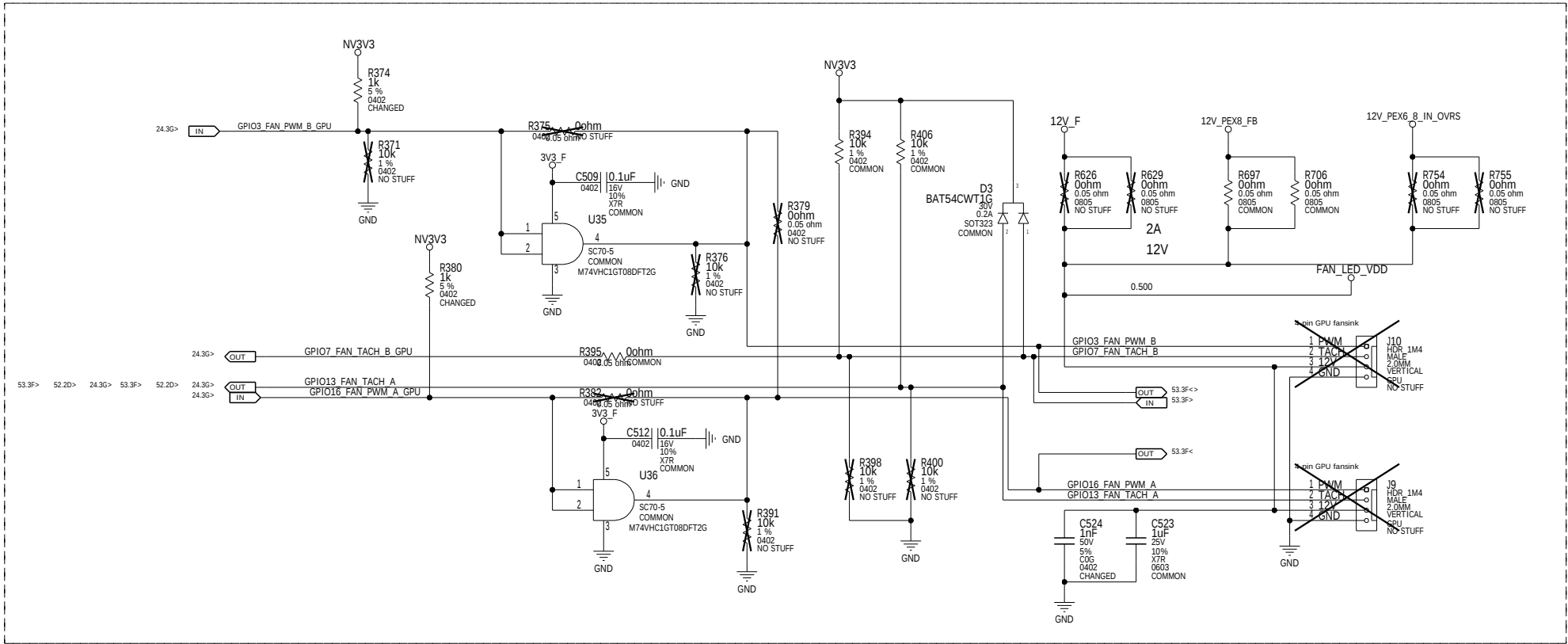
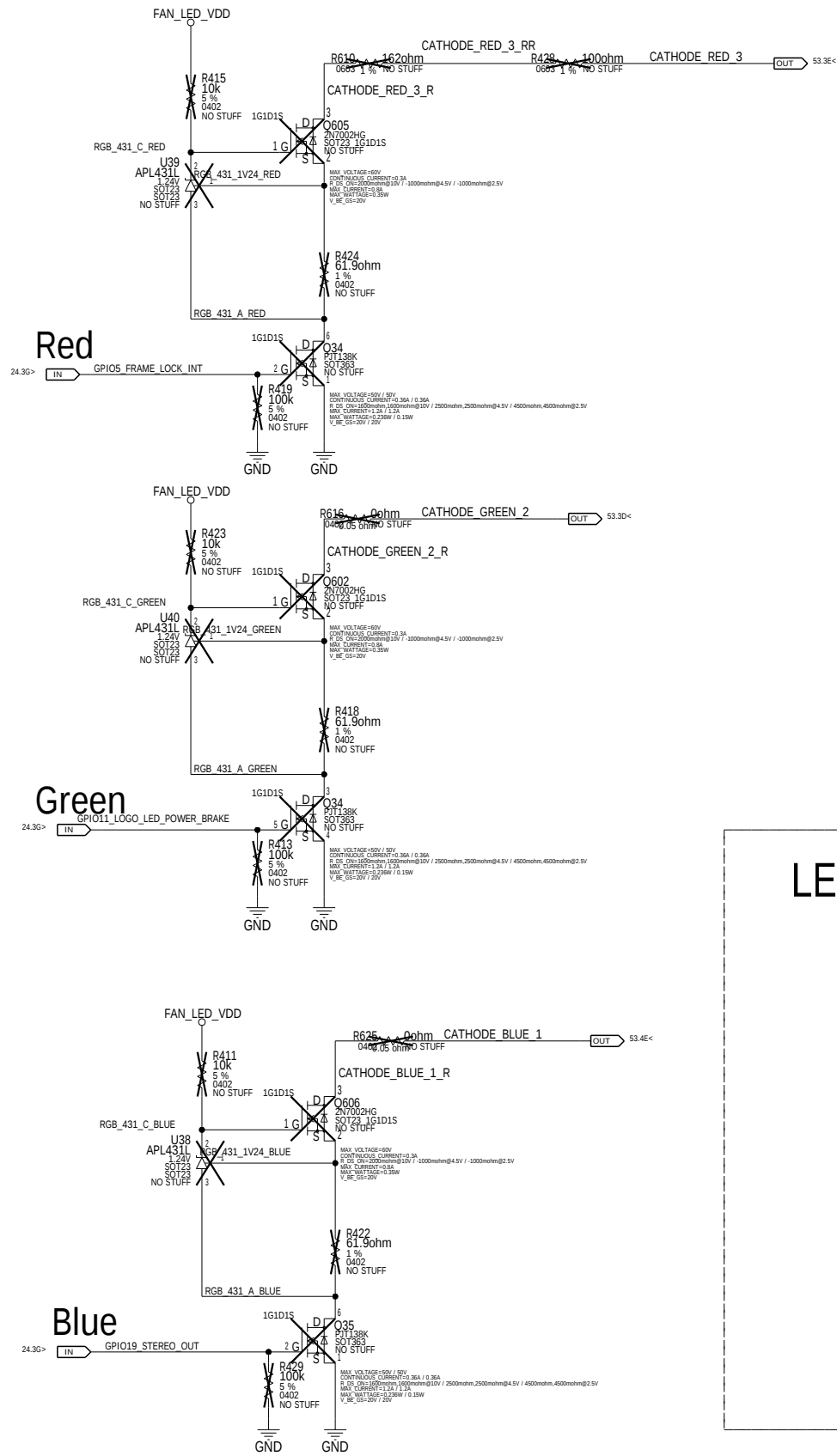


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PAGE 52: LED & FAN HEADERS



$$V_{out} = (1 + R_{top}/R_{bot}) * V_{ref}$$
$$= (1 + 287K/10K) * 0.6V$$
$$= 17.82V$$

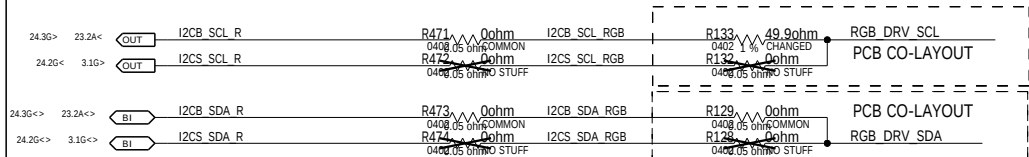
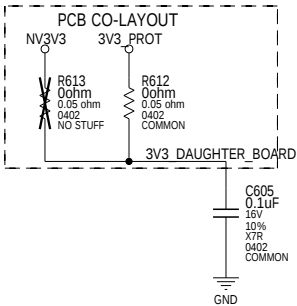
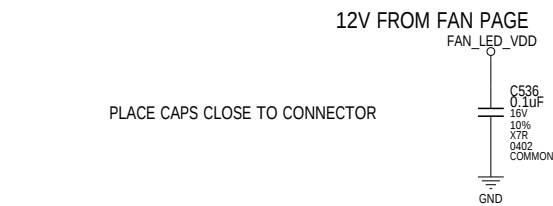
1

2

3

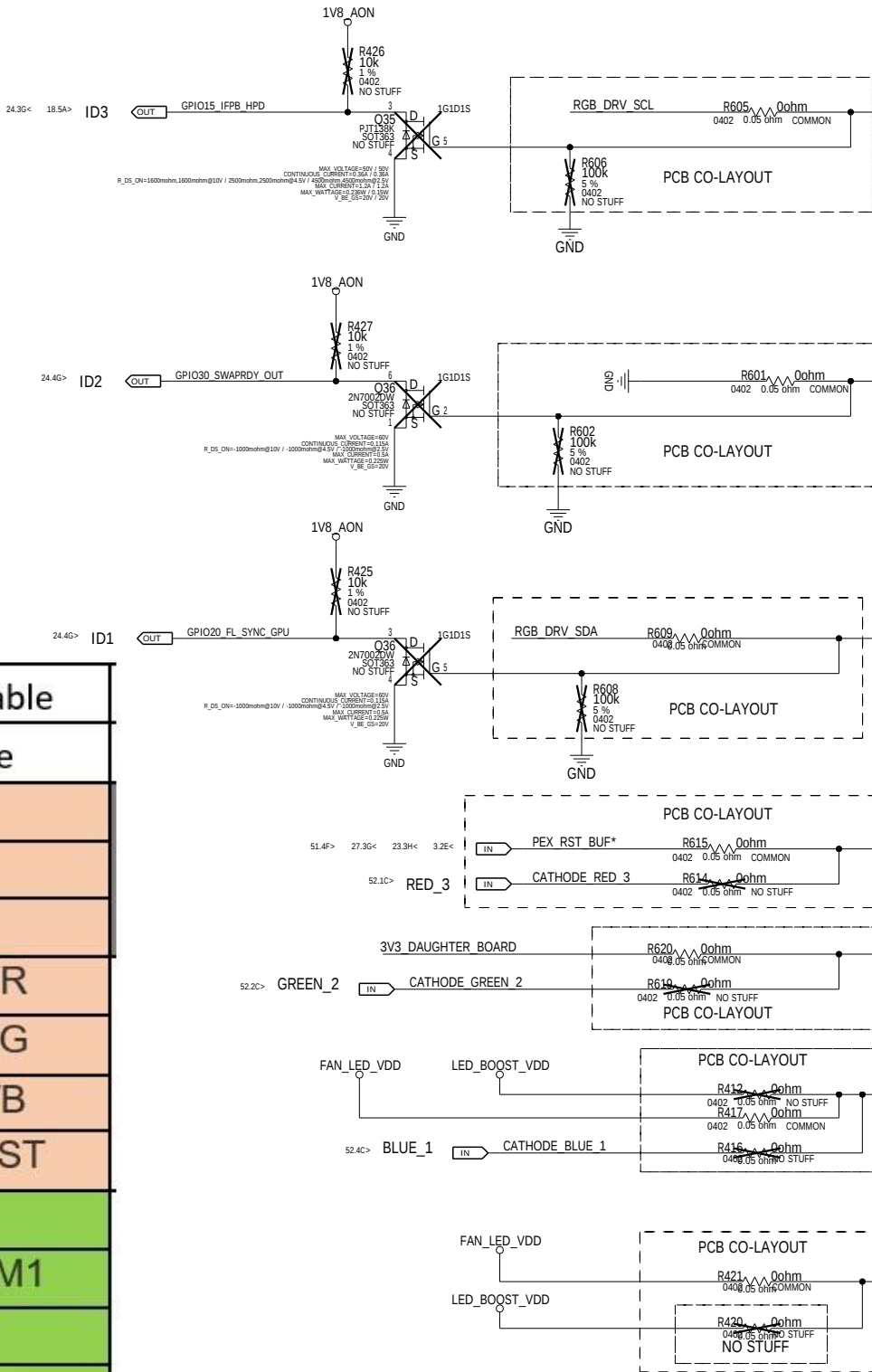
4

5



8-bit I2C Address of MCU on Daughter Board: TBD

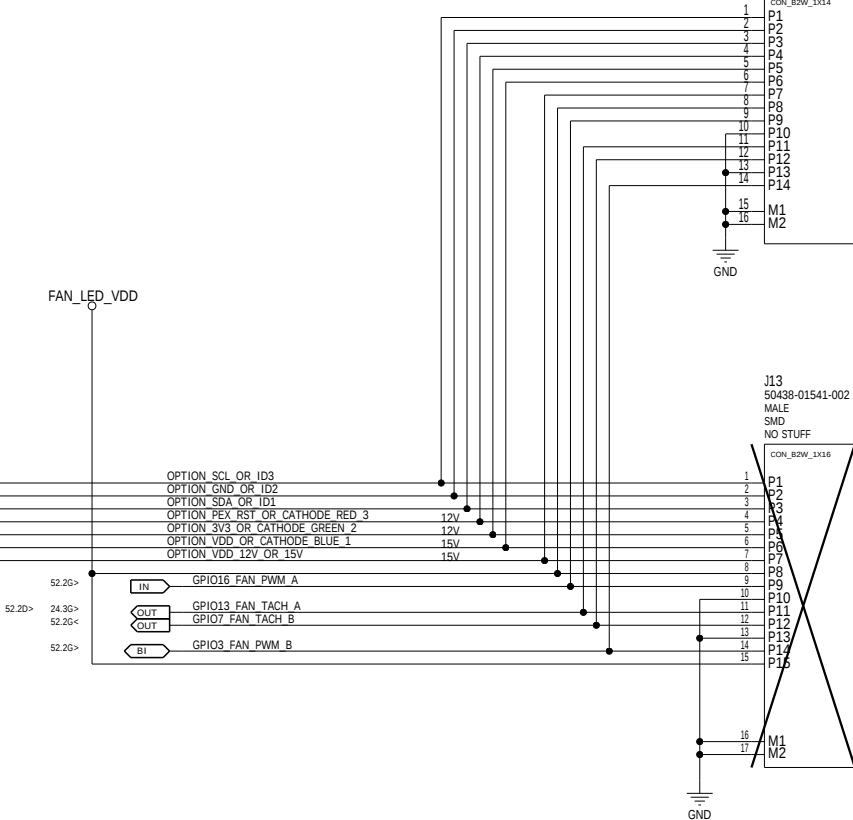
MCU Solution		For ONE ZONE RGB/cable	
PIN SEQ	Pin Name	PIN SEQ	Pin Name
1	I2C_SCL	1	ID3
2	GND	2	ID2
3	I2C_SDA	3	ID1
4	PEX_RST_BUF*	4	DRIVE3/R
5	NV3V3	5	DRIVE2/G
6	12V/BOOST	6	DRIVE1/B
7	12V	7	12V/BOOST
8	12V	8	12V
9	FAN_PWM1	9	FAN_PWM1
10	GND	10	GND
11	FAN_TACH1	11	FAN_TACH1
12	FAN_TACH2	12	FAN_TACH2
13	GND	13	GND
14	FAN_PWM2	14	FAN_PWM2
		15	12V



14-PIN STRAIGHT PRIMARY SOURCE -> 080-1586-000: ACES \$0.115

14-PIN STRAIGHT SECOND SOURCE -> 080-1600-000: WIESON \$0.2

FOR MCU SOLUTION



FOR ONE ZONE RGB SOLUTION

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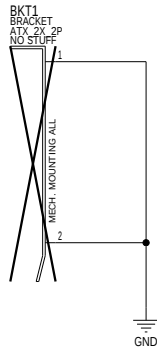
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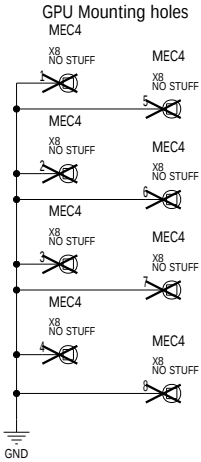
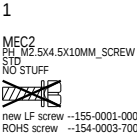
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Brackets:



Bracket Screw



STIFFENER

