PG180-A02

256b GDDR6 x16
TALL DP + DP + DP + HDMI/DP + USB

TABLE OF CONTENTS

base on V372-02S change for D18 Z
1. P.23 remove SLI & BRIDGE_LED_VDD & SLI_BRG_PRST*
2. P.52 remove LED change FAN connector
3. P.53 remove LED
4. P.38&44 add FUSE
5. P.5~14 mem add < >
6. P.53 LED use V336-0D
7. P.32 remove
8. P.35~38 dual MOS
9. P.33 change dual MOS
10. P.43 remove
11. P.31 change to UP1666
12. P.21 remove colay DP

2019/06/17
1.add NV link

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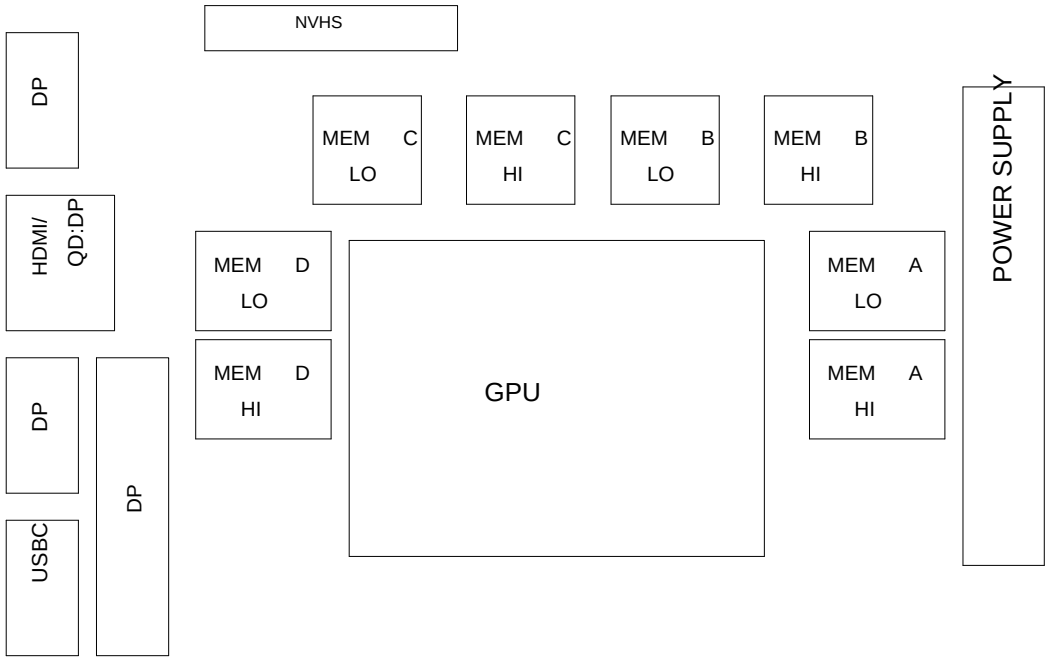
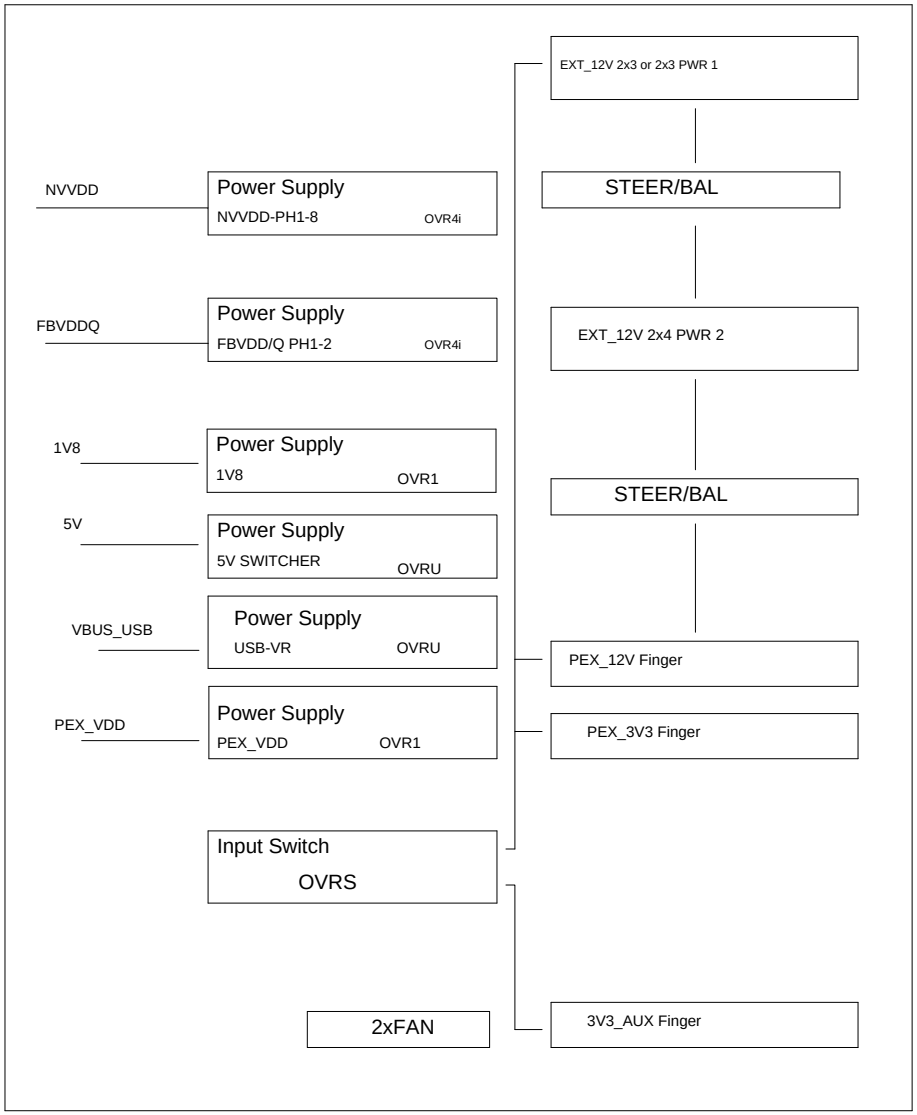
Page2: Block Diagram





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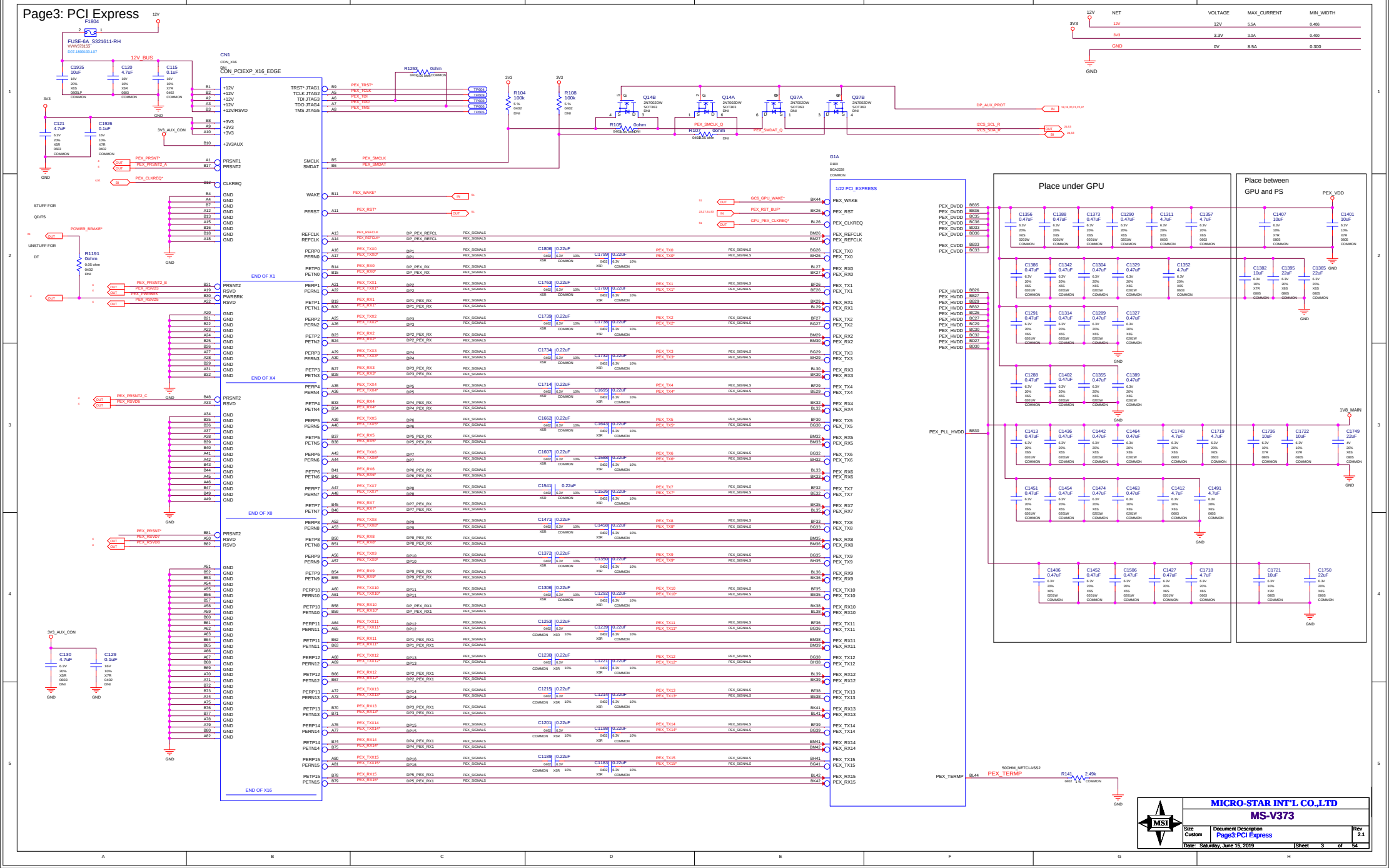
Page3: PCI Express



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	0.406
3V3	3.3V	3.0A	0.400
GND	0V	8.5A	0.300

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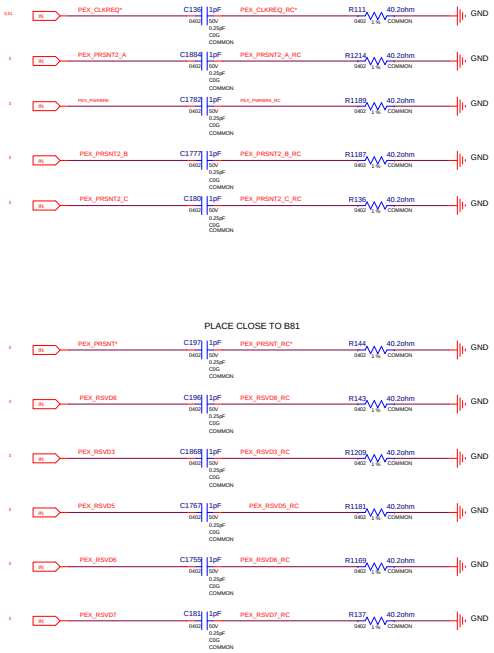
Page4: PCI Termination



PLACE CLOSE TO B81

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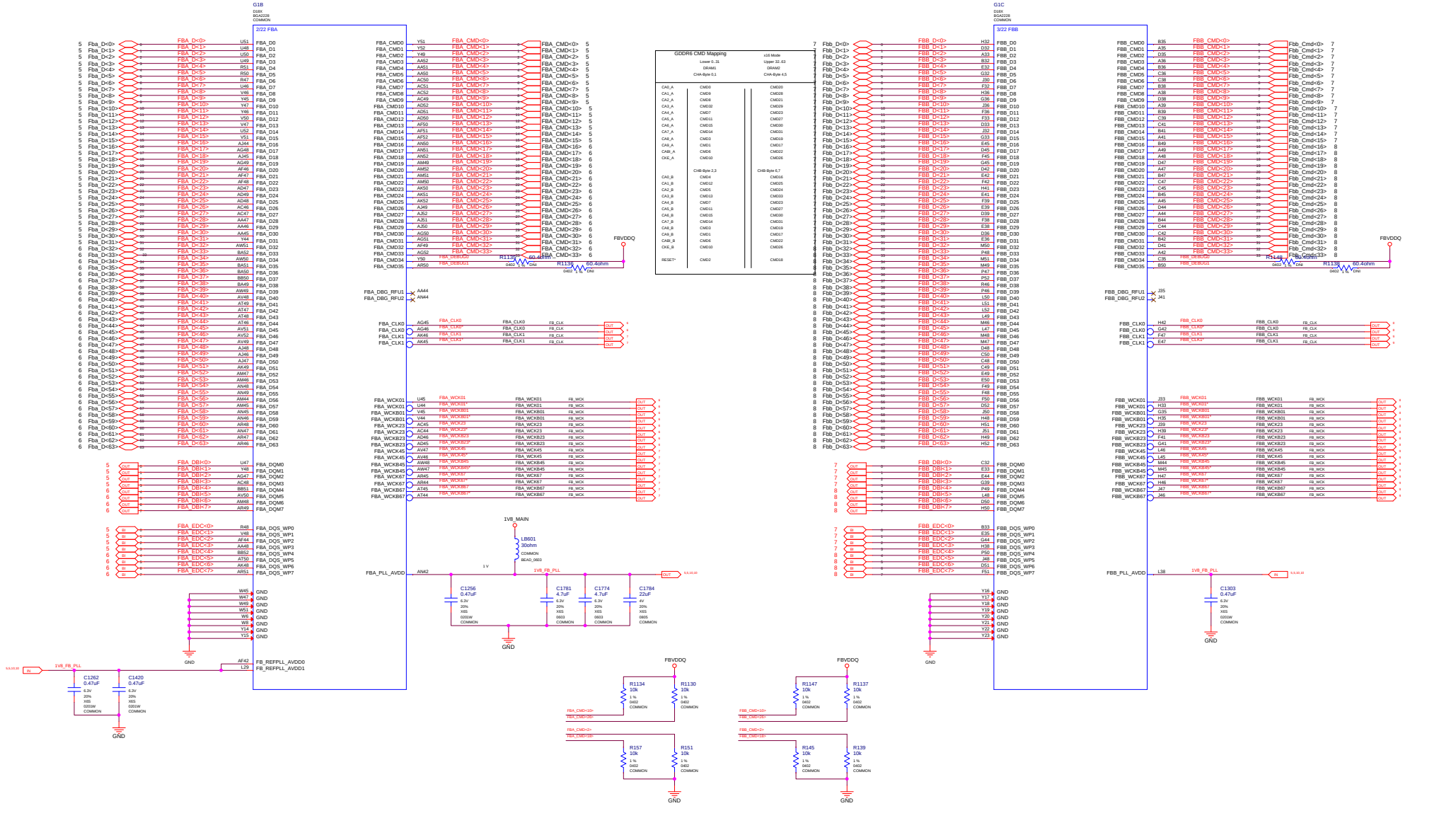
Page5: MEMORY: GPU Partition A/B



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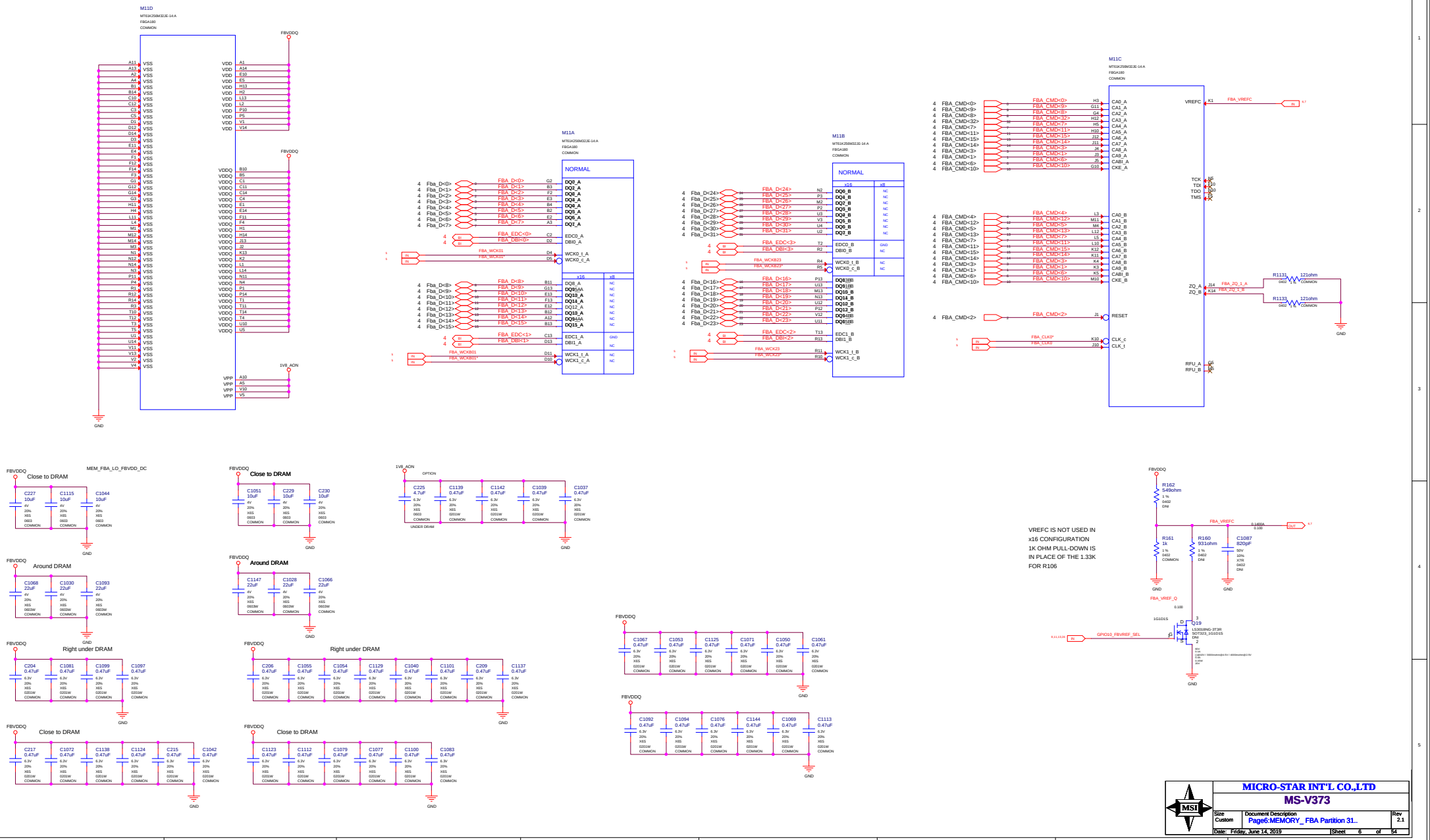
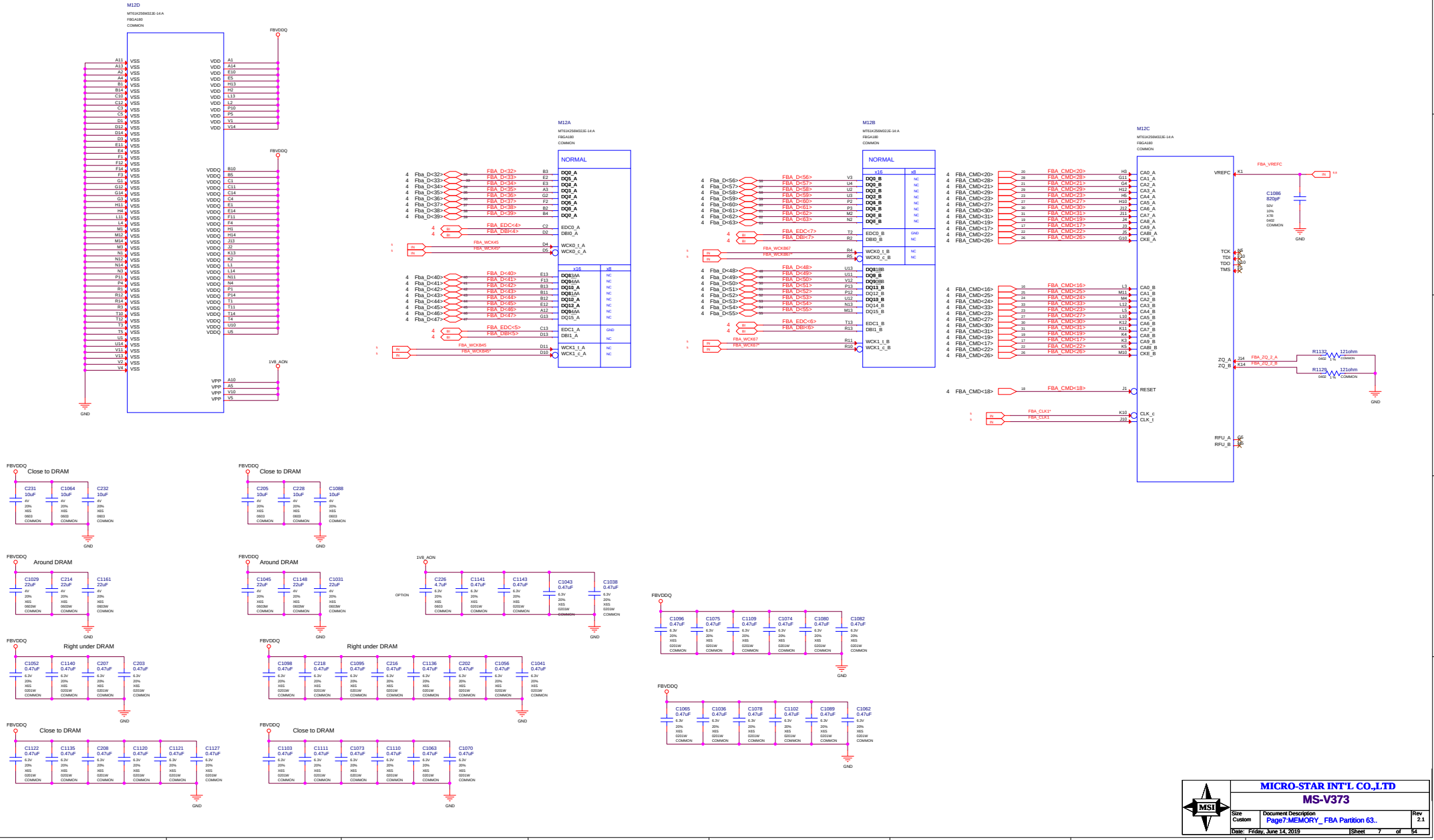
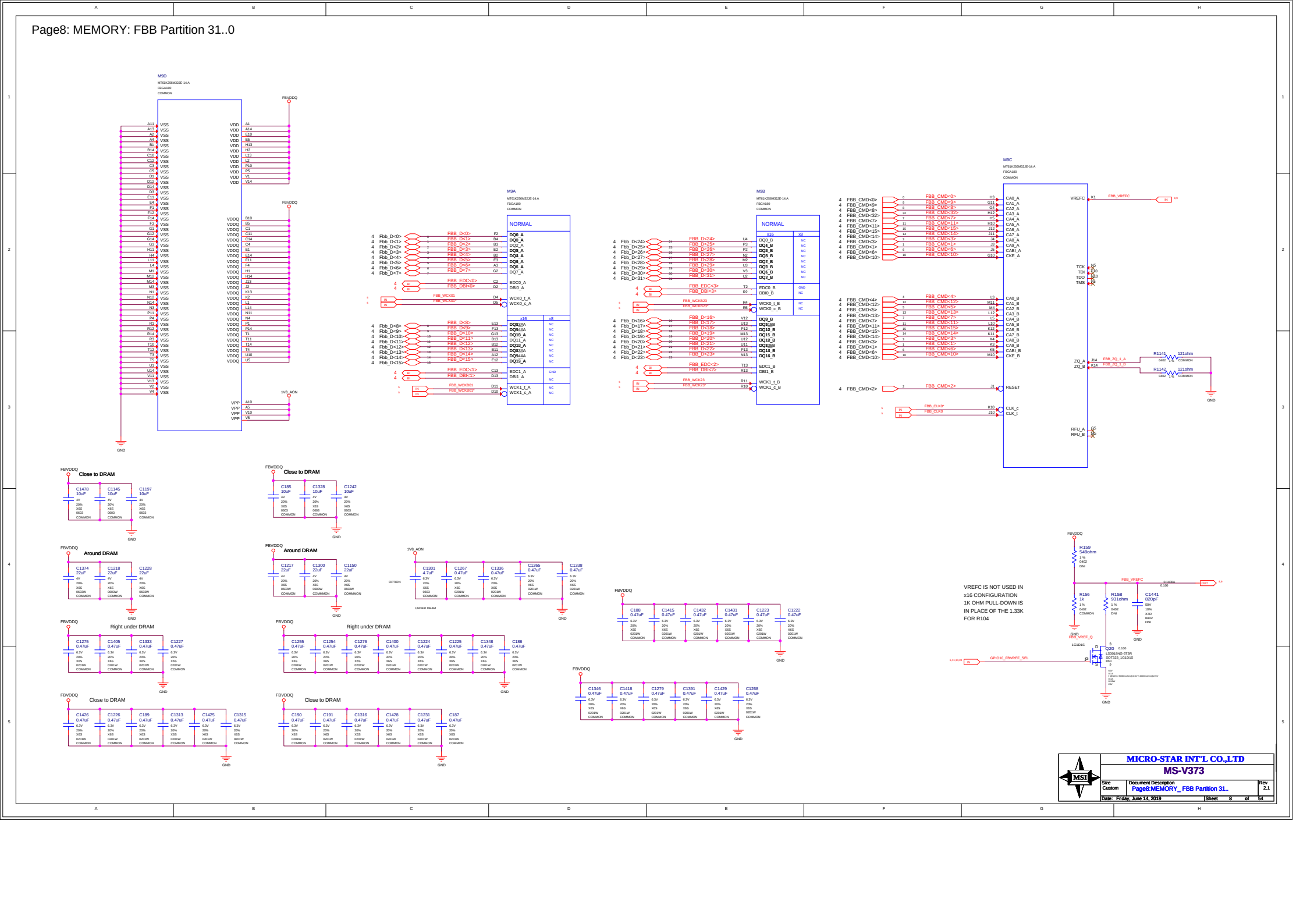
Page6: MEMORY: FBA Partition 31..0



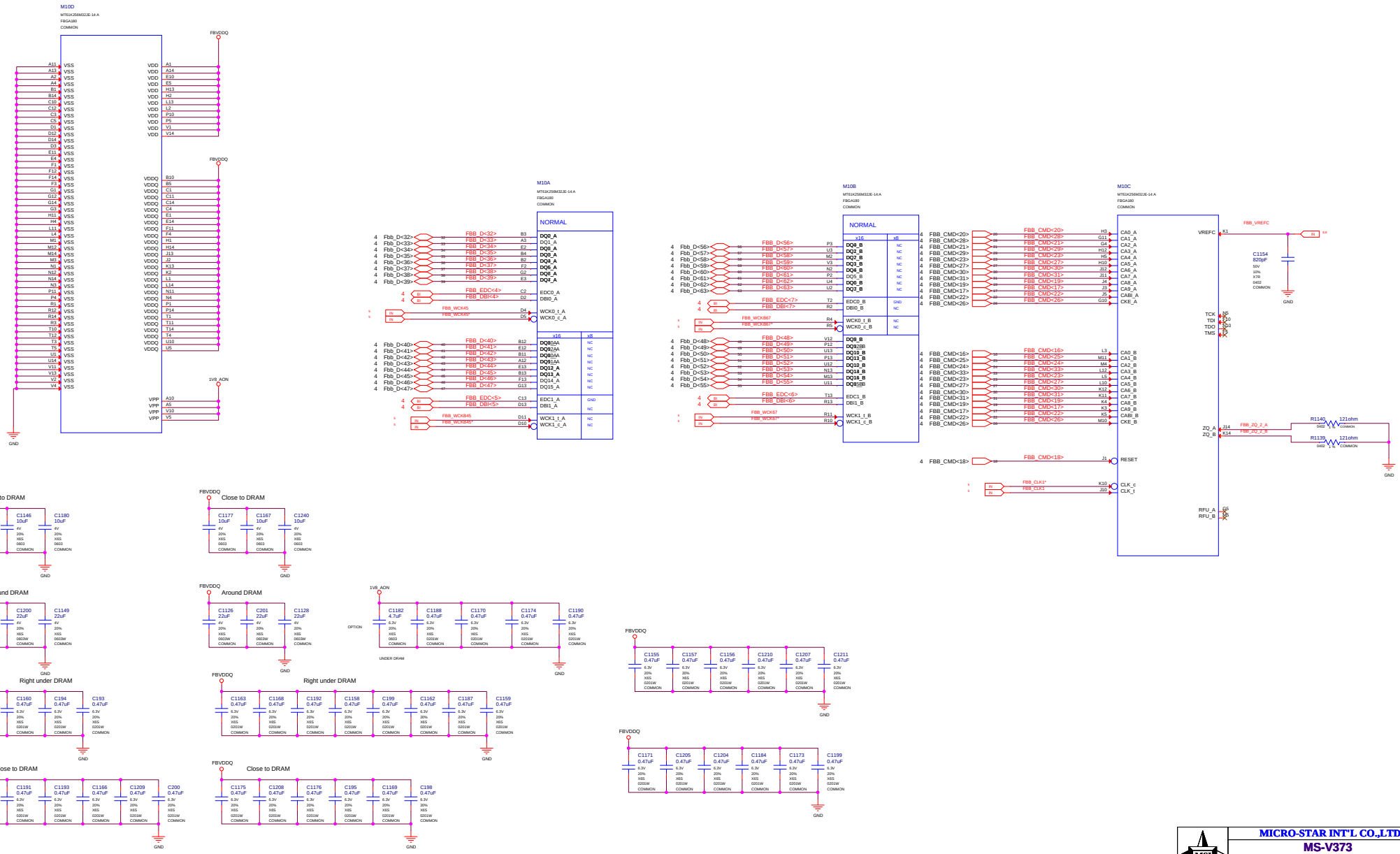
Page7: MEMORY: FBA Partition 63..32



Page8: MEMORY: FBB Partition 31..0



Page9: MEMORY: FBB Partition 63..32



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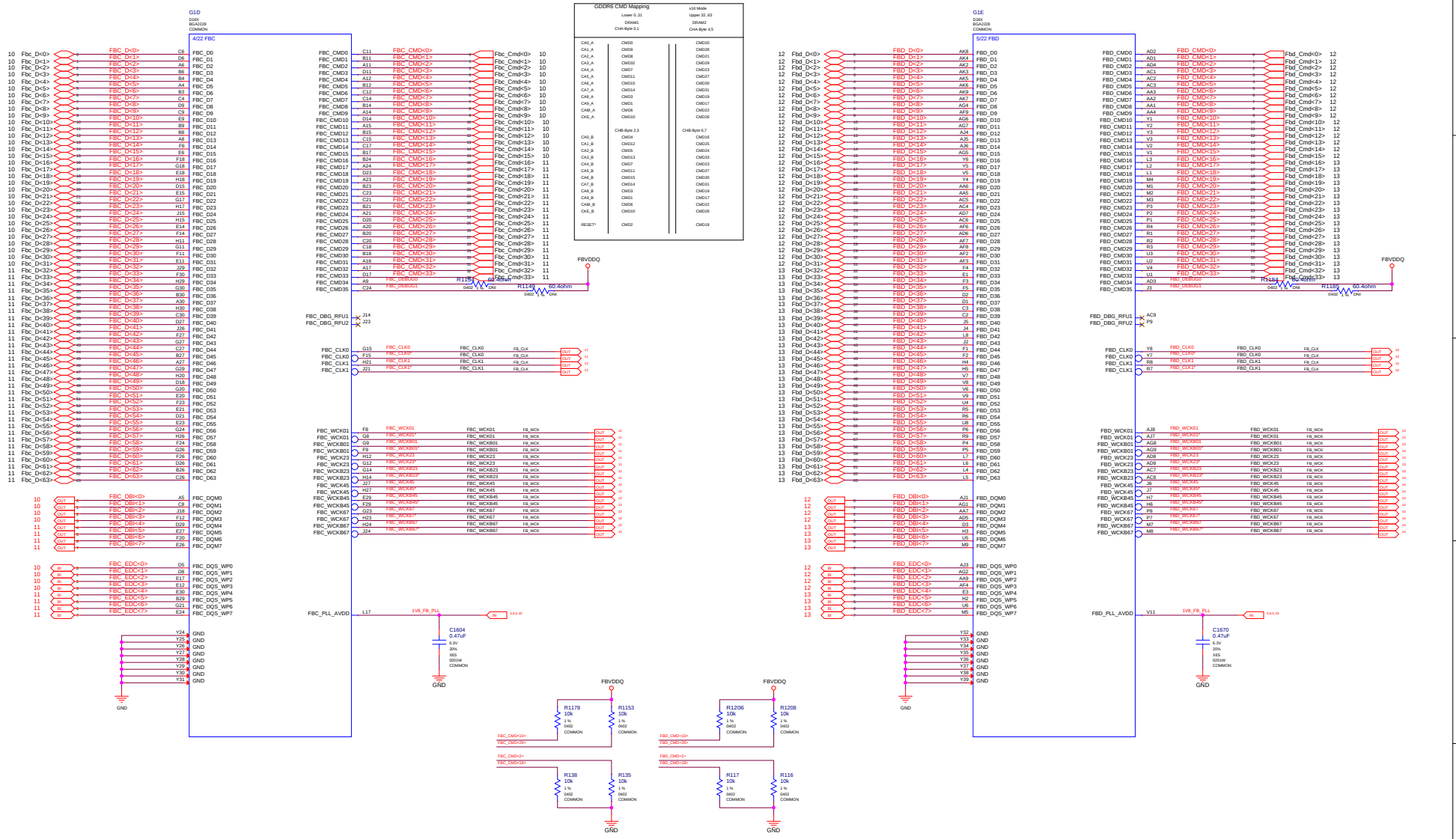
Page10: MEMORY: GPU Partition C/D



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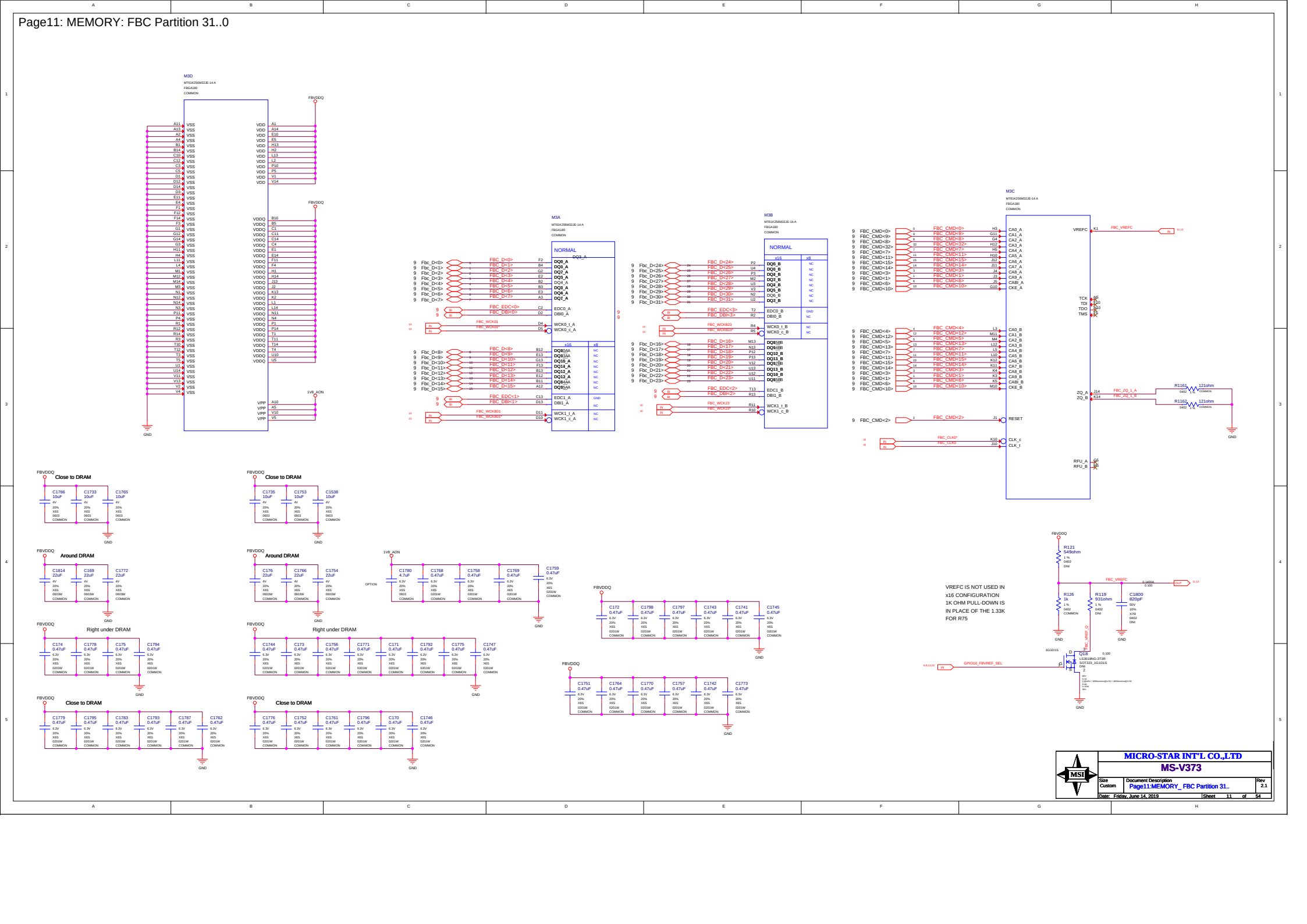
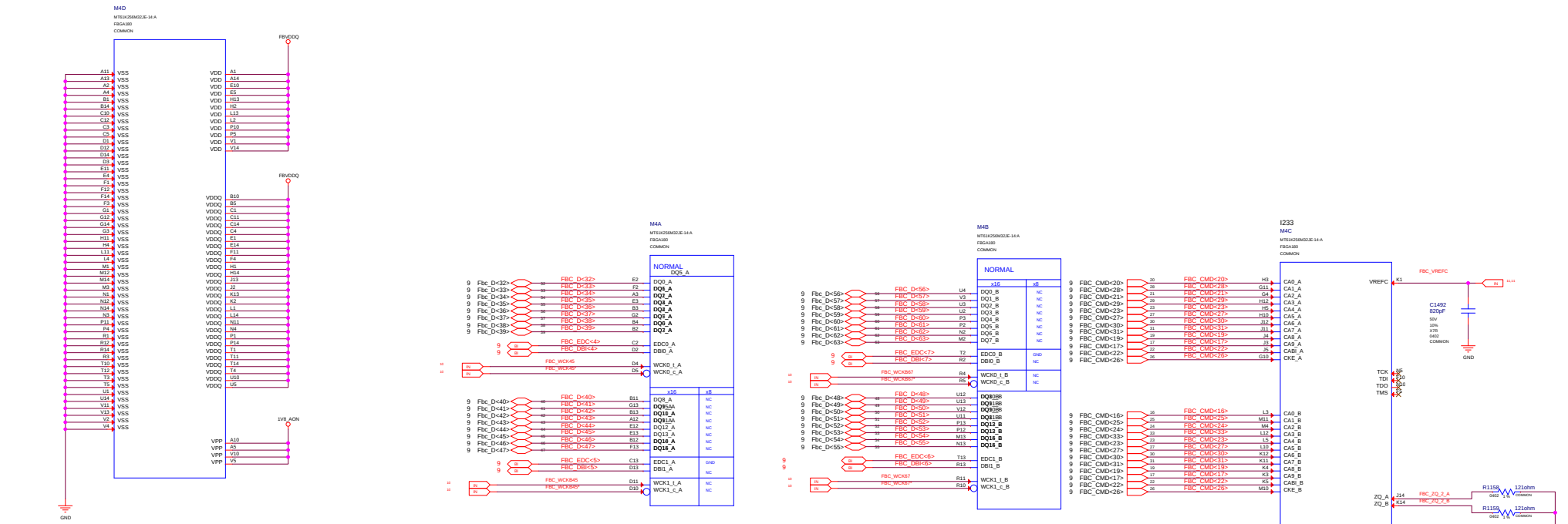
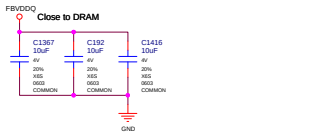
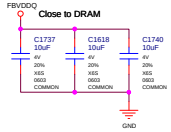
Page11: MEMORY: FBC Partition 31..0

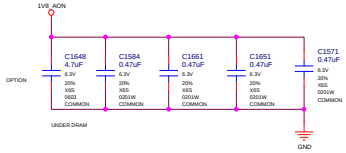


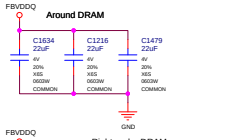
Page12: MEMORY: FBC Partition 63..32

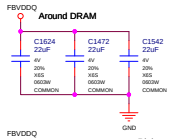


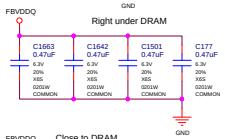


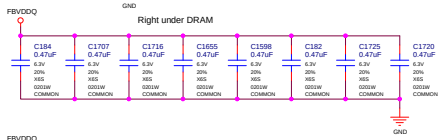


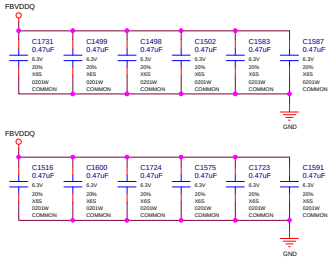


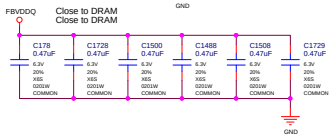


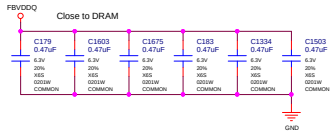












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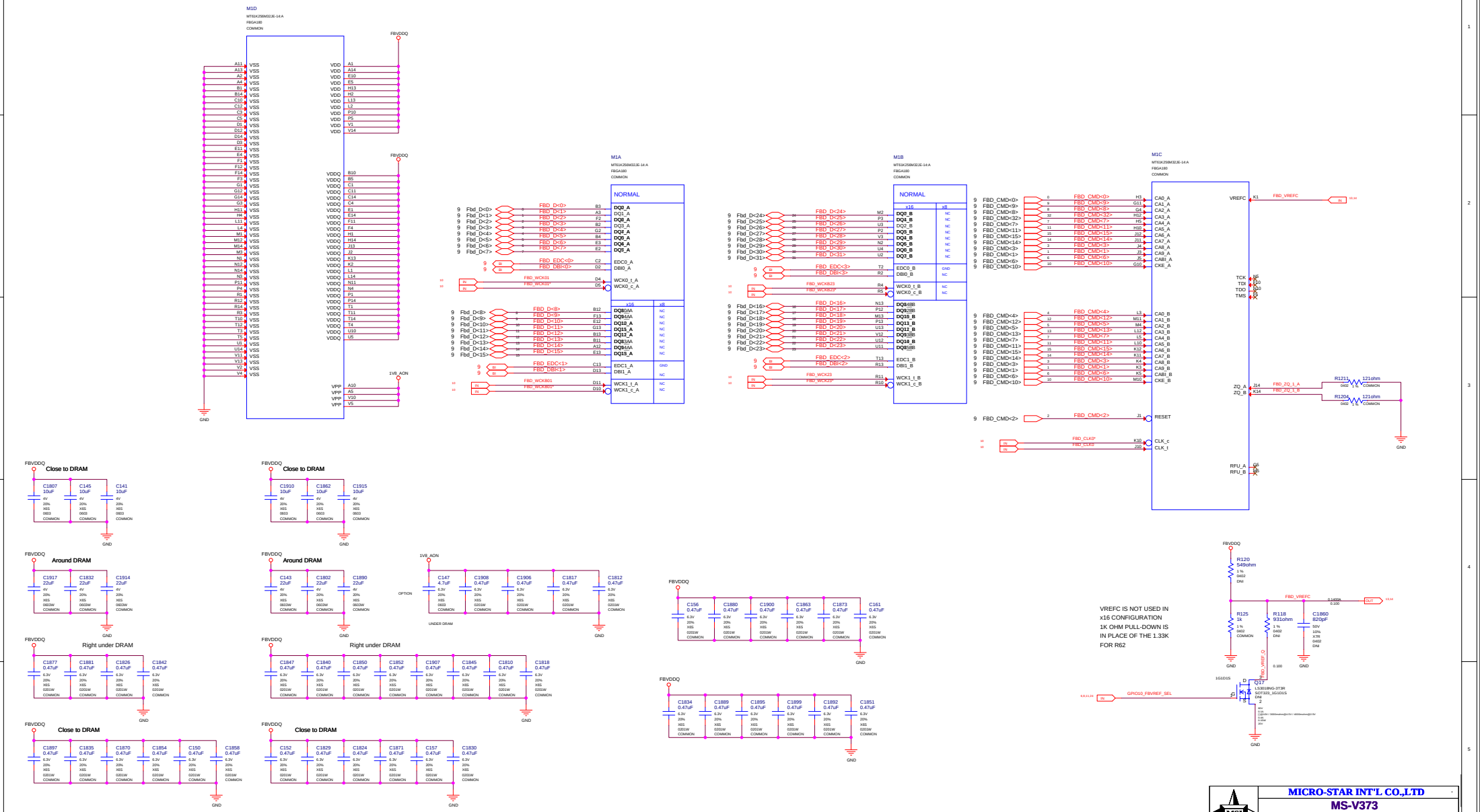

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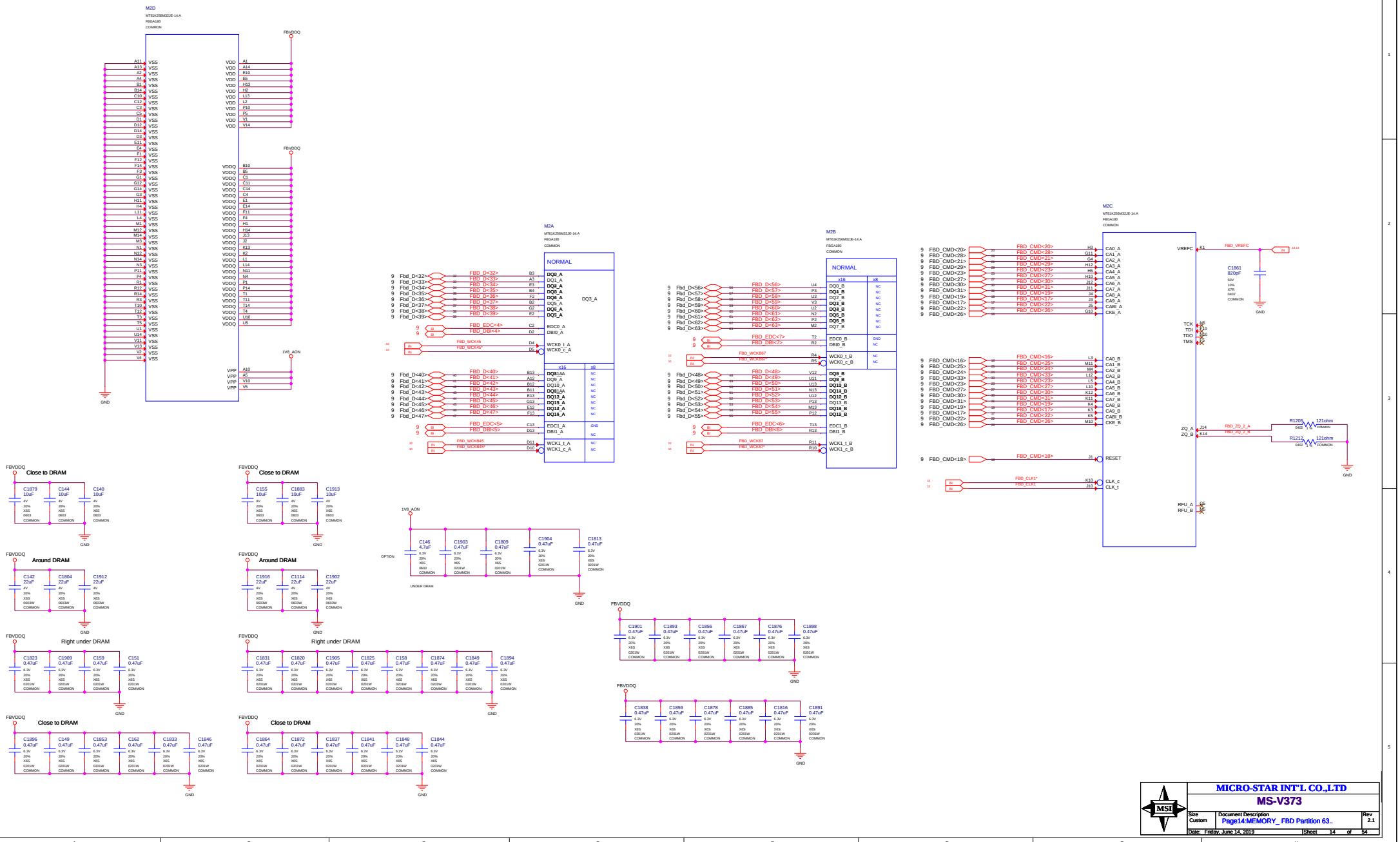
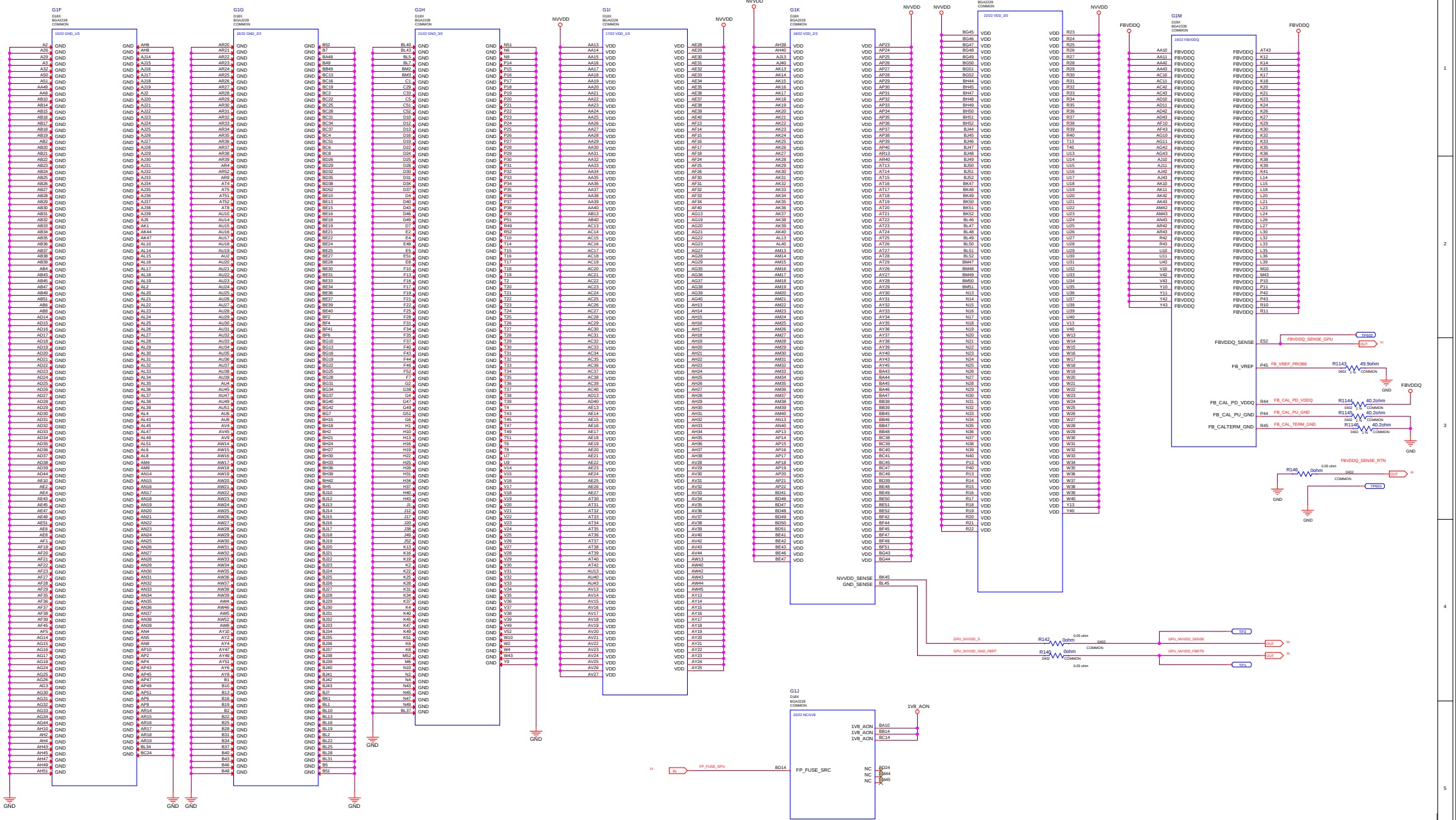
Page14: MEMORY: FBD Partition 63..32

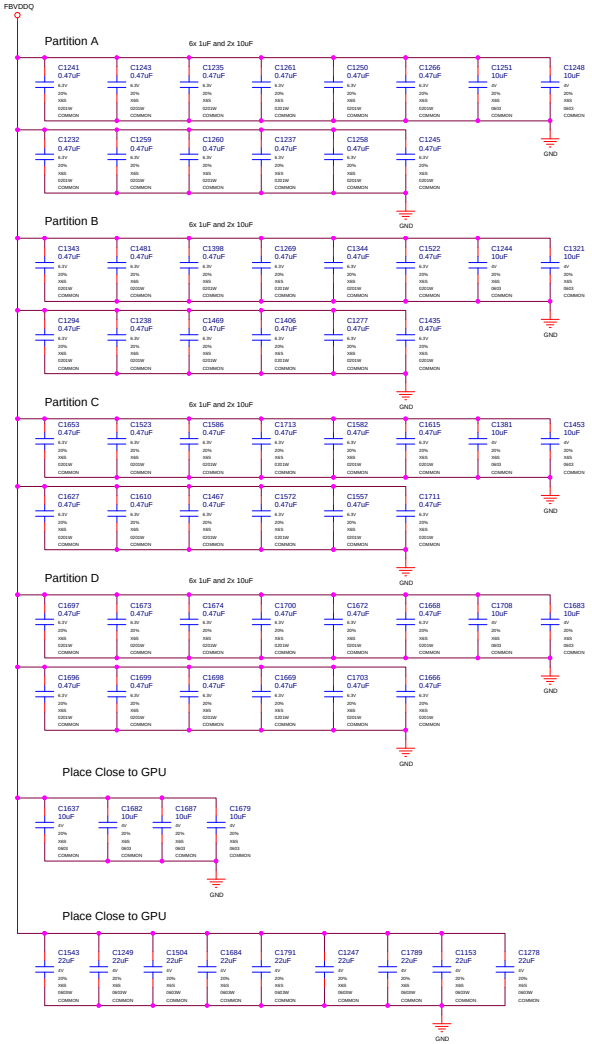


Page15: GPU PWR and GND



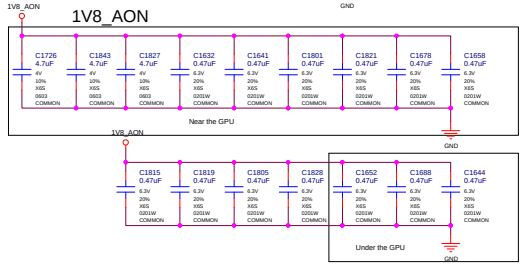
Page16: GPU Decoupling

FBVDDQ

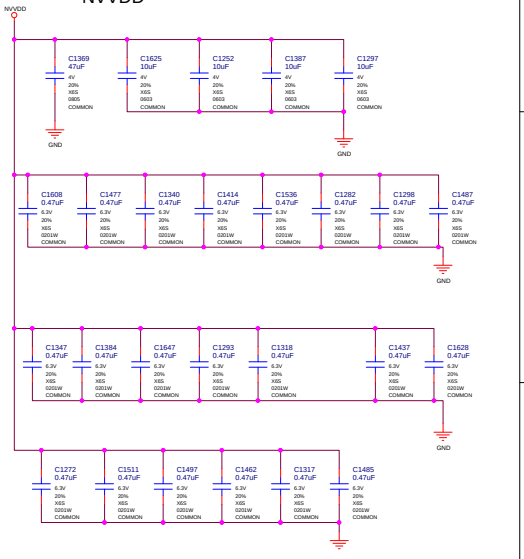


NVVDD

1V8_AON



NVVDD



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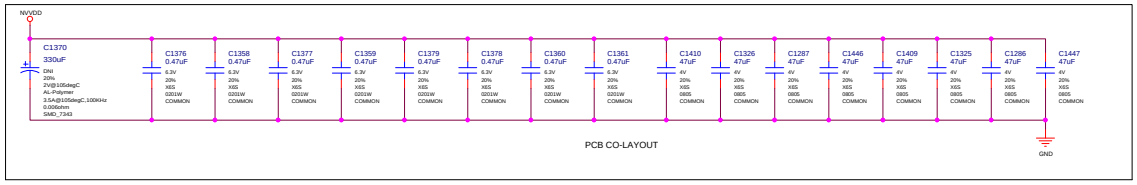
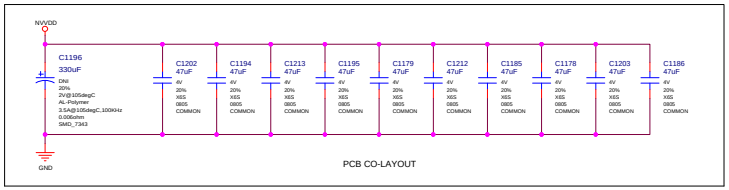
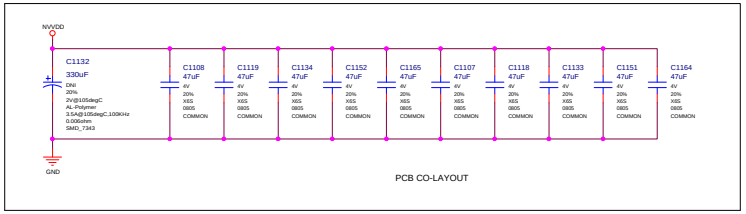
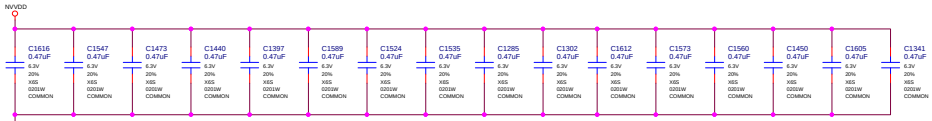
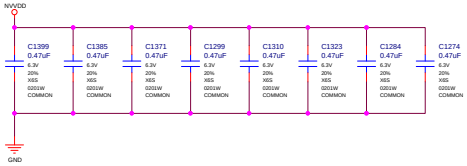
Page17: GPU Decoupling

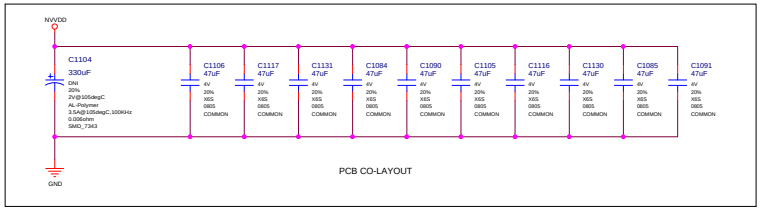


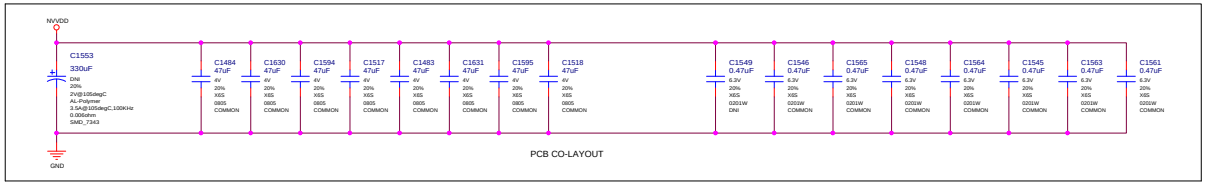












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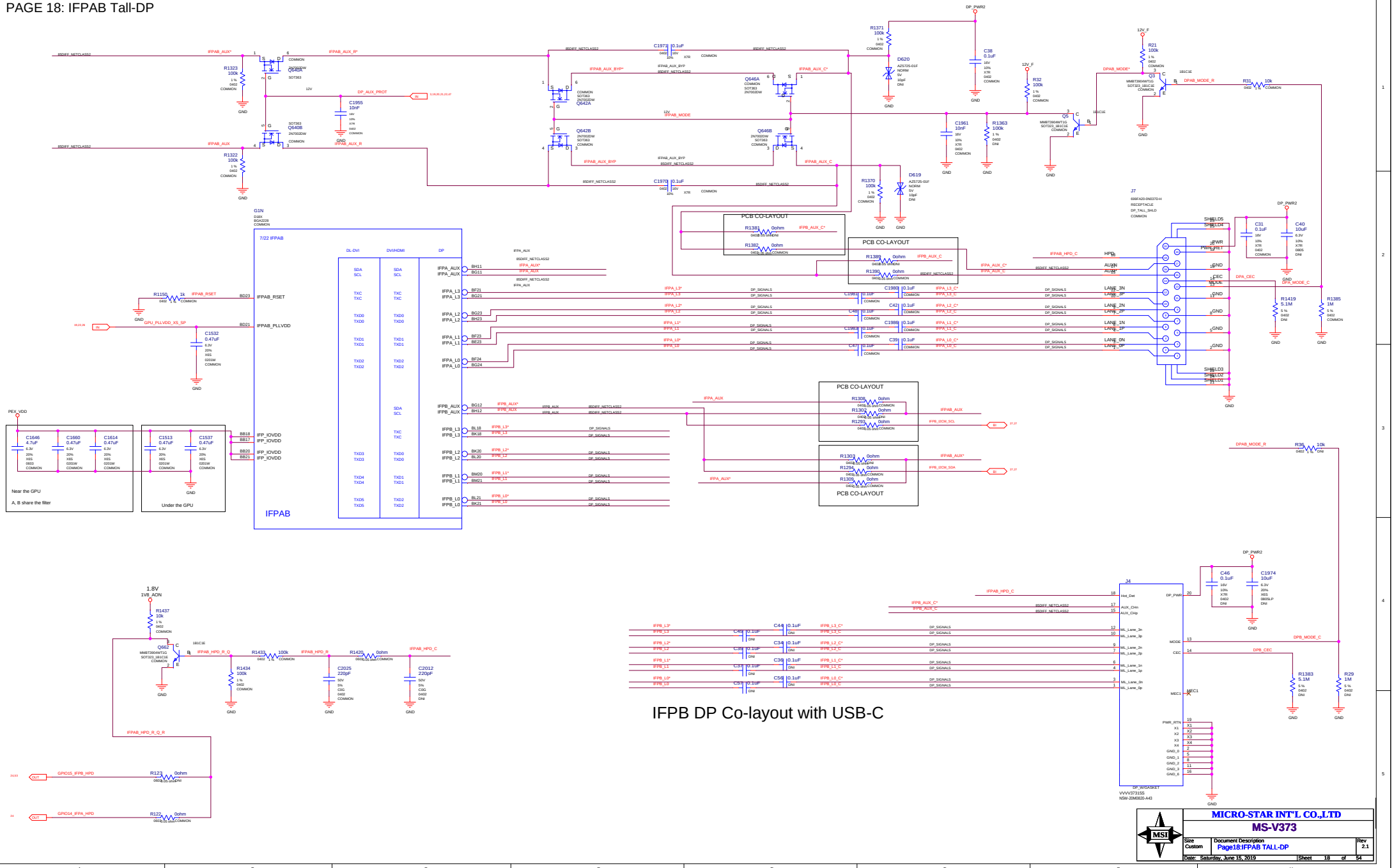
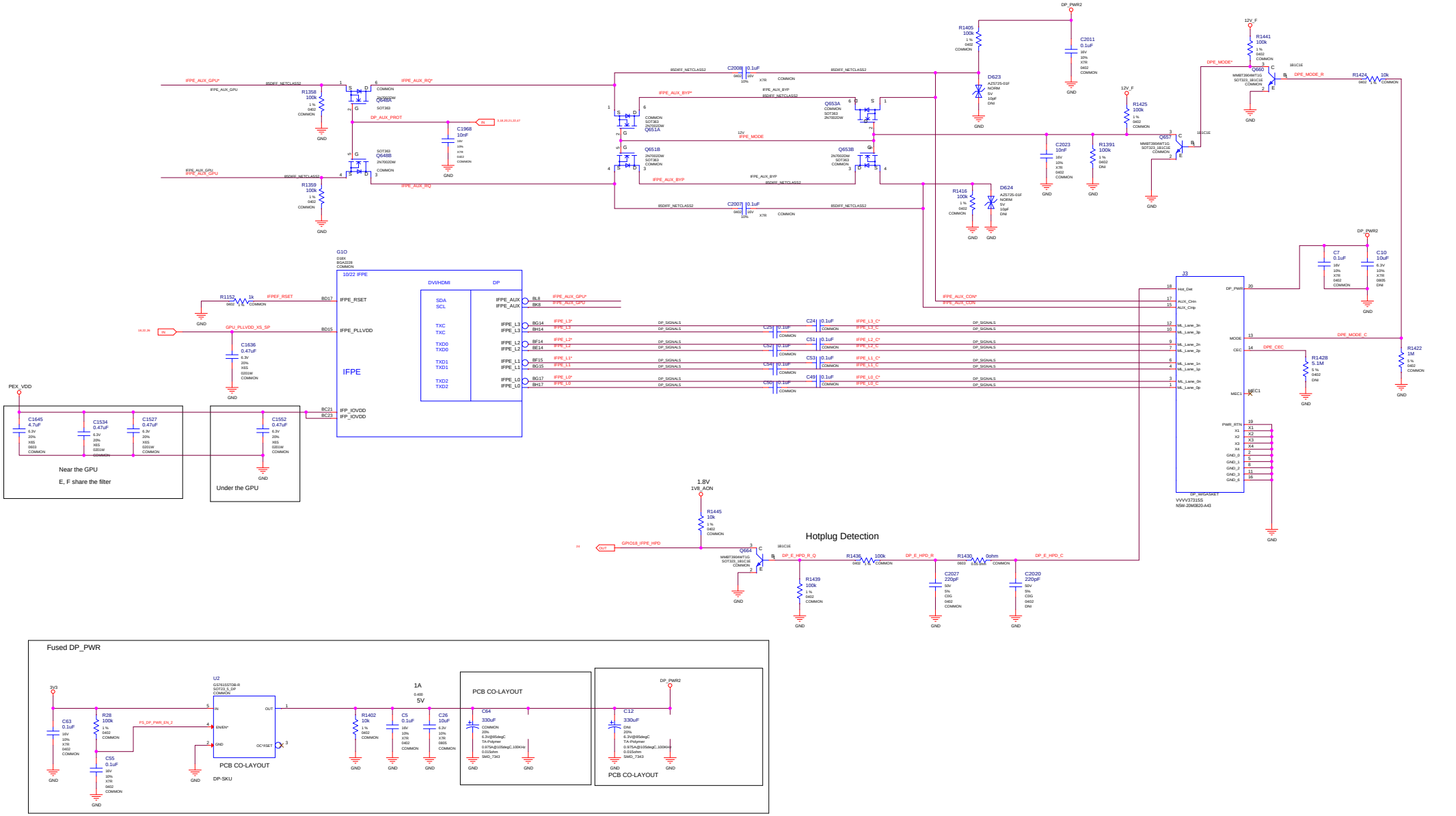
PAGE 18: IFPAB Tall-DP



IFPB DP Co-layout with USB-C

PAGE 19: IFPE DP



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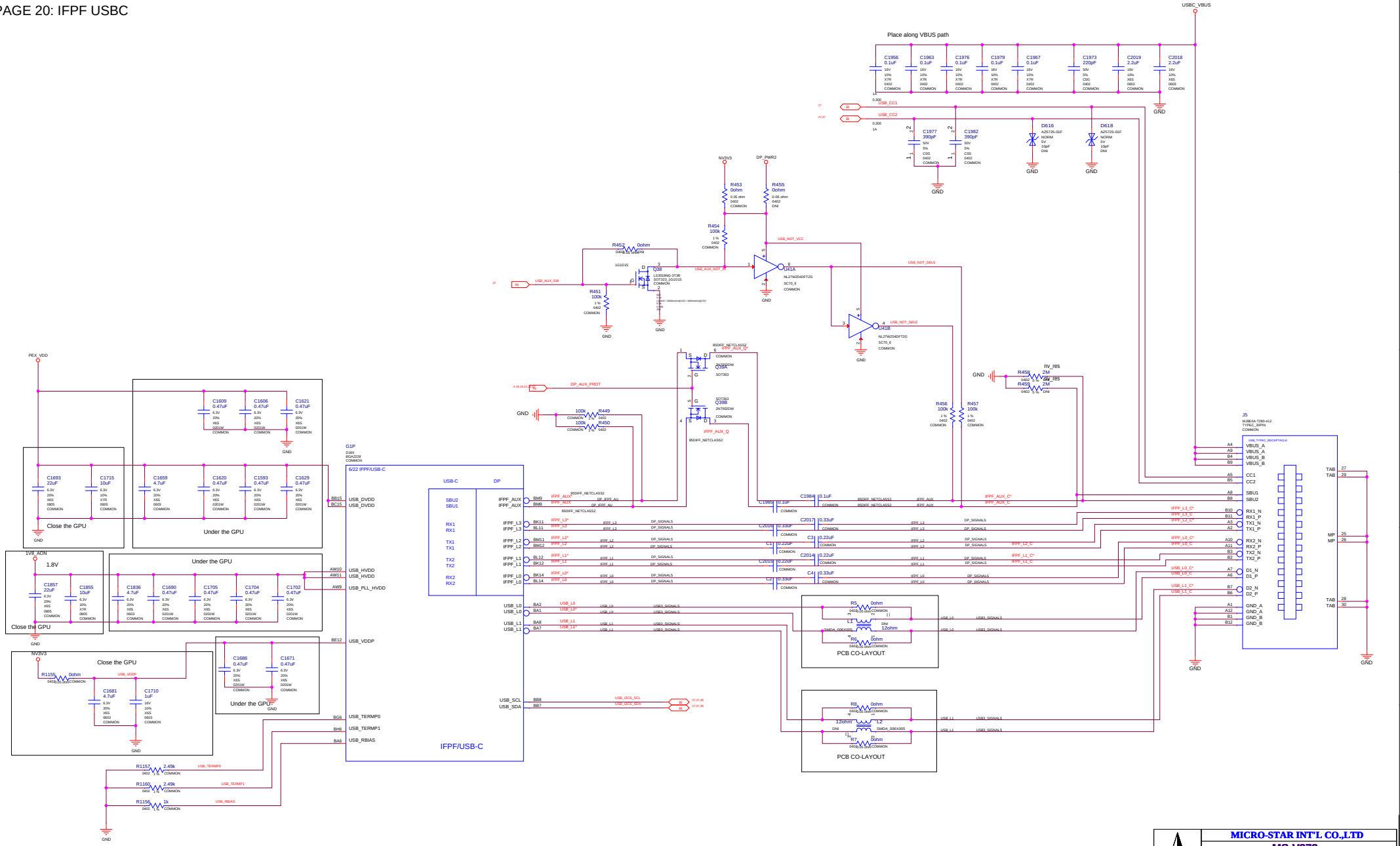
PAGE 20: IFPF USBC



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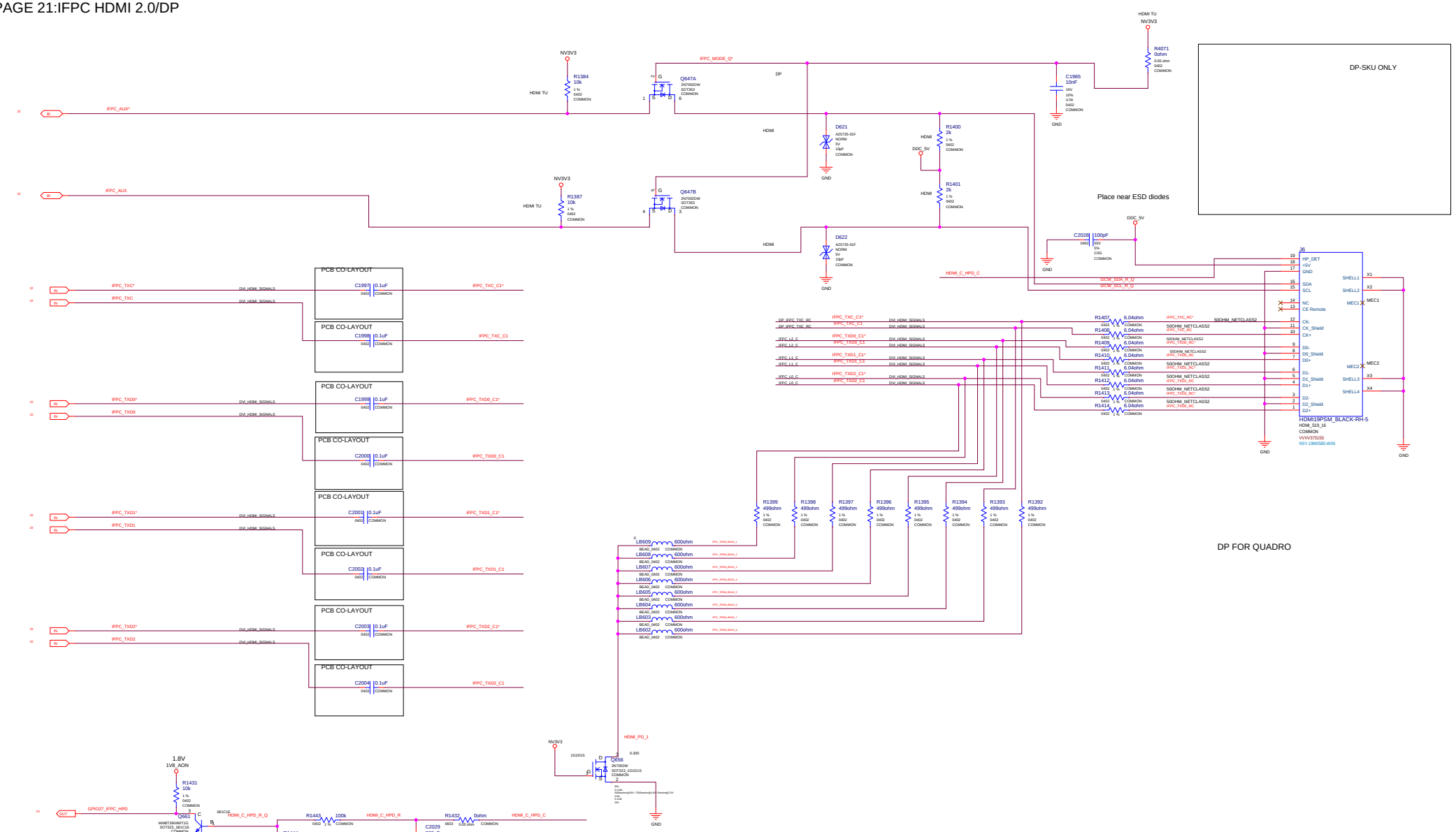
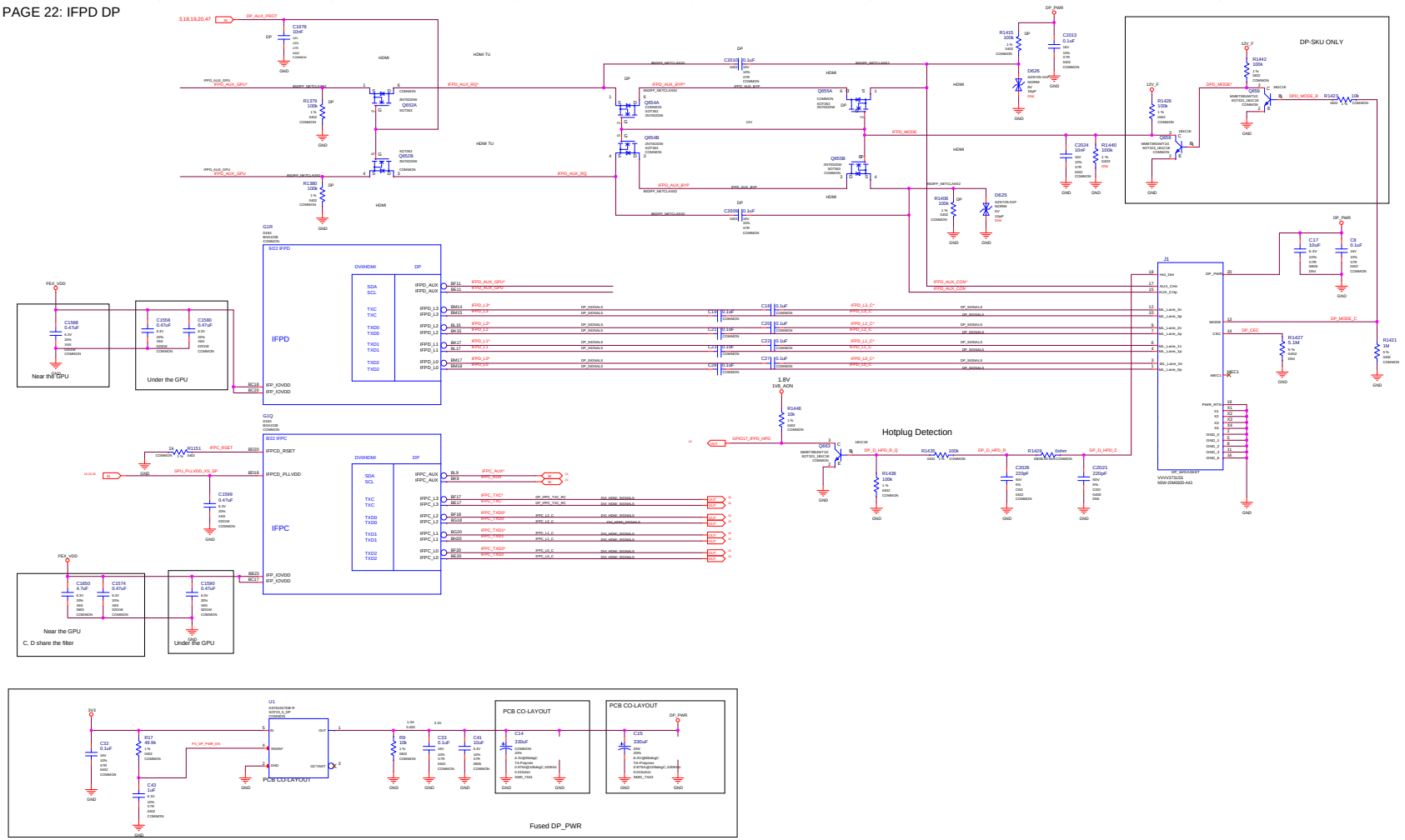
PAGE 21:IFPC HDMI 2.0/DP



PAGE 22: IFPD DP



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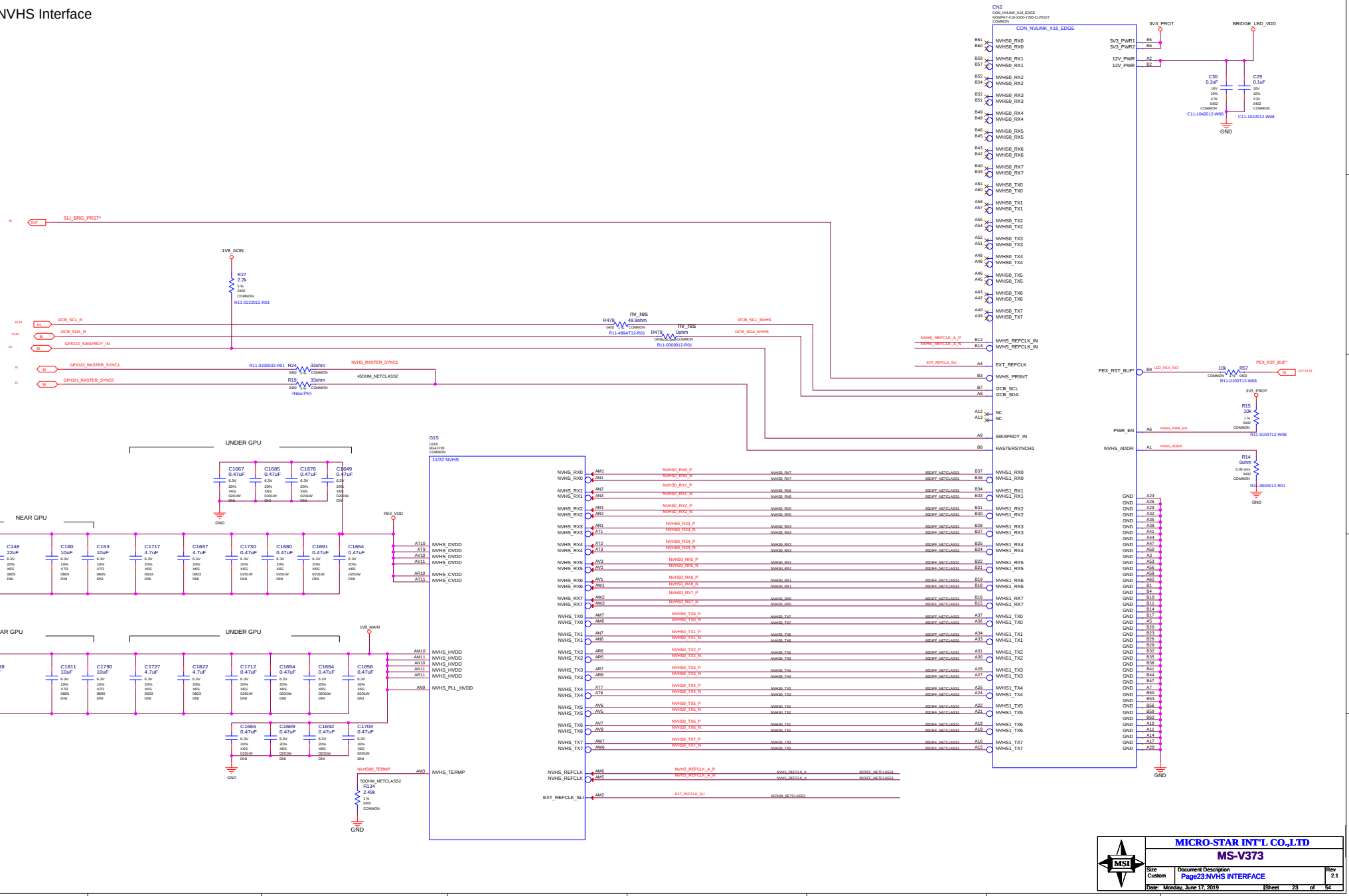
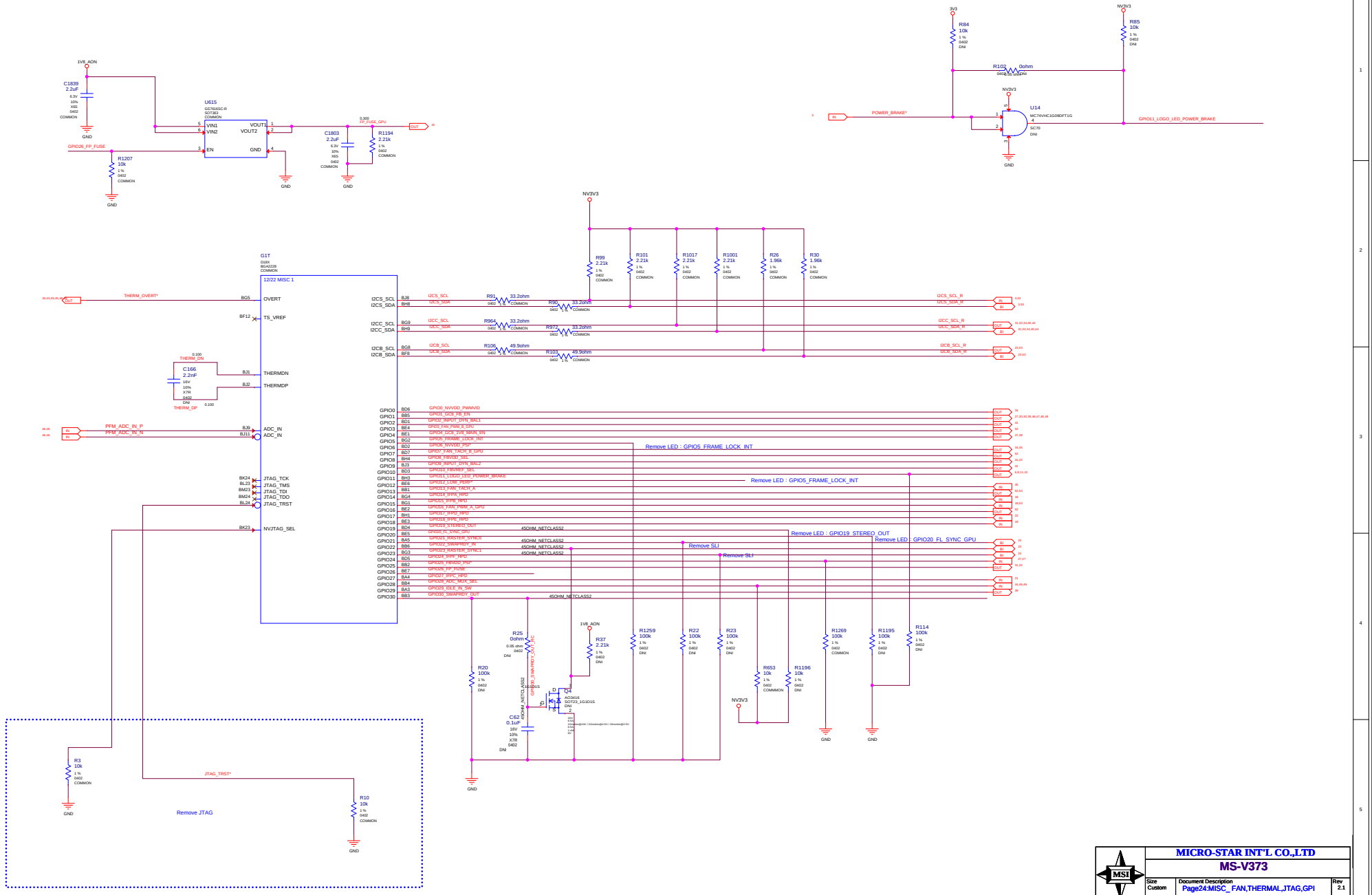
PAGE 23: NVHS Interface



PAGE 24: MISC: Fan, Thermal, JTAG, GPIO, STEREO



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PAGE 25: MISC: ROM, Straps

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]		
L	L	L	00000	RAMCFG TBD	
L	L	H	00001	RAMCFG TBD	DEFAULT
L	H	L	00010	RAMCFG TBD	
L	H	H	00011	RAMCFG TBD	
H	H	L	00110	RAMCFG TBD	
H	H	H	00111	RAMCFG TBD	

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

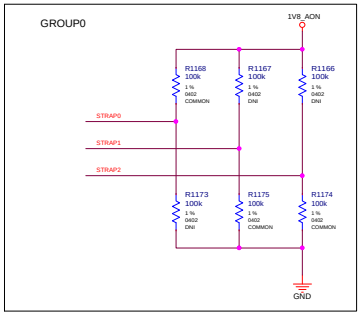
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	

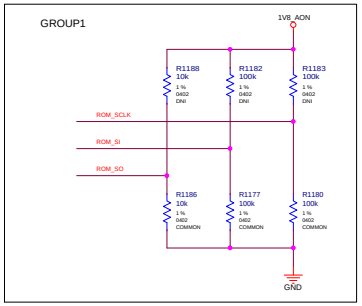
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

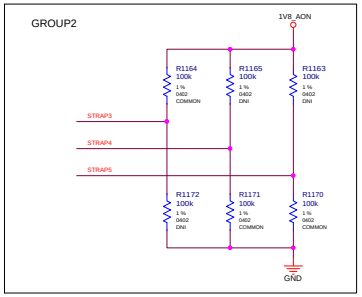
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

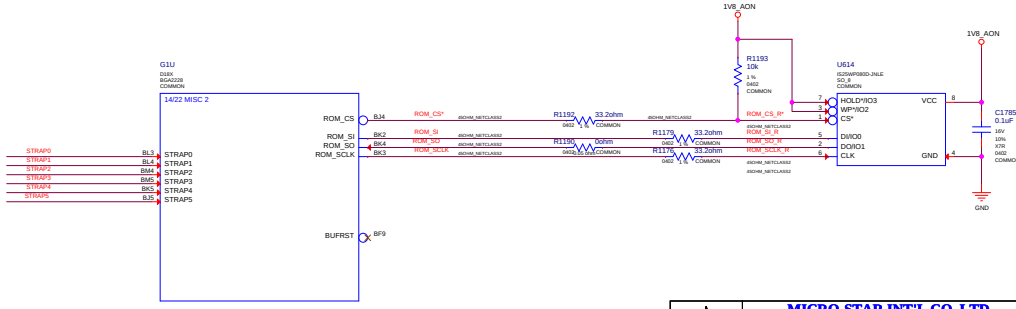
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE









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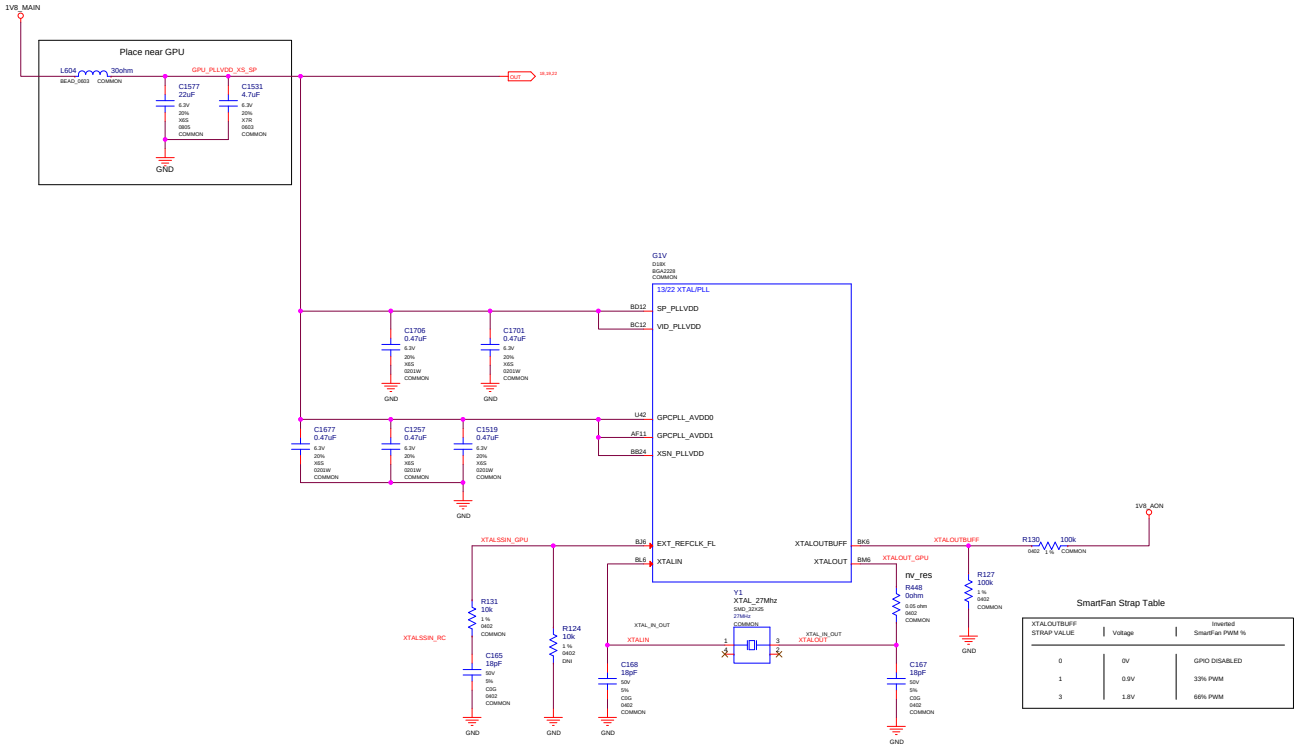
PAGE 26: MISC: XTAL. PLL



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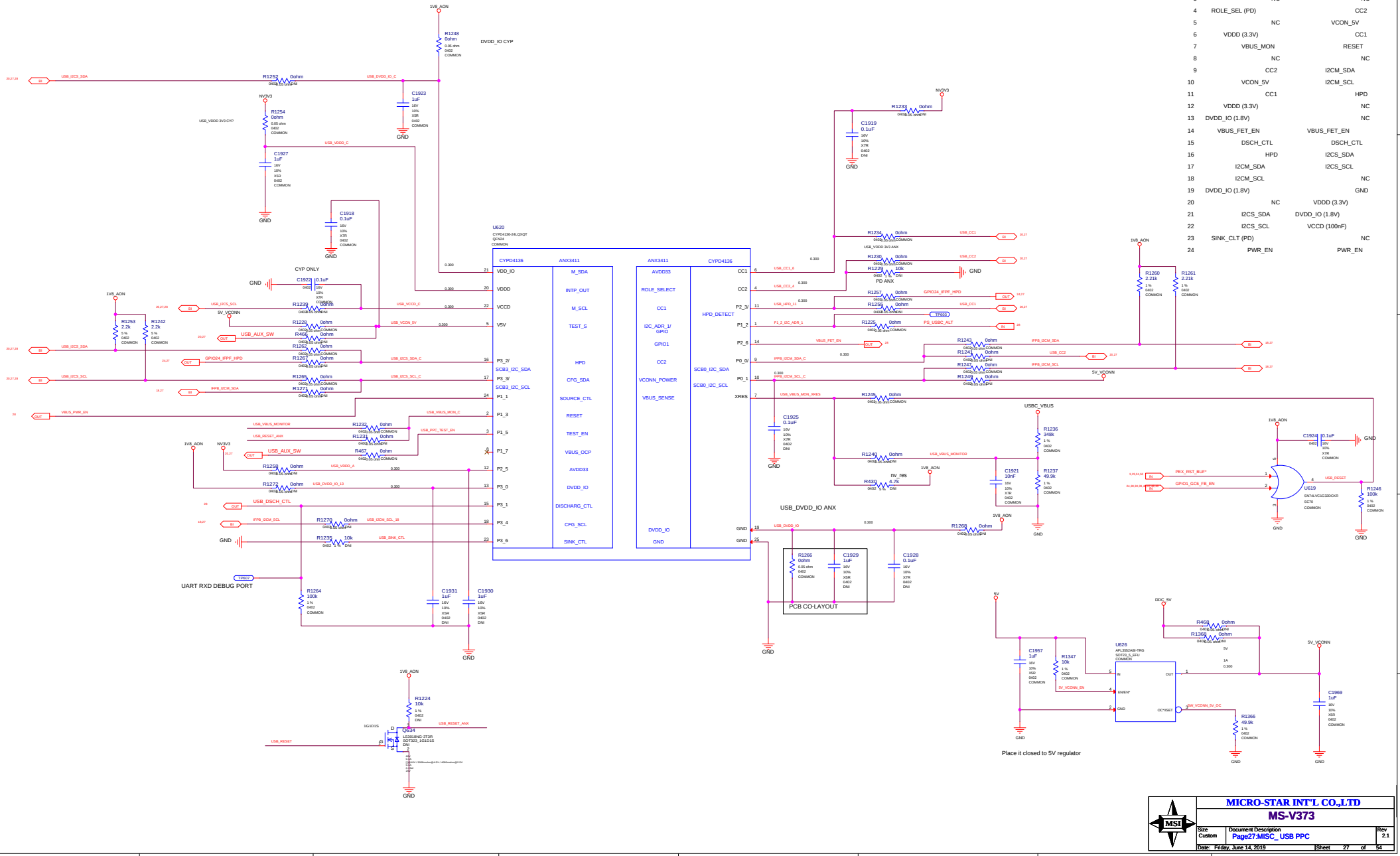
PAGE 27: MISC: USB PPC



PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CTL (PD)	NC
24	PWR_EN	PWR_EN

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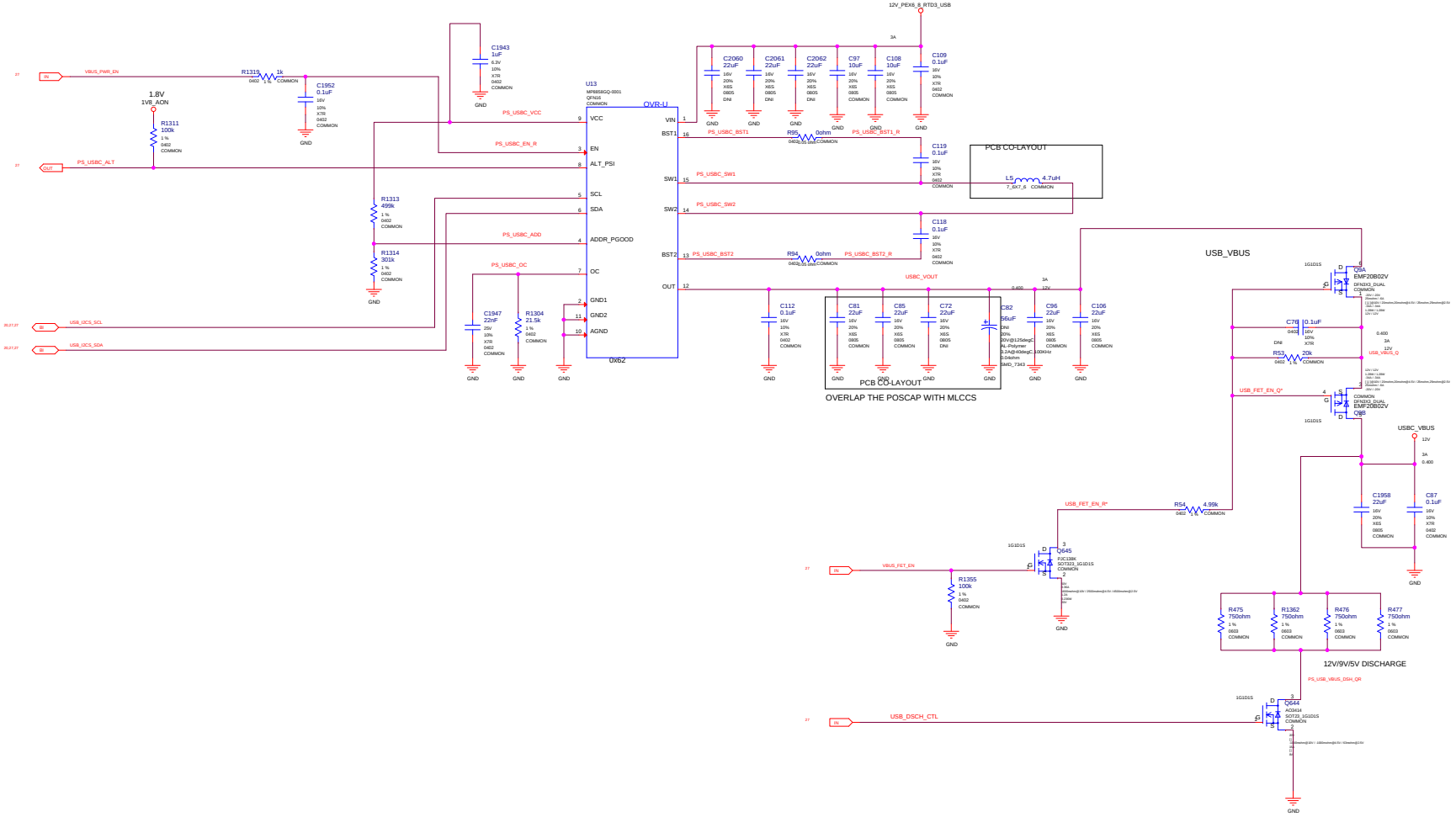
PAGE 28: PS: USB VR



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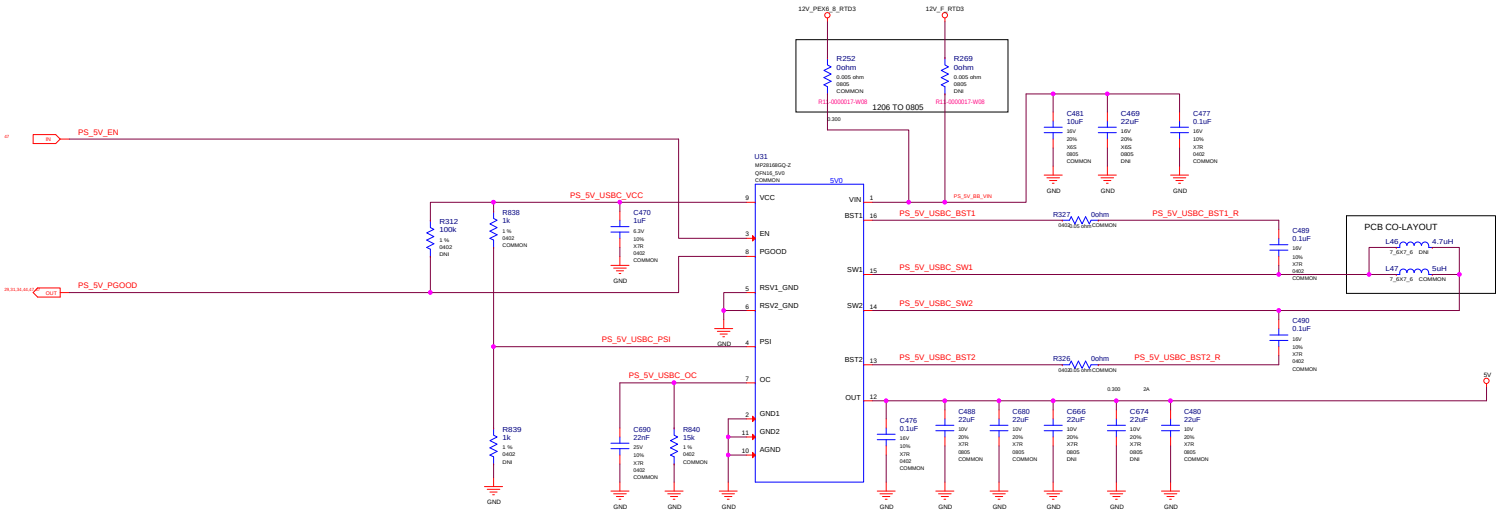
PAGE 29: PS: 5V, 5V_BACKUP



remove

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Size: Custom	Document Description: Page29:PS_ 5V, 5V BACKUP	Rev: 2.1
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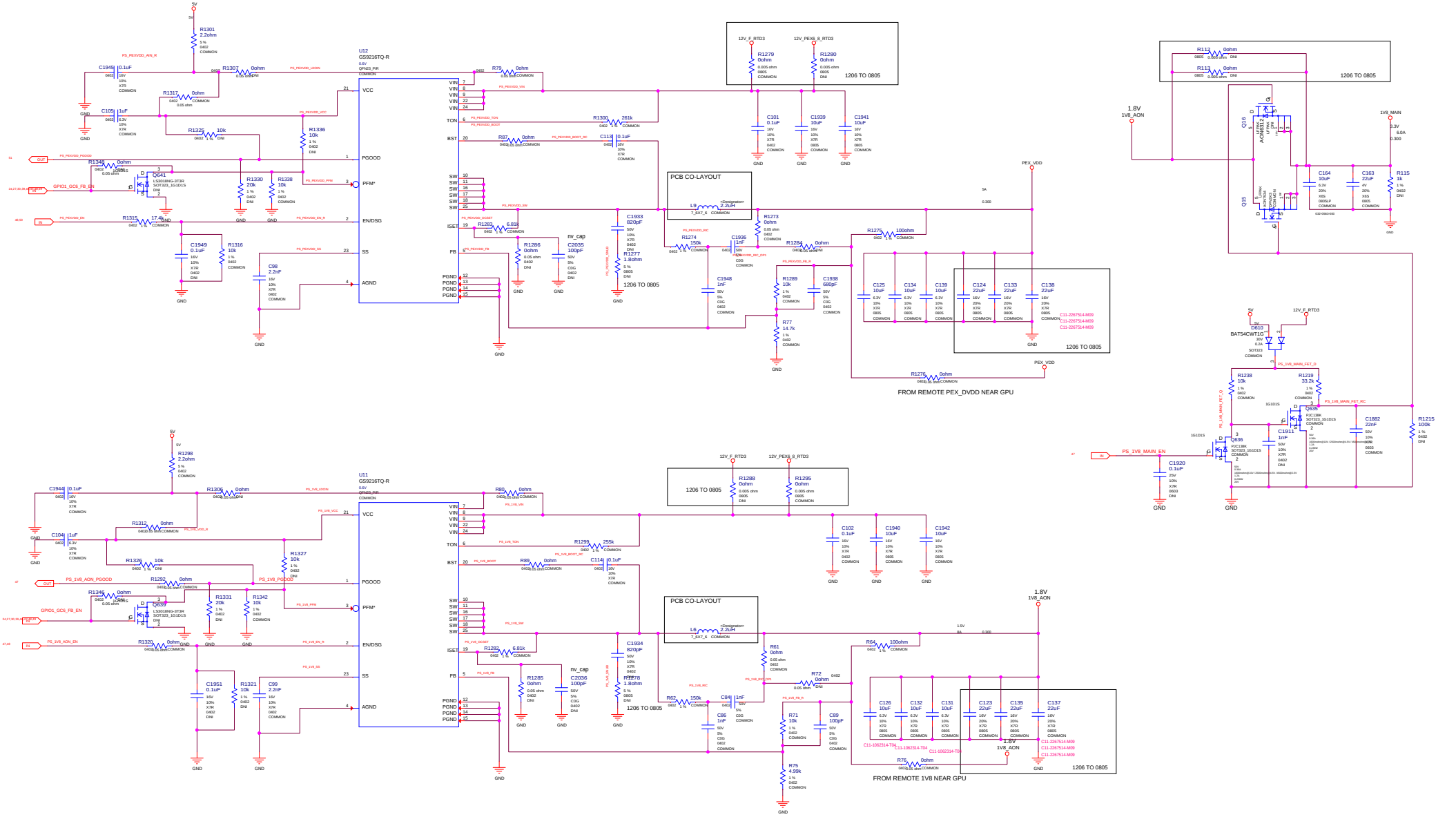
PAGE 30: PS: PEXVDD, 1V8



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Size: Custom	Document Description: Page30:PS_ PEXVDD, 1V8	Rev: 2.1
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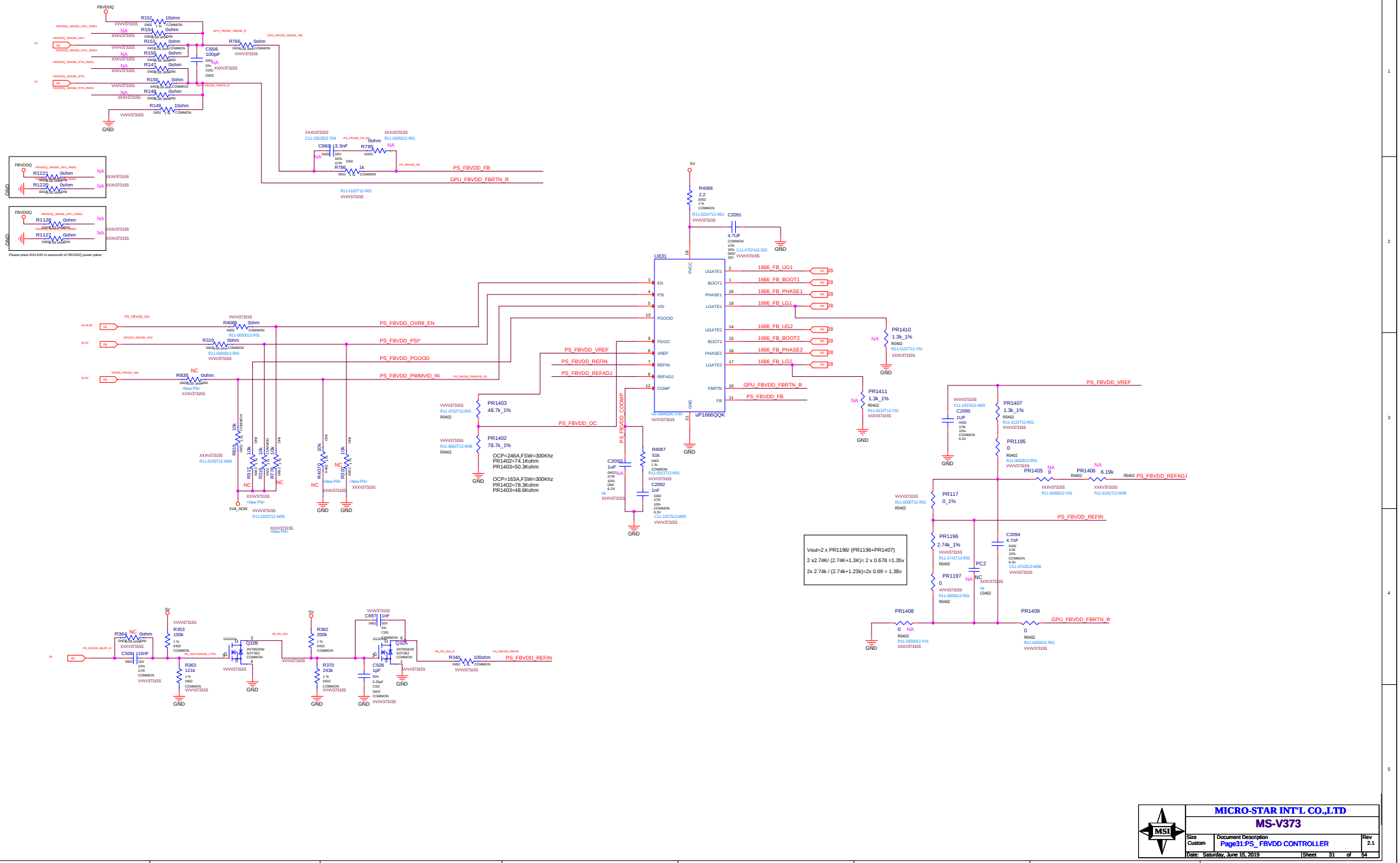
PAGE 31: PS: FBVDD Controller



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PAGE 32: PS: FBVDD Controller OVR3

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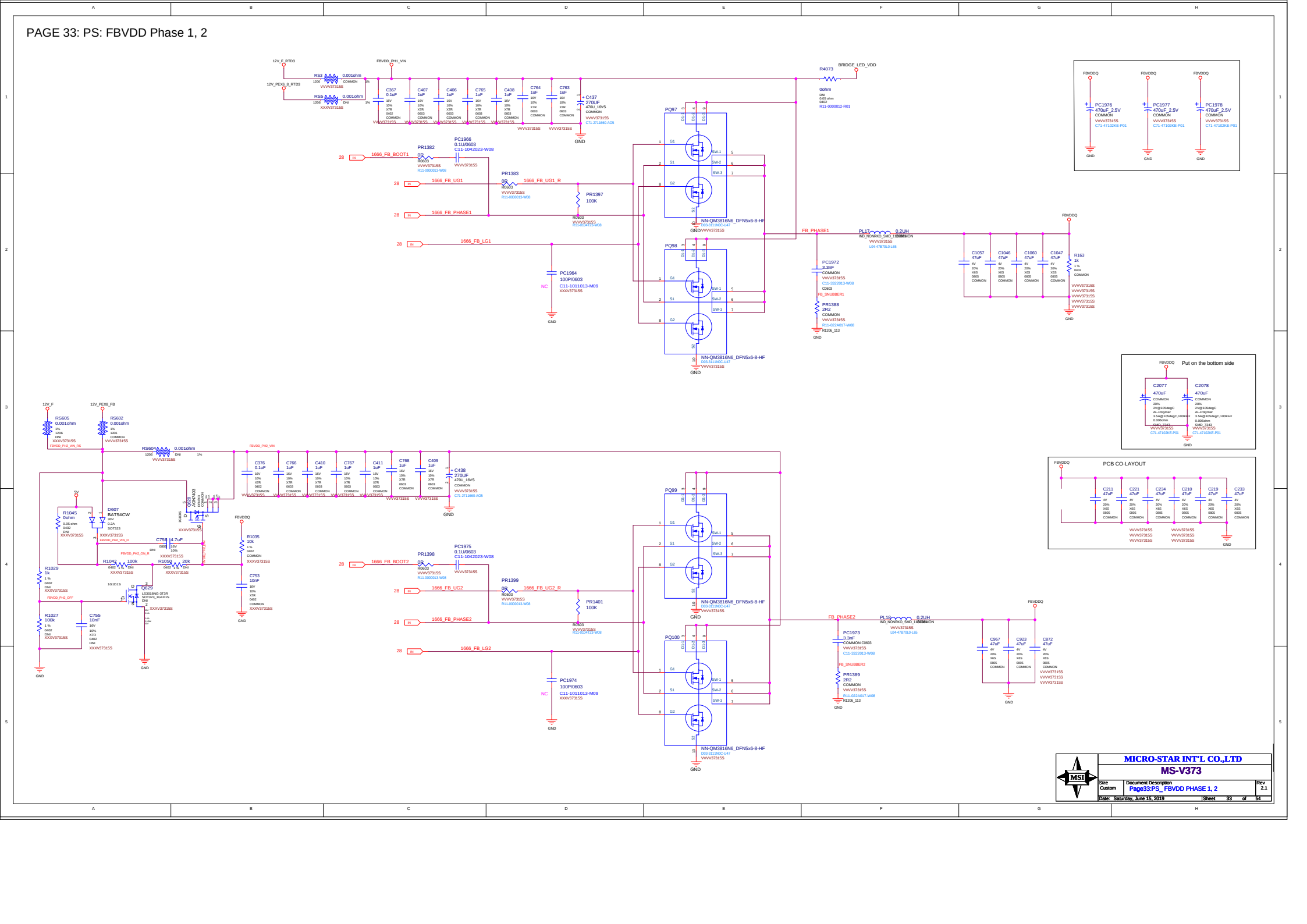
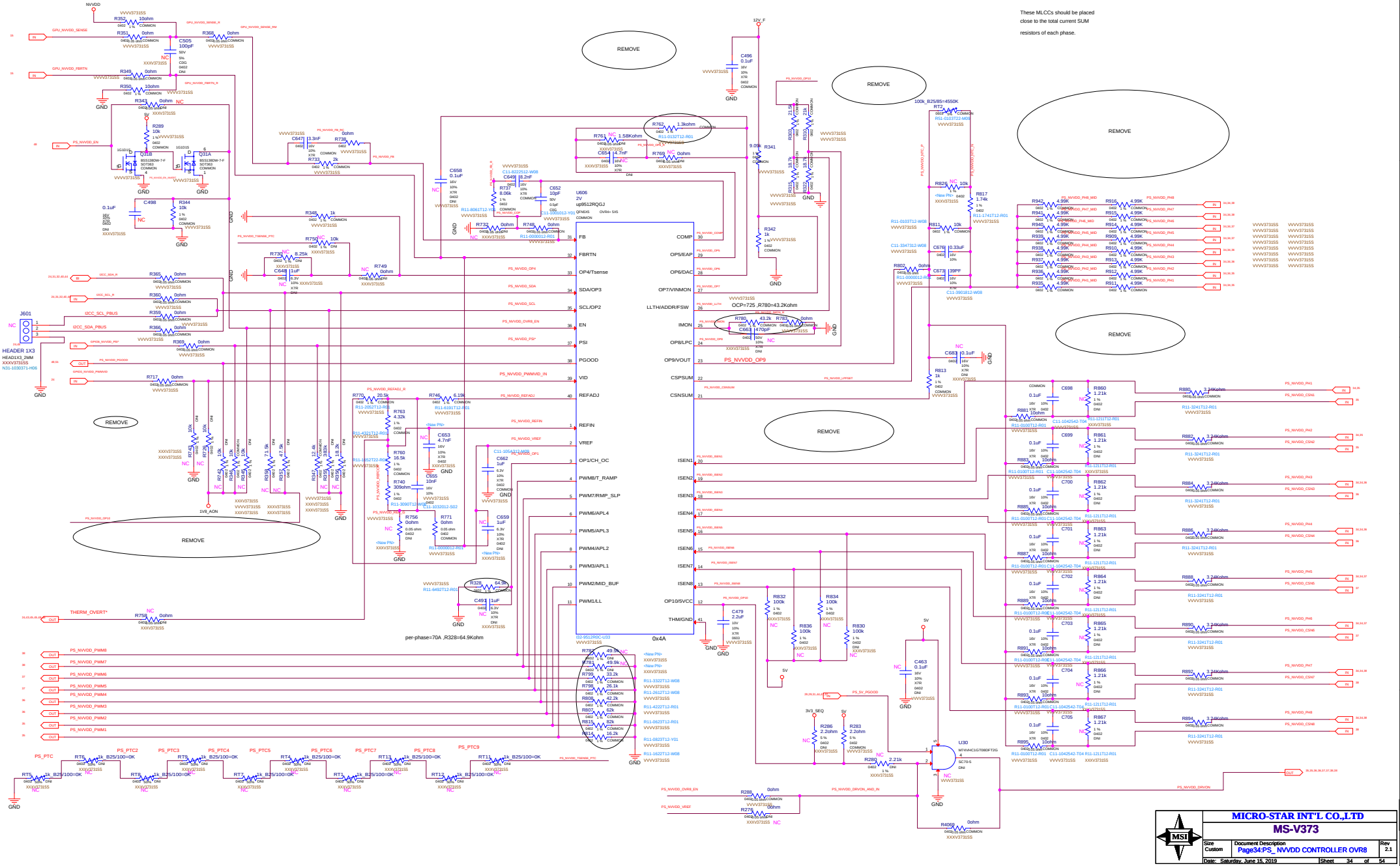
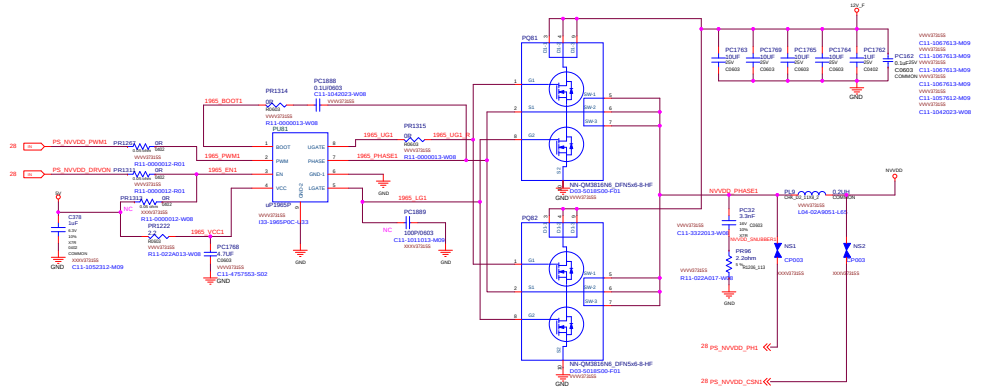
PAGE 33: PS: FBVDD Phase 1, 2

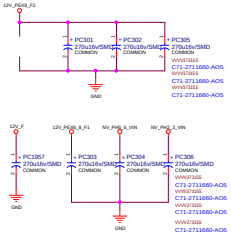


PAGE 34: PS: NVVDD Controller OVR8

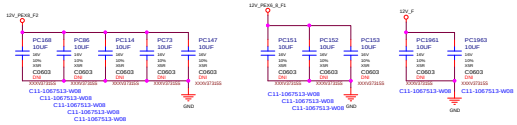


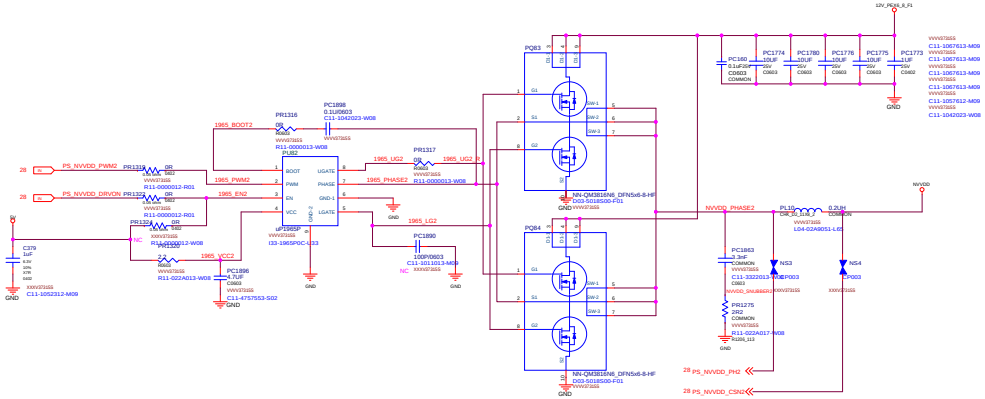


EXT_12V Input CAP



Backup





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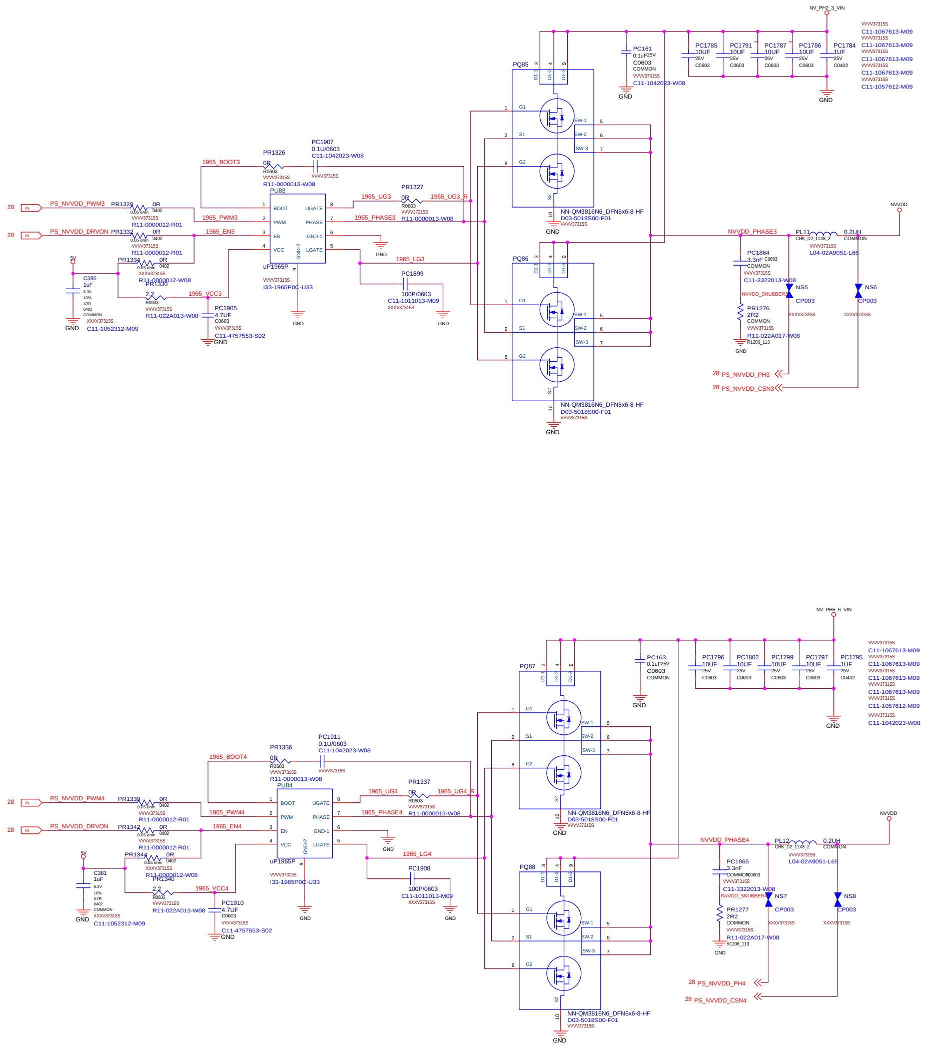
PAGE 36: PS: NVVDD Phase 3, 4



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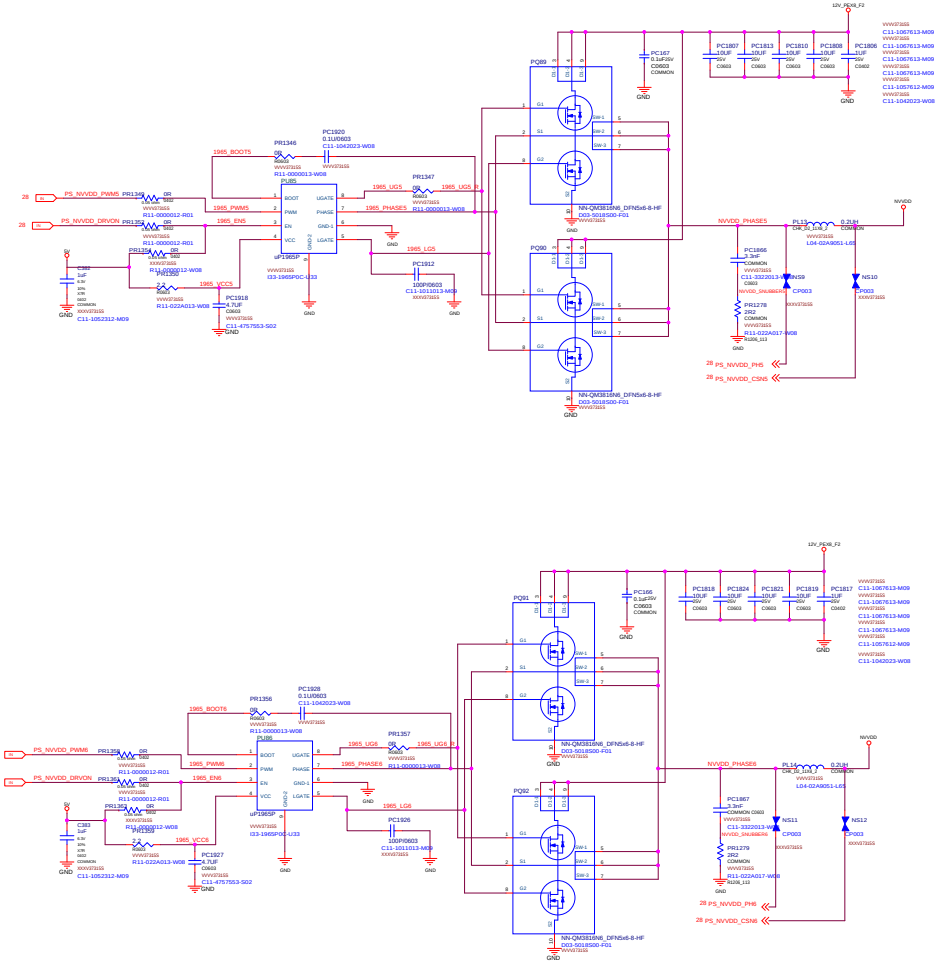

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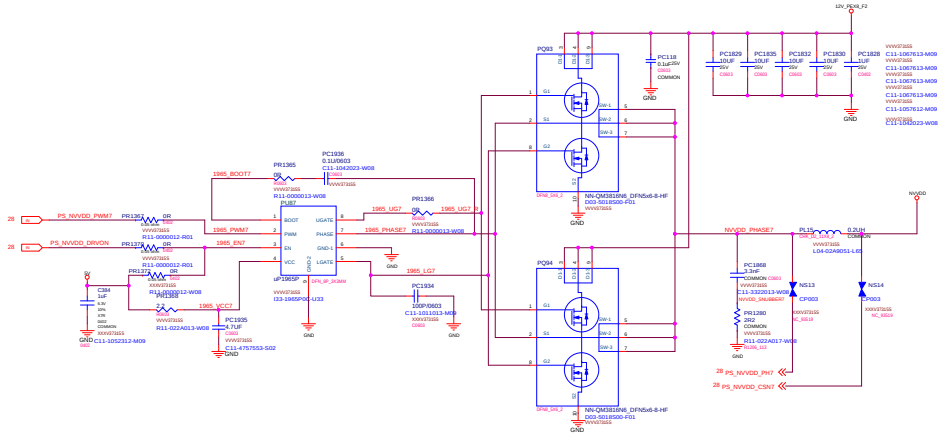
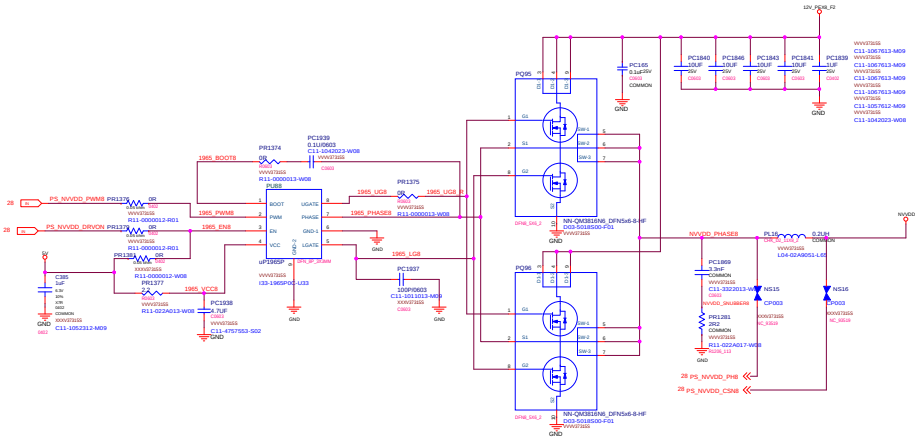
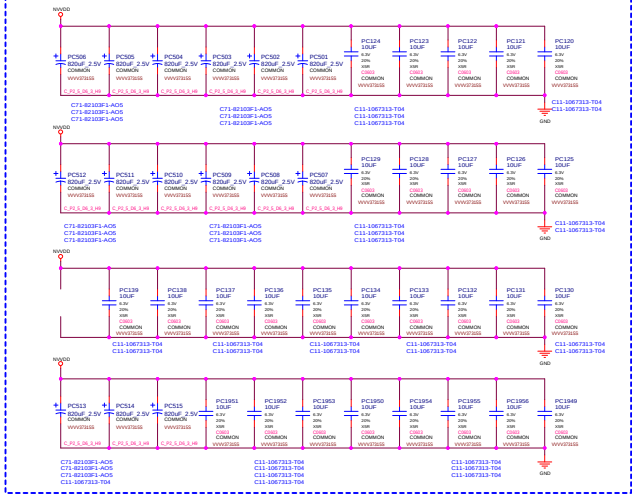




NVVDD Output CAP



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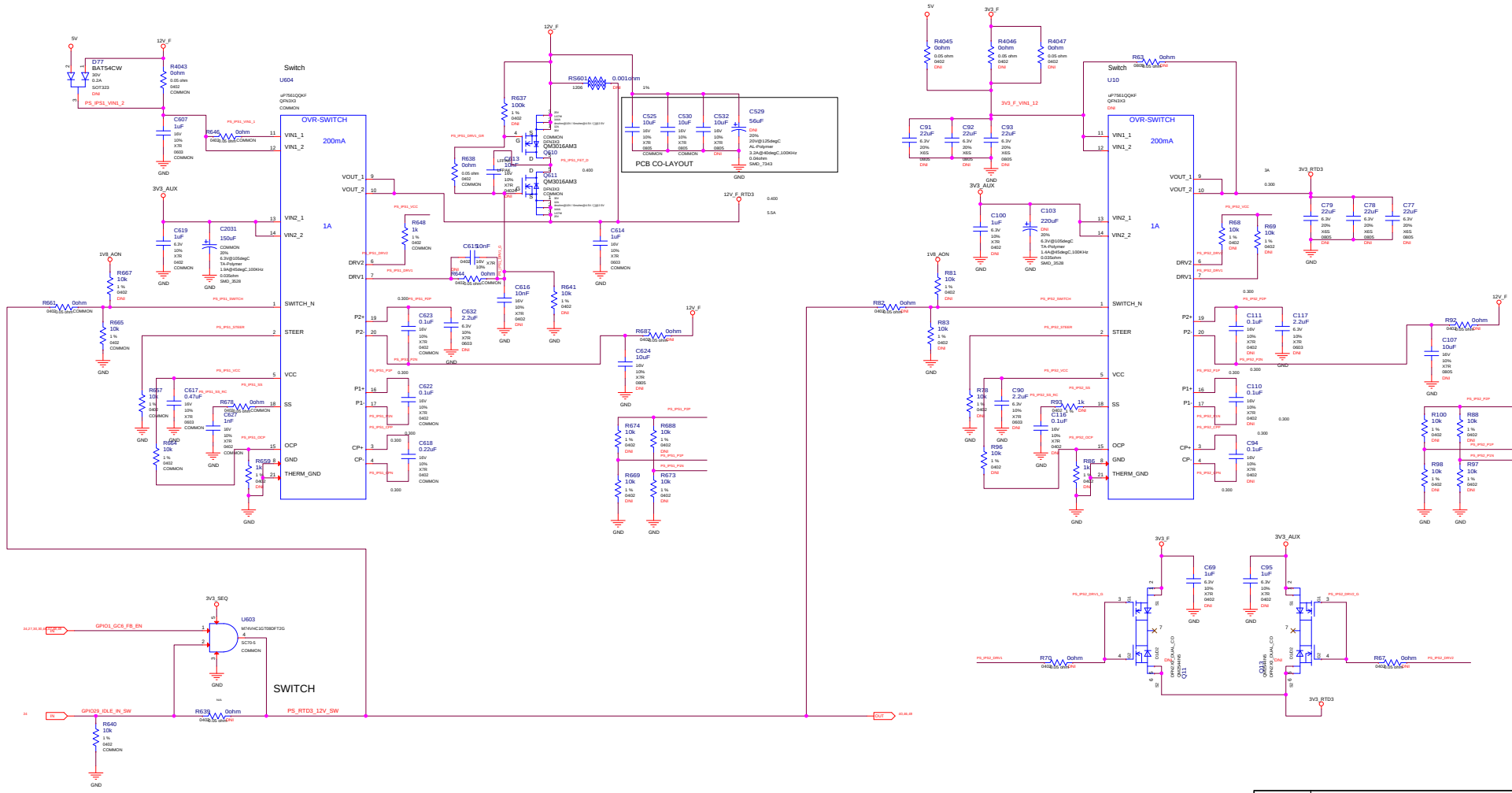
AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



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MS-V373			
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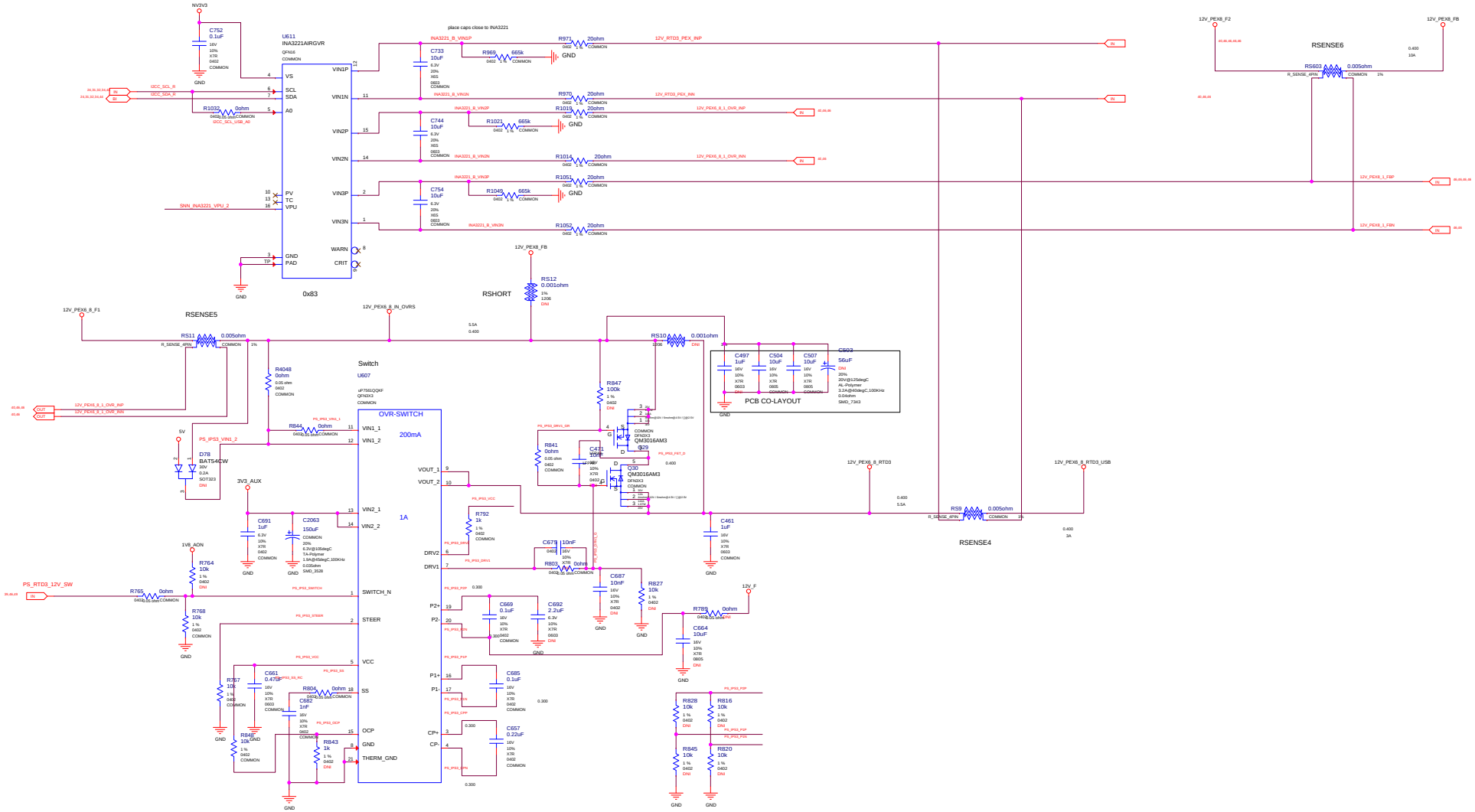

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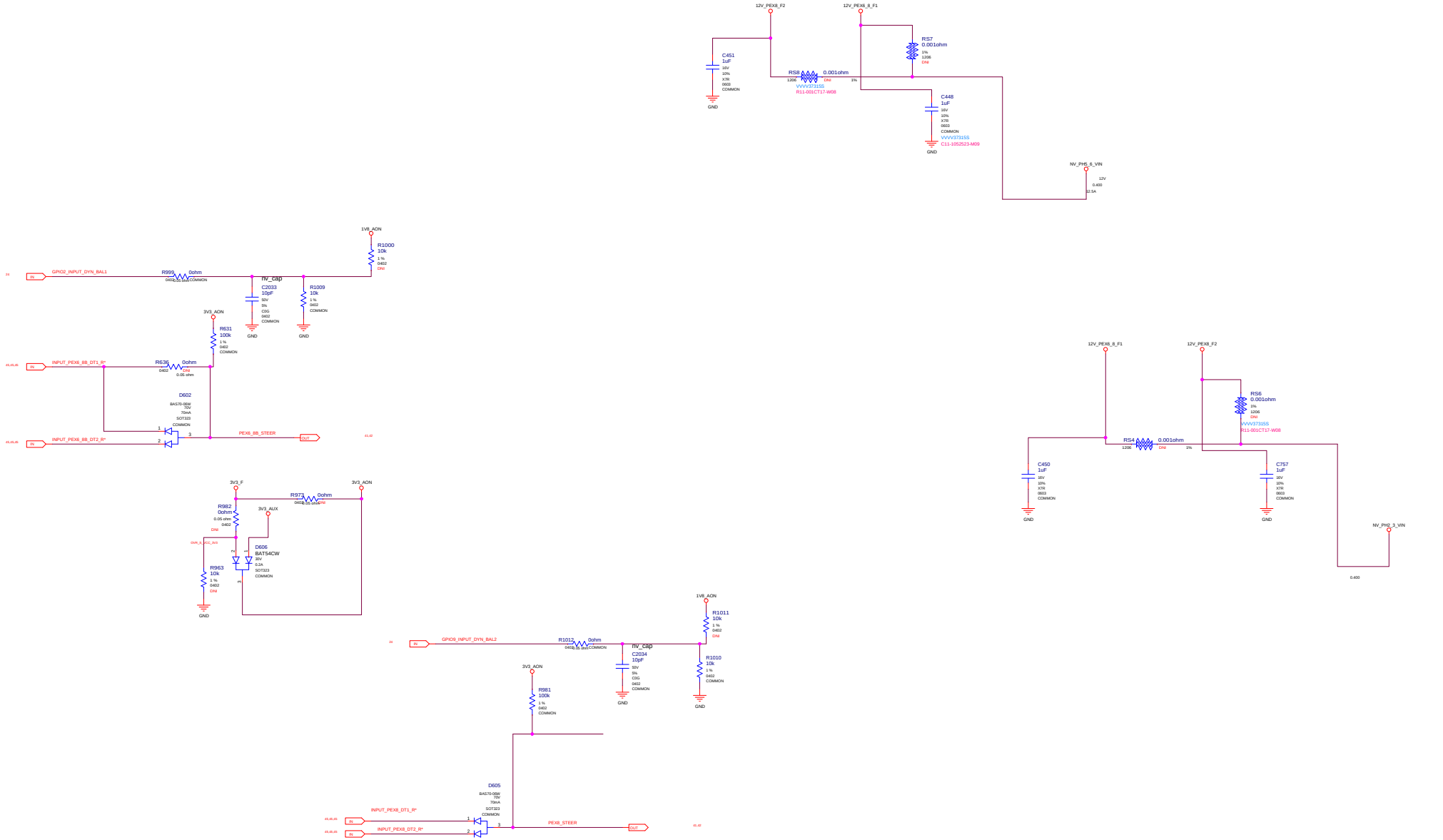
PAGE 41: PS: INPUT SWITCH Rail Balance



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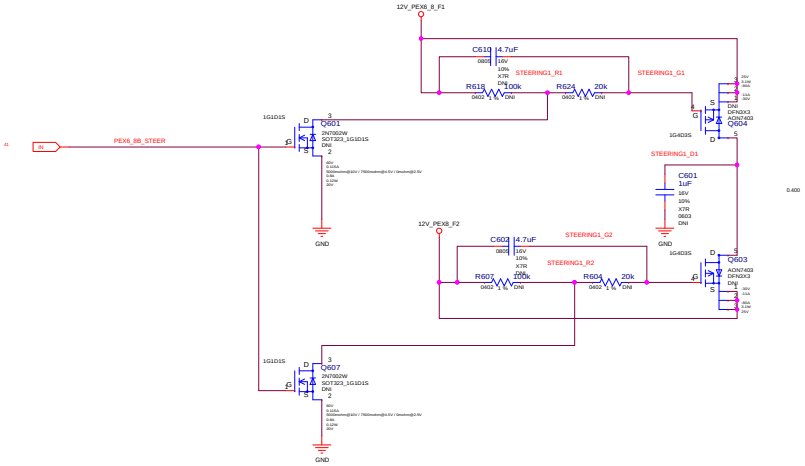
PAGE 42: PS: 12V CURRENT STEERING

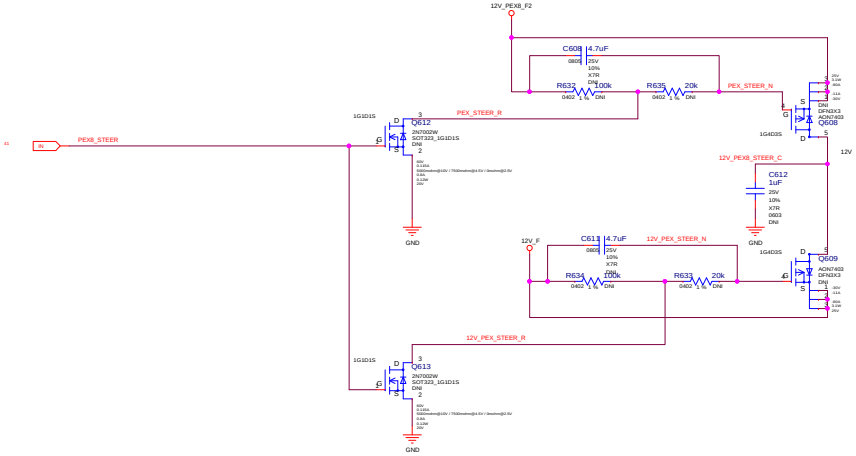
12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



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Size: Custom	Document Description: Page42:PS_ 12V CURRENT STEERING	Rev: 2.1
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PAGE 43: PS: VR THERMAL PROTECTION

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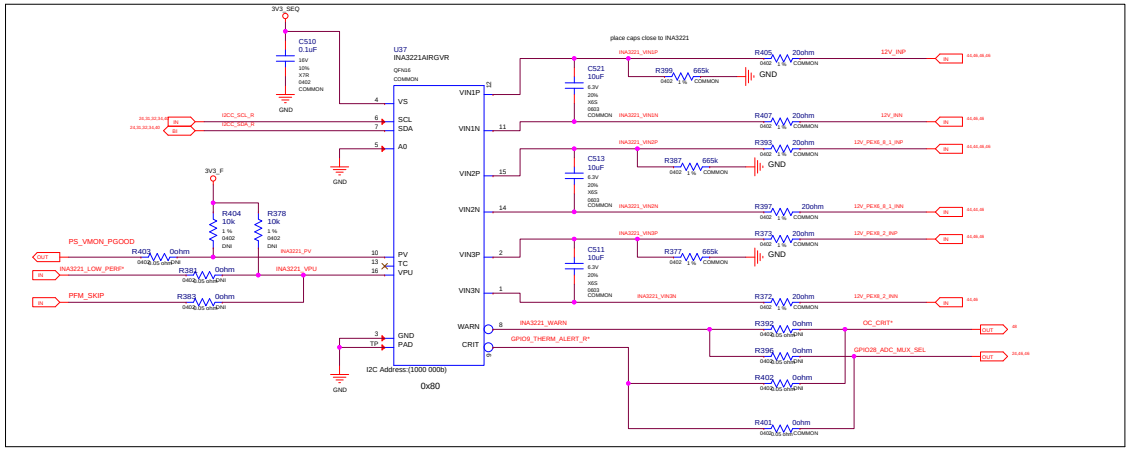
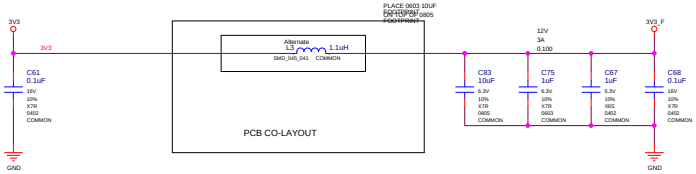
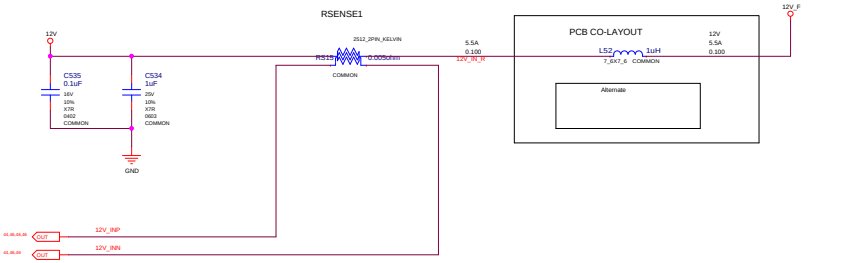
PAGE 44: PS: Inputs, Filtering, and Monitoring



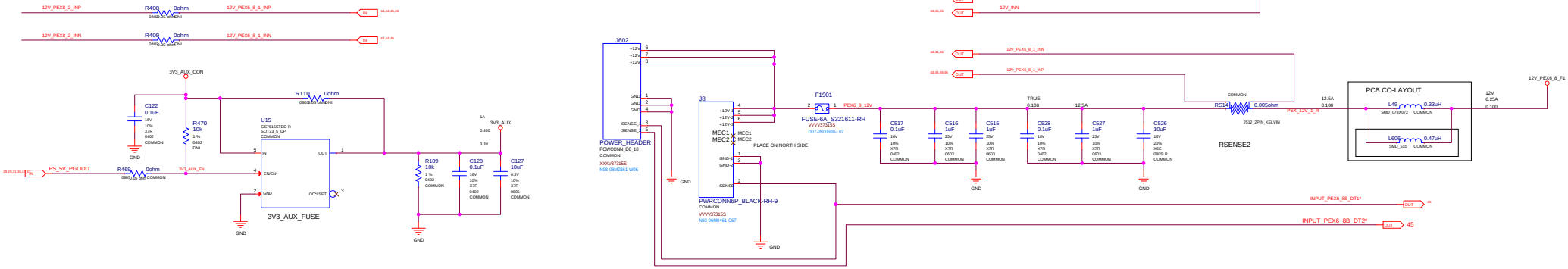
PEX 3V3 INPUT - 10W



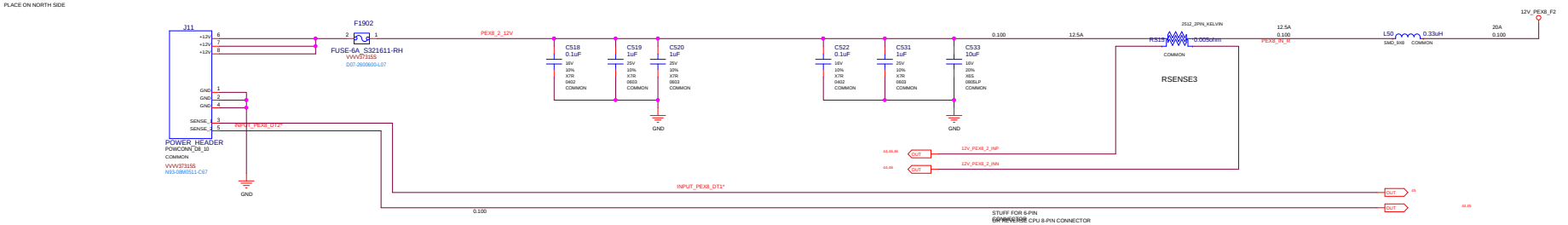
PEX_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



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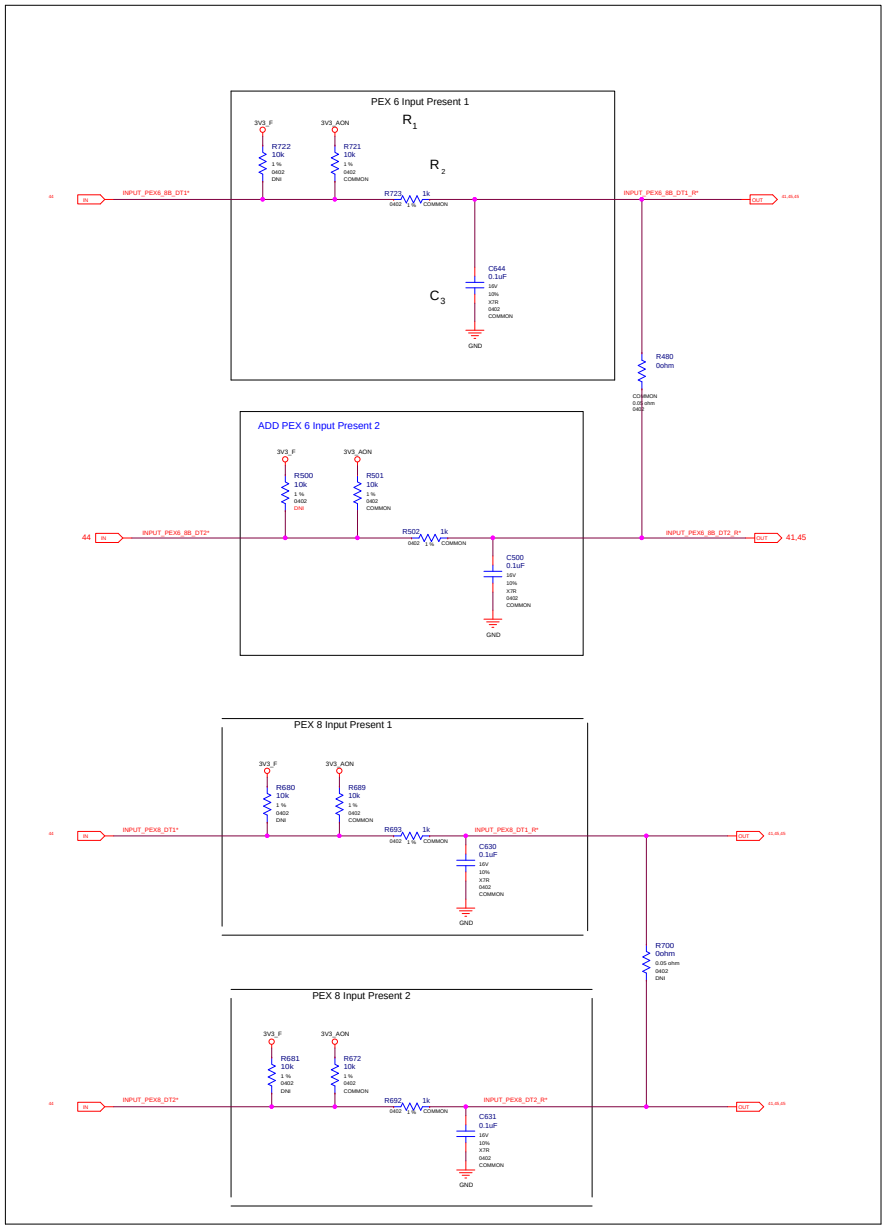
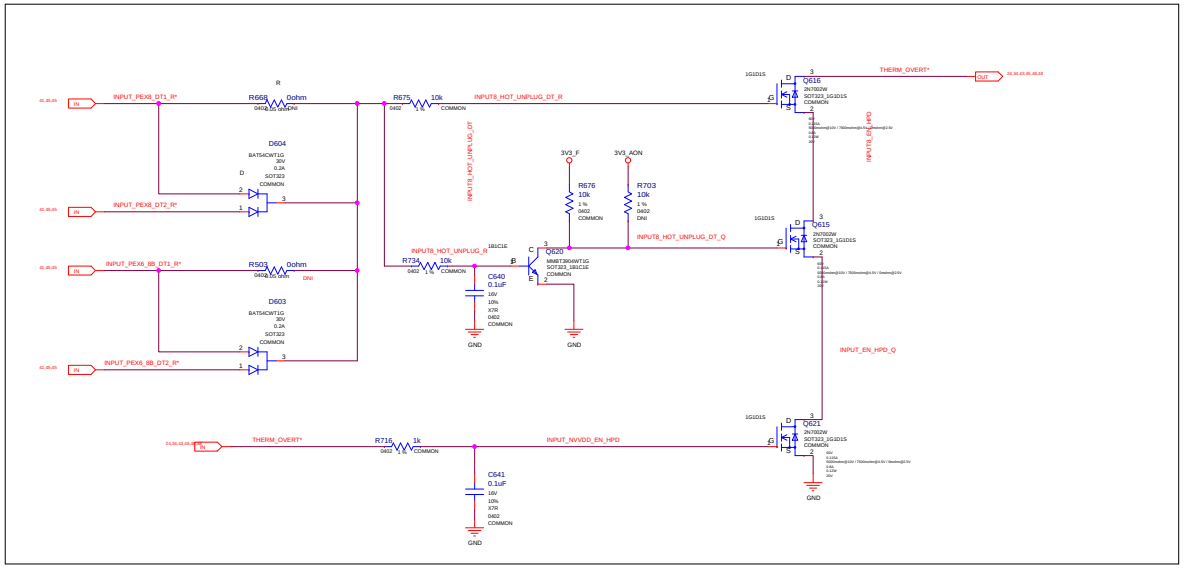
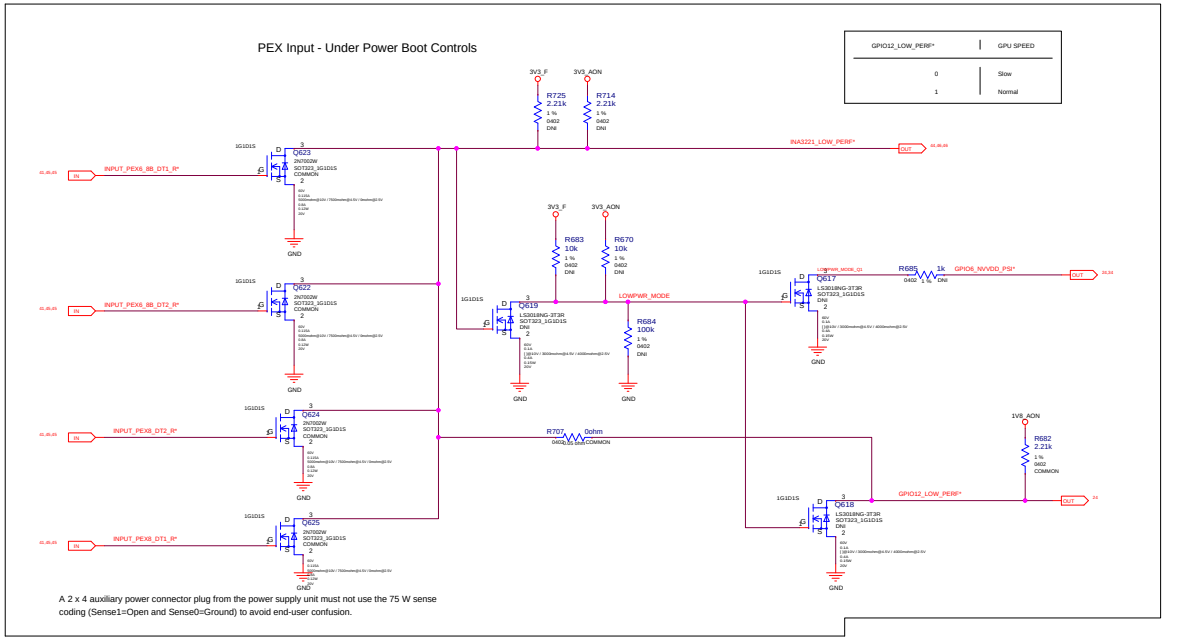
PAGE 45: PS: Current Steering, Hot Unplug Detect







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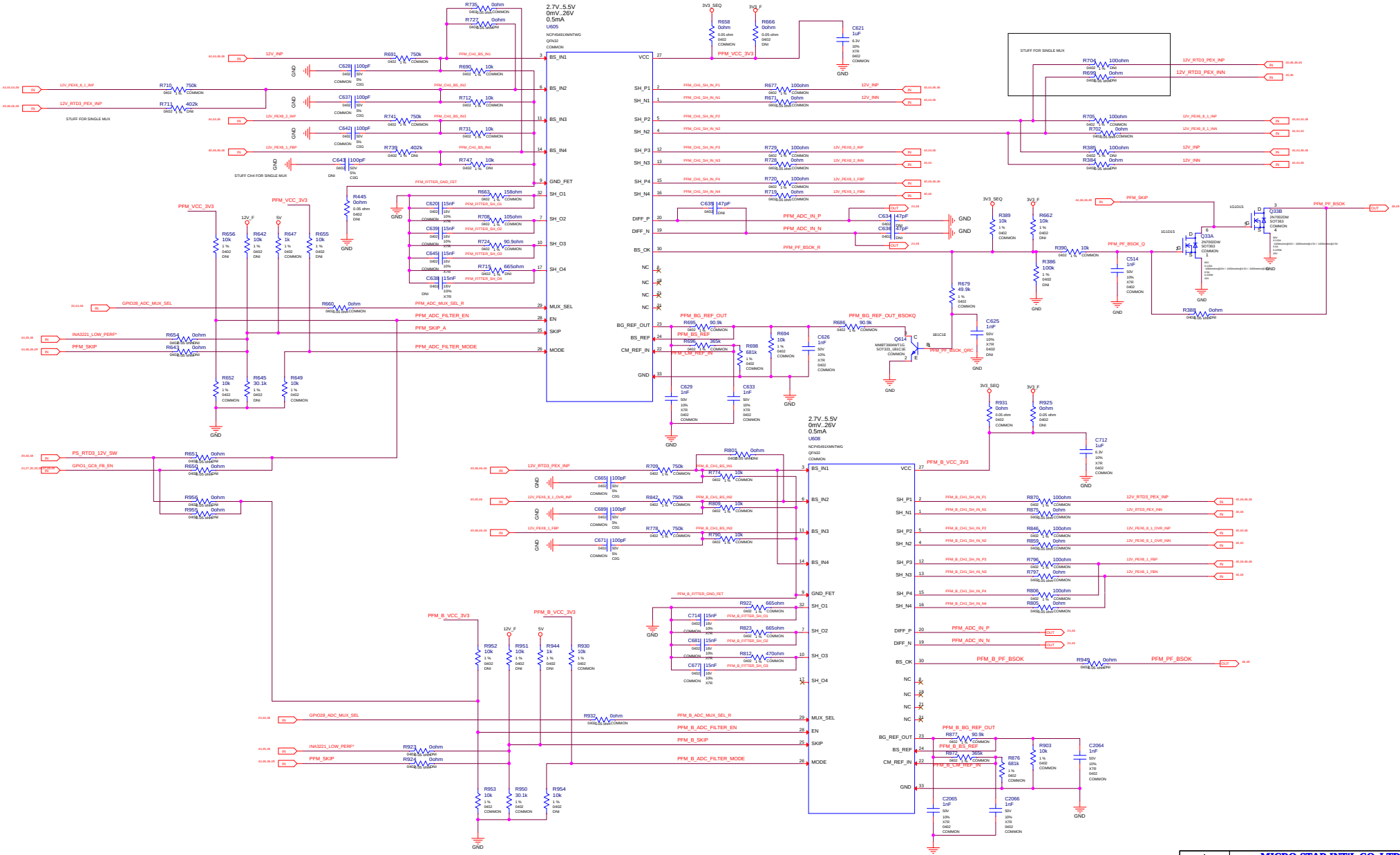
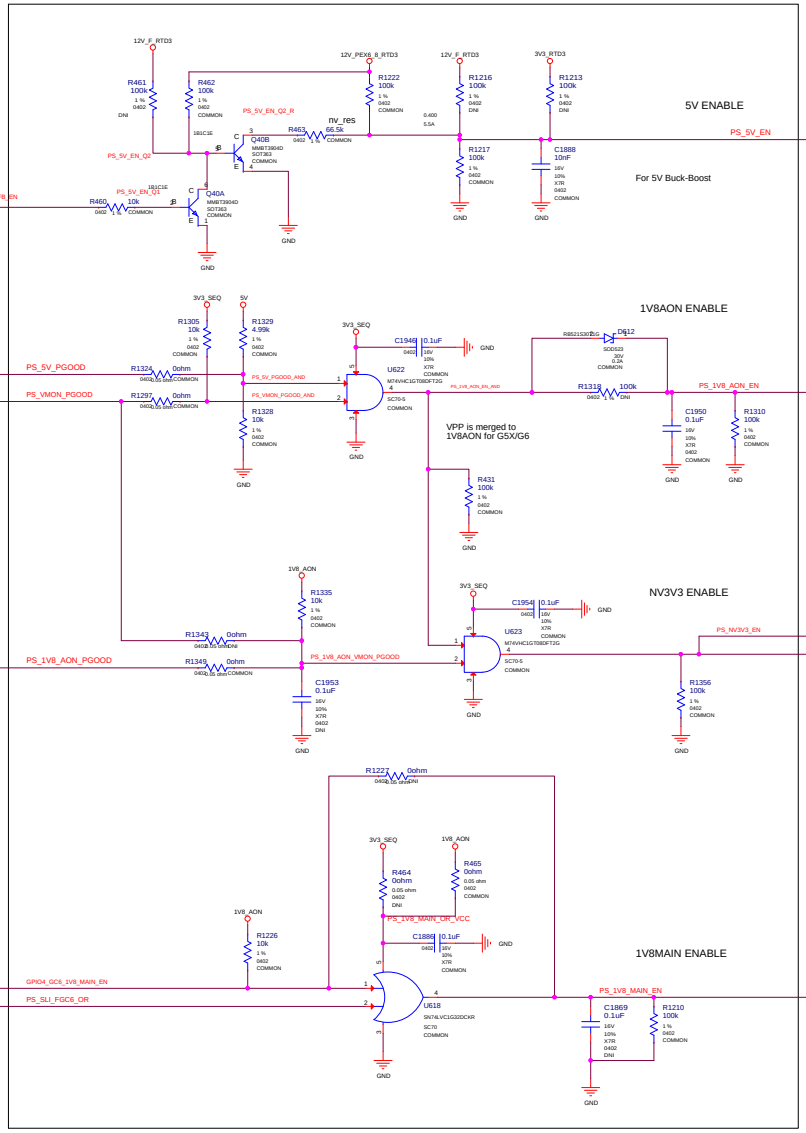
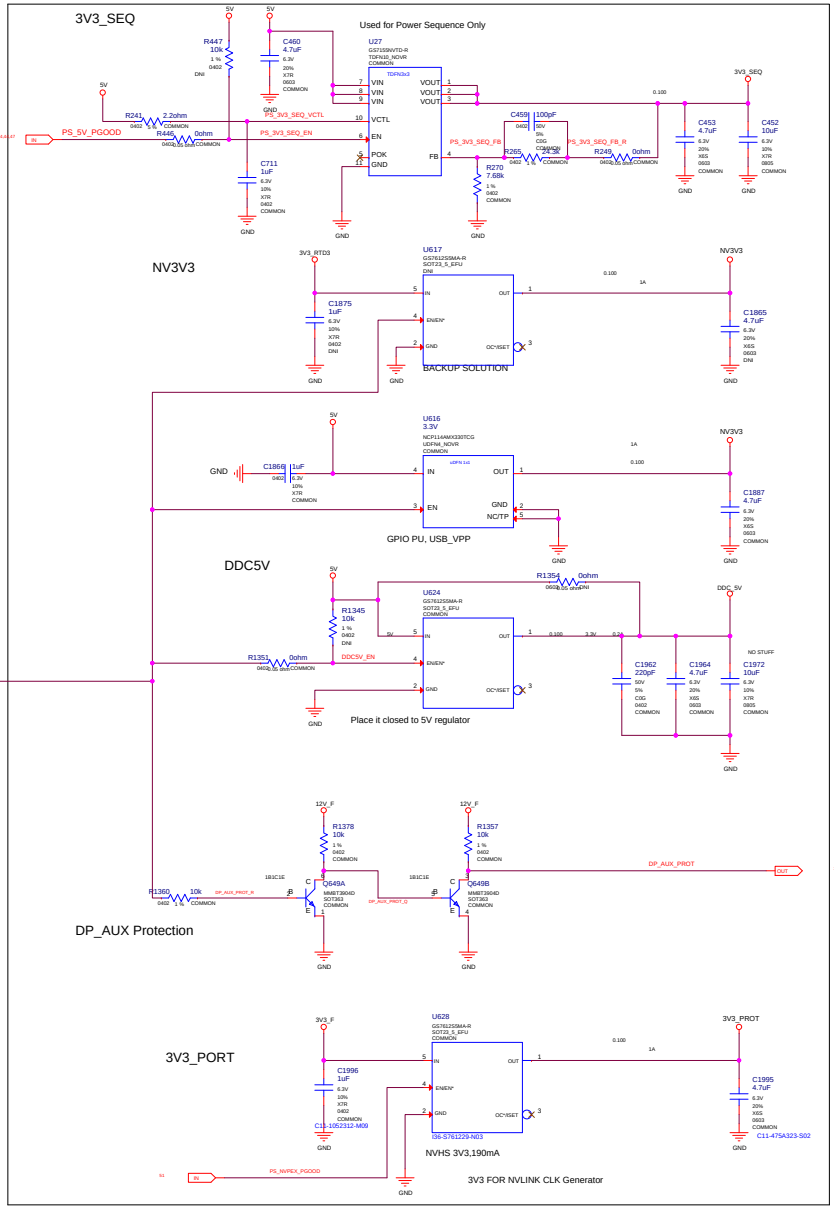
PAGE46; PS: Pre-Filter



PAGE 47: SEQUENCE:5V,1V8,NV3V3 ENABLE





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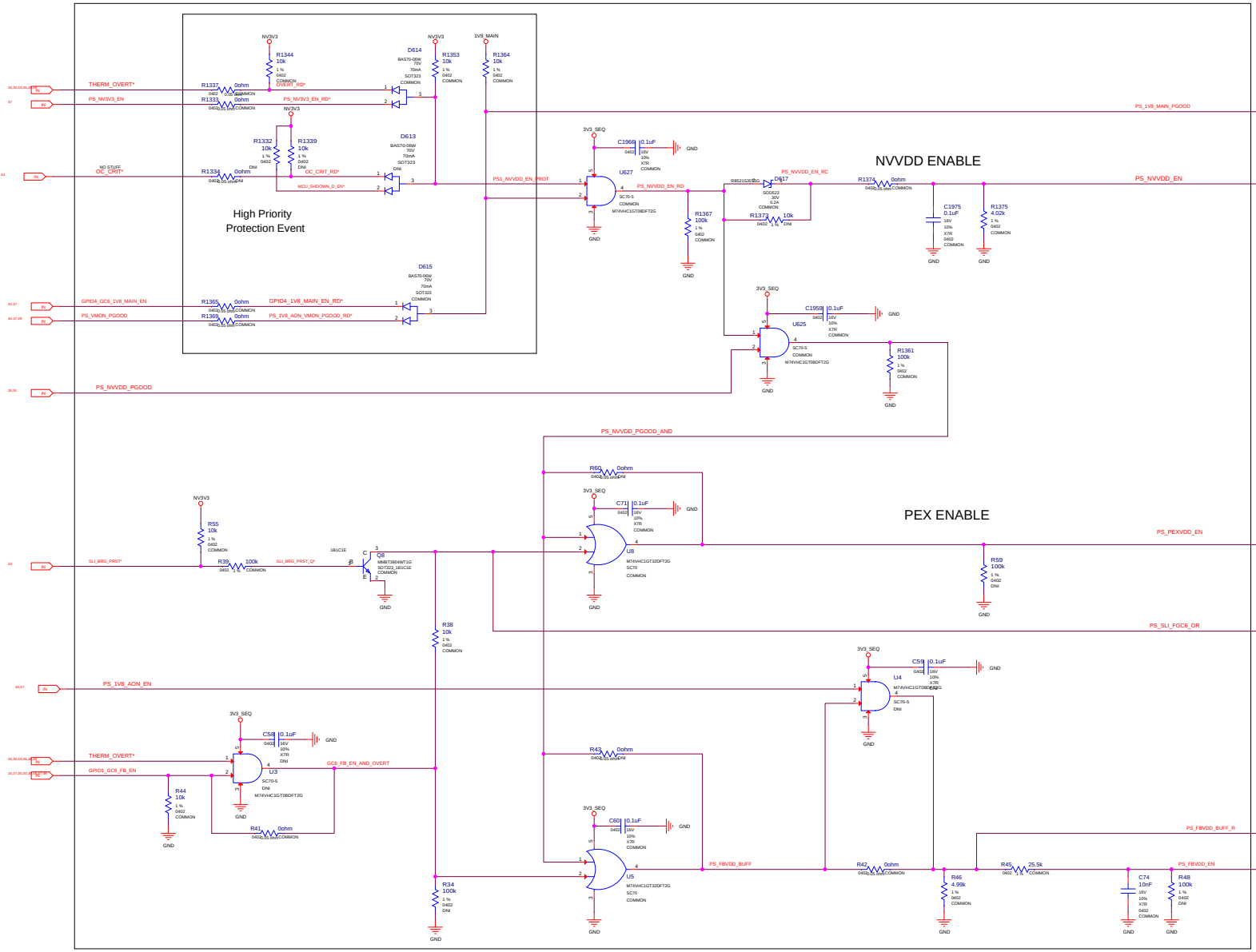
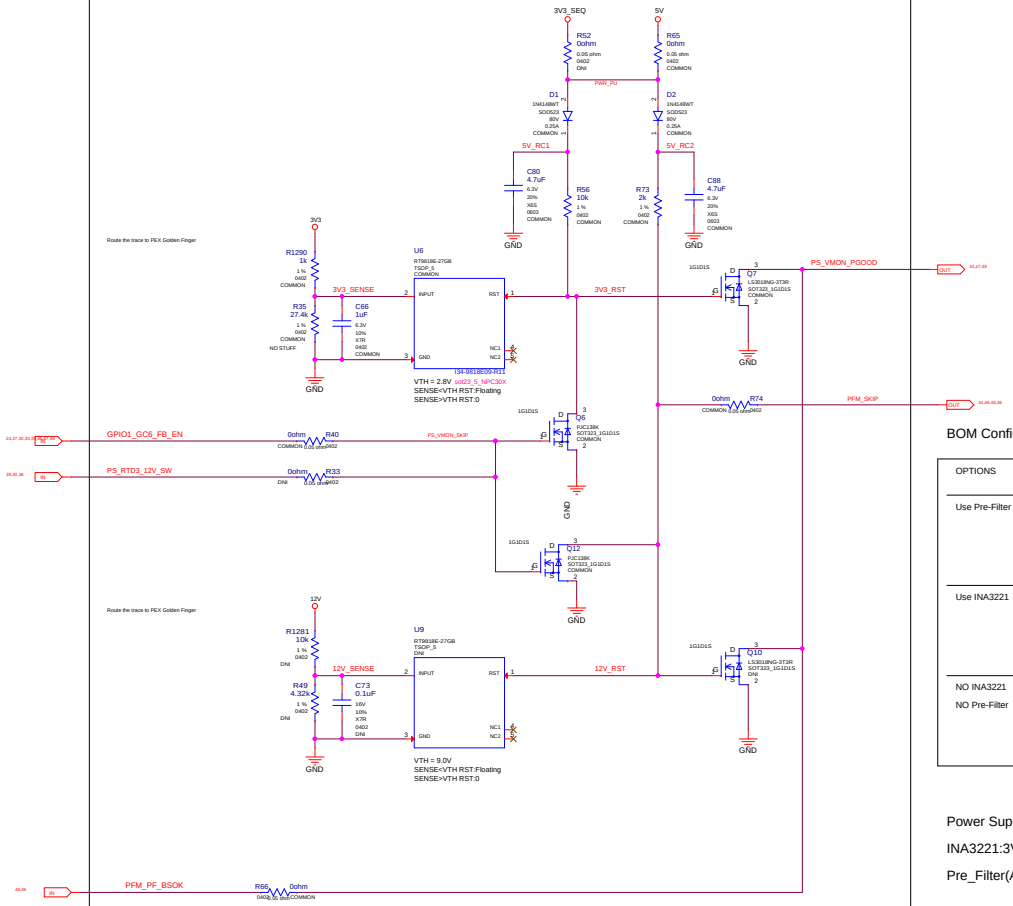
PAGE 48: SEQUENCE:NV,PEX,FB ENABLE



PCIE Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX

and All Input 12Vs

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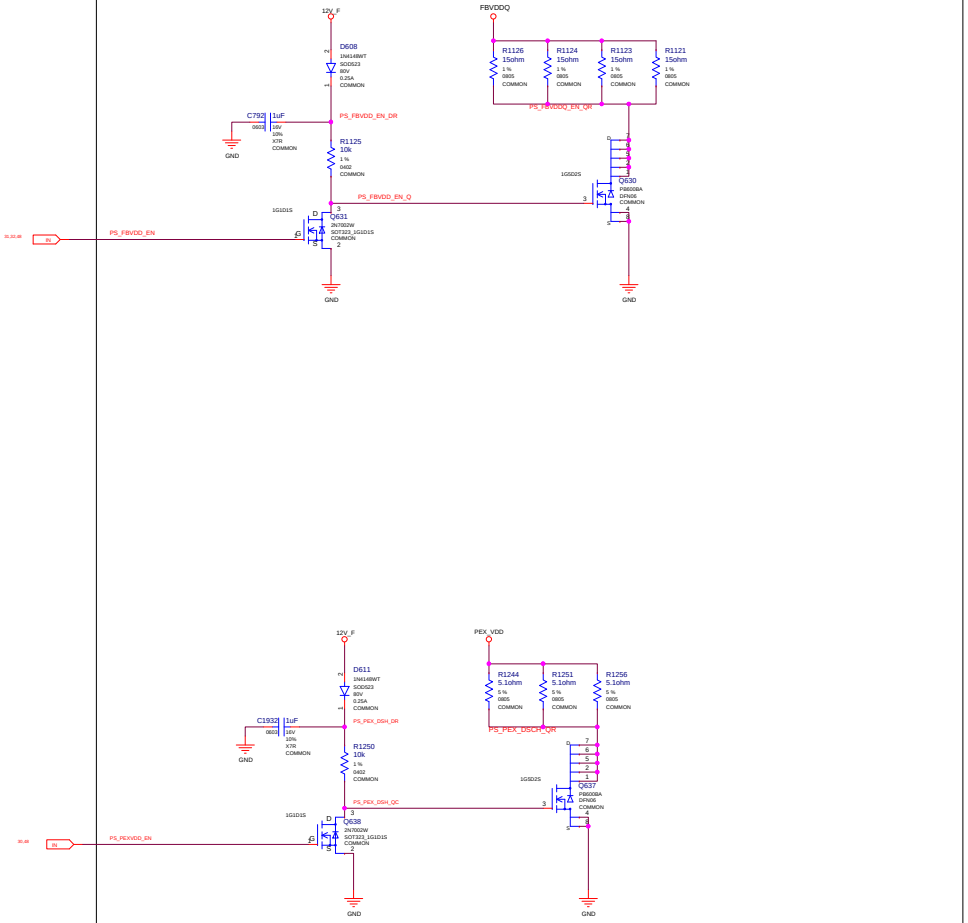
PAGE 50: SEQUENCE:DISCHARGE



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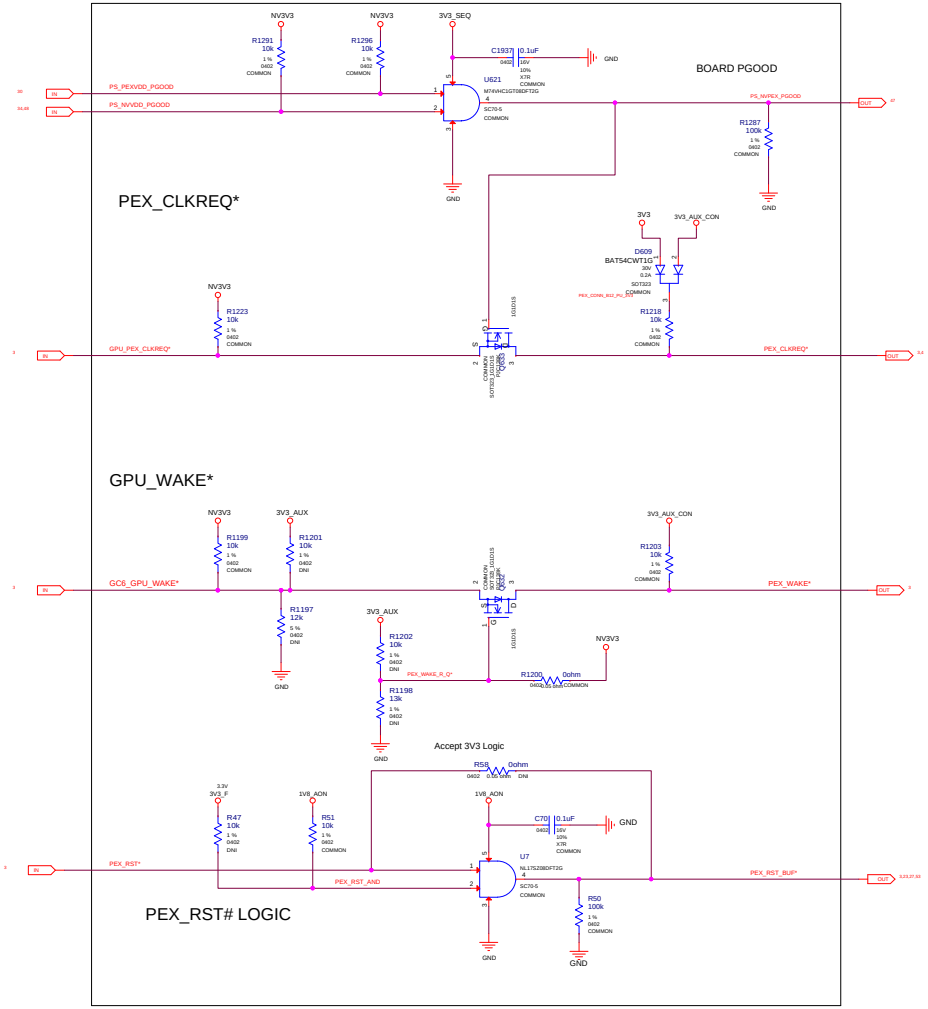
PAGE 51: SEQUENCE:MISC



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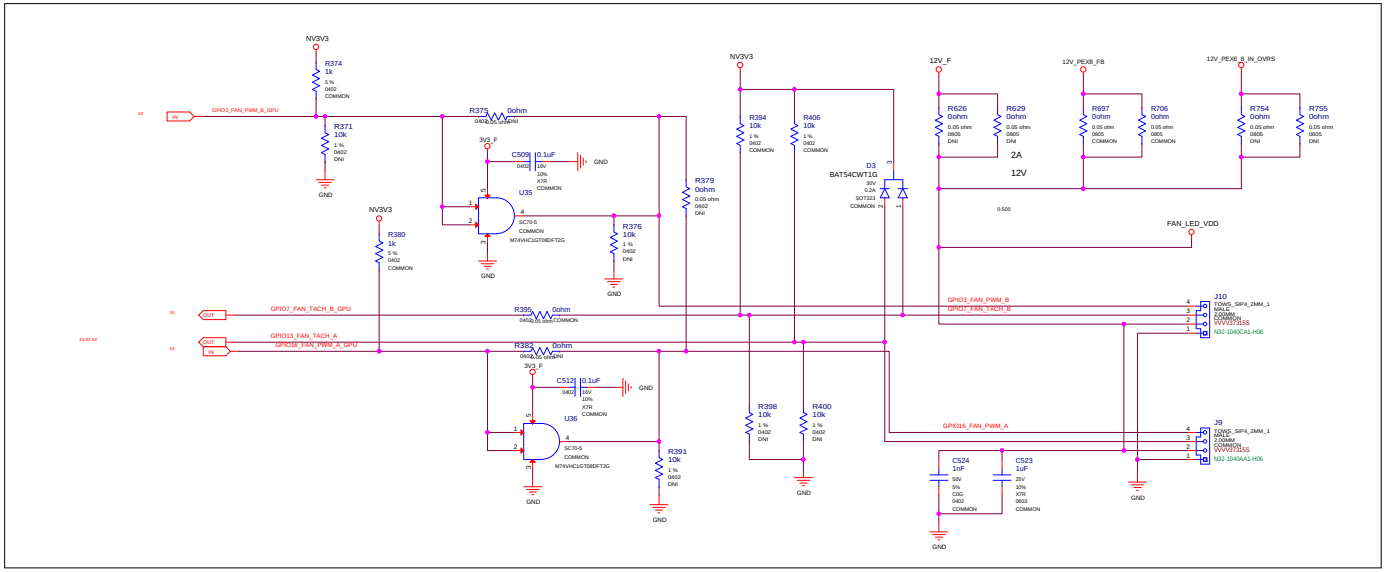
PAGE 52: LED & FAN HEADERS



LED BOOST

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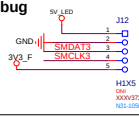
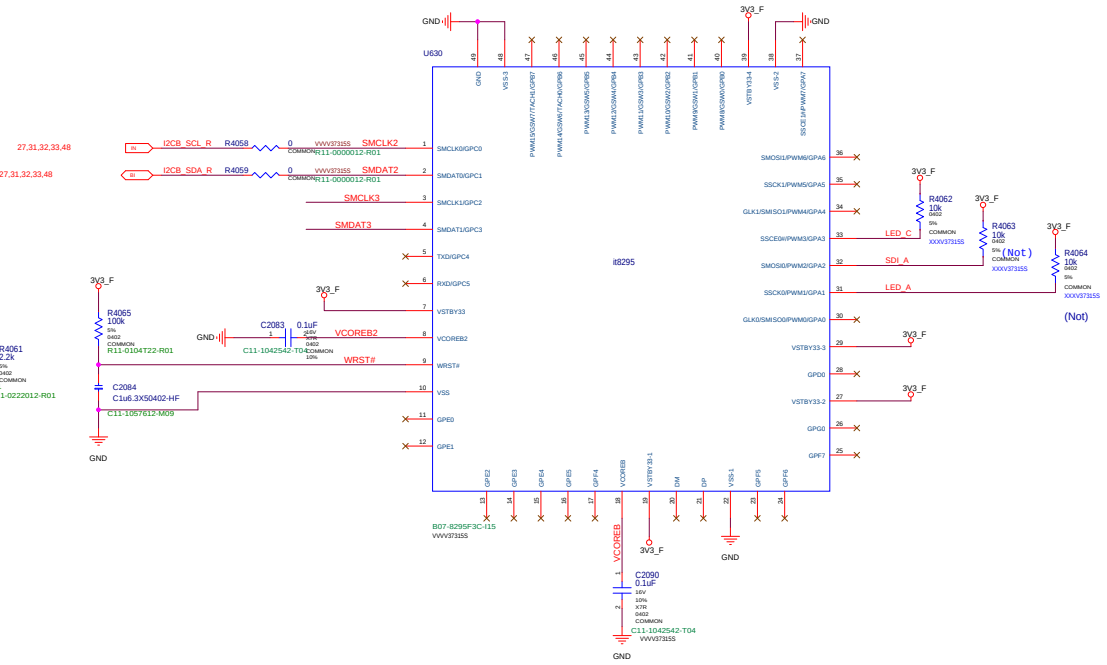
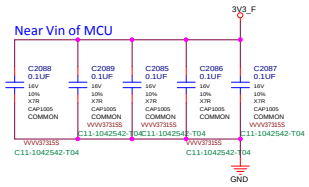
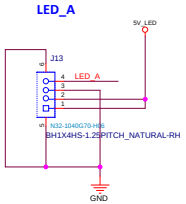
Firmware Programming

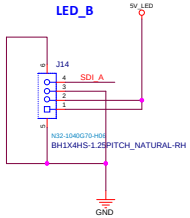
Debug

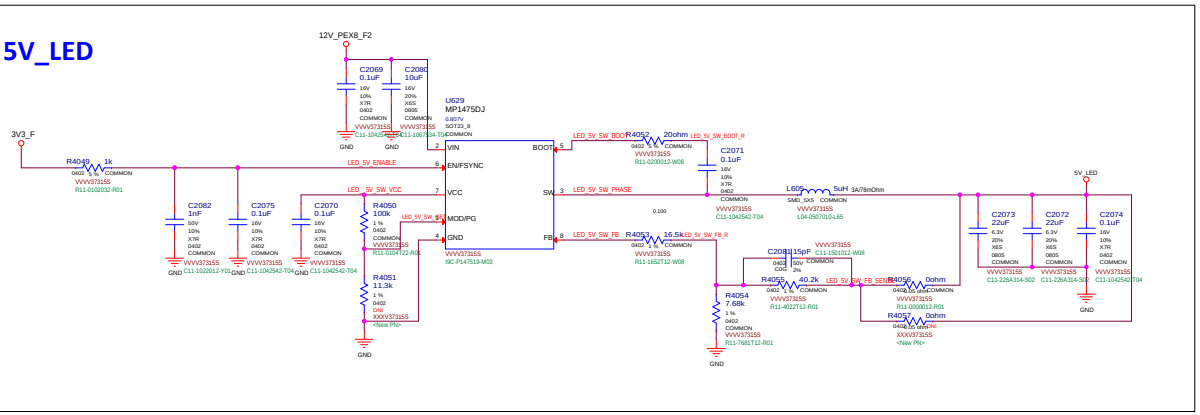












PAGE 54:MECHANICAL;BRACKET/THERMAL SOLUTION

FAN
STIFFNER
NO PINS
VVVV37315S
E32-0406170-K08

HS1
STIFFNER
NO PINS
XXXV37315S
OE3-V303002

HS2
STIFFNER
NO PINS
XXXV37315S
OE3-V320101

PCIE
STIFFNER
NO PINS
VVVV37315S
E24-V330020-P09

Screw

BKTSCREW1
VVVV37315S
E41-1304009-H75

BKTSCREW2
VVVV37315S
E41-1304009-H75

HDMISCREW1
VVVV37315S
E43-1303012-H75

TYPE-C
VVVV37315S
E43-1203040-P65

HI_DP
VVVV37315S
E43-1203040-P65

BOARD STIFFENER
No connected mounting pins
MEC501
Back Cover
NOPIN
DNI

Brackets:

BKT1
BRACKET
ATX_2X_2P
DNI
MECH MOUNTING ALL
GND

J18
impedence

J19
impedence

J17
X_PIN1*2

J16
X_PIN1*2

FM1 FM2 FM3 FM4
FM5 FM6 FM7 FM8
OPT
F_PAD_X

PCB
PCB
109-GN982-00A
COMMON
VVVV37315S
PD0-0V37320-E48

HDMI_FEE
HDMI
$$$$$$
HDMI_FEE
COMMON
VVVV37315S
Y01-RHDM003-000

GPU Socket Symbol
BGA SOCKET ASSY
12 connected mounting pins
MEC3
SOCKET_BGA
128PIN
DNI
GND

GPU Mounting holes
MEC4-1
MEC4-2
MEC4-3
MEC4-4
MEC4-5
MEC4-6
MEC4-7
MEC4-8
D18X
X8
DNI
GND

STIFFENER

Mechanical Holes Symbol

MEC10 MEC11 MEC12 MEC13 MEC14
MEC15 MEC16 MEC17 MEC18 MEC19
H_R220D125
GND

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