

PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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NV_PN

600-1G180-BASE-200

PCB REV

PG180-A02

BOM REV

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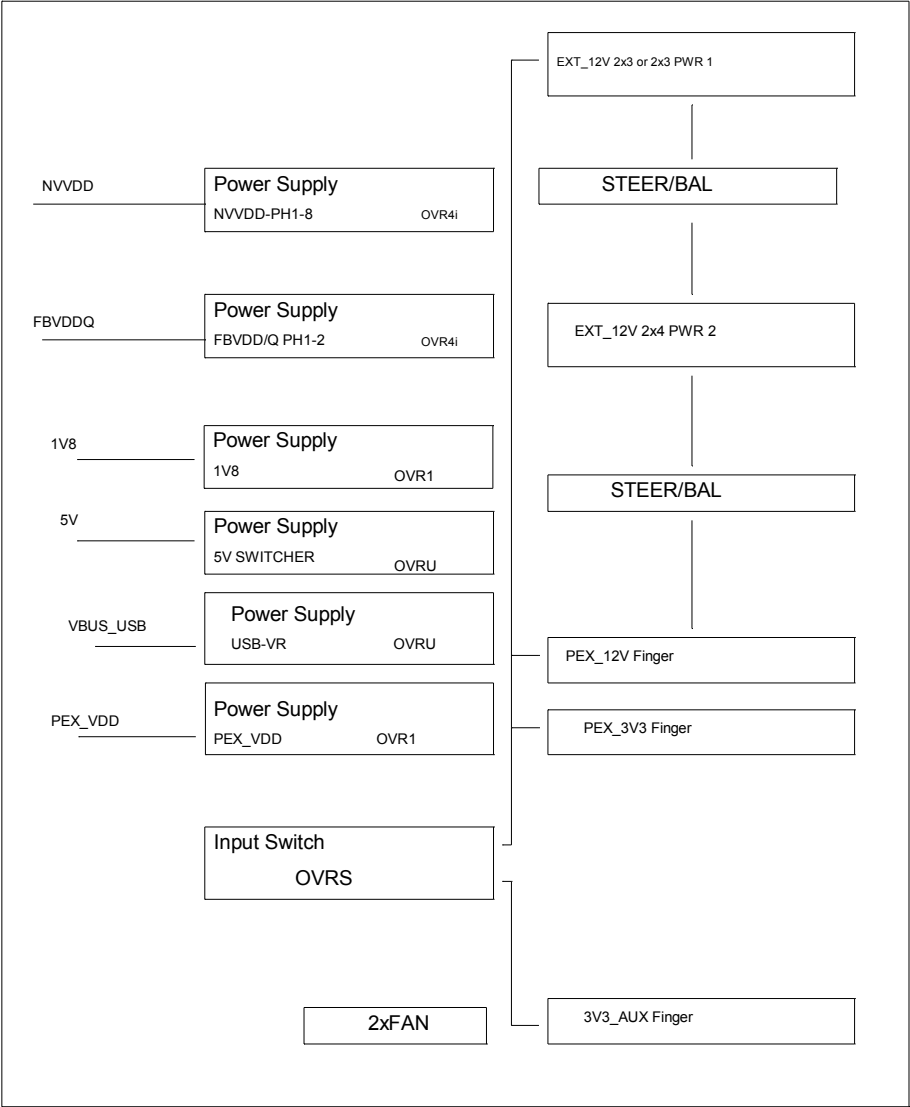
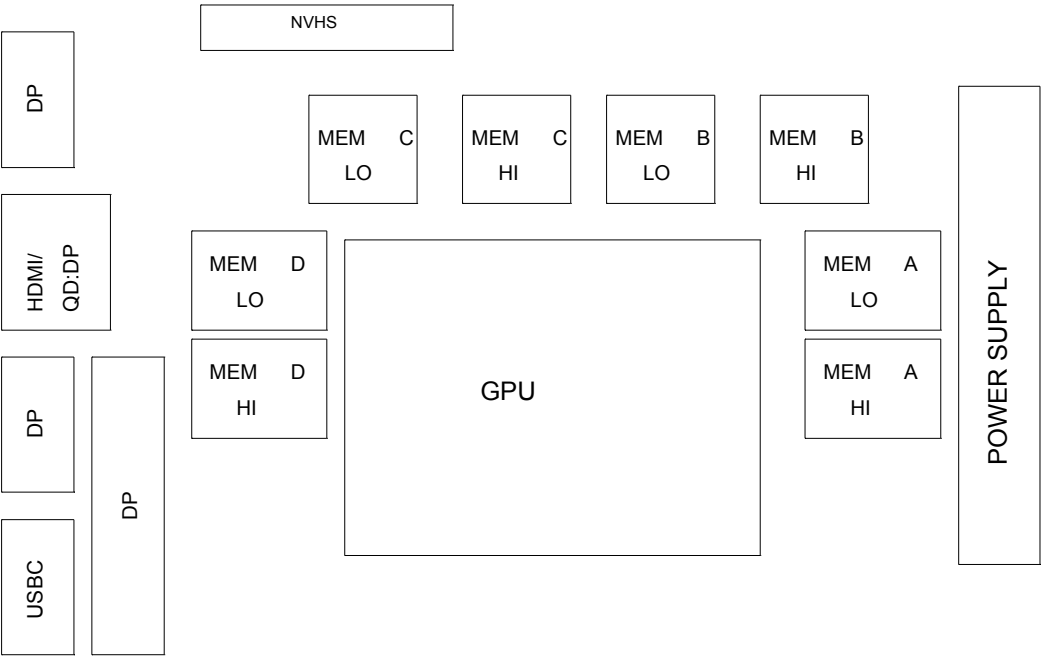
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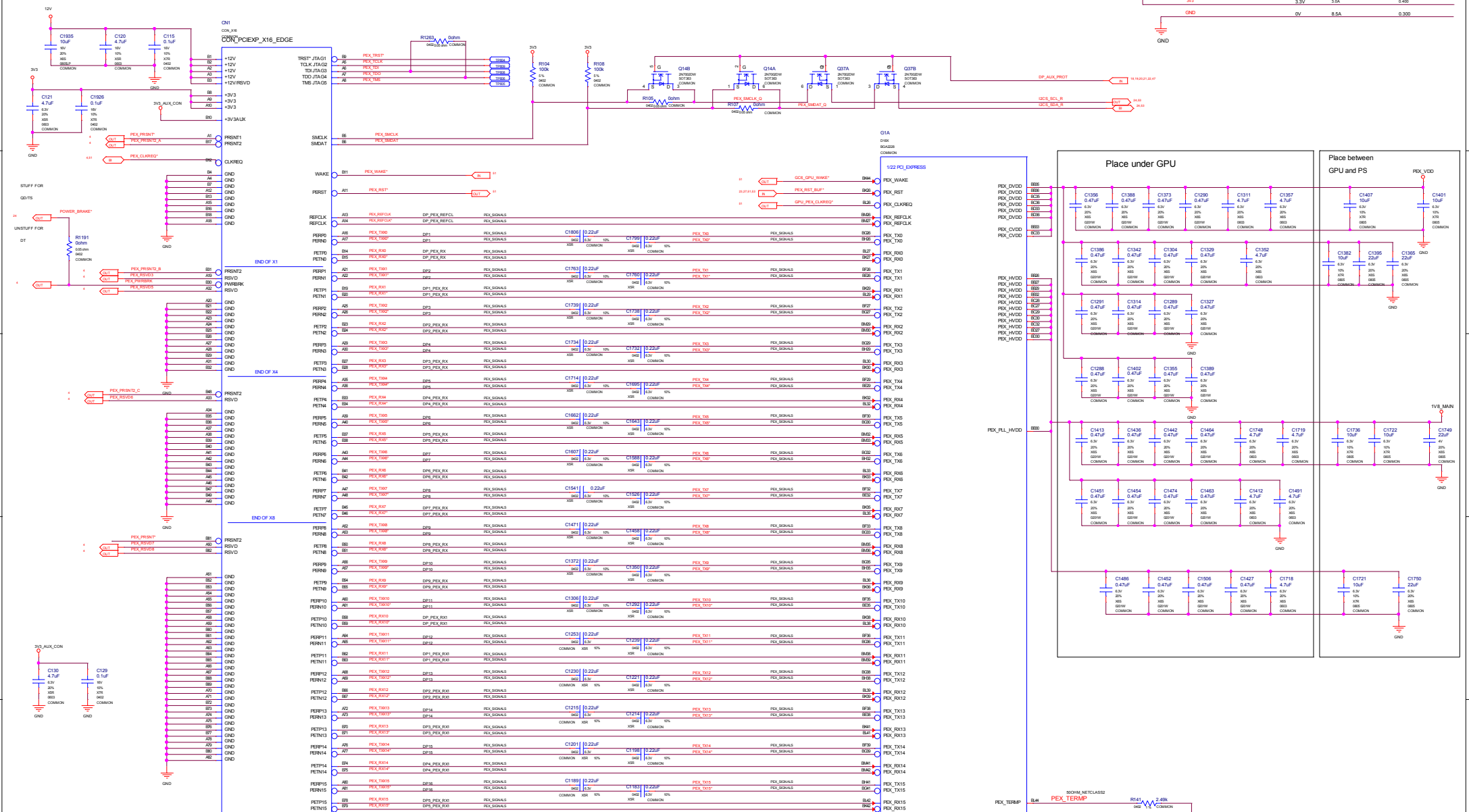


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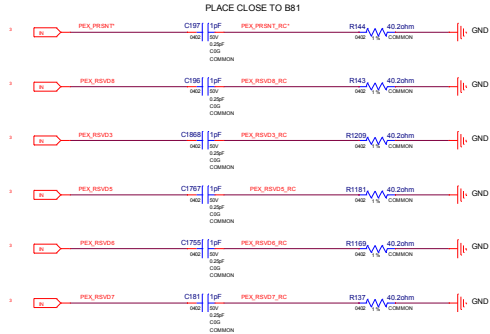
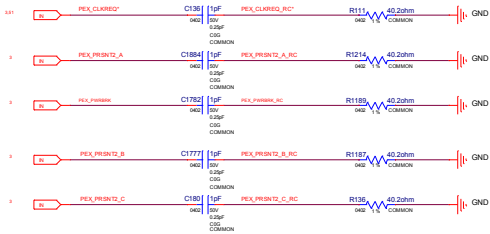
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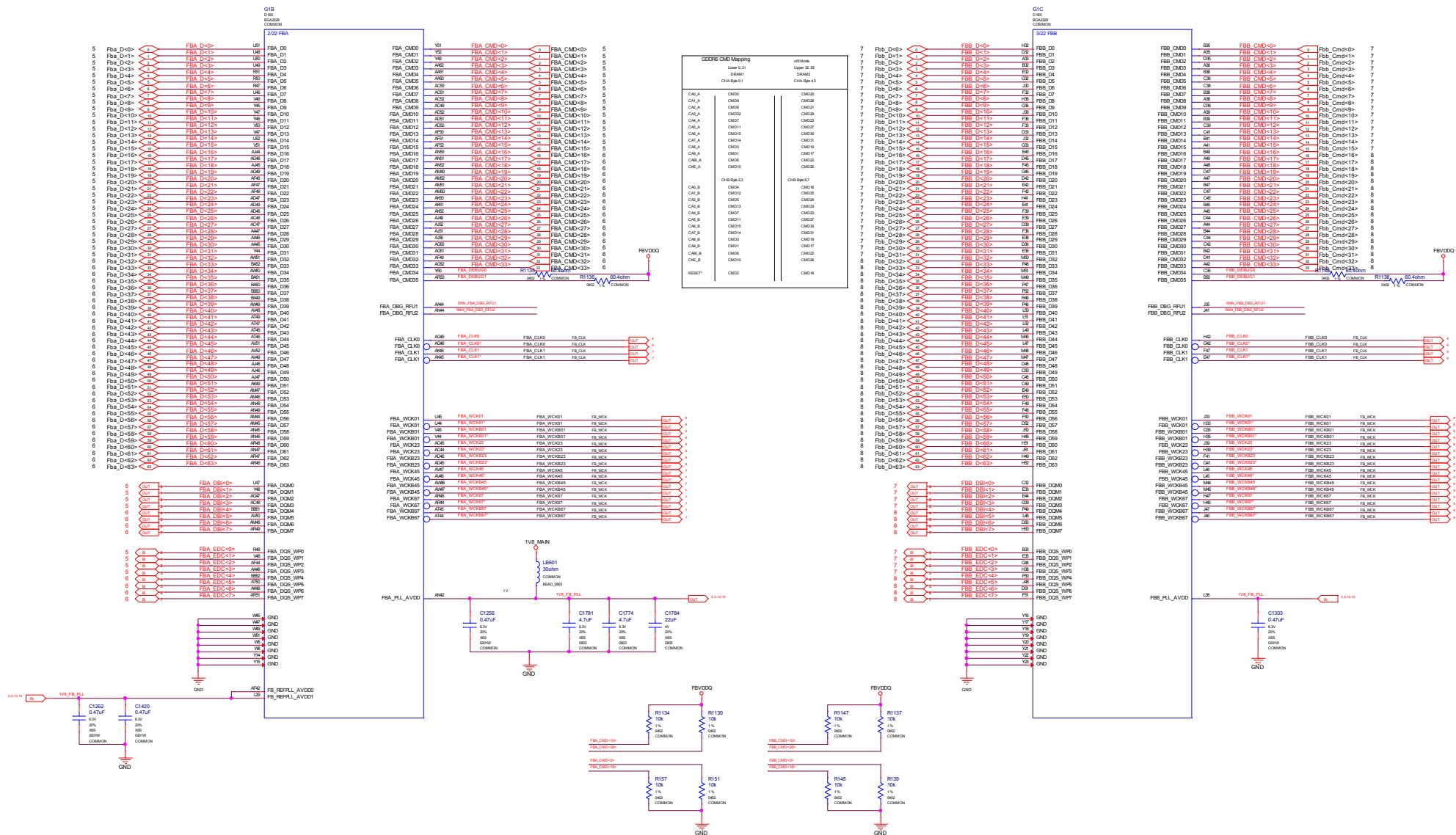
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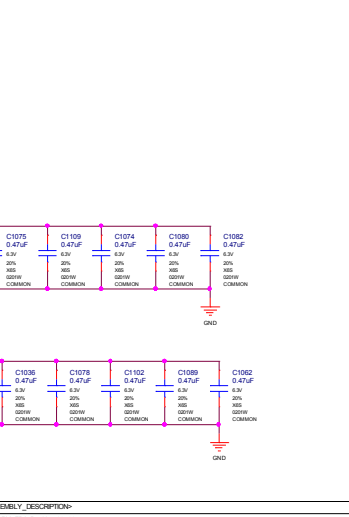
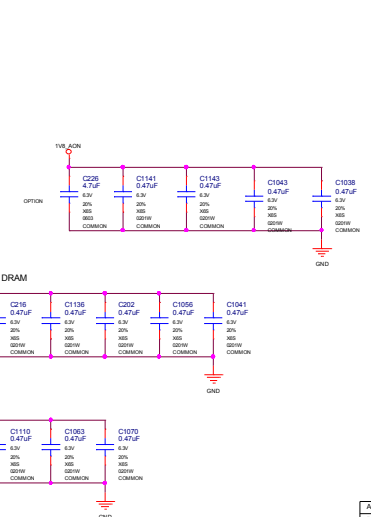
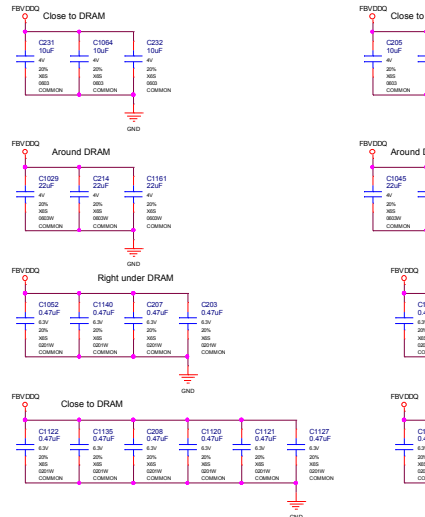
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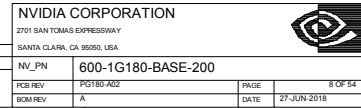
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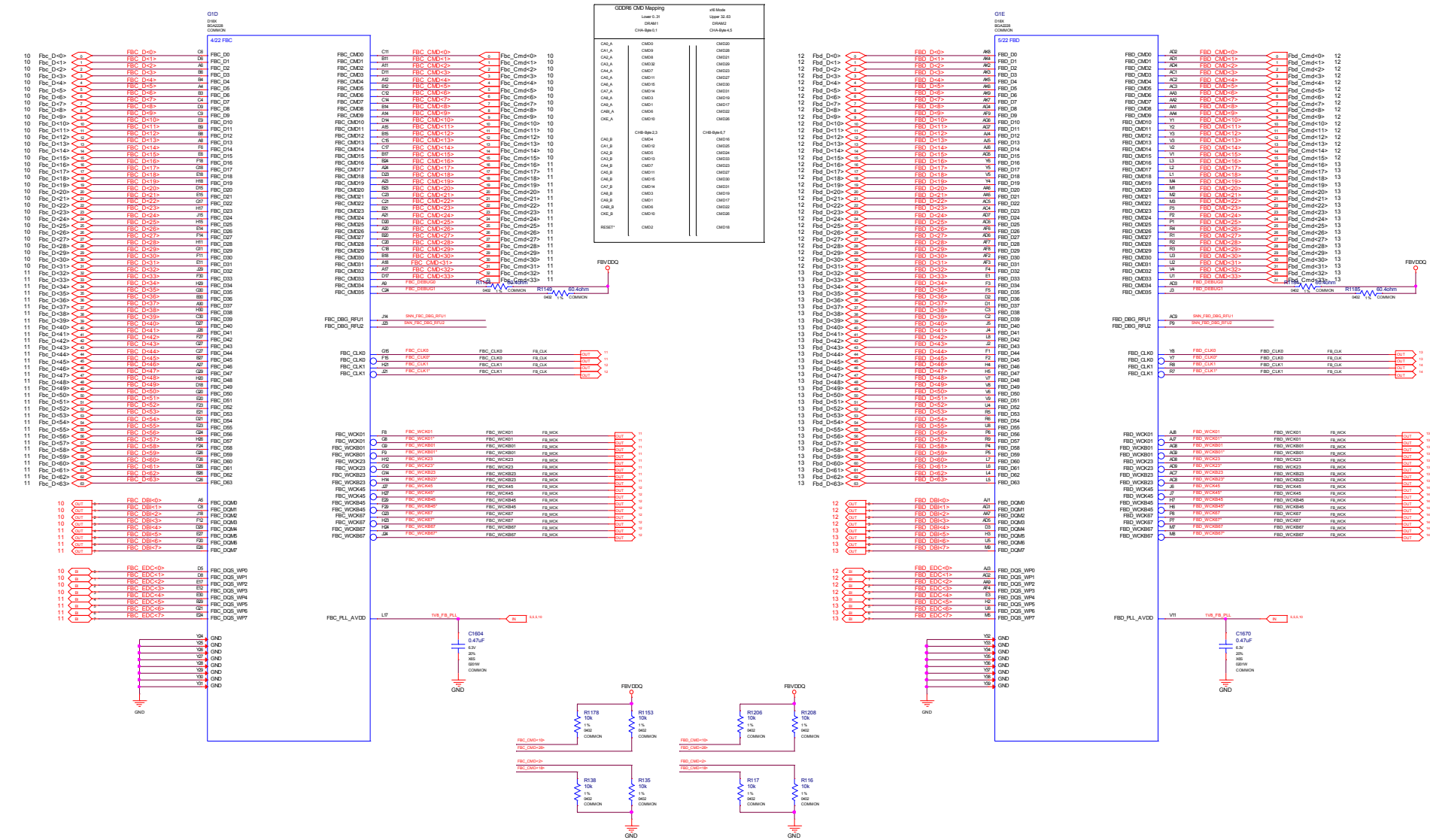


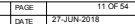
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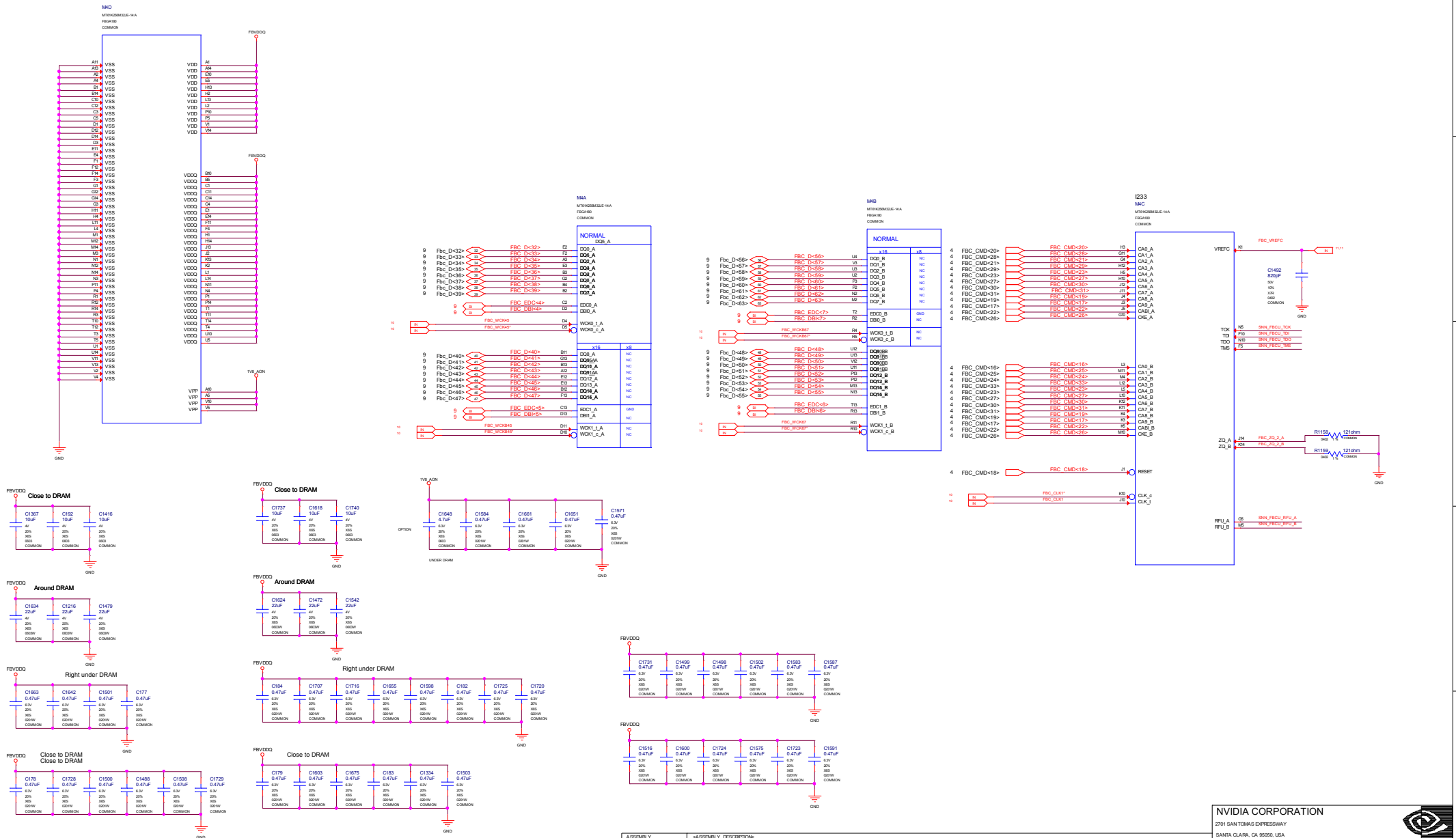




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PAGE DETAIL	MEMORY: FBB Partition 31.0







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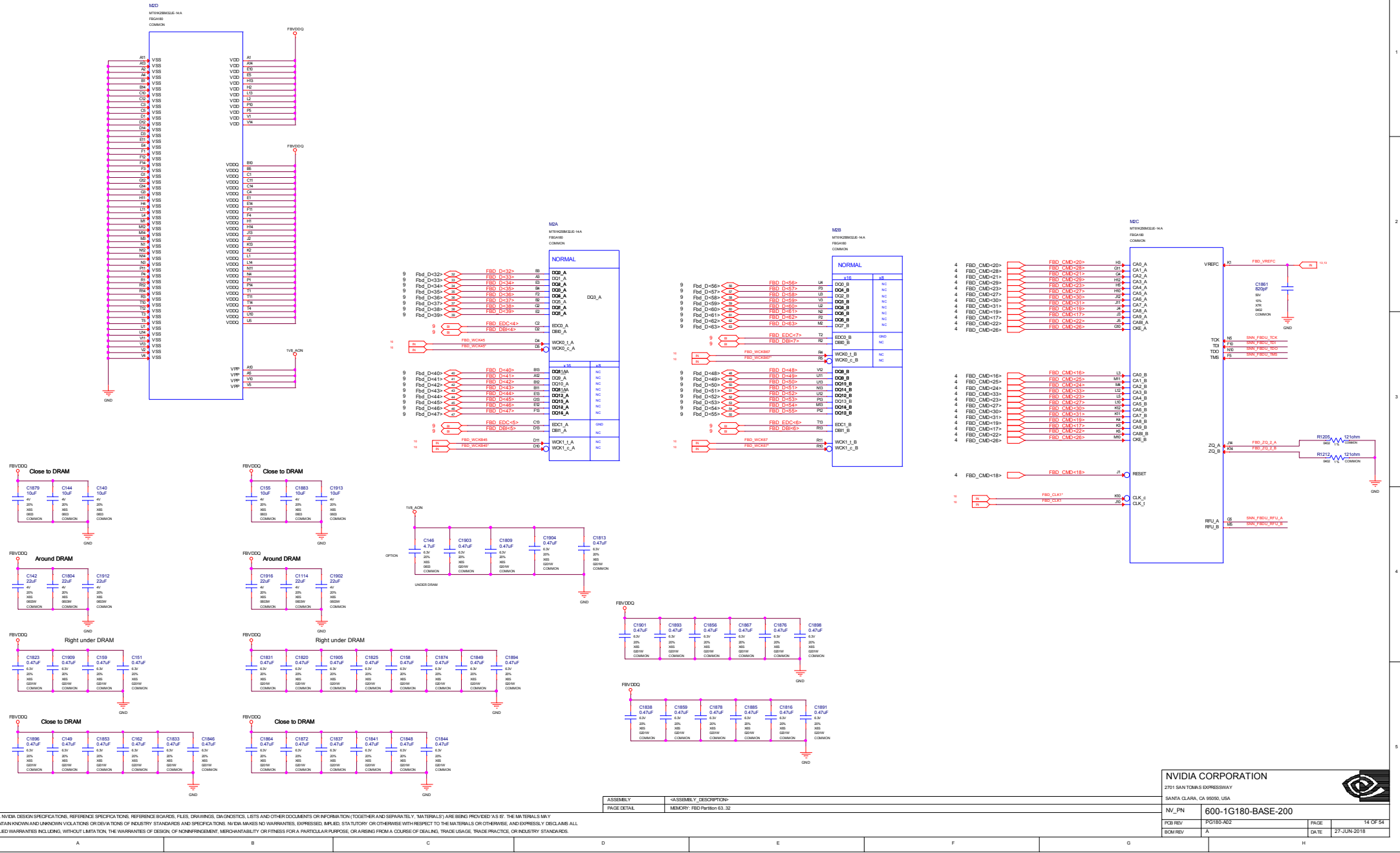
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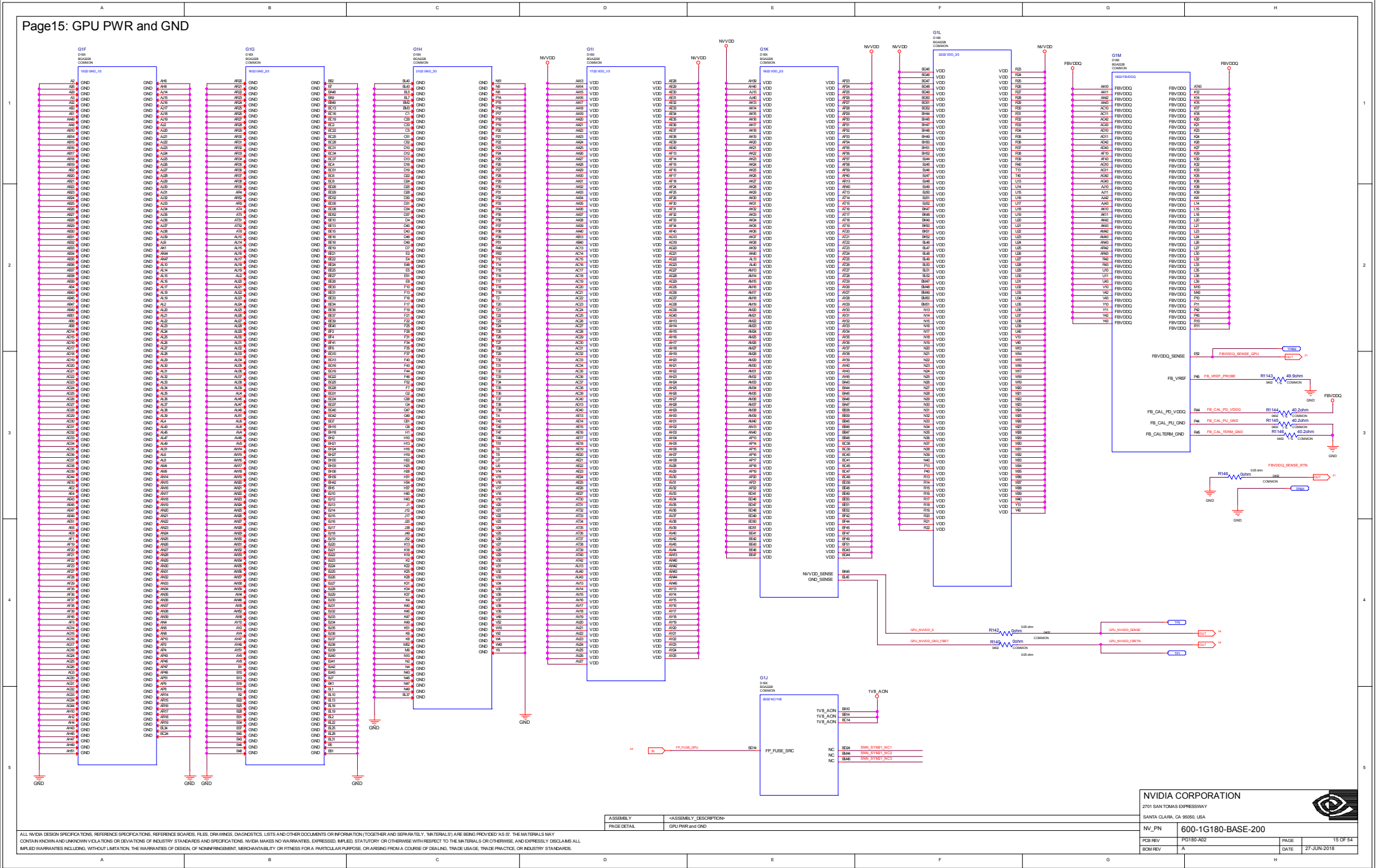
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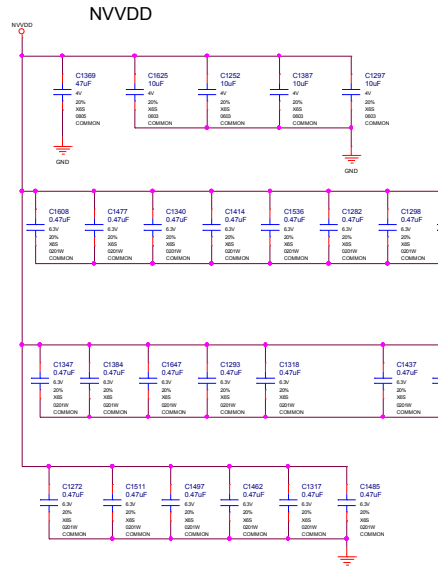
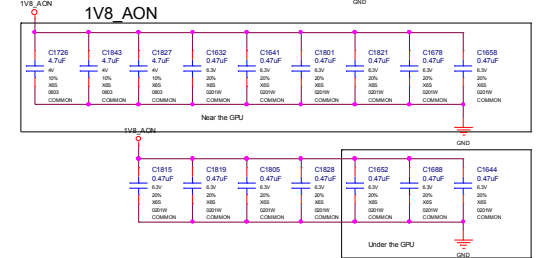
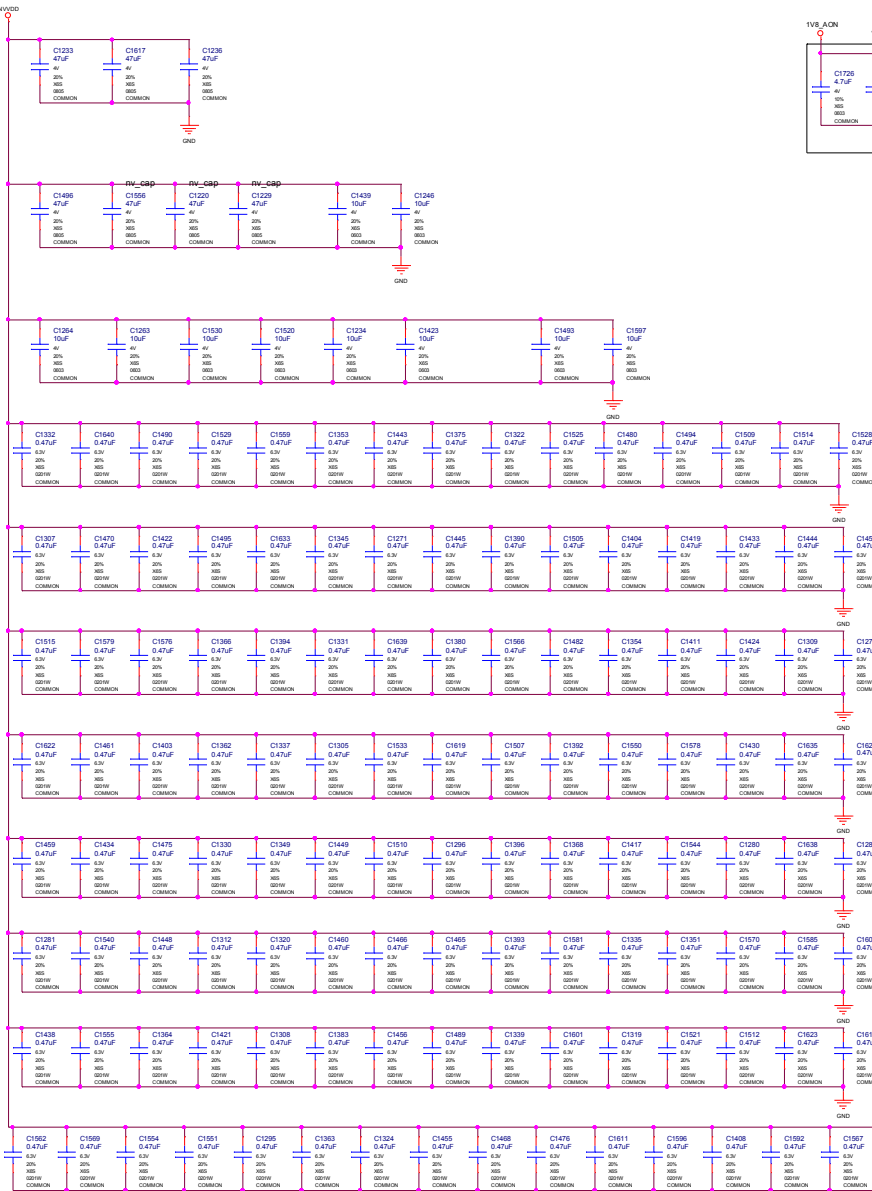
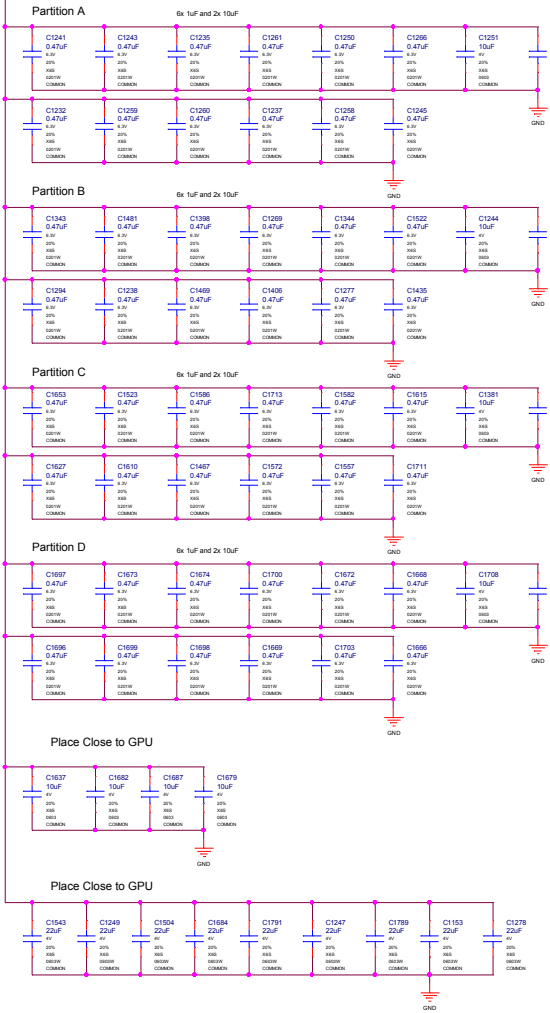
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NVDD

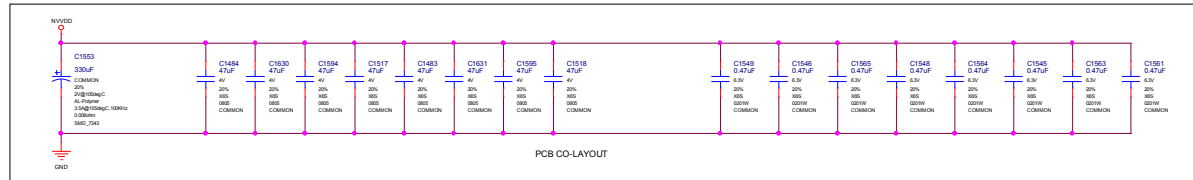
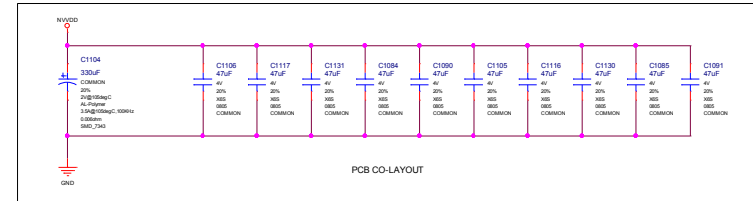
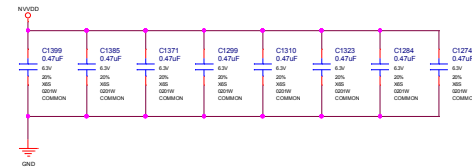
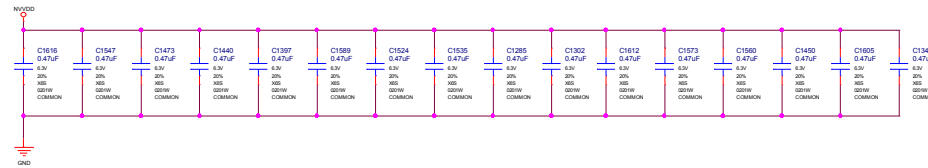
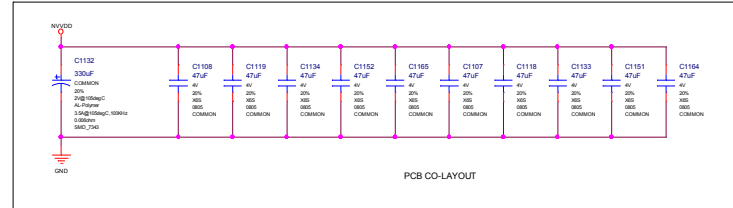
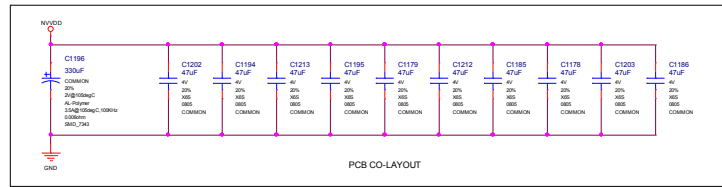
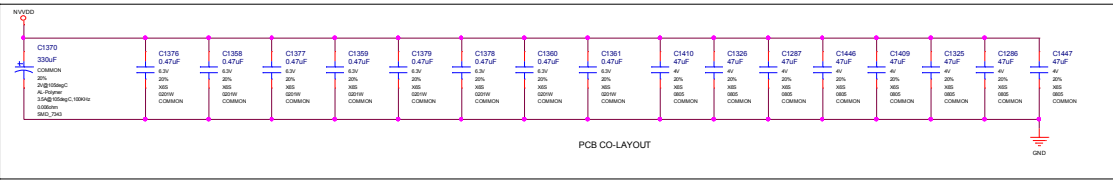
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ASSEMBLY	ASSEMBLY DESCRIPTION
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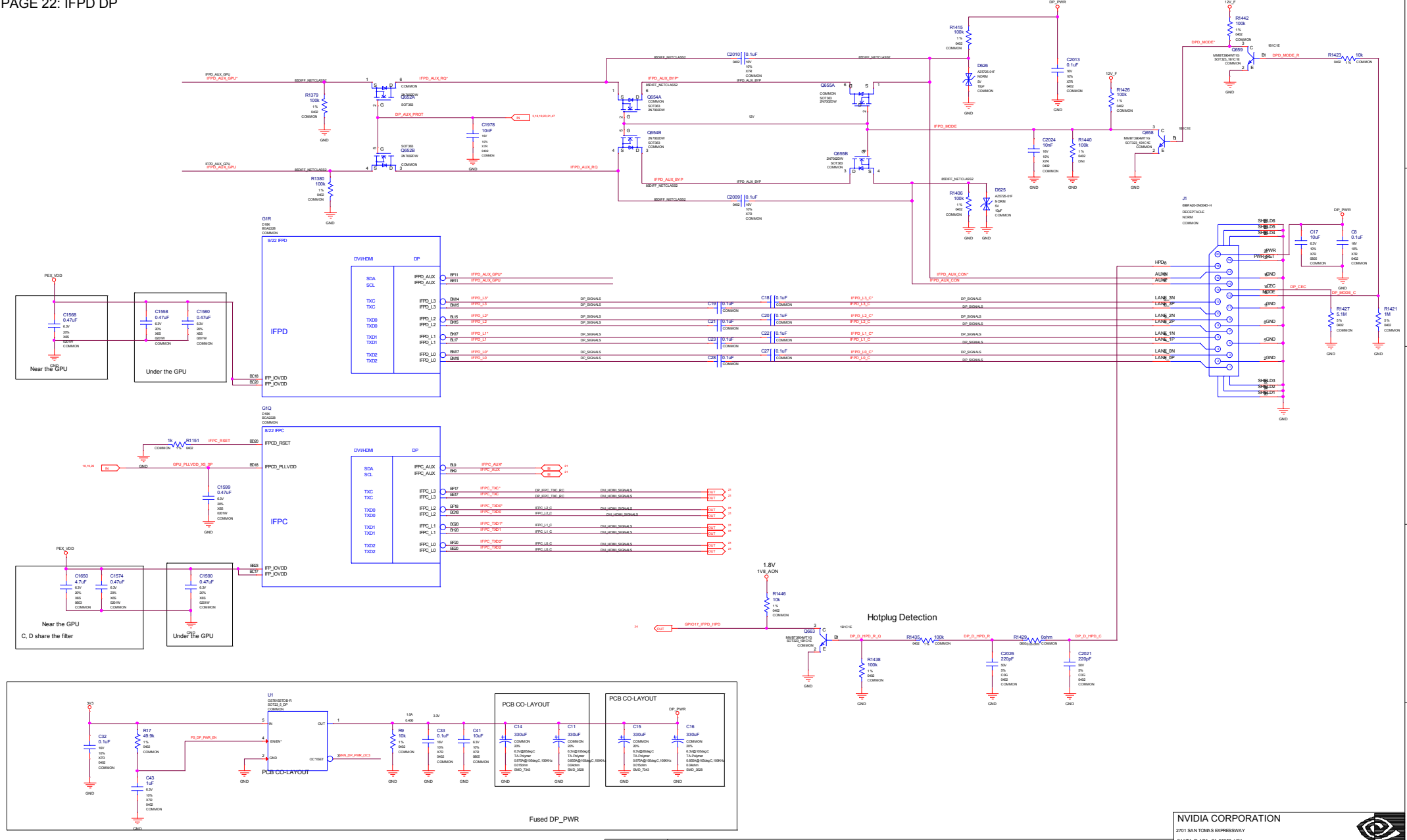
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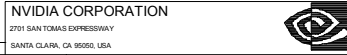
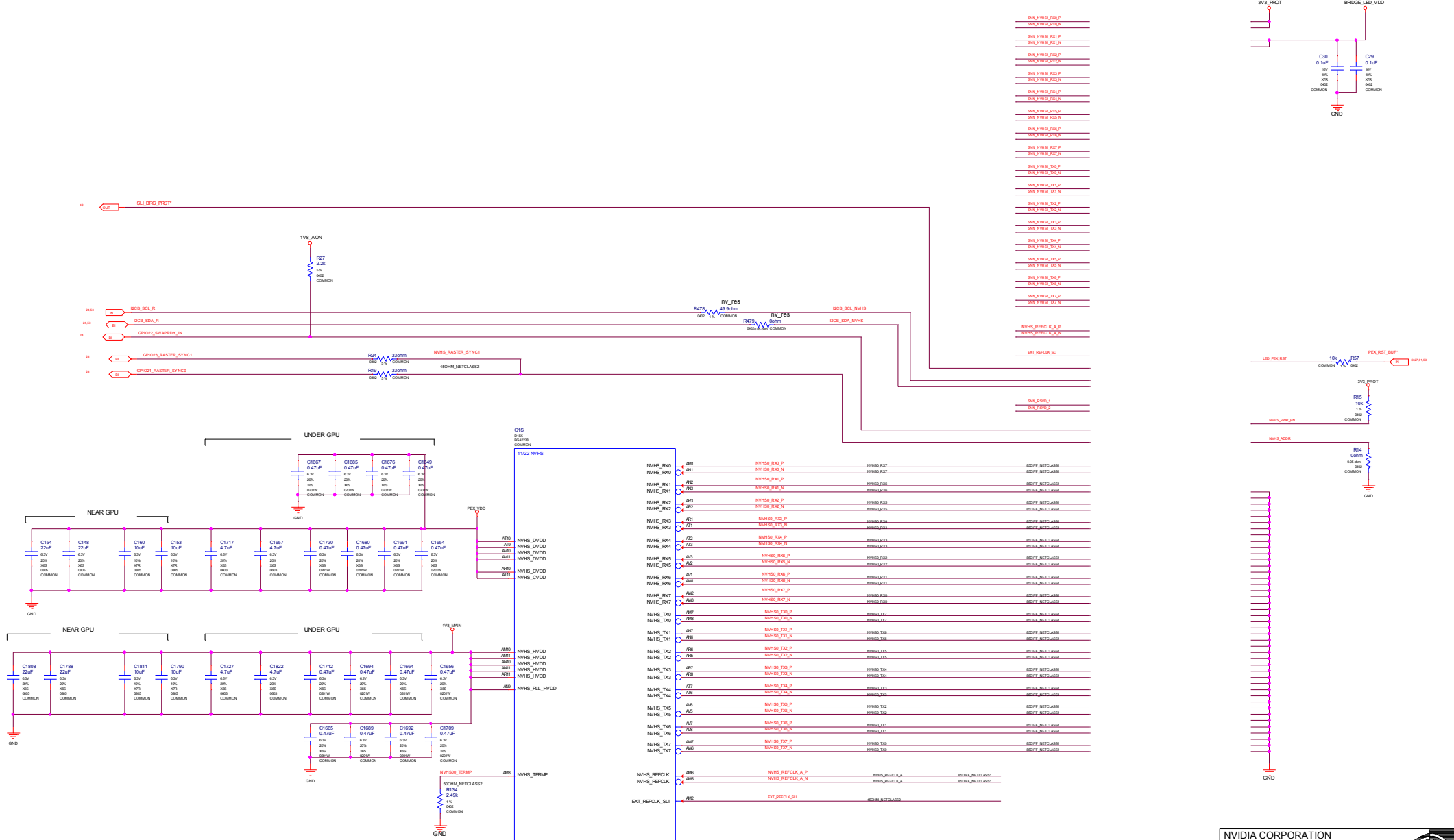
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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	NVHS INTERFACE

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
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1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

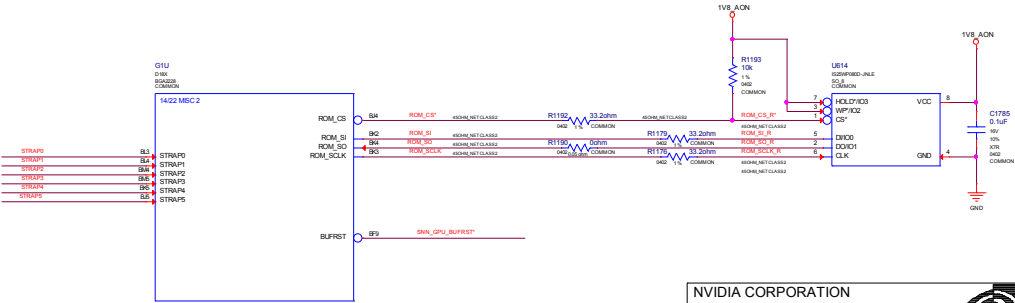
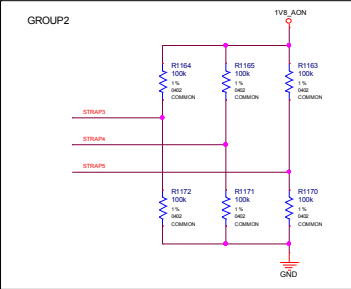
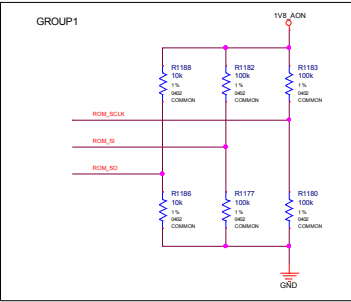
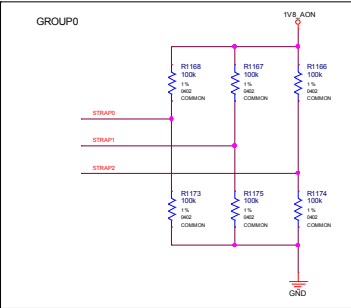
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Default

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE:DETAIL	MISC3: ROM STRAPS

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NV_PN

600-1G180-BASE-200

PCB REV

PG180-A02

ROM REV

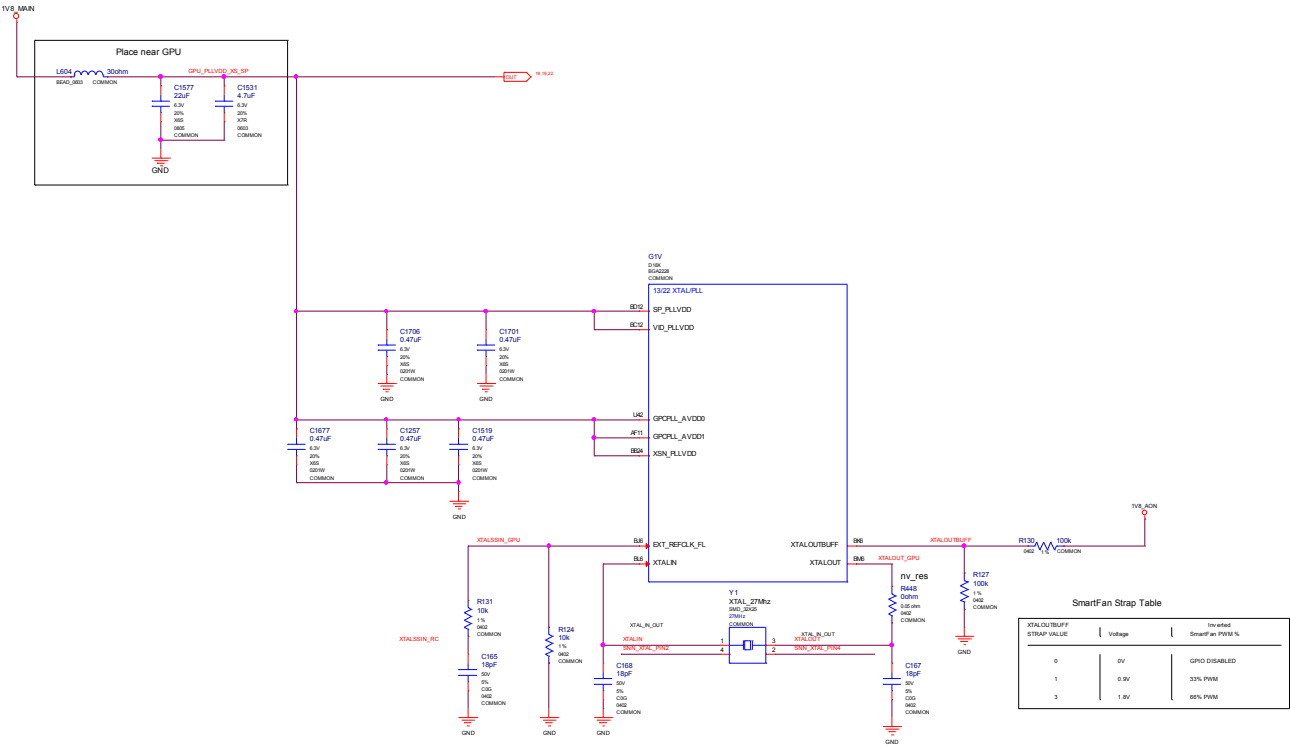
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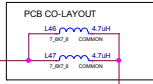
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PAGE DETAIL	MISC XTAL_PLL

NVIDIA CORPORATION			
2701 SANTOMAS EXPRESSWAY			
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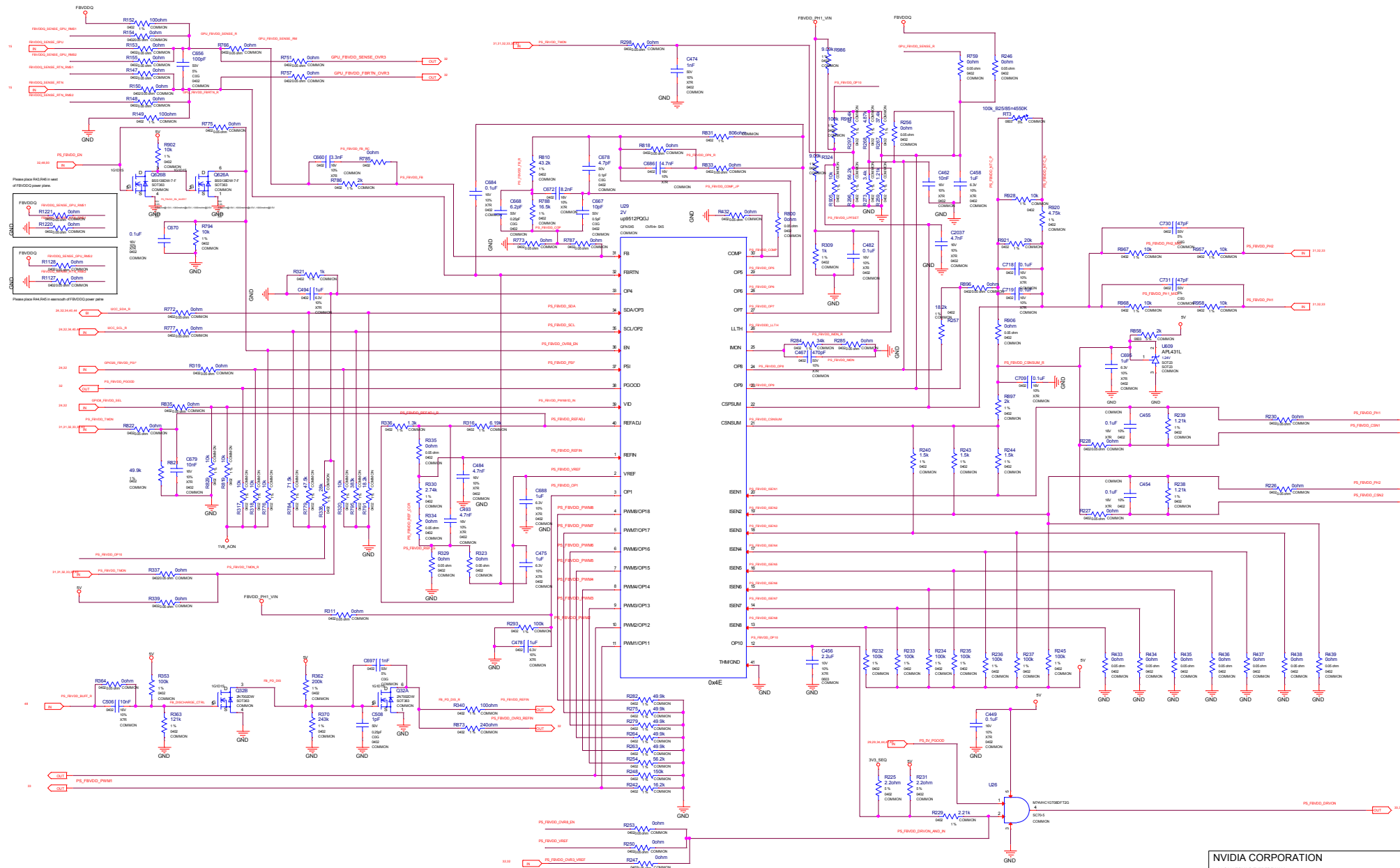


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PAGE DETAIL	MISC: USB PPC



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NV_PN 600-1G180-BASE-200

PCB REV PG180-A02

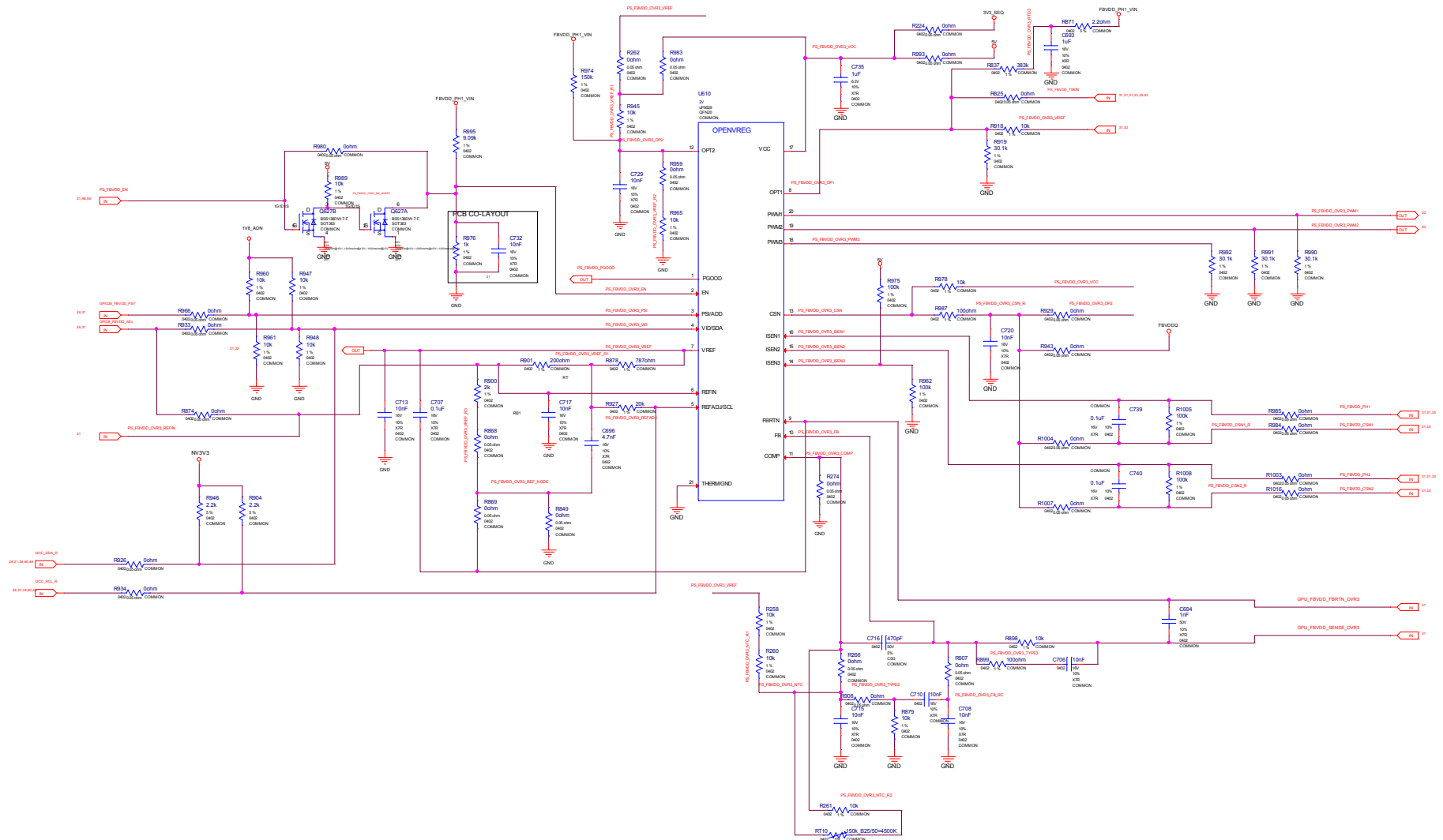
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PAGE DETAIL	PS: FBVDD CONTROLLER



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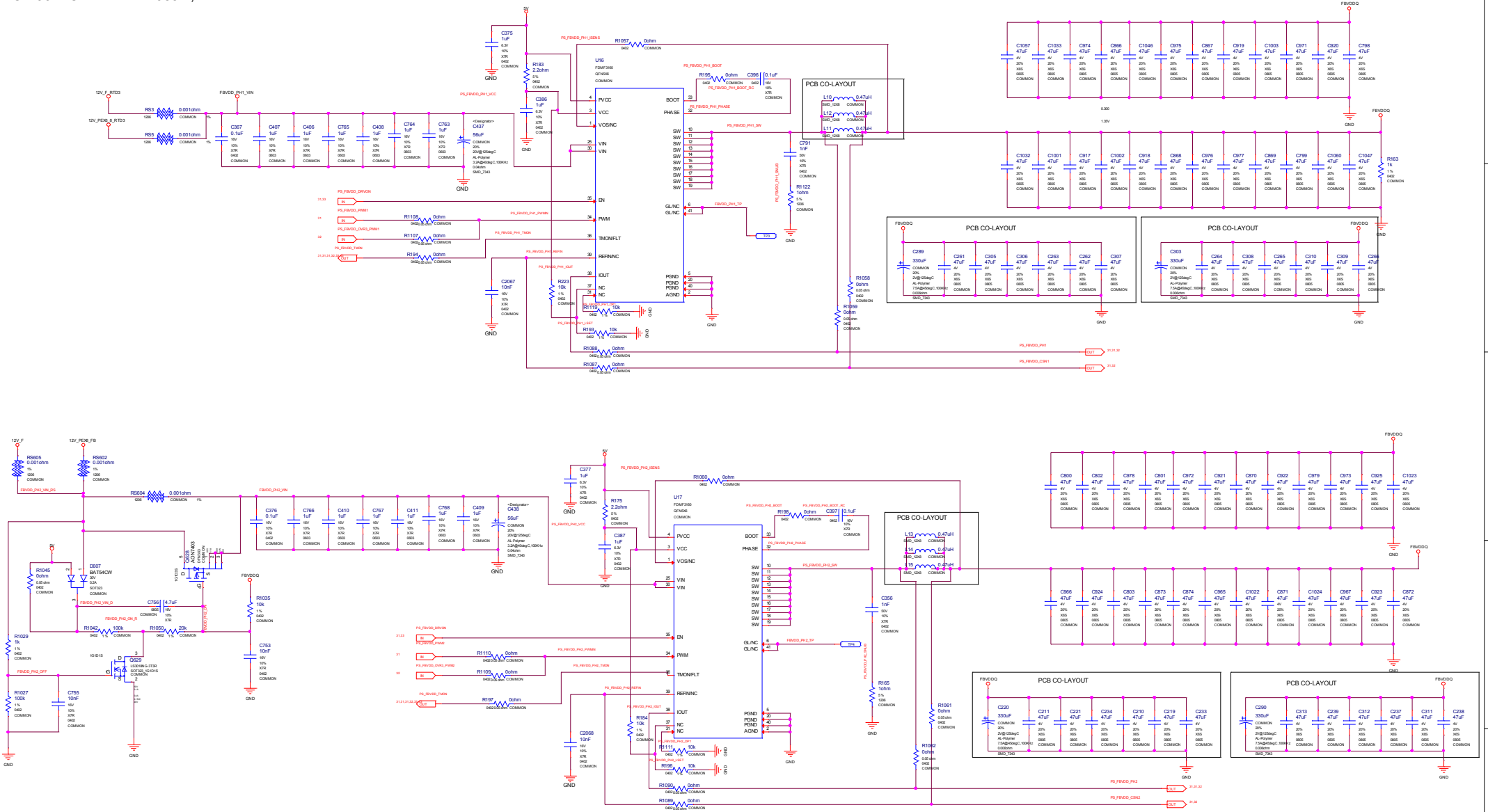
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NV_PN 600-1G180-BASE-200

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PS: FBVDD CONTROLLER OVR3

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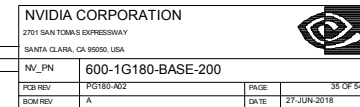
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Figure 1: Schematic representation of the 1200 bp DNA region. The diagram shows a linear DNA sequence with various restriction sites (EcoRI, XbaI, KpnI, SmaI, PstI, SalI, BamHI, HindIII, ClaI, XhoI, NotI, SpeI, KpnI, SmaI, PstI, SalI, BamHI, HindIII, ClaI, XhoI, NotI, SpeI) and a central region labeled 'COMMON'. The sequence is flanked by two regions labeled 'P1' and 'P2'. The sequence is shown in a 3D perspective, with the top strand in red and the bottom strand in blue. The sequence is numbered from 1 to 1200 bp. The sequence is shown in a 3D perspective, with the top strand in red and the bottom strand in blue. The sequence is numbered from 1 to 1200 bp.

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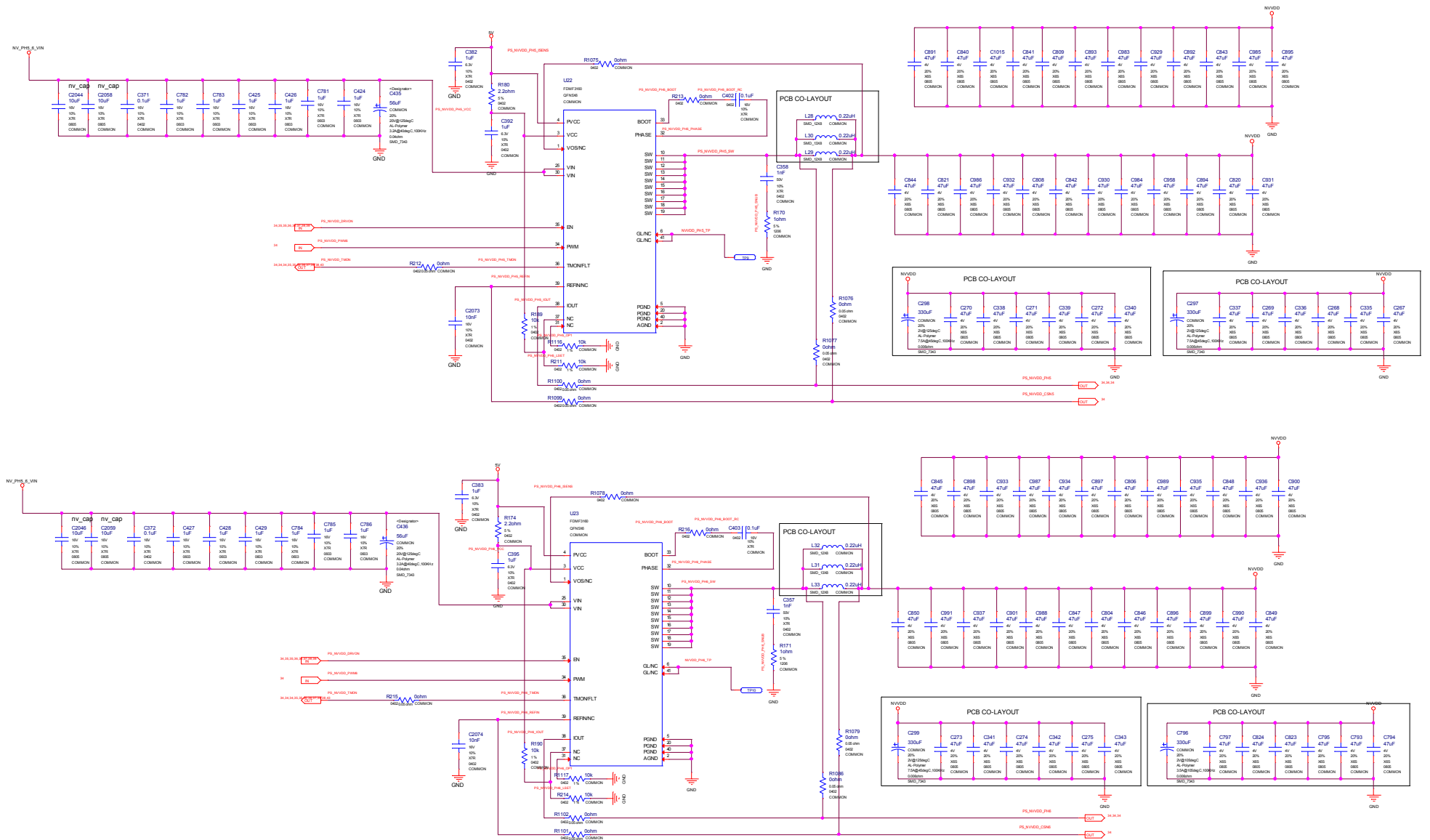




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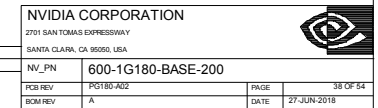
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NV_PN	600-1G180-BASE-200
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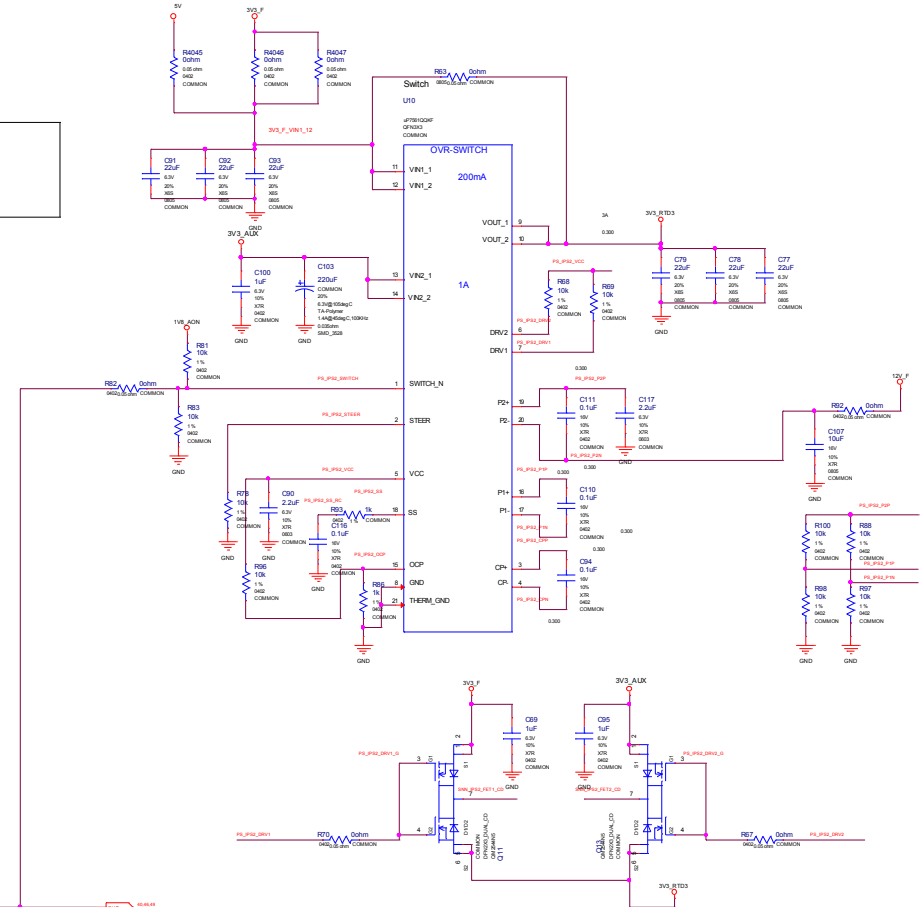
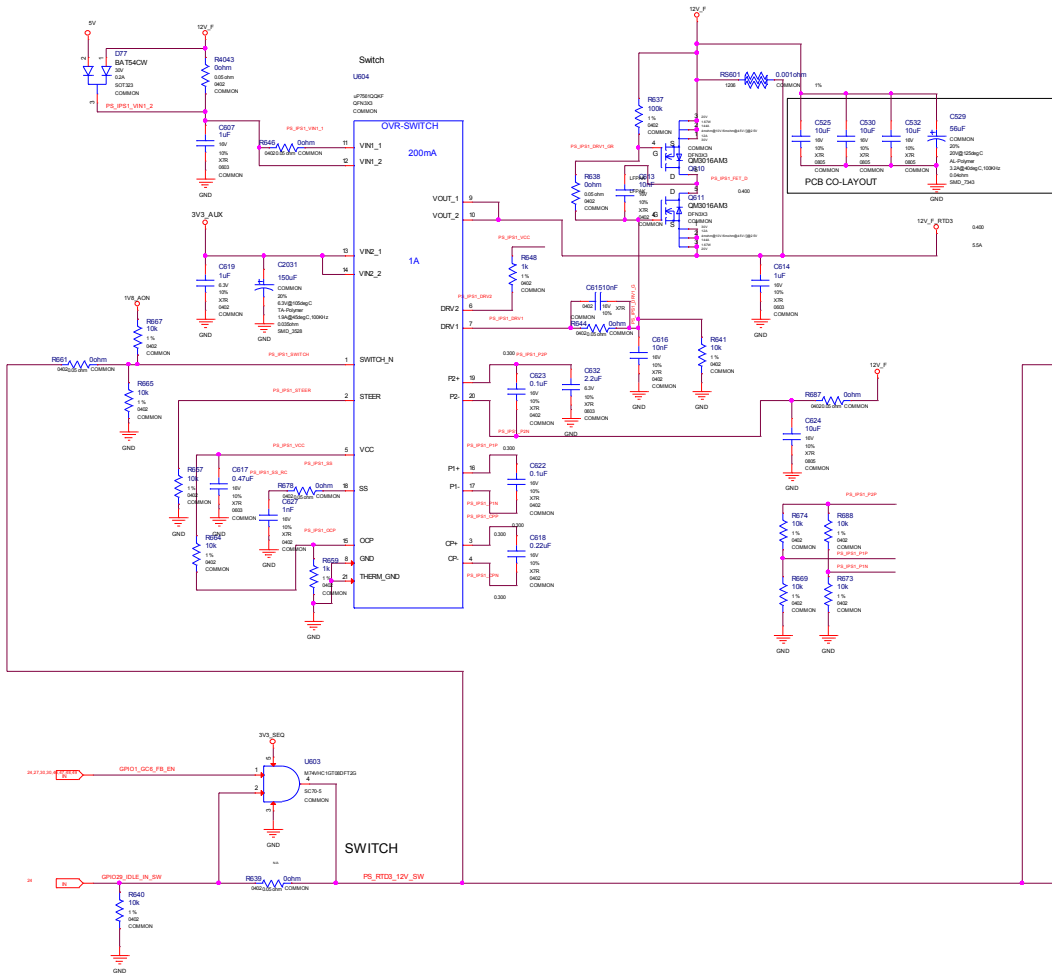


AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE: DETAIL	PS: INPUT SWITCH RTD3

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PCB REV PG180-A02
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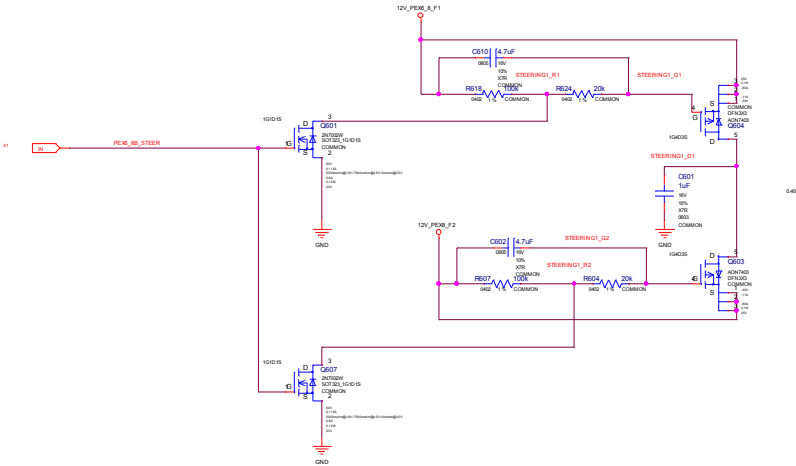


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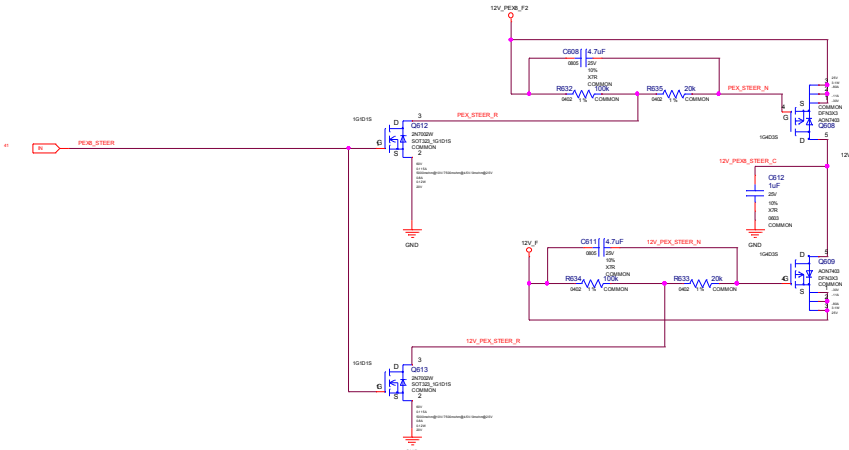


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12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



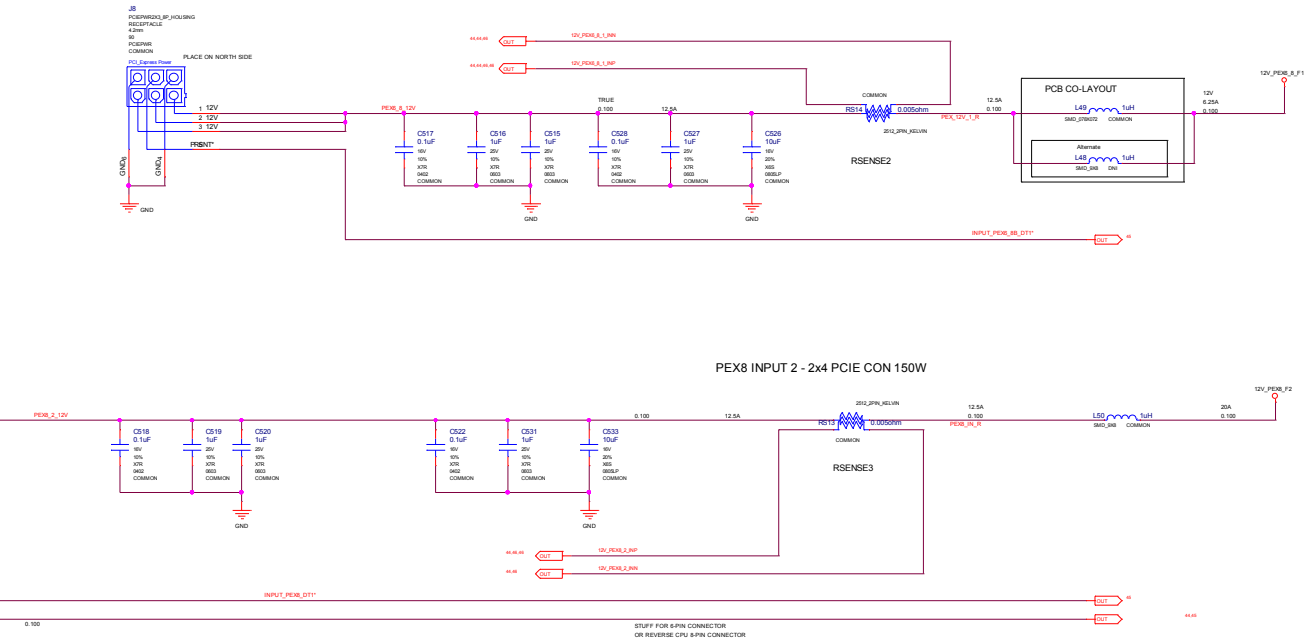
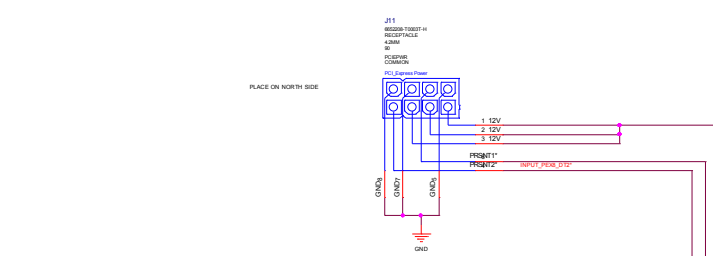
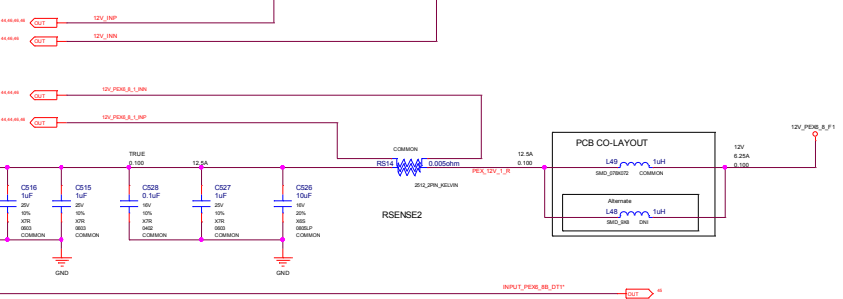
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GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



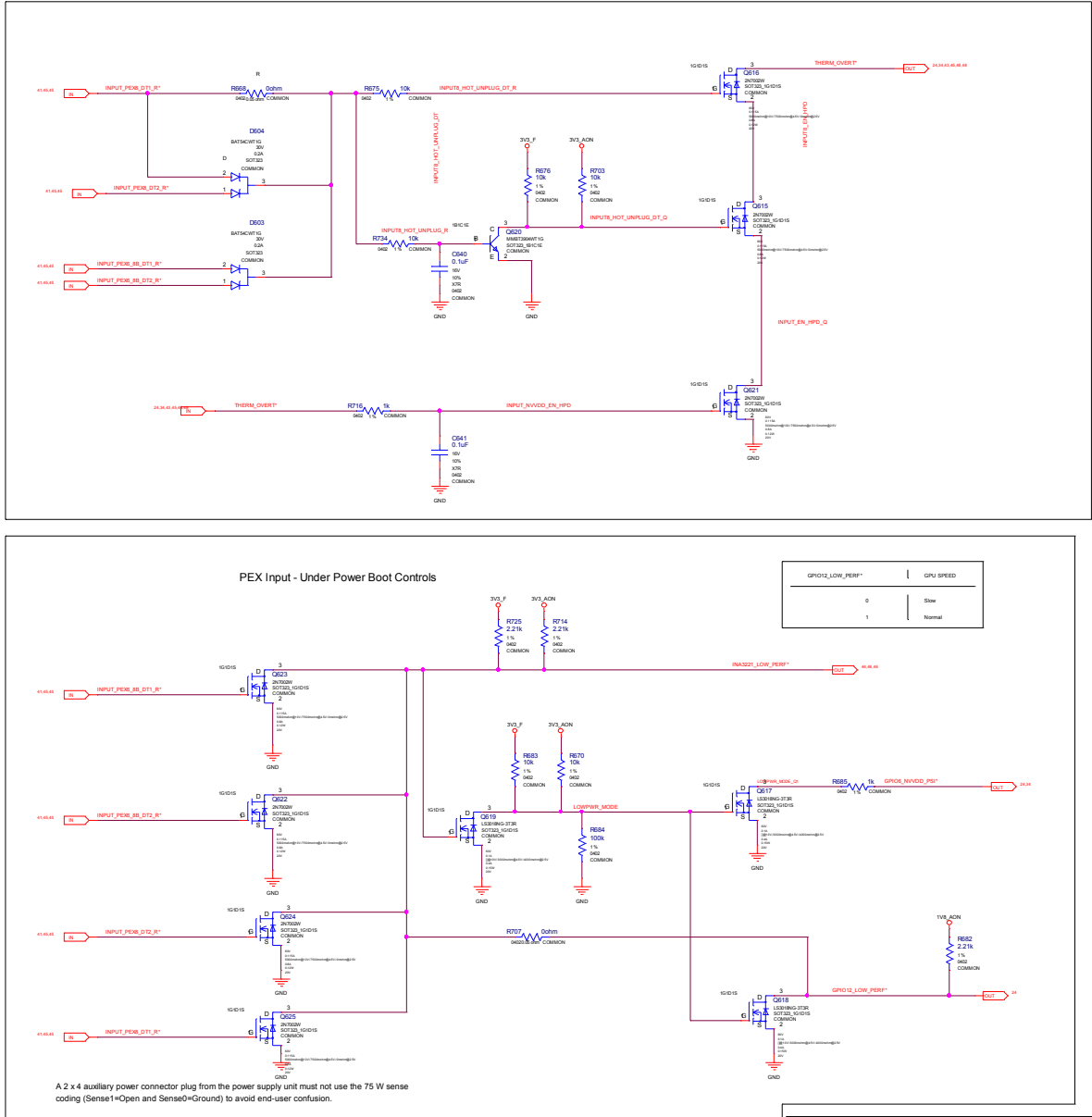
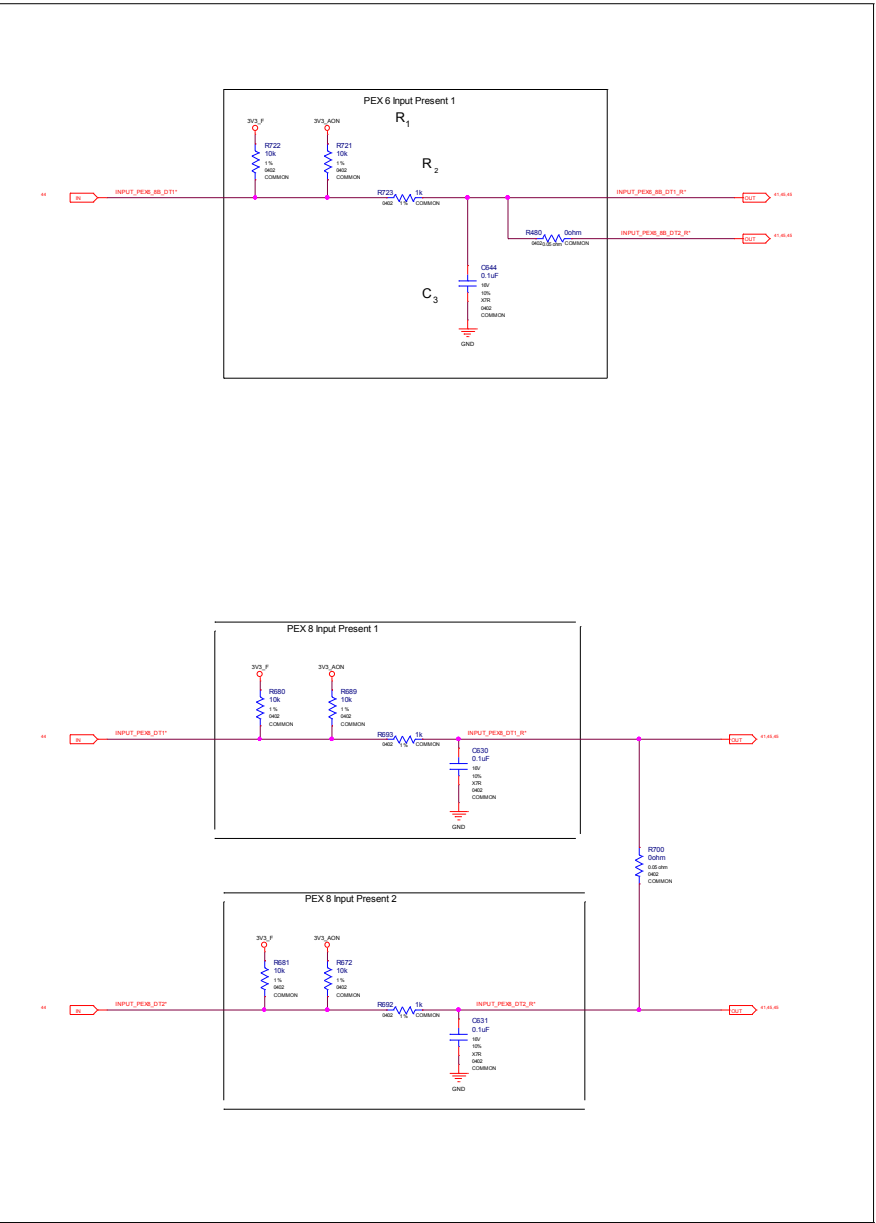
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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PS: 12V CURRENT STEERING

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PS: CURRENT STEERING, HOT UNPLUG DETECT

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PCB REV

PG180-A02

BCM REV

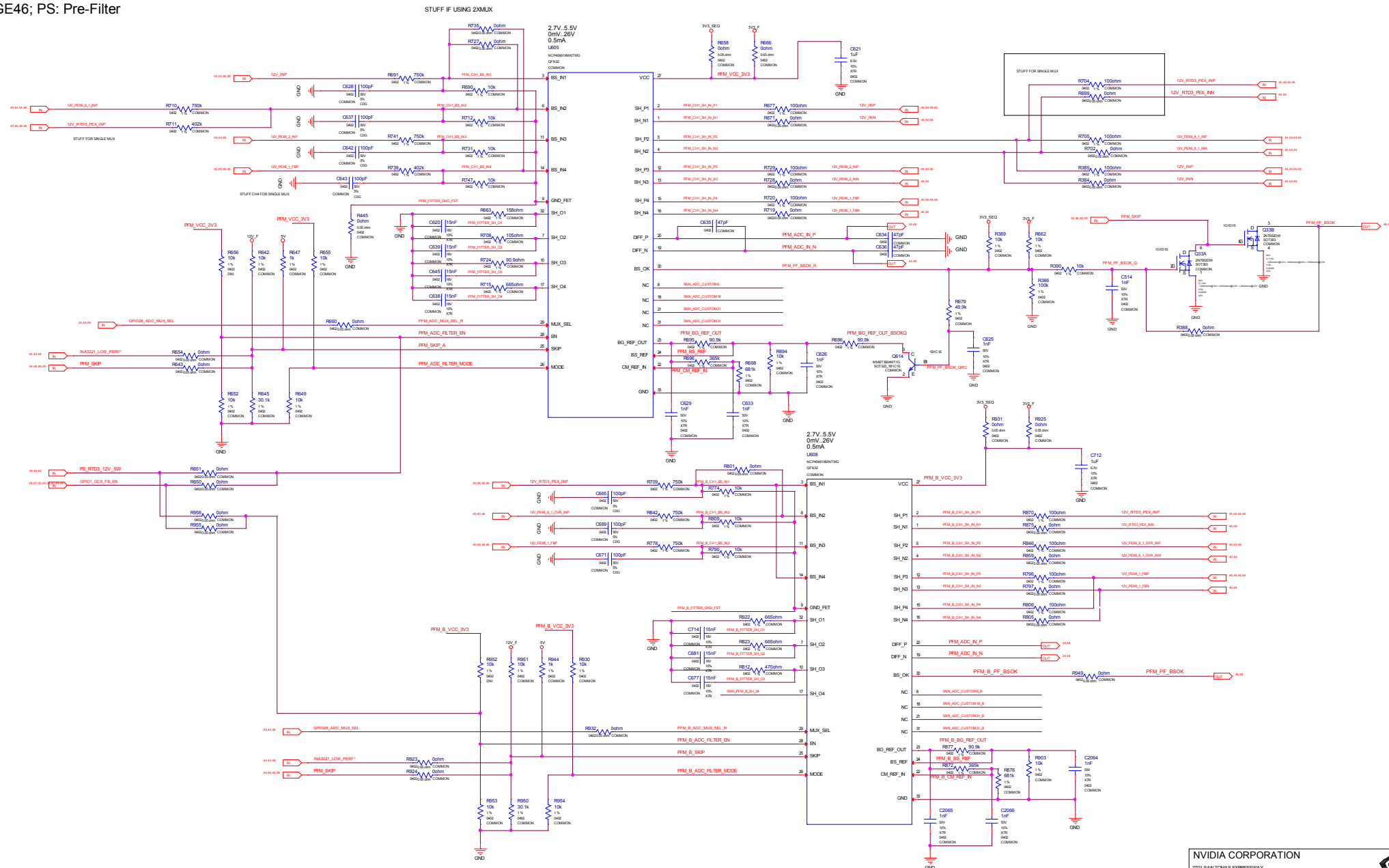
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NVIDIA CORPORATION

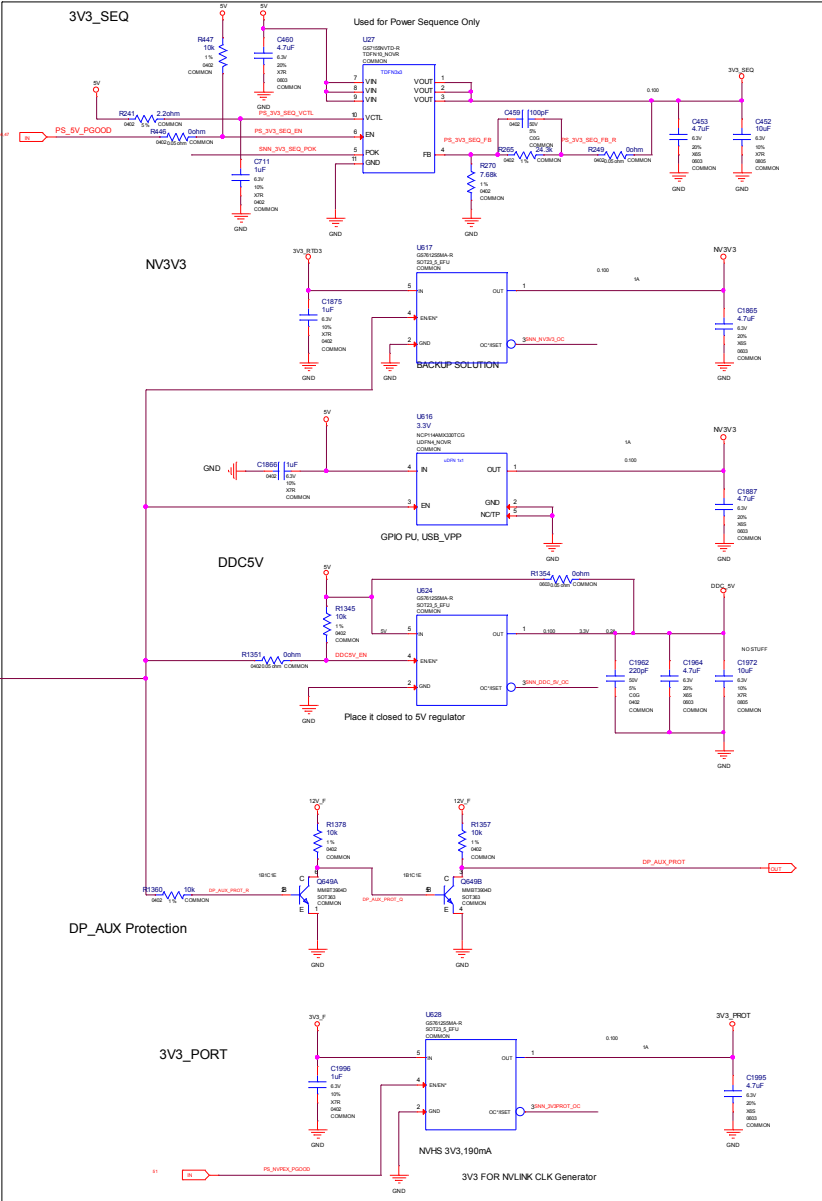
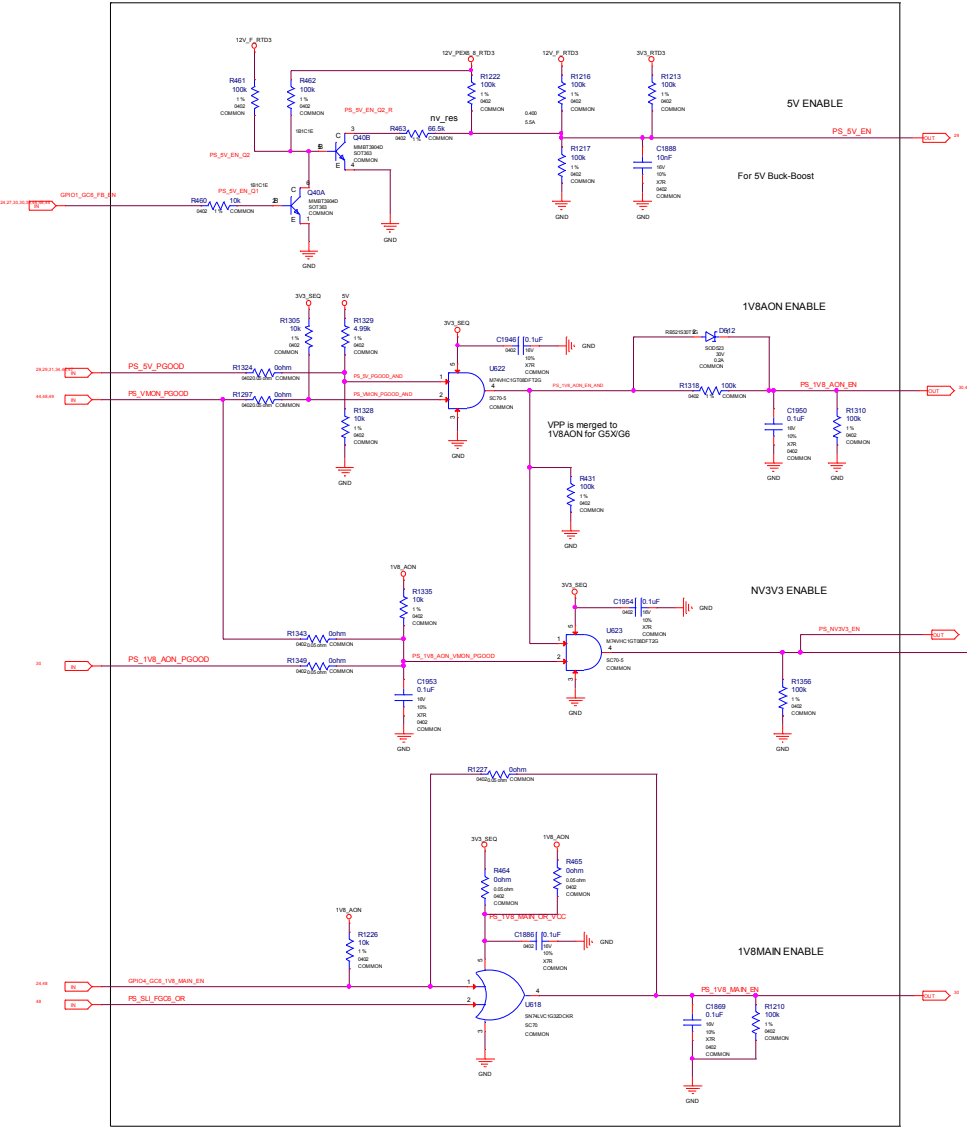
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NV_PN	600-1G180-BASE-200
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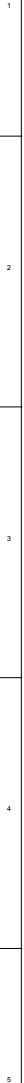
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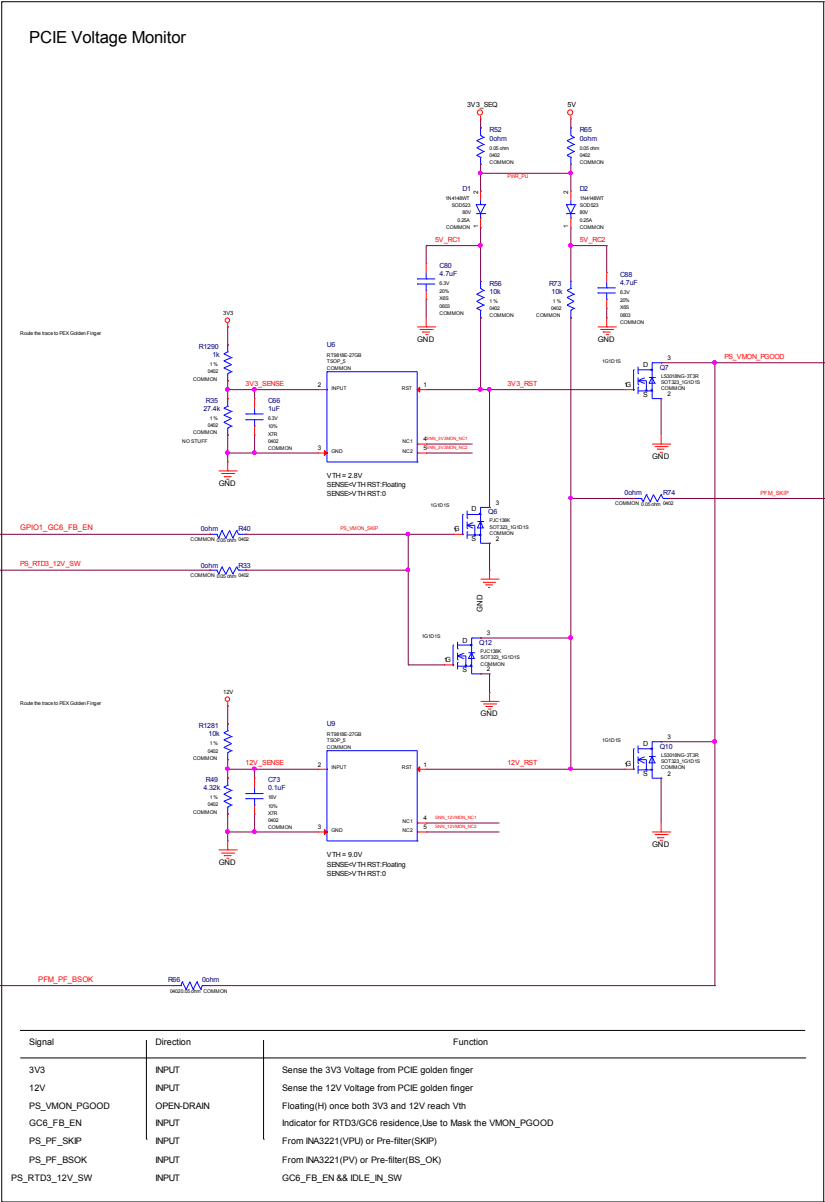
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NVIDIA CORPORATION	
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NV_PN	600-1G180-BASE-200
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ASSEMBLY	<ASSEMBLY__DESCRIPTION>
PAGE DETAIL	SEQUENCE: NV, PEX, FB ENABU

A	B	C	D	E	F	G	H
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BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ
Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs

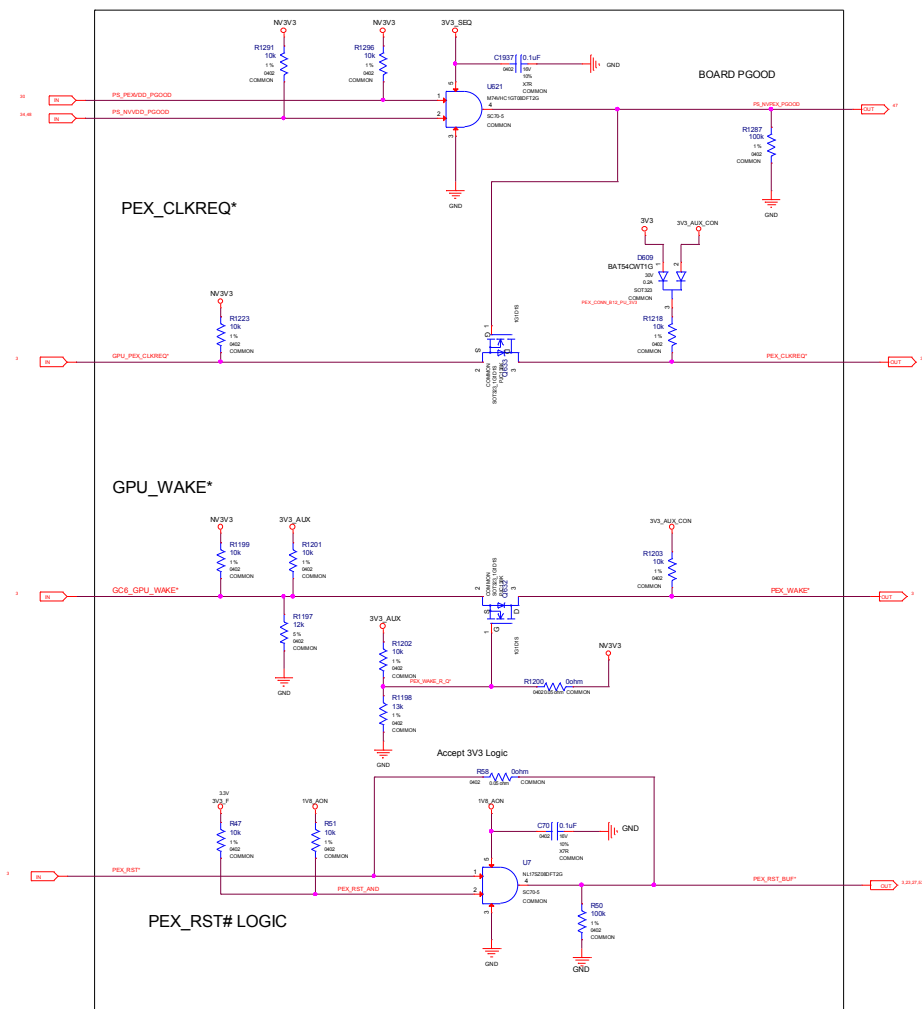


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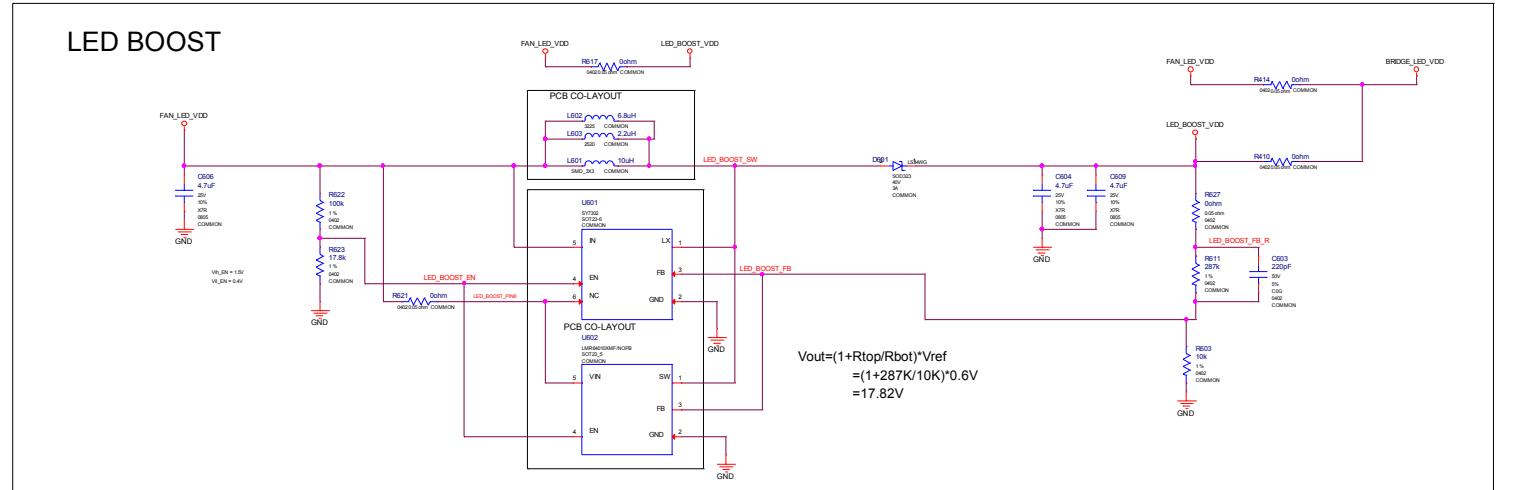
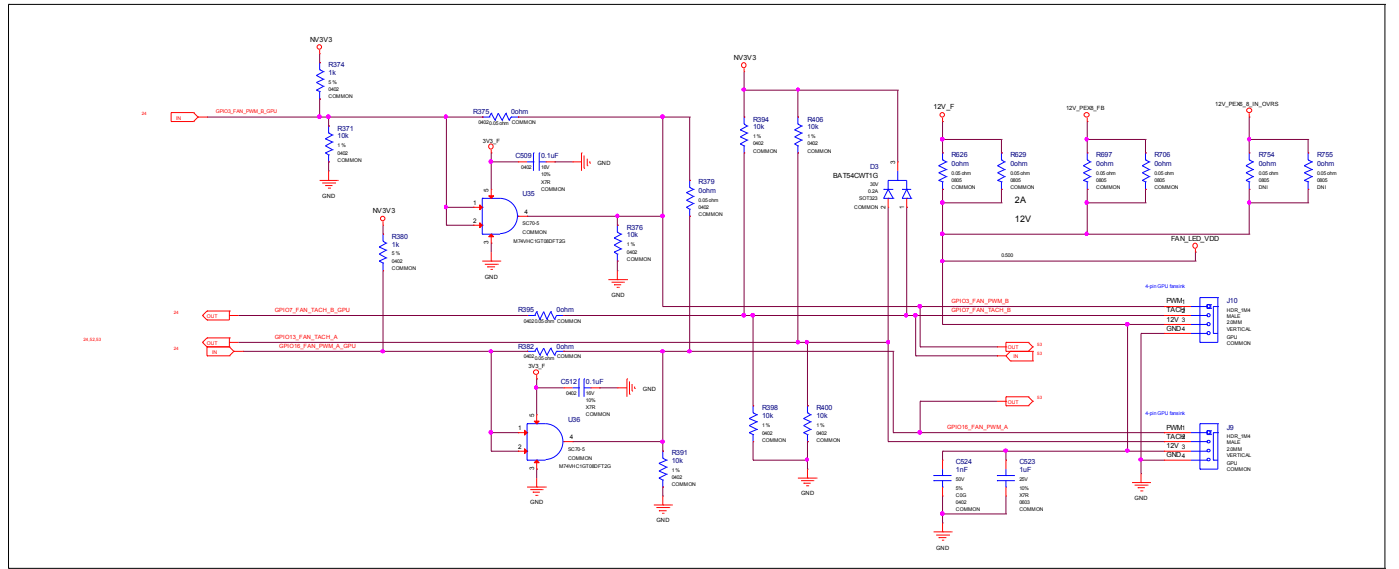
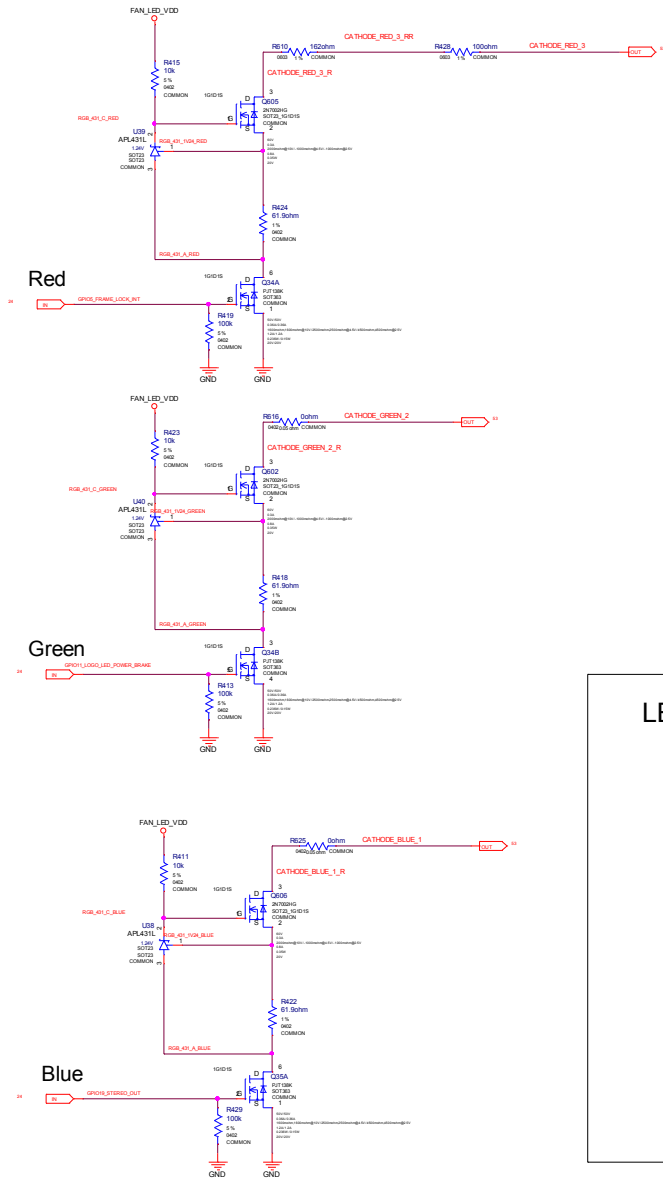
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PAGE DETAIL	LED & FAN HEADERS

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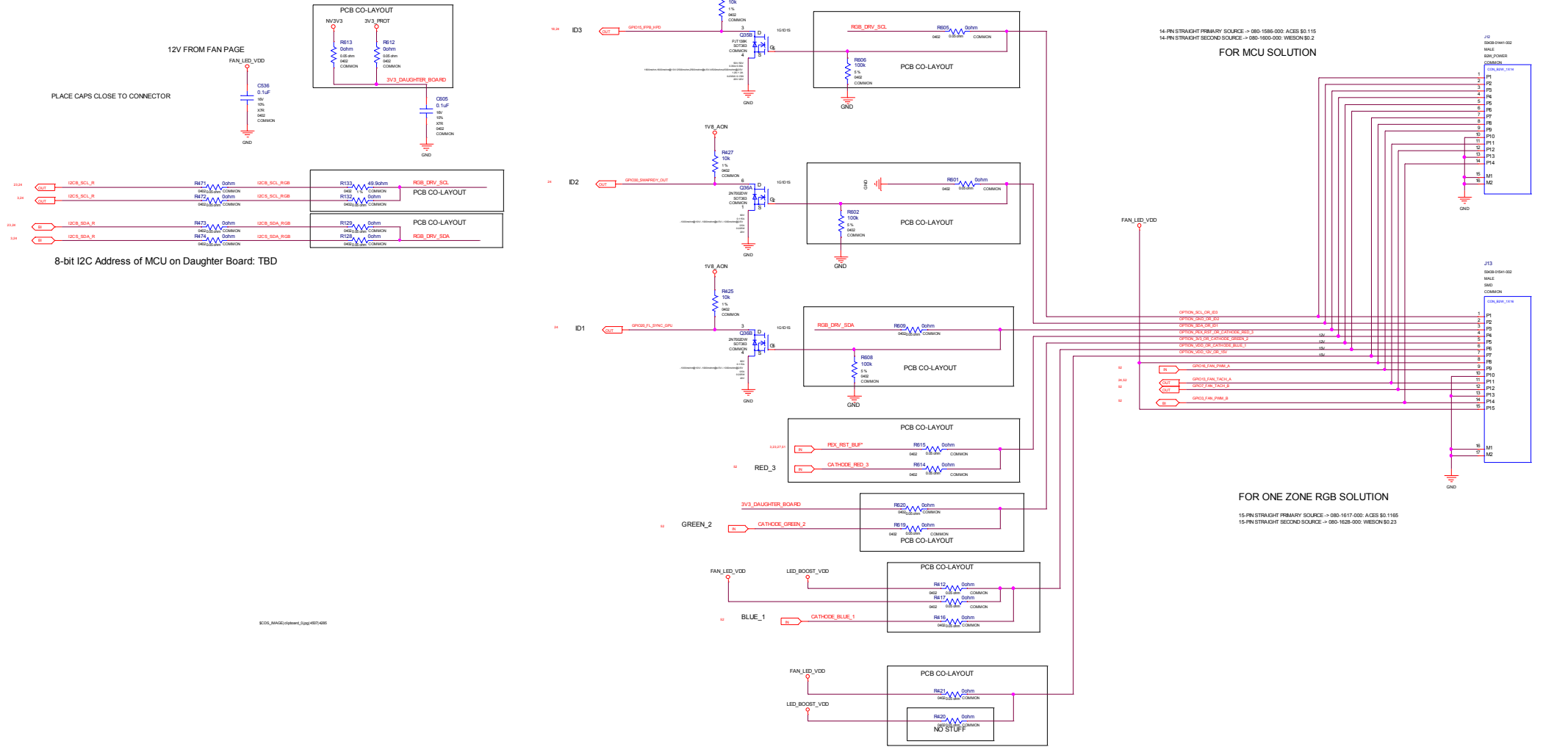
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BCM REV	A	DATE	27-JUN-2018

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	LED 2

NVIDIA CORPORATION	
2701 SAN TOMAS EXPRESSWAY	
SANTA CLARA, CA 95050, USA	
NV_PN	600-1G180-BASE-200
PCB REV	PG180-A02
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MEC2

PH_M2.5X4.5X13MM_SCREW

STD

COMMON

new LF screw — 155-0025-000.

ROHS screw — 154-0025-700.

No connected mounting pins

MEC501
Black Cover
NIPIN
COMBON

Diagram of a 12-pin connector with pins numbered 1 to 12. The pins are arranged in a single row, with pins 1 through 8 on the left and pins 9 through 12 on the right. A label '12 connected mounting pins' is positioned above the connector.

MEC3
SOCKET_BGA
12PIN
COMMON

MECI-1
DSB-SS Mounting Hole
X/D
COMMON

MECI-2
DSB-SS Mounting Hole
X/D
COMMON

MECI-3
DSB-SS Mounting Hole
X/D
COMMON

MECI-4
DSB-SS Mounting Hole
X/D
COMMON

MECI-5
DSB-SS Mounting Hole
X/D
COMMON

MECI-6
DSB-SS Mounting Hole
X/D
COMMON

MECI-7
DSB-SS Mounting Hole
X/D
COMMON

MECI-8
DSB-SS Mounting Hole
X/D
COMMON

MECI-9
DSB-SS Mounting Hole
X/D
COMMON

MECI-10
DSB-SS Mounting Hole
X/D
COMMON

GND

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Mechanical: Bracket/Thermal Solution



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