

PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

TABLE OF CONTENTS

Page	Description
1	Table of Contents
2	Block Diagram
3	PCI Express
4	PCI Termination
5	MEMORY: GPU Partition A/B
6	MEMORY: FBA Partition 31..0
7	MEMORY: FBA Partition 63..32
8	MEMORY: FBB Partition 31..0
9	MEMORY: FBB Partition 63..32
10	MEMORY: GPU Partition C/D
11	MEMORY: FBC Partition 31..0
12	MEMORY: FBC Partition 63..32
13	MEMORY: FBD Partition 31..0
14	MEMORY: FBD Partition 63..32
15	GPU PWR and GND
16	GPU Decoupling
17	GPU DECOUPLING
18	IFPAB TALL-DP
19	IFPE DP
20	IFPF USBC
21	IFPC HDMI 2.0/DP
22	IFPD DP
23	NVHS INTERFACE
24	MISC: FAN,THERMAL,JTAG,GPIO,STEREO
25	MISC3: ROM, STRAPS

Page	Description
26	MISC: XTAL, PLL
27	MISC: USB PPC
28	PS: USB VR
29	PS: 5V, 5V BACKUP
30	PS: PEXVDD, 1V8
31	PS: FBVDD CONTROLLER
32	PS: FBVDD CONTROLLER OVR3
33	PS: FBVDD PHASE 1, 2
34	PS: NVVDD CONTROLLER OVR8
35	PS: NVVDD Phase 1, 2
36	PS: NVVDD Phase 3, 4
37	PS: NVVDD Phase 5, 6
38	PS: NVVDD Phase 7, 8
39	PS: INPUT SWITCH RTD3
40	PS: INPUT SWITCH RTD3 USB
41	PS: INPUT SWITCH RAIL BALANCE
42	PS: 12V CURRENT STEERING
43	PS: VR THERMAL PROTECTION
44	PS: INPUTS, FILTERING AND MONITORING
45	PS: CURRENT STEERING,HOT UNPLUG DETECT
46	PS: PRE-FILTER
47	SEQUENCE: 5V, 1V8, NV3V3 ENABLE
48	SEQUENCE: NV, PEX, FB ENABLE
49	SEQUENCE: PCIE VOLTAGE MONITOR
50	SEQUENCE: DISCHARGE

Page	Description
51	SEQUENCE: MISC
52	LED & FAN HEADERS
53	LED 2
54	Mechanical: Bracket/Thermal Solution

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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	Table of Contents

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NV_PN

600-1G180-BASE-200

PCB REV

PG180-A02

BOM REV

A

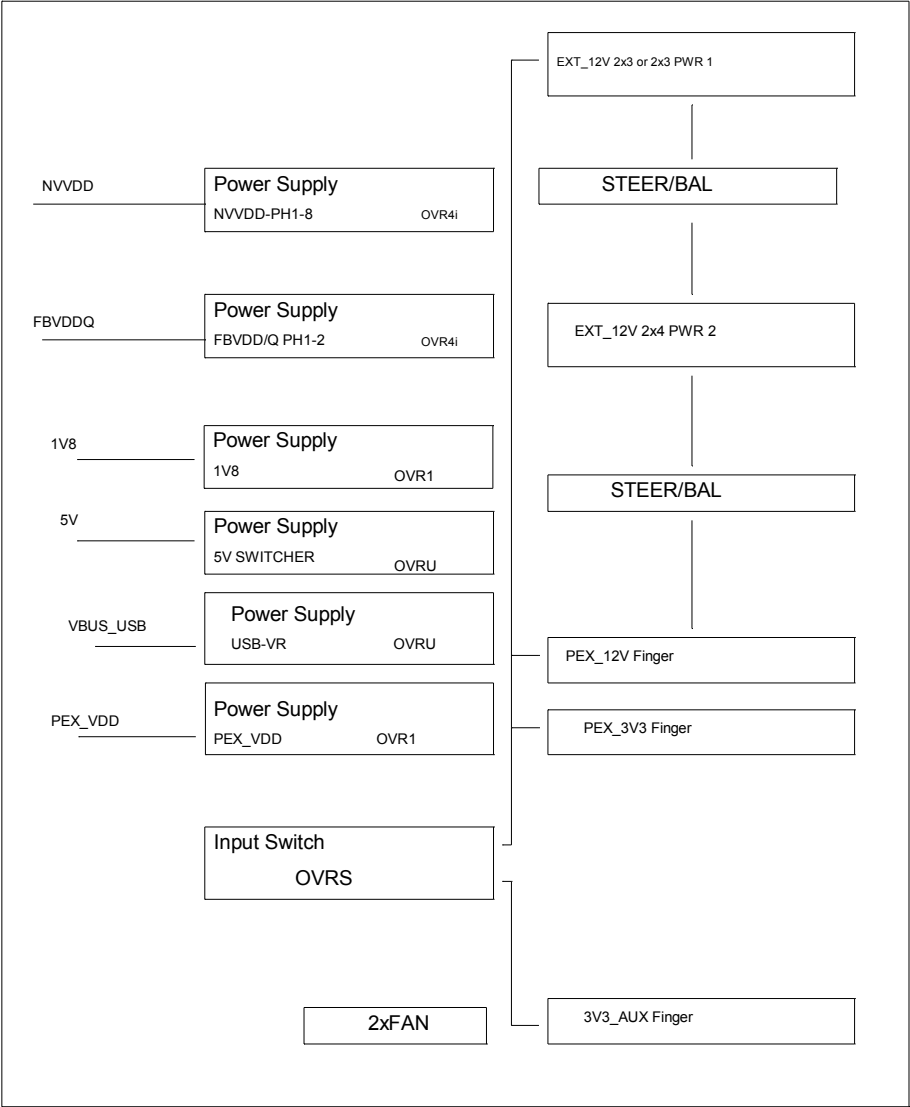
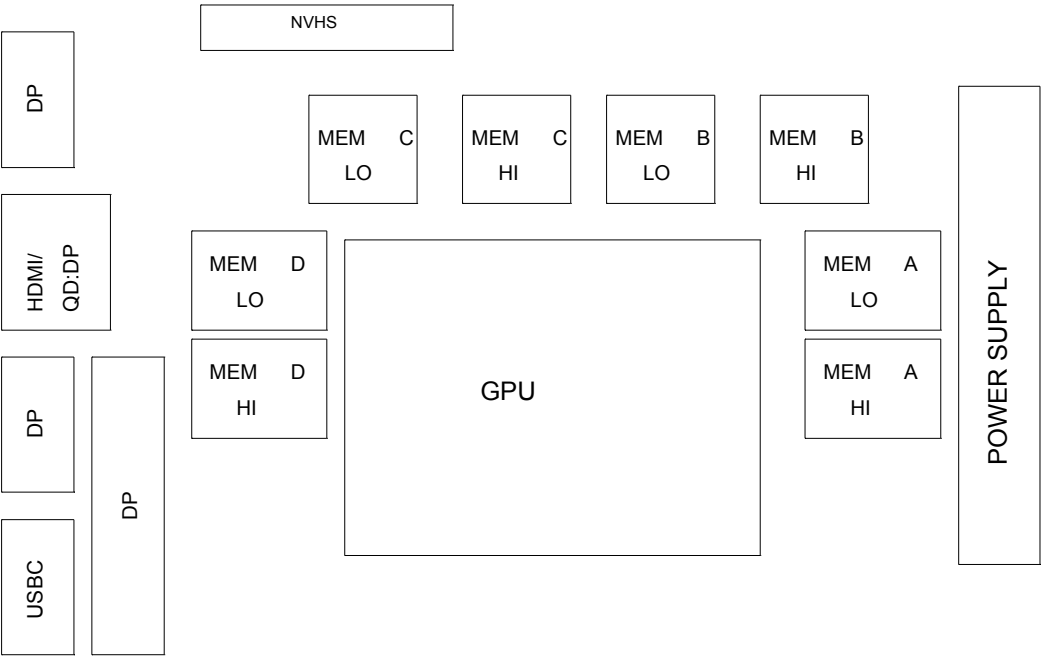
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1 OF 54

DATE

27-JUN-2018



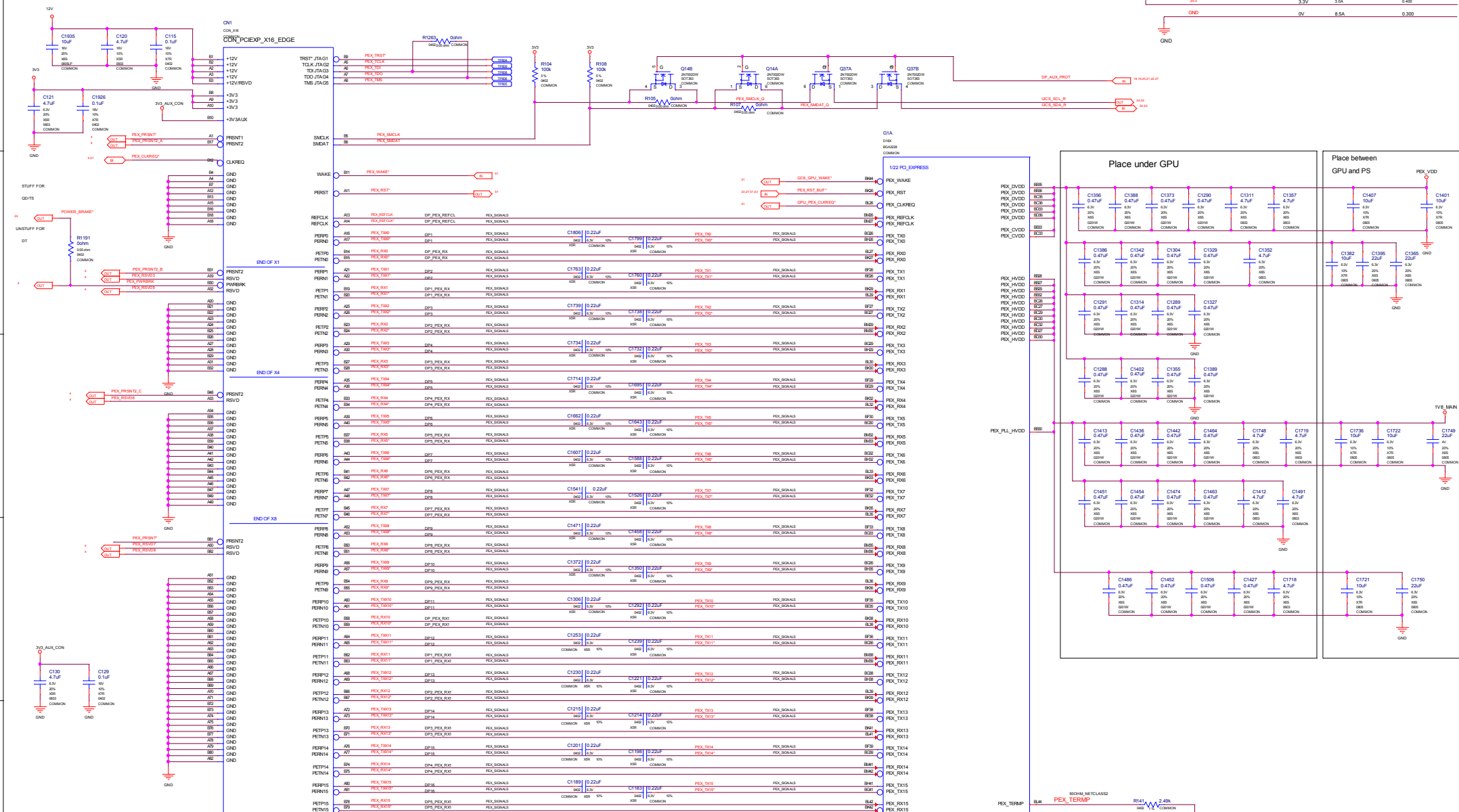


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BOM REV	A	DATE	27-JUN-2018

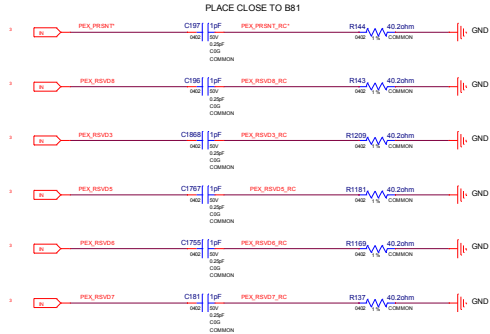
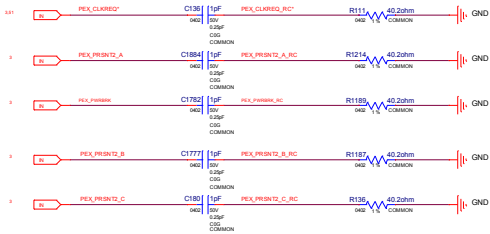




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BOM REV	A	DATE	27-JUN-2018	

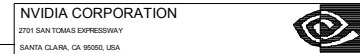
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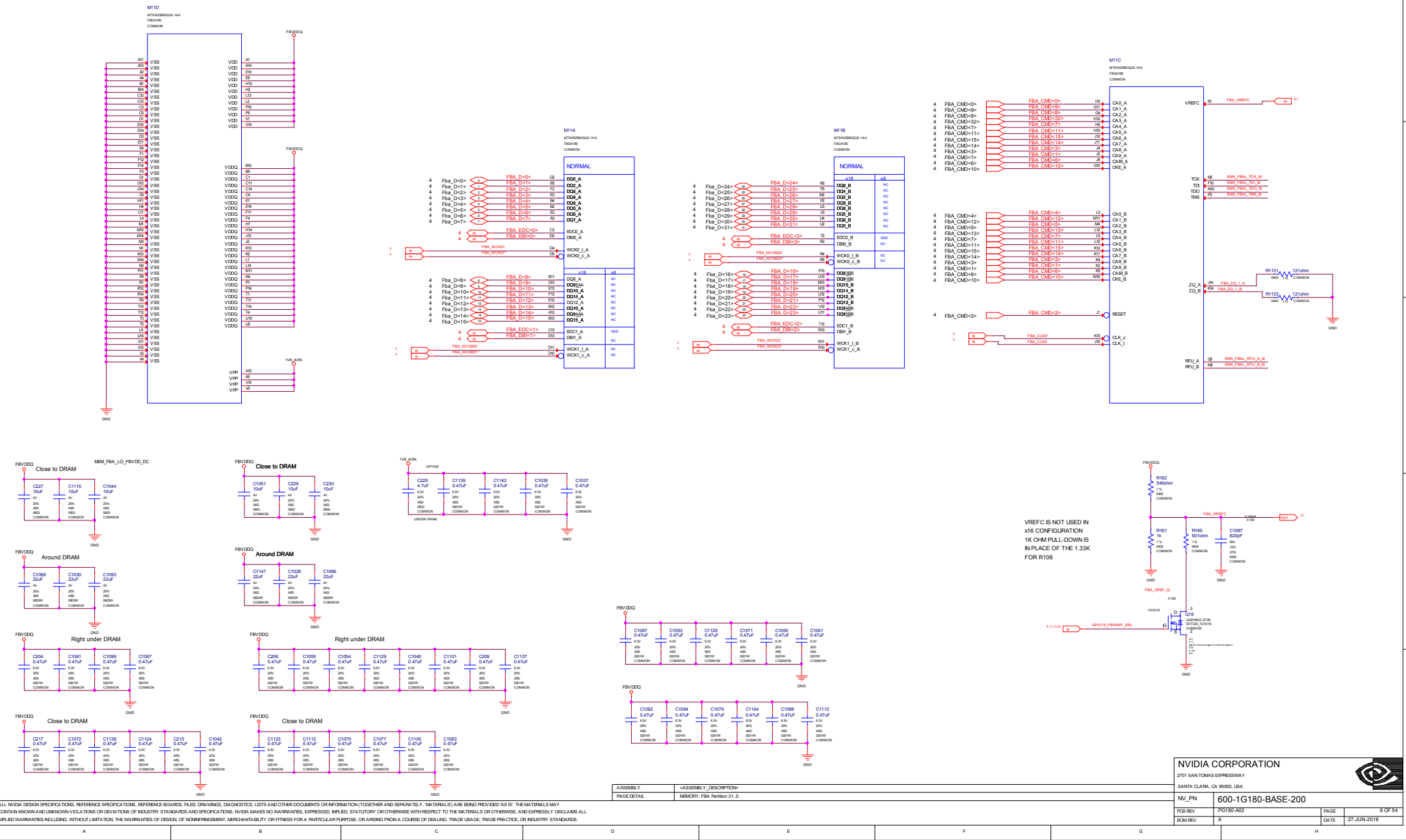
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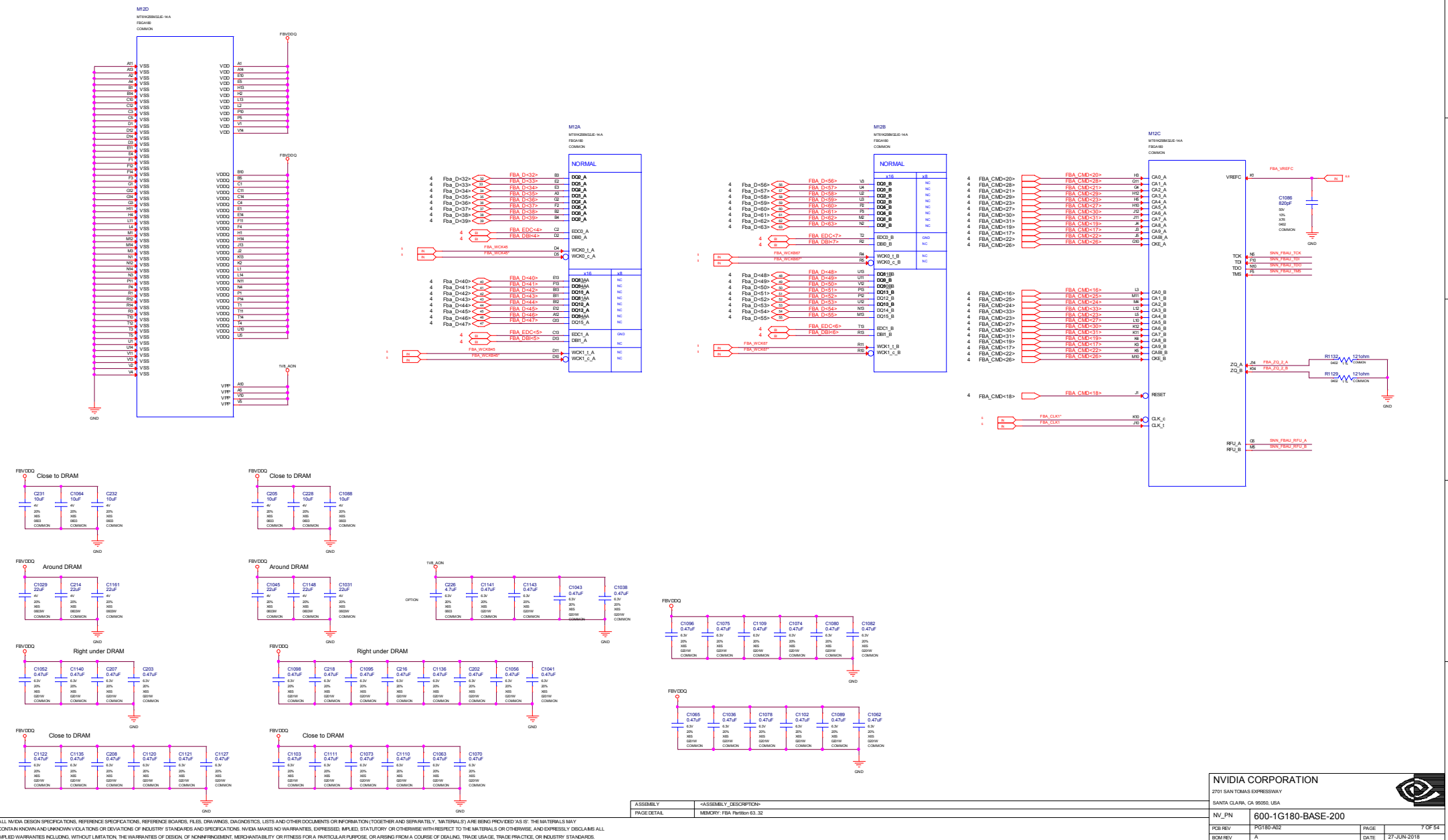
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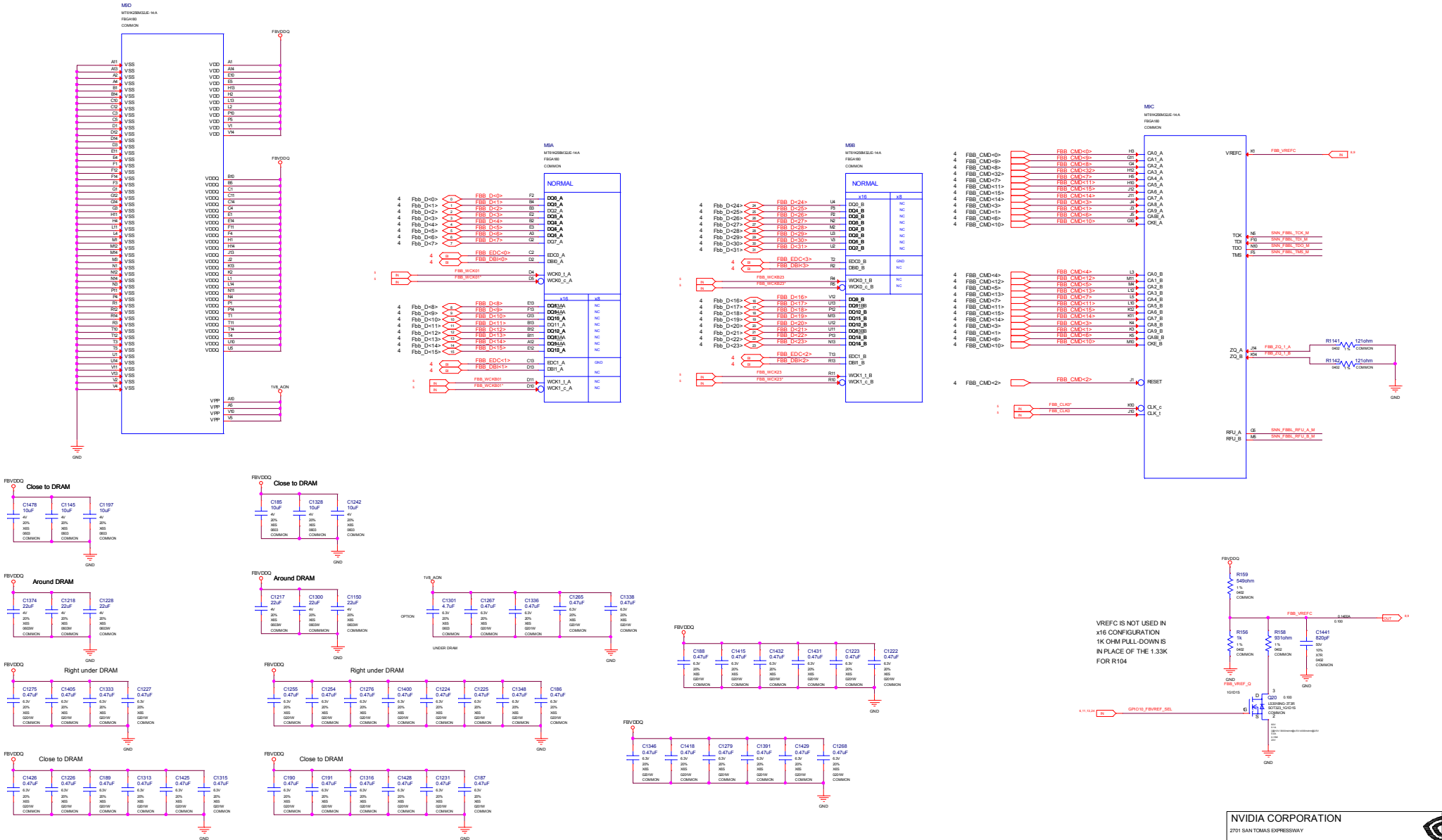
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PCB REV	PG180-A02	PAGE	4 OF 54
ROM REV	A	DATE	27 JUN 2018



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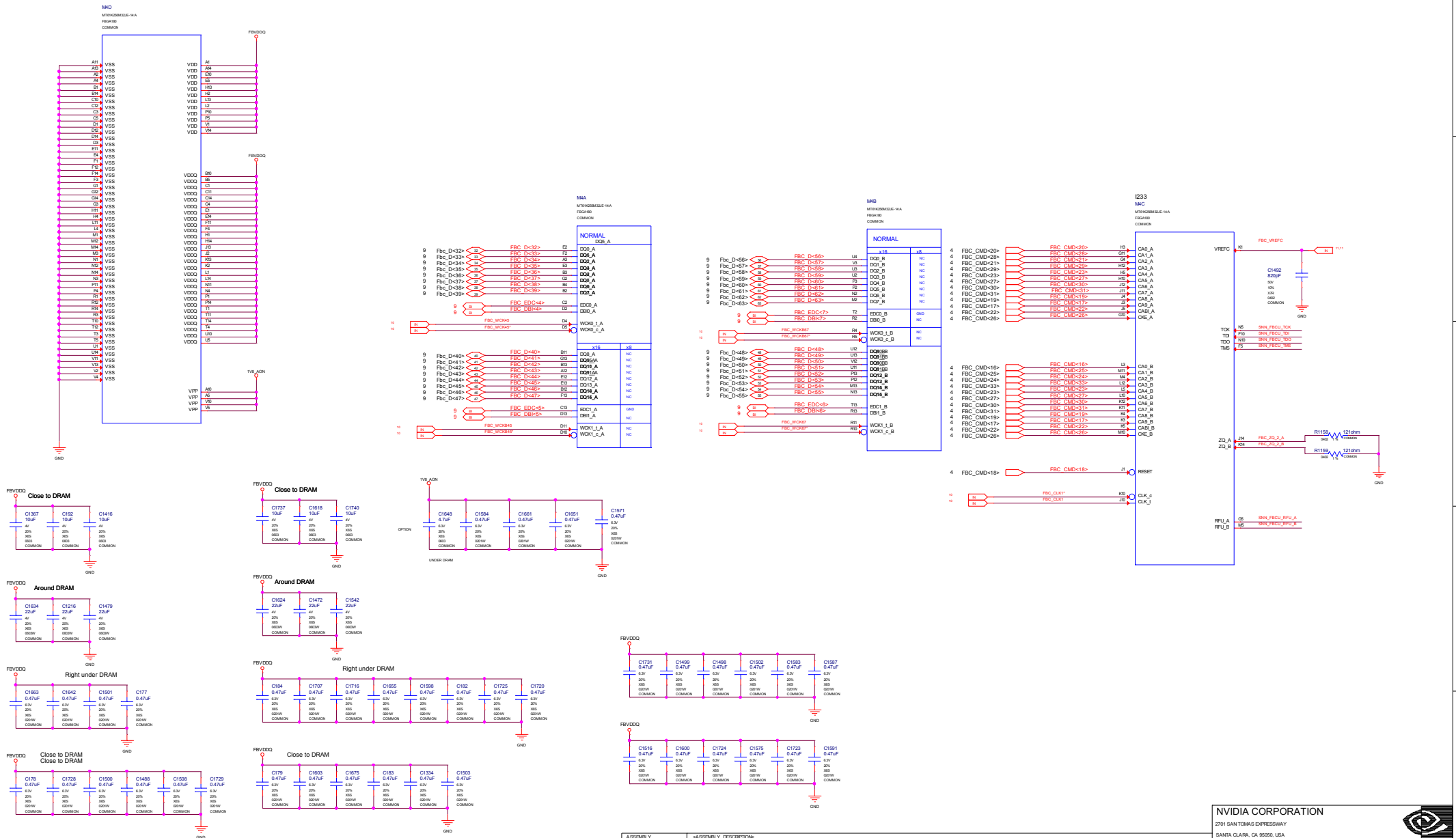


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PCB REV	P0180-A02
ICOM REV	A
PAGE	8 OF 54
DATE	27-JUN-2018

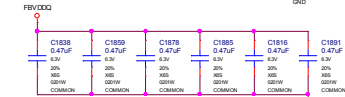
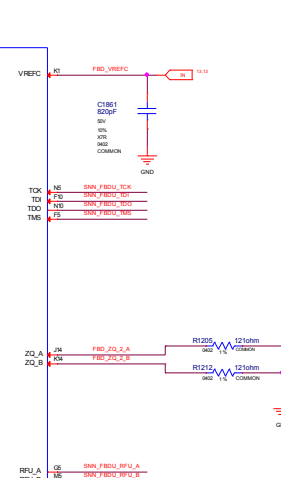




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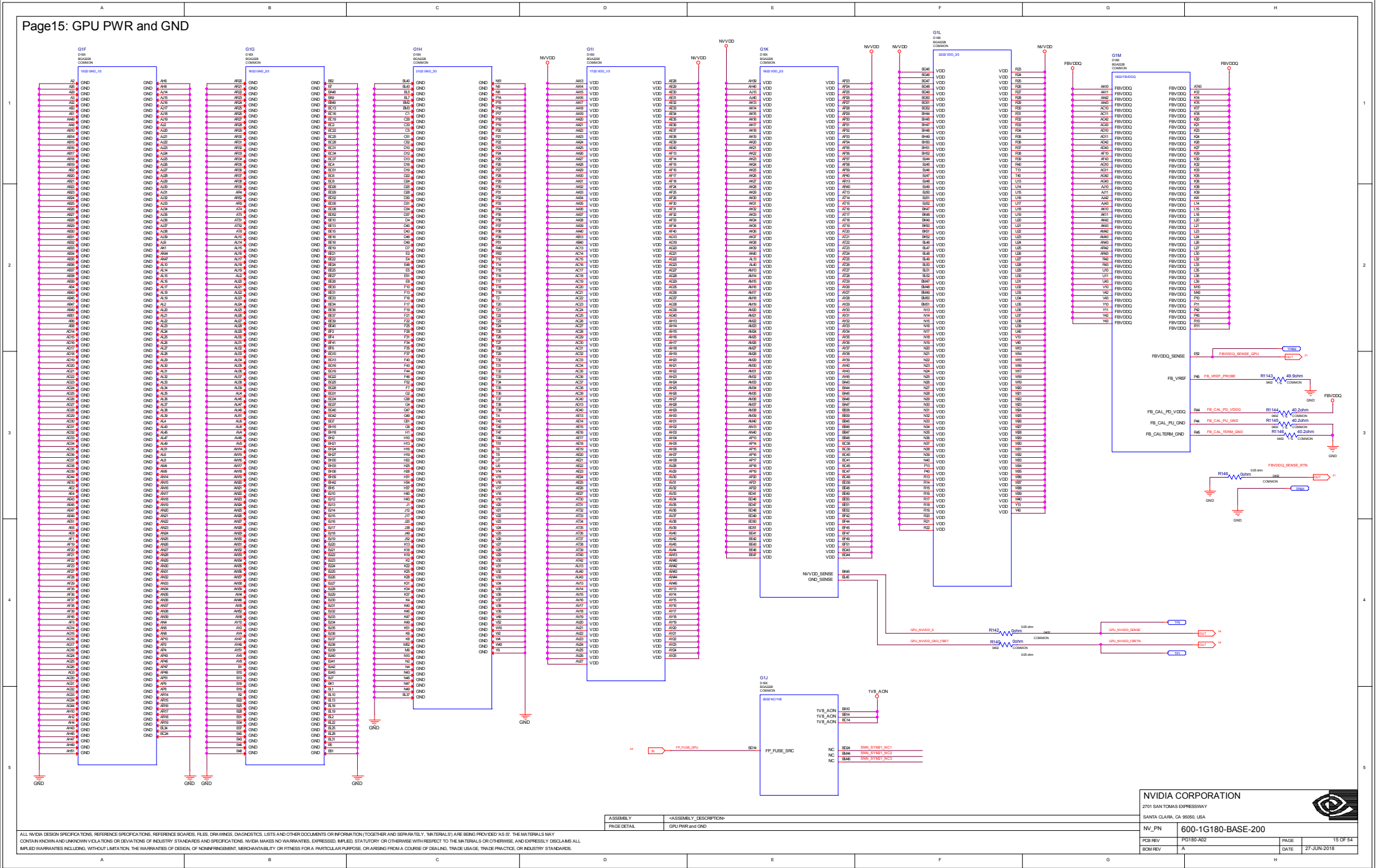
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PCB REV	PG180-A02
ICOM REV	A
PAGE	12 OF 54
DATE	27-JUN-2018



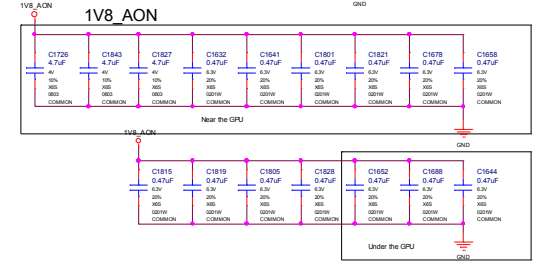
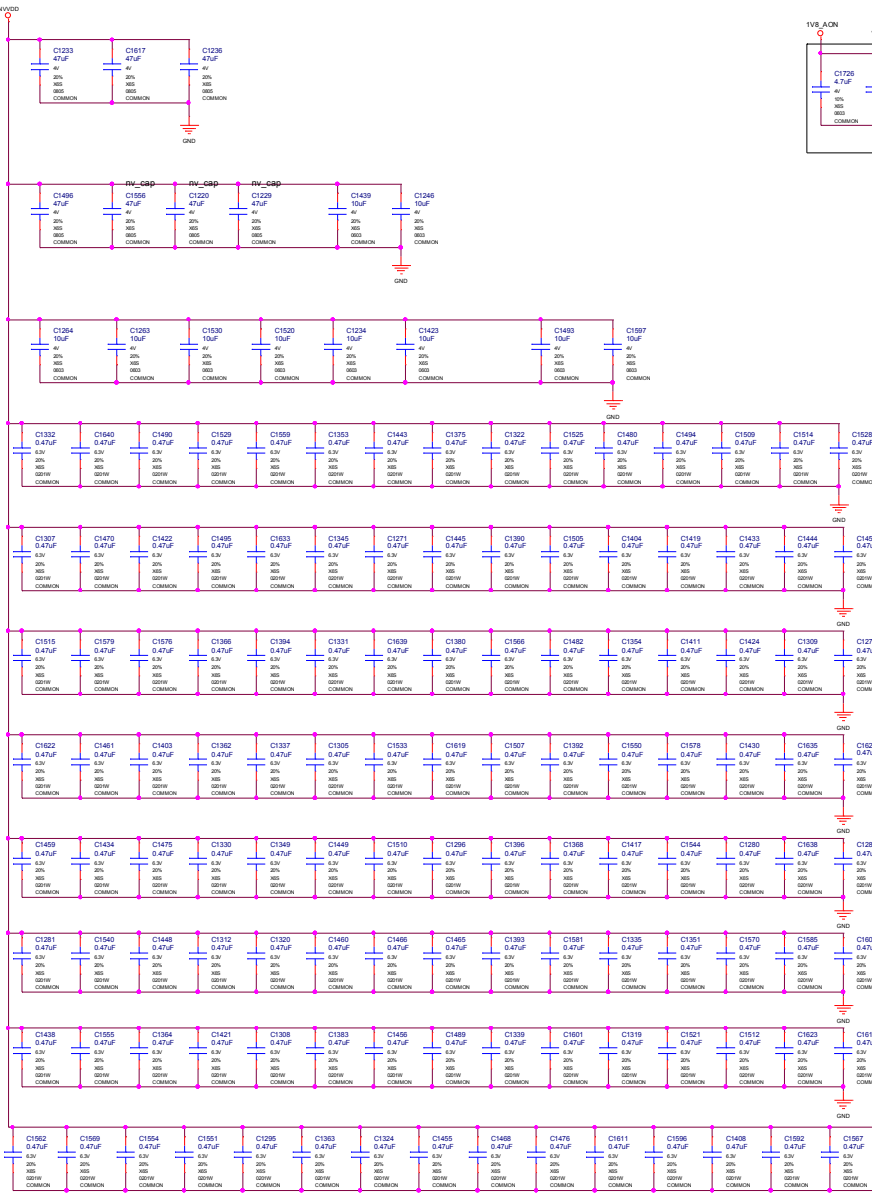
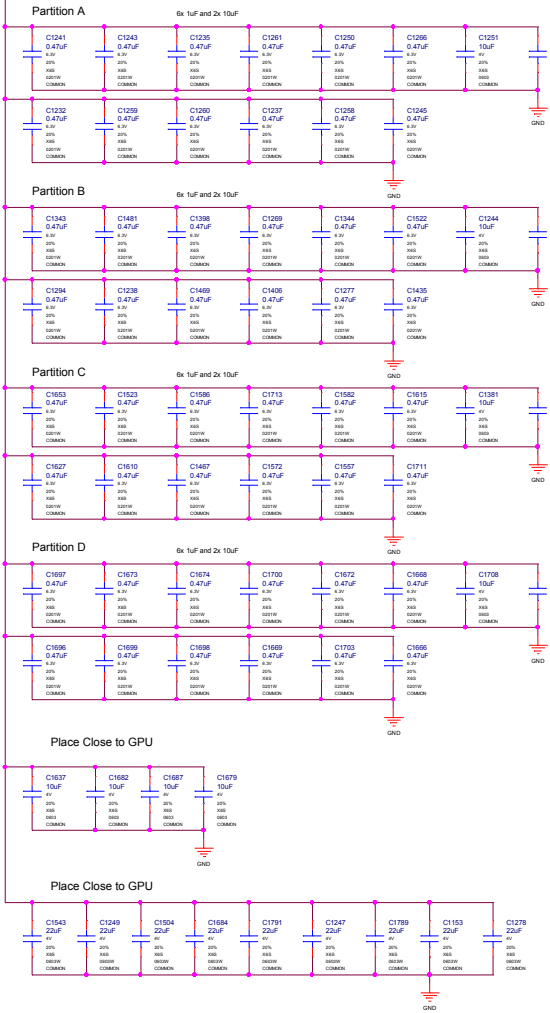
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PCB REV		PG180-A02		PAGE 14 OF 54
BOM REV		A		DATE 27-JUN-2018



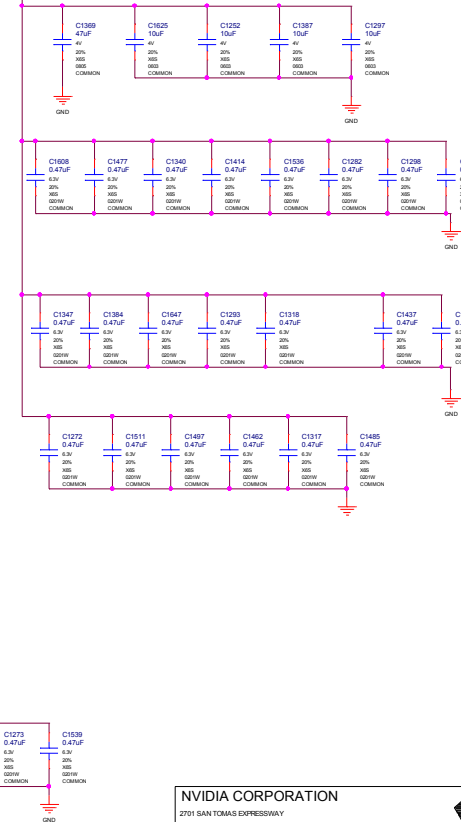


NVDD

FBVDDQ



NVDD



032-0532-000
XBS
0805

ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	GPU Decoupling

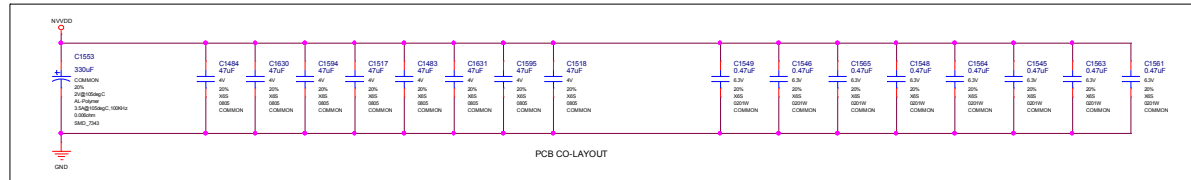
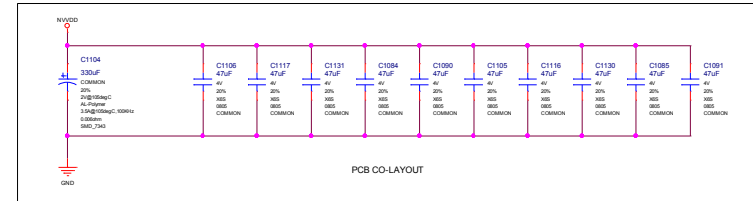
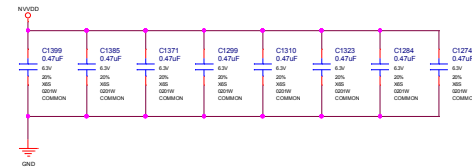
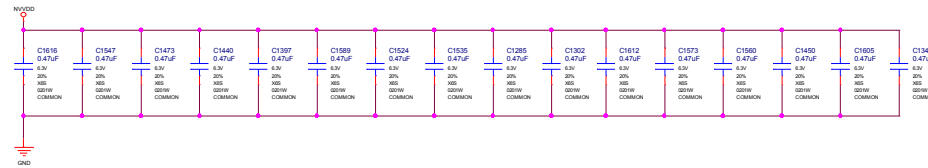
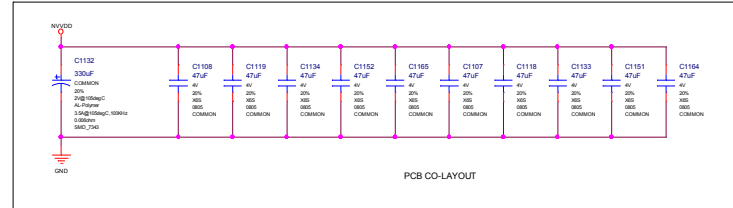
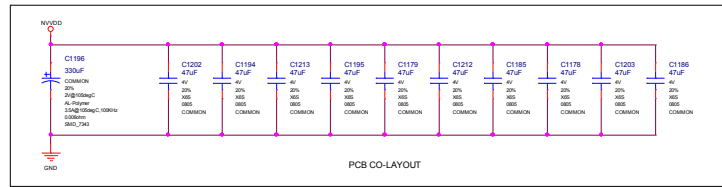
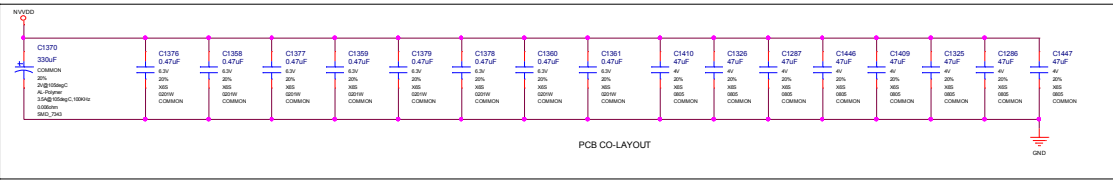
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NCV_P/N 600-IG180-BASE-200

FCB REV	PG180-A02	PAGE	18 OF 54
ROM REV	A	DATE	27-JUN-2018



ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	GPU DECOUPLING

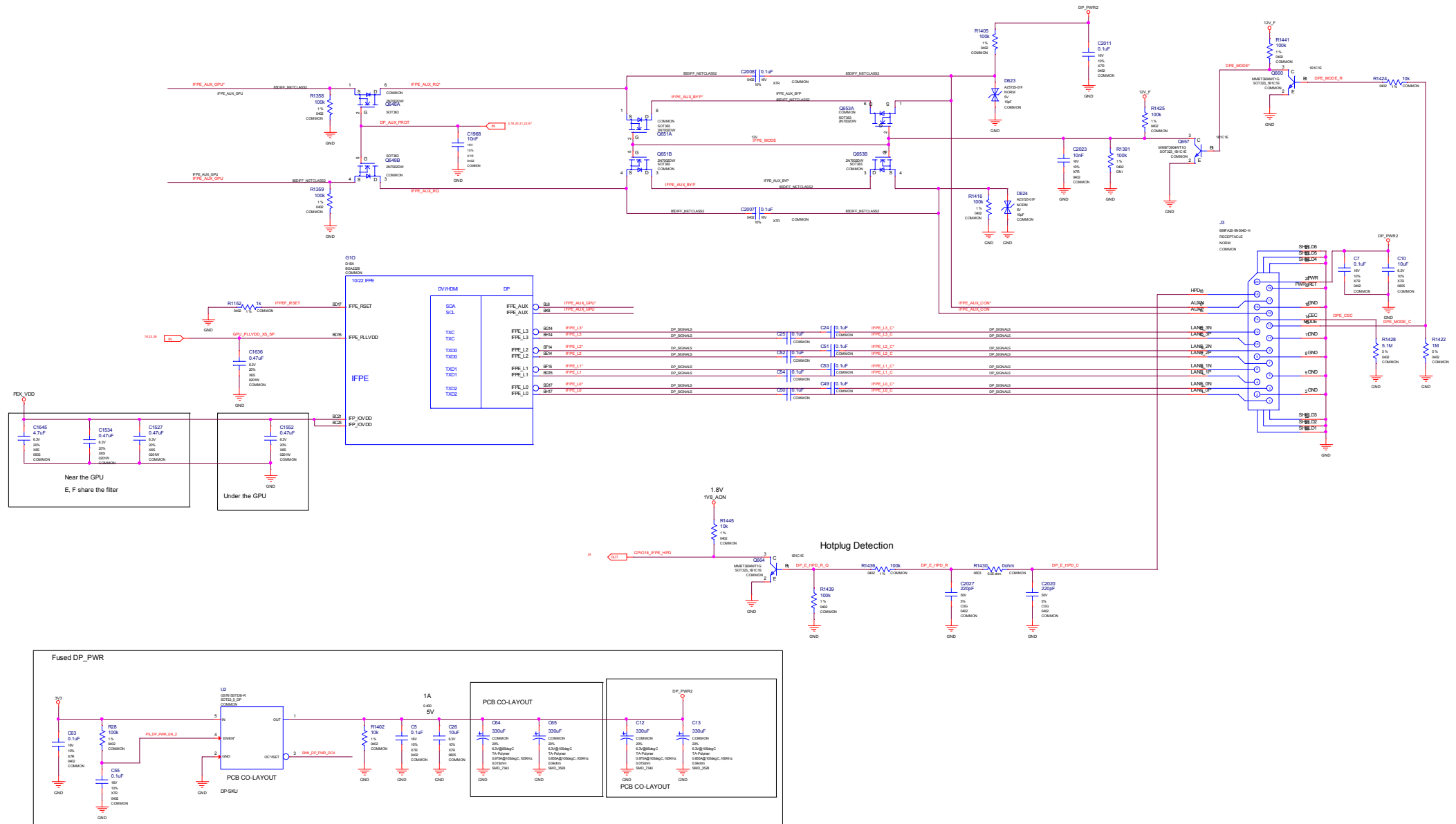
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NV_PN	600-1G180-BASE-200
PCB REV	PG180-A02
BCM REV	A
PAGE	17 OF 54
DATE	27-JUN-2018

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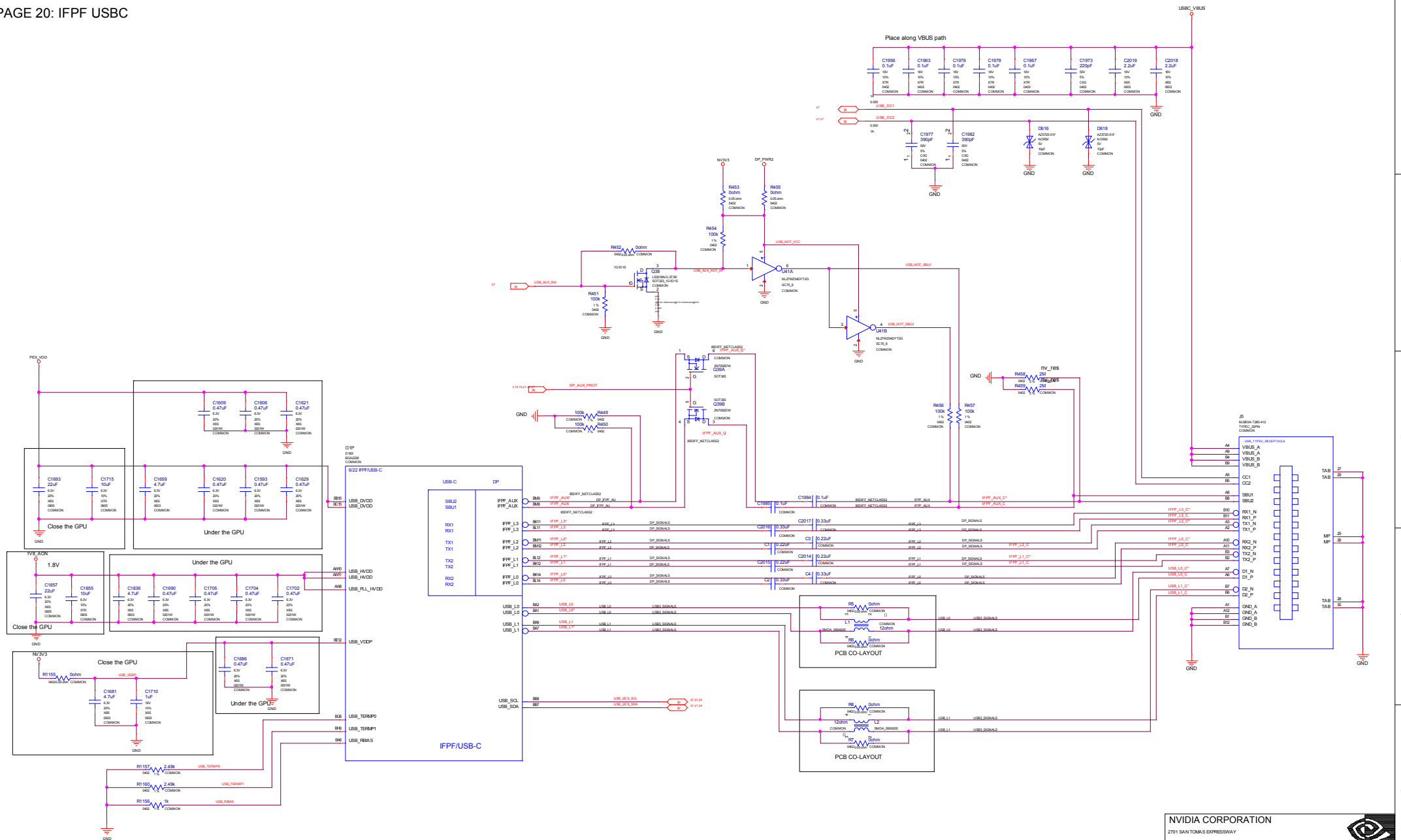
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PCB REV PG180-A02 PAGE 19 OF 54
BCM REV A DATE 27-JUN-2018

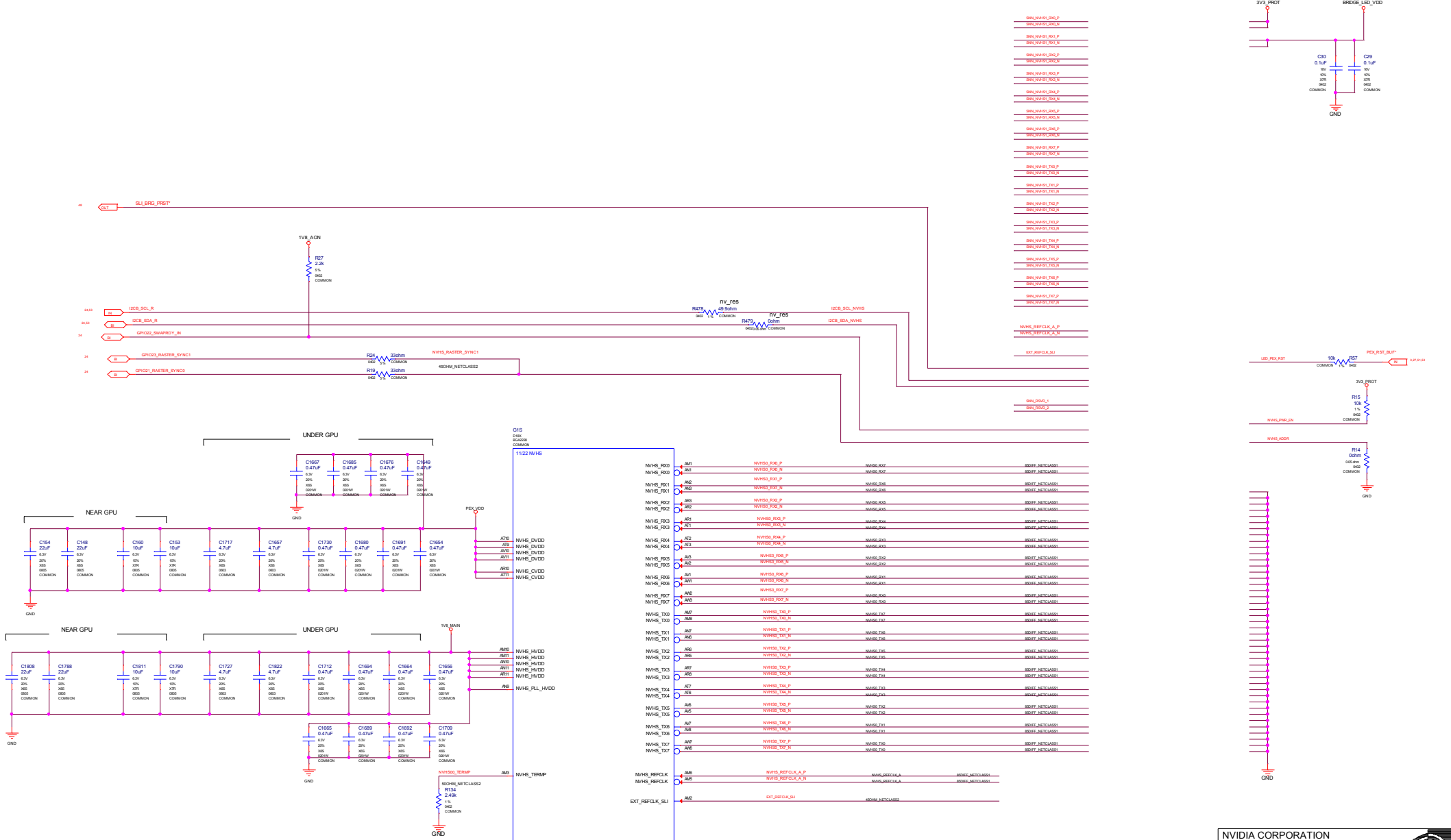
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INV_PN	600-1G180-BASE-200	PKG	26 OF 54
PCB REV	PG180-A02	DATE	27-JUN-2018
BCM REV	A		



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NV_PN		600-1G180-BASE-200	
PCB REV	PG180-A02	PAGE	23 OF 54
ROM REV	A	DATE	27 JUN 2018

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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	NVHS INTERFACE

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

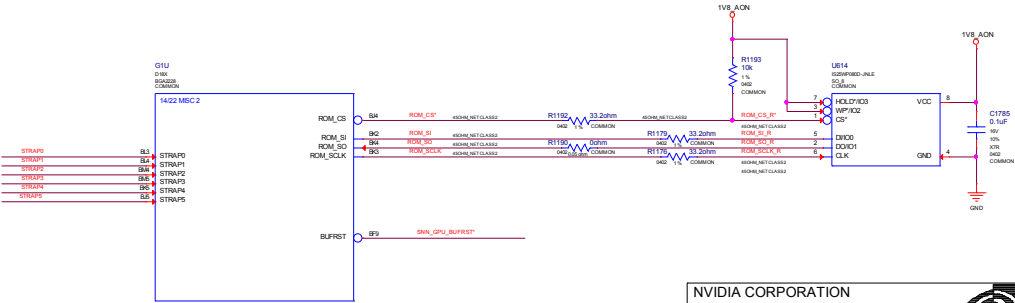
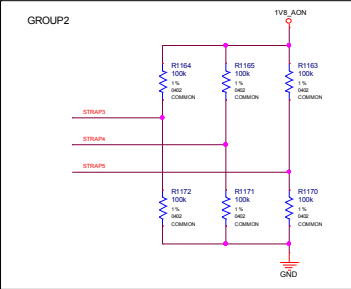
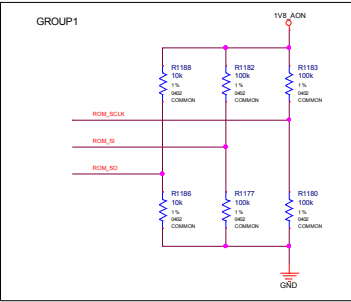
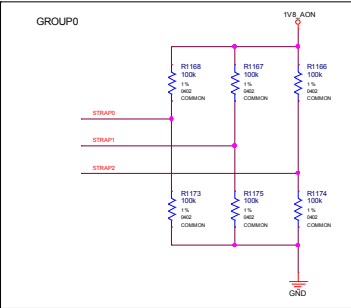
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STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

- 1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
- 1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
- 1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
- 1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Default

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE:DETAIL	MISC3: ROM STRAPS

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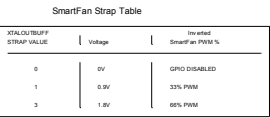
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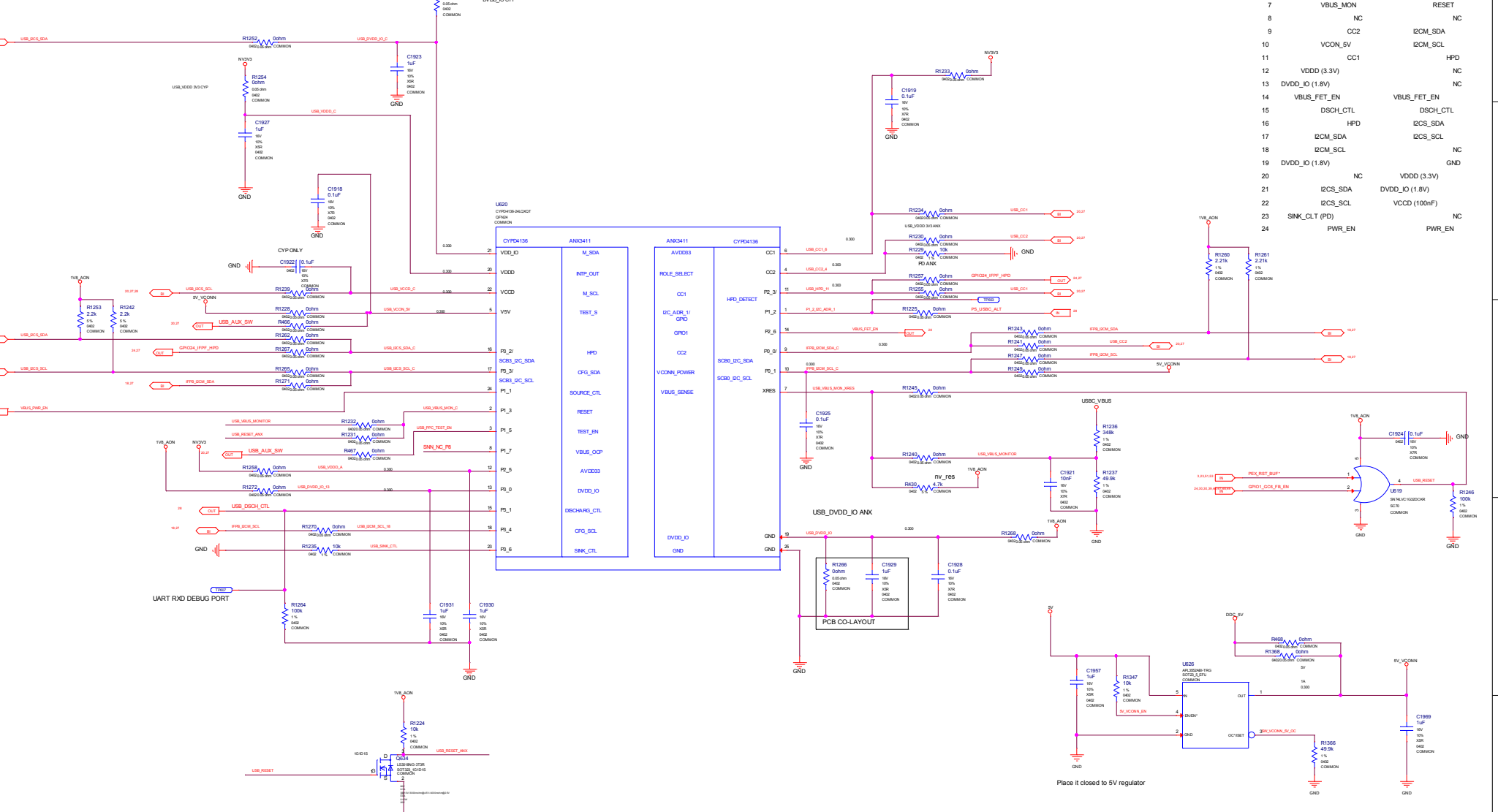
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27-JUN-2018

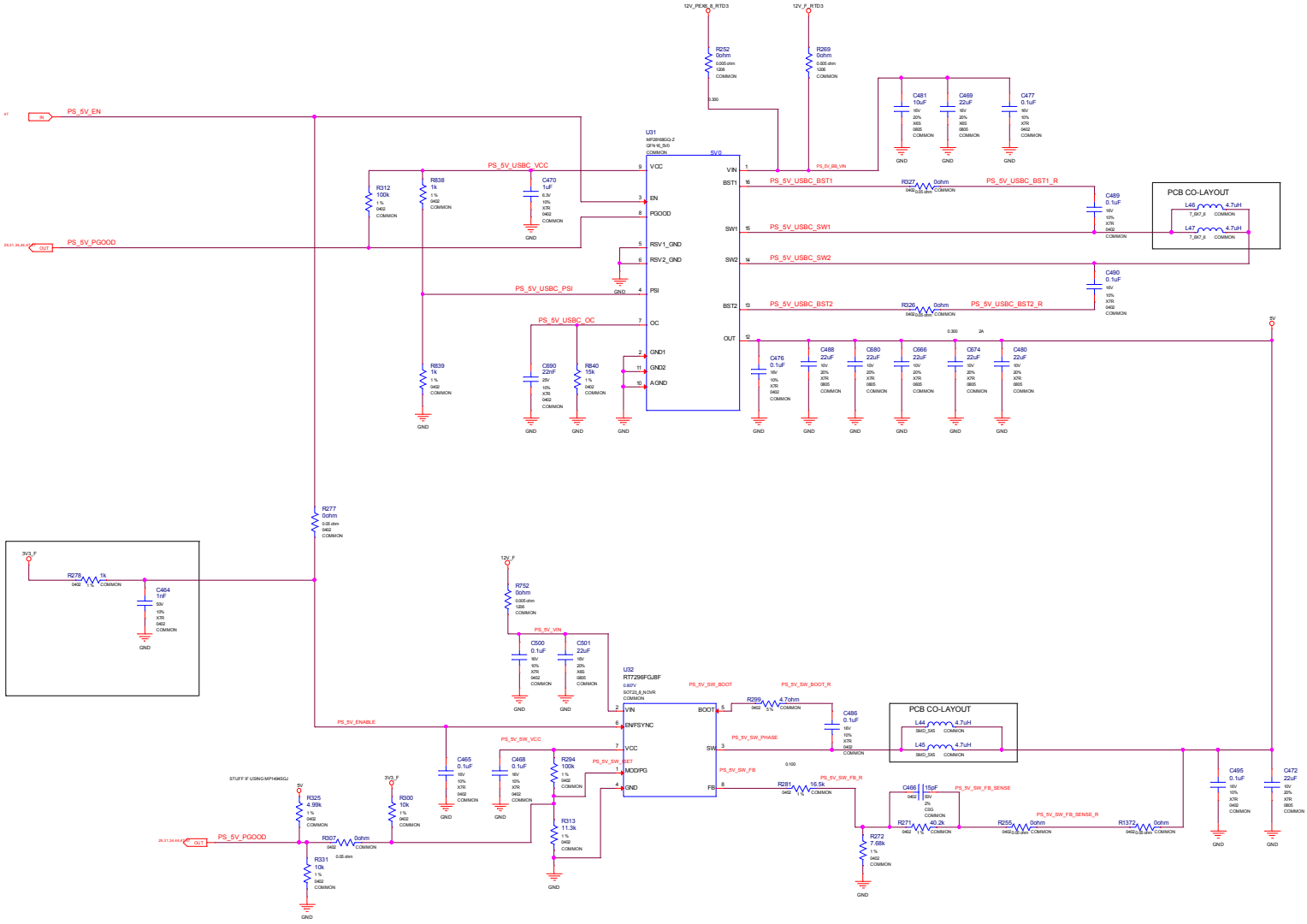


NV_PN	600-1G180-BASE-200		
PCB REV	PG180-A02	PAGE	26 OF 54
BOM REV	A	DATE	27-JUN-2018



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NV_PN		600-1G180-BASE-200		
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BOM REV	A	DATE	27-JUN-2018	

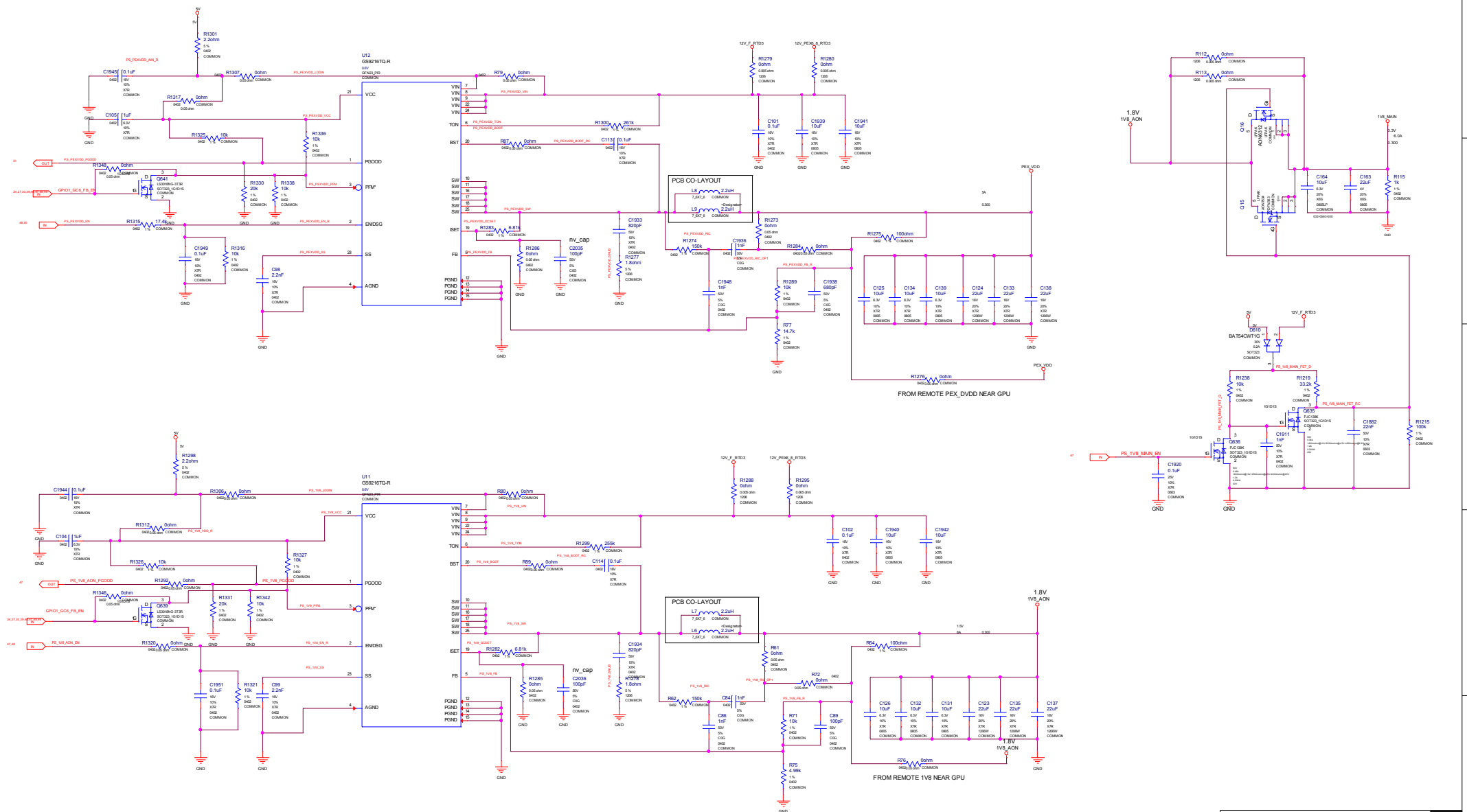
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PAGE:DETAIL	PS: 5V, 5V_BACKUP

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2701 SANTOMAS EXPRESSWAY	
SANTA CLARA, CA 95050, USA	
NV_PN	600-1G180-BASE-200
PCB REV	PG180-A02
ROM REV	A
PAGE	29 OF 54
DATE	27-JUN-2018



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PEXVDD, 1V8

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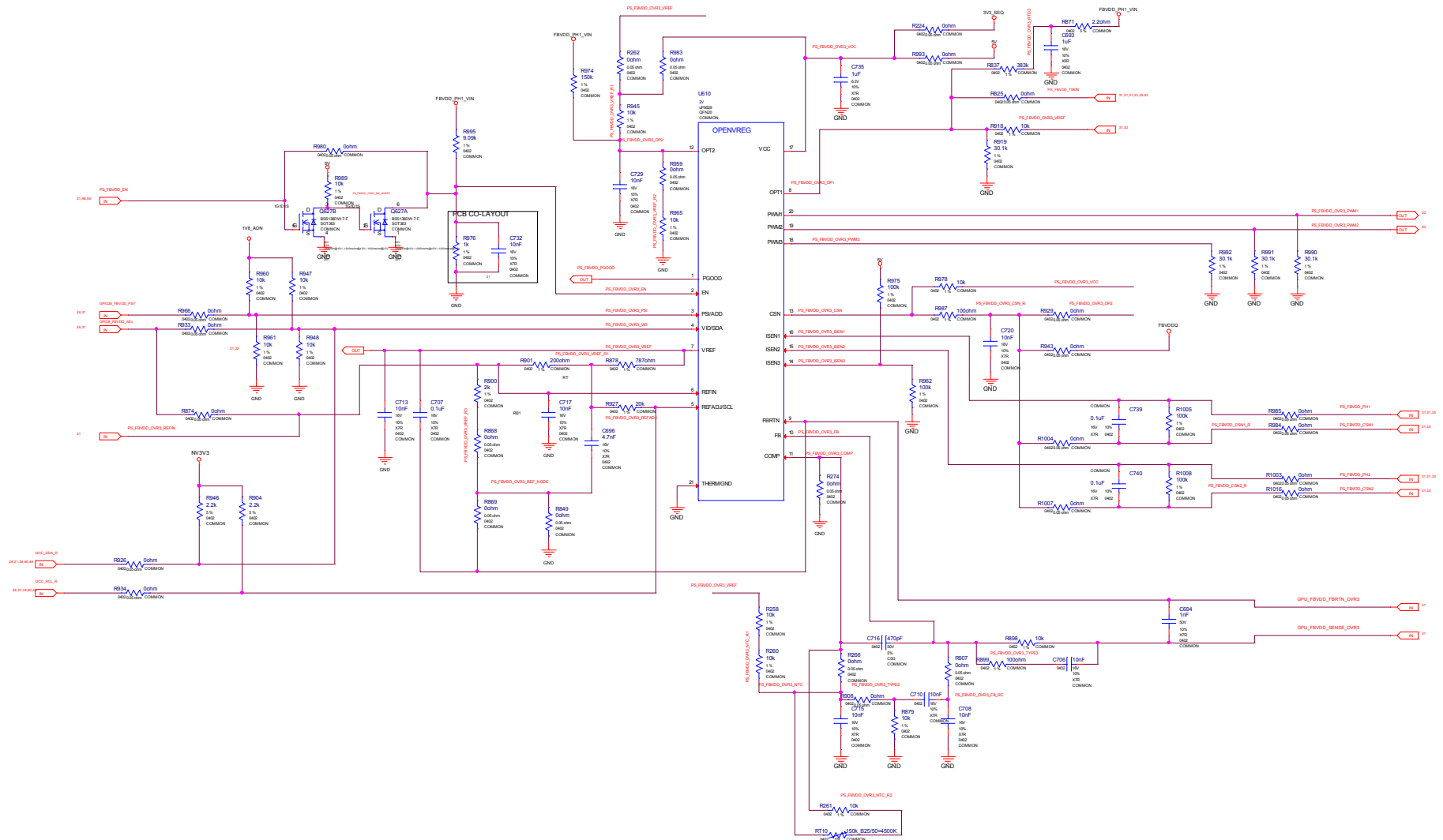
PCB REV	PG180-A02	PAGE	30 OF 54
BCM REV	A	DATE	27-JUN-2018

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NV_PN	600-1G180-BASE-200		
PCB REV	PG180-A02	PAGE	31 OF 54
BOM REV	A	DATE	27-JUN-2018



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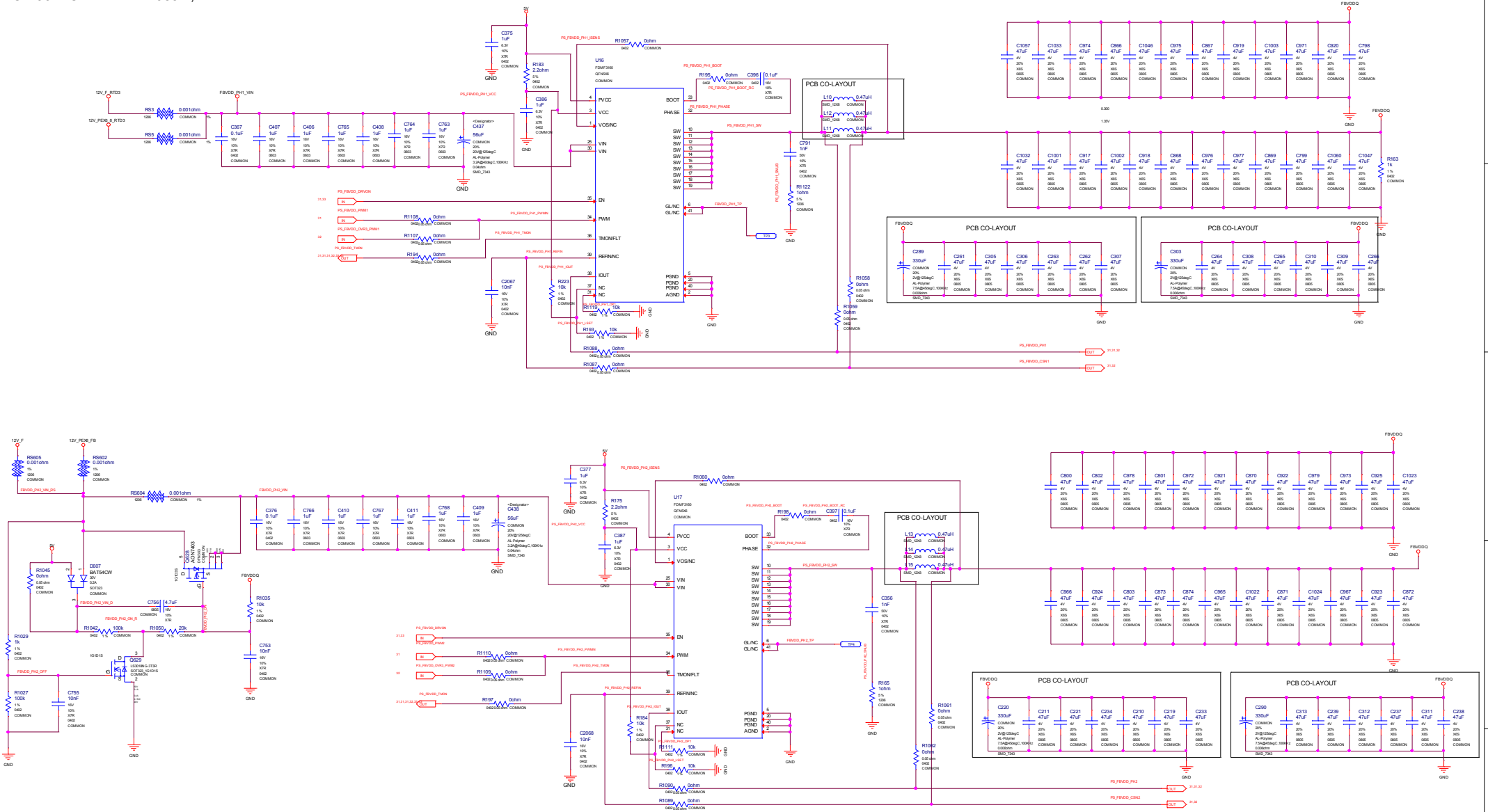
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NV_PN 600-1G180-BASE-200

PCB REV	PGT80-A02	PAGE	32 OF 54
BCM REV	A	DATE	27-JUN-2018

ASSEMBLY	ASSEMBLY DESCRIPTION
PCB DETAIL	PS: FBVDD CONTROLLER OVR3

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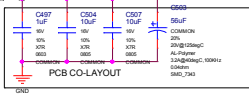
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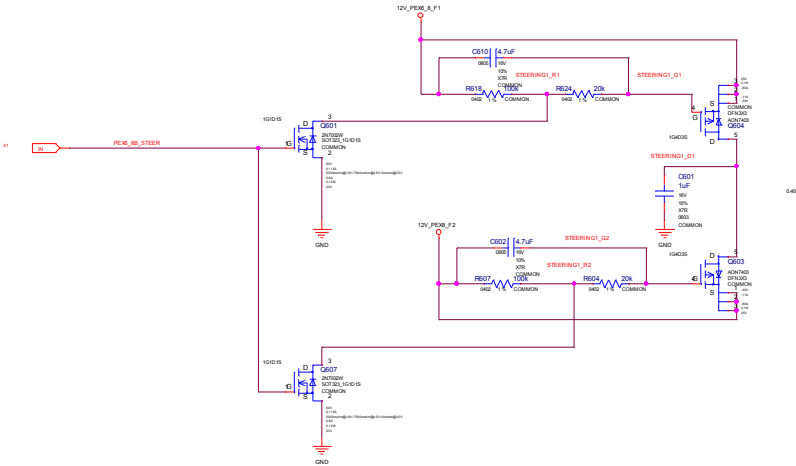
PCB REV	PG180-A02	PAGE	33 OF 54
BCM REV	A	DATE	27-JUN-2018

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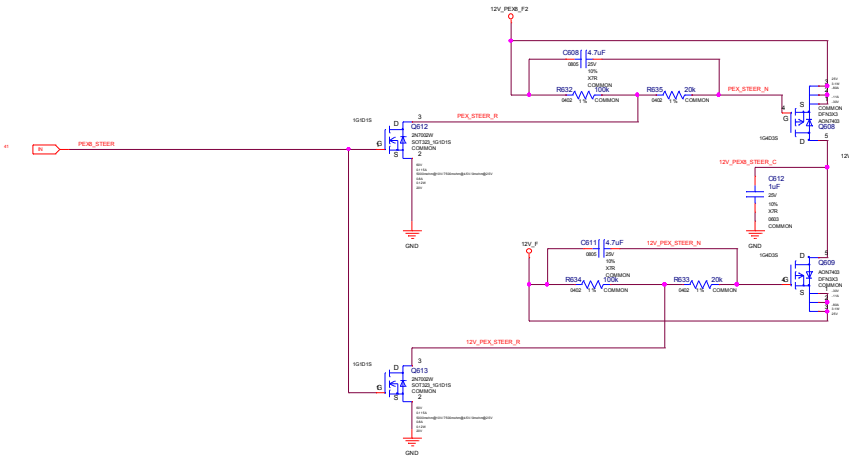


NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN		600-1G180-BASE-200	
PCB REV	P1G180-A02	PAGE	40 OF 54
BOM REV	A	DATE	27-JUN-2018

12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



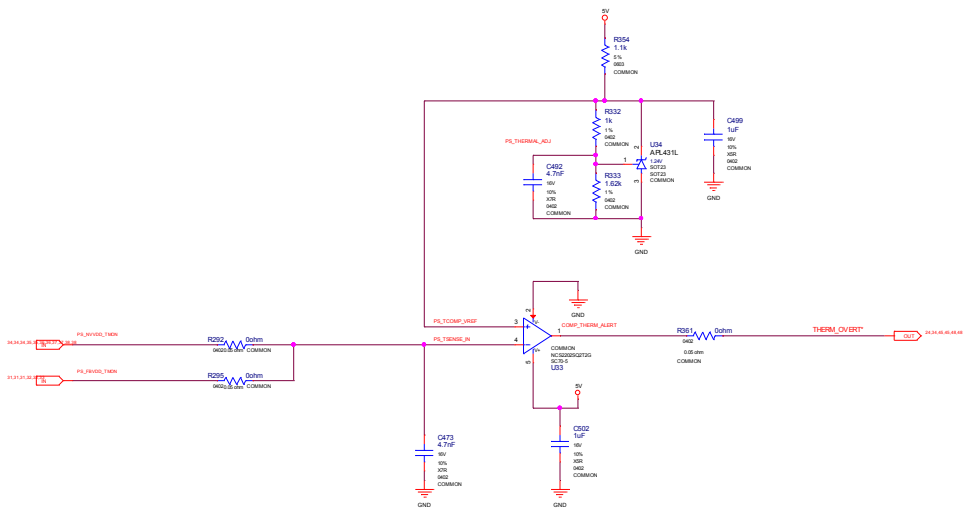
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	PS: 12V CURRENT STEERING

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2701 SAN TOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-1G180-BASE-200		
PCB REV	PG180-A02	PAGE	42 OF 54
BCM REV	A	DATE	27-JUN-2018

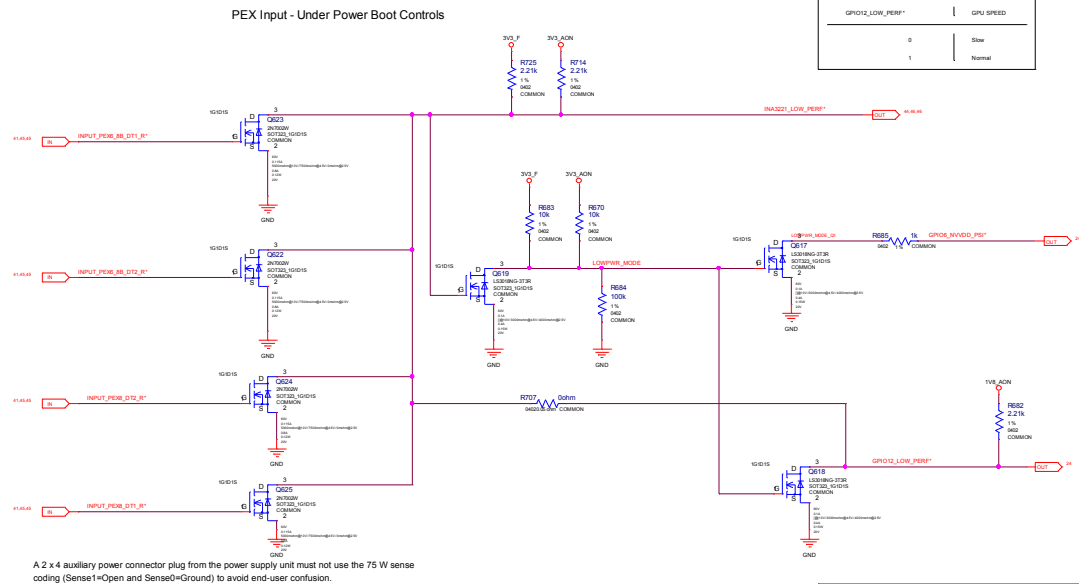
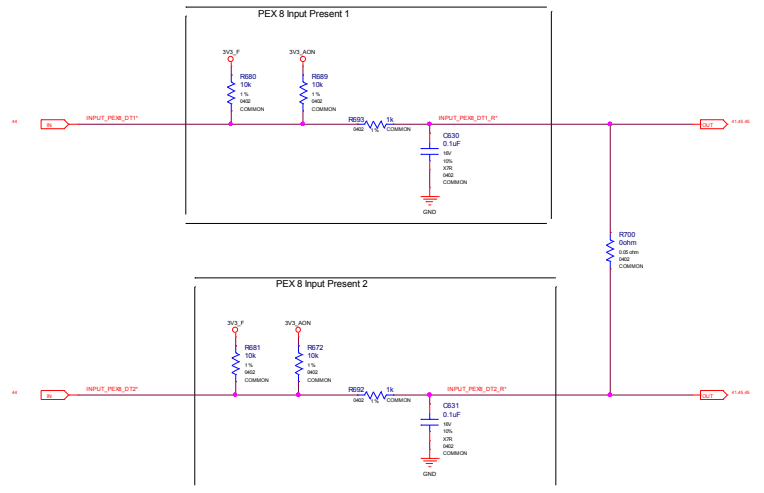


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2701 SANTOMAS EXPRESSWAY			
SANTA CLARA, CA 95050, USA			
NV_PN	600-1G180-BASE-200		
PCB REV	PG180-A02	PAGE	43 OF 54
ROM REV	A	DATE	27 JUN 2018

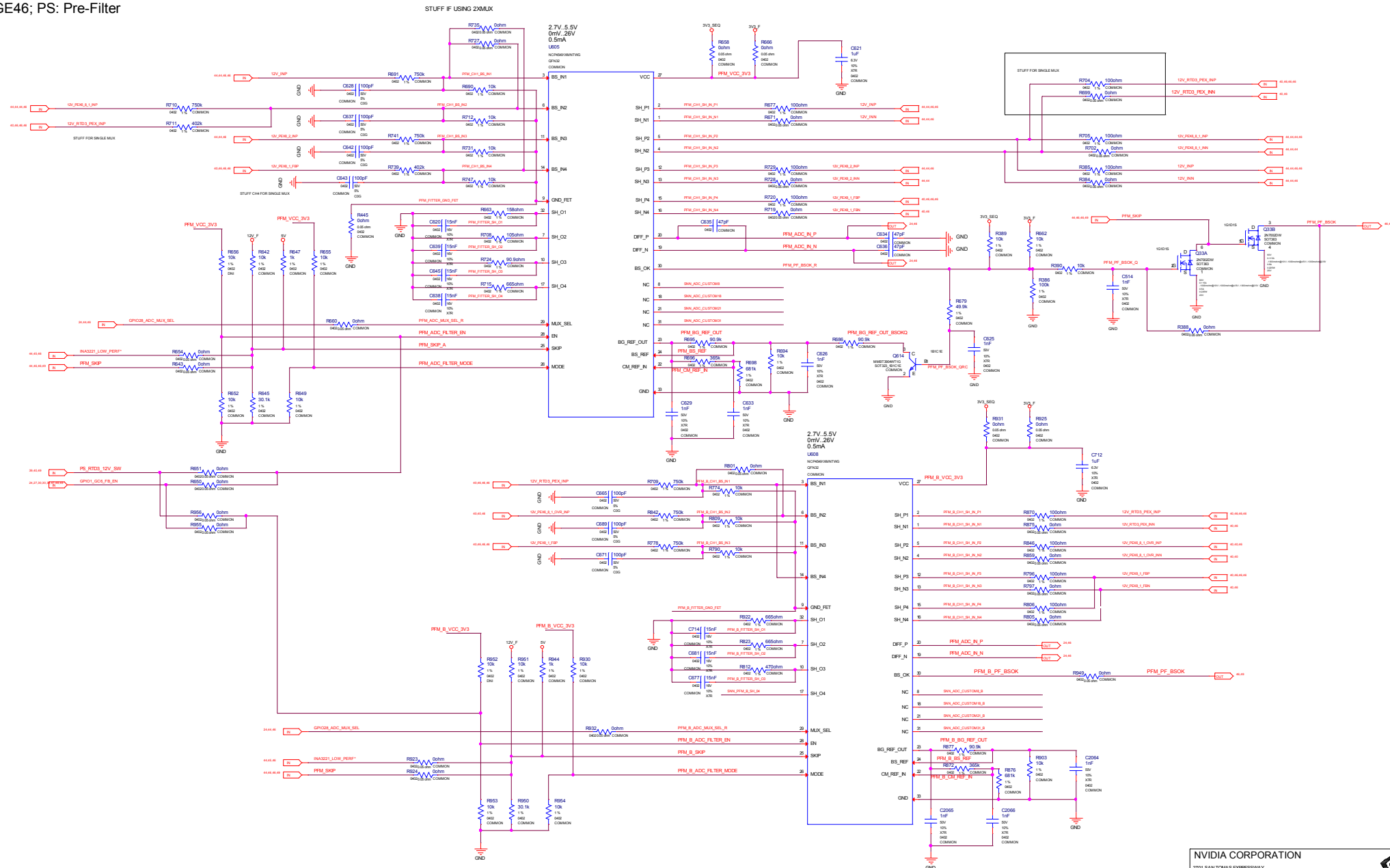




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DATE	27-JUN-2018
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NVIDIA CORPORATION

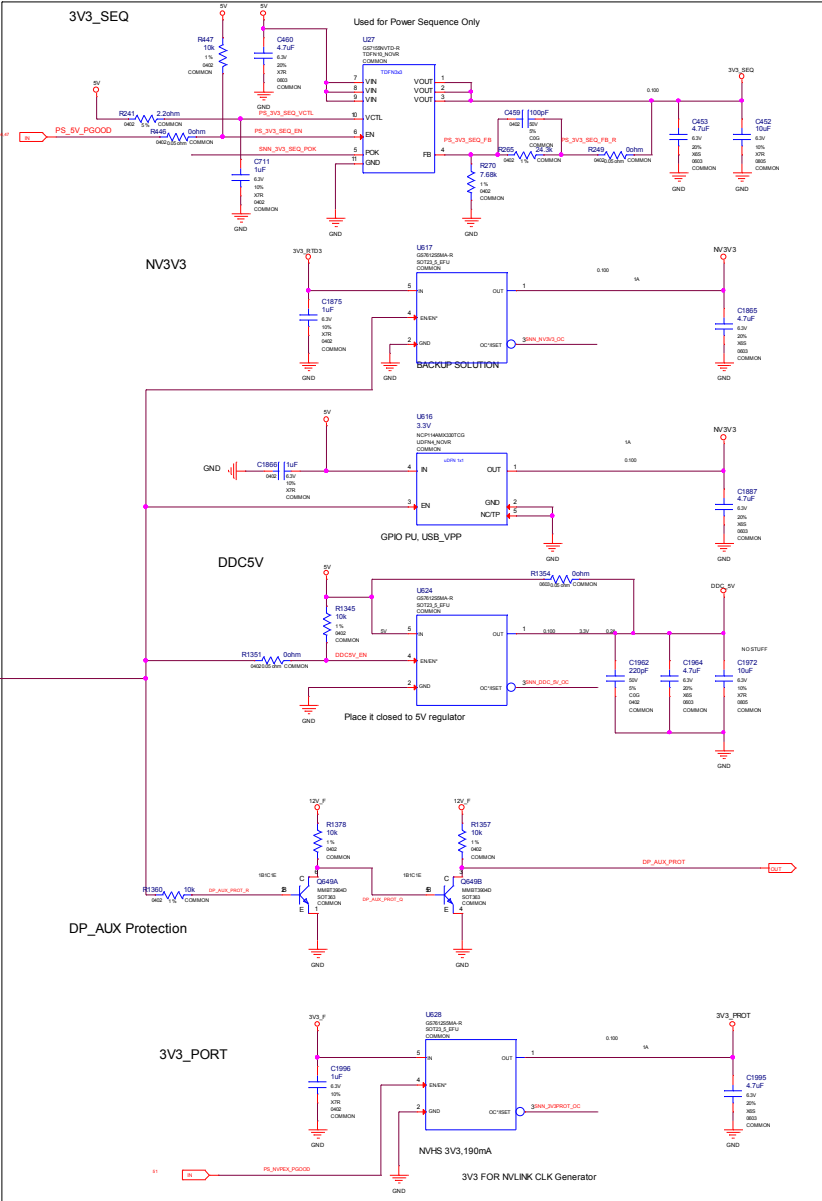
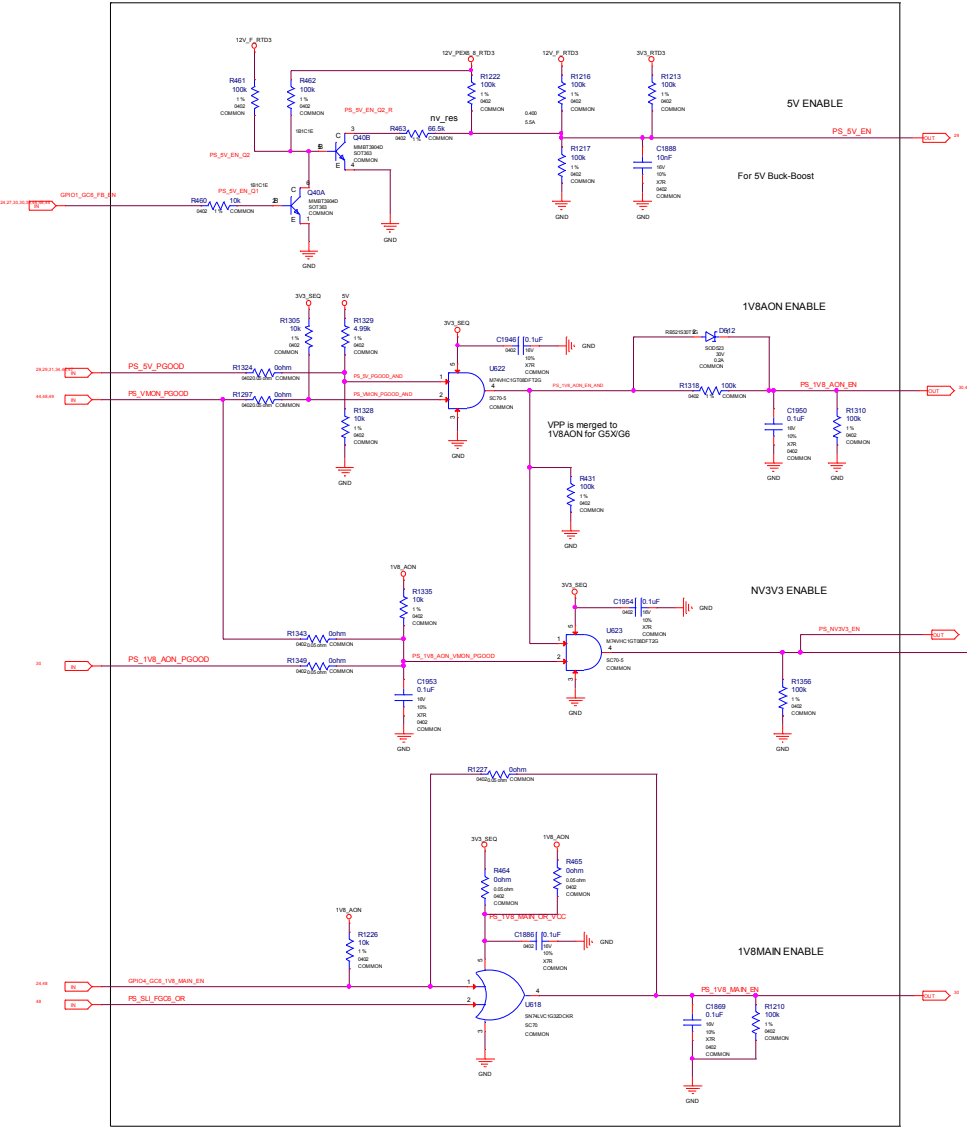
2701 SAN TOMAS EXPRESSWAY
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NV_PN	600-1G180-BASE-200
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PCB REV	PG180-A02	PAGE	46 OF 5
BOM REV	A	DATE	27-JUN-2018

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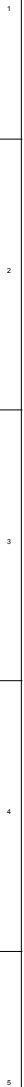


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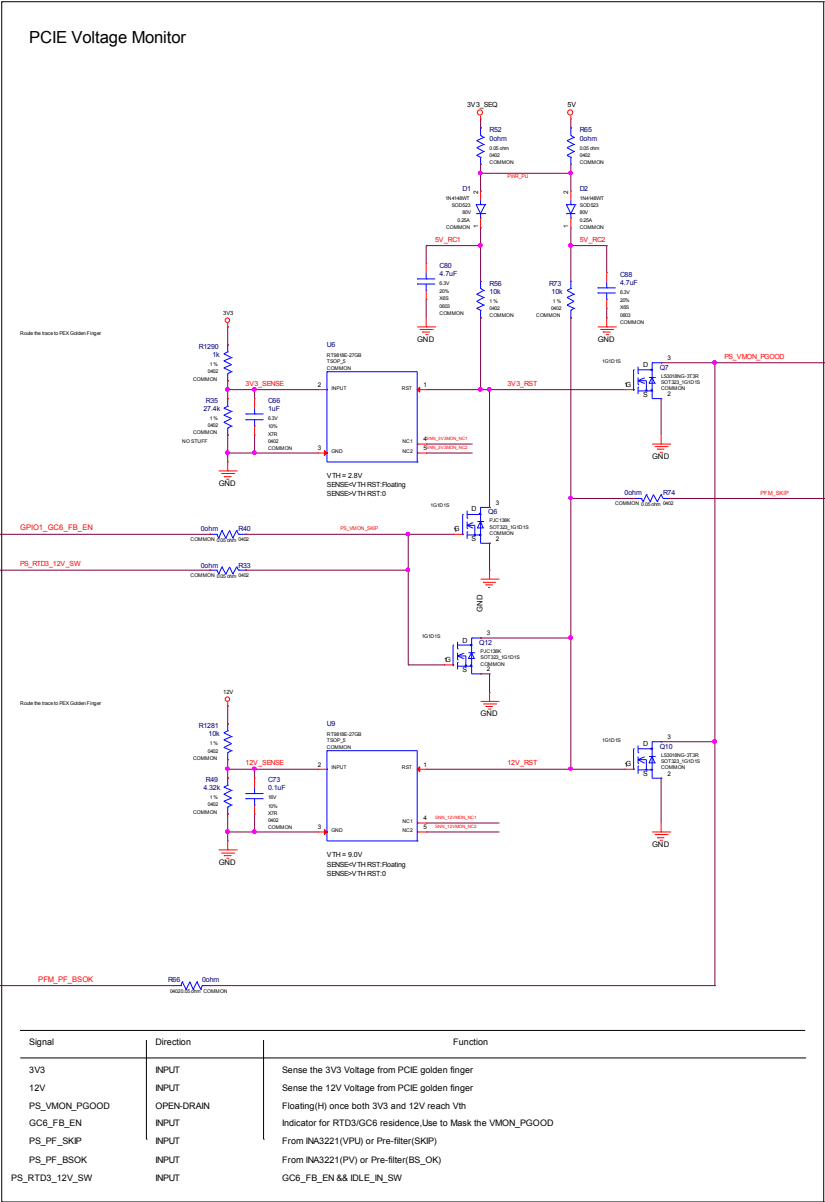
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NV_PN	600-1G180-BASE-200
PCB REV	PG180-A02
DATE	27-JUN-2018
PCB REV	A
DATE	27-JUN-2018





ASSEMBLY	<ASSEMBLY__DESCRIPTION>
PAGE DETAIL	SEQUENCE: NV, PEX, FB ENABU

A	B	C	D	E	F	G	H
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BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ
Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs

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PCB REV

PG180-A02

ROM REV

A

PAGE

49 OF 54

DATE

27-JUN-2018

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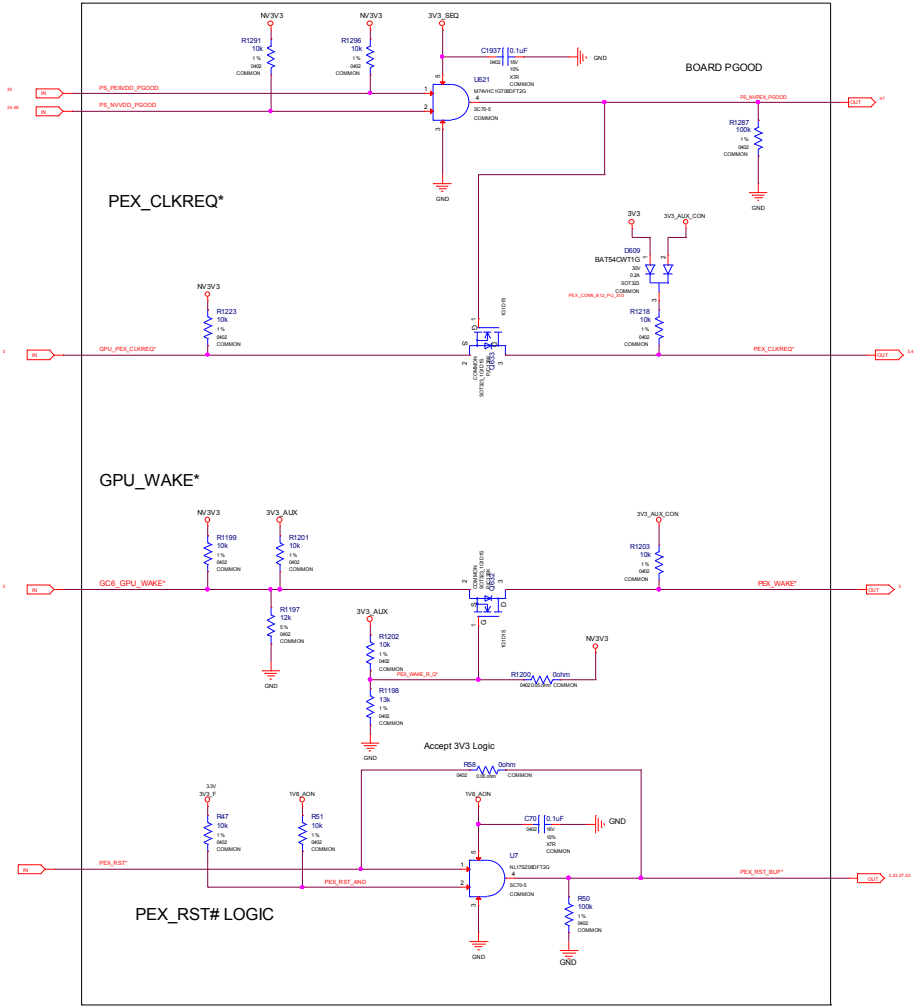
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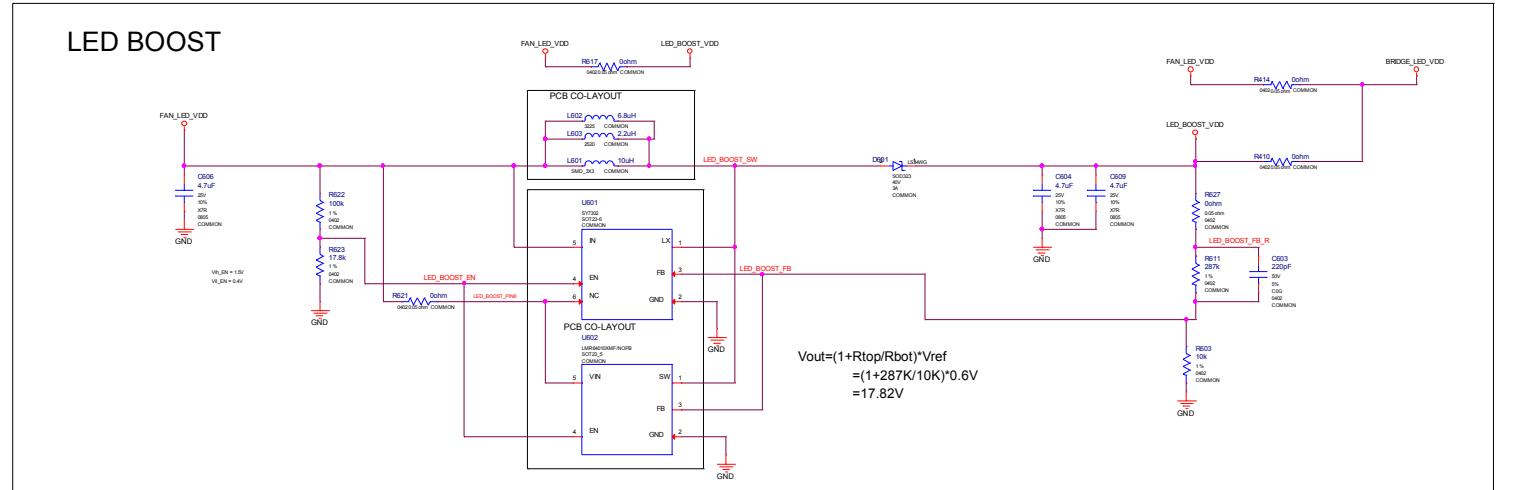
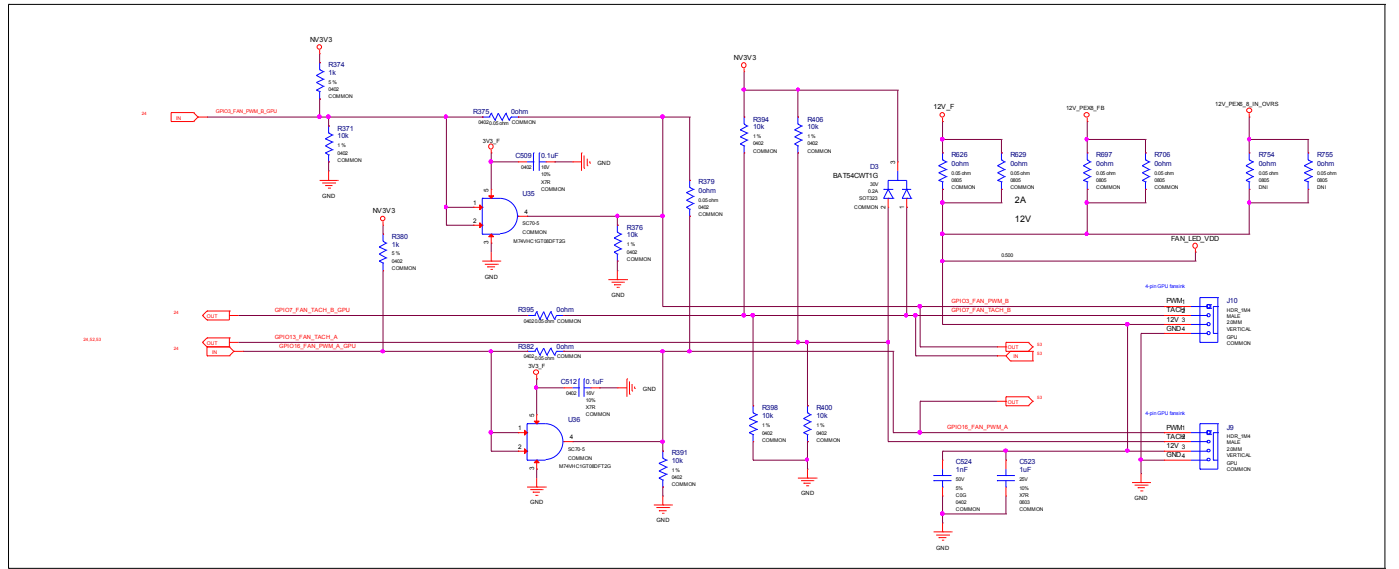
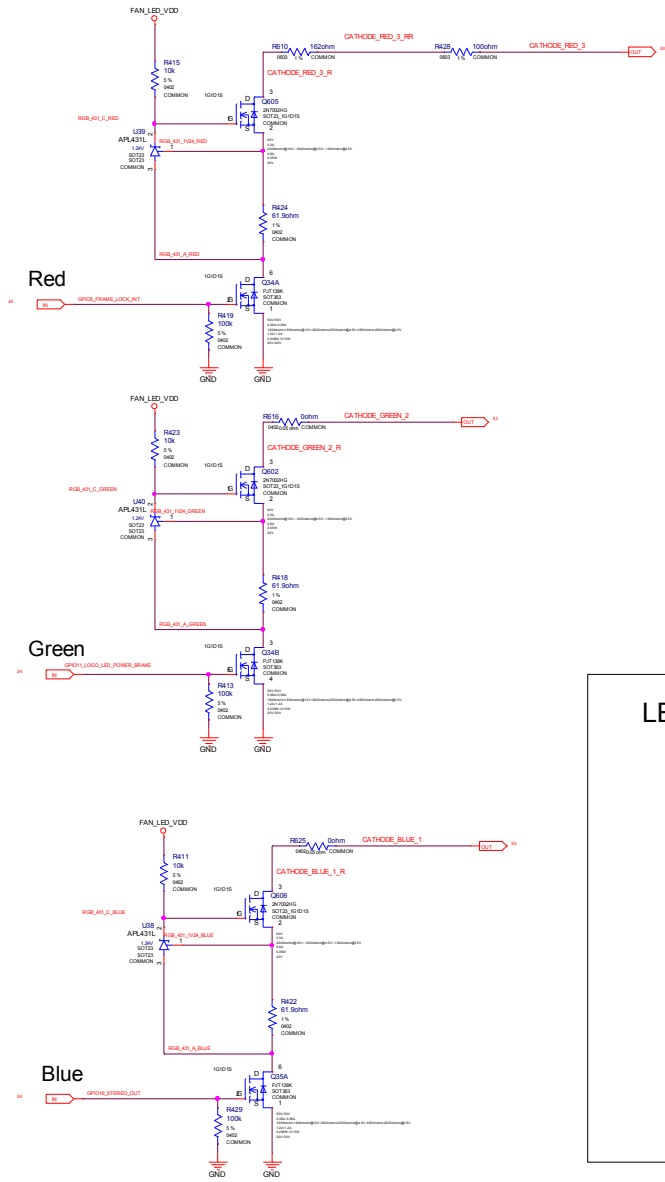
PCB REV	PG180-A02	PAGE	50 OF 54
BOM REV	A	DATE	27-JUN-2018



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PAGE DETAIL	SEQUENCE: MISC

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NV_PN	600-1G180-BASE-200		
PCB REV	PG180-A02	PAGE	51 OF 54
BCM REV	A	DATE	27-JUN-2018

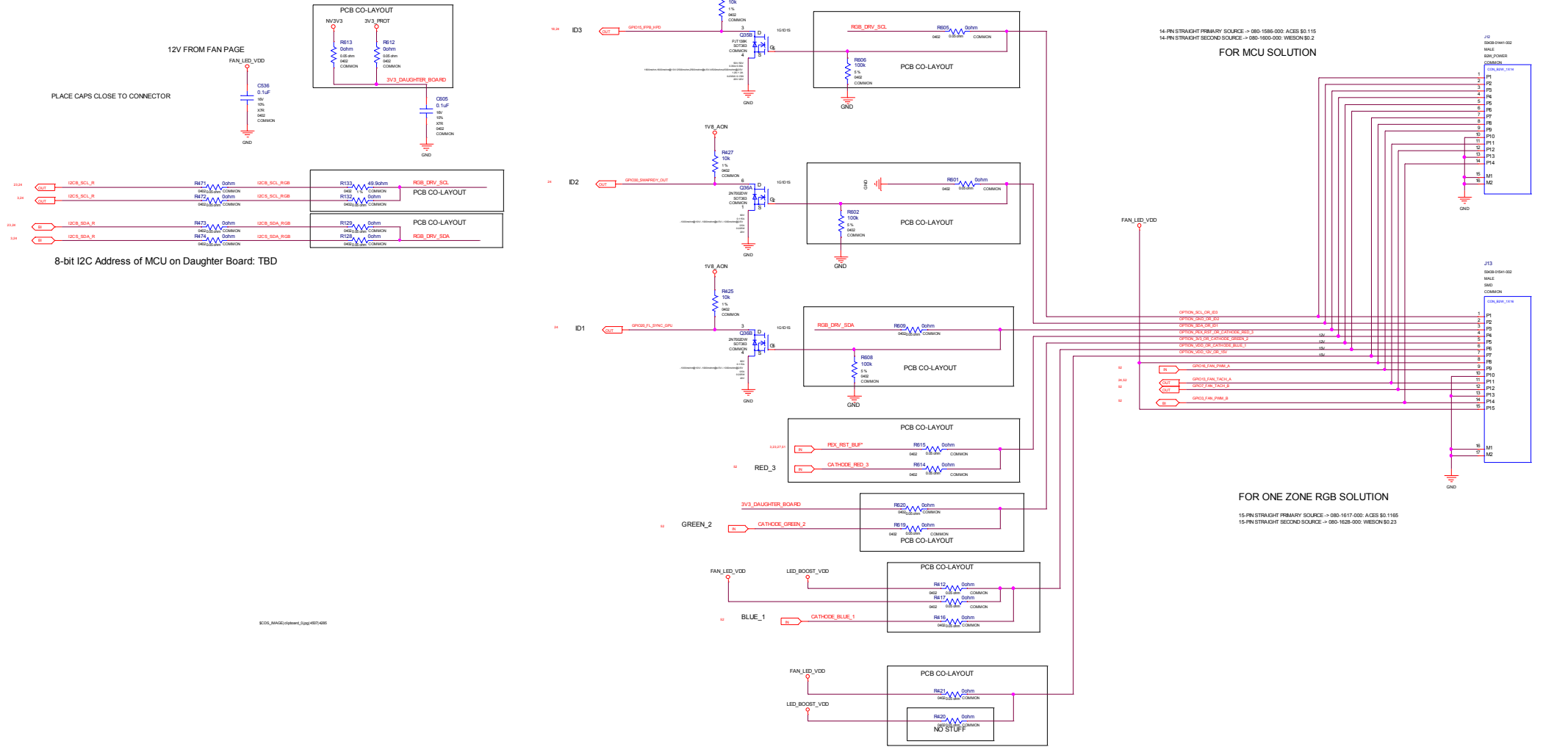


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PAGE DETAIL	LED & FAN HEADERS

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NV_PN	600-1G180-BASE-200
PCB REV	PG180-A02
BCM REV	A
PAGE	52 OF 54
DATE	27-JUN-2018



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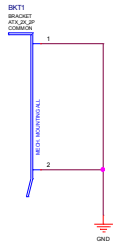
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ASSEMBLY	ASSEMBLY DESCRIPTION
PAGE DETAIL	LED 2

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PCB REV	PG180-A02
PCB REV	A
DATE	27-JUN-2018



Brackets:



Bracket Screw



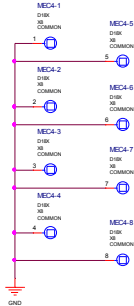
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MEC501

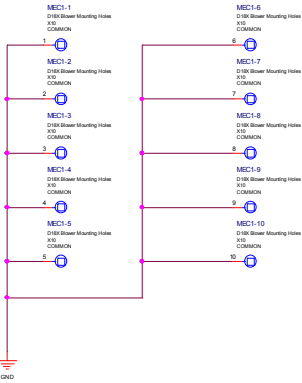
GPU Socket Symbol



GPU Mounting holes



Mechanical Holes Symbol



STIFFENER

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NV_PN	600-1G180-BASE-200	PAGE	54 OF 54
PCB REV	PG180-A02	DATE	27-JUN-2018
BCM REV	A		