

PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

TABLE OF CONTENTS

Page	Description	Page	Description	Page	Description
1	Table of Contents	26	MISC: XTAL, PLL	51	SEQUENCE: MISC
2	Block Diagram	27	MISC: USB PPC	52	LED & FAN HEADERS
3	PCI Express	28	PS: USB VR	53	LED 2
4	PCI Termination	29	PS: 5V, 5V BACKUP	54	Mechanical: Bracket/Thermal Solution
5	MEMORY: GPU Partition A/B	30	PS: PEXVDD, 1V8		
6	MEMORY: FBA Partition 31..0	31	PS: FBVDD CONTROLLER		
7	MEMORY: FBA Partition 63..32	32	PS: FBVDD CONTROLLER OVR3		
8	MEMORY: FBB Partition 31..0	33	PS: FBVDD PHASE 1, 2		
9	MEMORY: FBB Partition 63..32	34	PS: NVVDD CONTROLLER OVR8		
10	MEMORY: GPU Partition C/D	35	PS: NVVDD Phase 1, 2		
11	MEMORY: FBC Partition 31..0	36	PS: NVVDD Phase 3, 4		
12	MEMORY: FBC Partition 63..32	37	PS: NVVDD Phase 5, 6		
13	MEMORY: FBD Partition 31..0	38	PS: NVVDD Phase 7, 8		
14	MEMORY: FBD Partition 63..32	39	PS: INPUT SWITCH RTD3		
15	GPU PWR and GND	40	PS: INPUT SWITCH RTD3 USB		
16	GPU Decoupling	41	PS: INPUT SWITCH RAIL BALANCE		
17	GPU DECOUPLING	42	PS: 12V CURRENT STEERING		
18	IFPAB TALL-DP	43	PS: VR THERMAL PROTECTION		
19	IFPE DP	44	PS: INPUTS, FILTERING AND MONITORING		
20	IFPF USBC	45	PS: CURRENT STEERING,HOT UNPLUG DETECT		
21	IFPC HDMI 2.0/DP	46	PS: PRE-FILTER		
22	IFPD DP	47	SEQUENCE: 5V, 1V8, NV3V3 ENABLE		
23	NVHS INTERFACE	48	SEQUENCE: NV, PEX, FB ENABLE		
24	MISC: FAN,THERMAL,JTAG,GPIO,STEREO	49	SEQUENCE: PCIE VOLTAGE MONITOR		
25	MISC3: ROM, STRAPS	50	SEQUENCE: DISCHARGE		

base on V372-02S change for D18 Z

1. P.23 remove SLI & BRIDGE_LED_VDD & SLI_BRG_PRST*

2. P.52 remove LED change FAN connector

3. P.53 remove LED

4. P.38/44 add FUSE

5. P.5~14 mem add <>

6. P.53 LED use V336-0D

7. P.32 remove

8. P.35~38 dual MOS

9. P.33 change dual MOS

10. P.43 remove

11. P.31 change to UP1666

12. P.21 remove colay DP

0727:

page 24: REMOVE GPIO29_IDLE_IN_SW
remove GPIO9_INPUT_DYN_BAL2

page 29: 12V_F RTD3 change to 12V_F

page 30: 12V_F RTD3 change to 12V_F

page 33: 12V_F RTD3 change to 12V_F
移除保護線路

page 39: remove INPUT SWITCH RTD3

page 40: remove INPUT SWITCH RTD3 USB

page 44: remove INA3221

page 46: remove PFM_SKIP net
remove PS_RTD3_12V_SW net

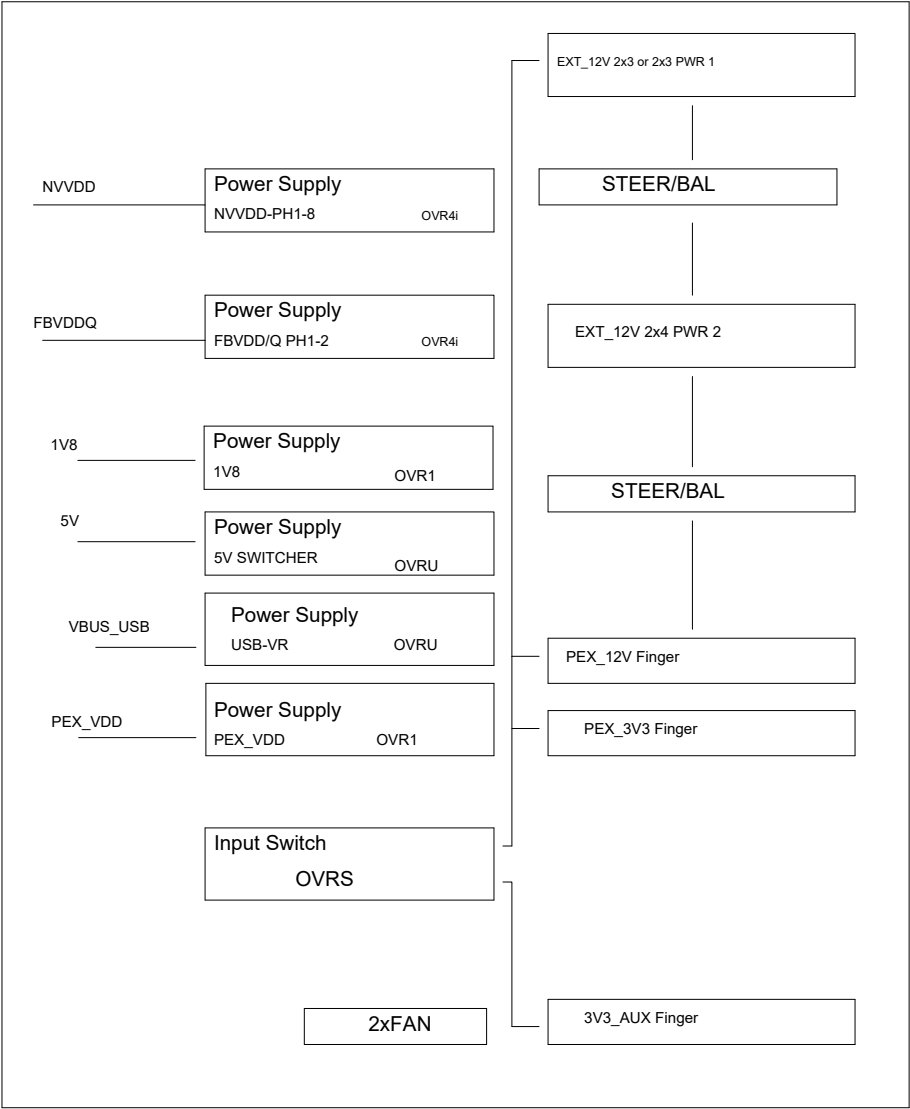
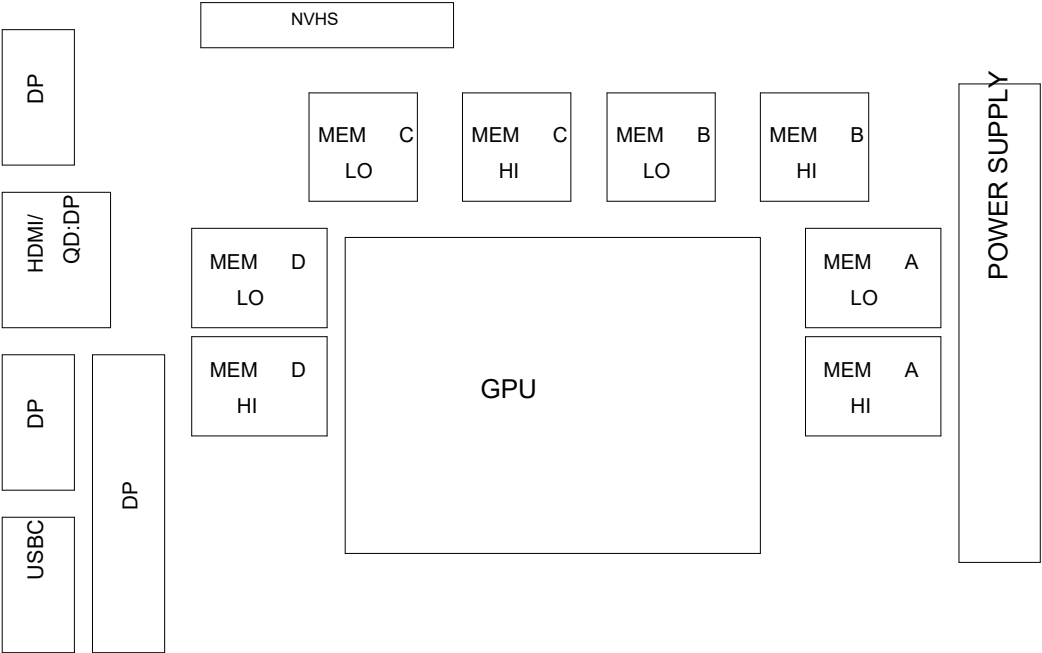
page 47: remove PS_VMON_PGOOD net
12V_F RTD3 change to 12V_F
remove 3V3_PORT
remove 3V3_RTD3 change to nv3v3

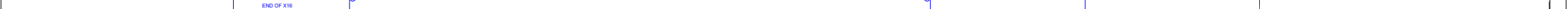
page 48: remove OC_CRIT* NET from ina3221
remove PS_VMON_PGOOD net

page 49: PCIE Voltage Monitor1

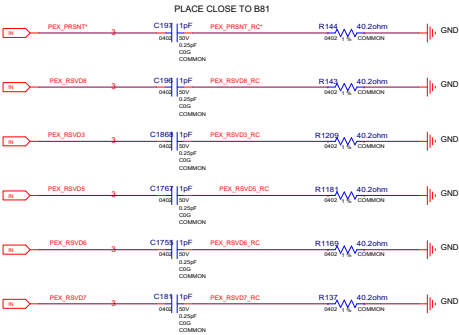
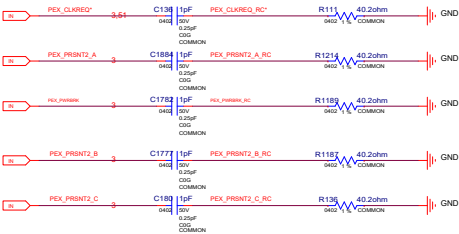
page 52: REMOVE VIN =>12V_PEX6_8_IN_OVRS

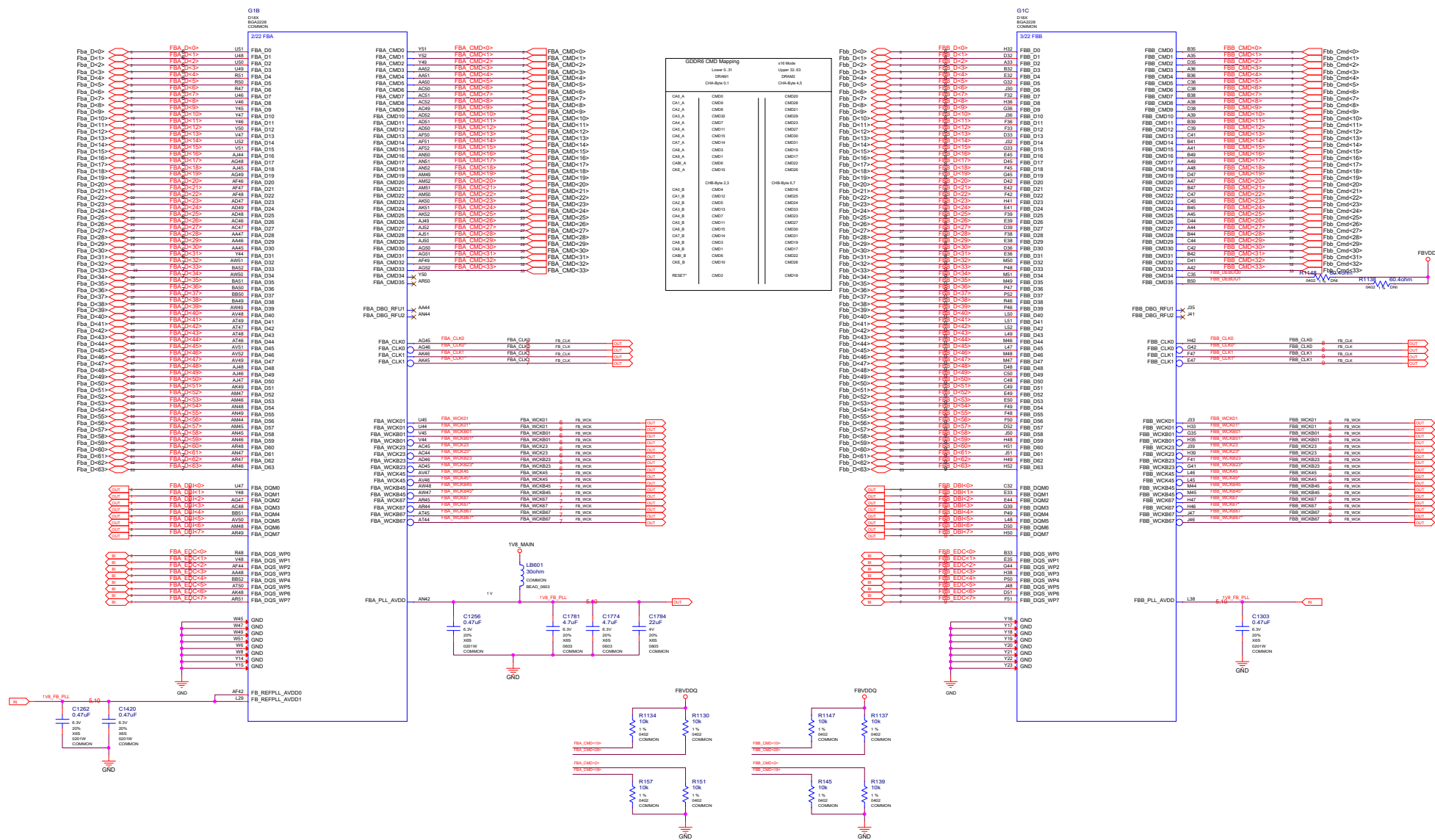
page 54: change GPU scrow holes to small size

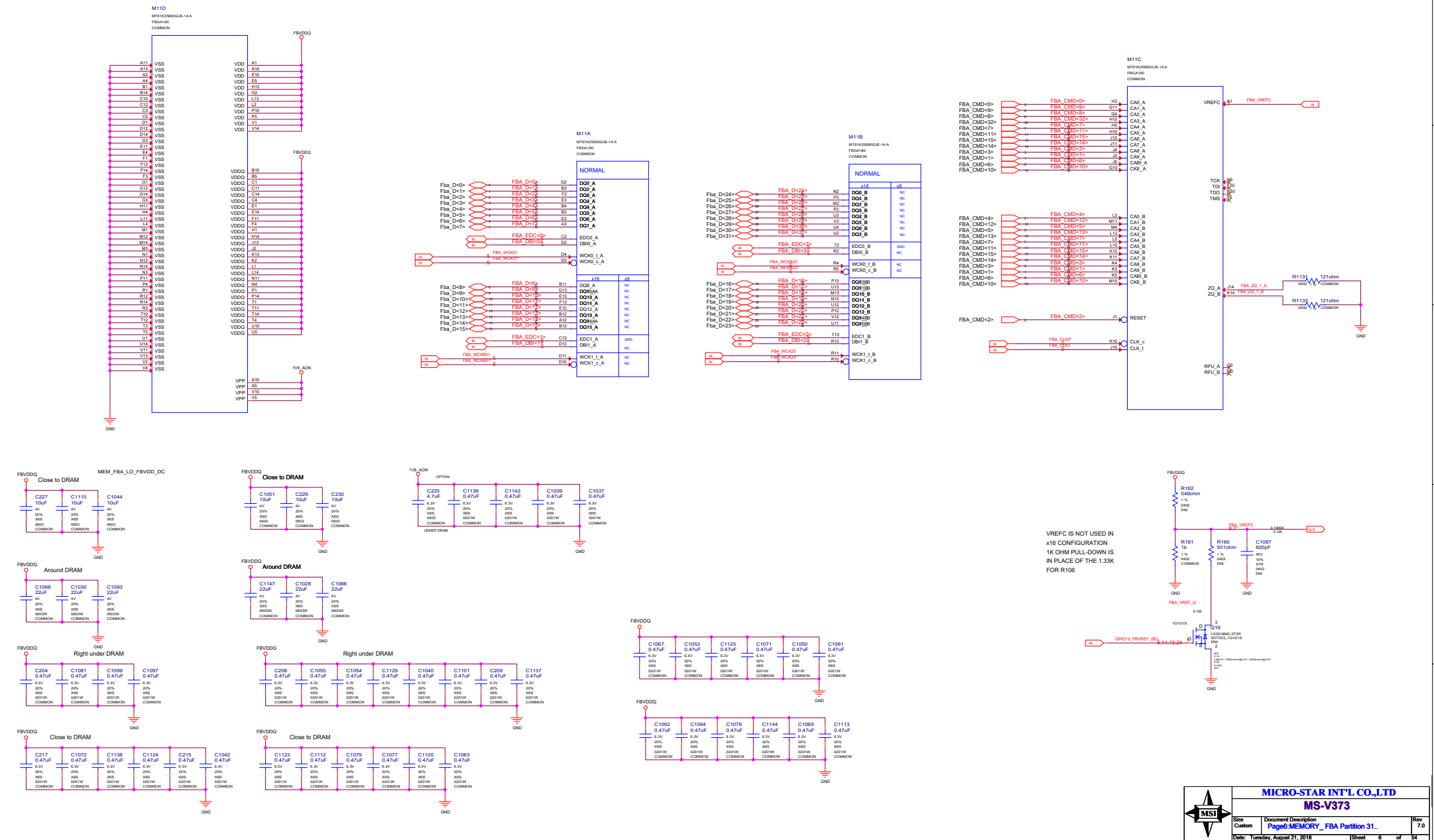


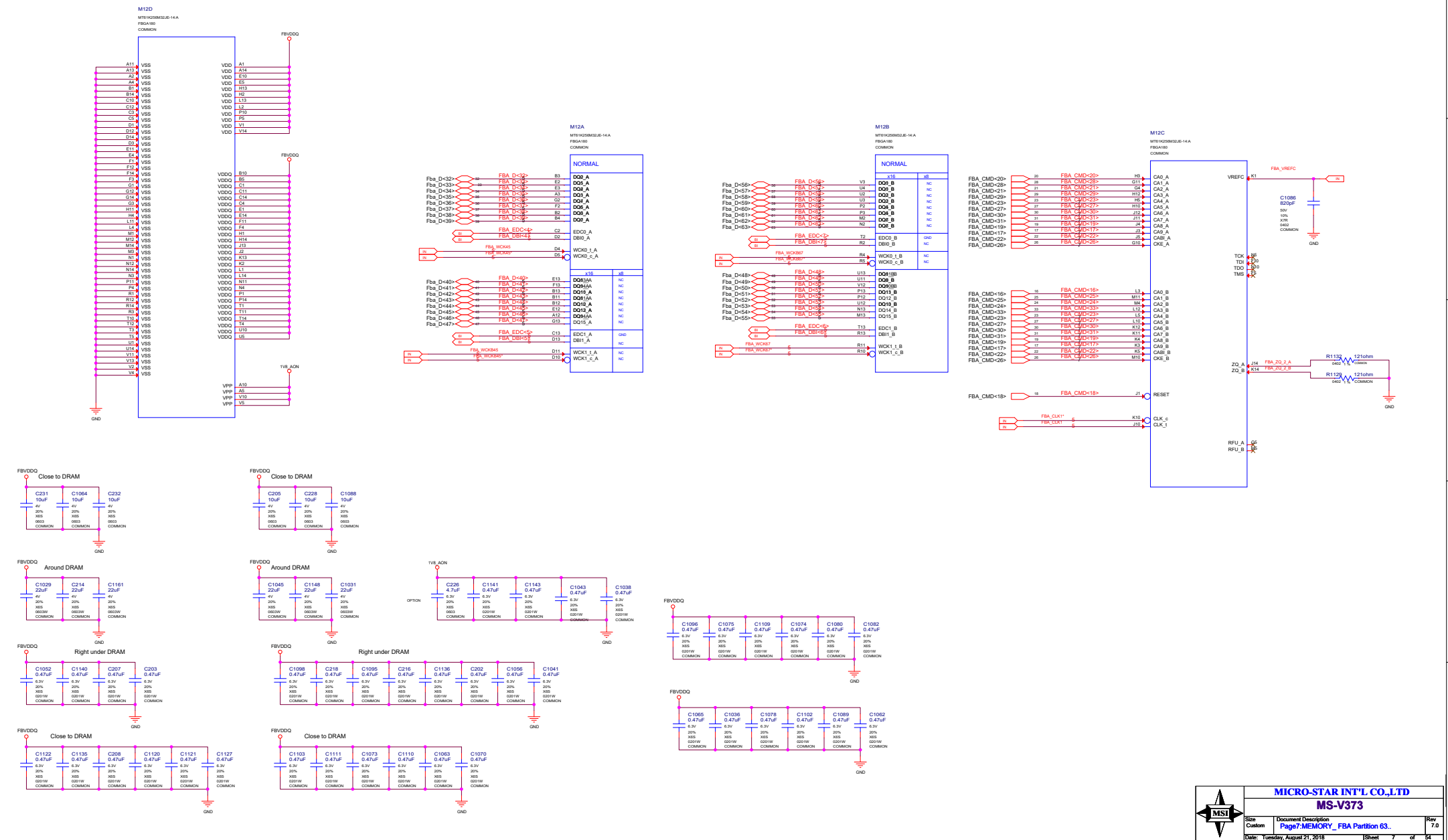


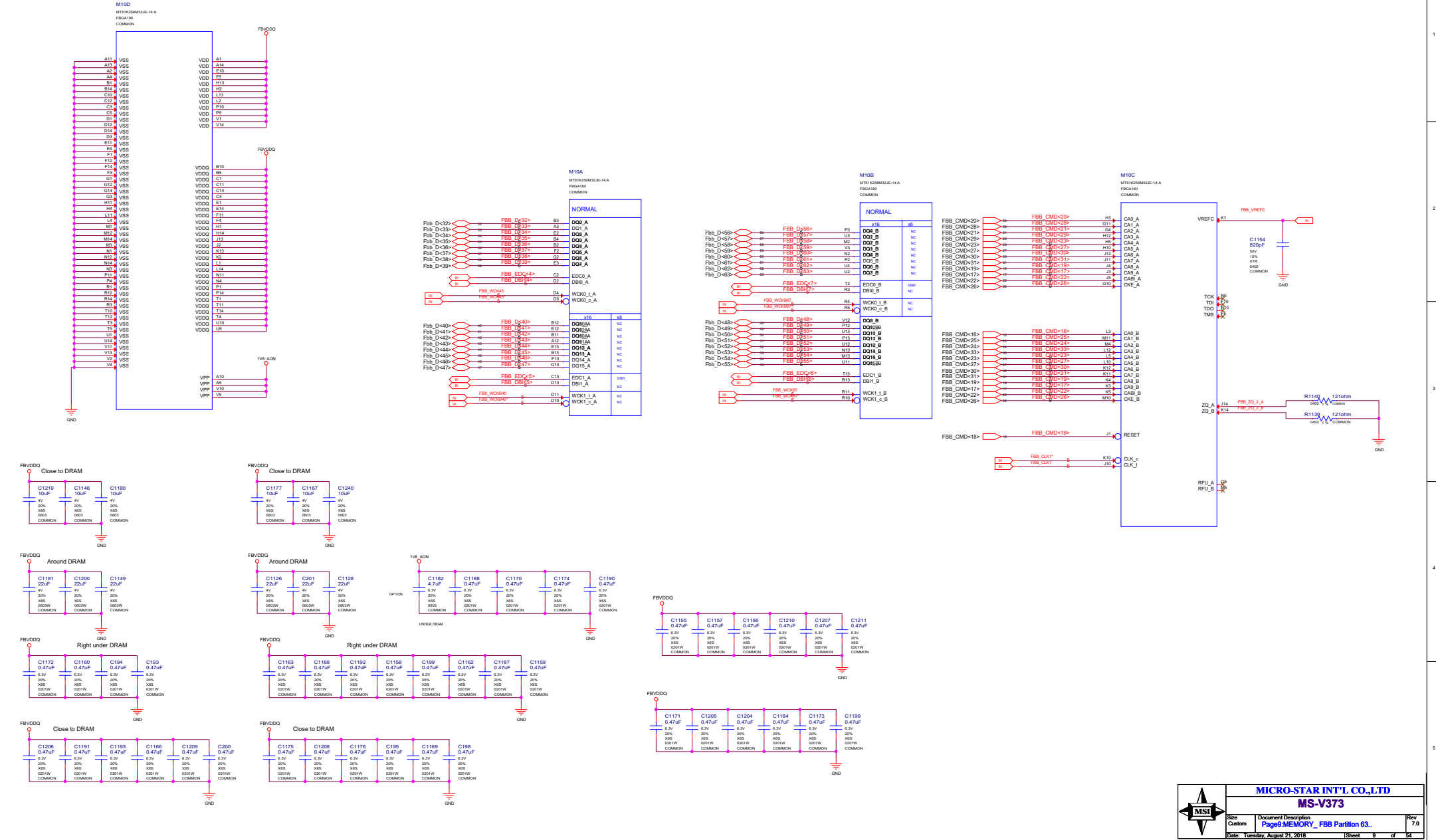
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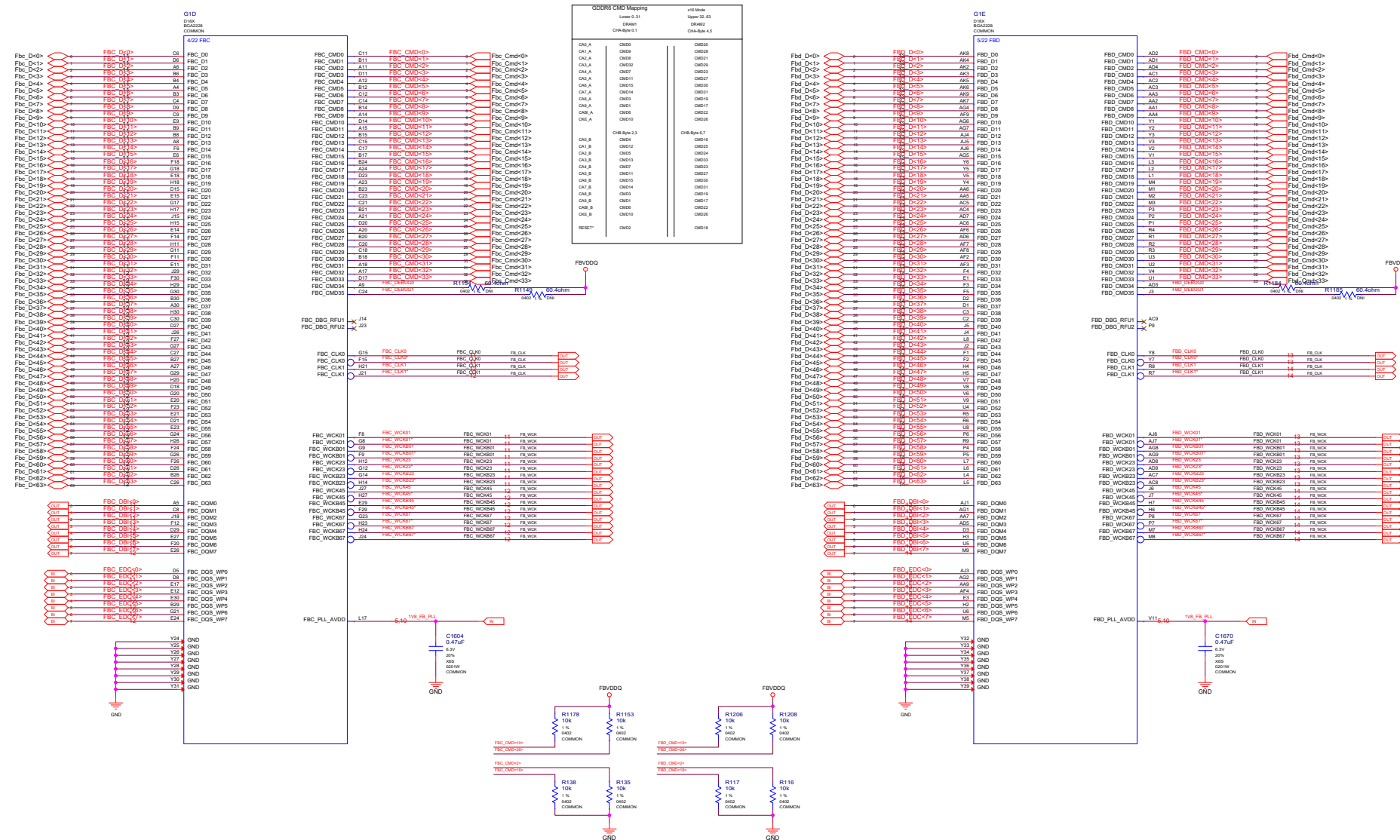


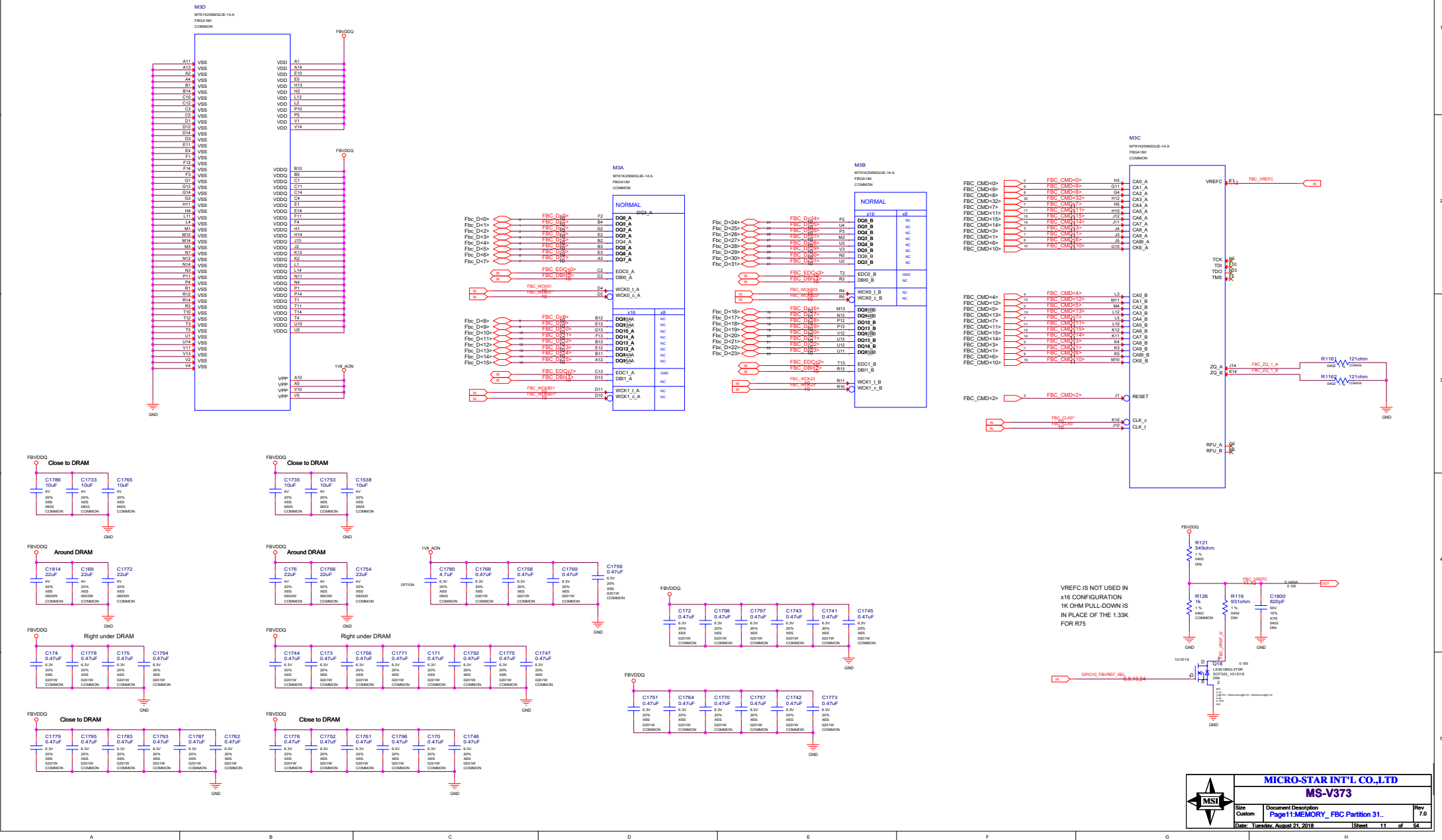


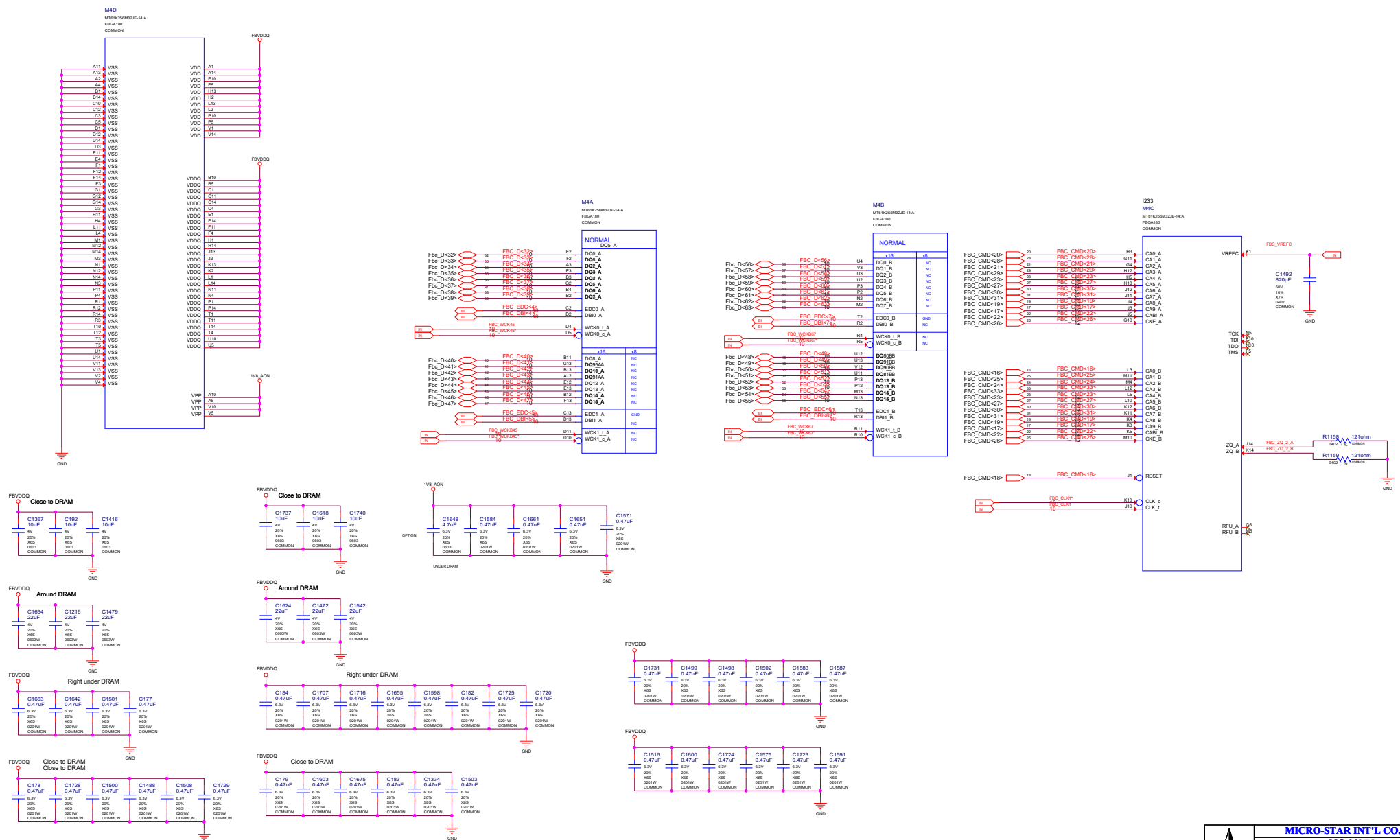


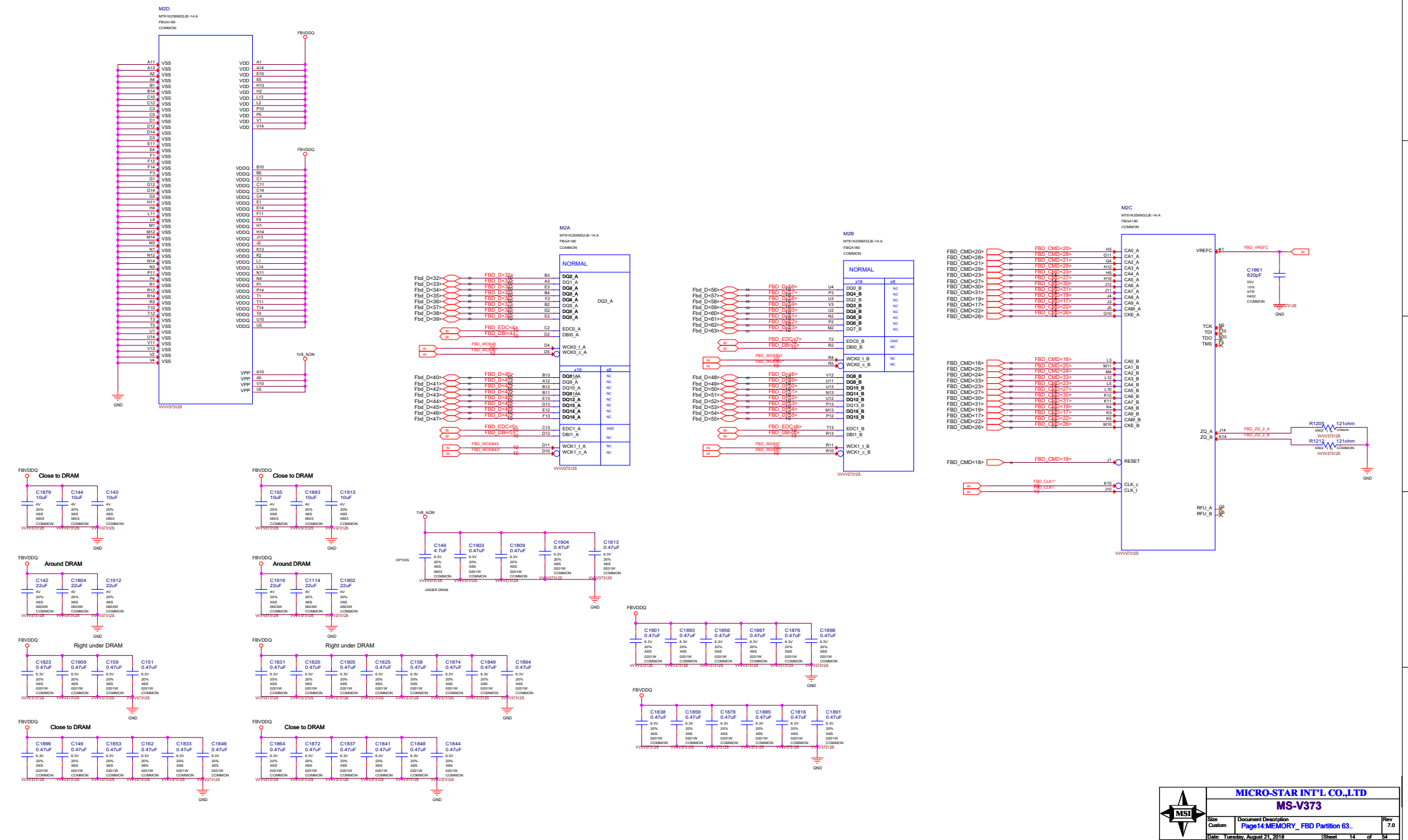


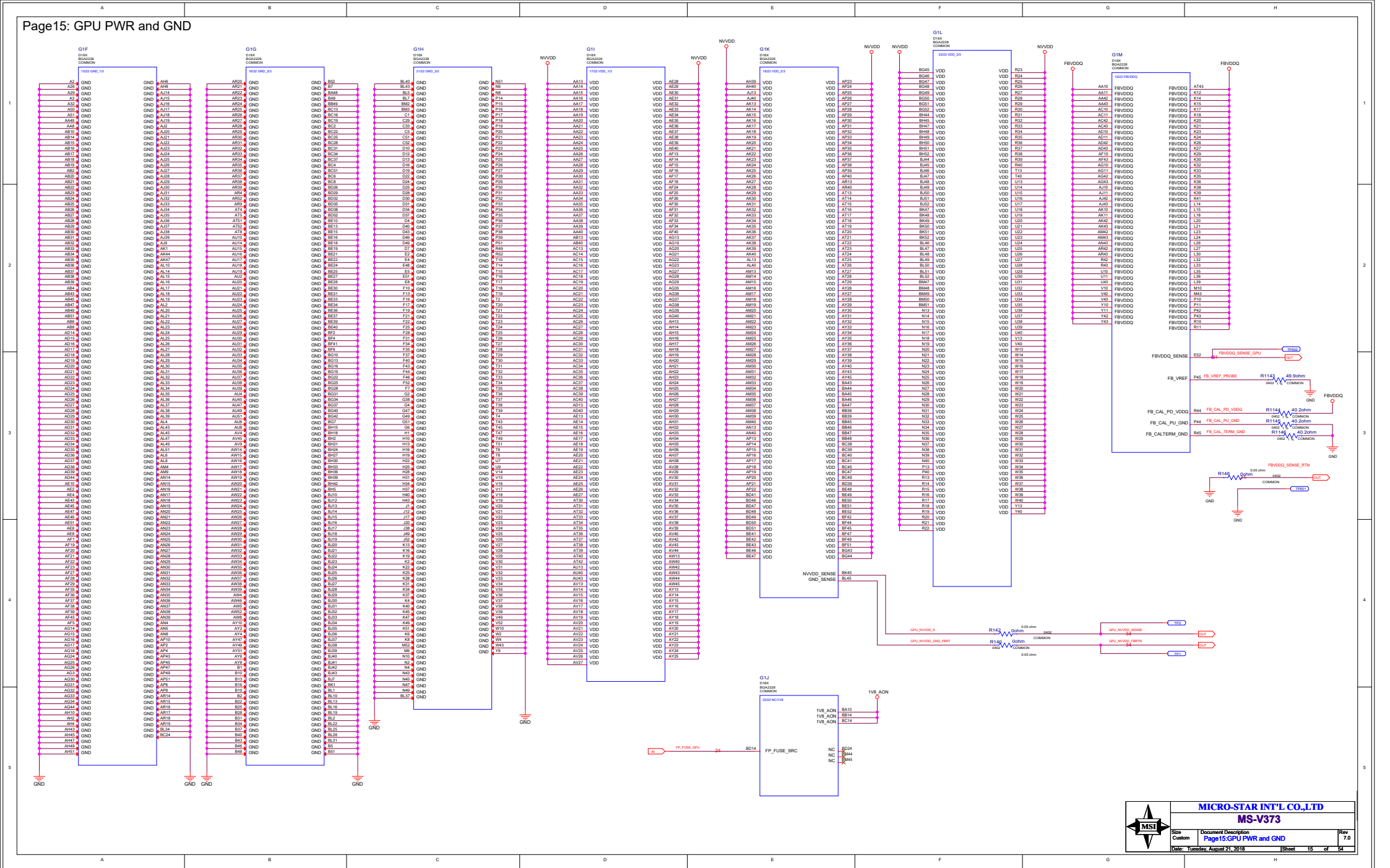












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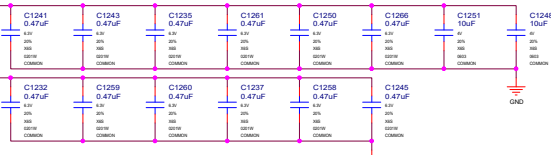
MS-V373

Size Custom	Document Description Page15:GPU PWR and GND	Rev 7.0
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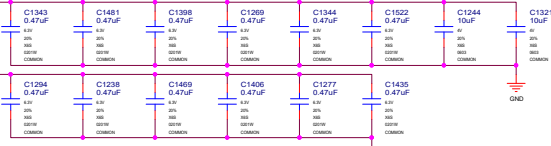
NVVDD

FBVDDQ

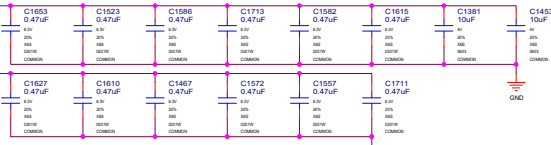
Partition A



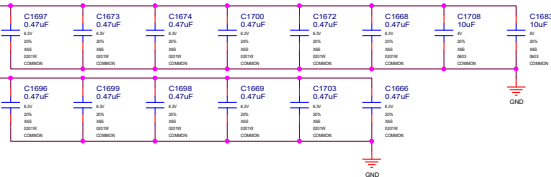
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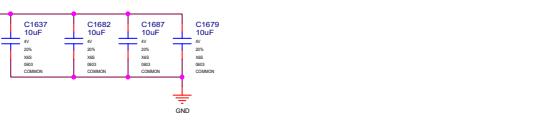
Partition C



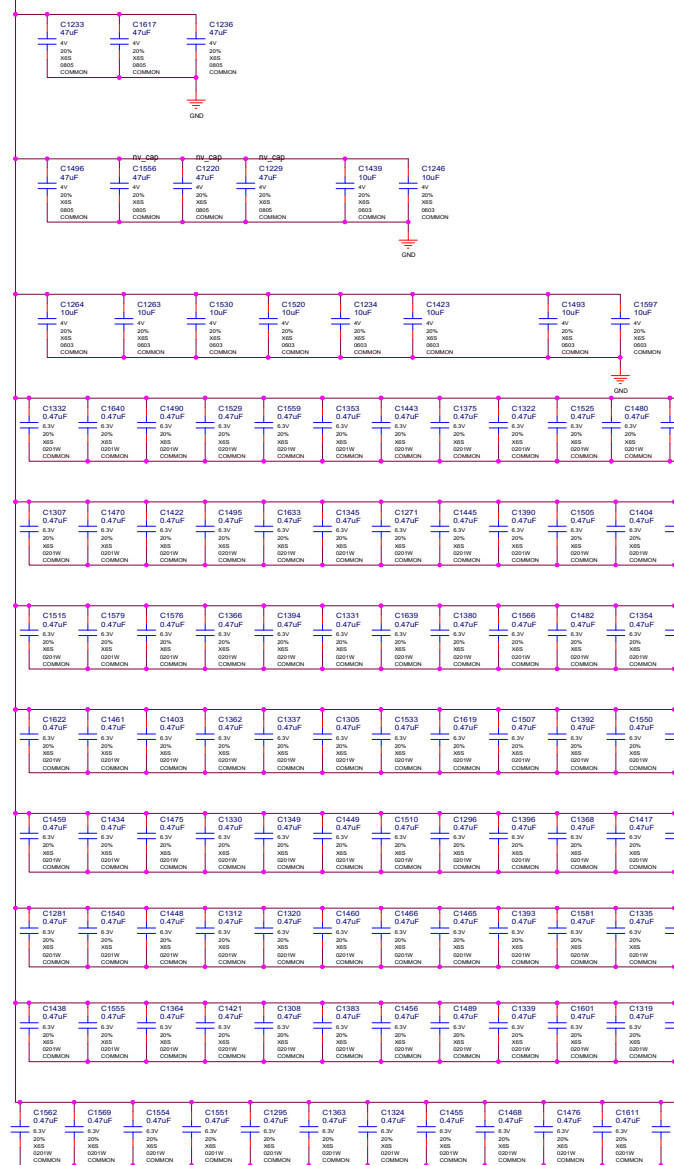
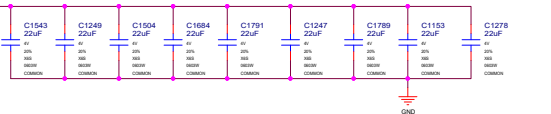
Partition D



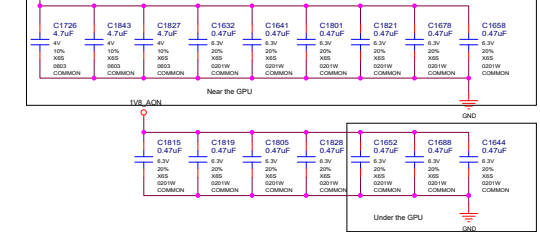
Place Close to GPU



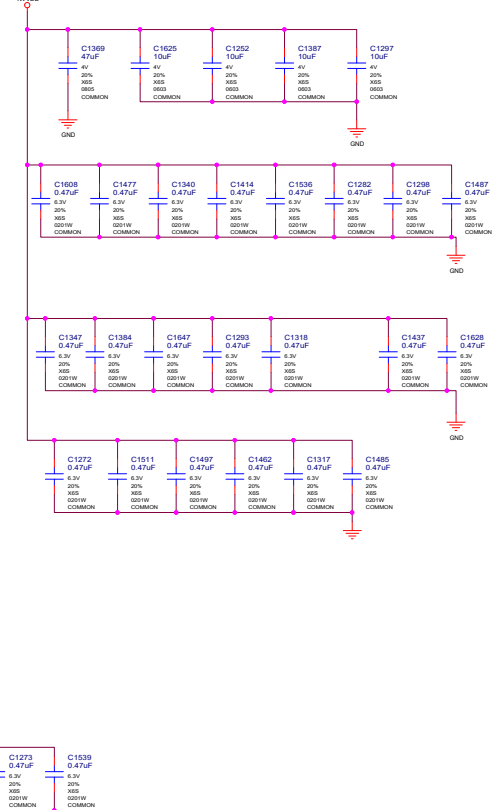
Place Close to GPU

032-0532-000
XES
0805

1V8 AON



NVVDD

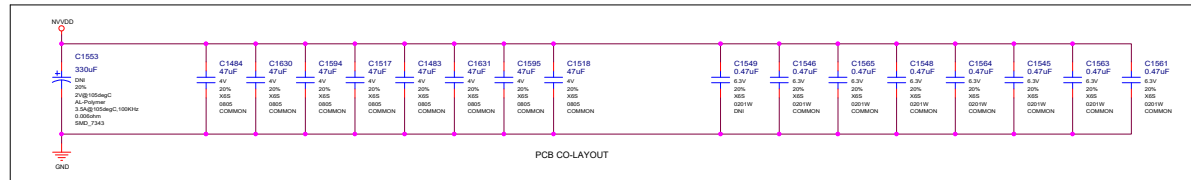
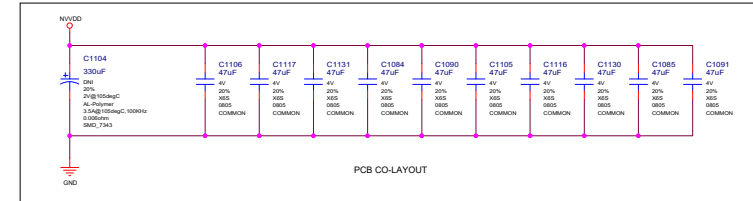
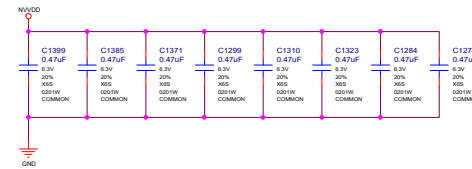
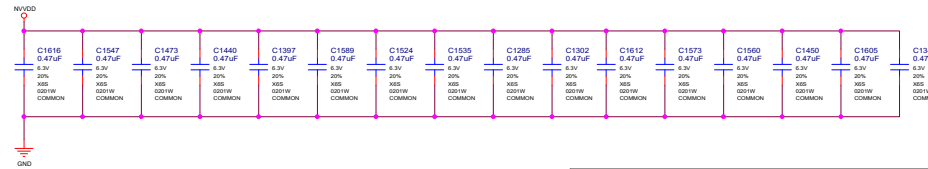
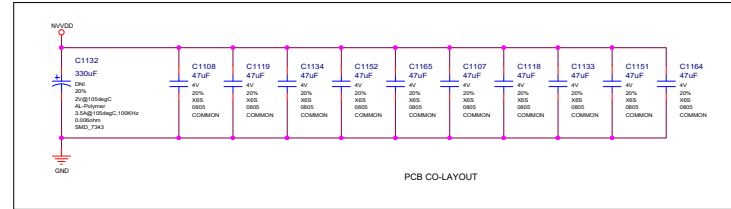
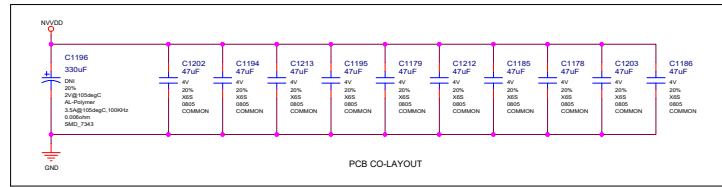
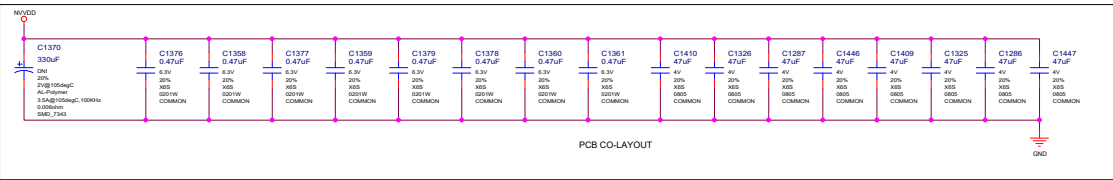


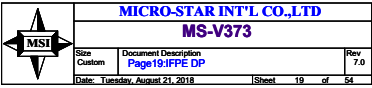
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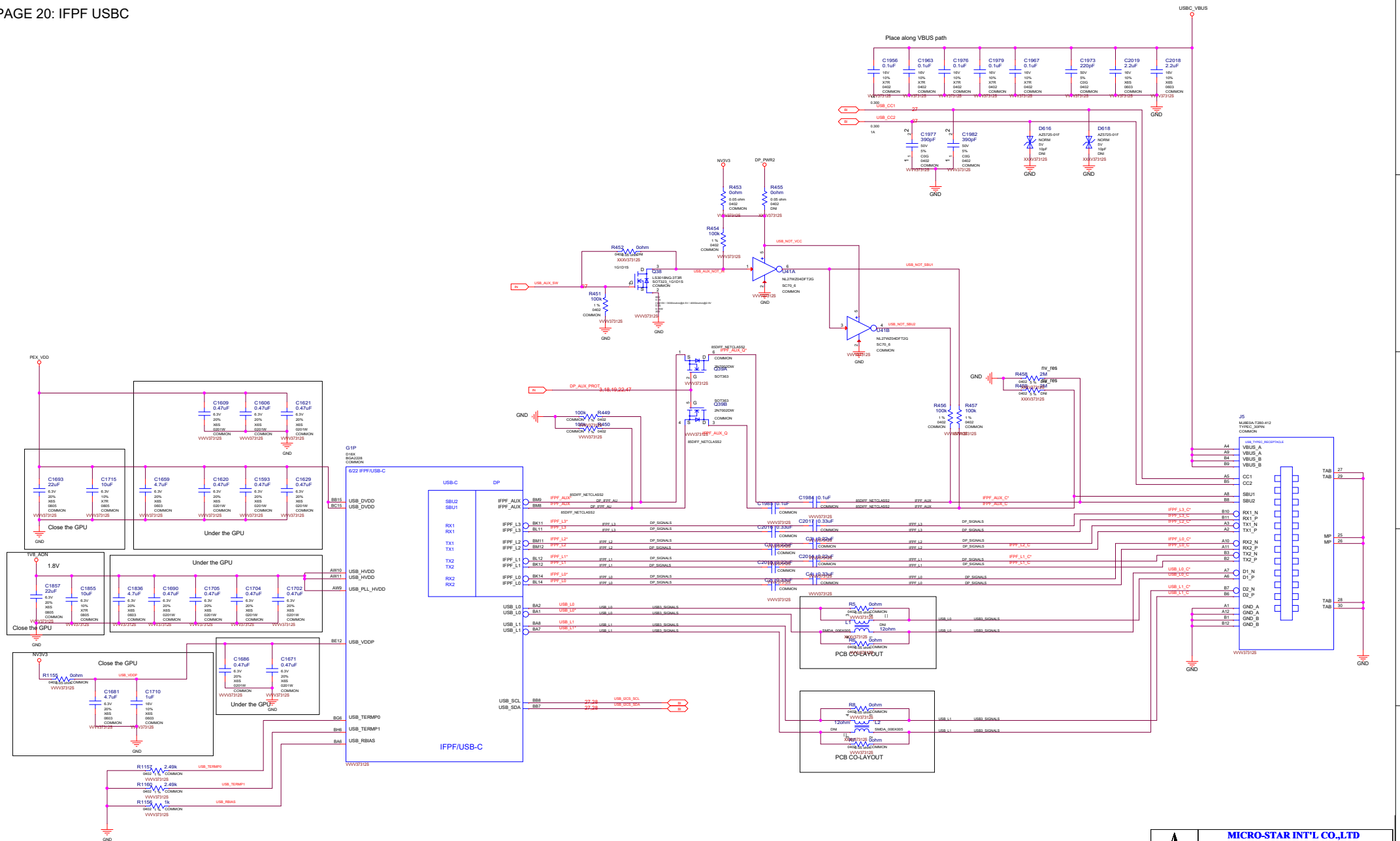
MS-V373

Date: Tuesday, August 21, 2018

Sheet 16 of 54

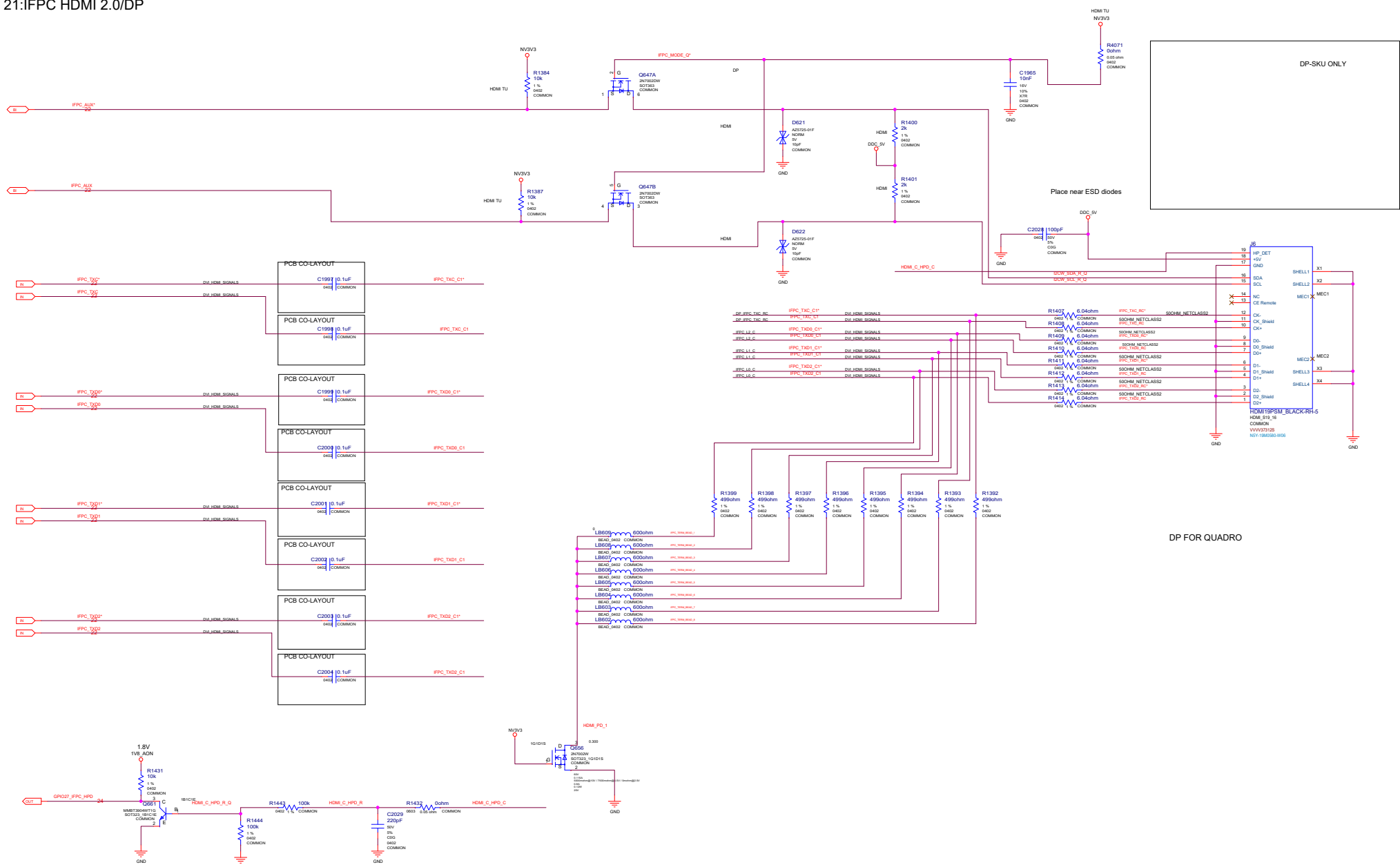




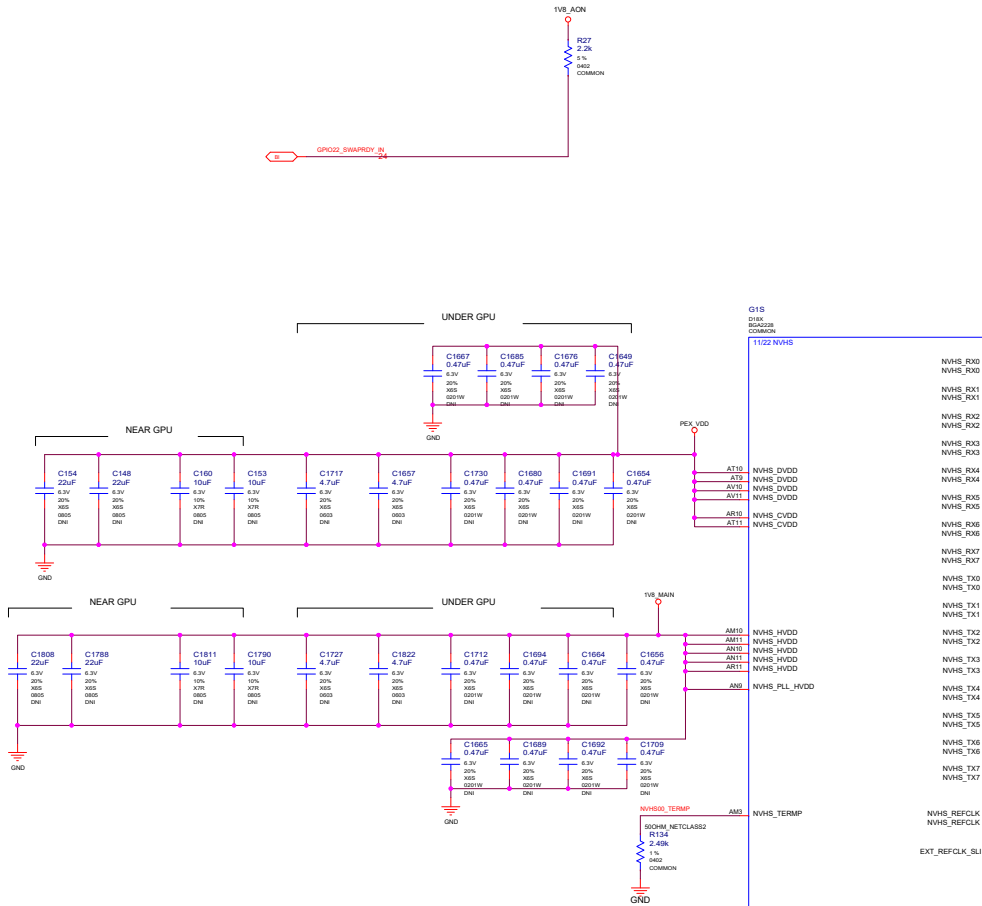


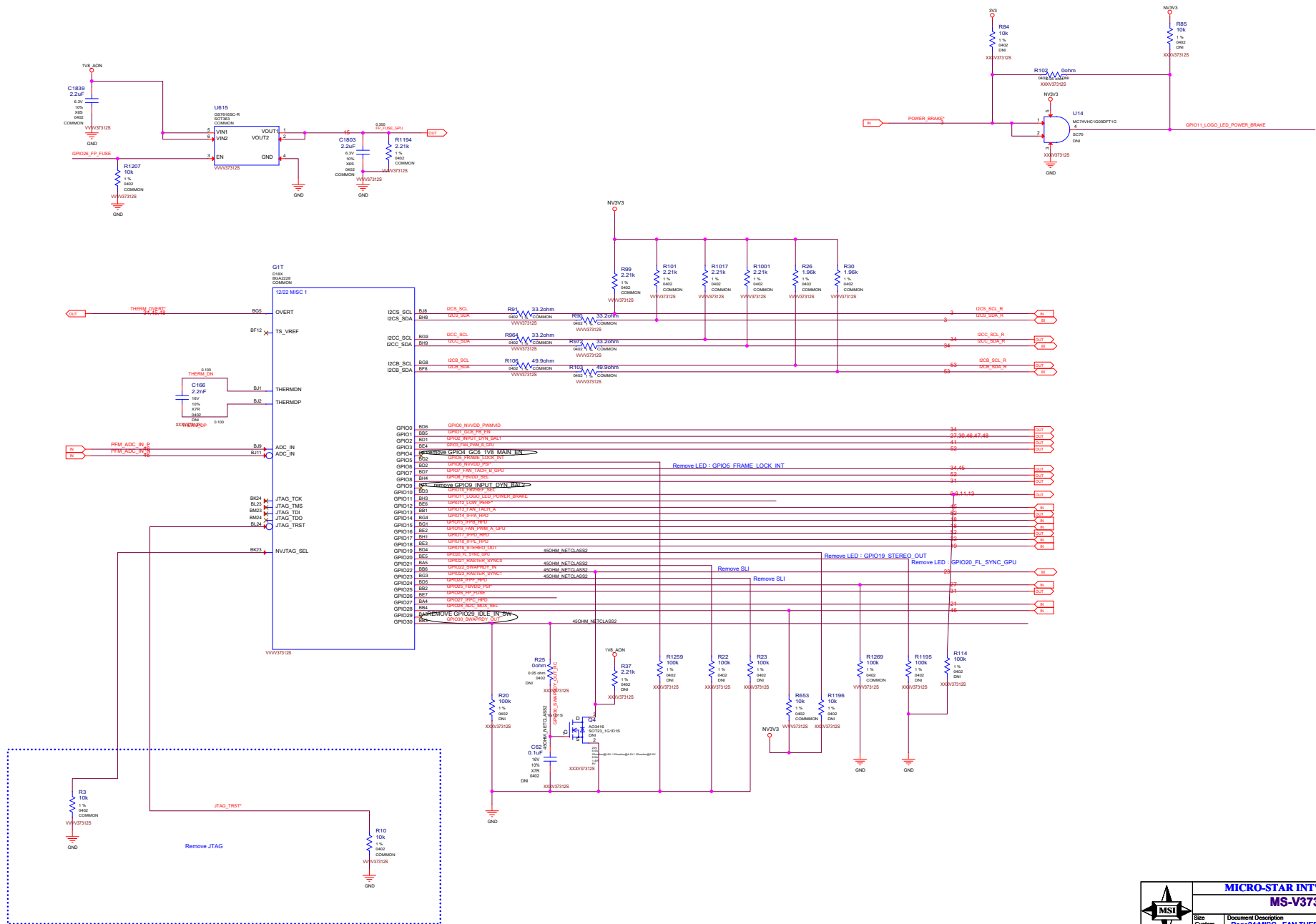
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MS-V373

Size Custom	Document Description Page20:IFPF USBC	Rev 7.0
Date: Tuesday, August 21, 2018		Sheet 20 of 54









H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]_FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

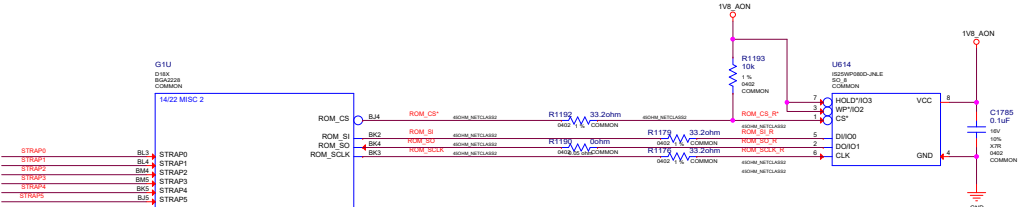
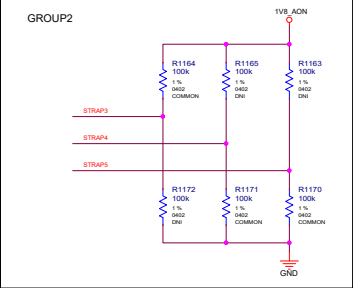
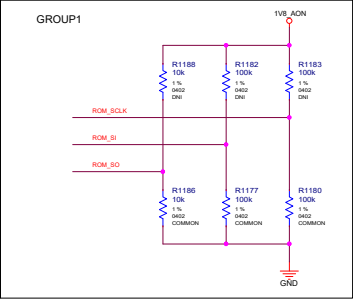
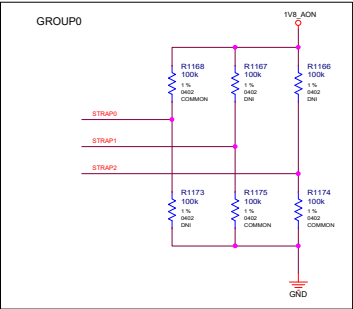
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

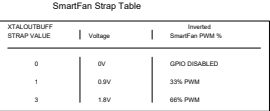
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

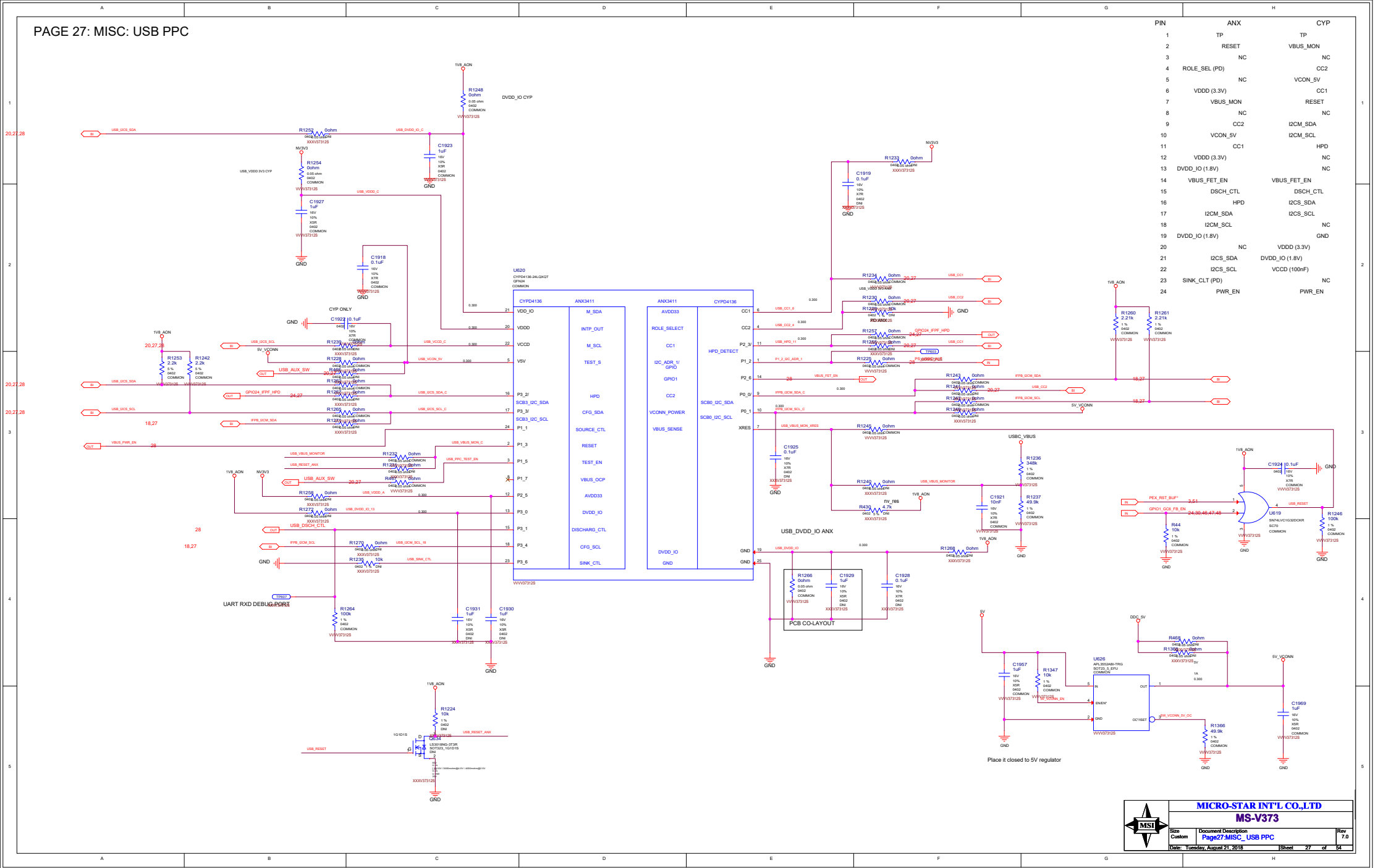
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

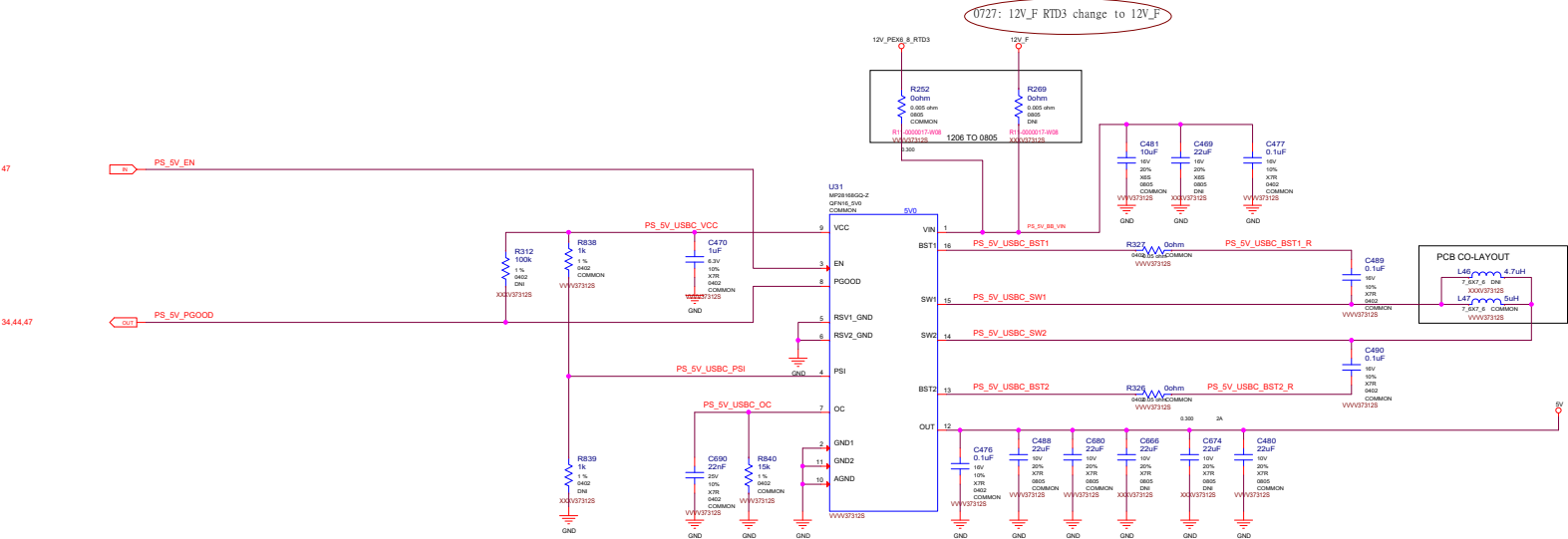
Default

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung

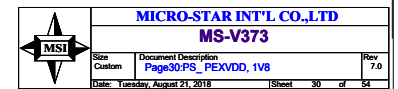
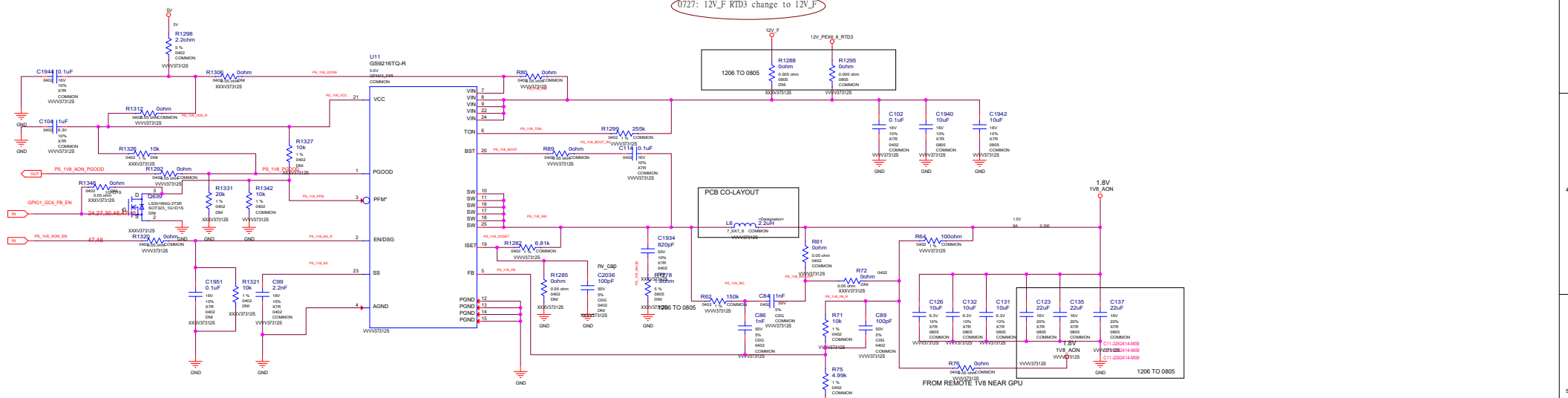
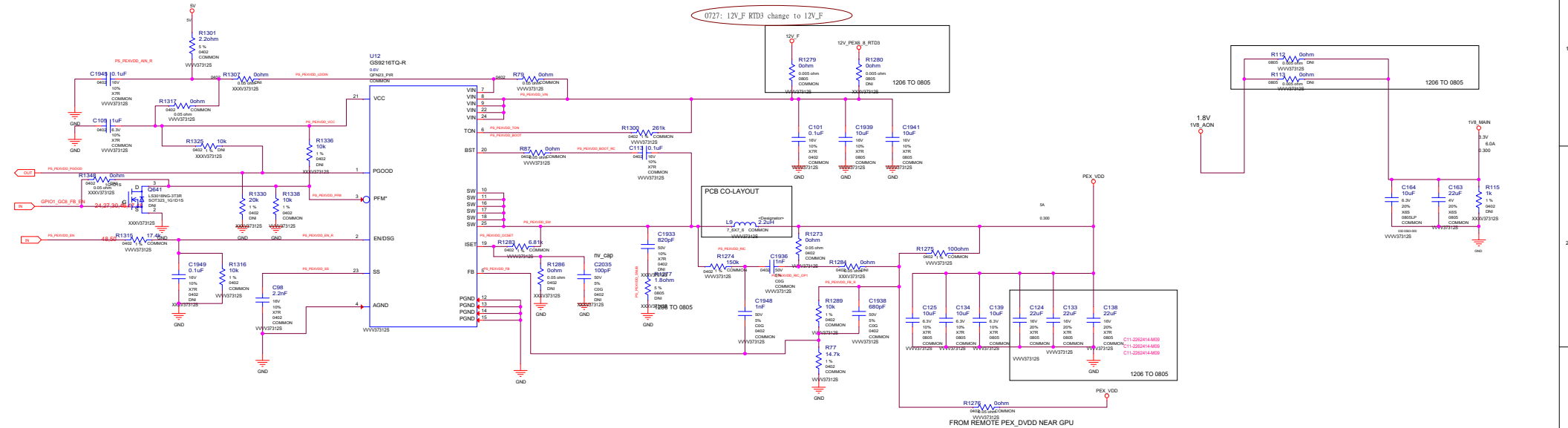






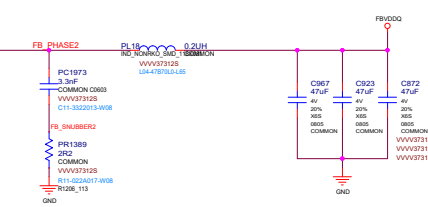
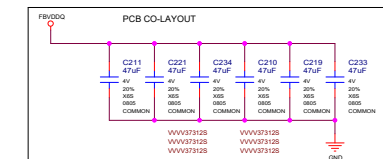
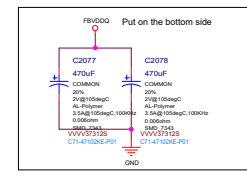
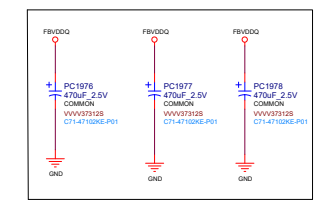
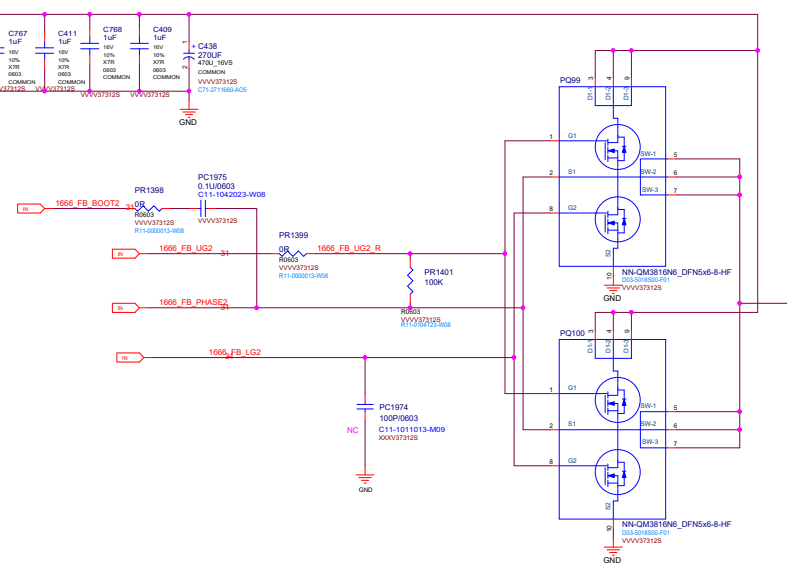
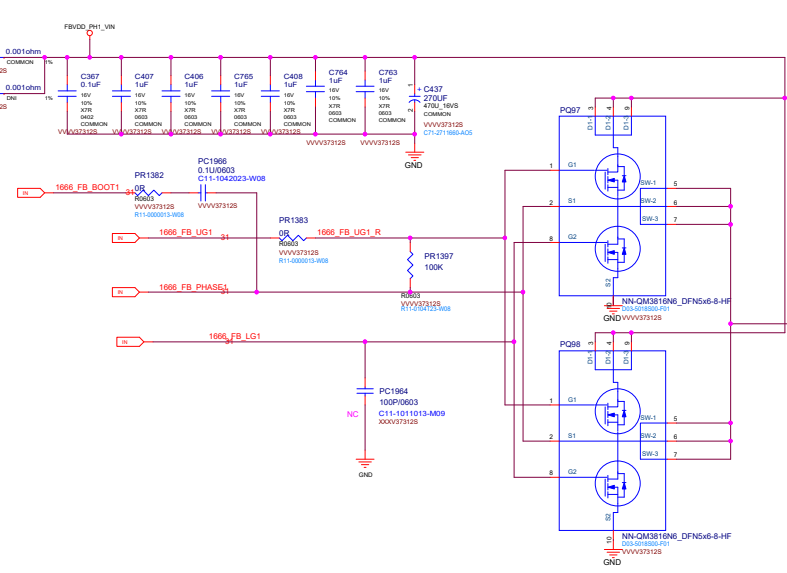
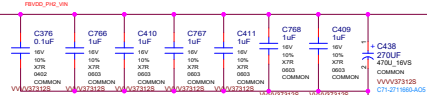


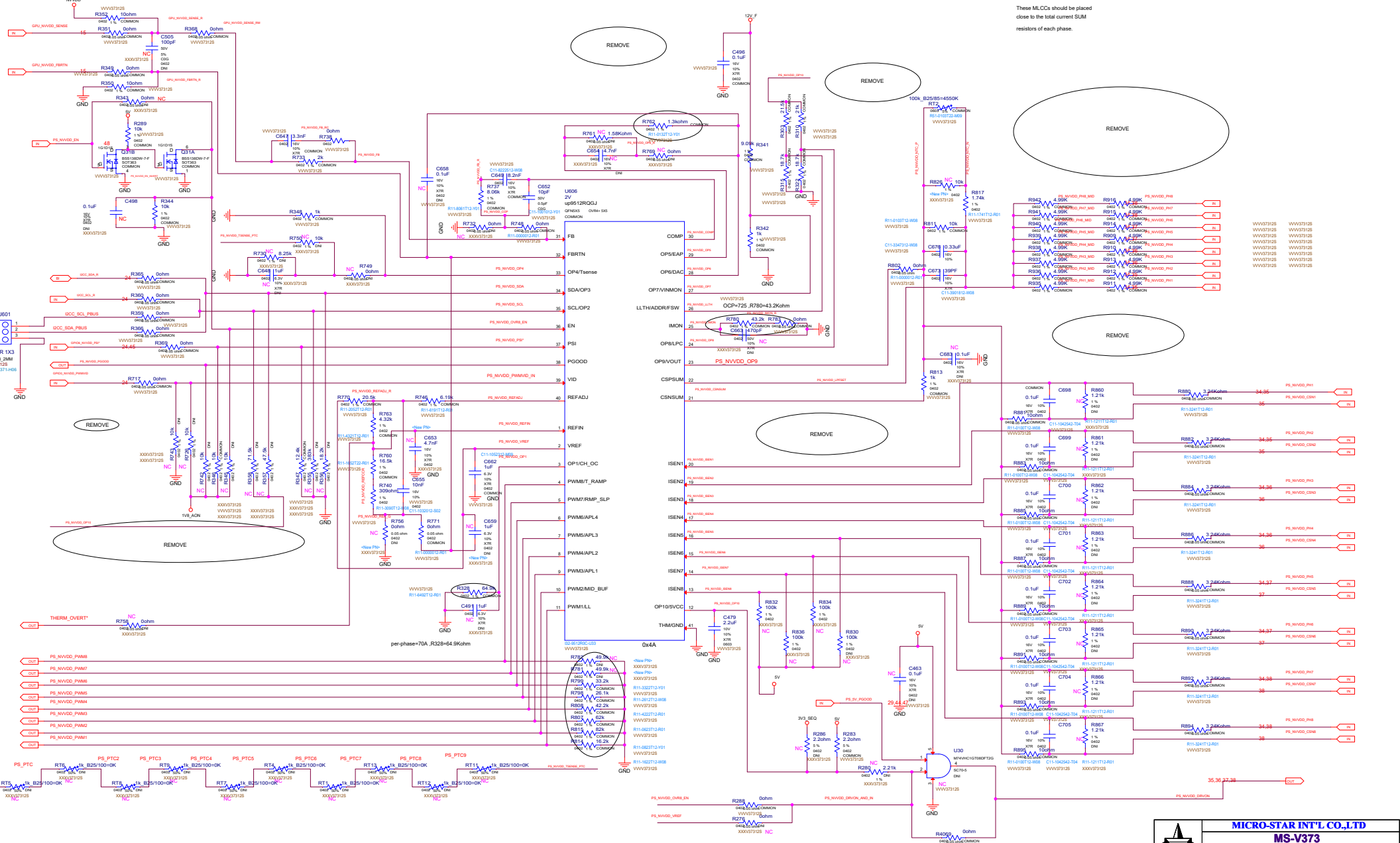
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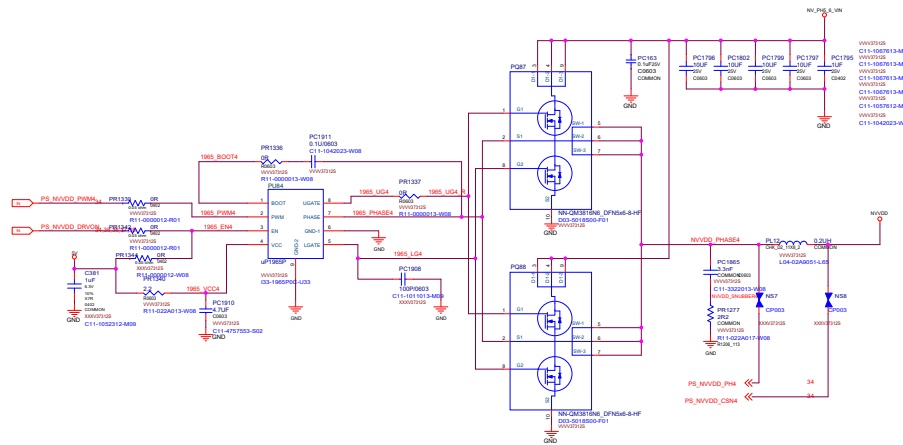
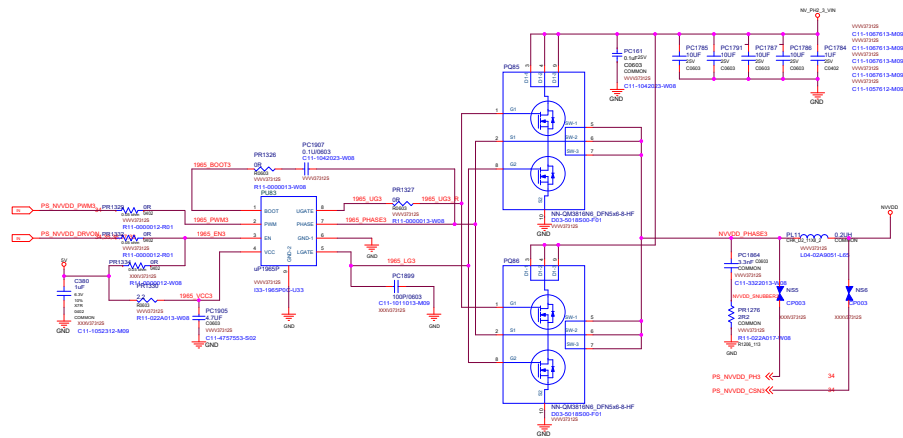
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MS-V373		
Size	Document Description	Rev
Custom	Page32:PS_FBVDD CONTROLLER OVR3	7.0
Date:	Tuesday, August 21, 2018	Sheet 32 of 54

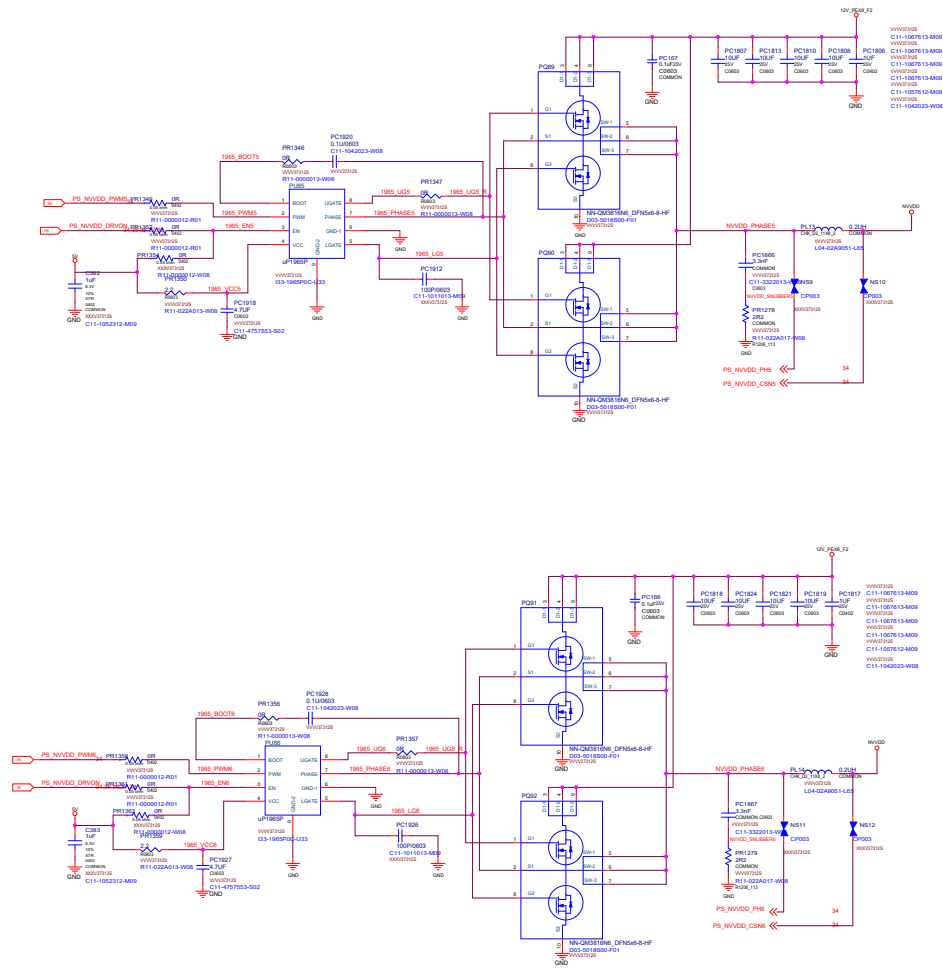


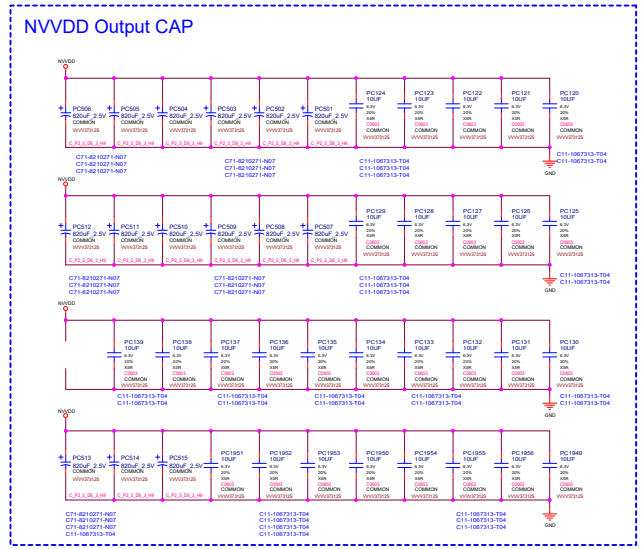
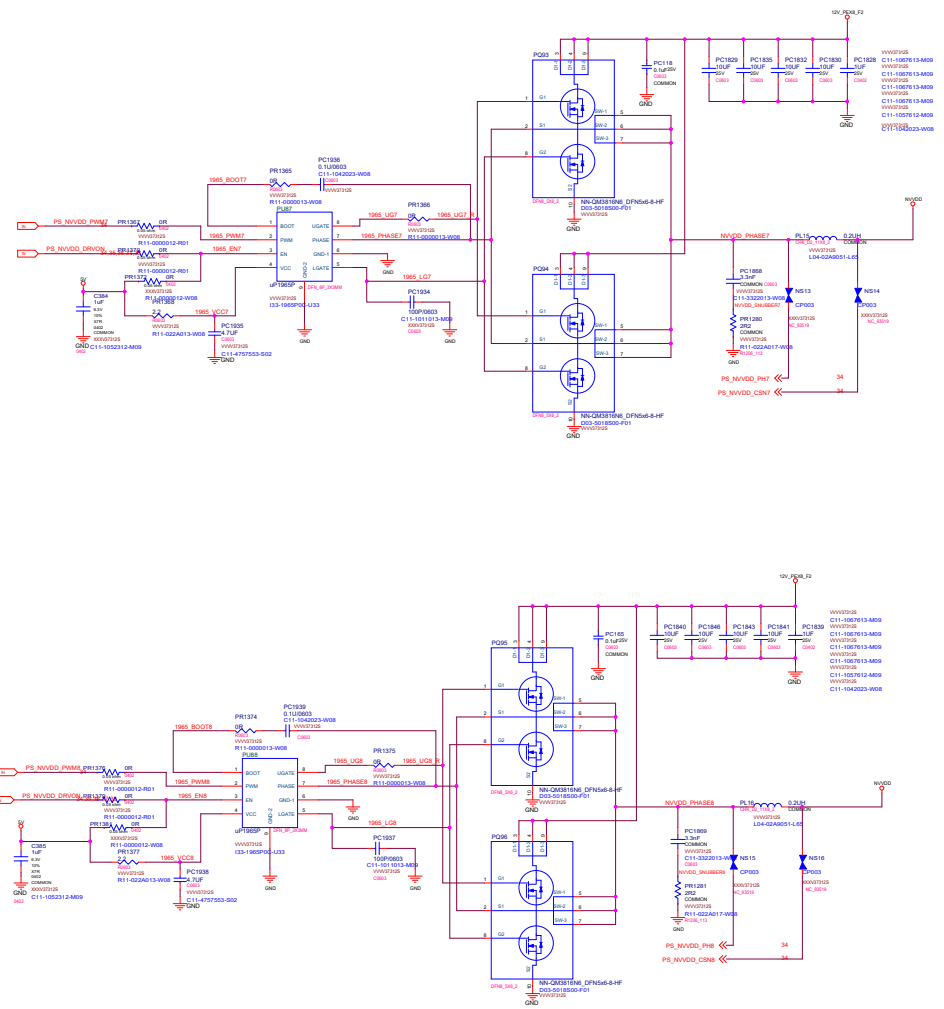


These MLCCs should be placed close to the total current SUM resistors of each phase.





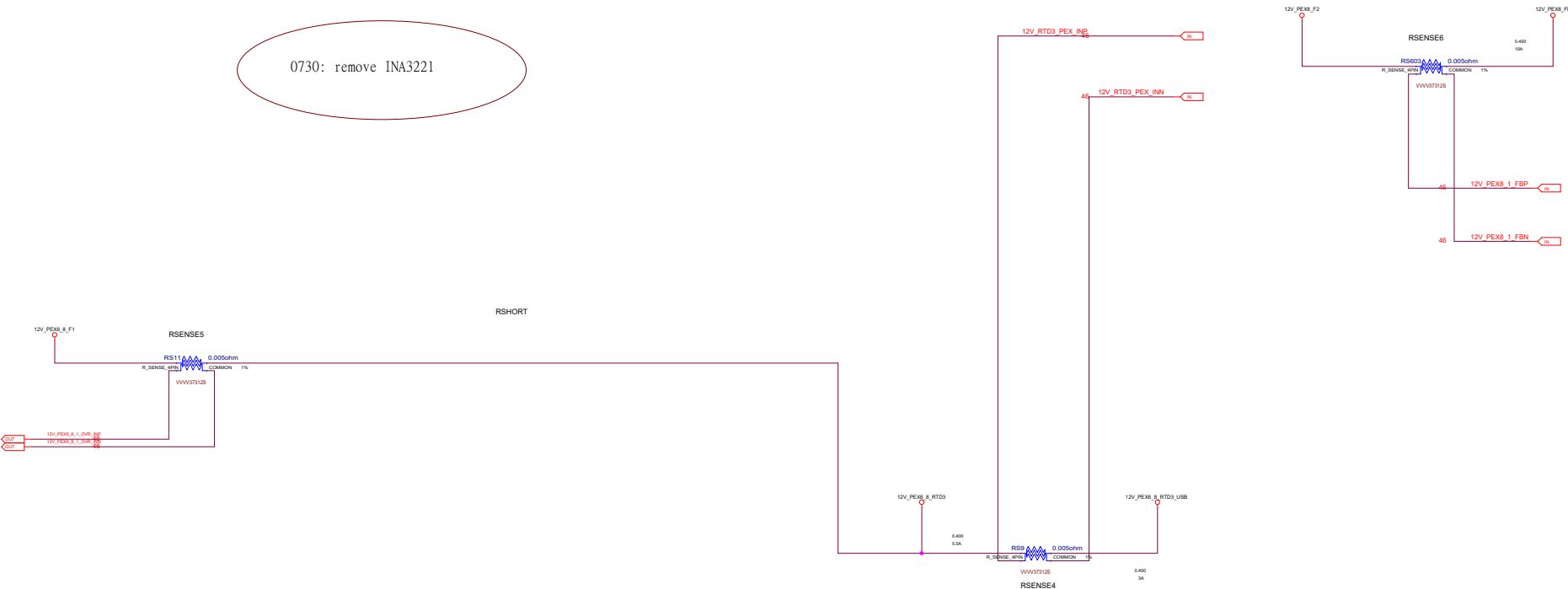


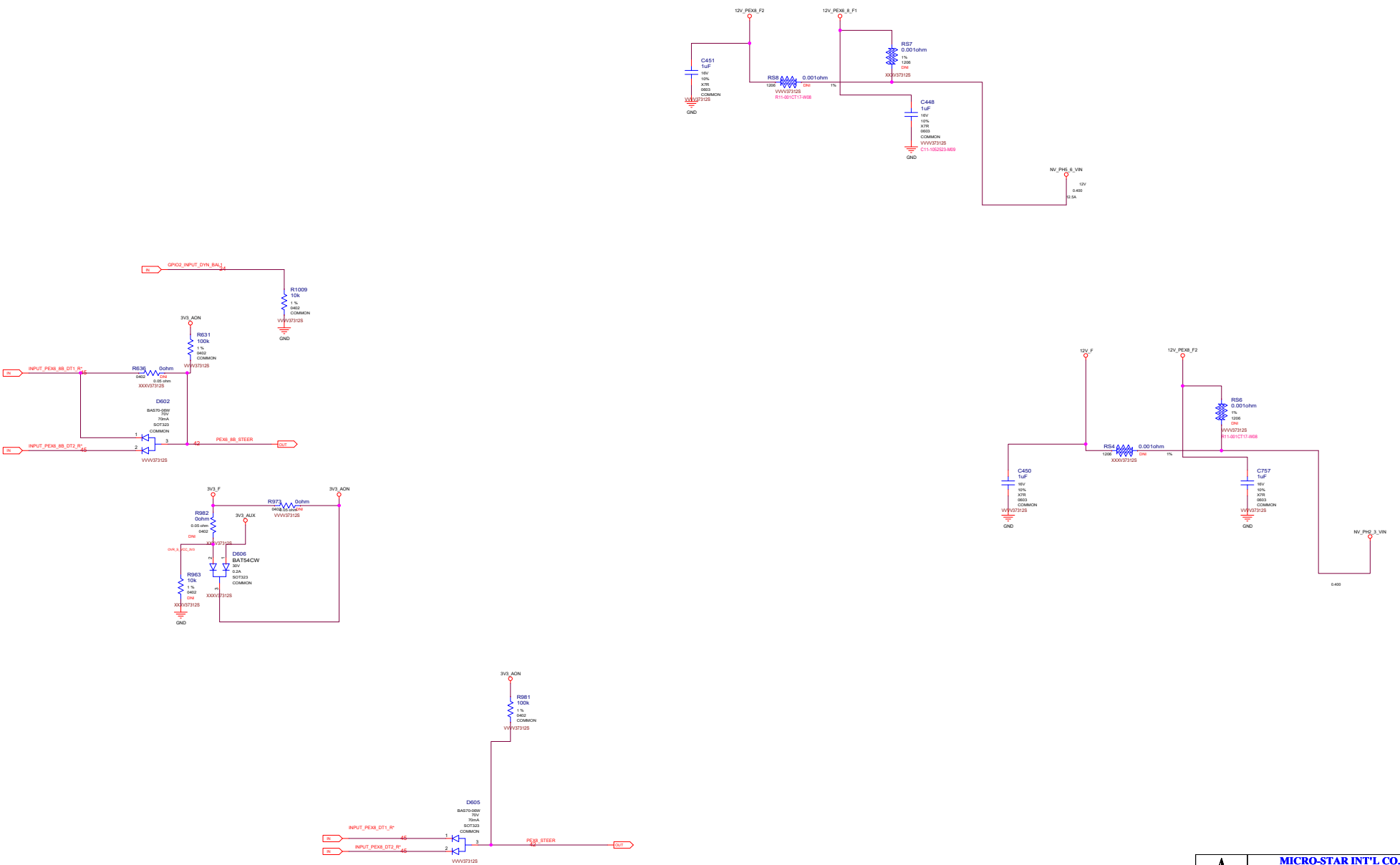


AND GATE LOGIC FOR P-BOARD			
GPI01	GPI029	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

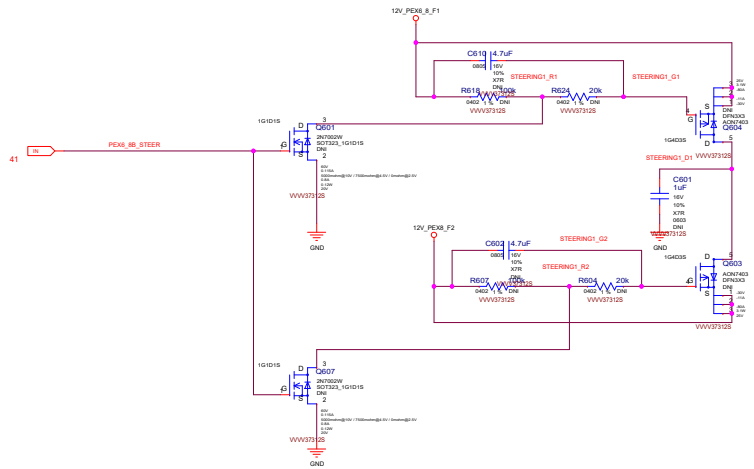
AND GATE LOGIC FOR P-BOARD			
GPI01	GPI029	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

0727: remove

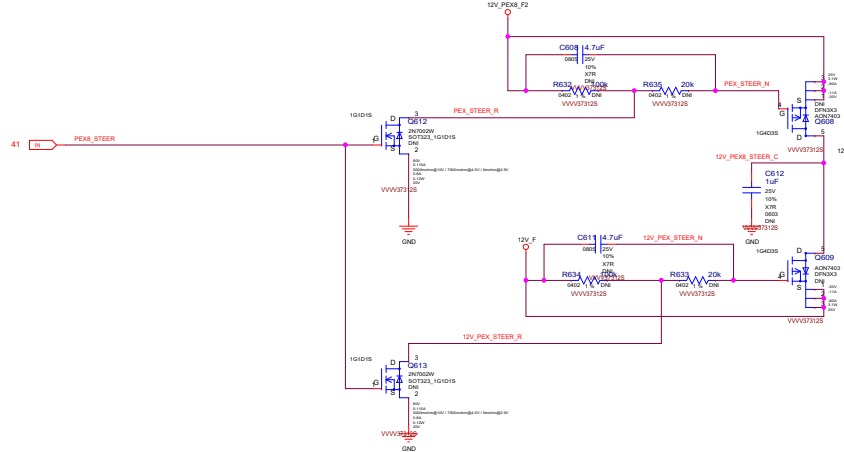




12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



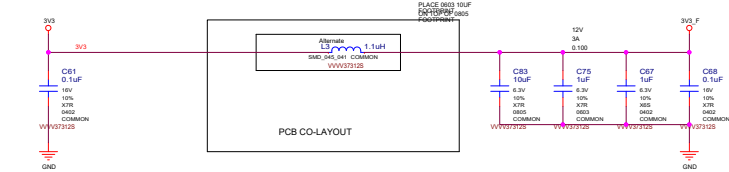


MICRO-STAR INT'L CO.,LTD		
MS-V373		
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Date: Tuesday, August 21, 2018		Sheet 43 of 54

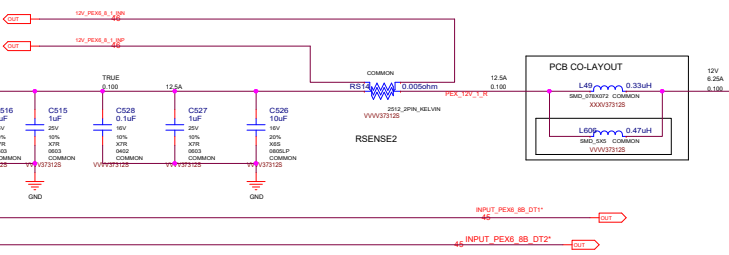
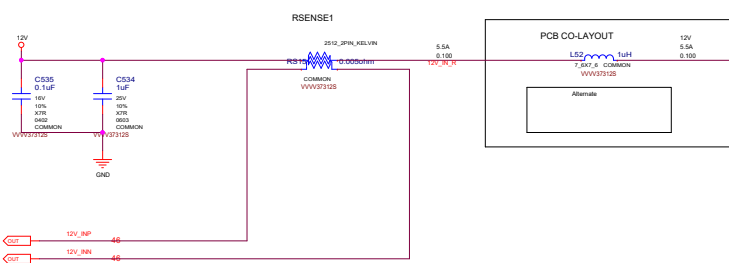
0727: remove U37

PEX6 INPUT 1 - 2x3 PCIE CON 75W

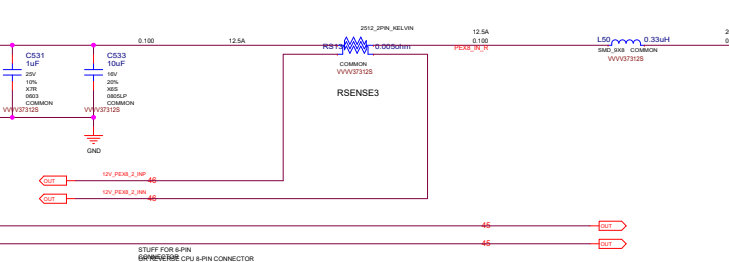
PEX 3V3 INPUT - 10W



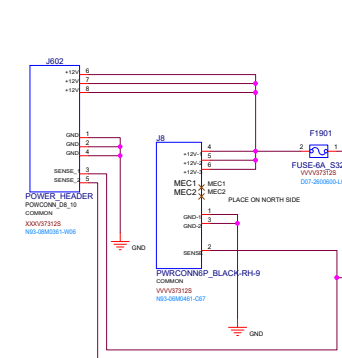
PEX_12V INPUT - 66W



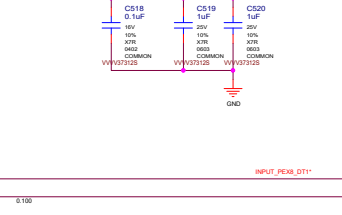
PEX8 INPUT 2 - 2x4 PCIE CON 150W

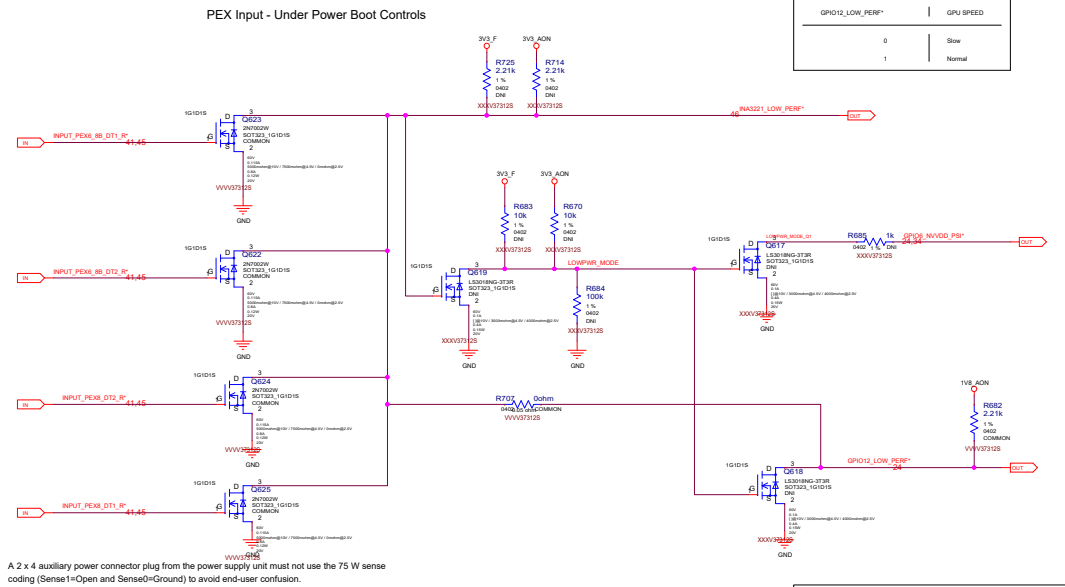
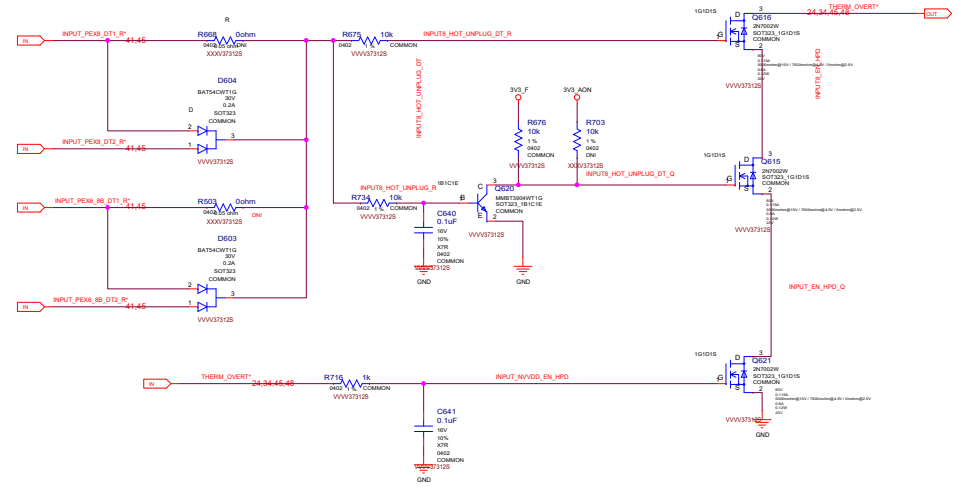
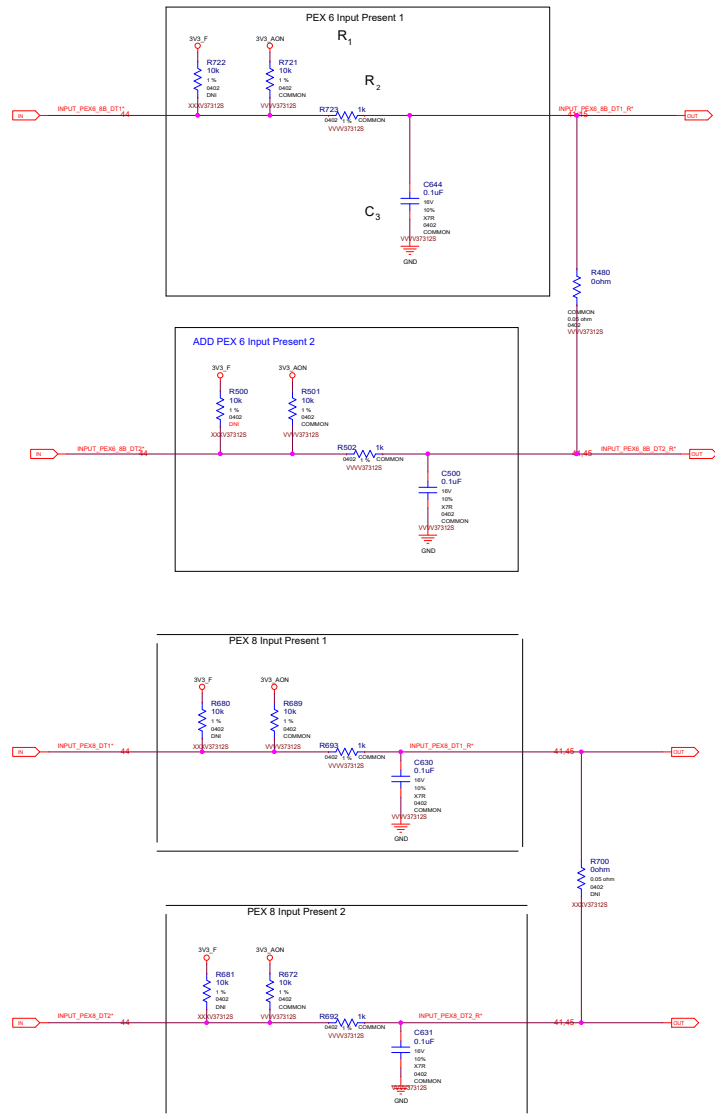


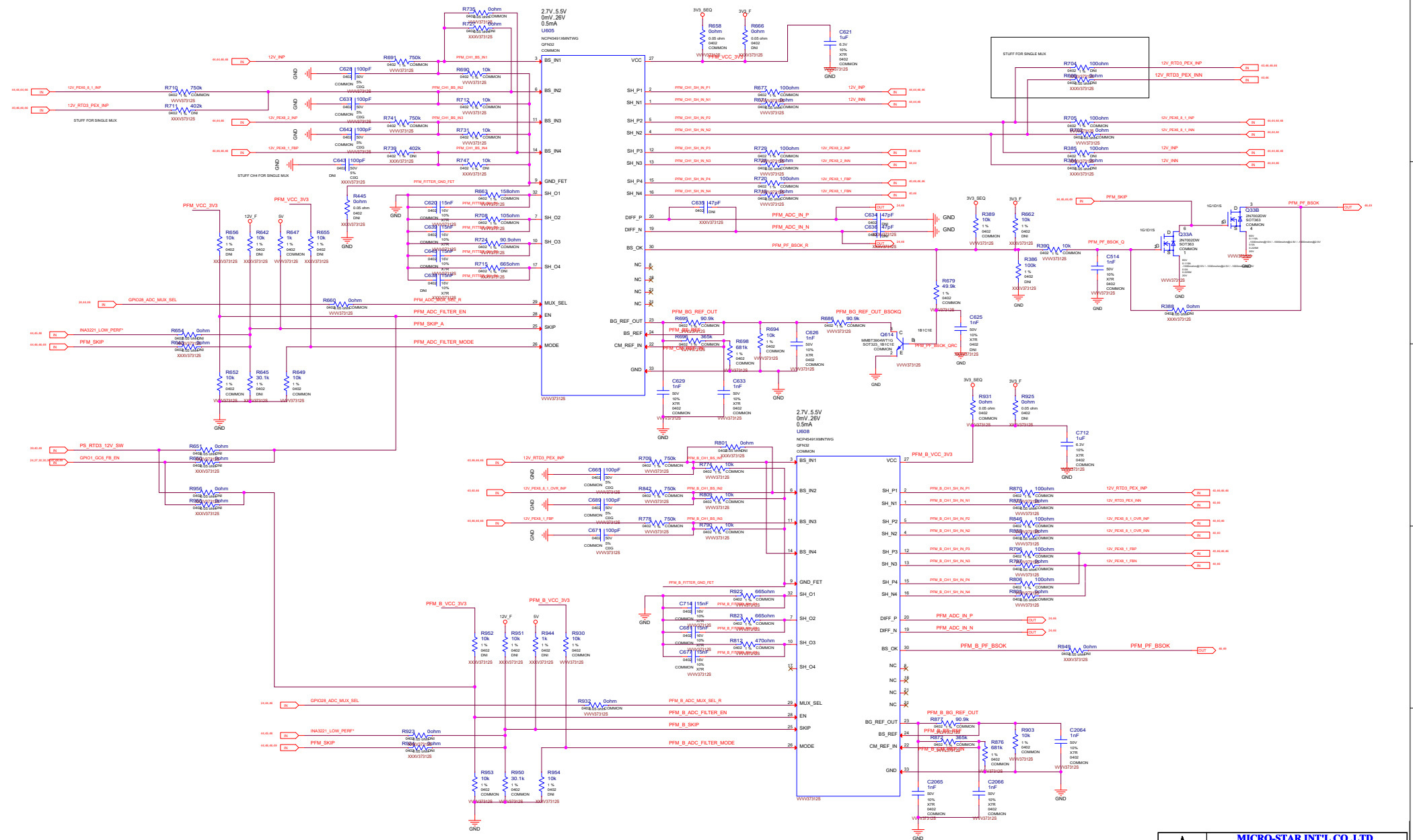
PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



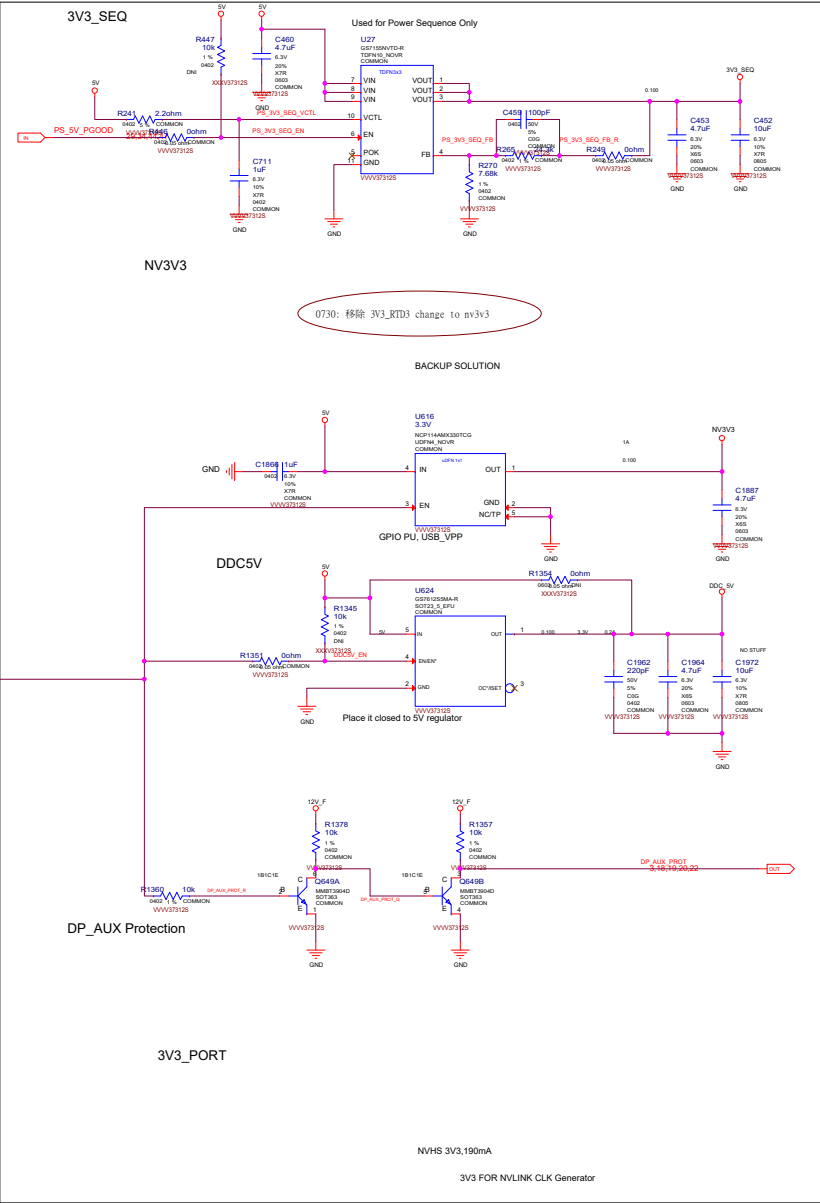
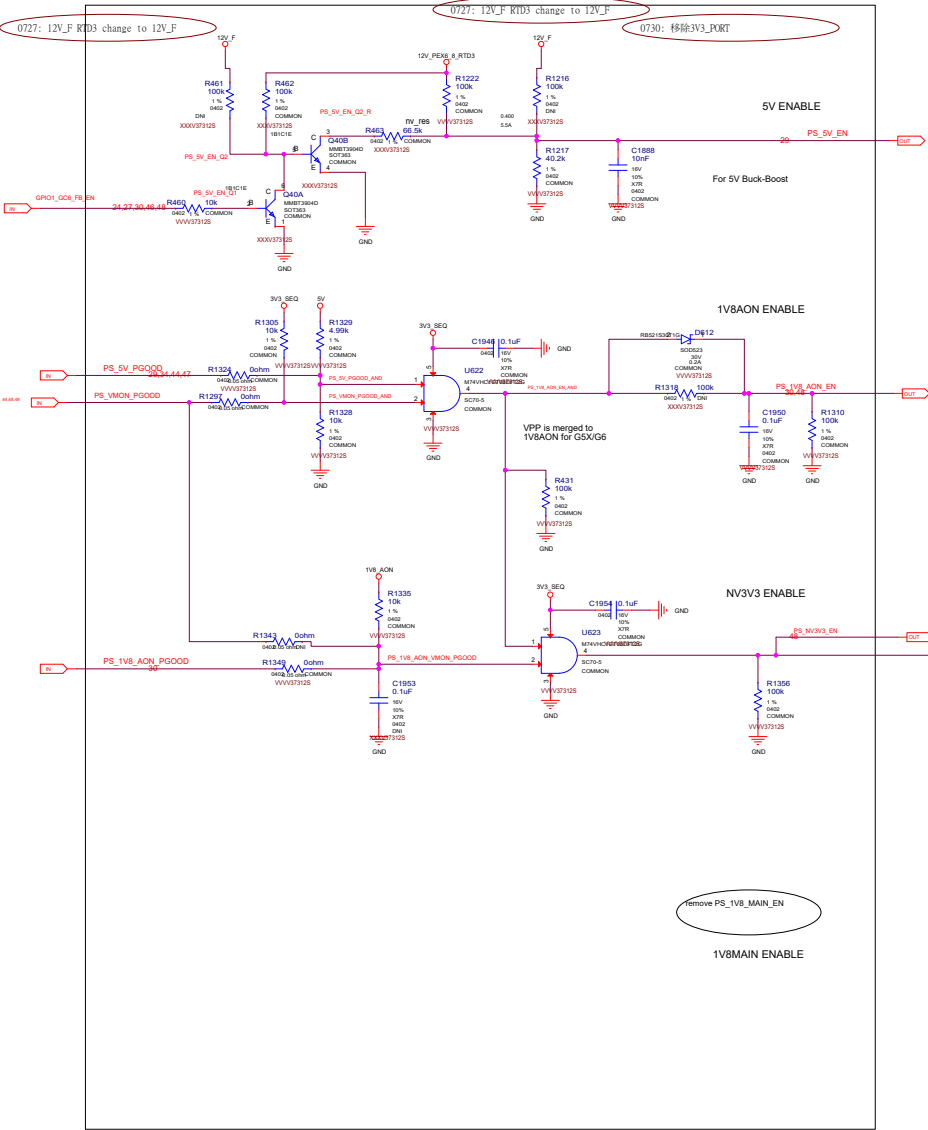


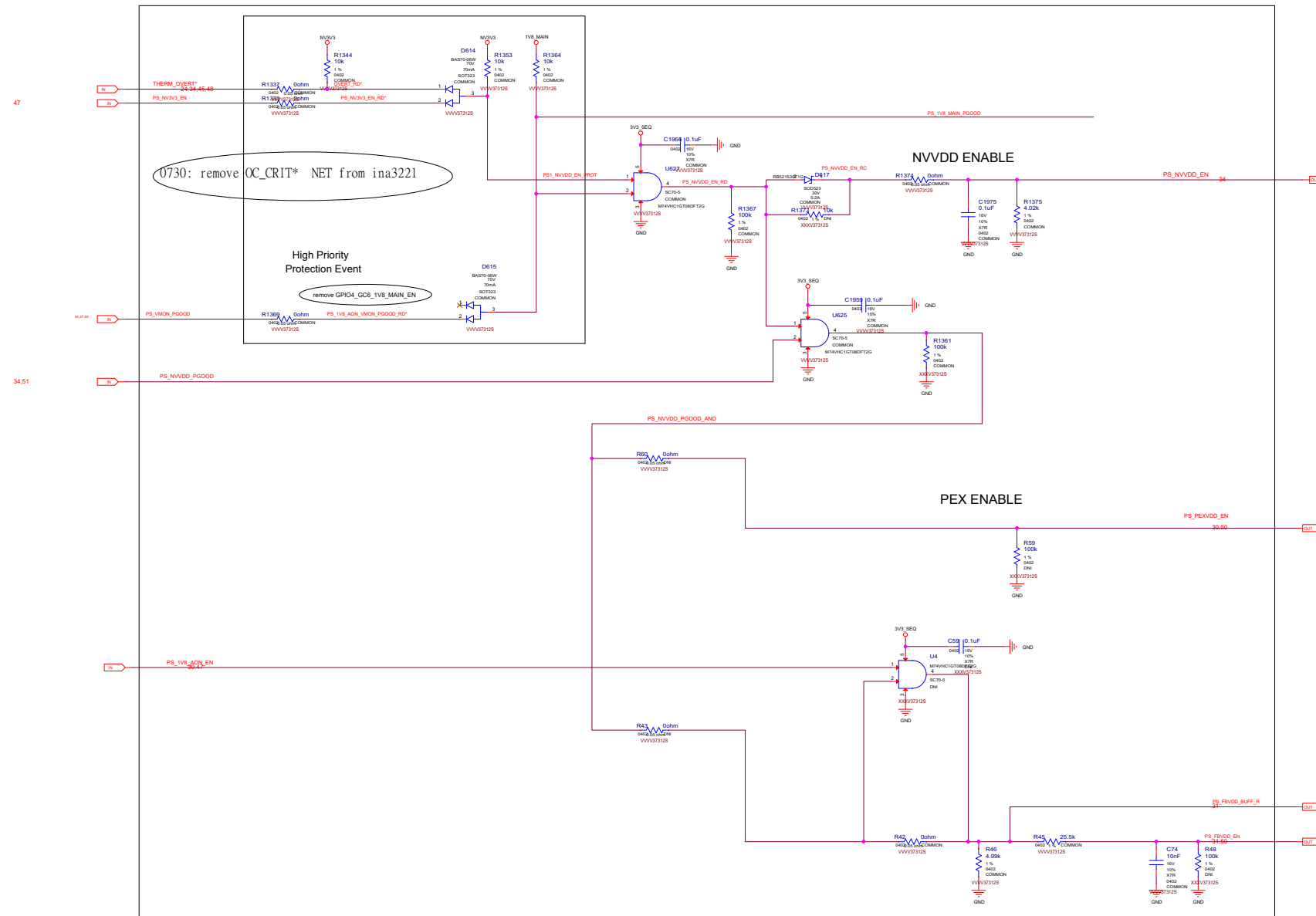


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MS-V373

Size Custom	Document Description Page46:PS_PRE-FILTER	Rev 7.0
Date: Tuesday, August 21, 2018		Sheet 46 of 54

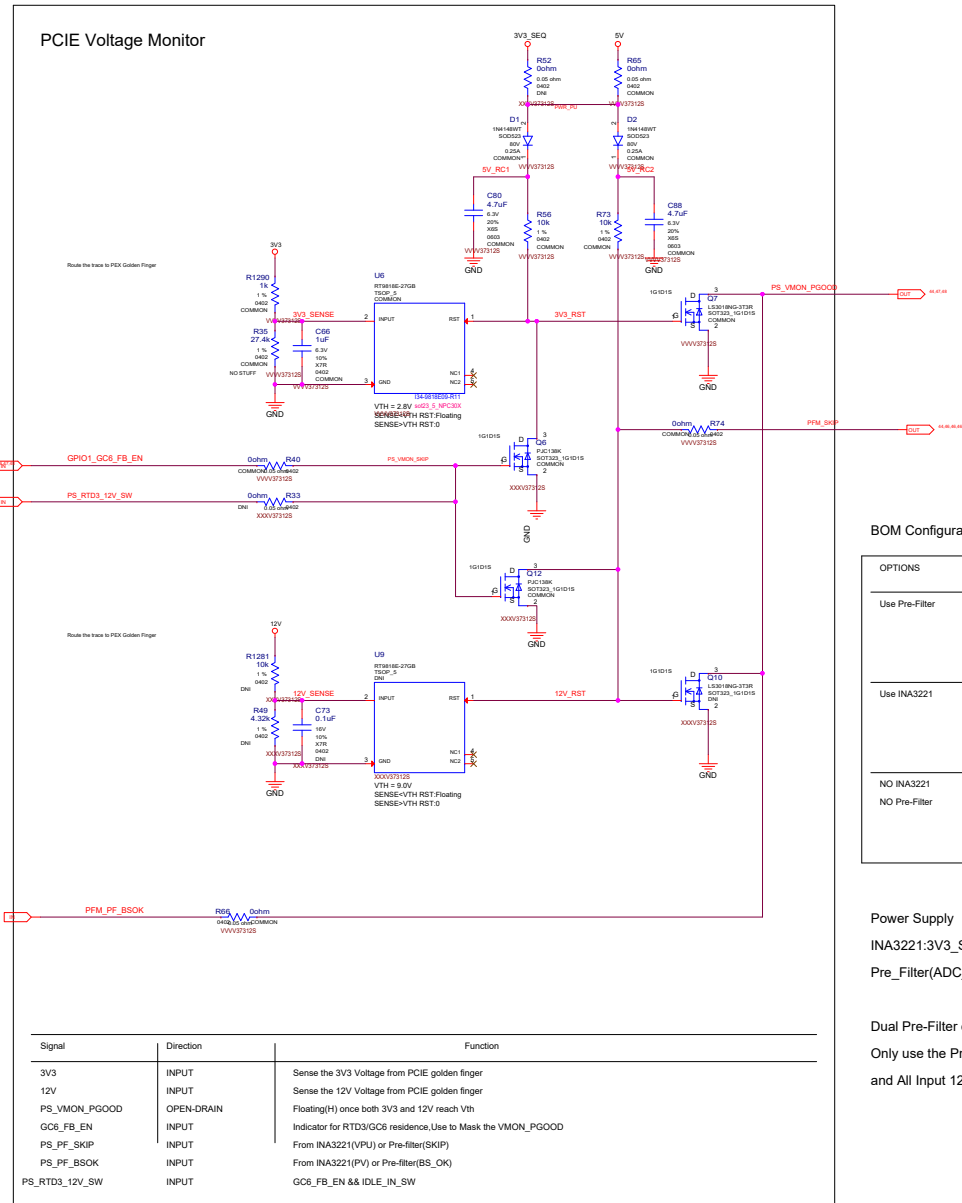




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MS-V373

Size Custom	Document Description Page48:SEQUENCE_ NV, PEX, FB ENAB
Date: Tuesday, August 21, 2018	Sheet 48



BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

Pre_Filter(ADC_MUX):3V3(PEX)

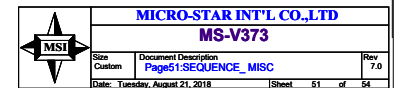
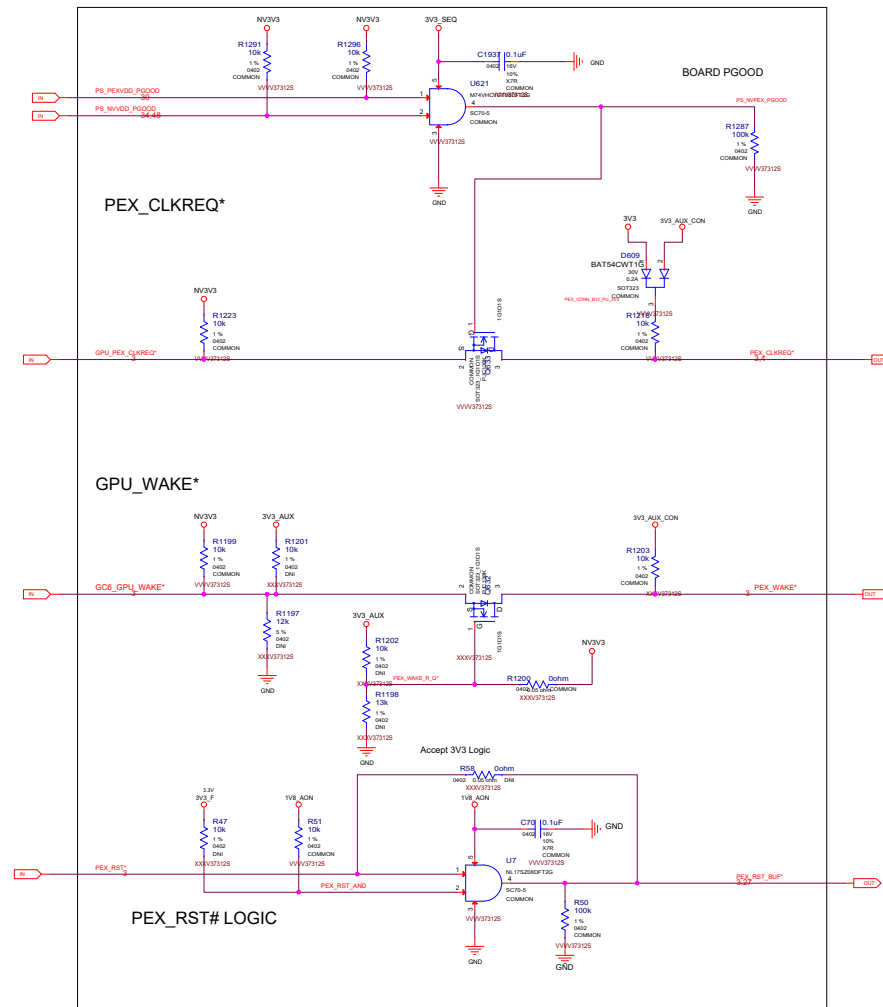
Dual Pre-Filter case:

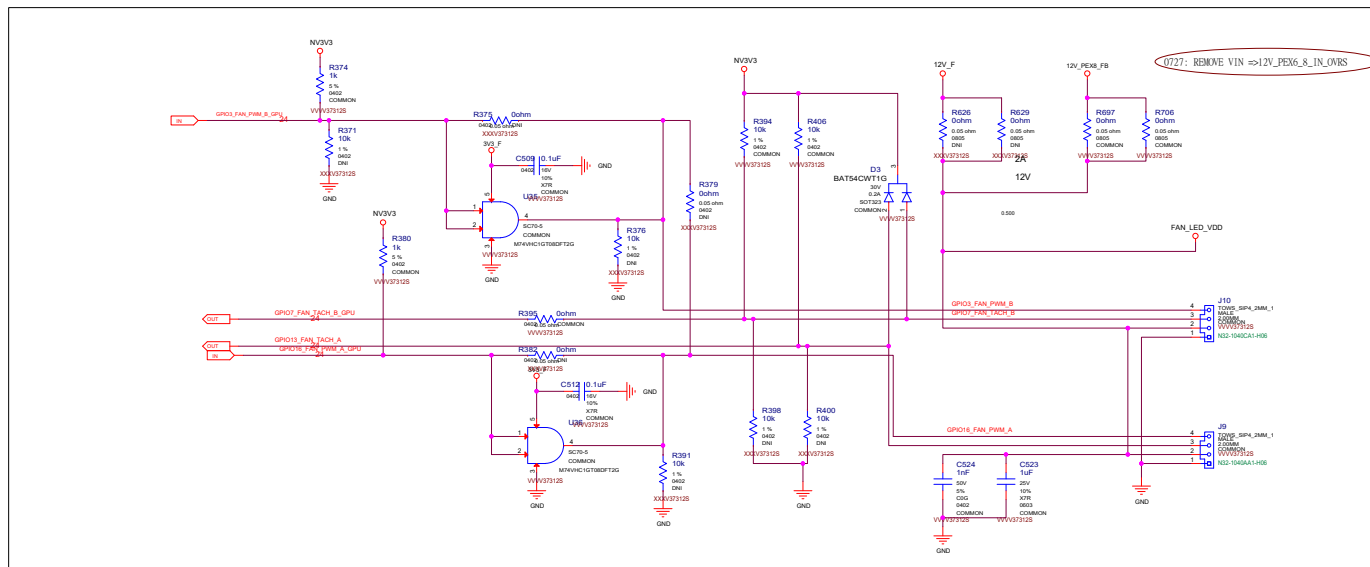
Only use the Primary Pre-Filter to sense 3V3PEX

and All Input 12Vs

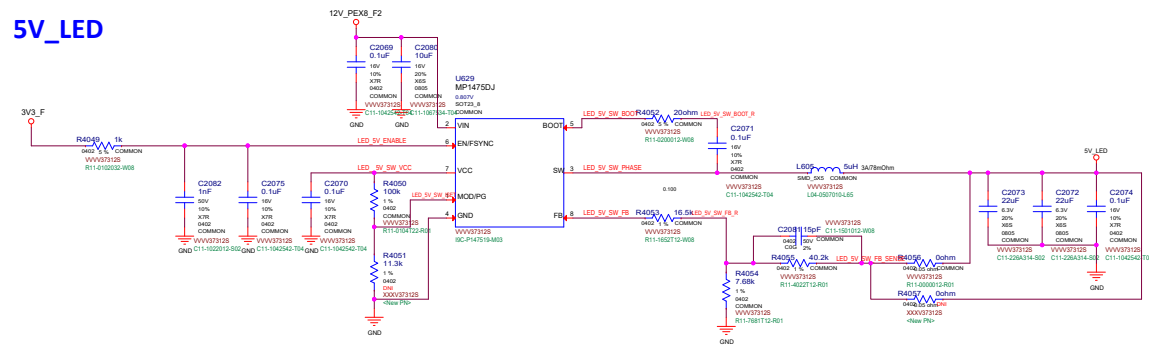
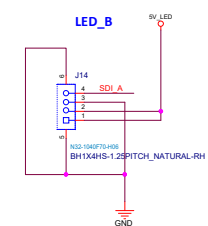
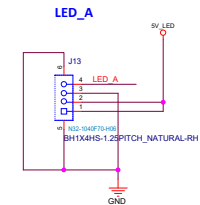
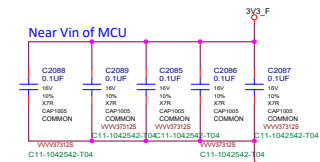
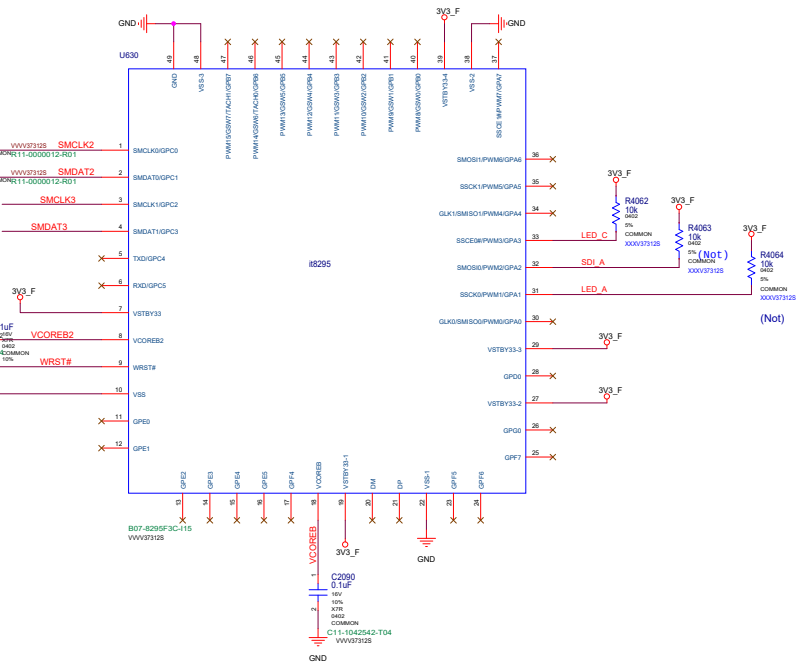
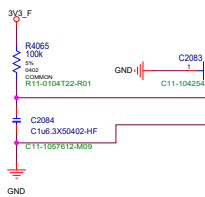
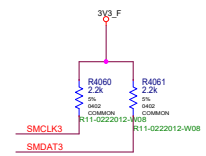
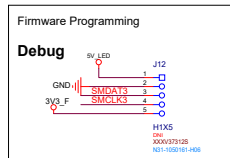
31.48

30.48





LED BOOST

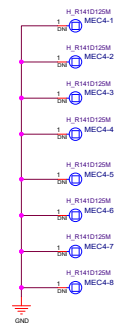
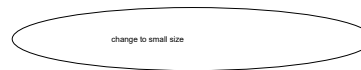
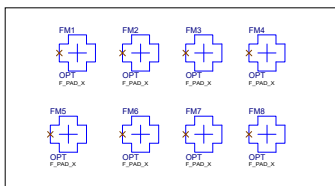
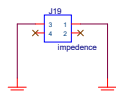
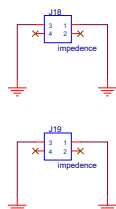
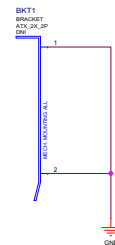




Screw



Brackets:



STIFFENER

Mechanical Holes Symbol

