

PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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52	LED & FAN HEADERS
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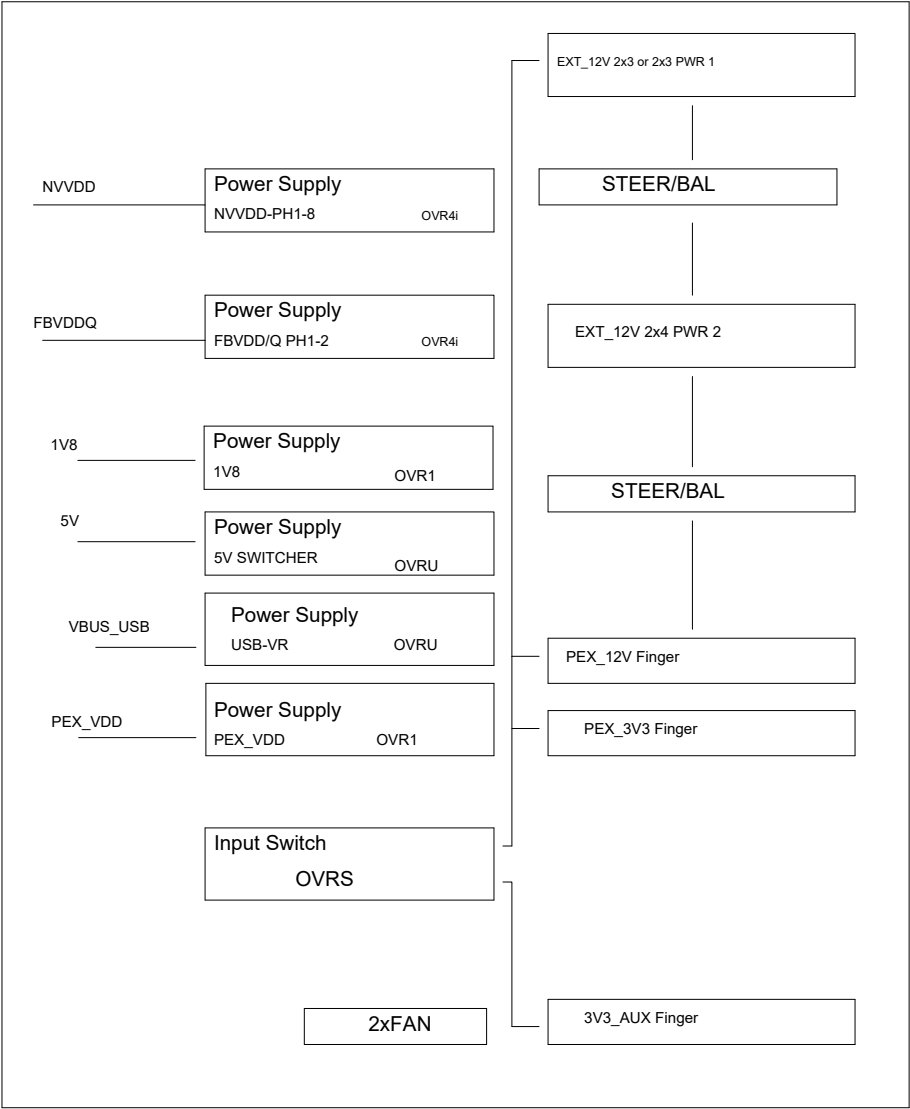
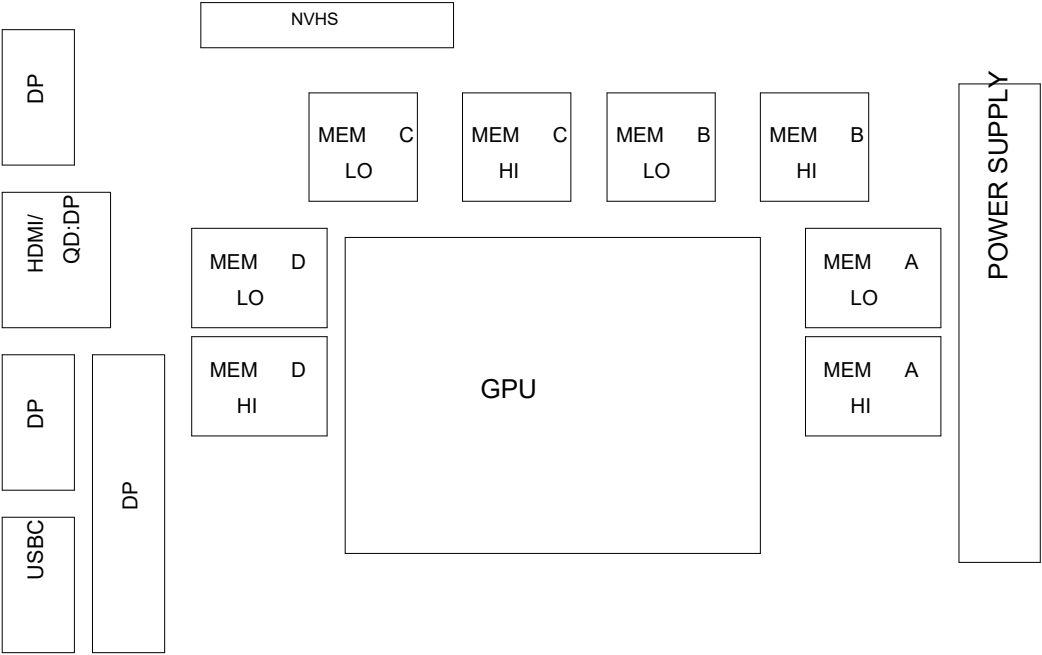
base on V372-02S change for D18 Z
1. P.23 remove SLI & BRIDGE_LED_VDD & SLI_BRG_PRST*
2. P.52 remove LED change FAN connector
3. P.53 remove LED
4. P.38/44 add FUSE
5. P.5~14 mem add <>
6. P.53 LED use V336-0D
7. P.32 remove
8. P.35~38 dual MOS
9. P.33 change dual MOS
10. P.43 remove
11. P.31 change to UP1666
12. P.21 remove colay DP

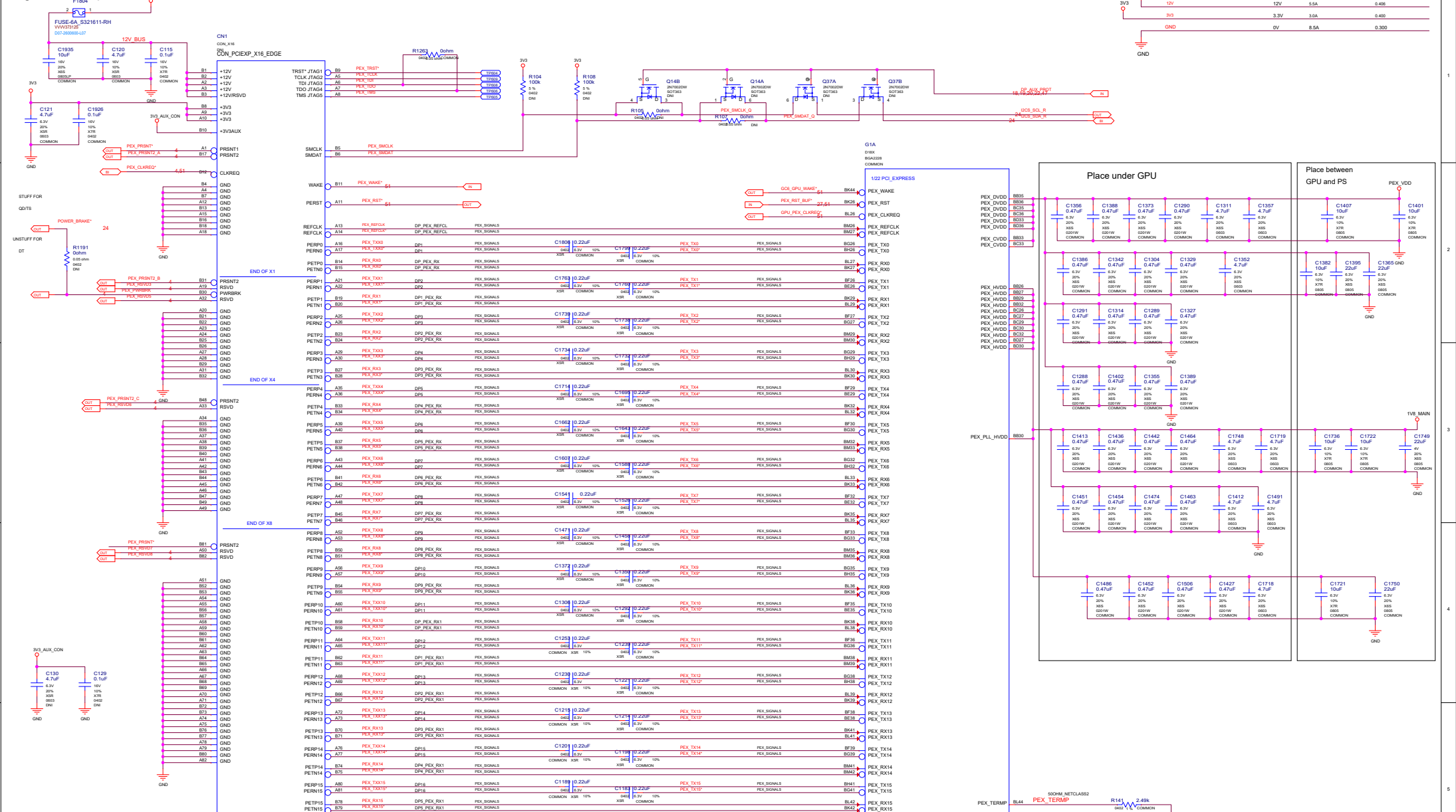
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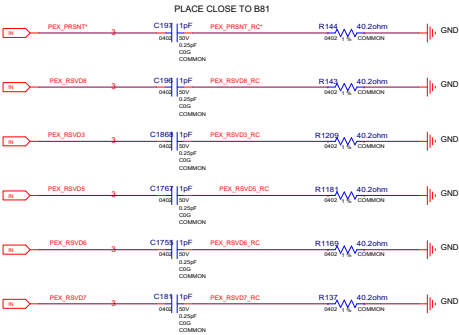
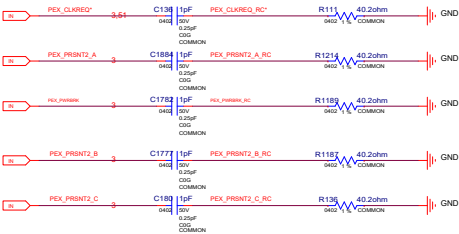
page 24: REMOVE GPIO29_IDLE_IN_SW
remove GPIO9_INPUT_DYN_BAL2
page 29: 12V_F RTD3 change to 12V_F
page 30: 12V_F RTD3 change to 12V_F
page 33: 12V_F RTD3 change to 12V_F
移除保護線路
page 39: remove INPUT SWITCH RTD3
page 40: remove INPUT SWITCH RTD3 USB
page 44: remove INA3221

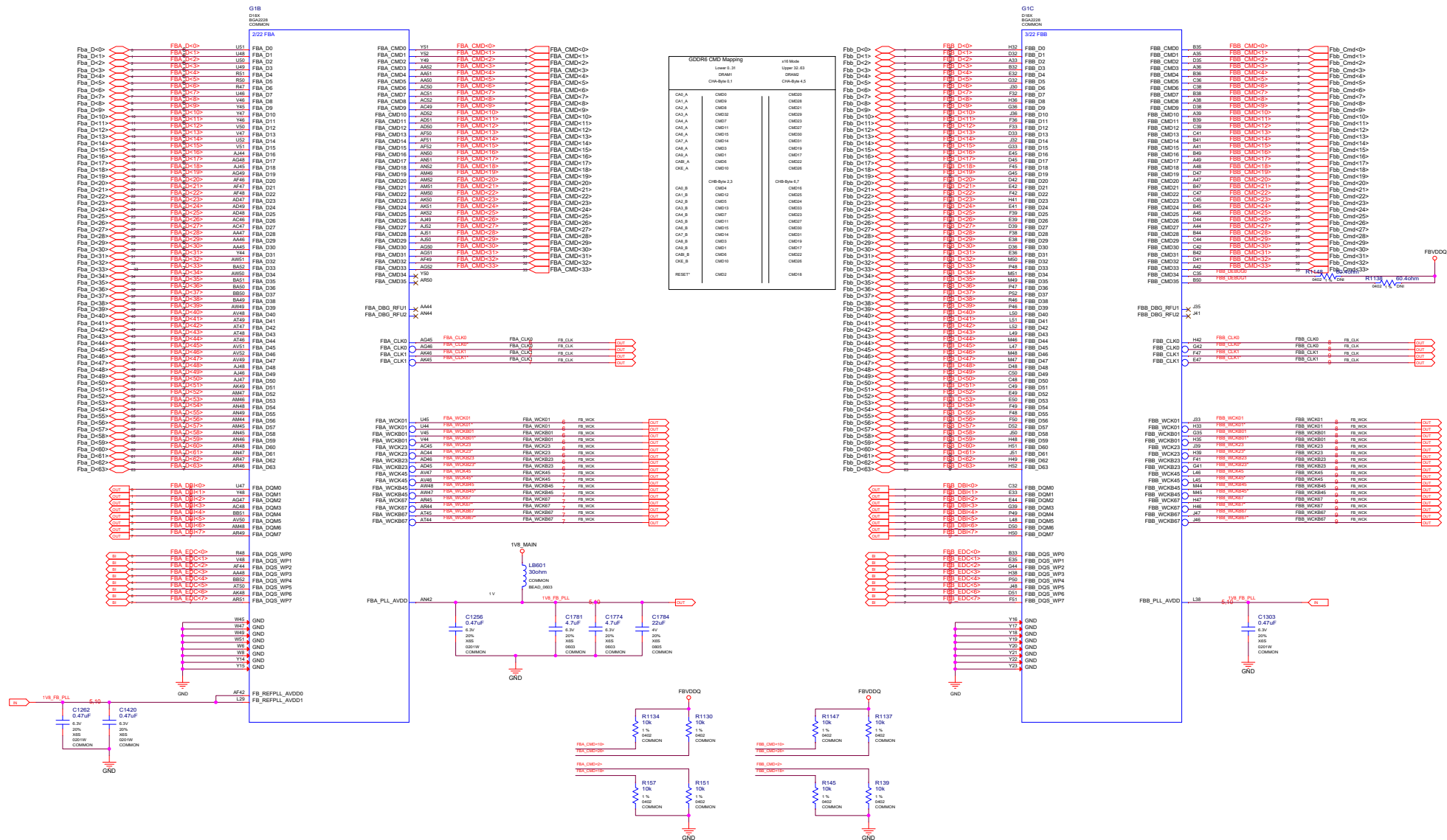
page 46: remove PFM_SKIP net
remove PS_RTD3_12V_SW net
page 47: remove PS_VMON_PGOOD net
12V_F RTD3 change to 12V_F
remove 3V3_PORT
remove 3V3_RTD3 change to nv3v3
page 48: remove OC_CRIT* NET from ina3221
remove PS_VMON_PGOOD net
page 49: PCIE Voltage Monitor1
page 52: REMOVE VIN =>12V_PEX6_8_IN_OVRS

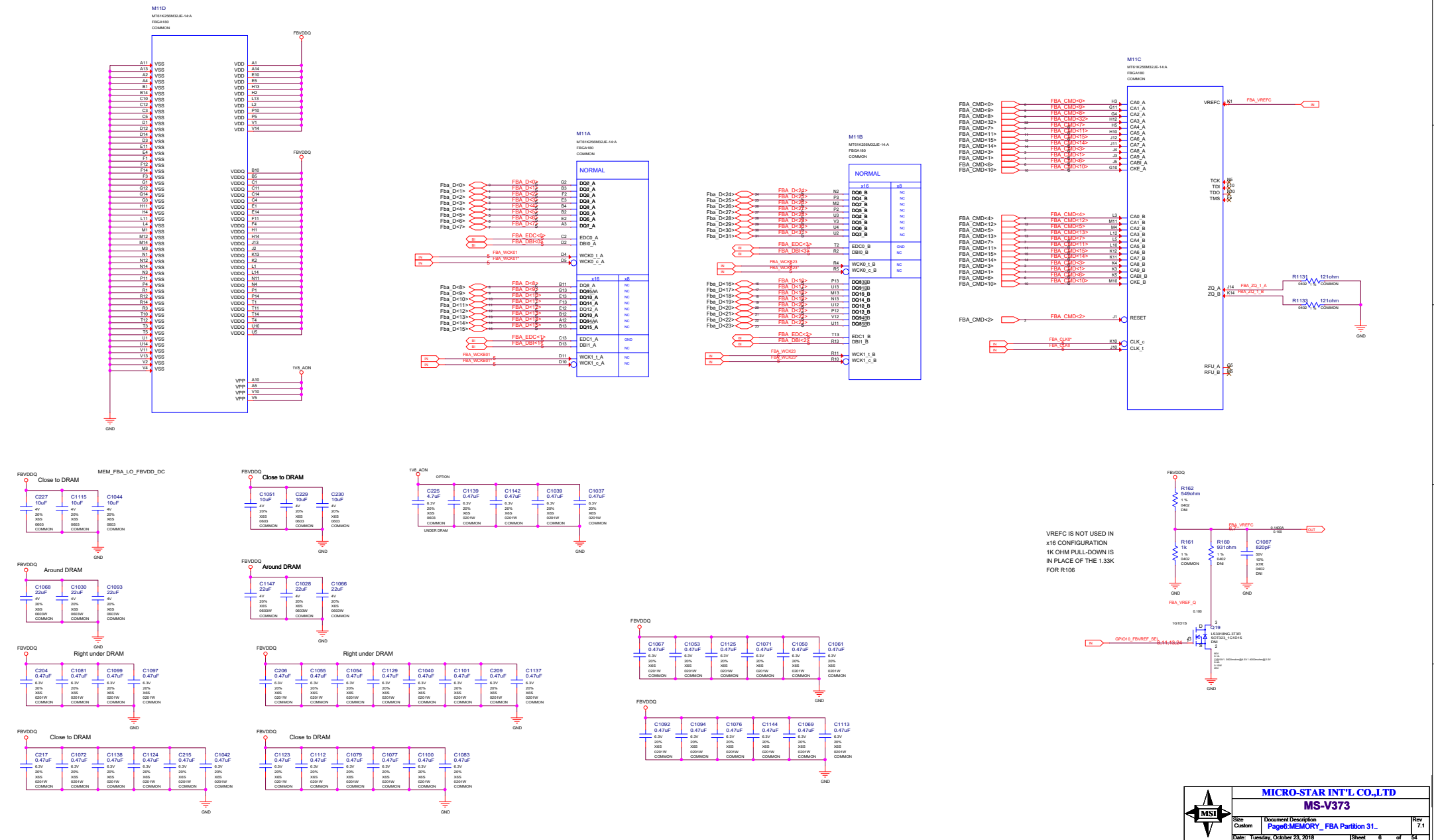
page 54: change GPU scrow holes to small size

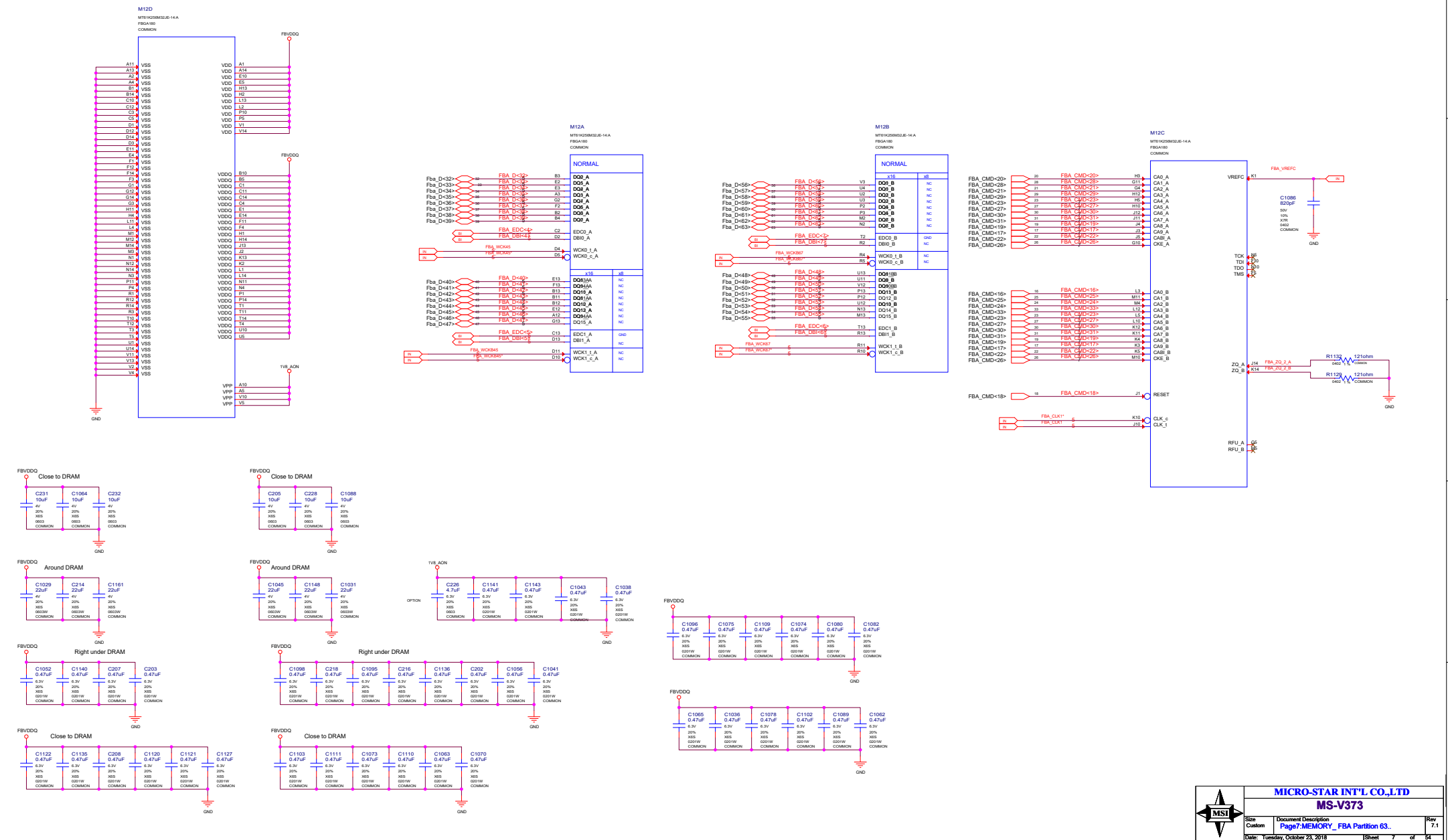


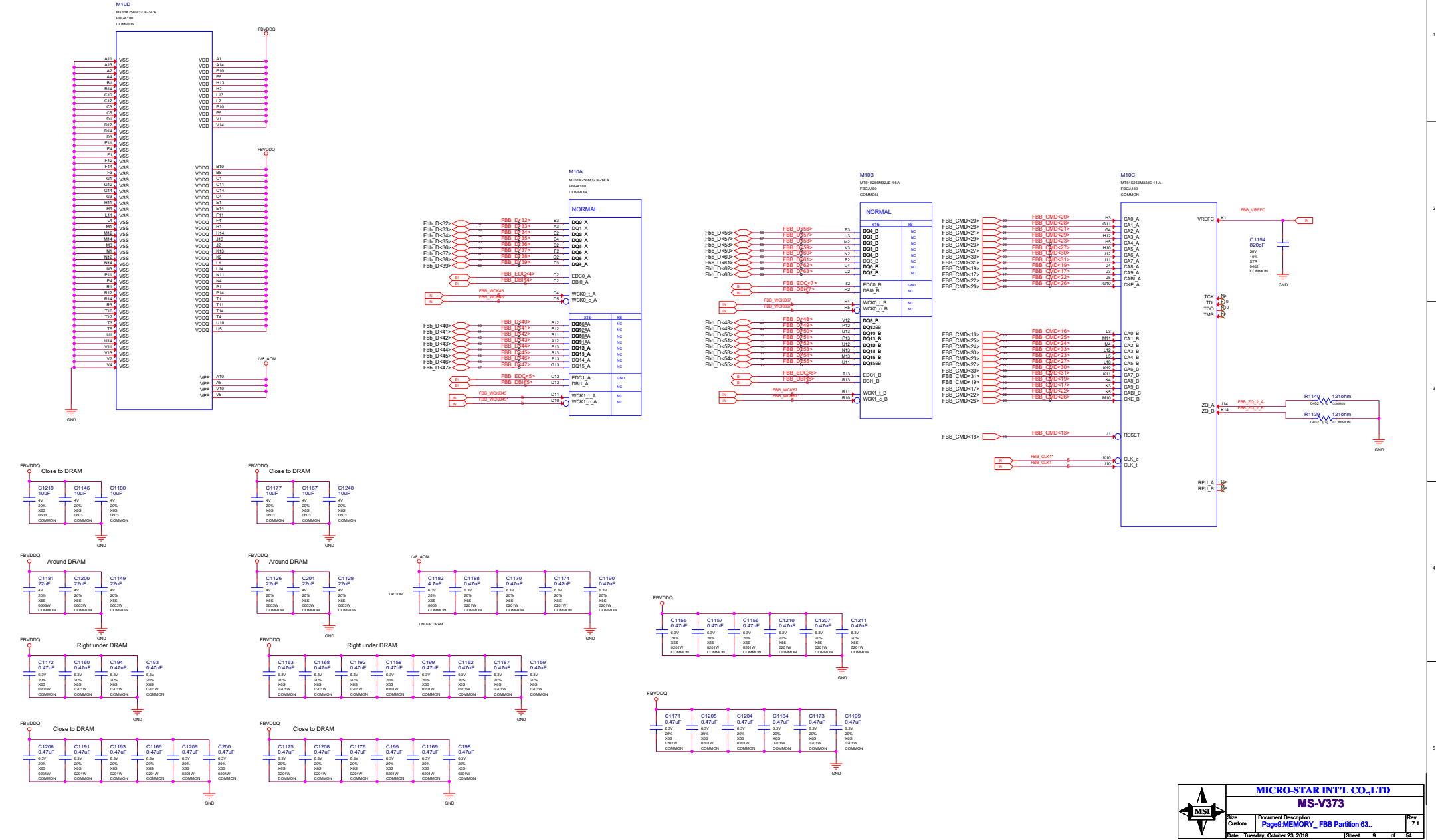


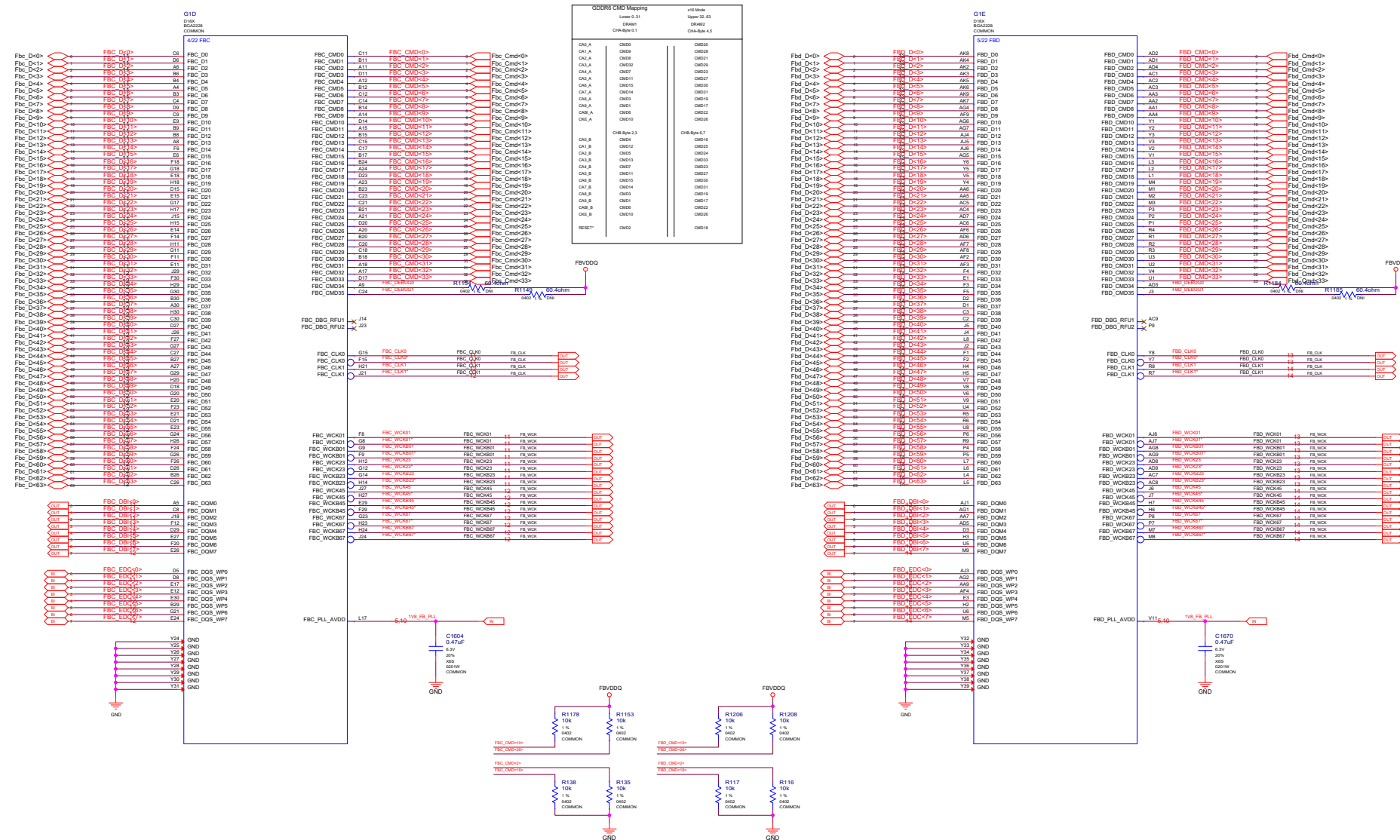


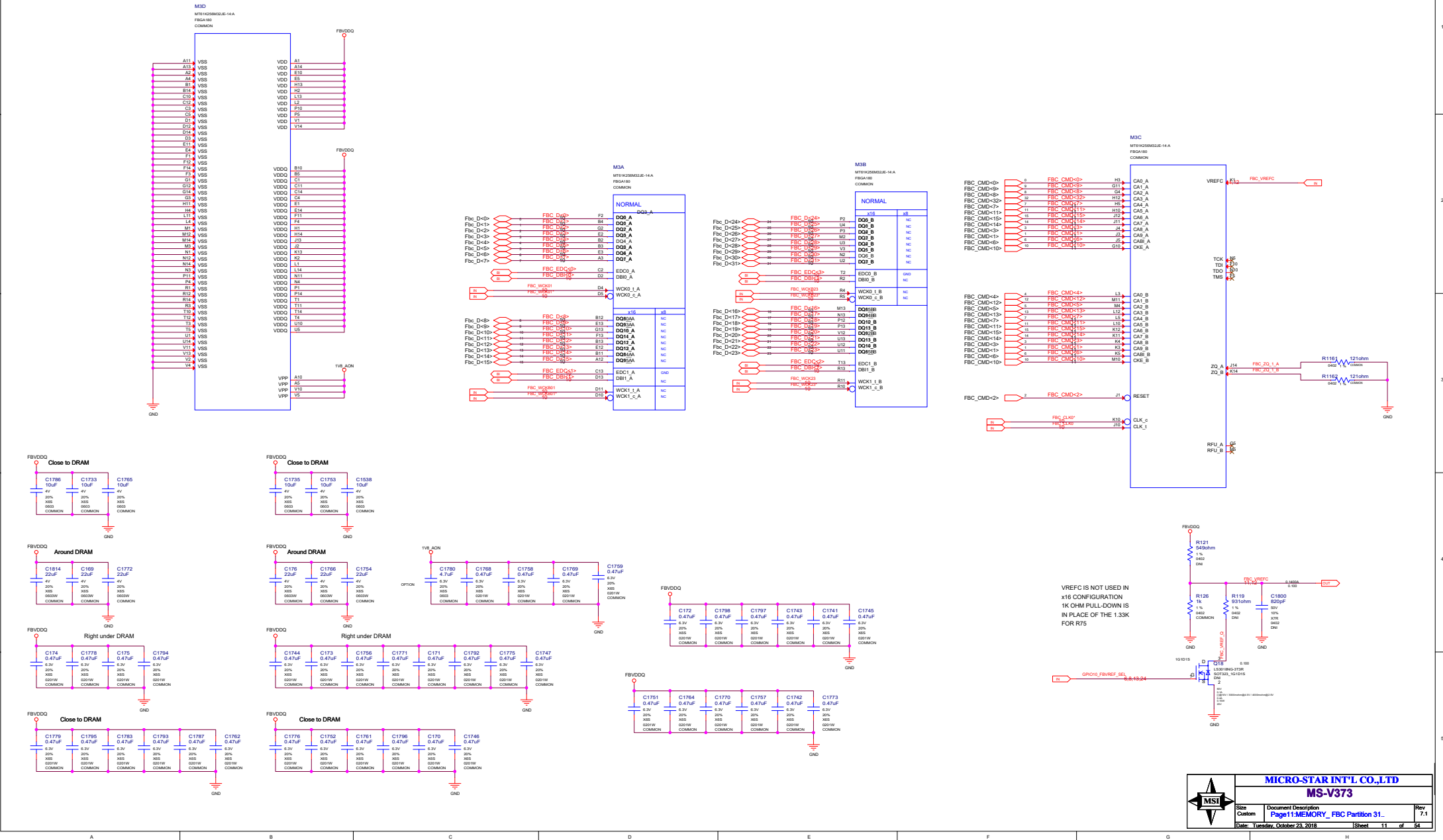


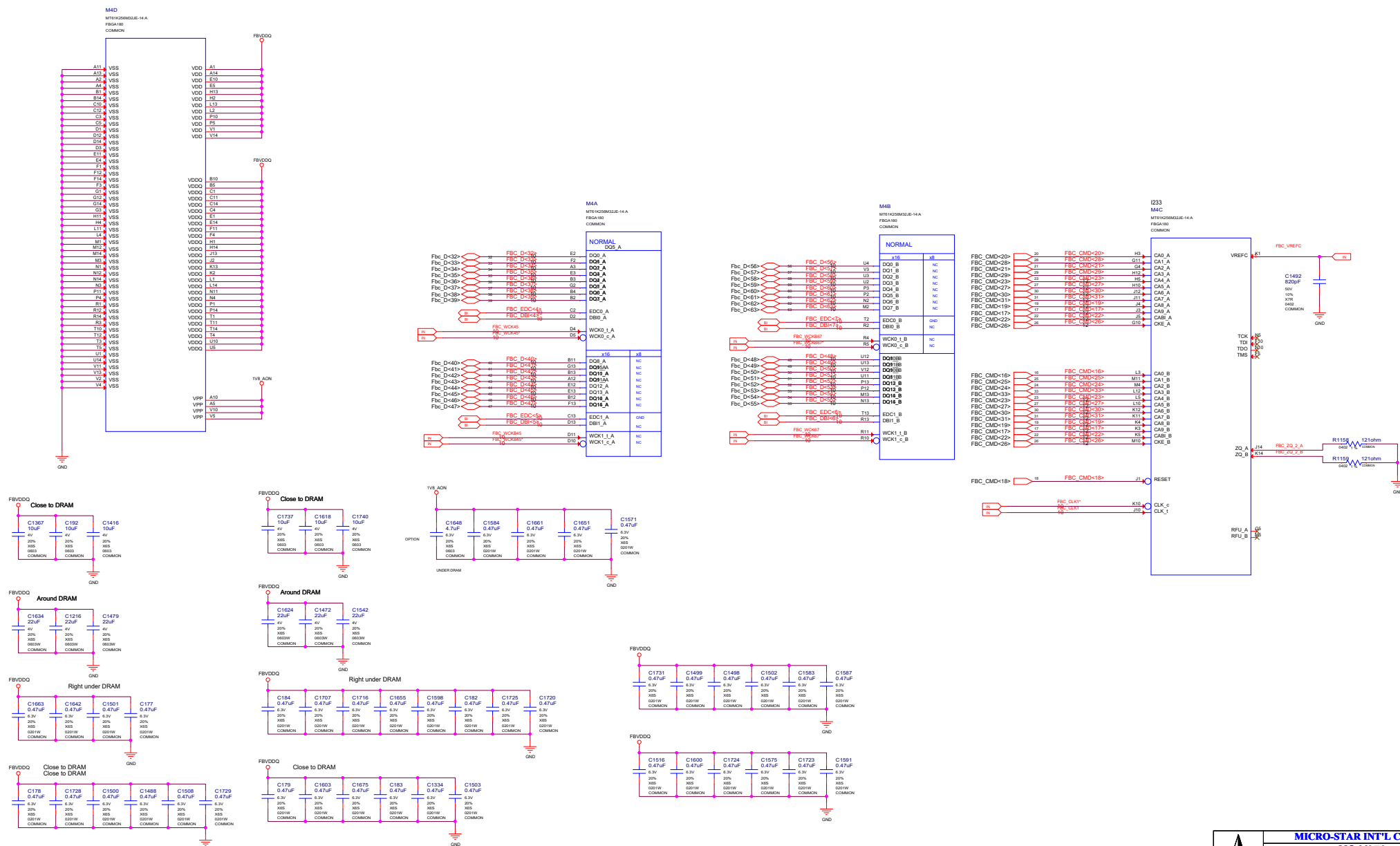


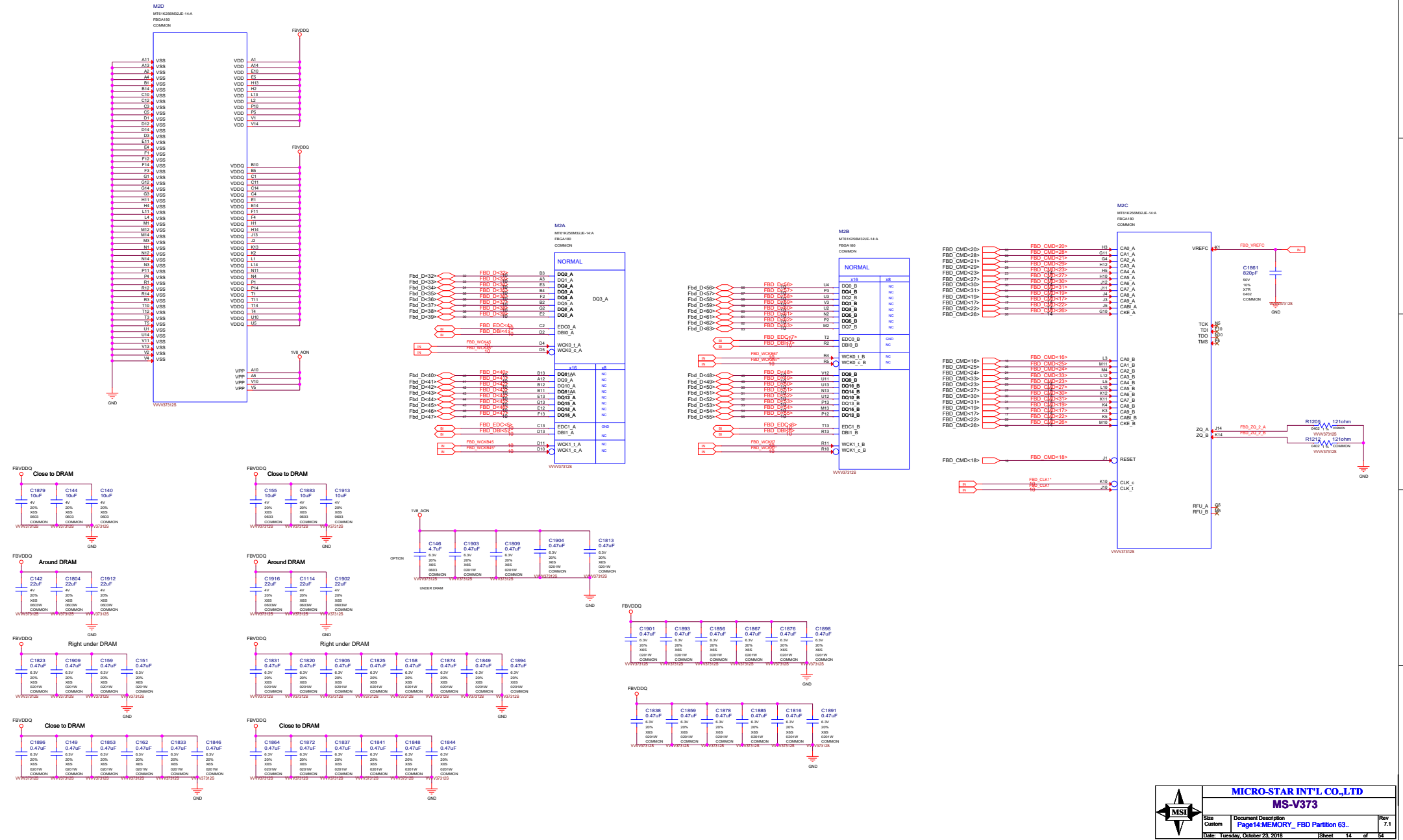


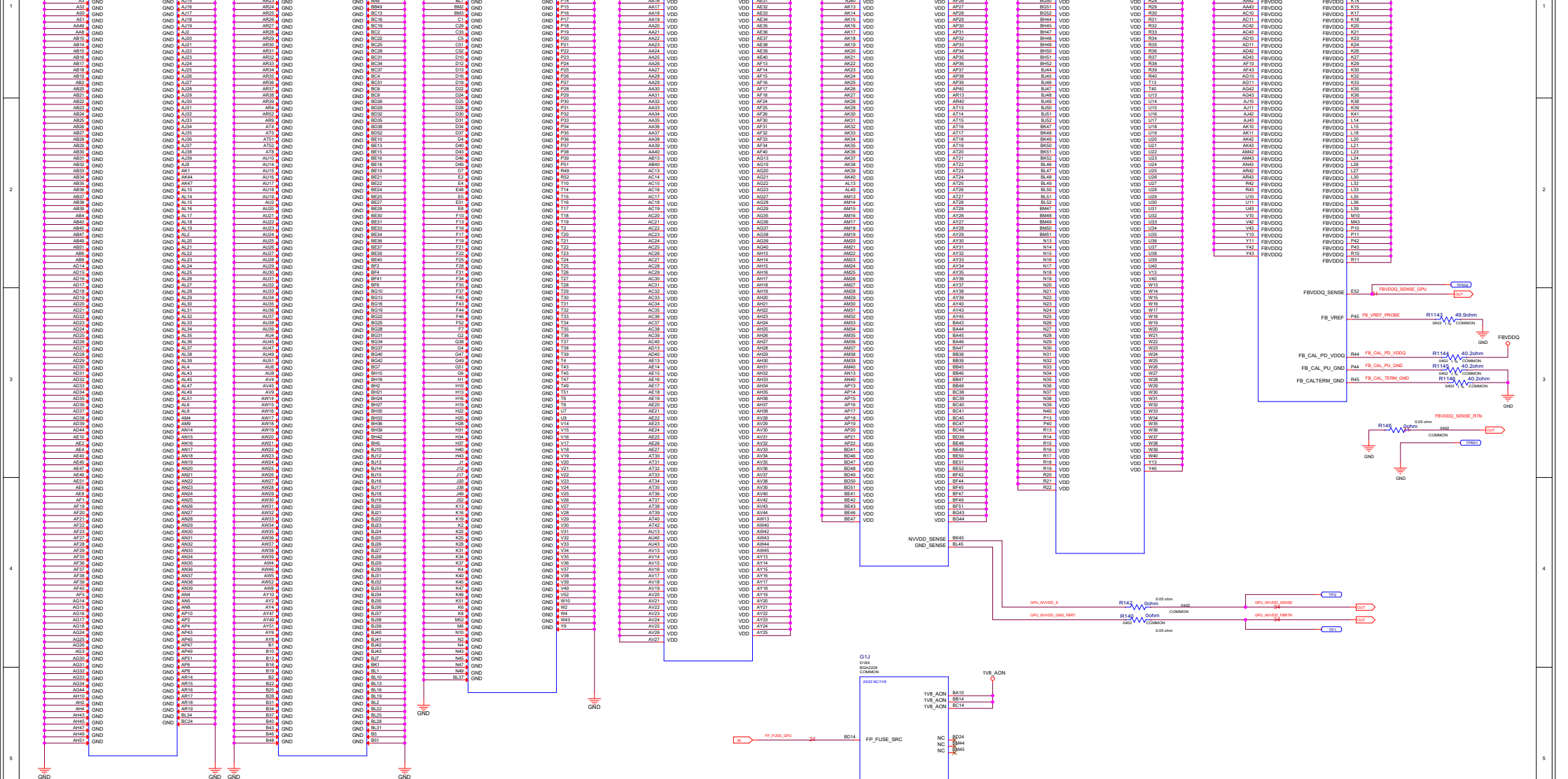








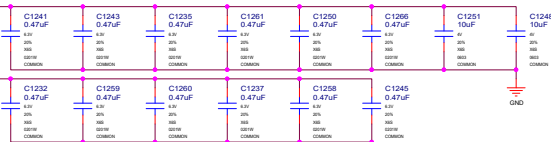




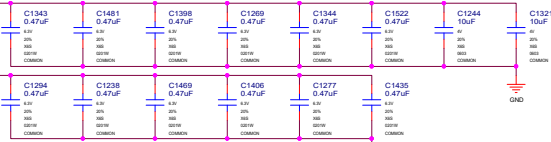
NVVDD

FBVDDQ

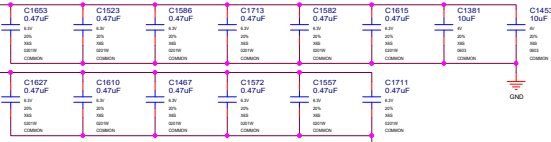
Partition A



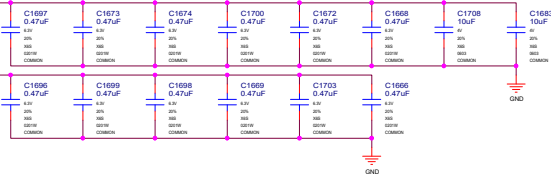
Partition B



Partition C



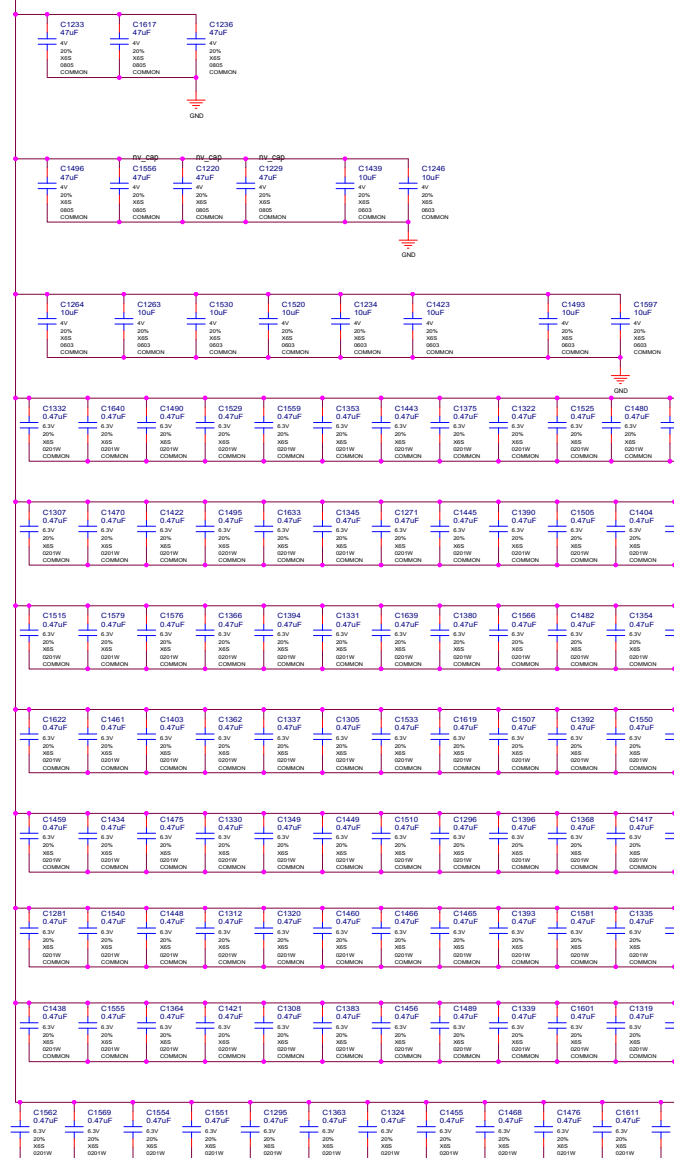
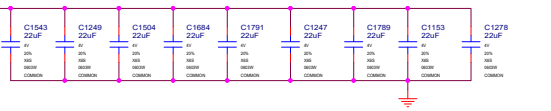
Partition D



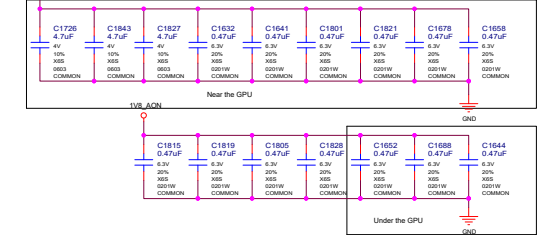
Place Close to GPU



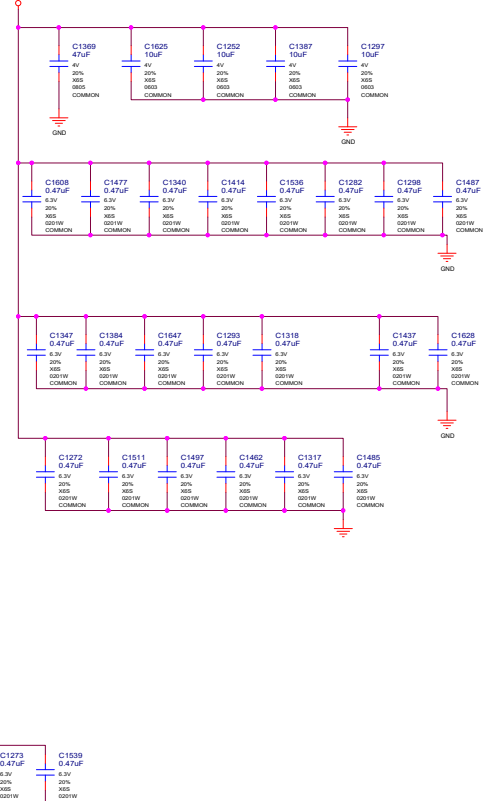
Place Close to GPU

032-0532-000
XES
0805

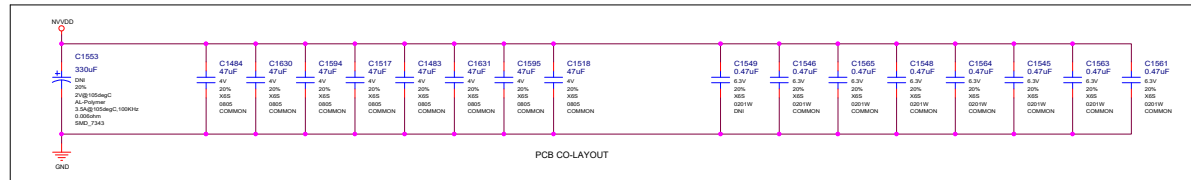
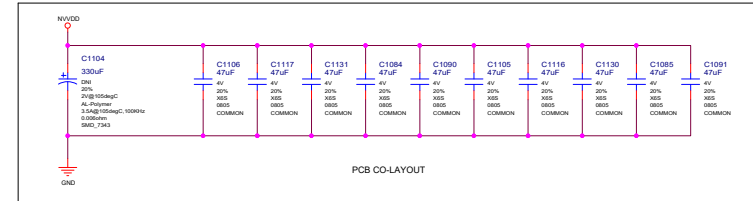
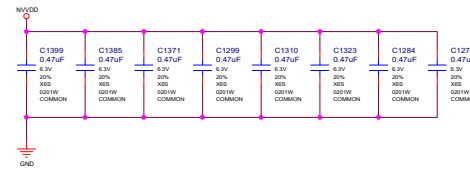
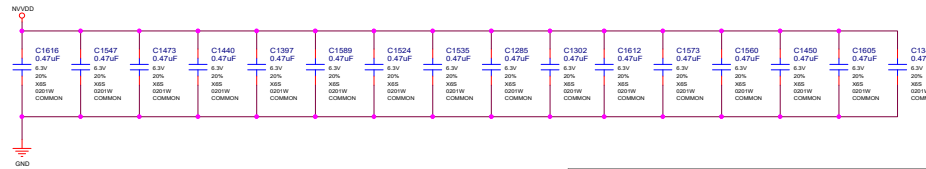
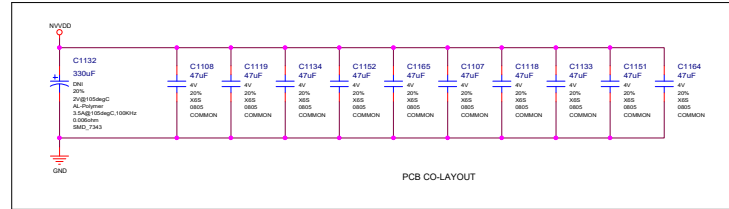
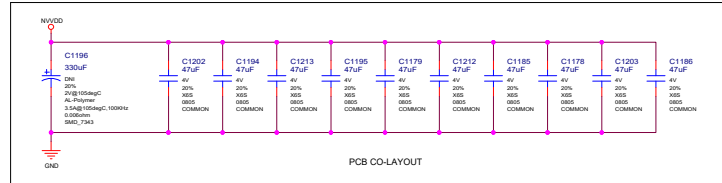
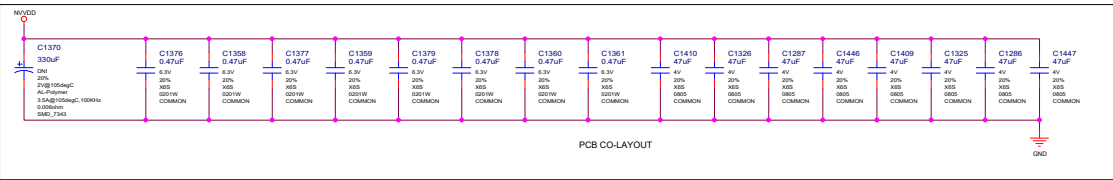
1V8 AON

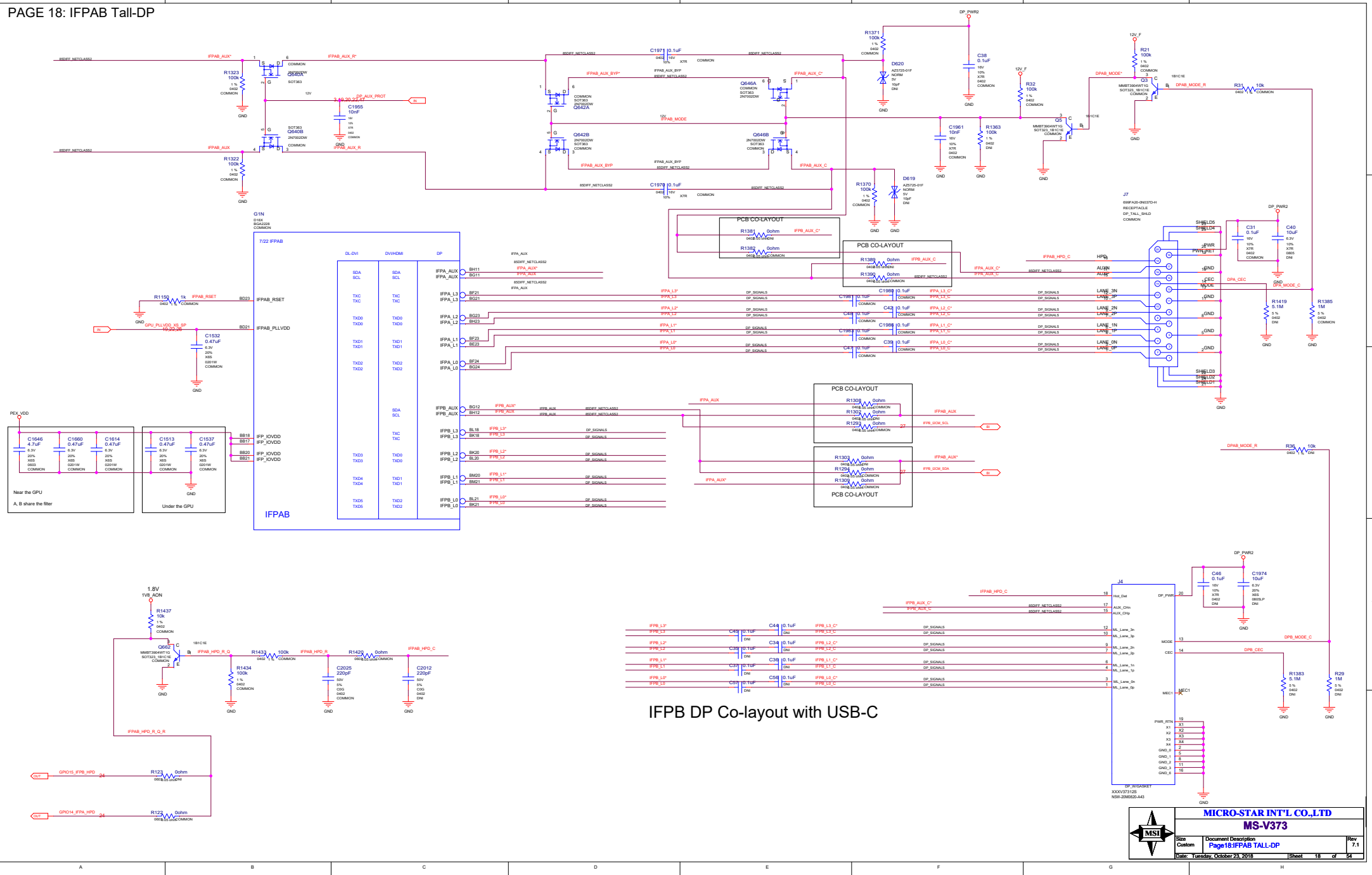


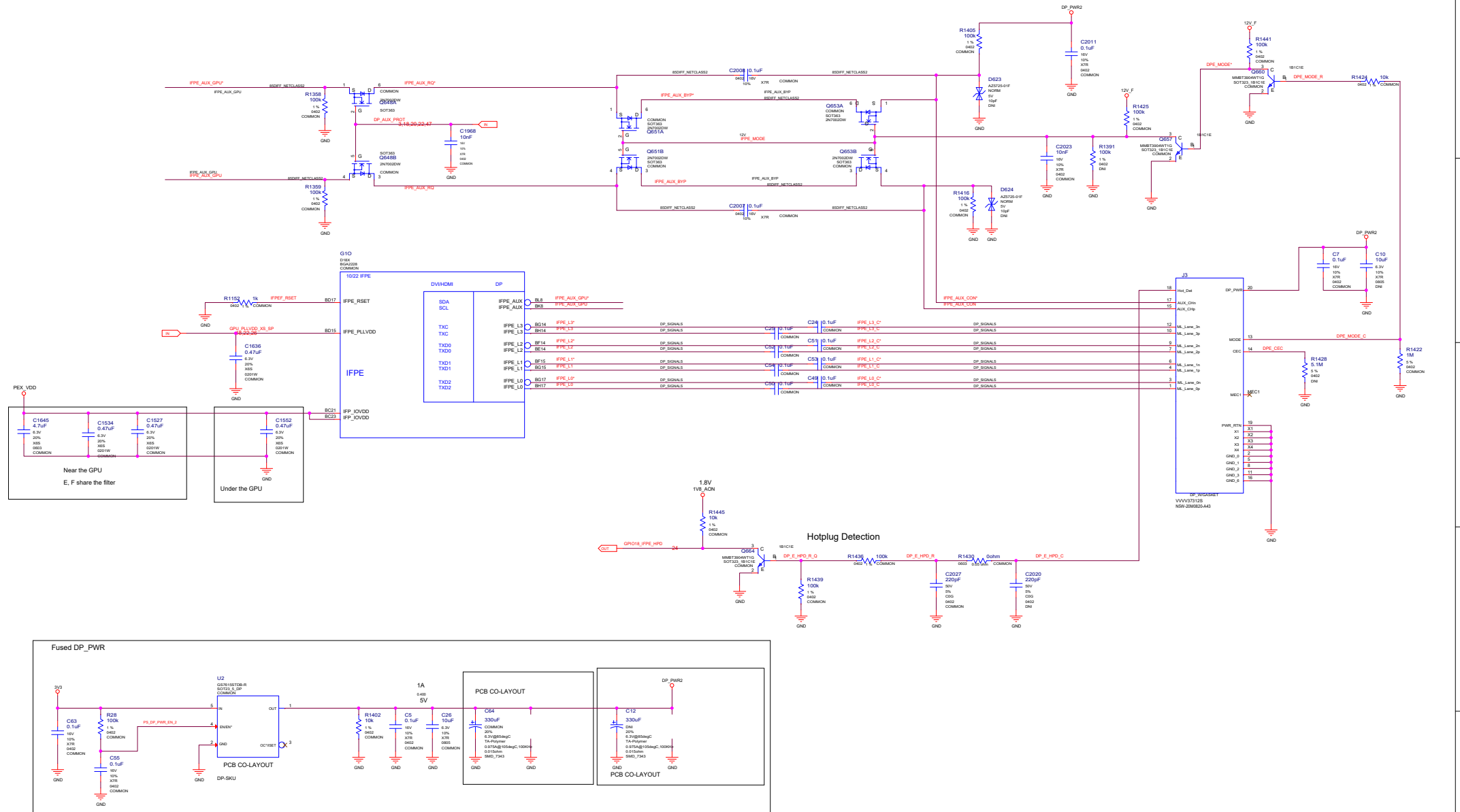
NVVDD

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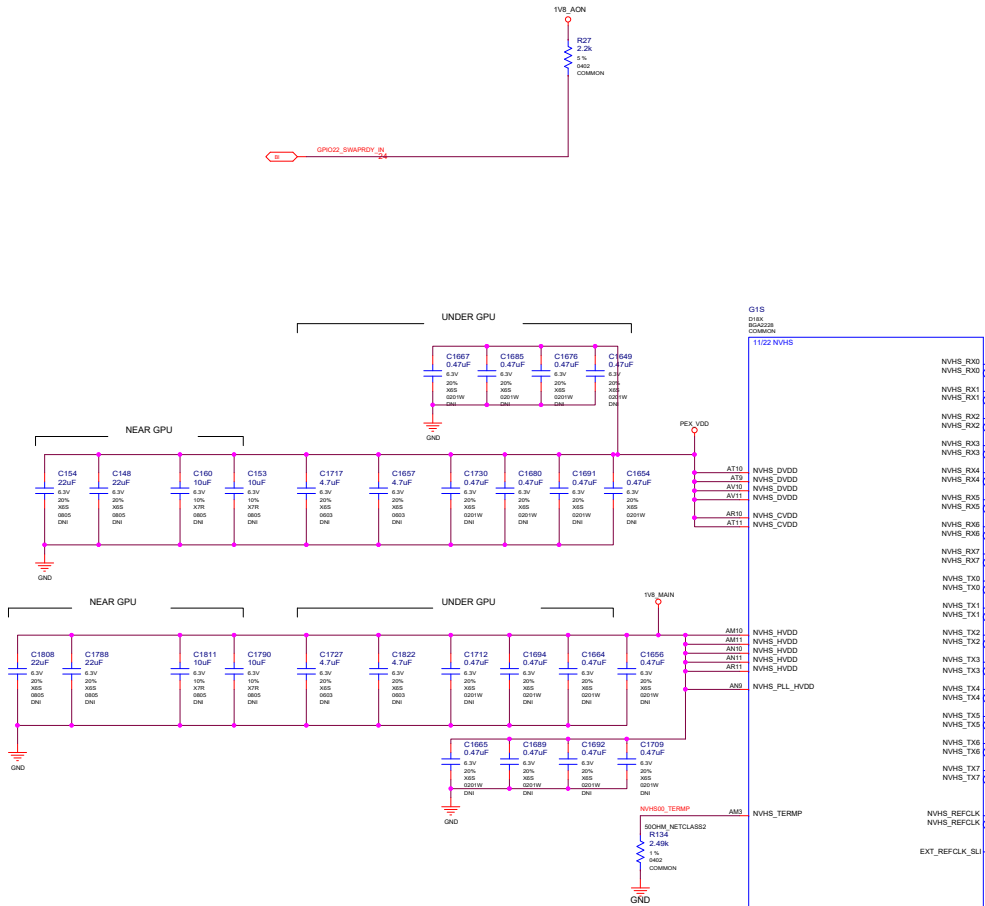
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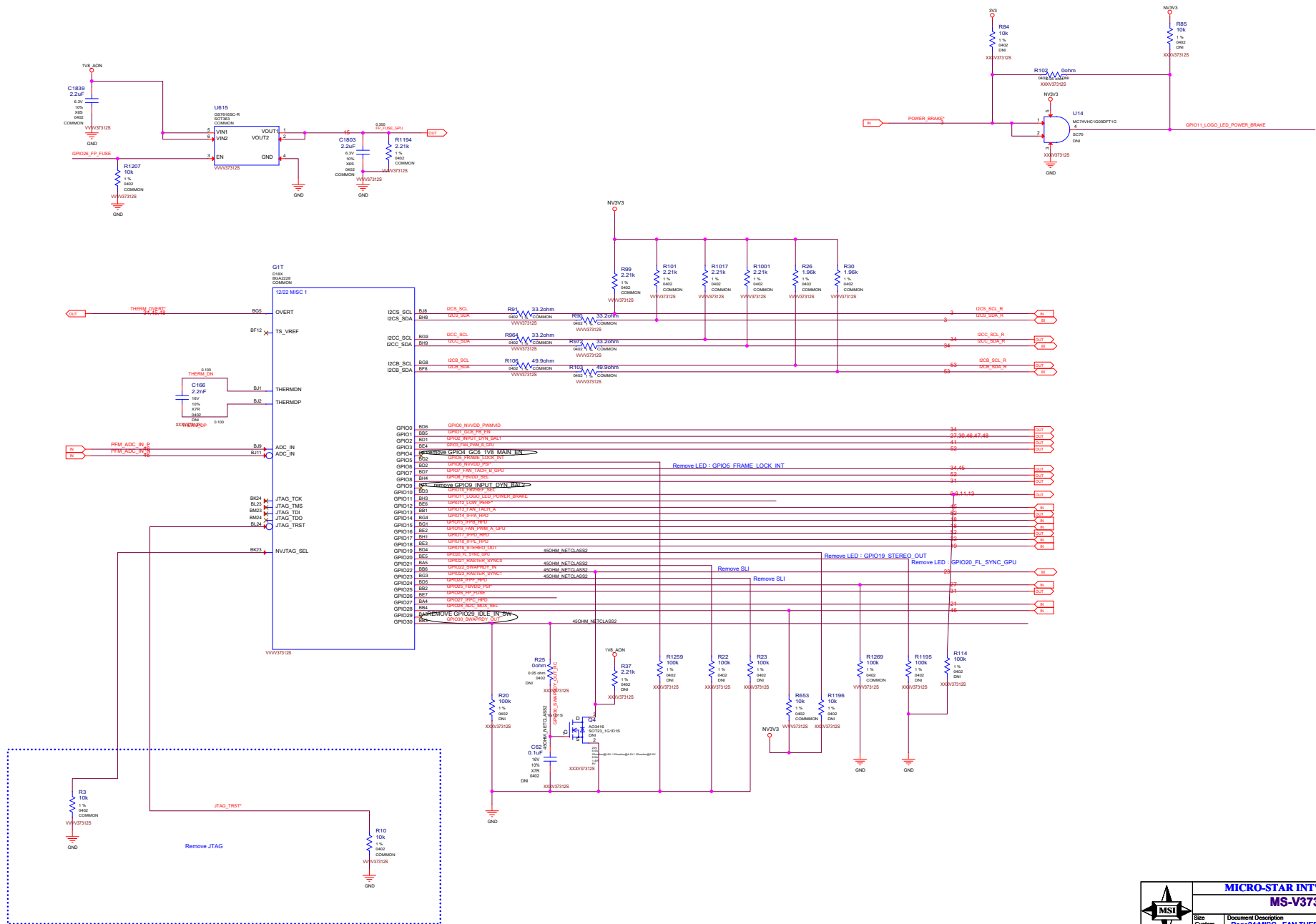












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Size Custom	Document Description Page24:MISC_ FAN,THERMAL,JTAG,GPI	Rev 7.1
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H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

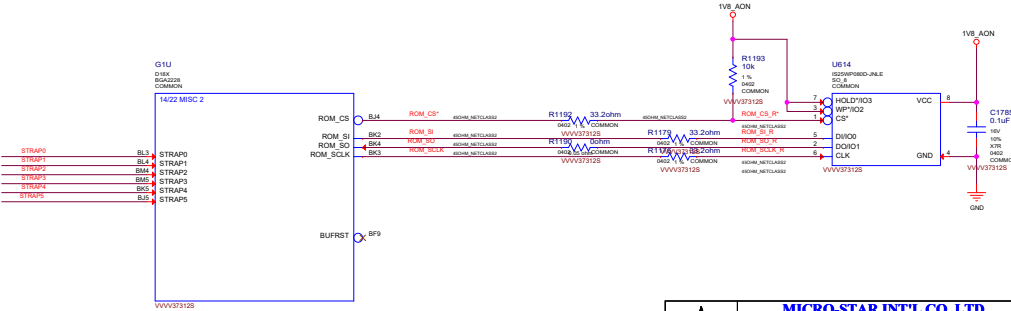
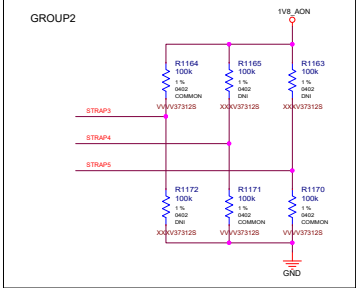
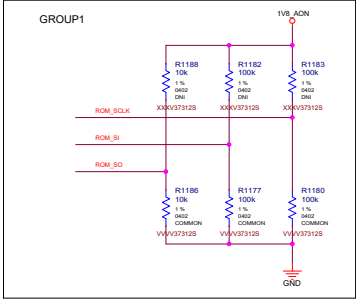
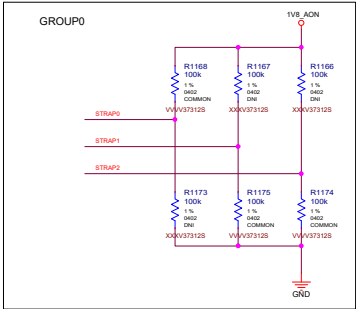
DEFAULT

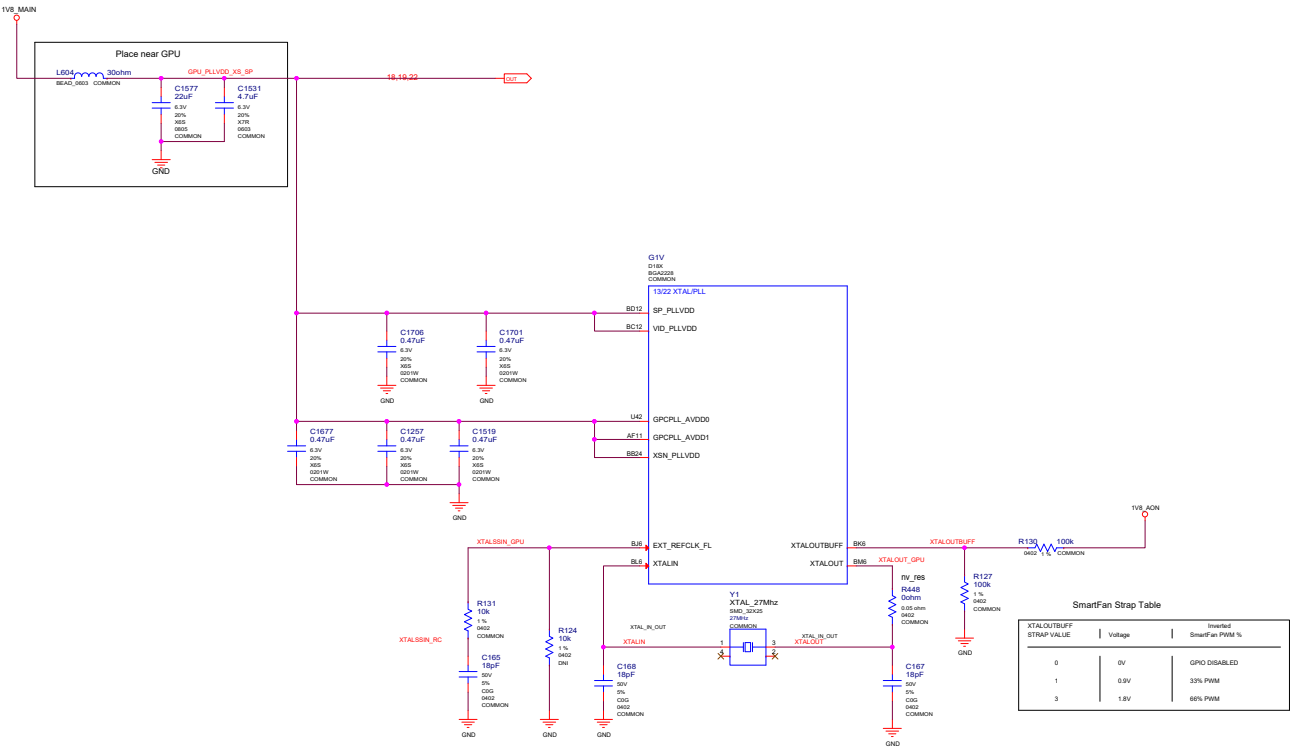
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

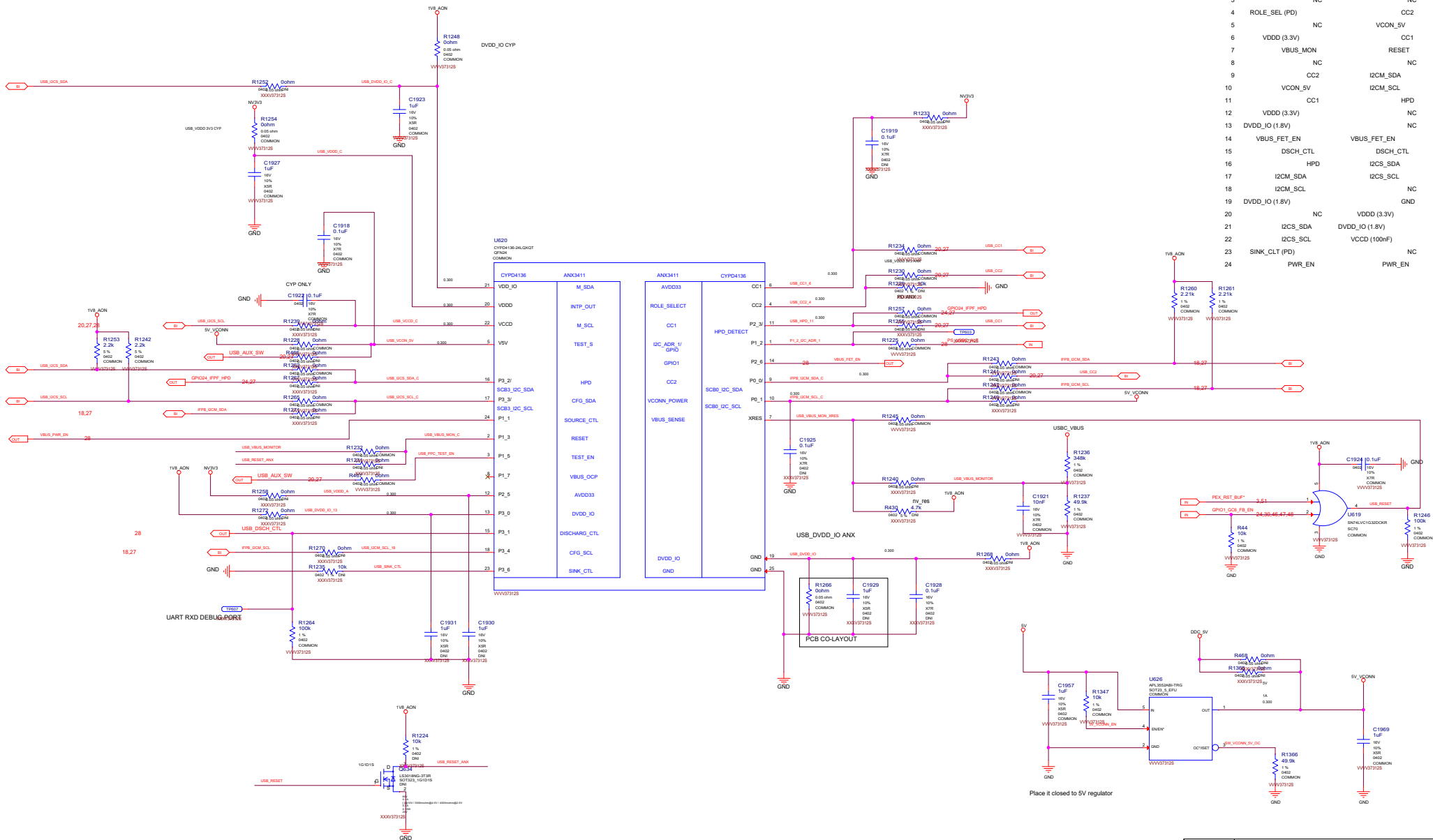
- 1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
- 1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL
- 1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
- 1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Default

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung







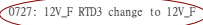
PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_SV
6	VDDO (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_SV	I2CM_SCL
11	CC1	HPD
12	VDDO (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDO (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (1000F)
23	SINK_CTL (PD)	NC
24	PWR_EN	PWR_EN



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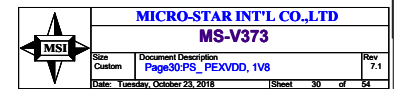
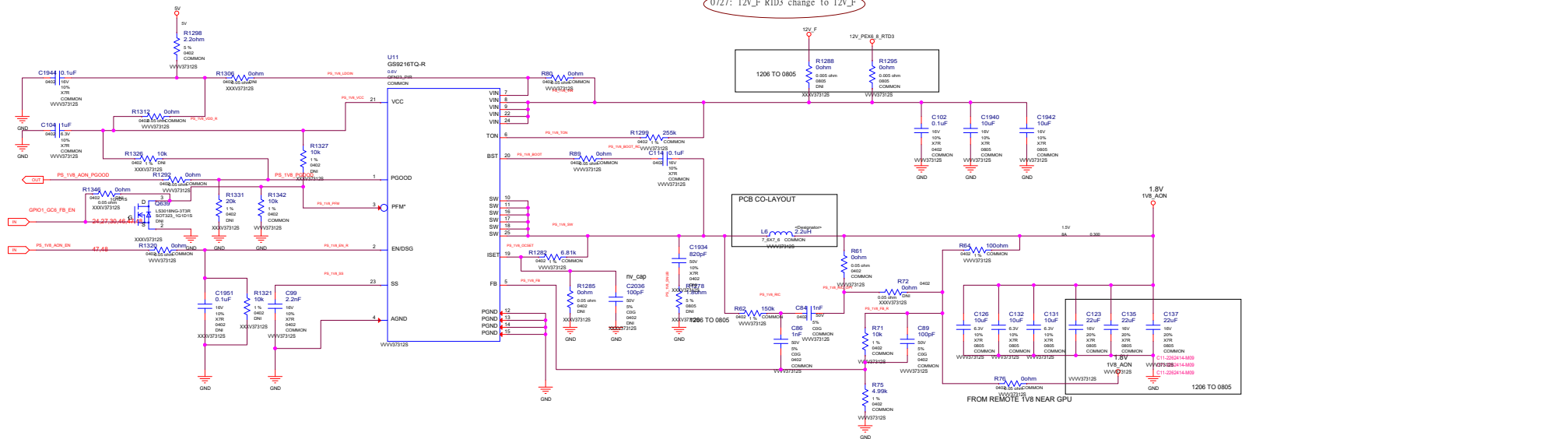
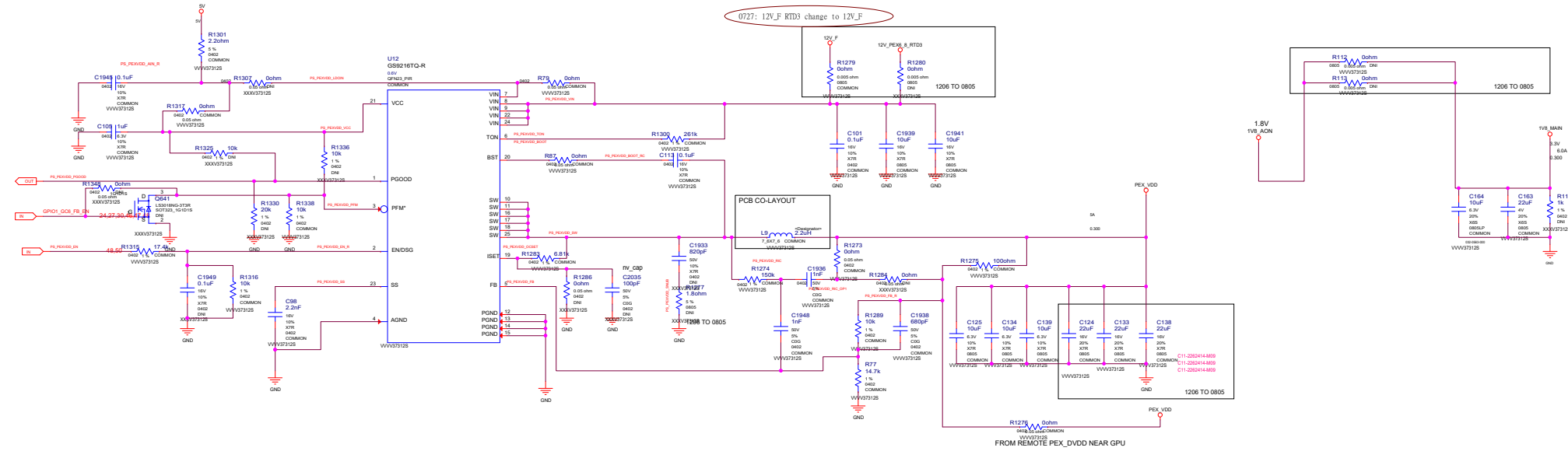
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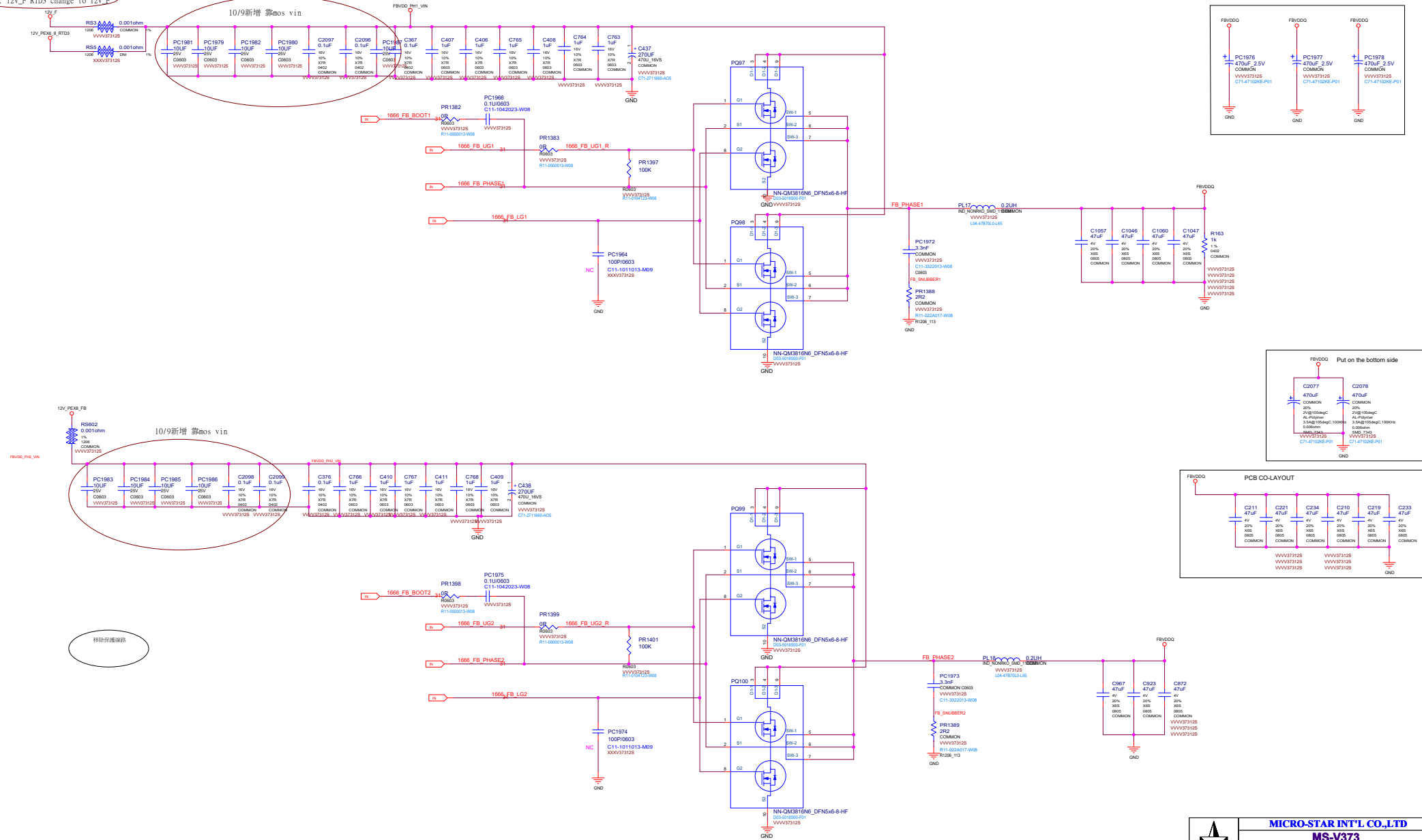


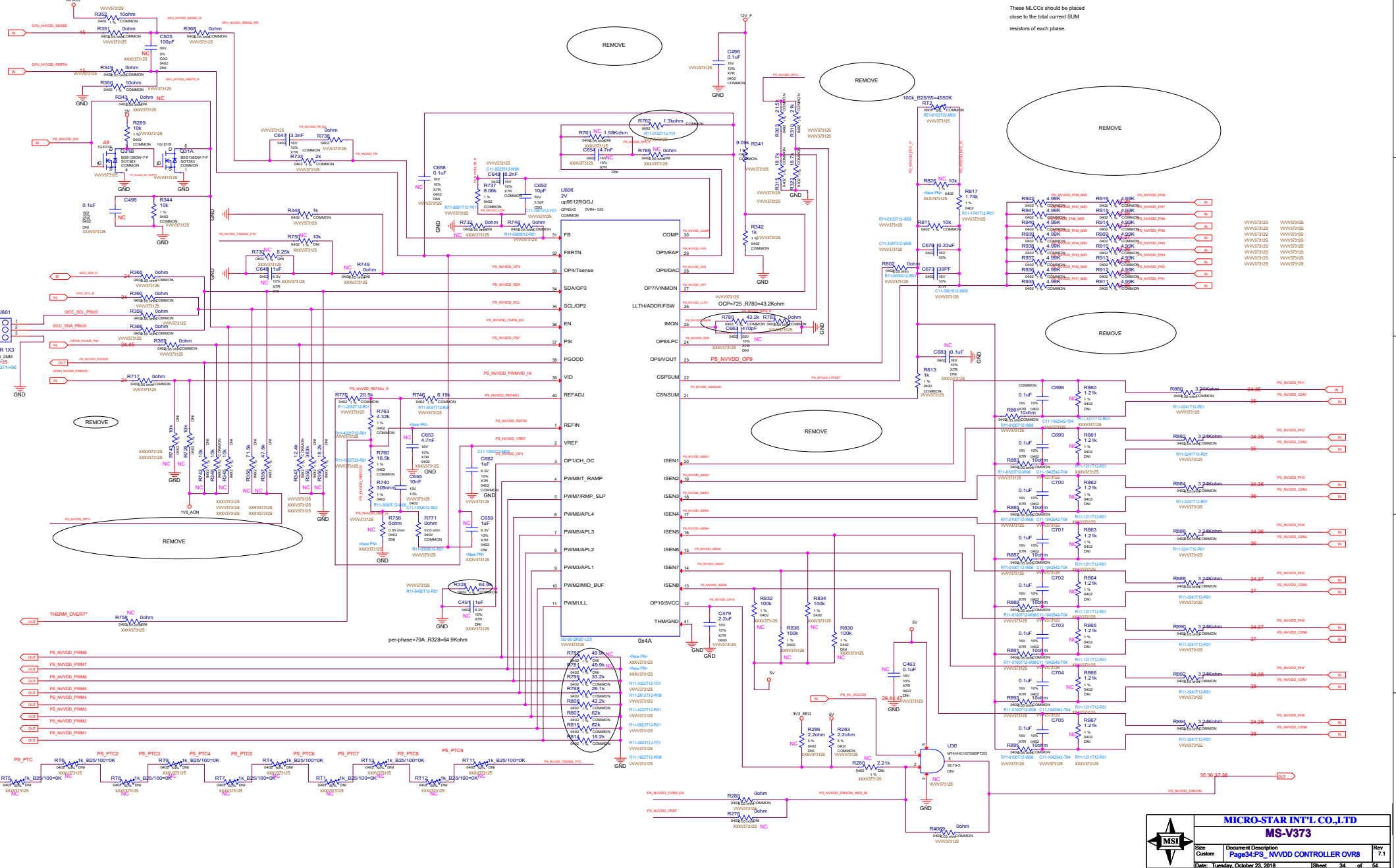
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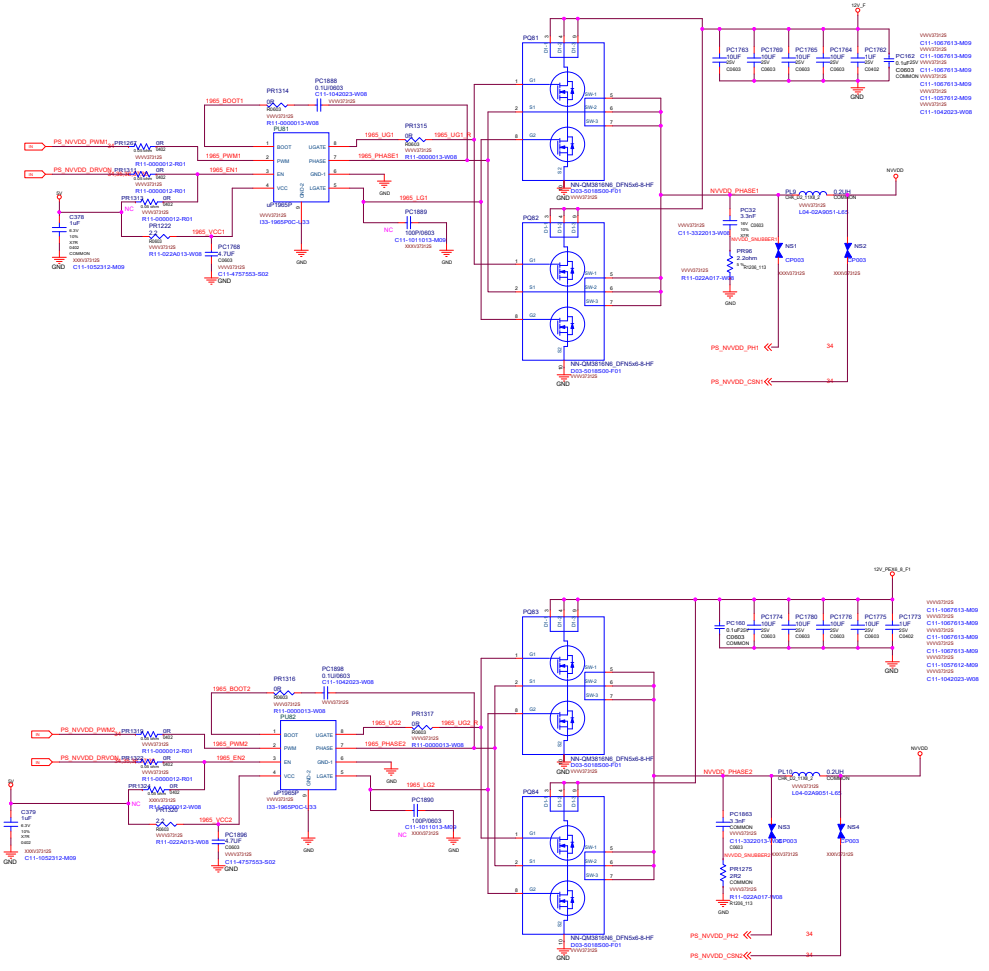
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Custom	Page32:PS_ FBVDD CONTROLLER OVR3	7.1
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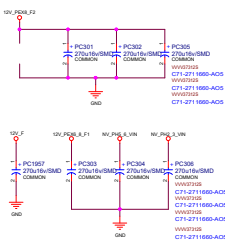
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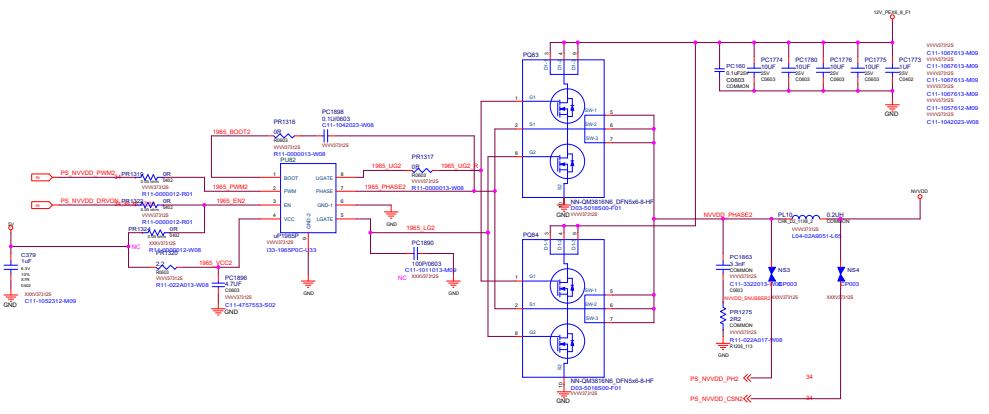
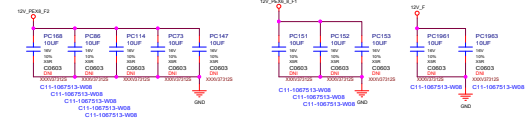


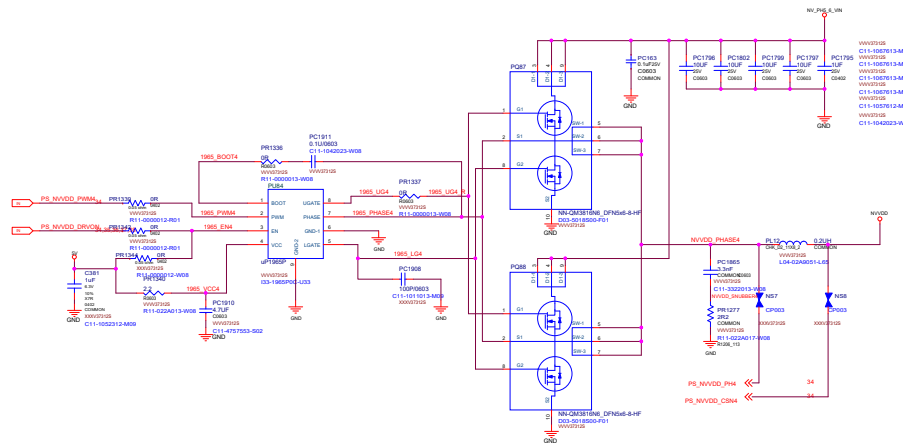
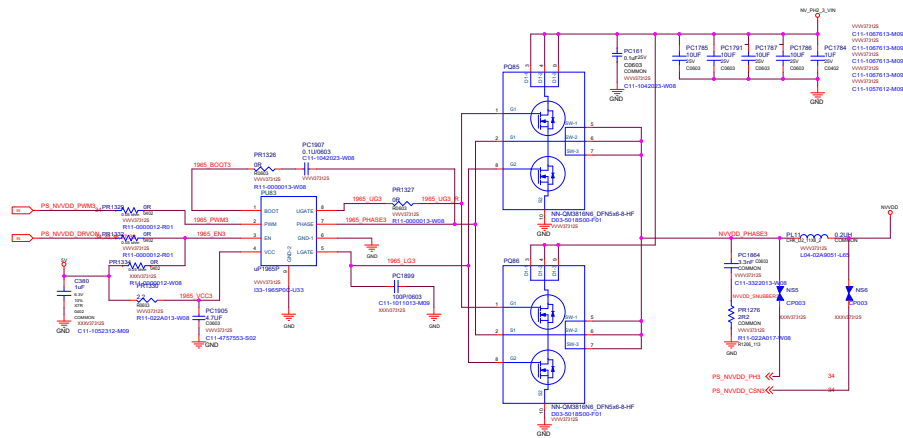


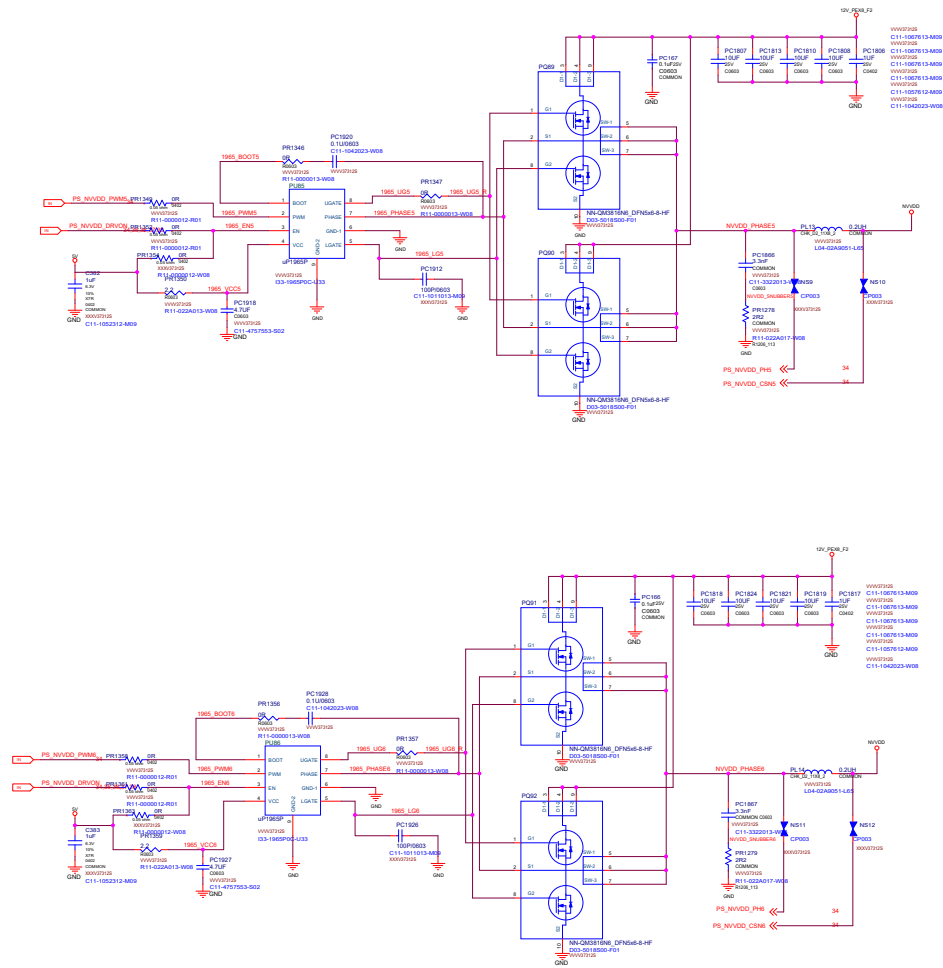
EXT_12V Input CAP

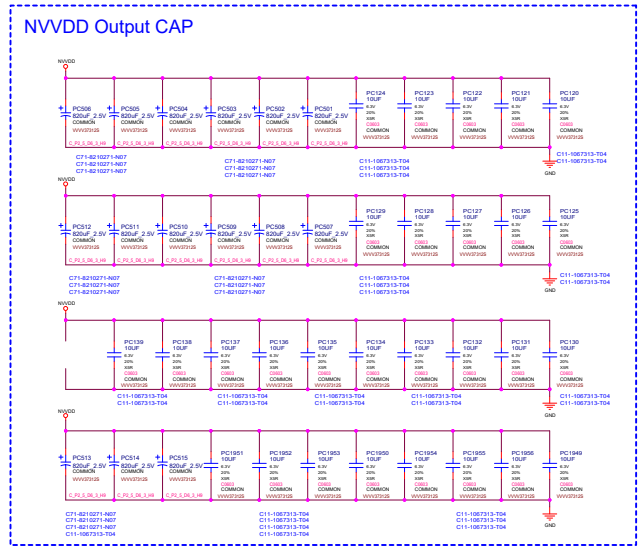
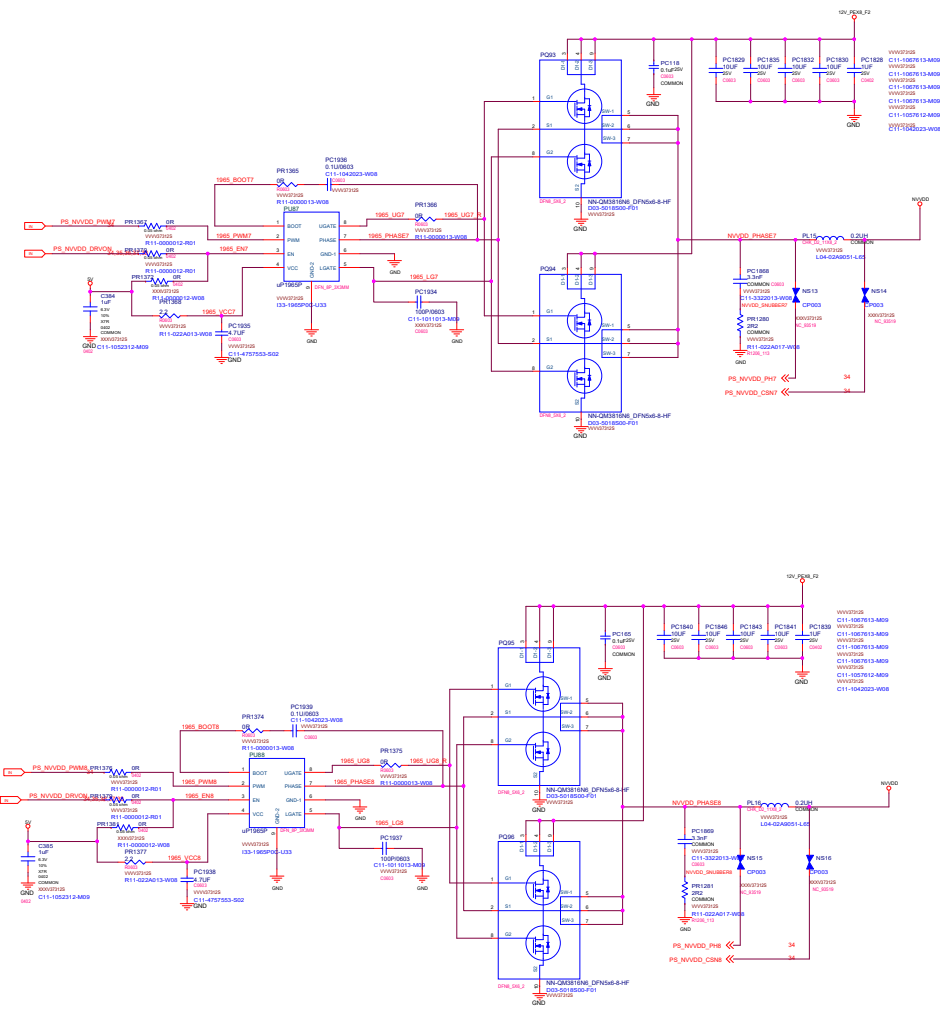


Backup





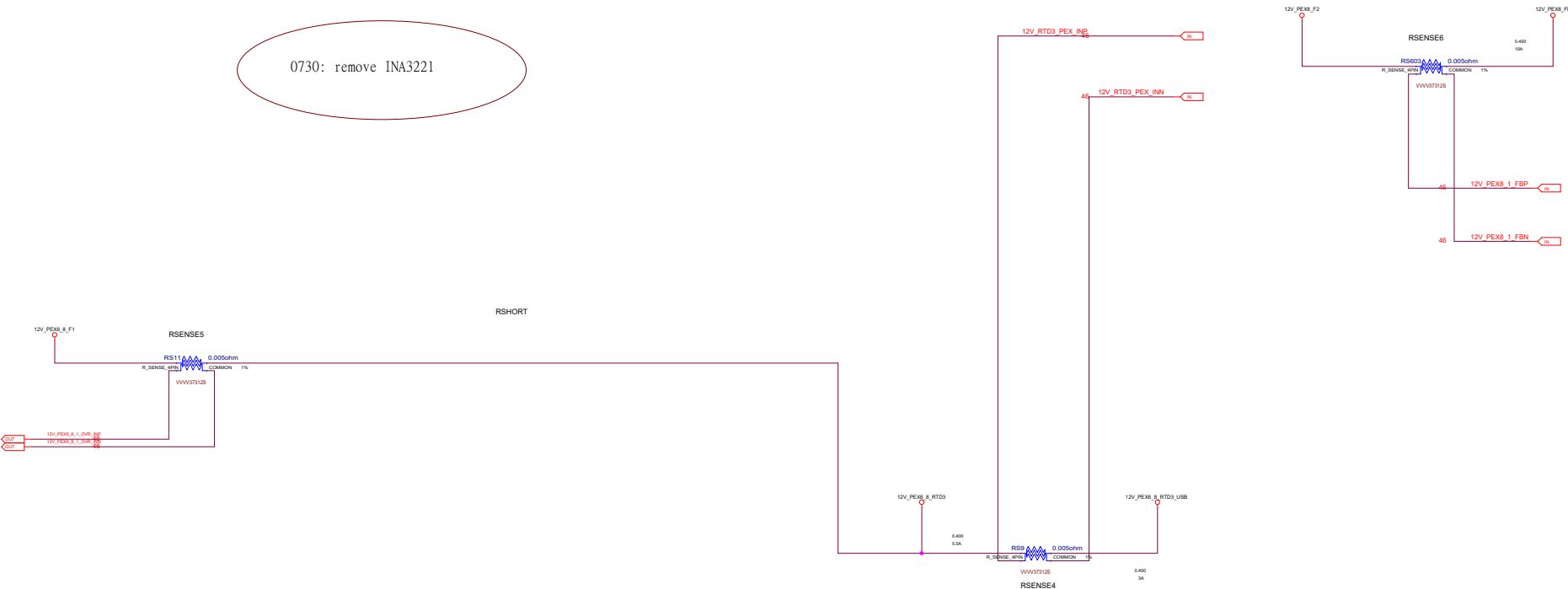


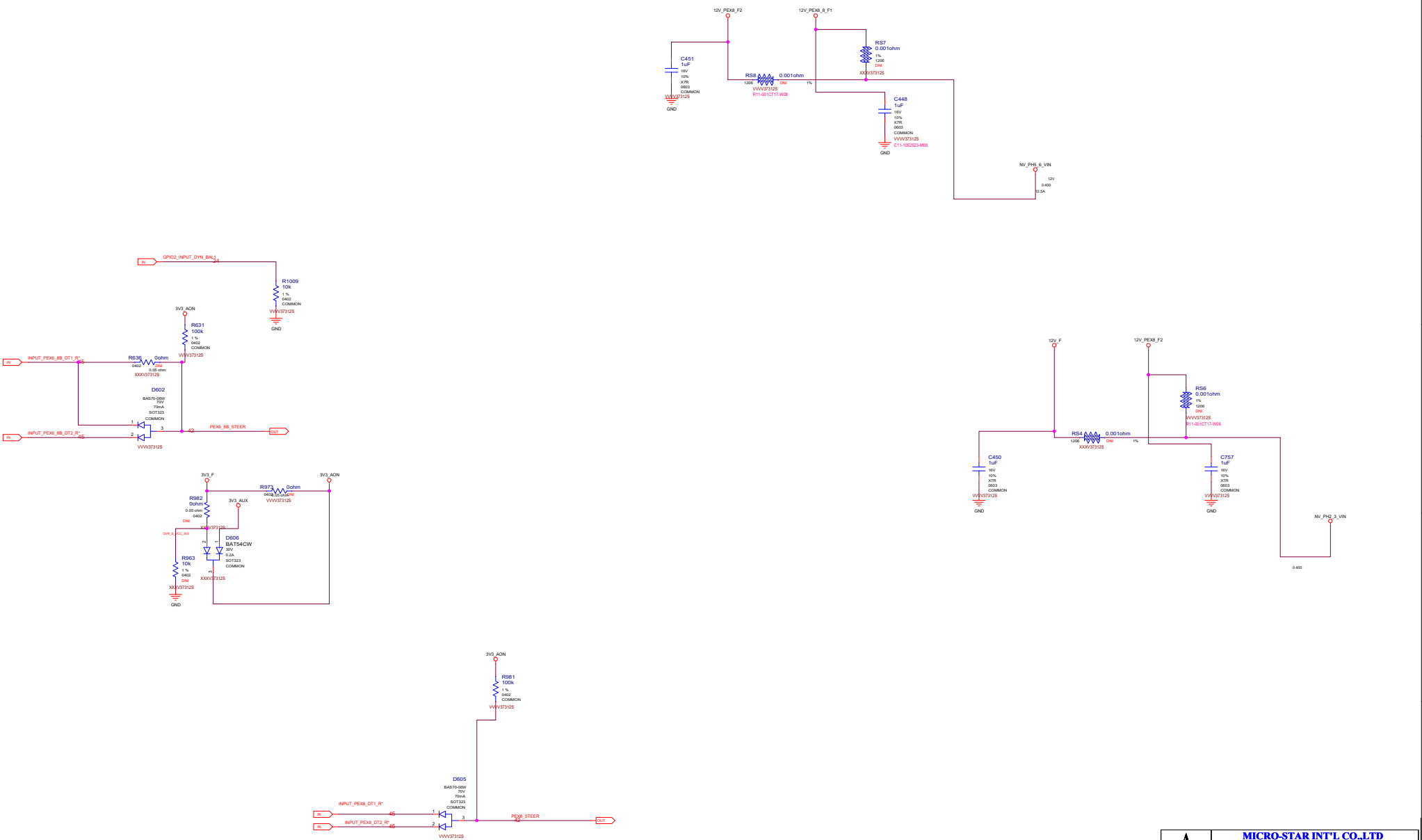


AND GATE LOGIC FOR P-BOARD			
GPI01	GPI029	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

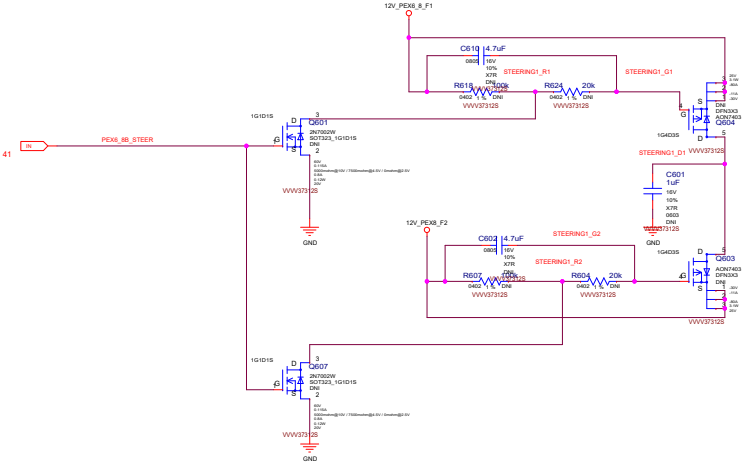
AND GATE LOGIC FOR P-BOARD			
GPI01	GPI029	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

0727: remove

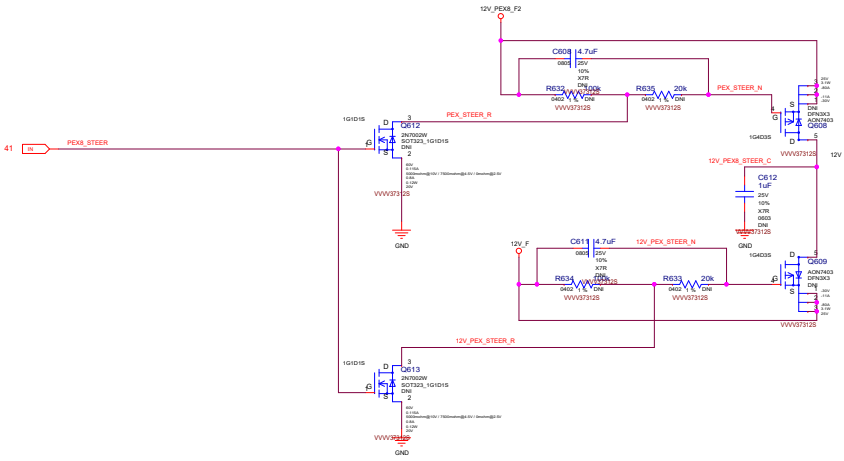




12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



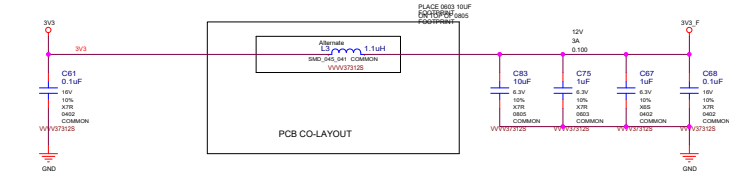


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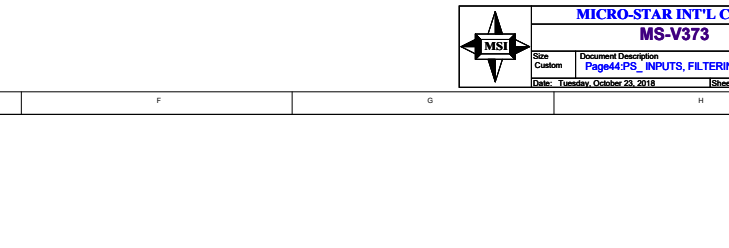
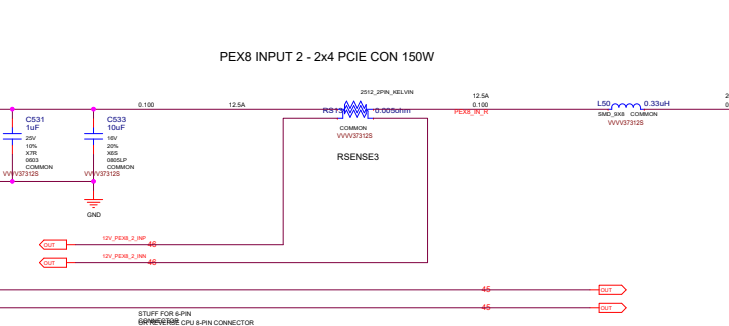
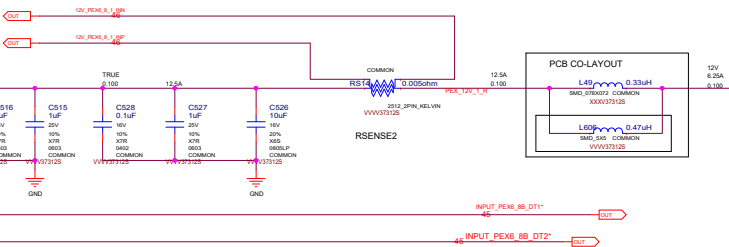
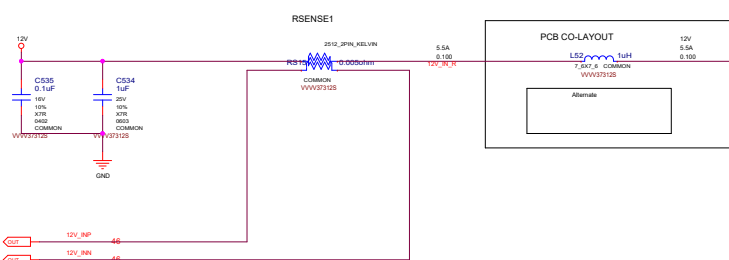
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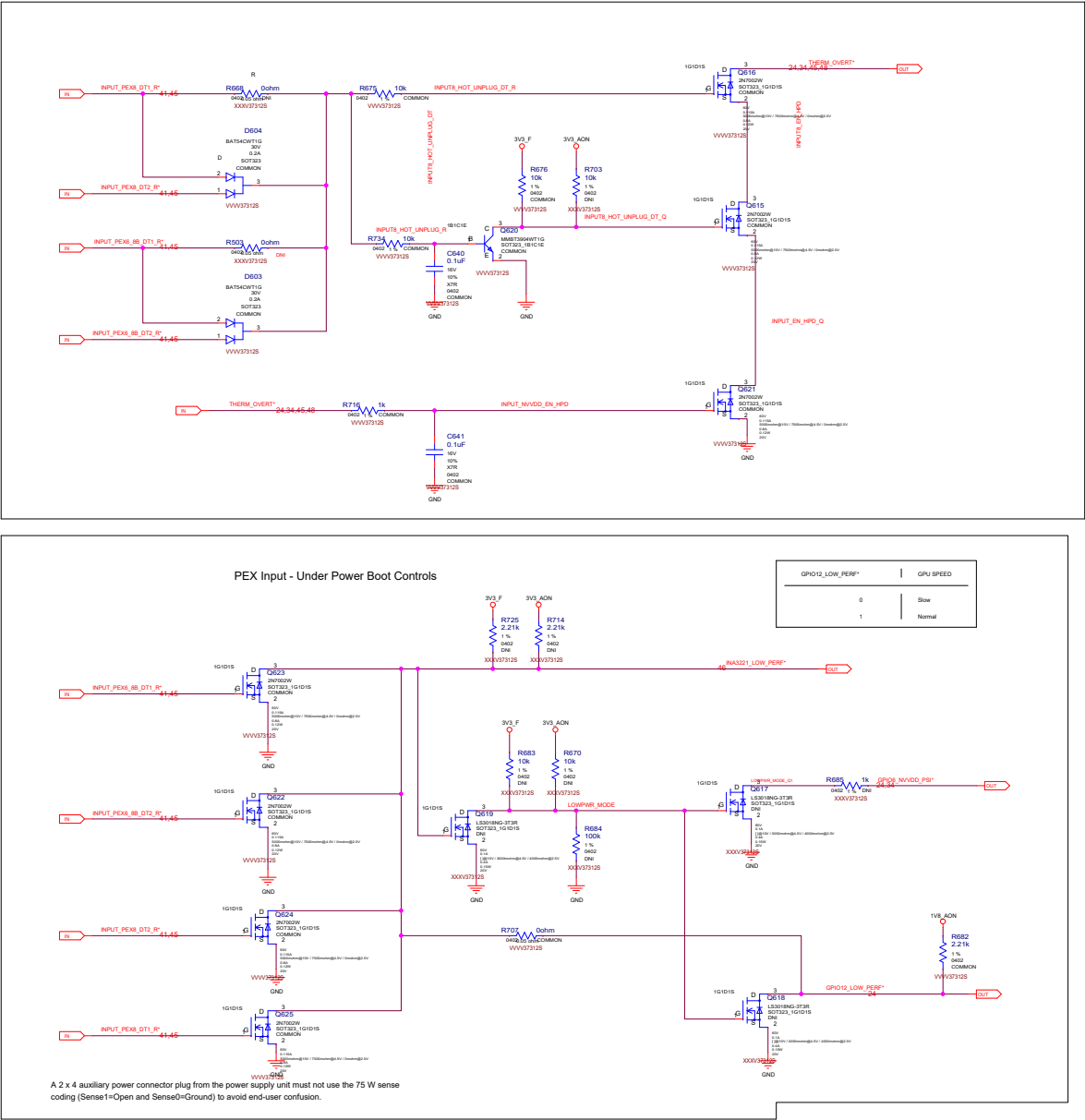
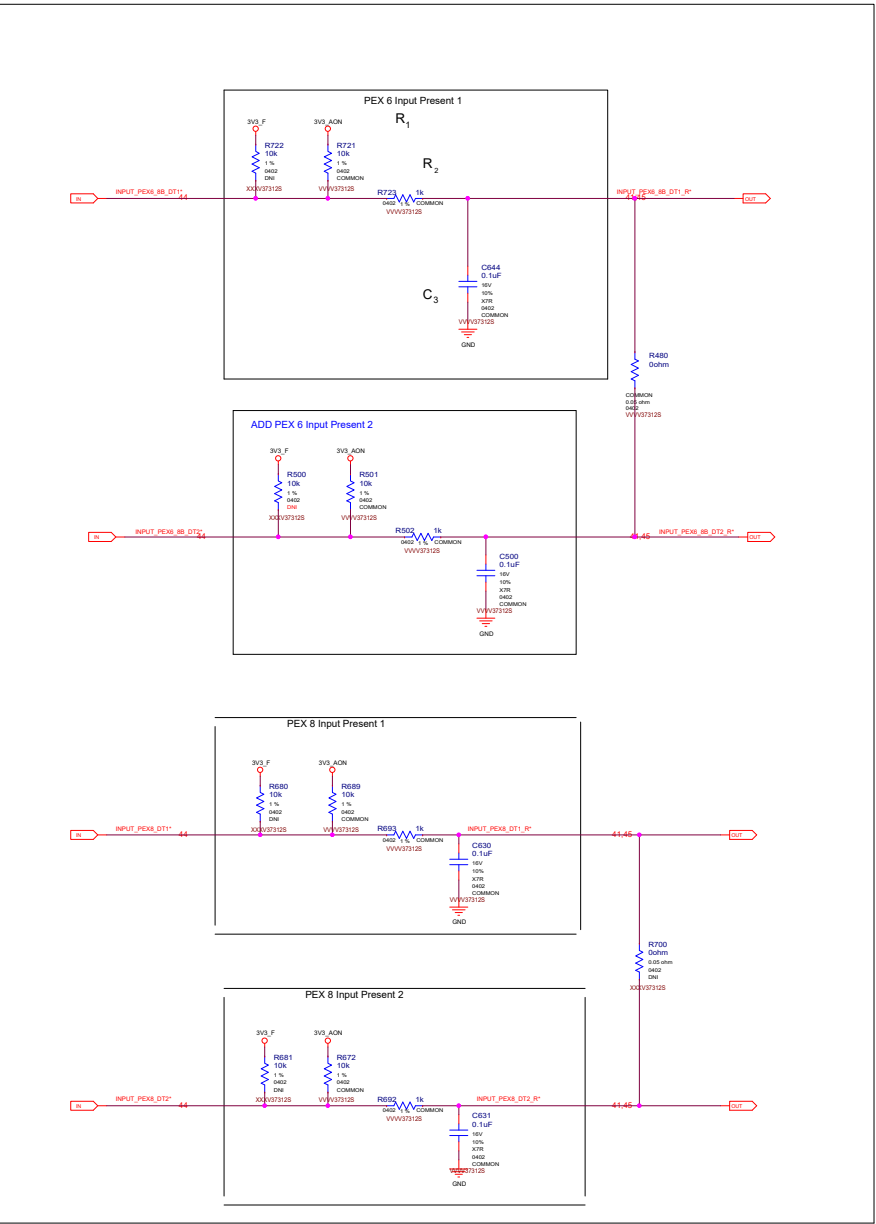
PEX6 INPUT 1 - 2x3 PCIE CON 75W

PEX 3V3 INPUT - 10W

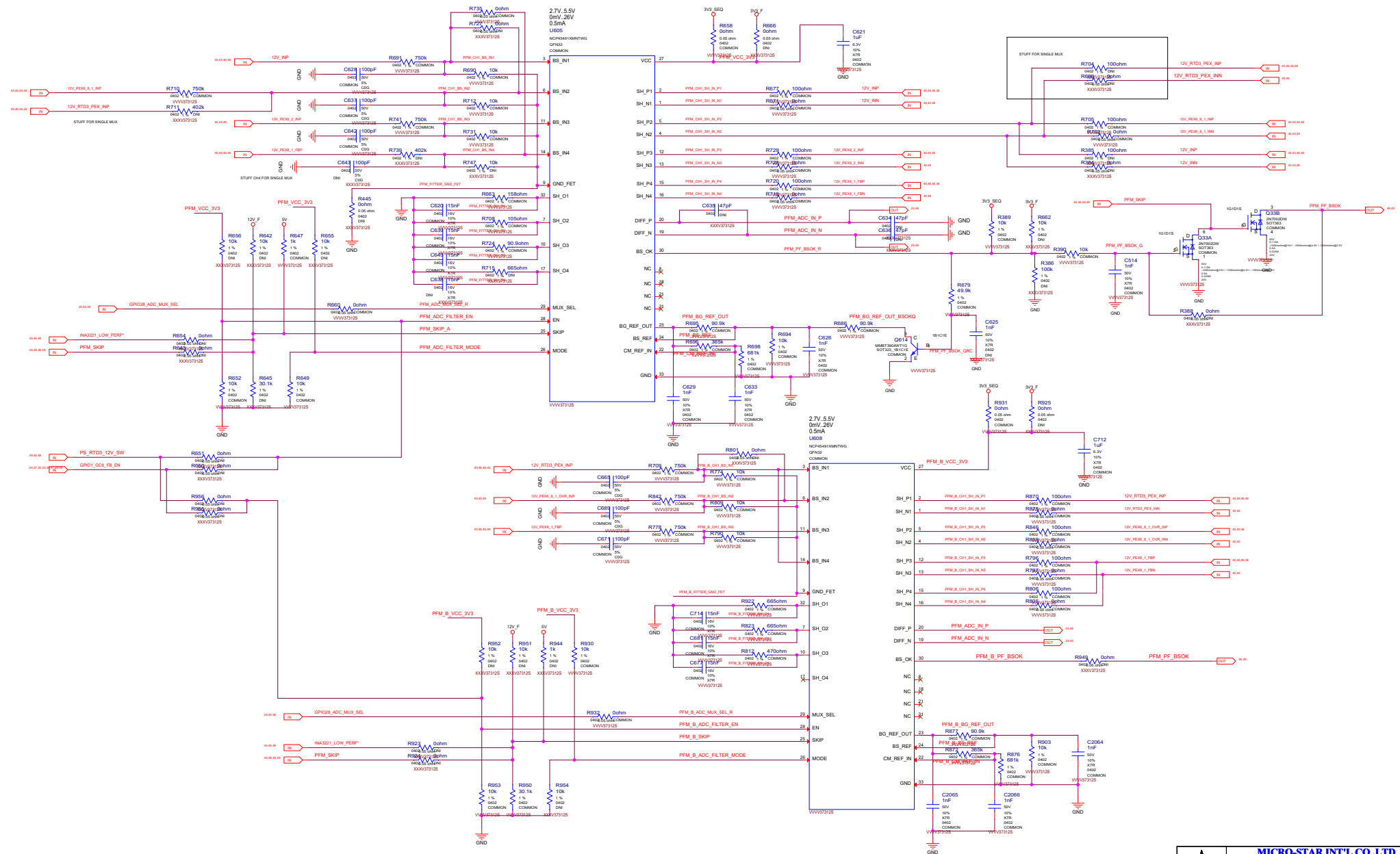


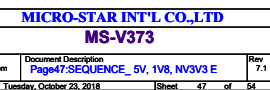
PEX_12V INPUT - 66W

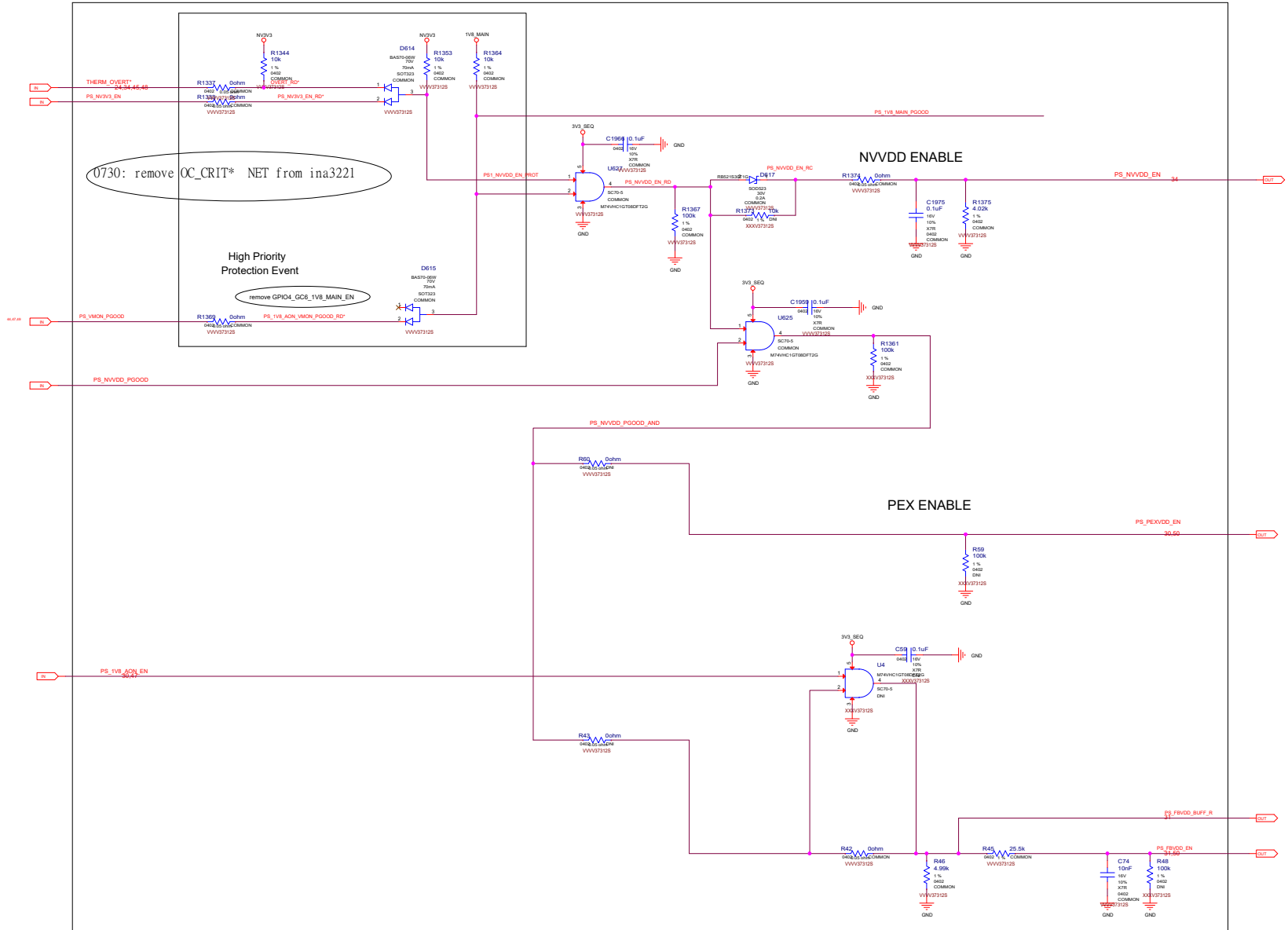


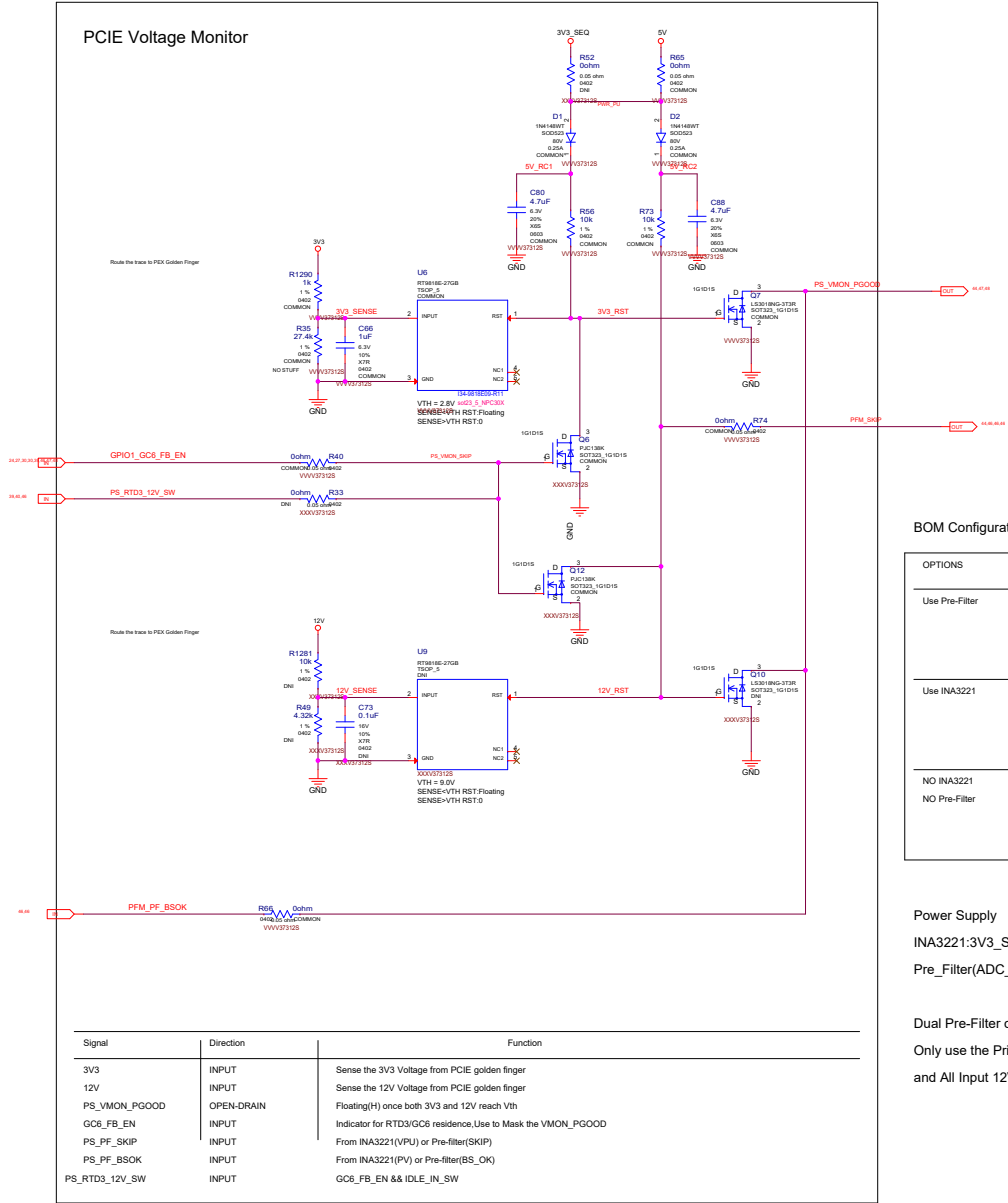


STUFF IF USING 2XMUX





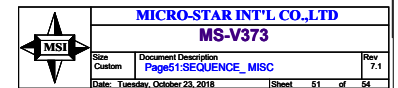
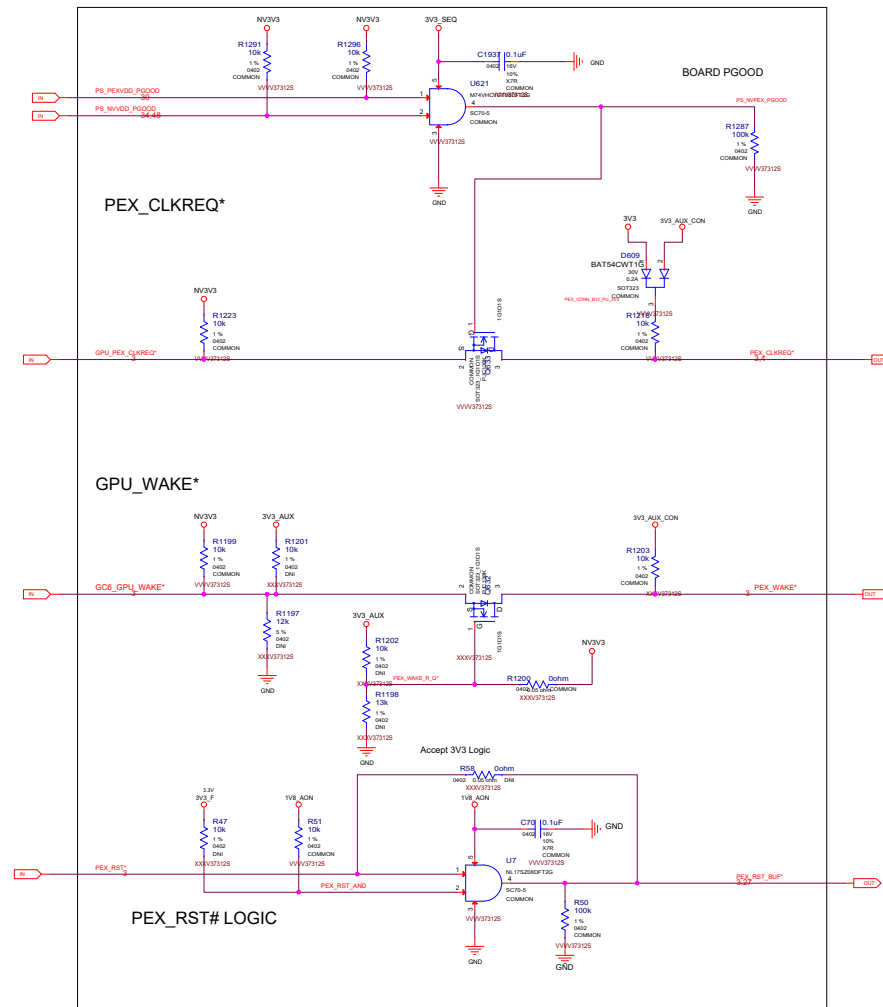


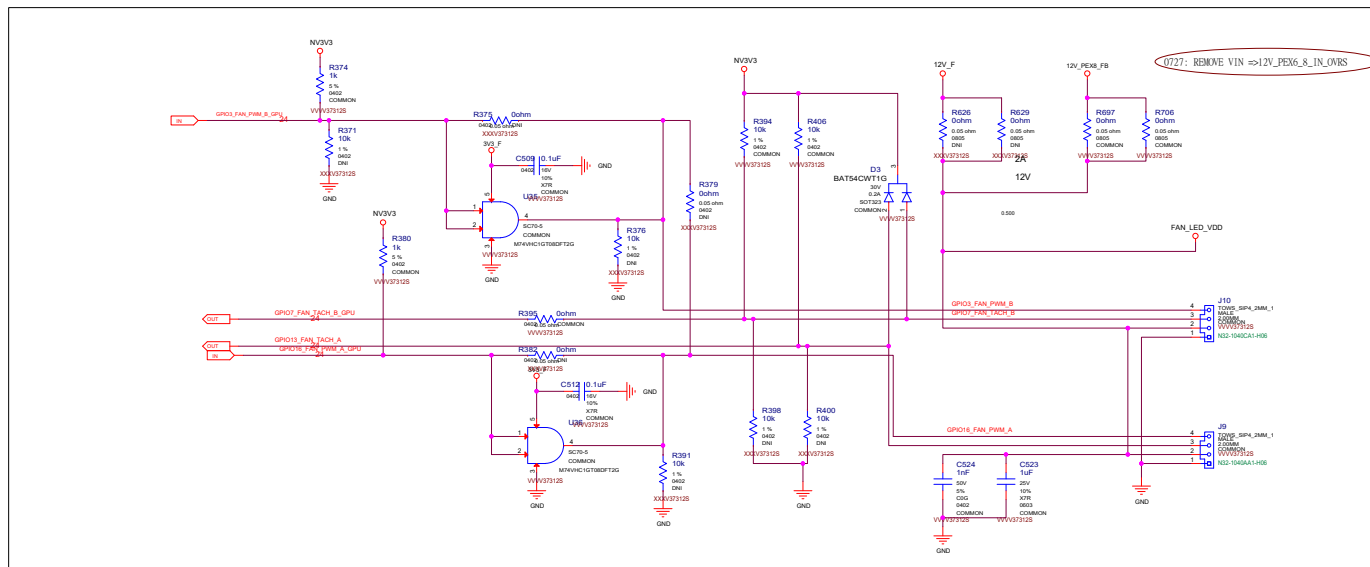


31.48

31.48

30.48



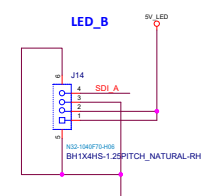
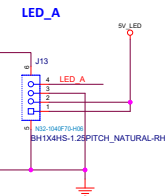
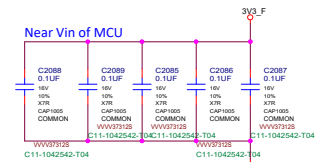
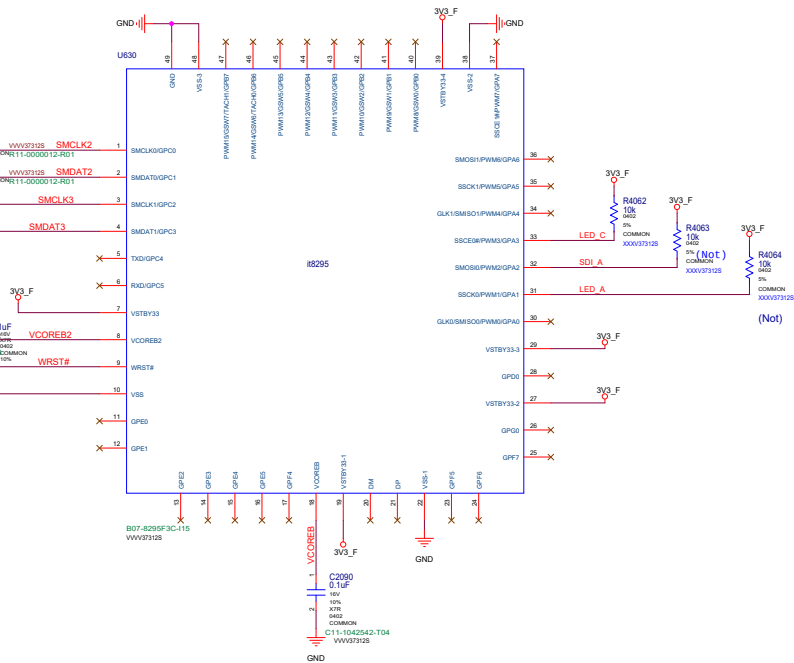
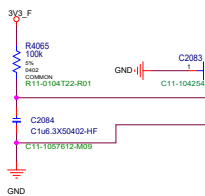
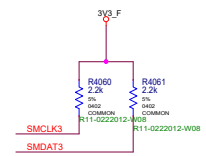
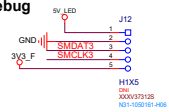


LED BOOST

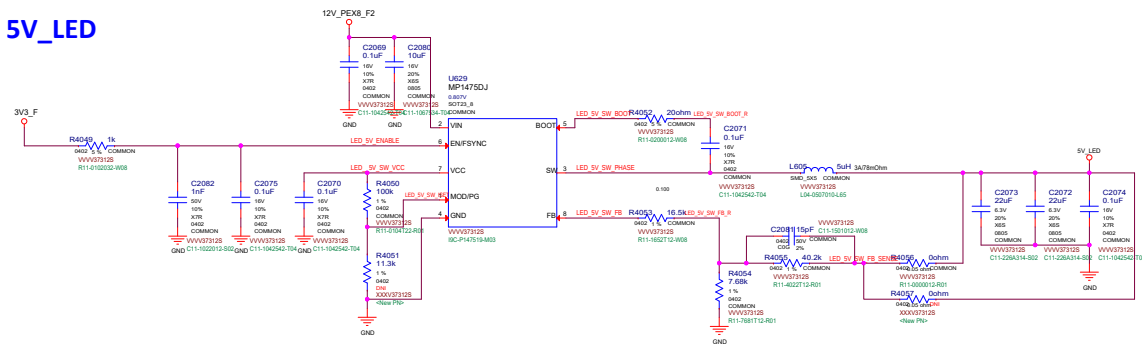
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	MS-V373		
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Firmware Programming

Debug



5V_LED

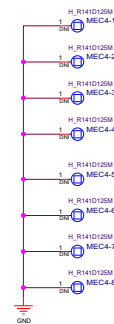
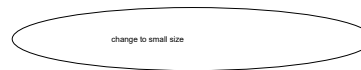
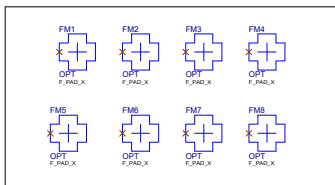
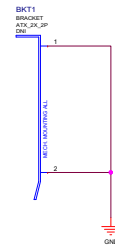




Screw



Brackets:



STIFFENER

Mechanical Holes Symbol

