

PG160-B02

8GB GDDR6, 256b, X16

Tall DVI-D + USBC/DP + DP + HDMI/DP + DP

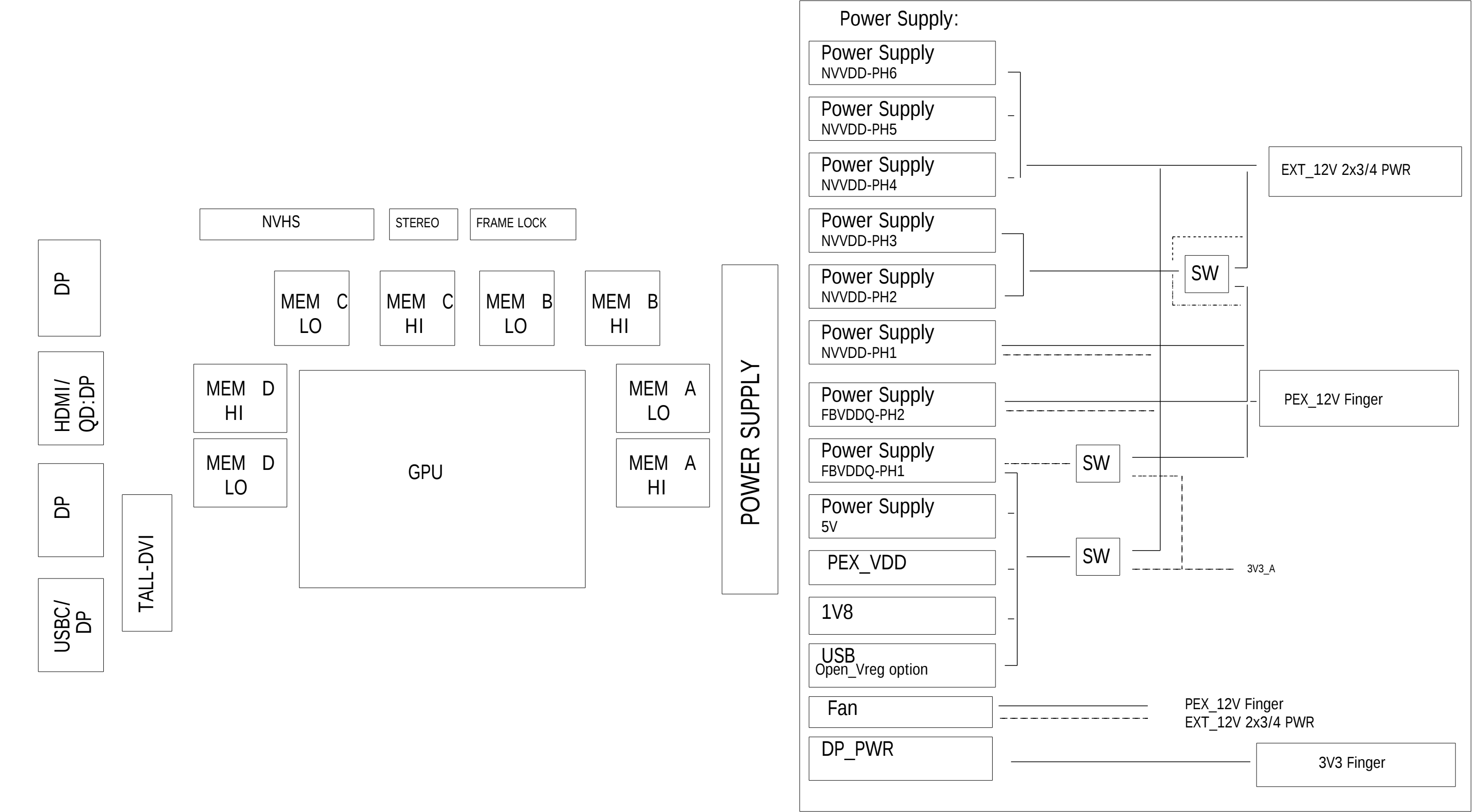
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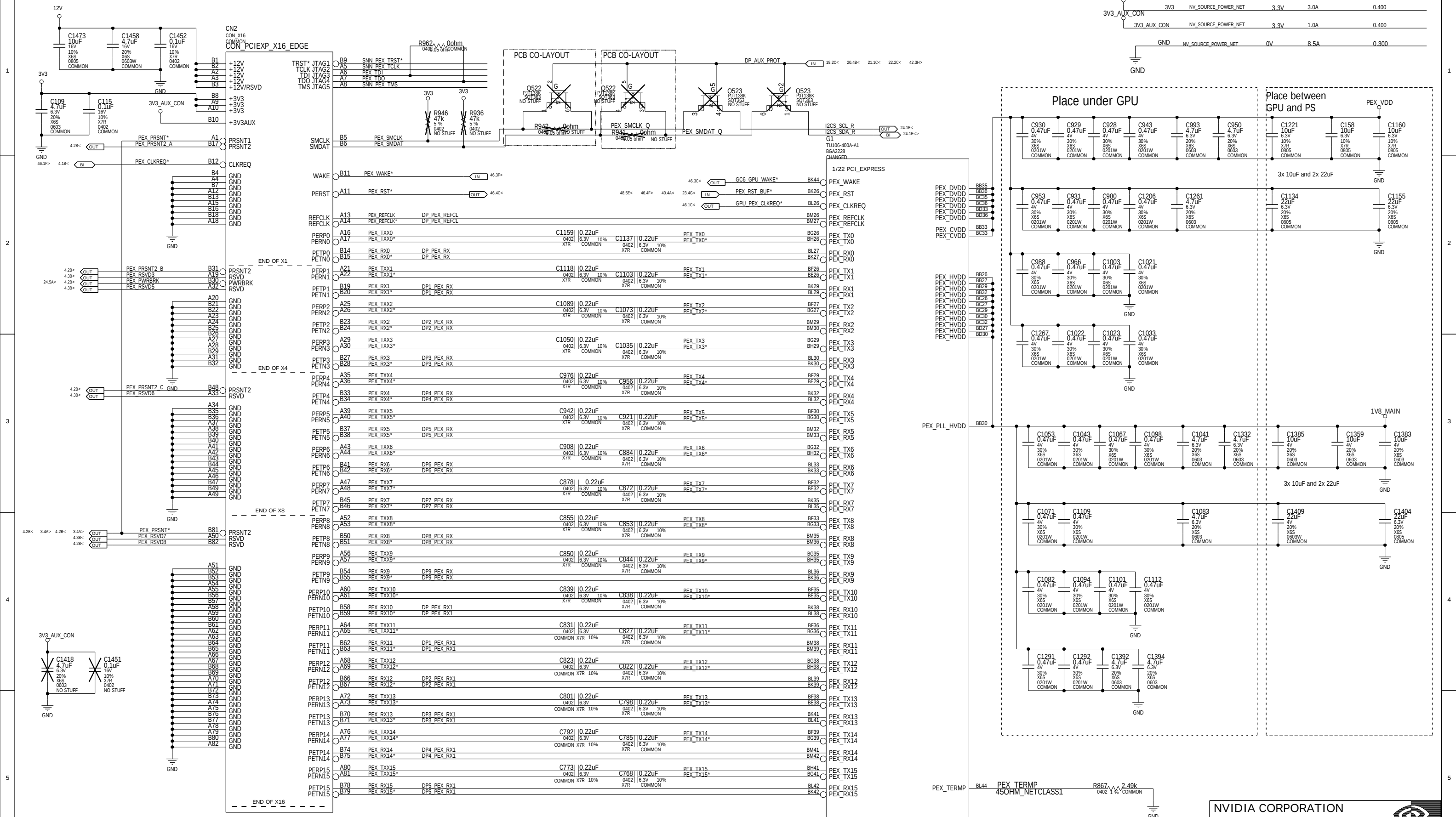
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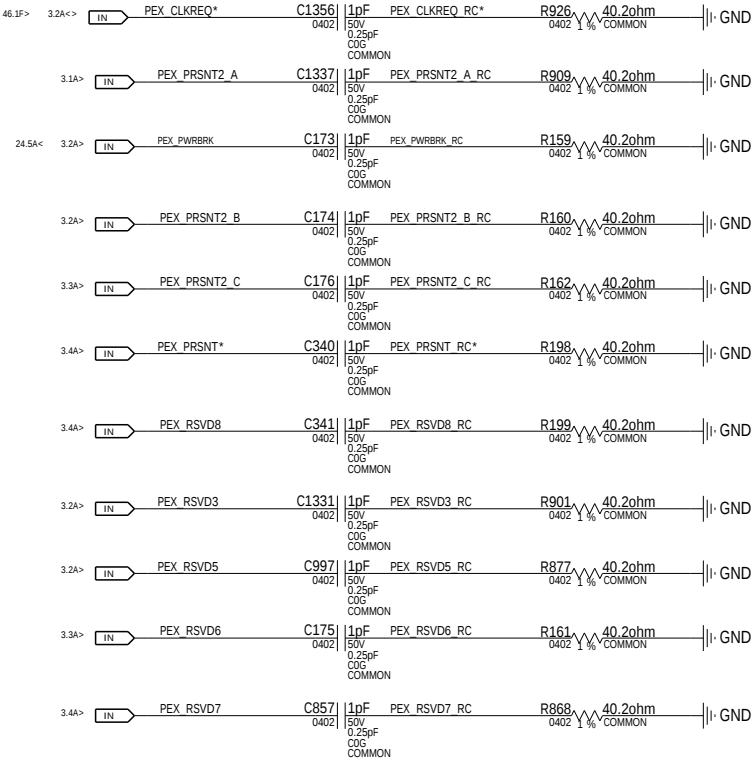
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Page3: PCI Express

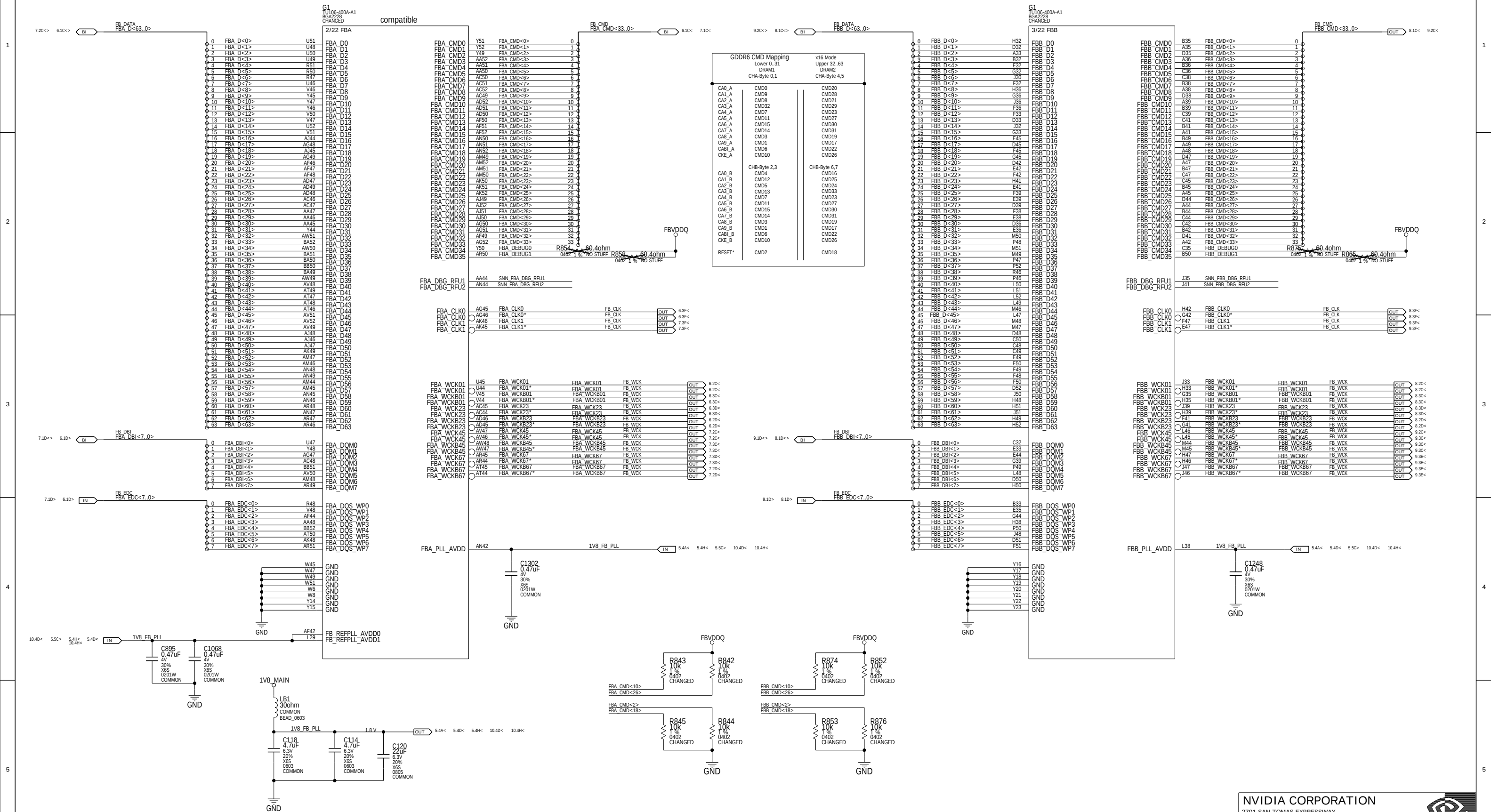


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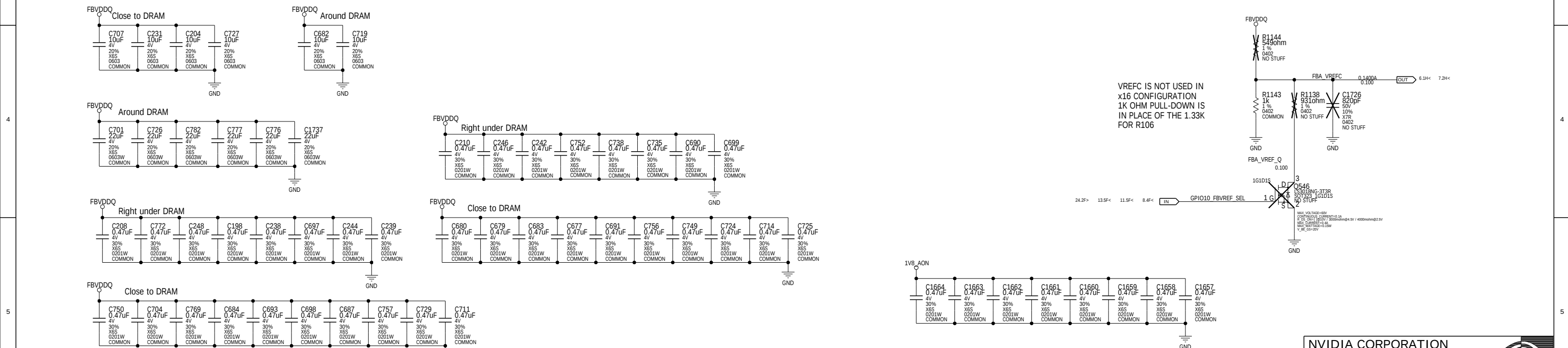
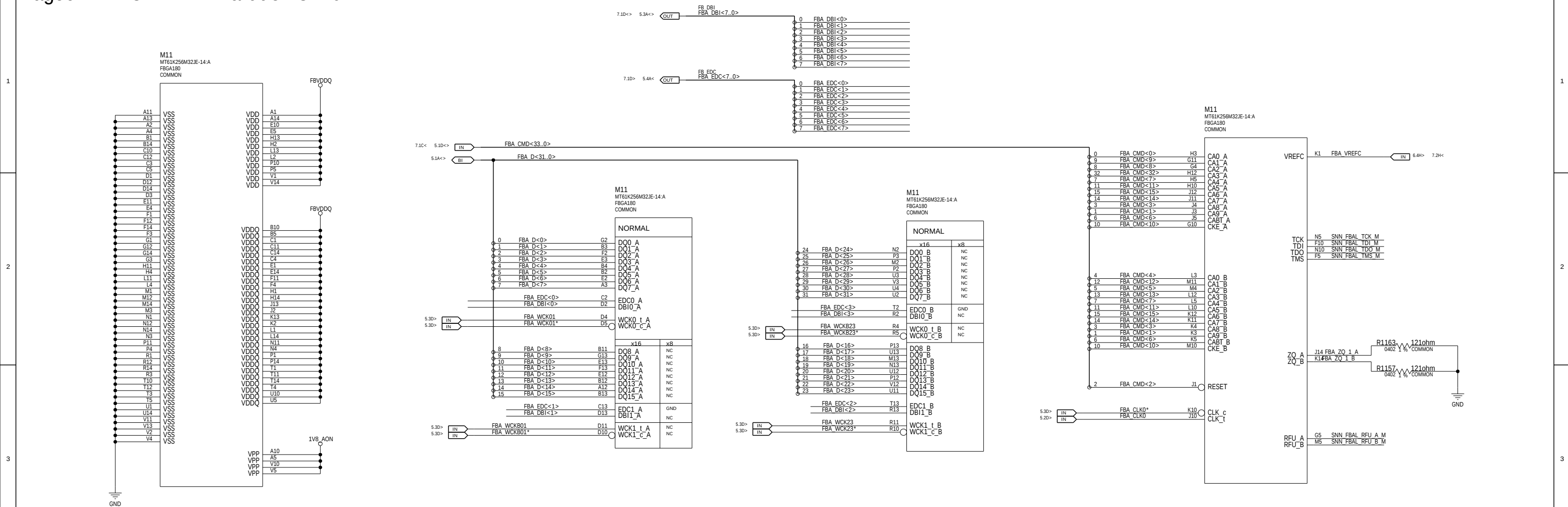


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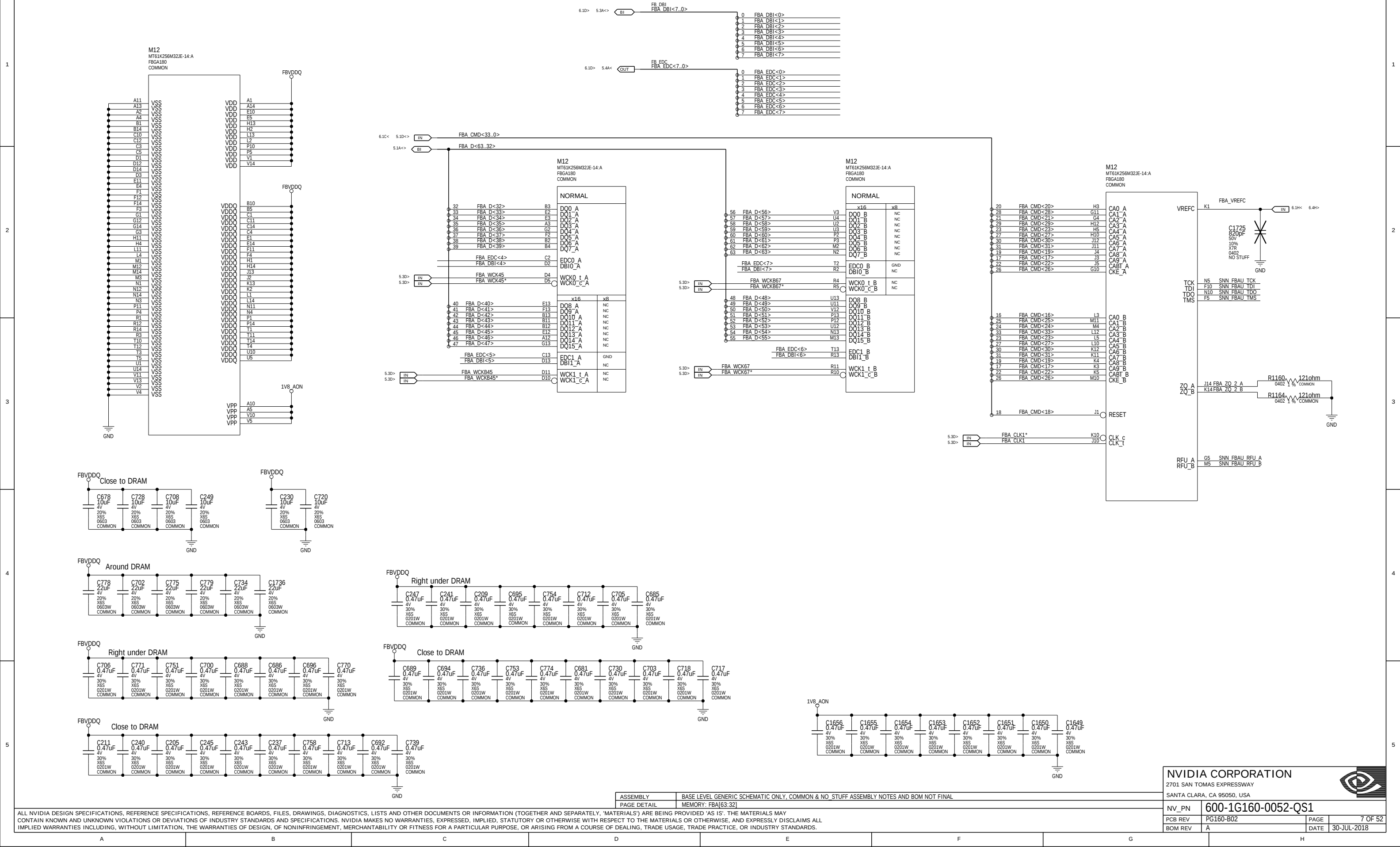
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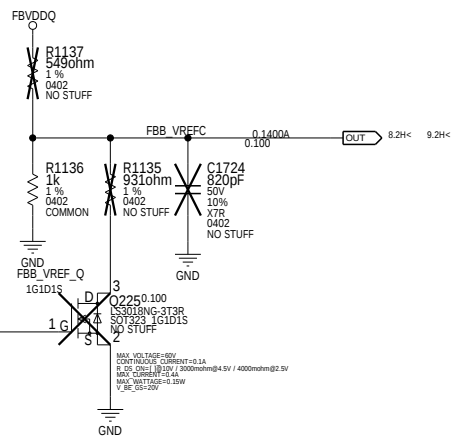
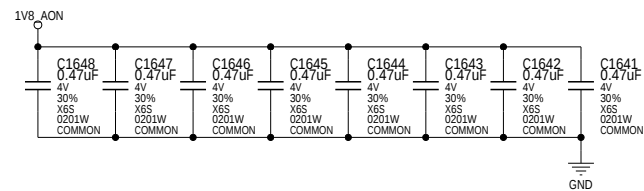
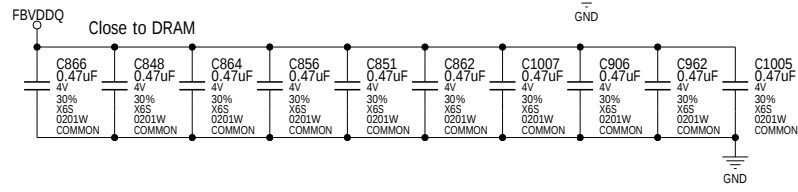
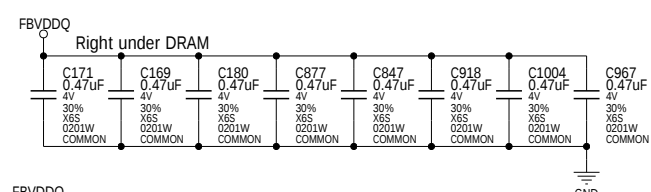
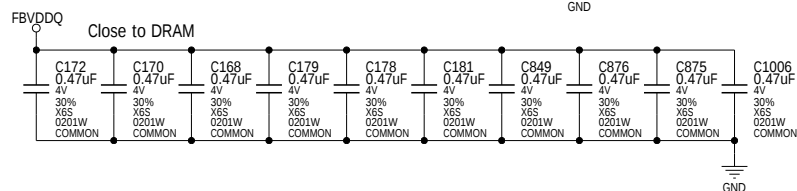
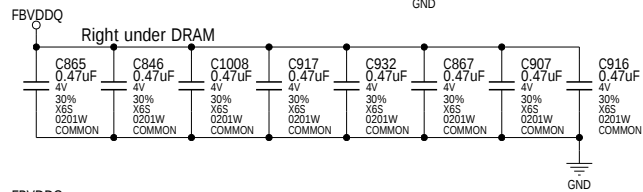
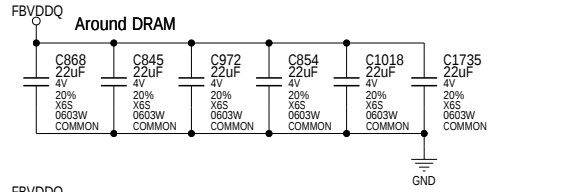
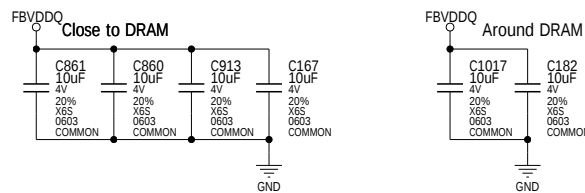
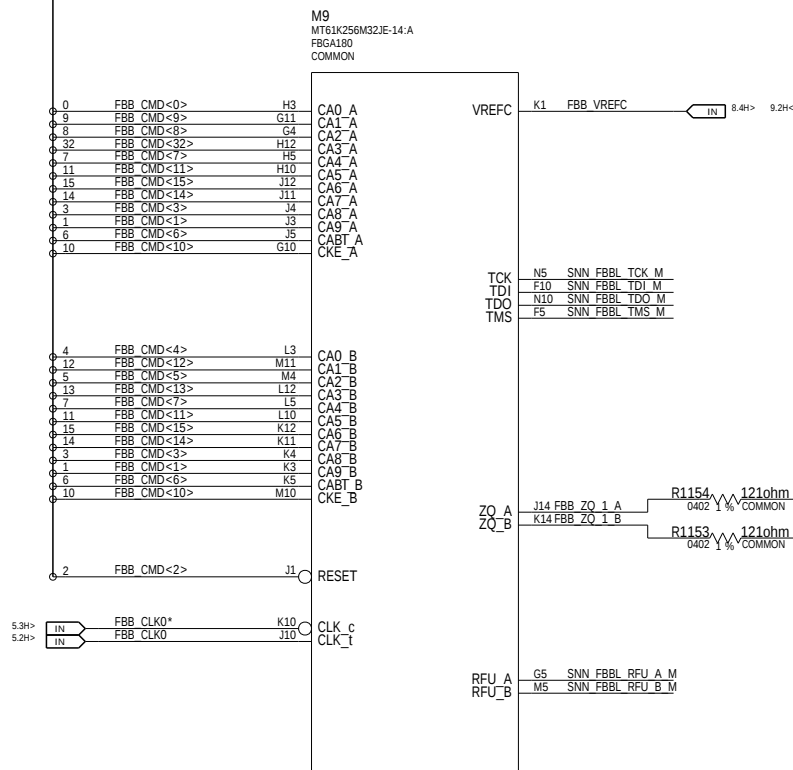
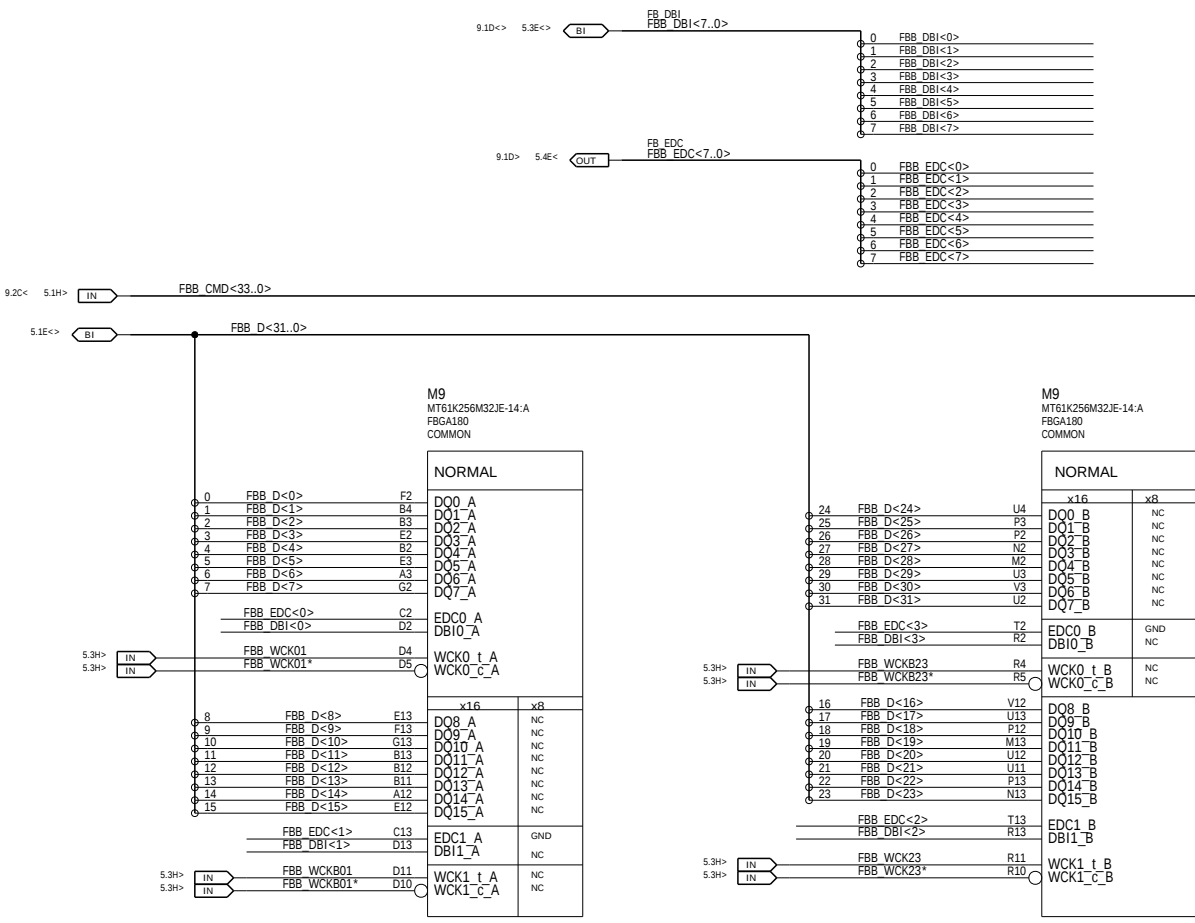
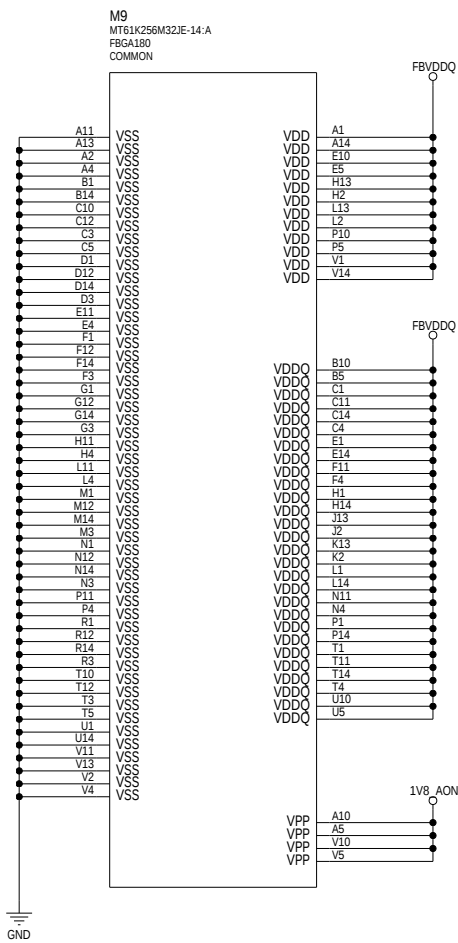
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Page8: MEMORY: FBB Partition 31..0



VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R104

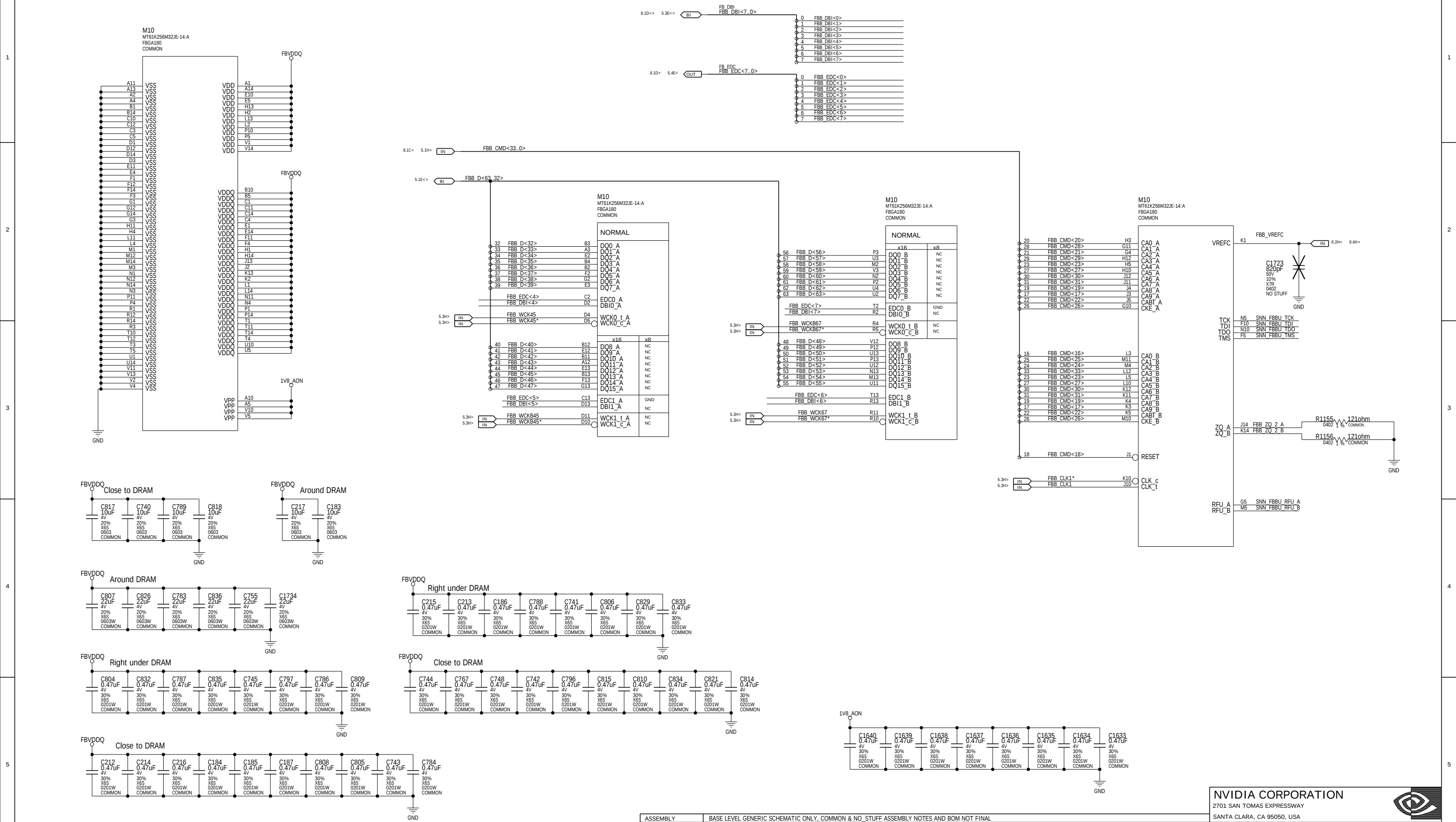
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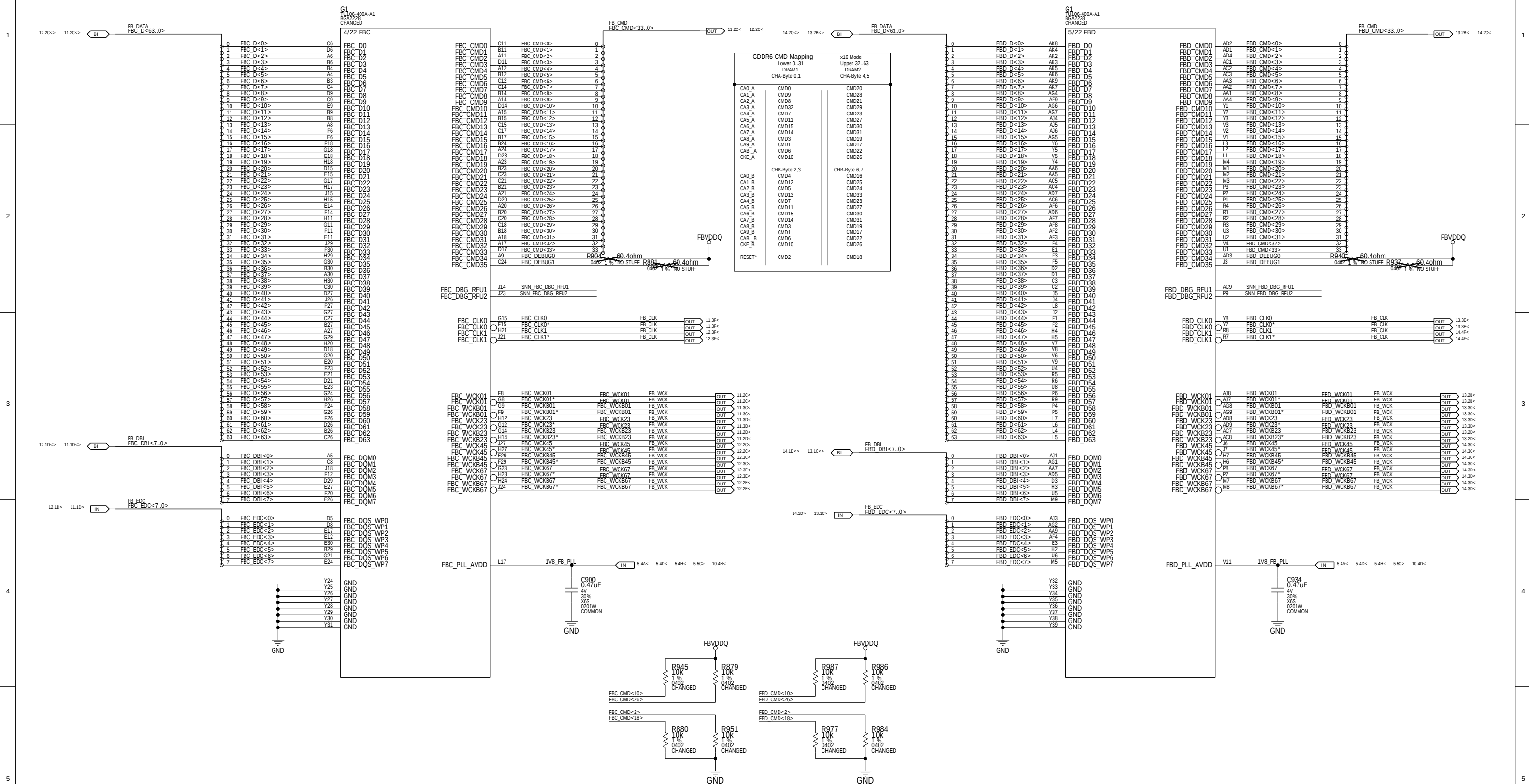
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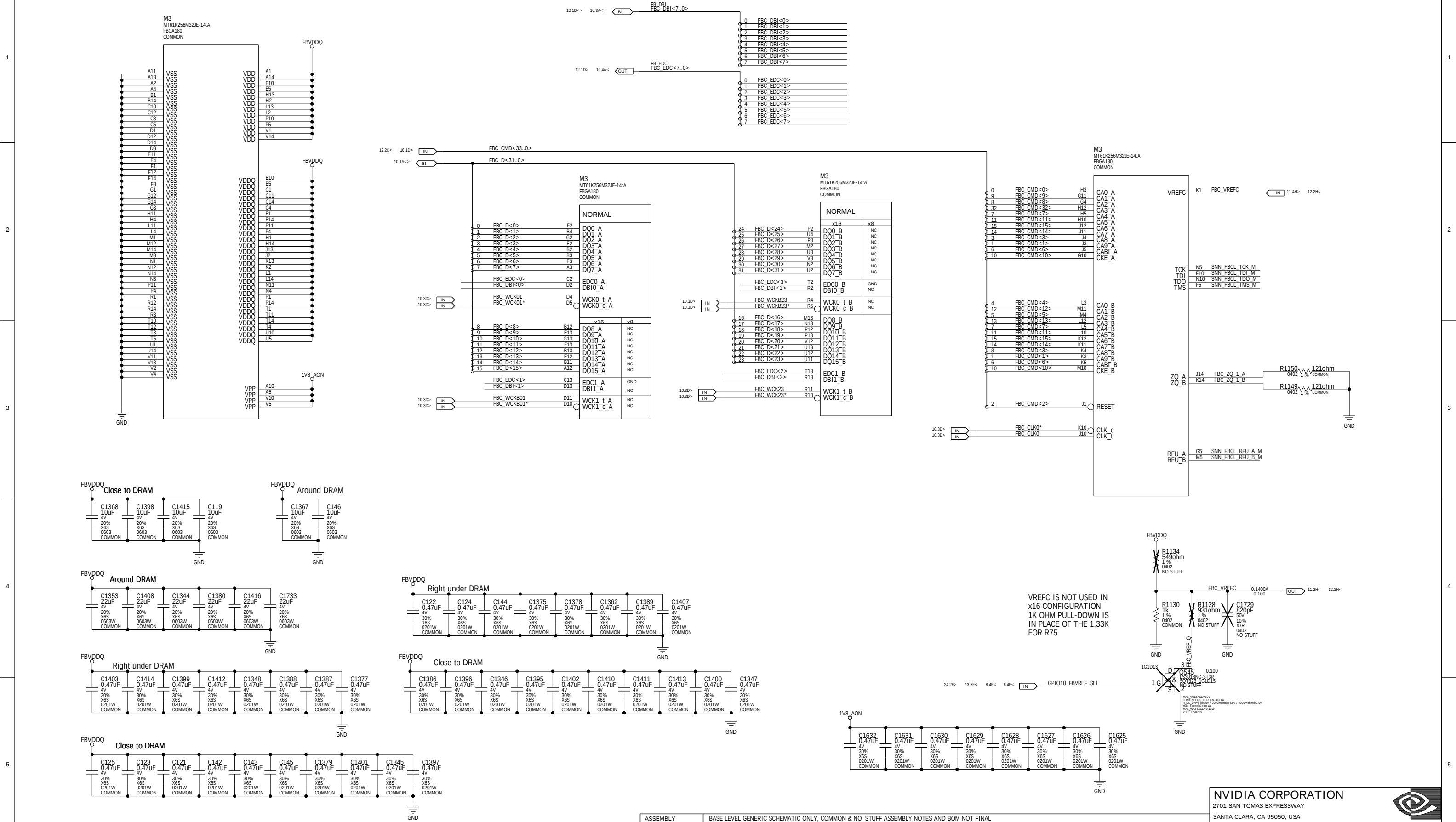


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Page10: MEMORY: GPU Partition C/D

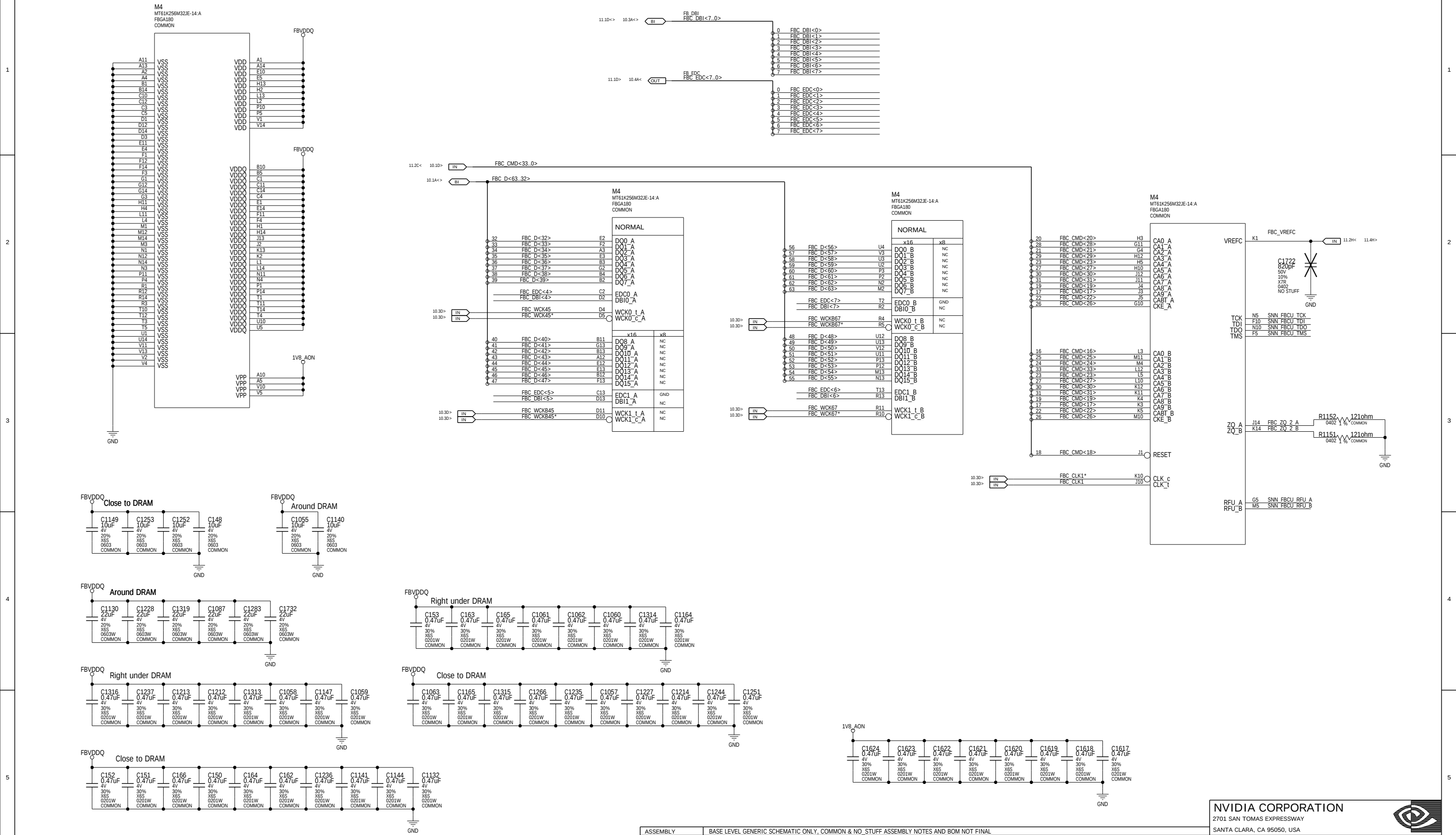


Page11: MEMORY: FBC Partition 31..0



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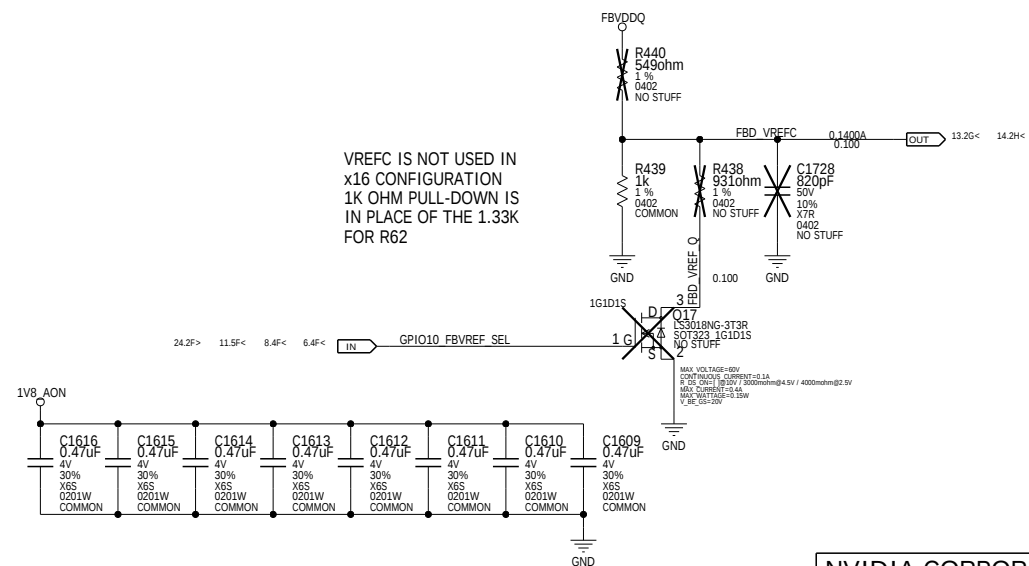
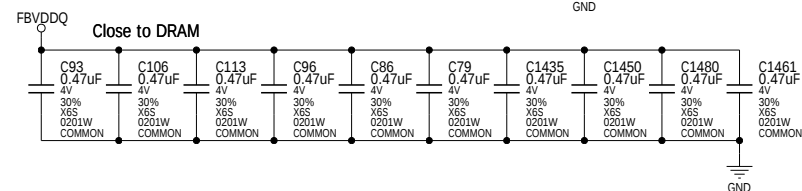
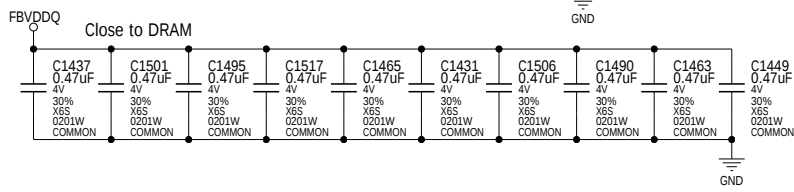
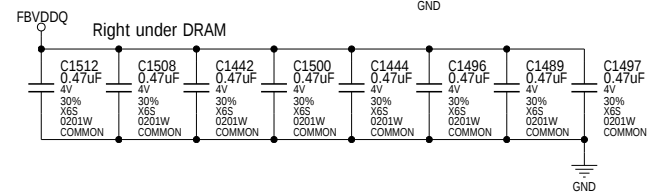
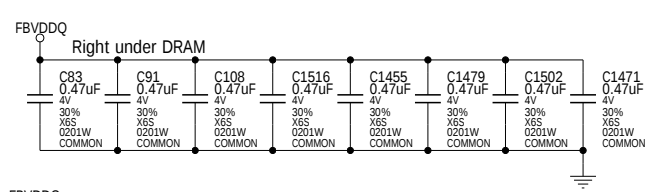
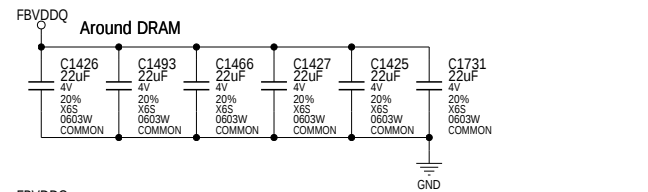
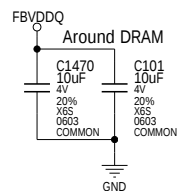
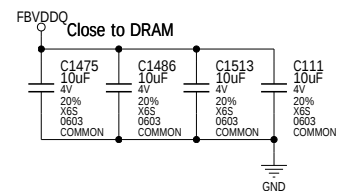
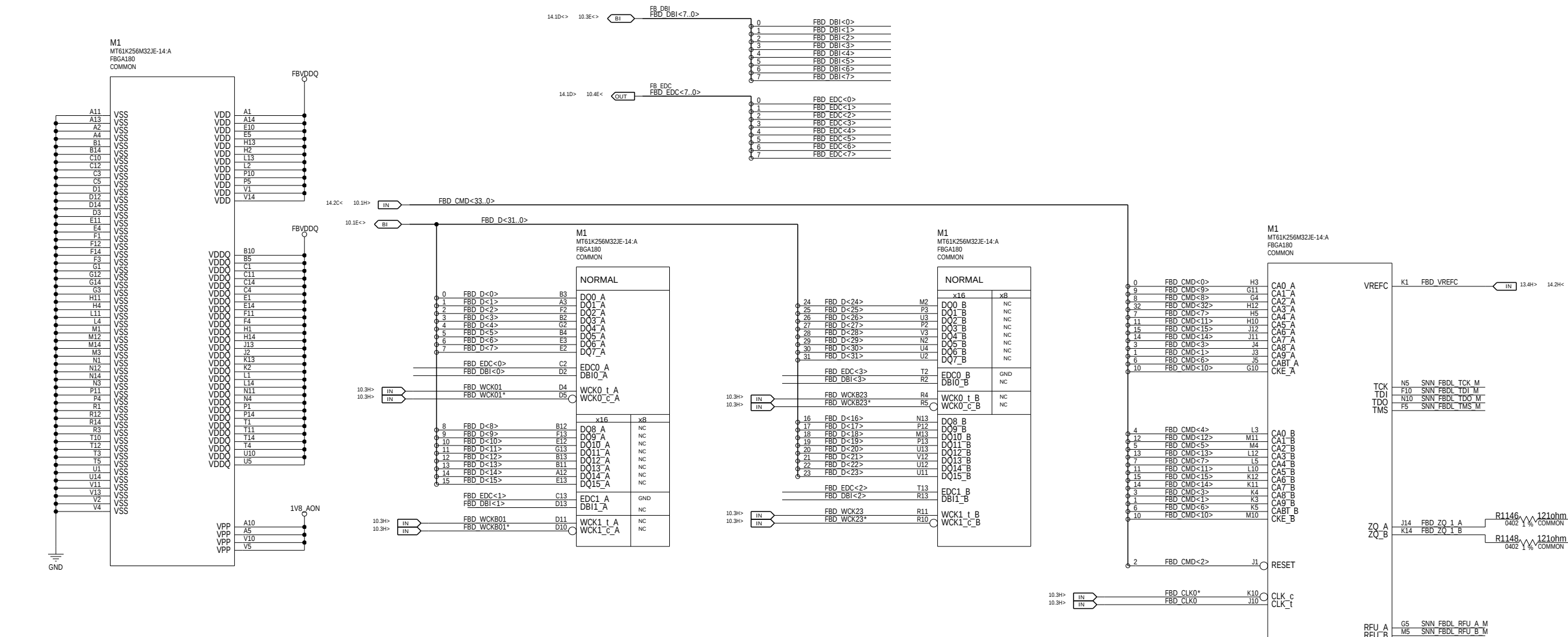
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PAGE DETAIL	MEMORY: FBC[63:32]

Page13: MEMORY: FBD Partition 31..0



VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R62

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
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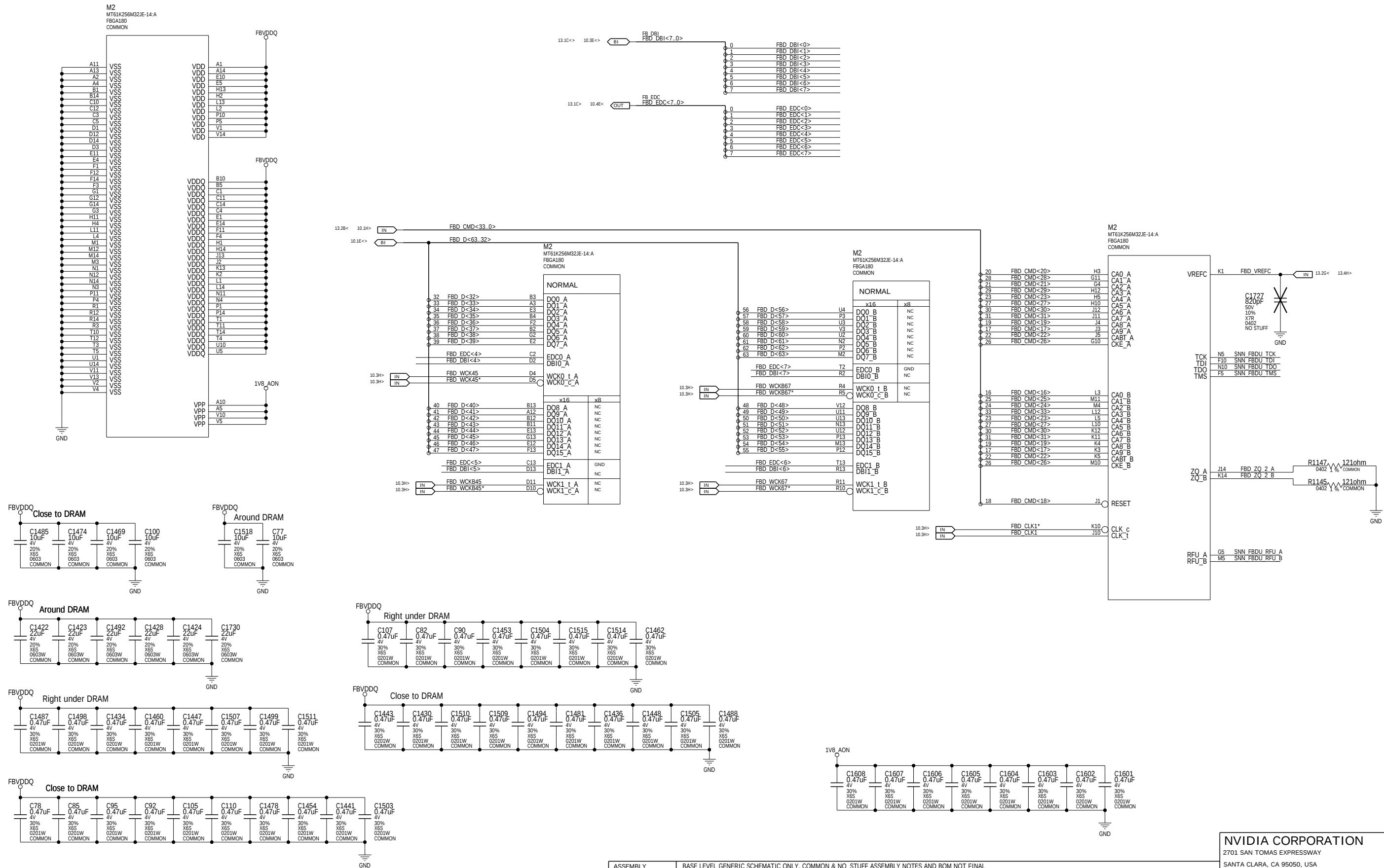
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Page14: MEMORY: FBD Partition 63..32

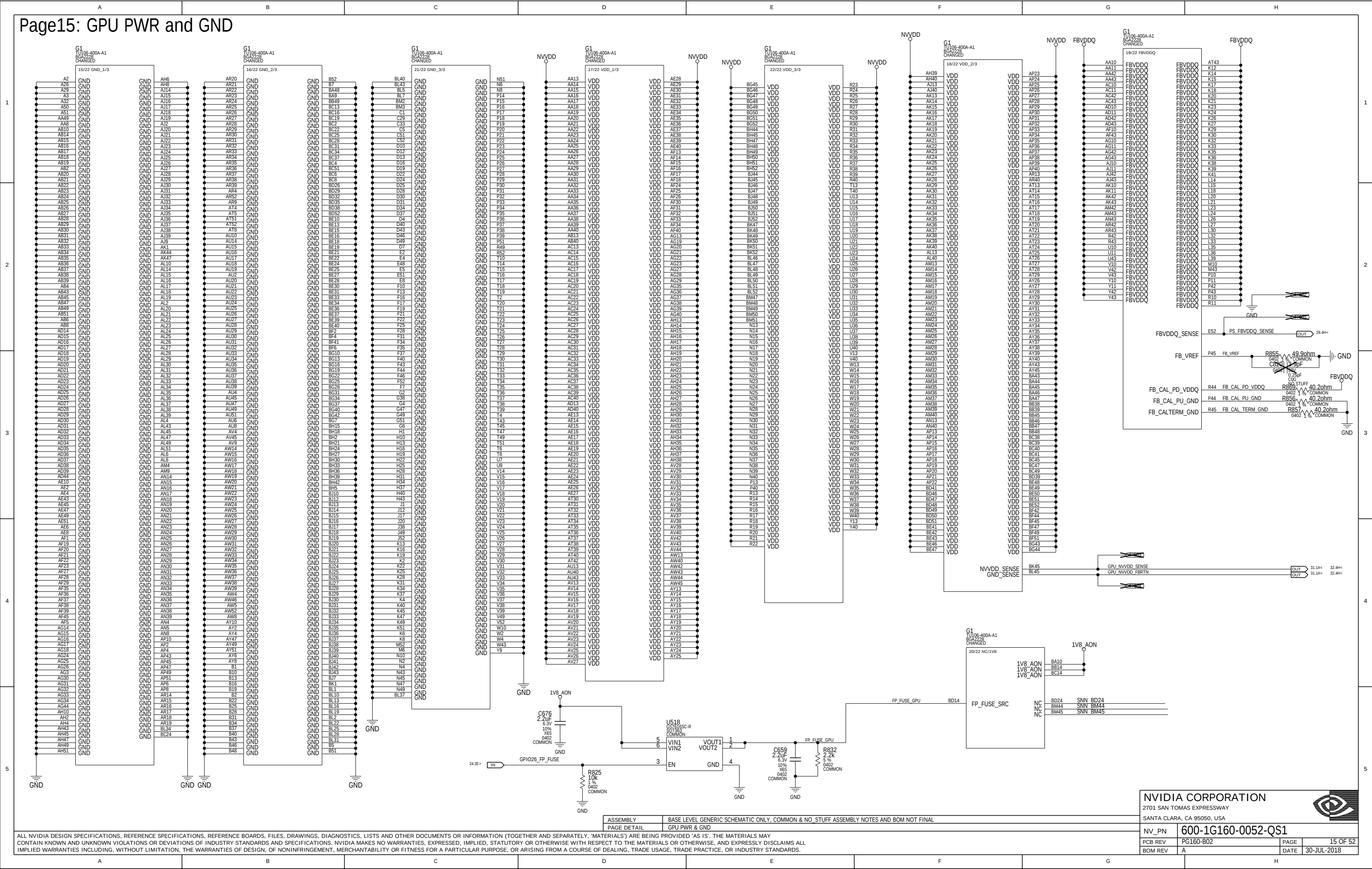


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PAGE DETAIL	MEMORY: FBD[63:32]

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Page15: GPU PWR and GND



Page16: GPU Decoupling 1

FBVDDQ

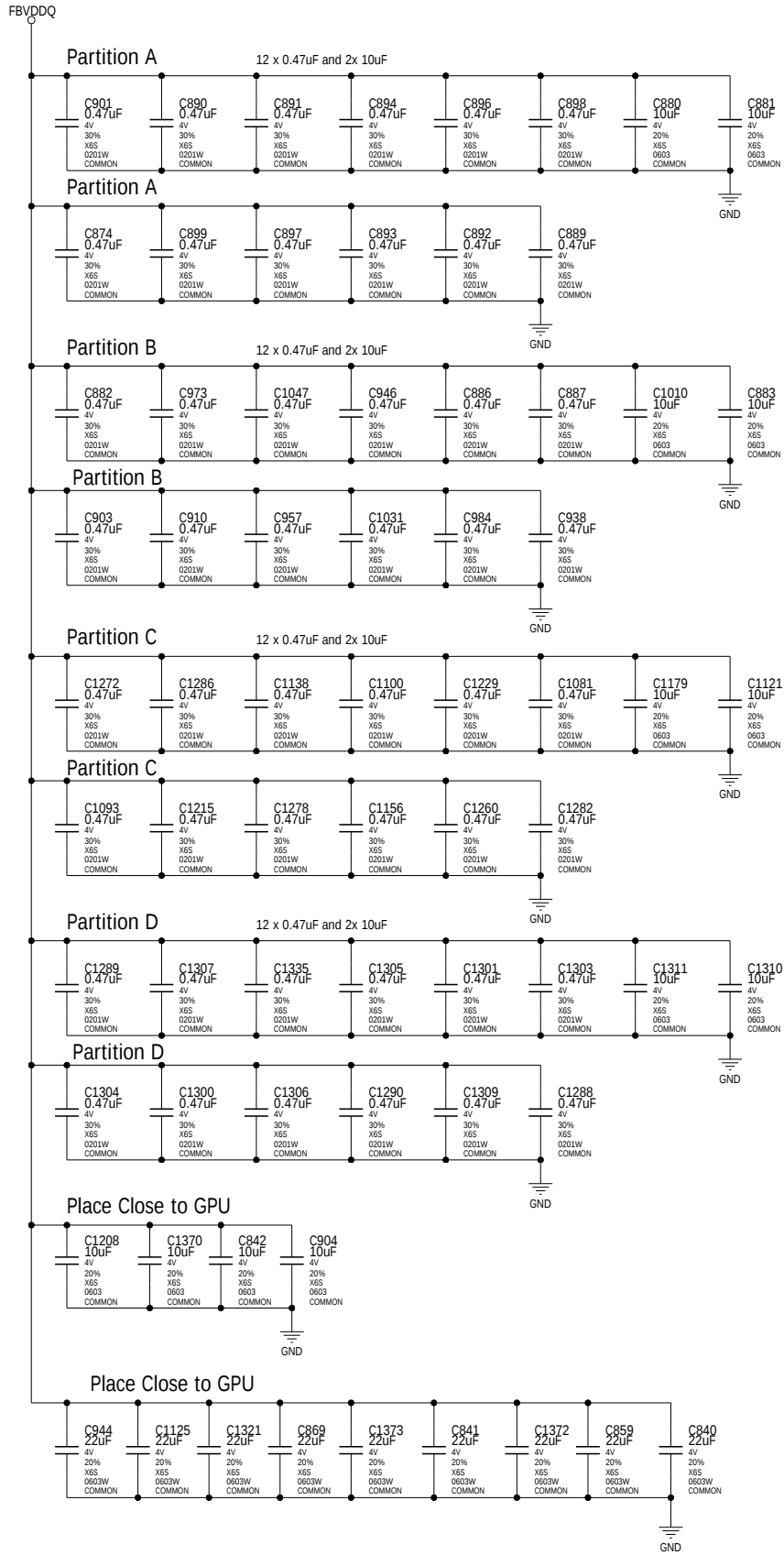
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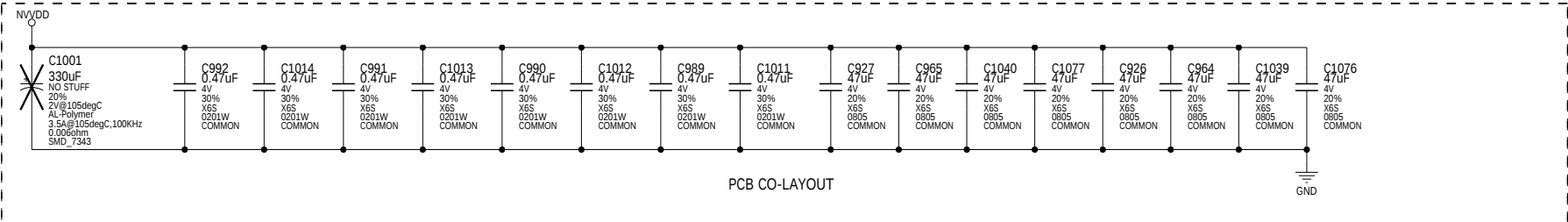
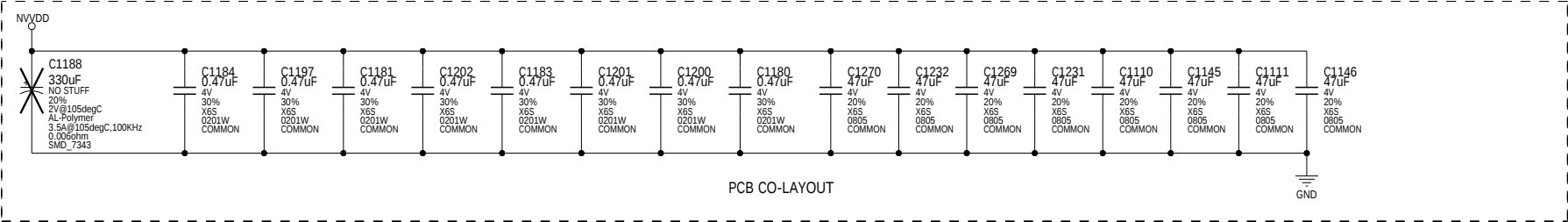
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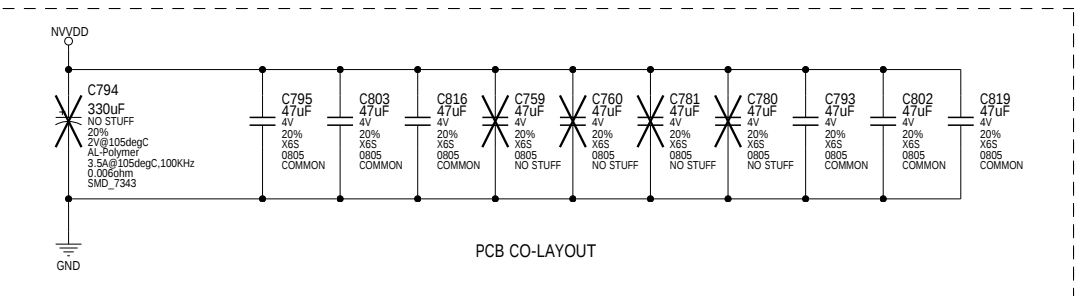
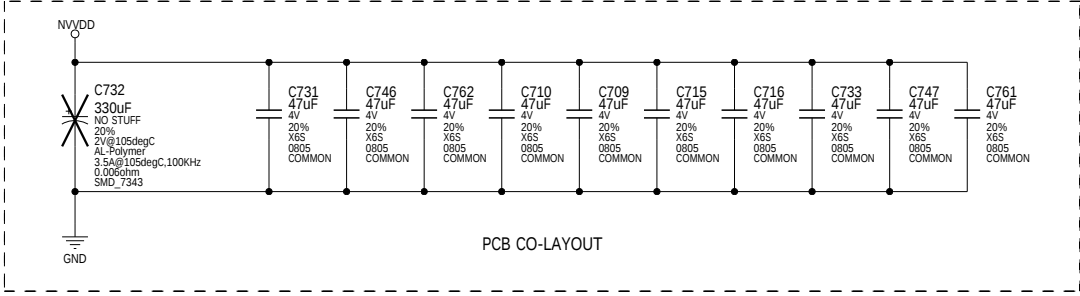
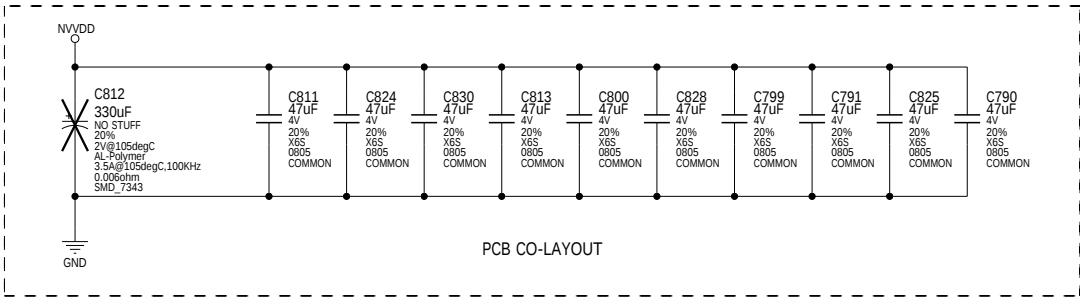
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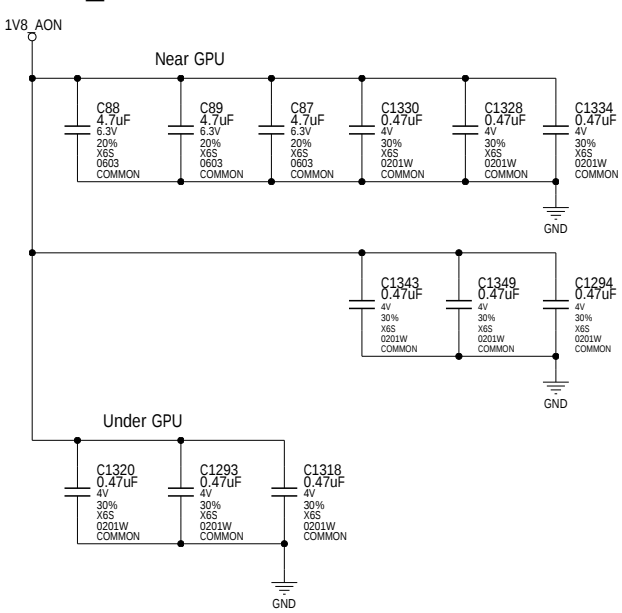
Under GPU



Near GPU



1V8_AON



1

2

3

4

5

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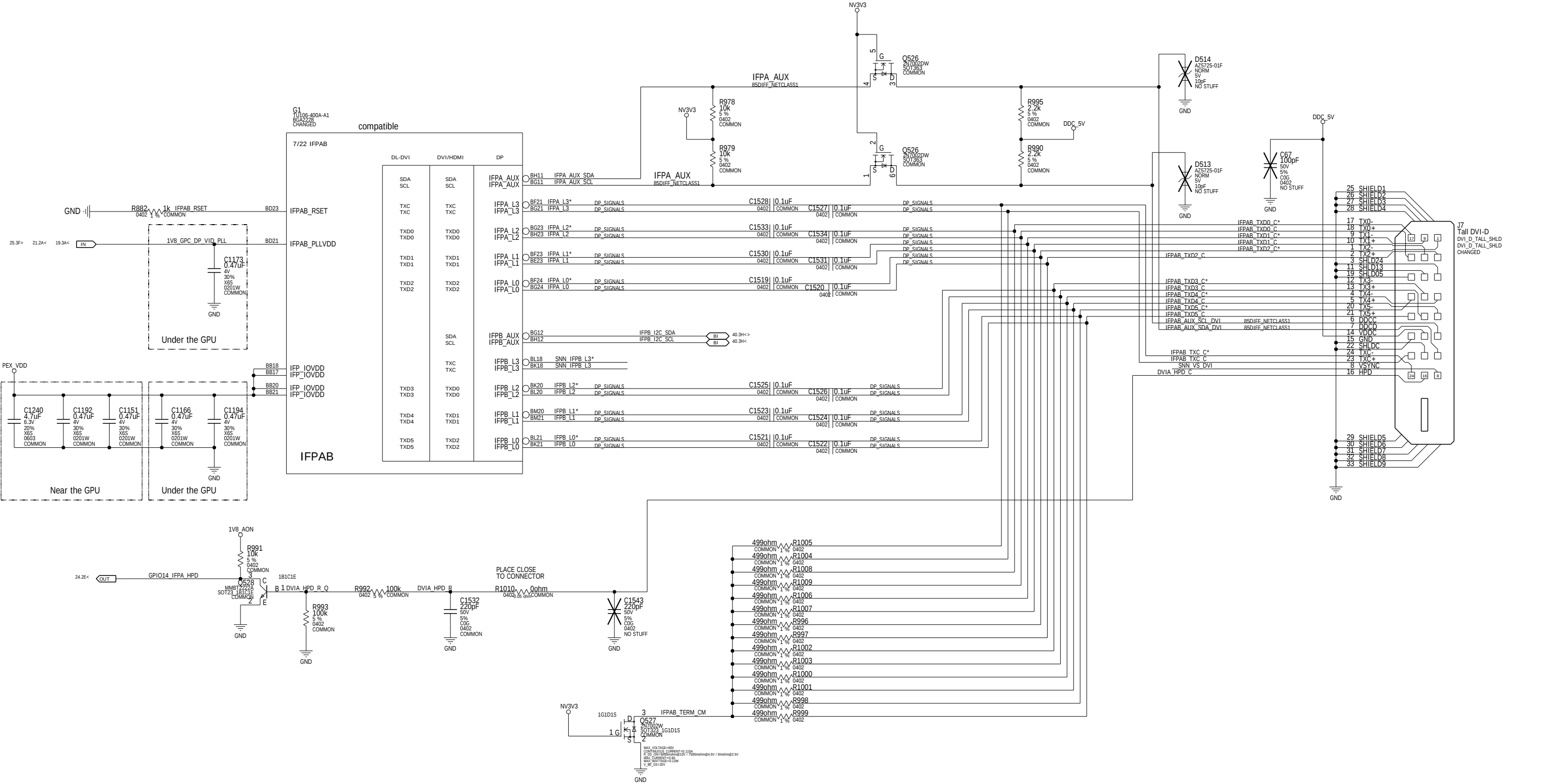
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Page17: GPU Decoupling 2

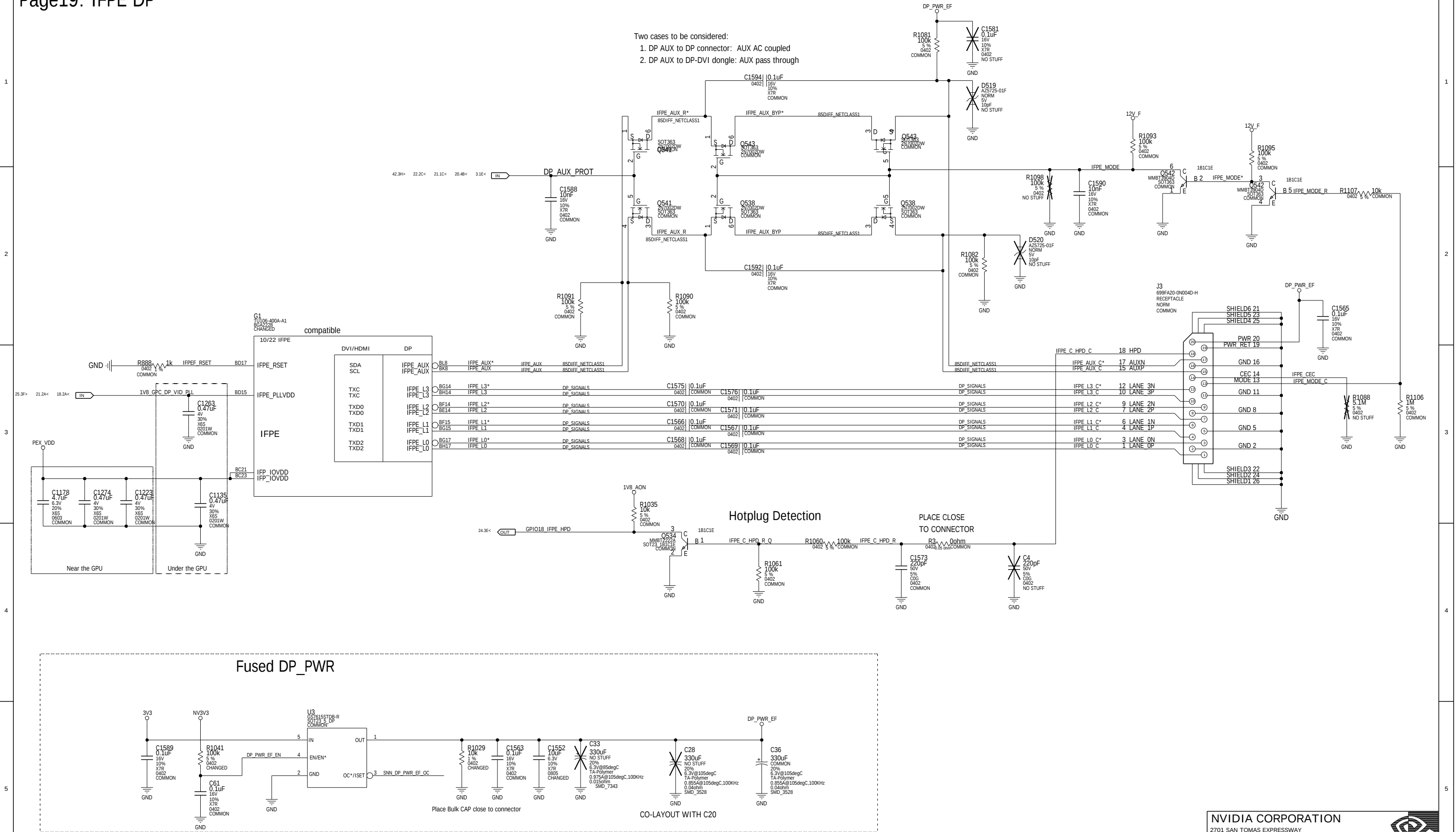
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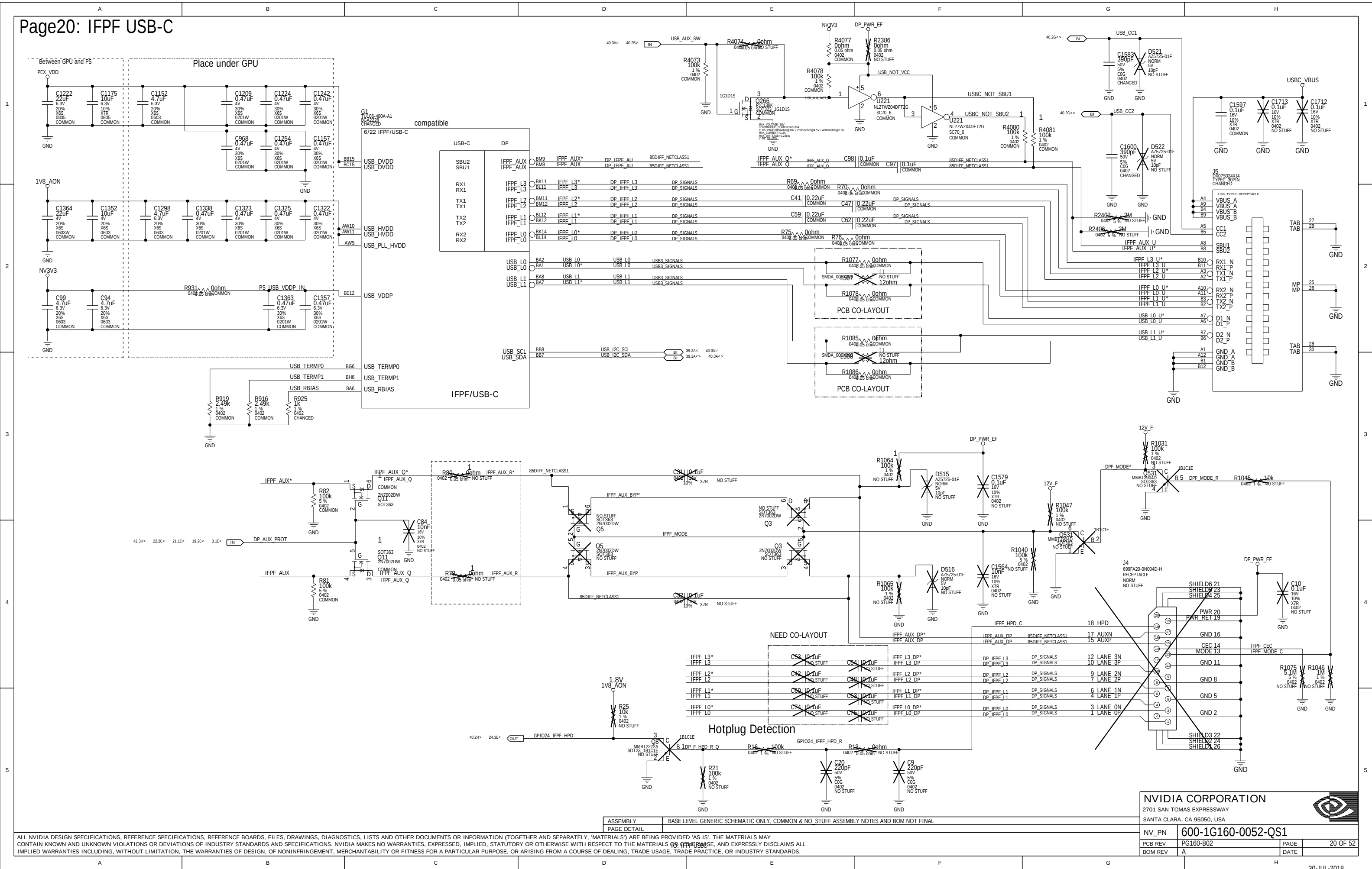


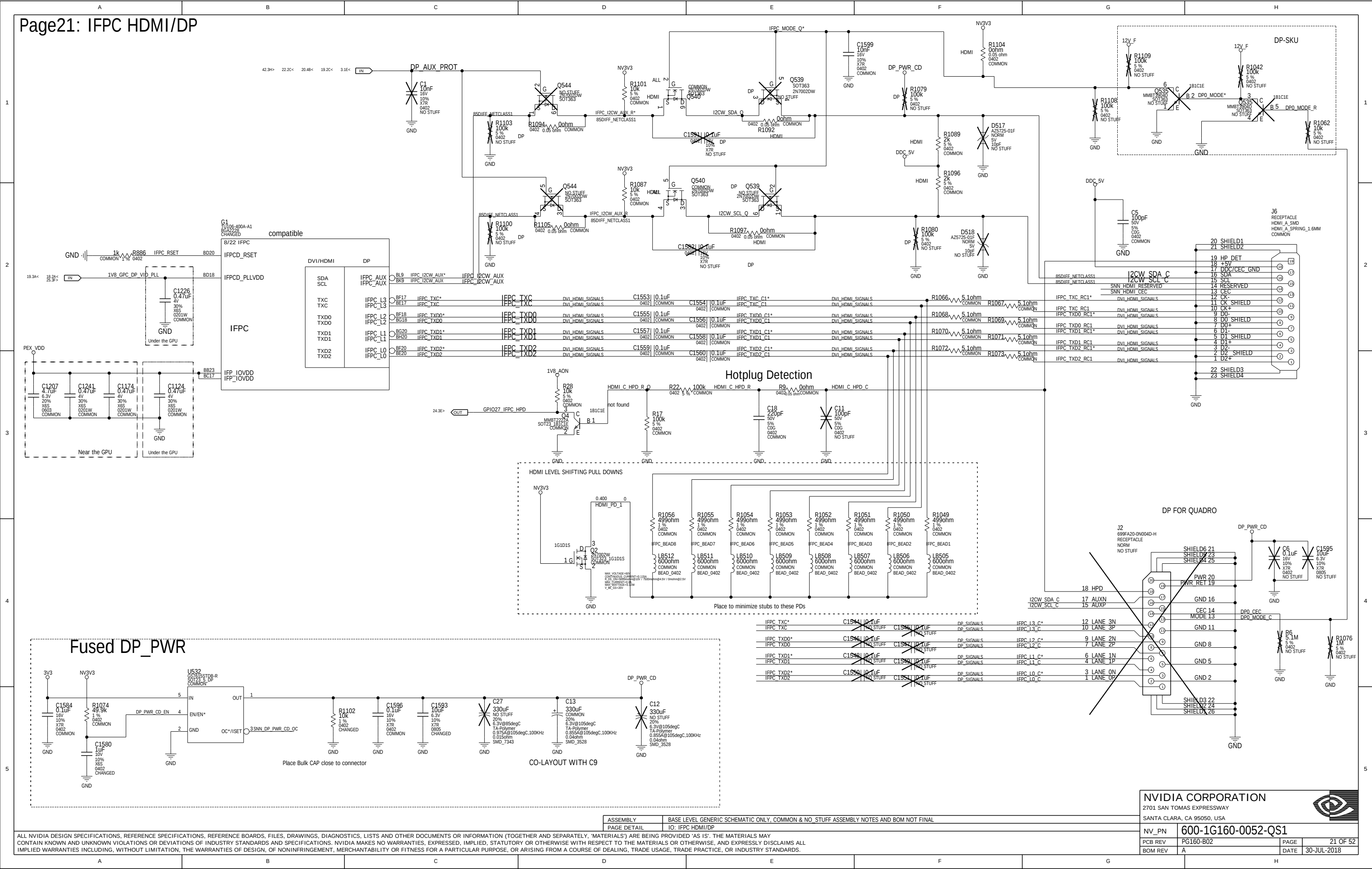
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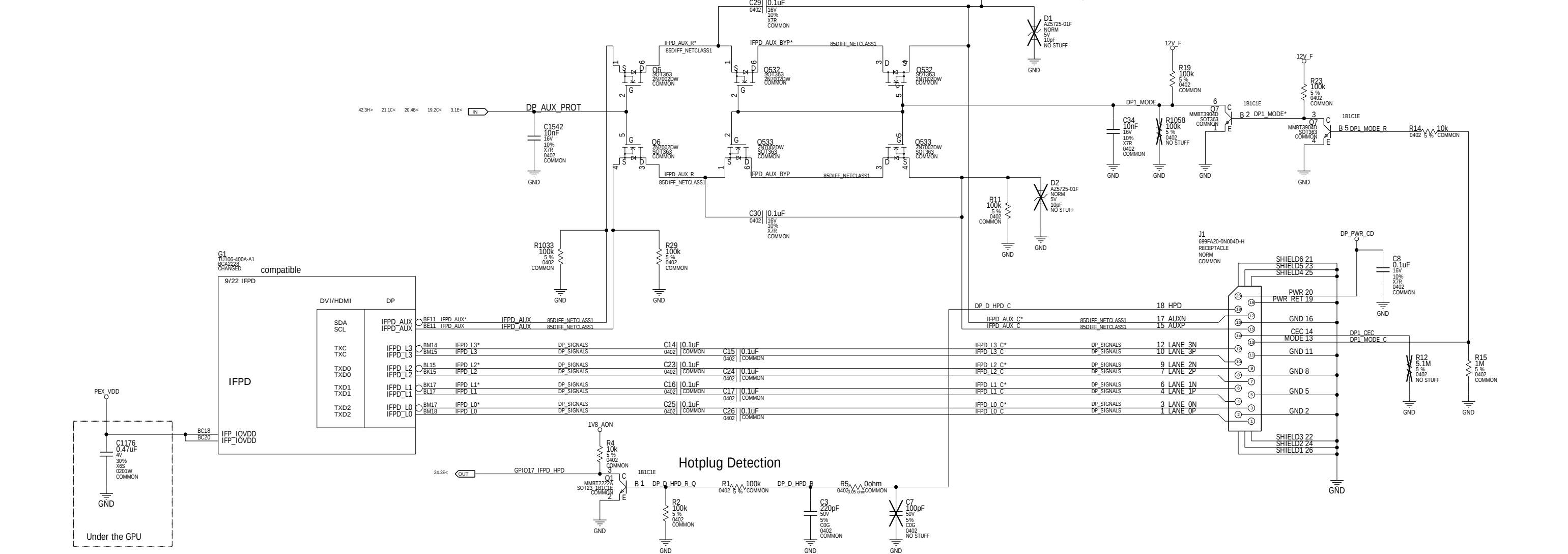


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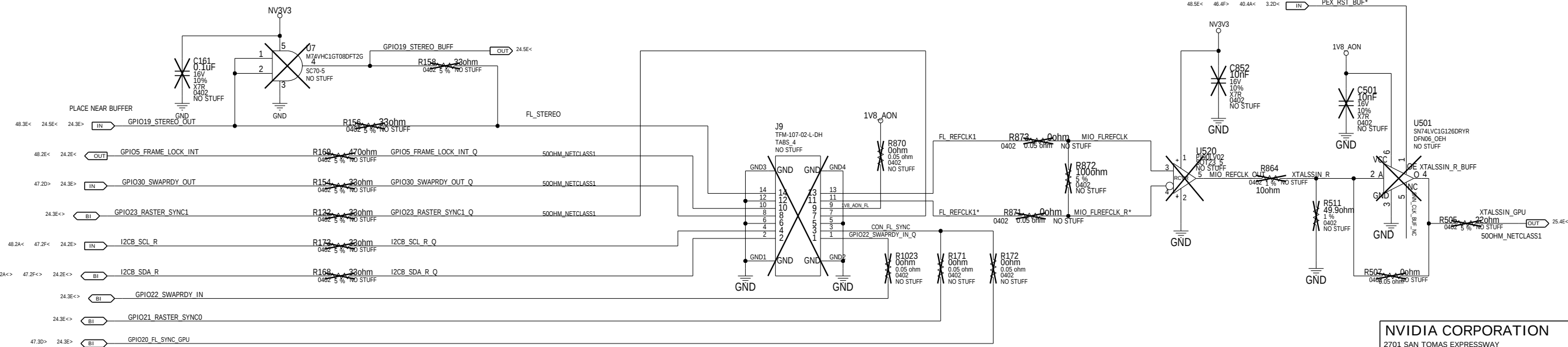
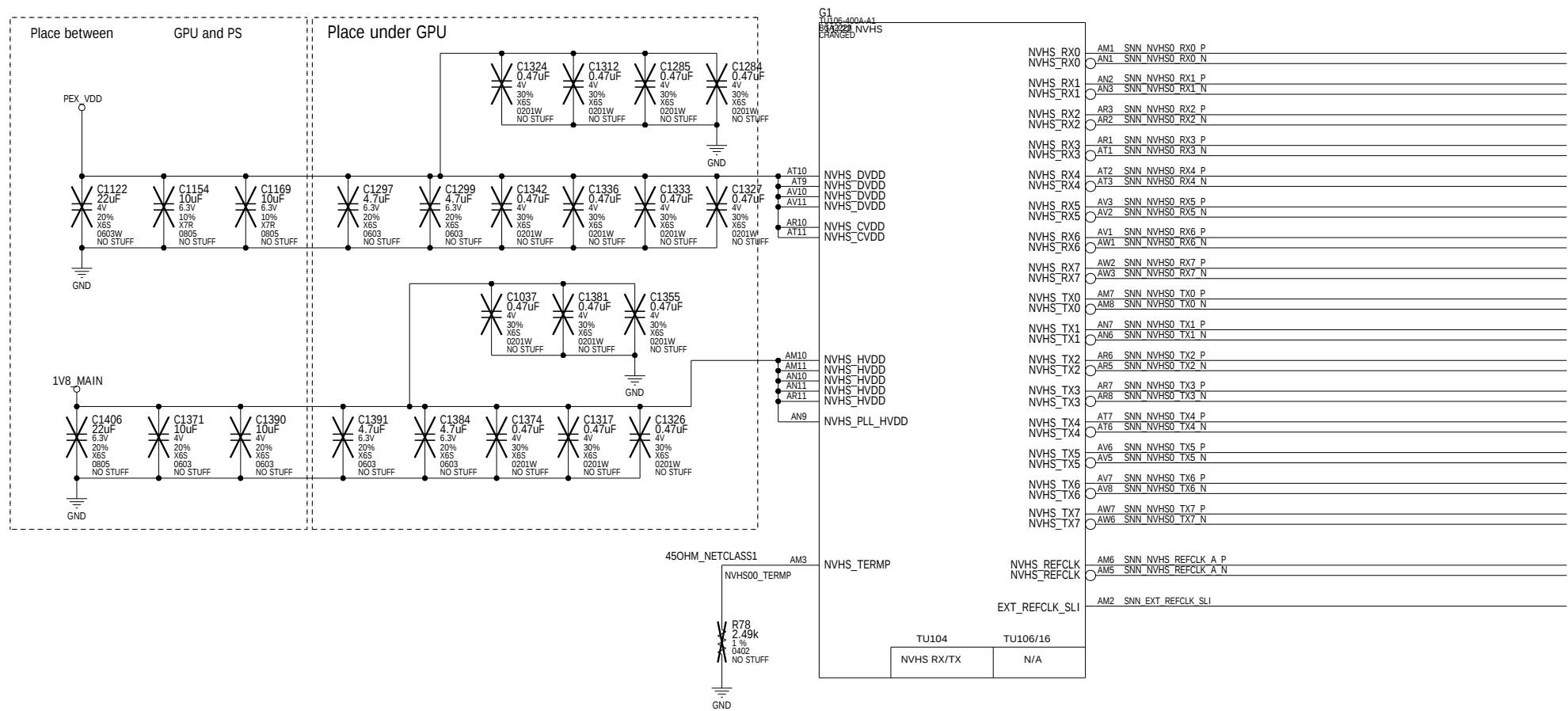
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- Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through



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Page23: NVHS Interface and Frame Lock



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PAGE DETAIL	IO: NVHS Interface and Frame Lock

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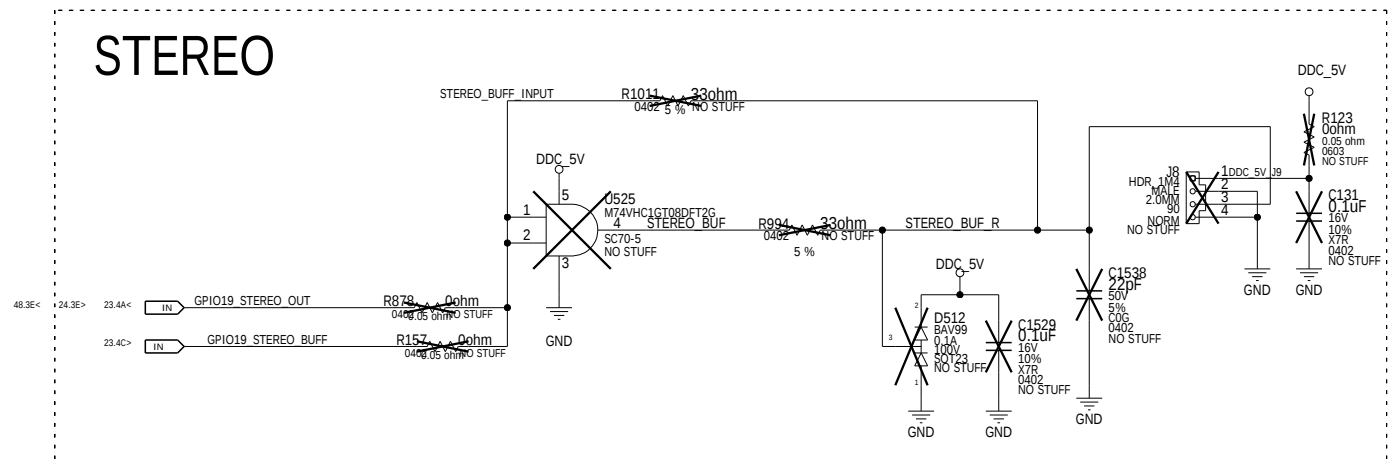
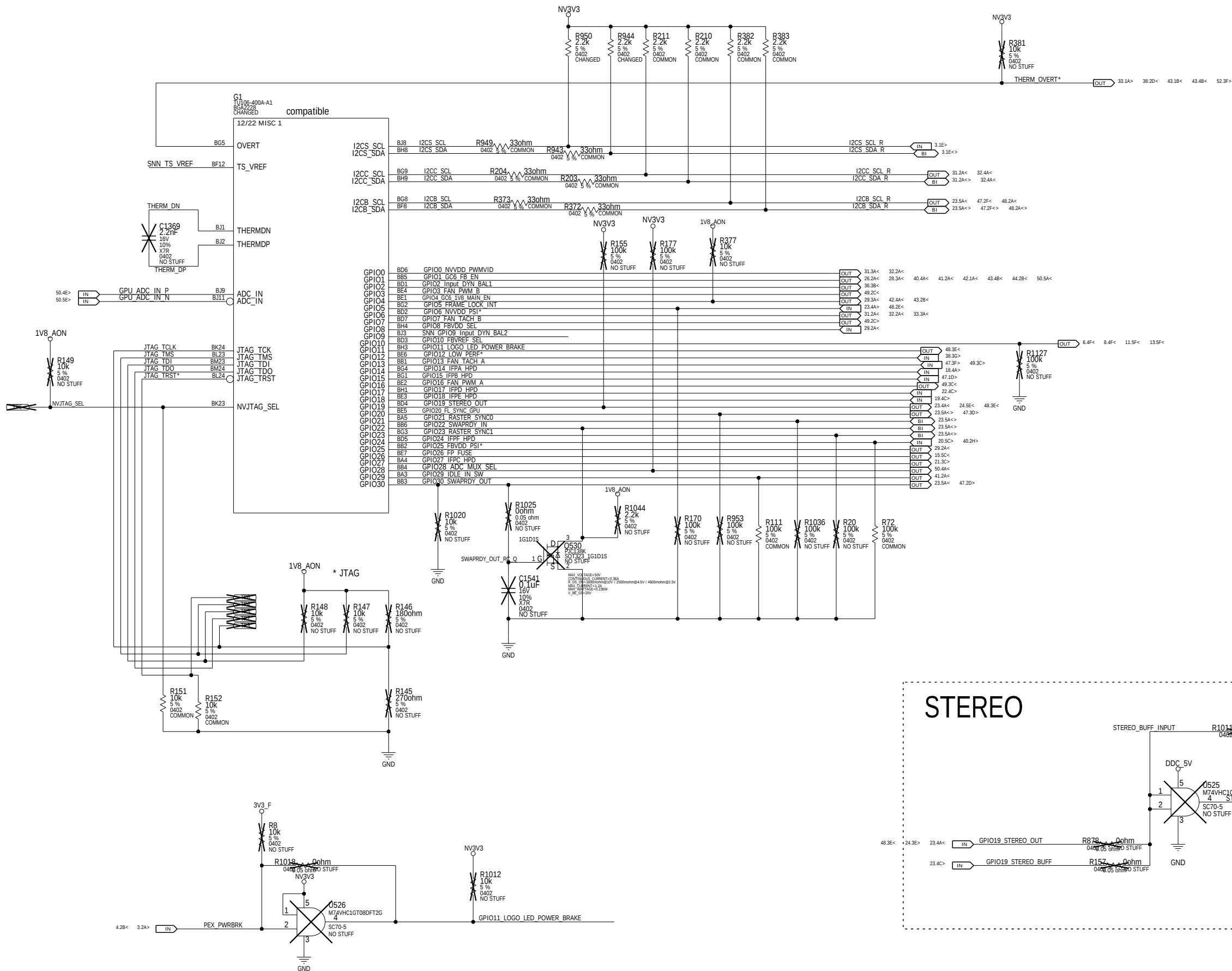
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	MISC1: Thermal, JTAG, GPIO, STEREO

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Page25: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

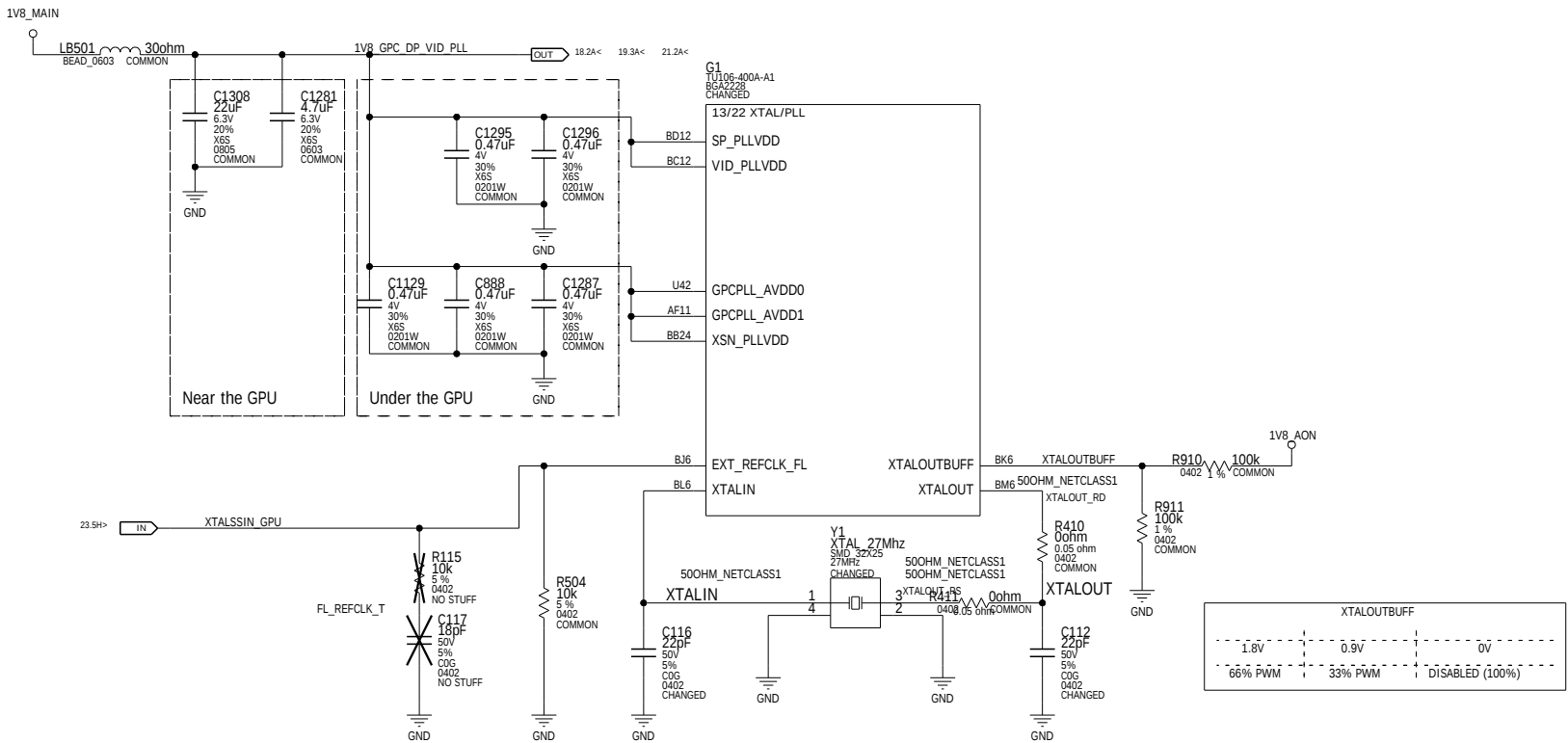
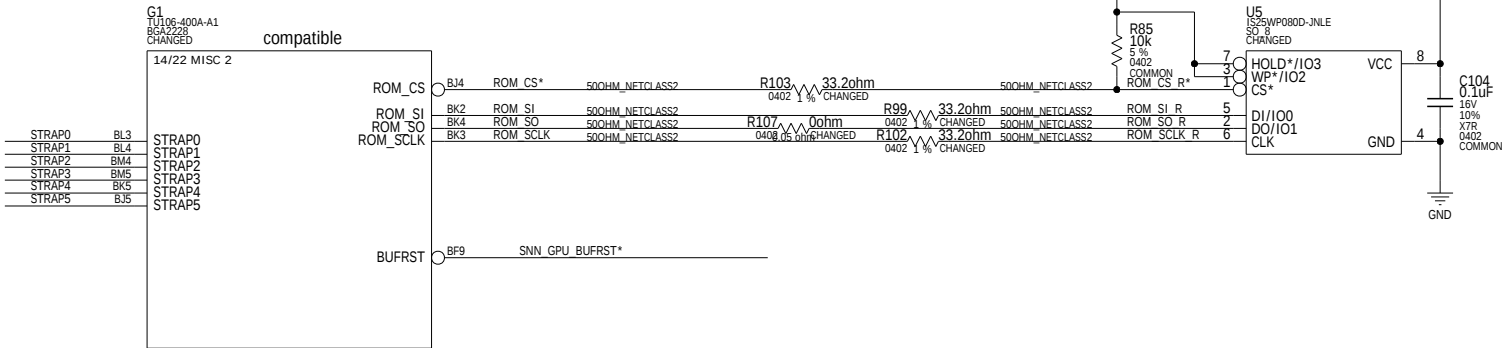
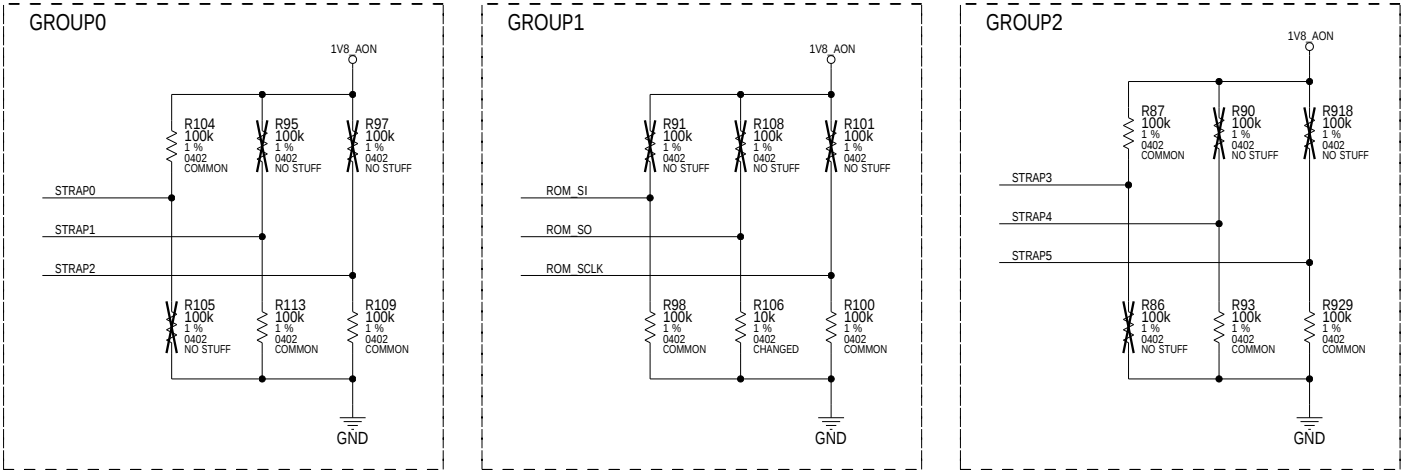
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

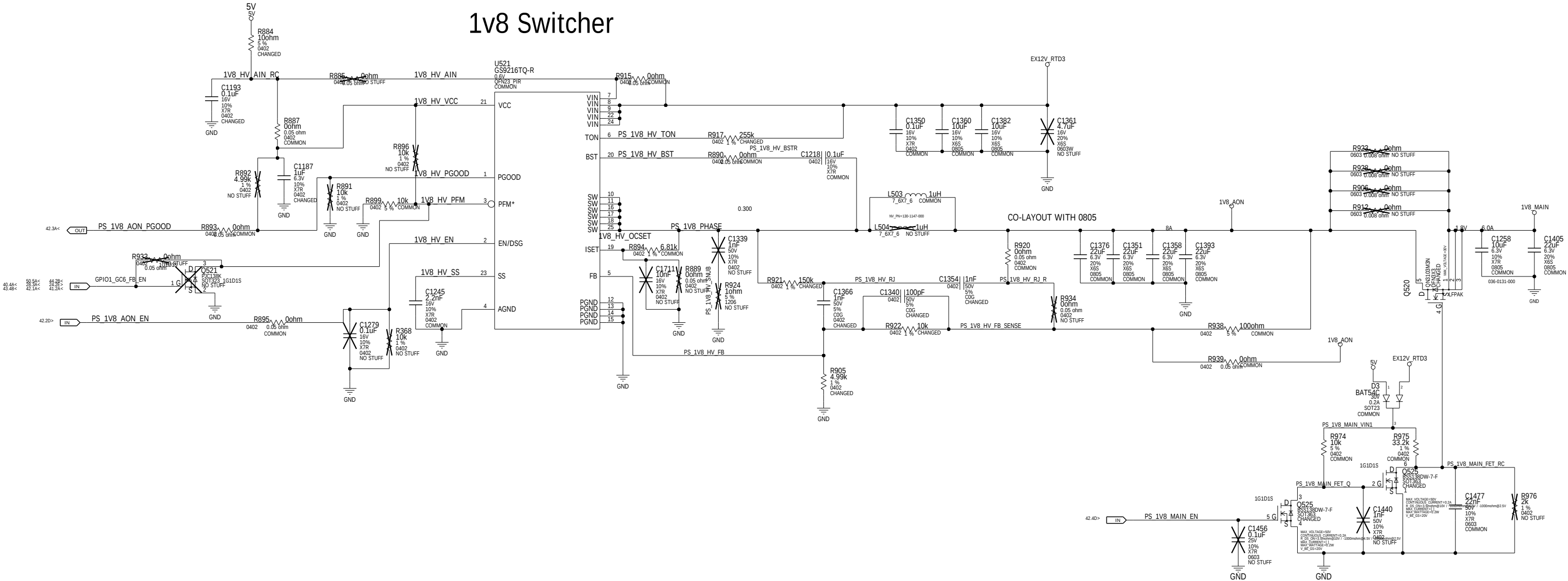
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

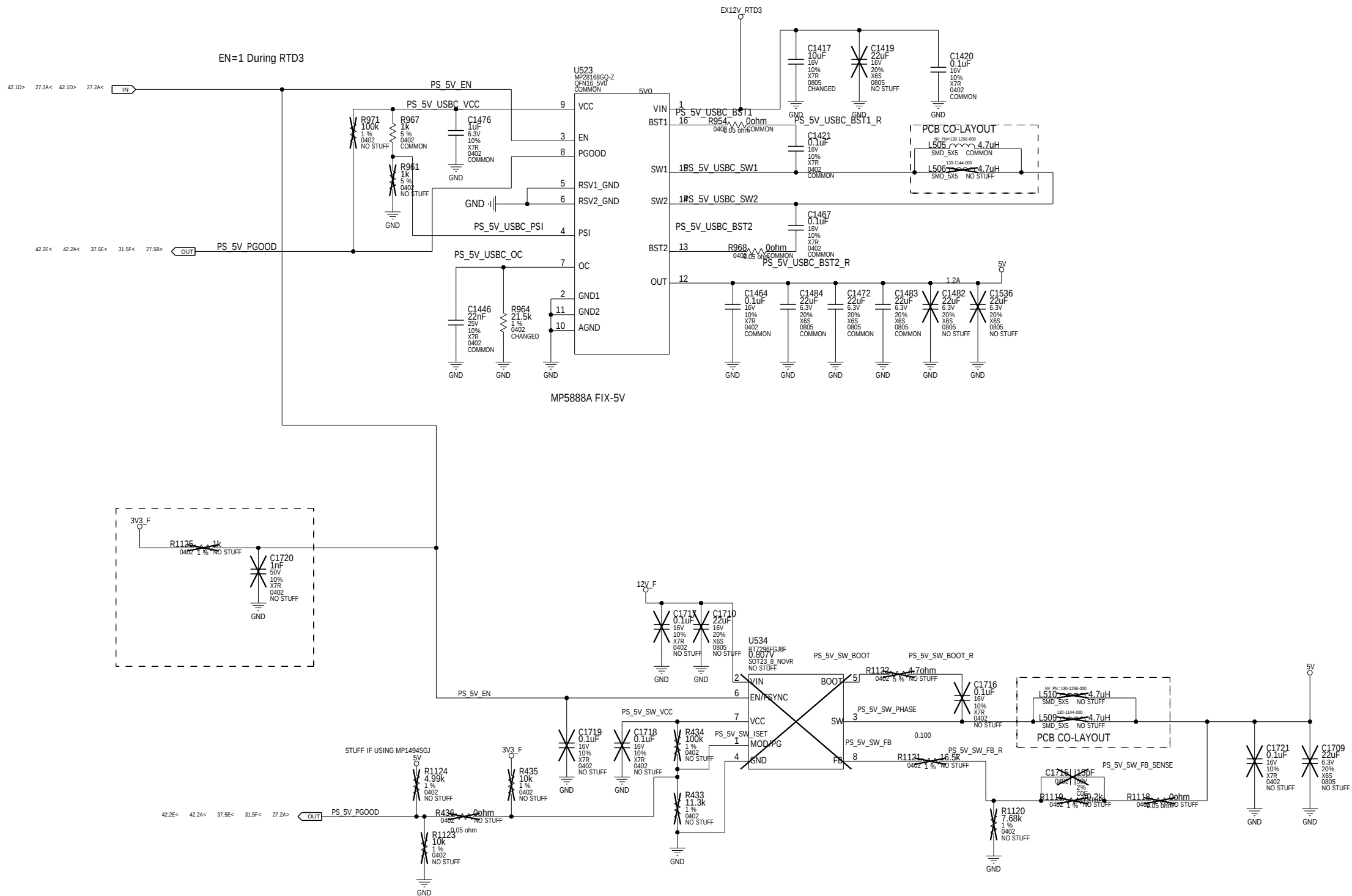
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



1v8 Switcher



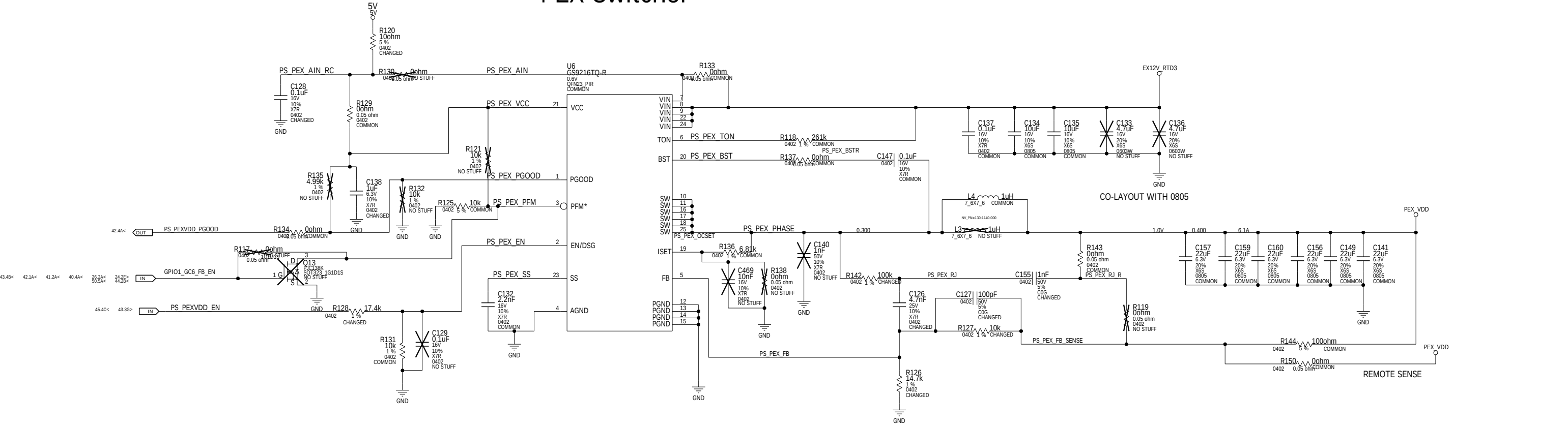
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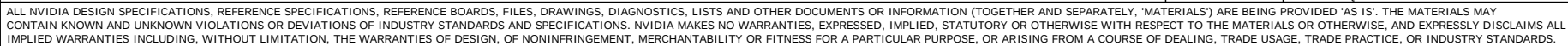
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PCB REV		P6160-B02		PAGE 27 OF 52
BOM REV		A		DATE 30-JUL-2018

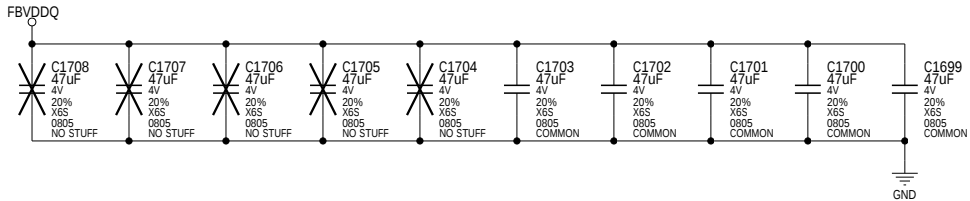
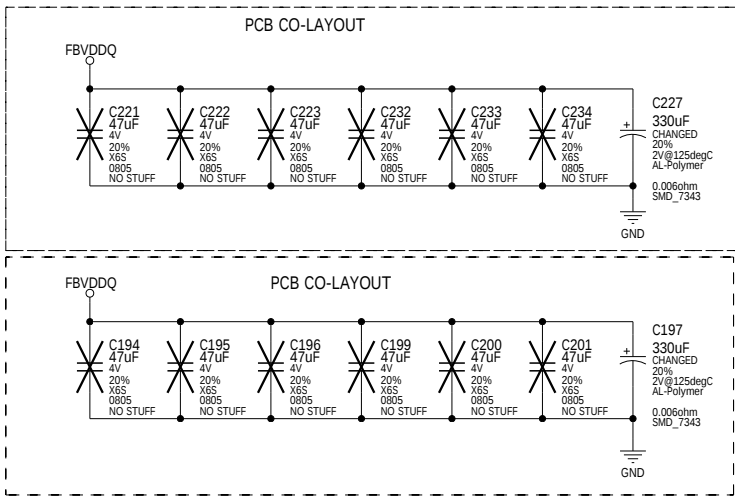
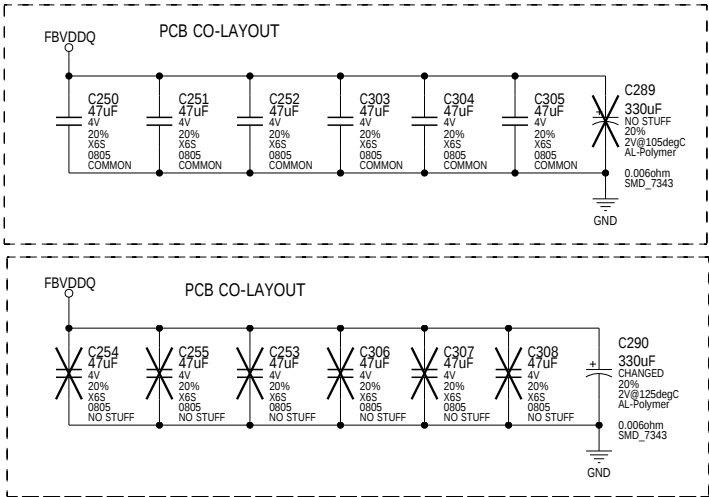
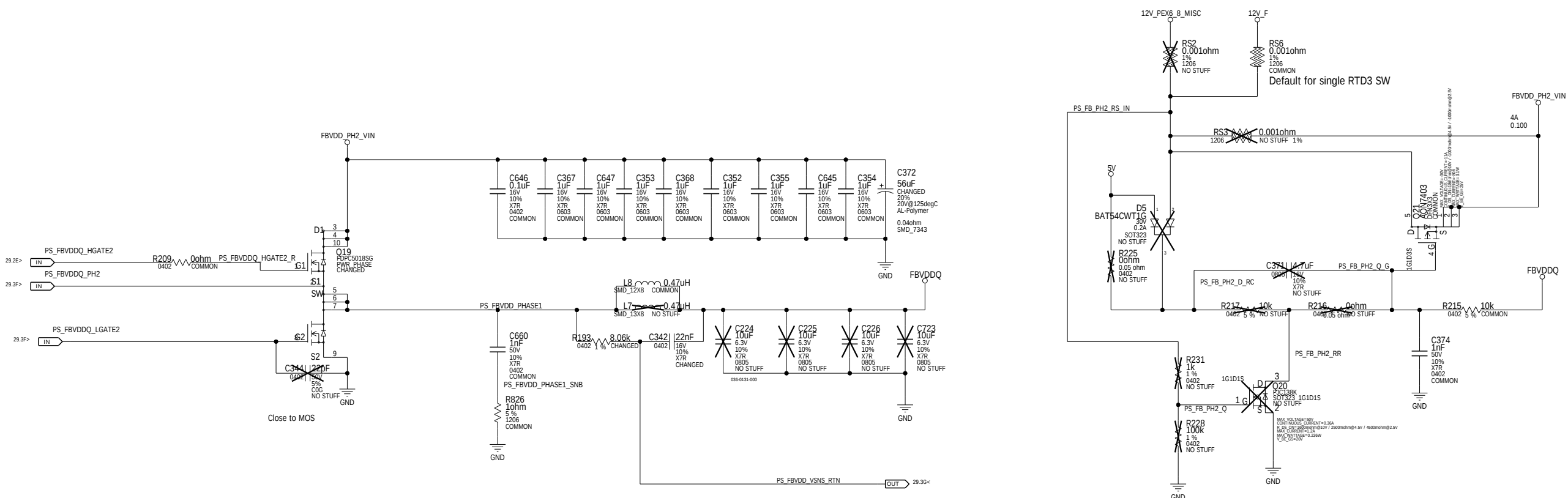
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PEX Switcher



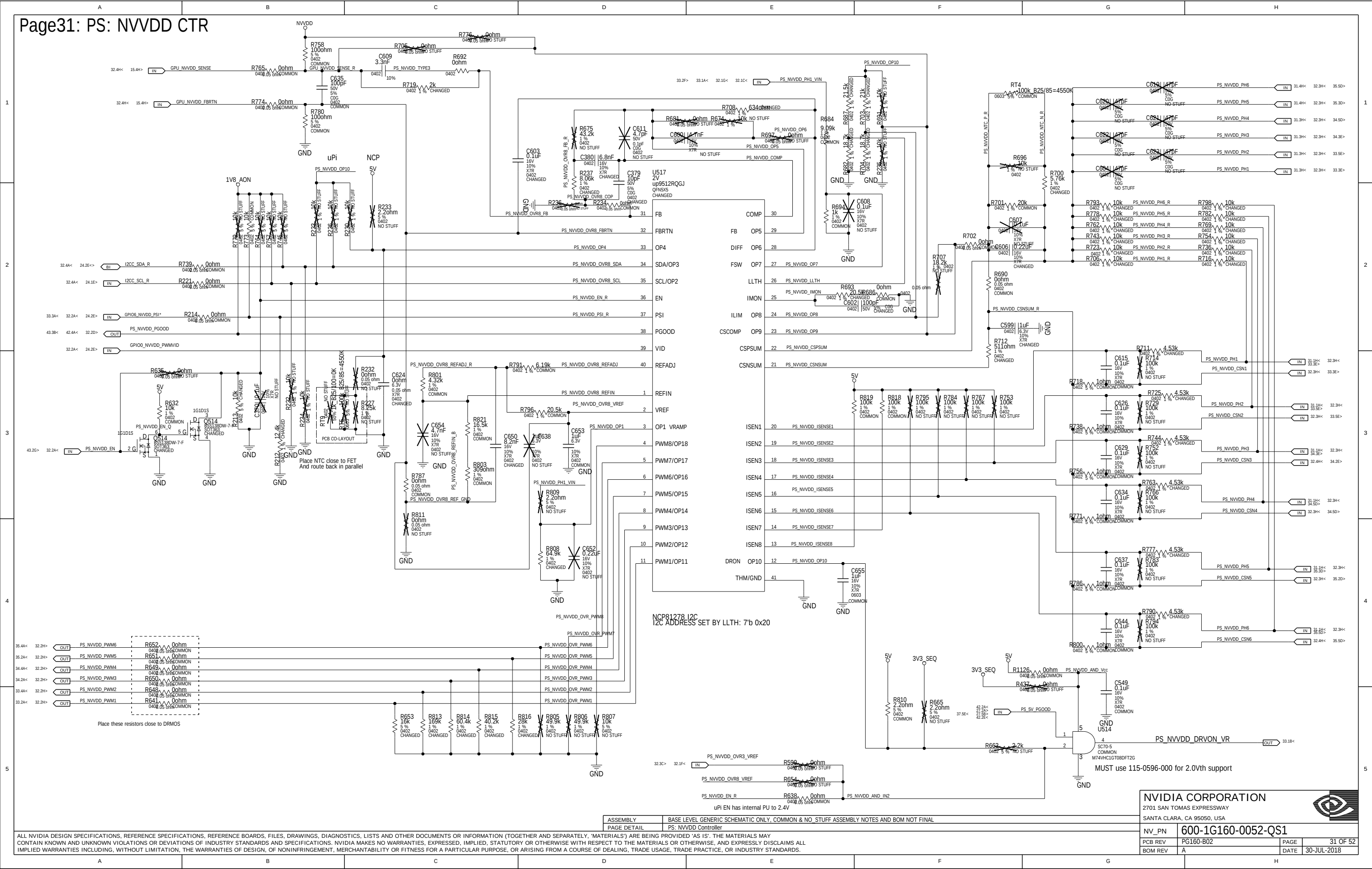
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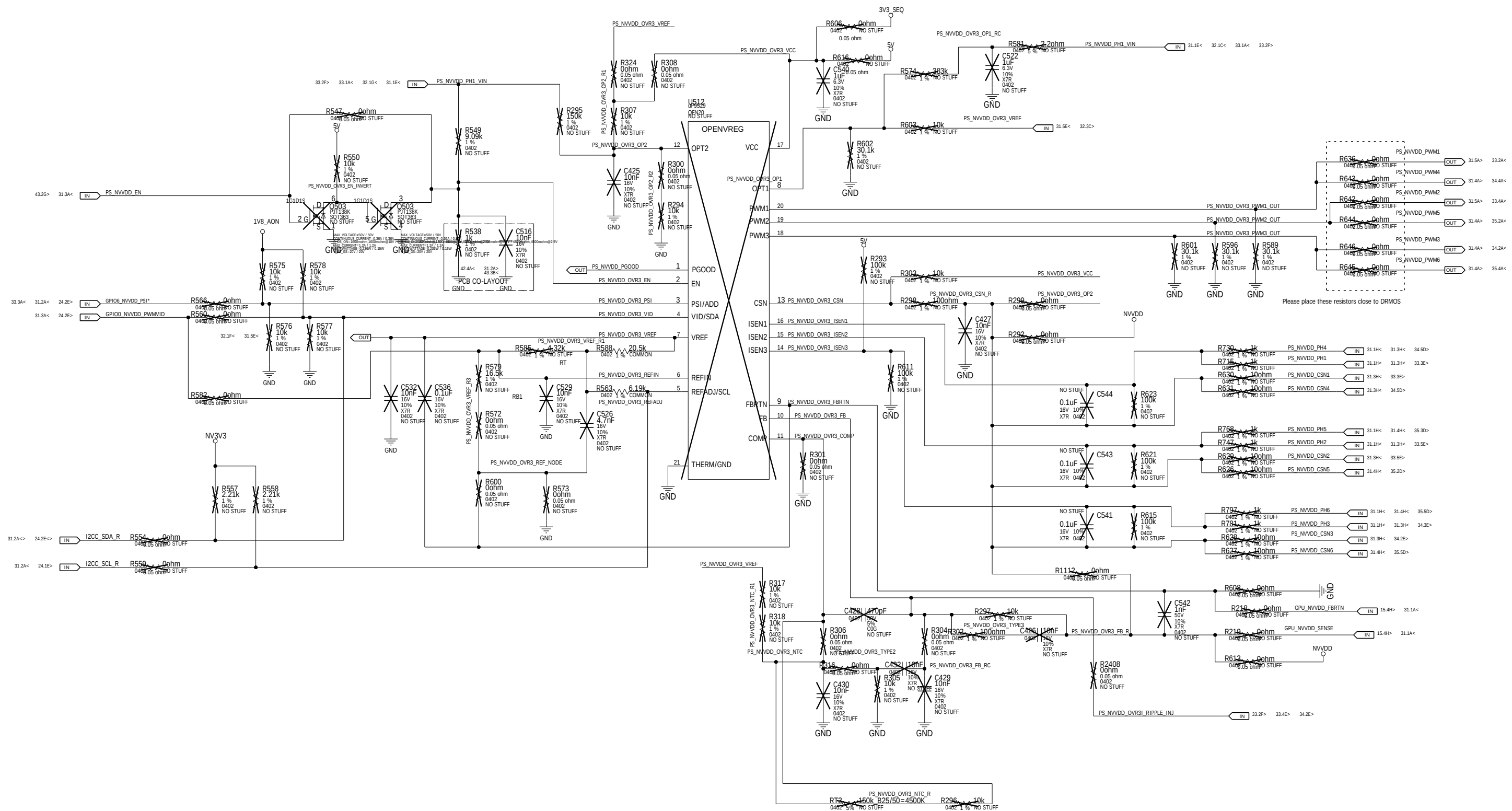


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Page31: PS: NVVDD CTR



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PAGE DETAIL	PS: NVVDD Controller OVR3i

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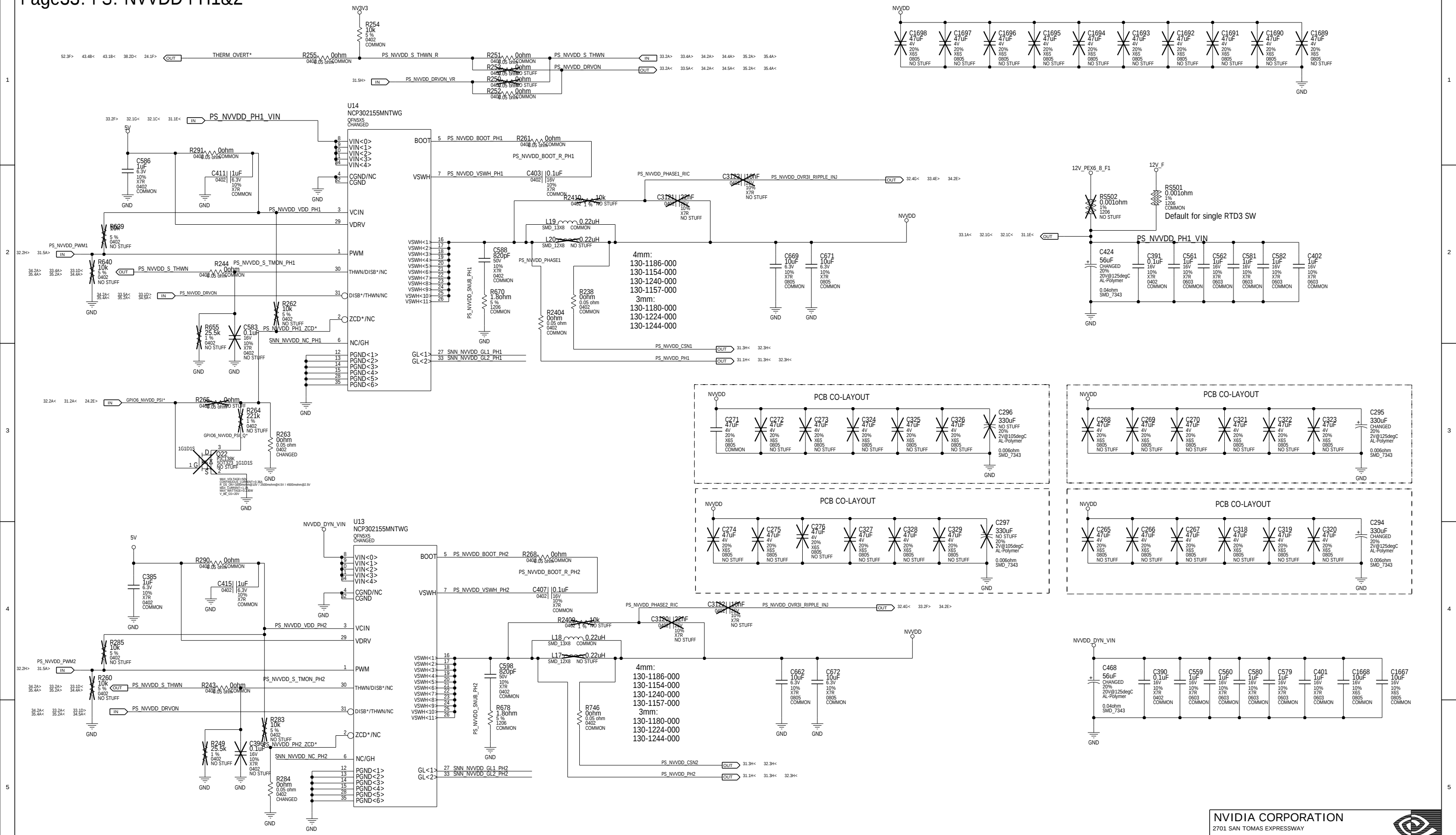
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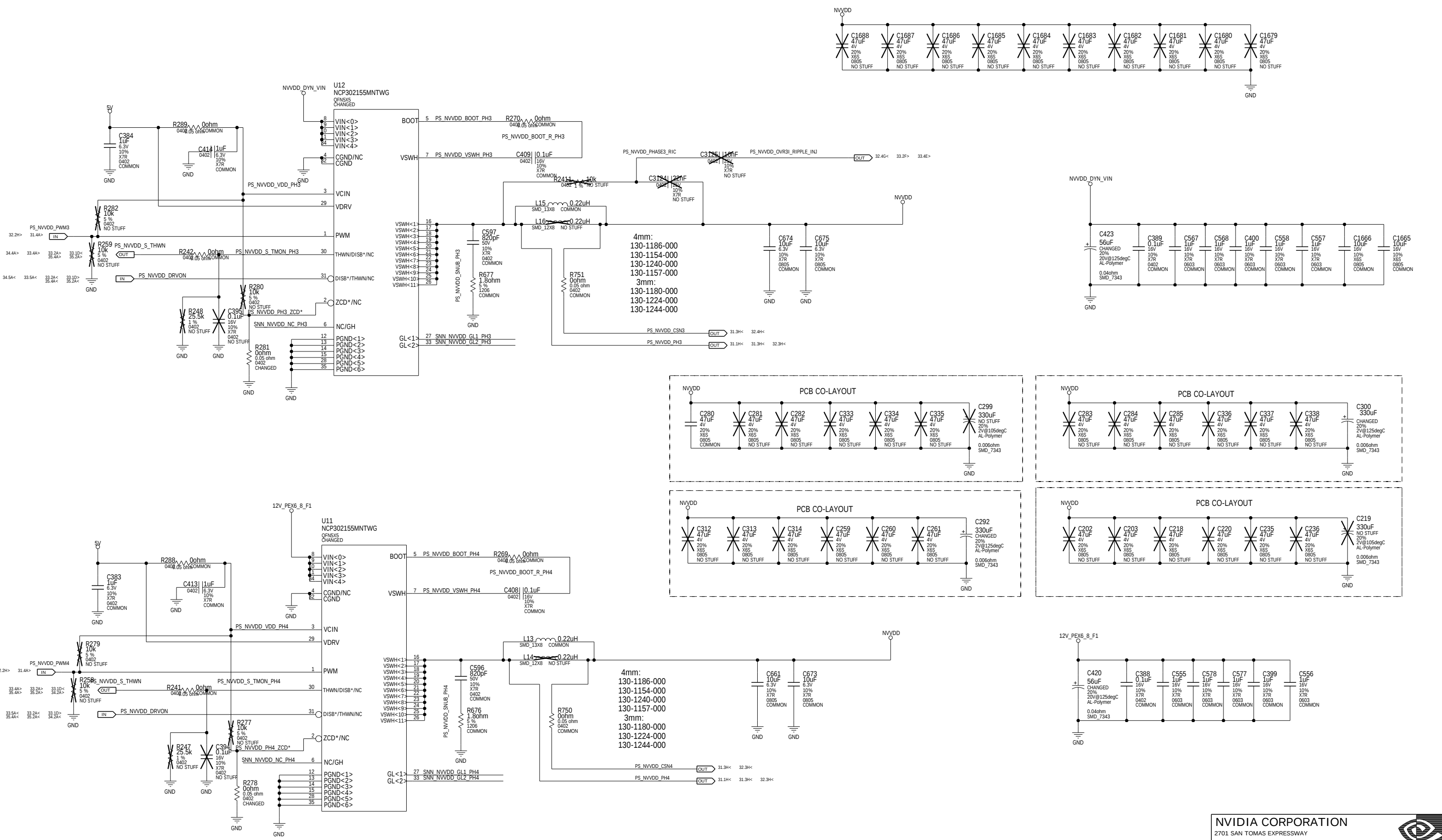
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BOM REV	A	DATE	30-JUL-2018

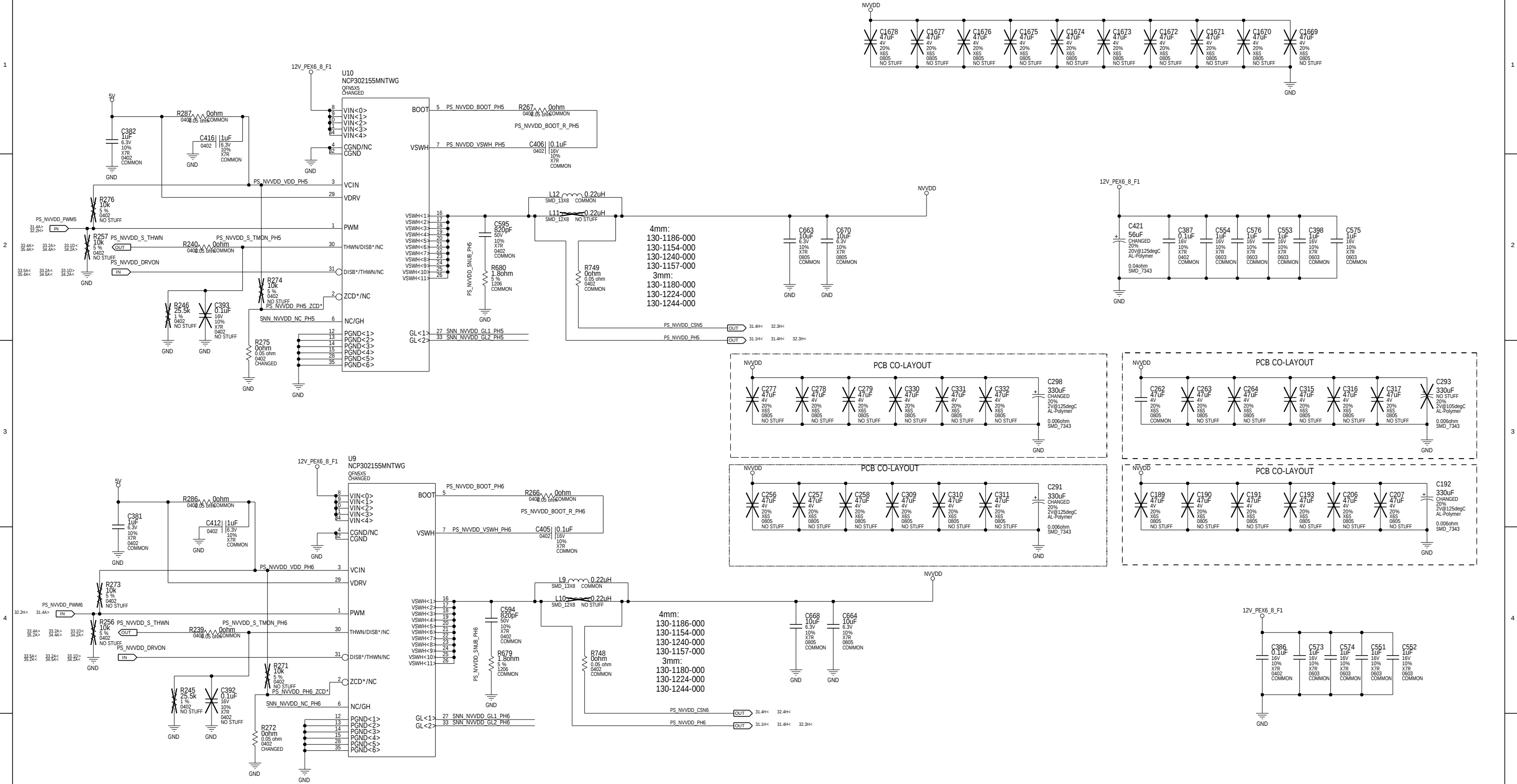




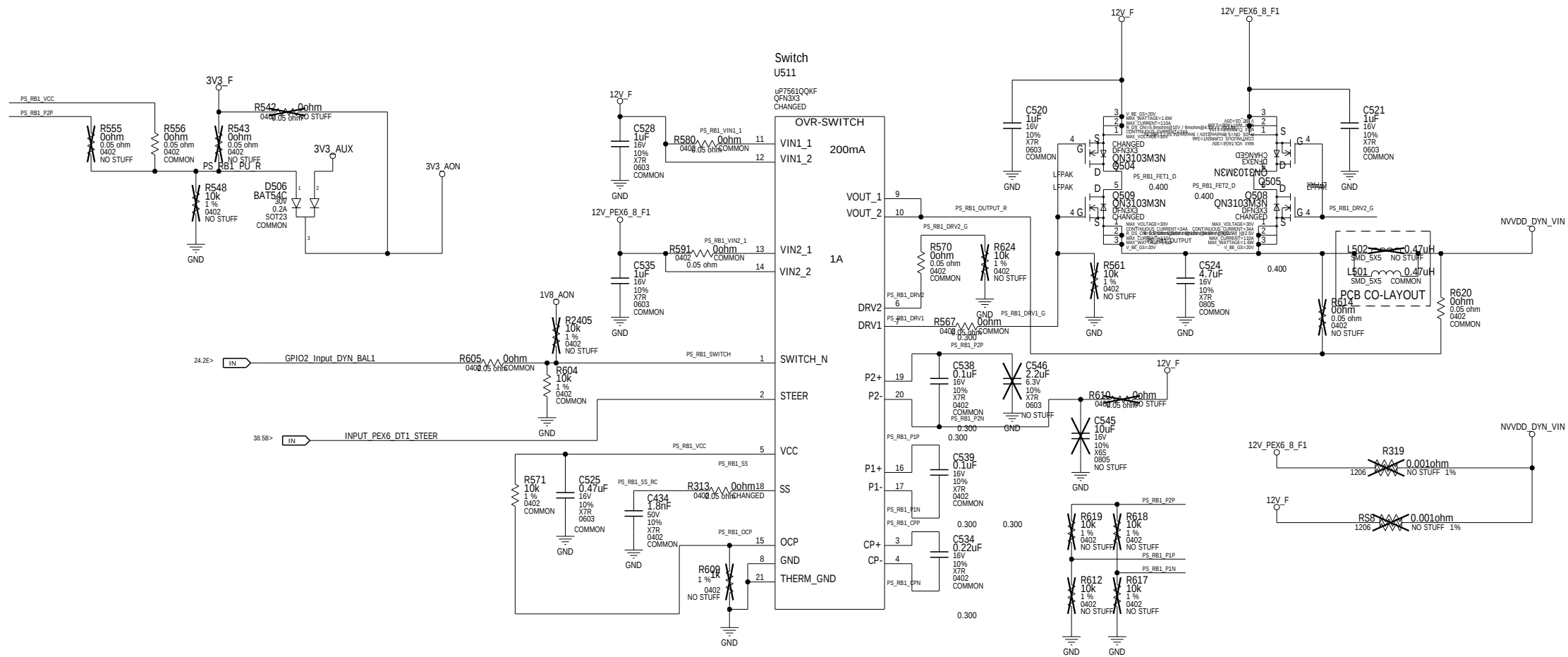
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Page35: PS: NVVDD PH5&6



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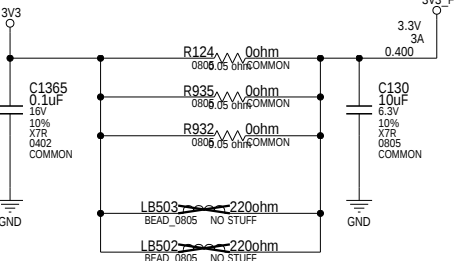


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PAGE DETAIL	PS: Input Power Balancing Switcher

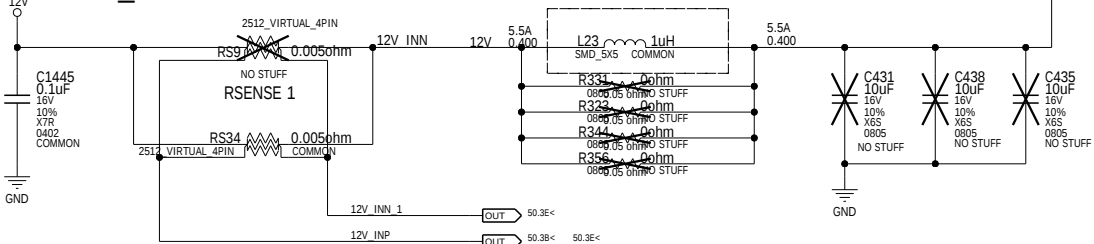
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Page37: PS: Inputs, Filtering, and Monitoring

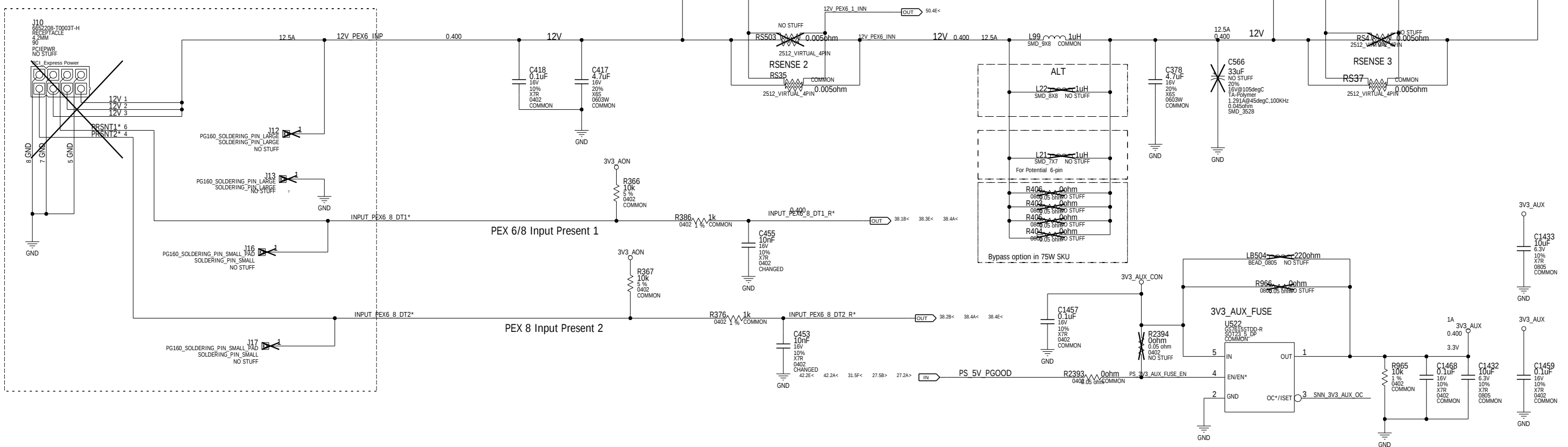
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX8 INPUT 1 - 2x4 PCIE CON 150W



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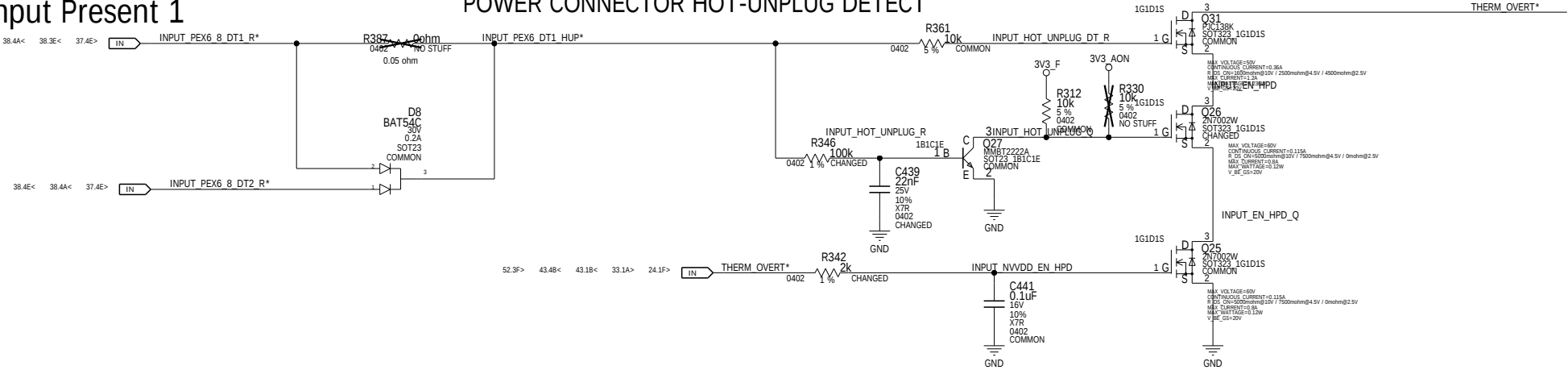
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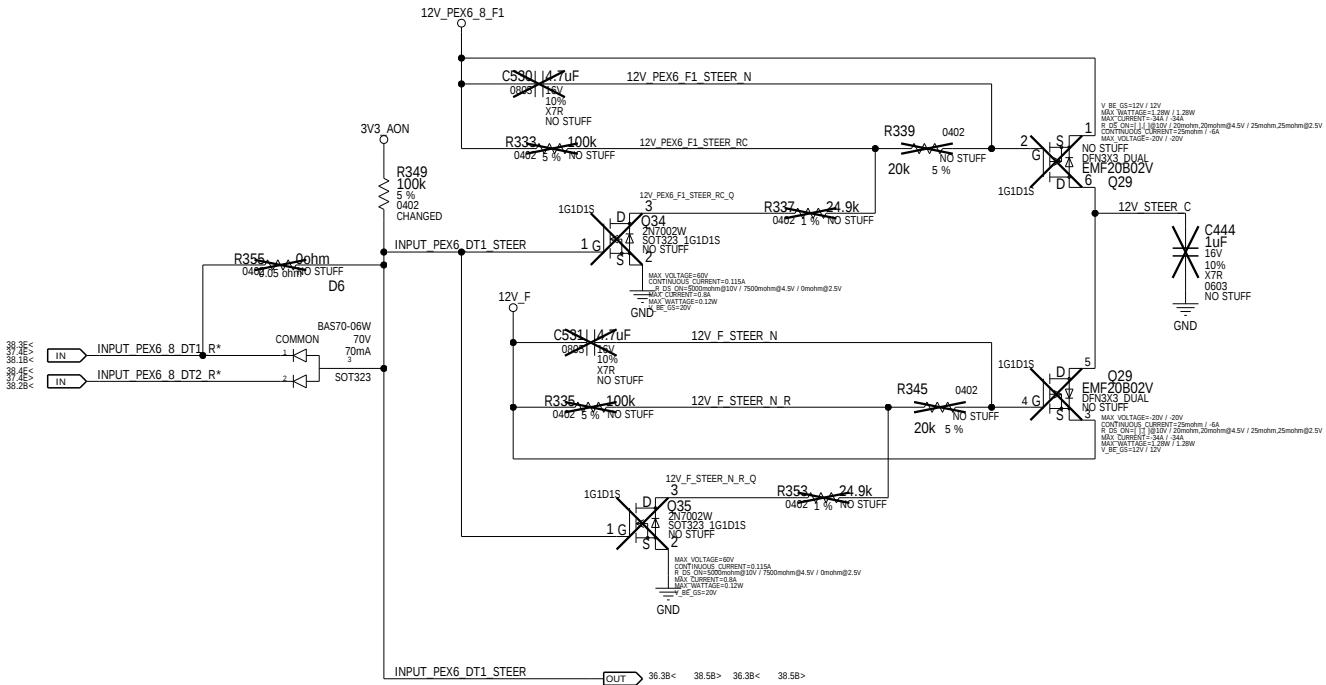
PEX Input Present 1

POWER CONNECTOR HOT-UNPLUG DETECT

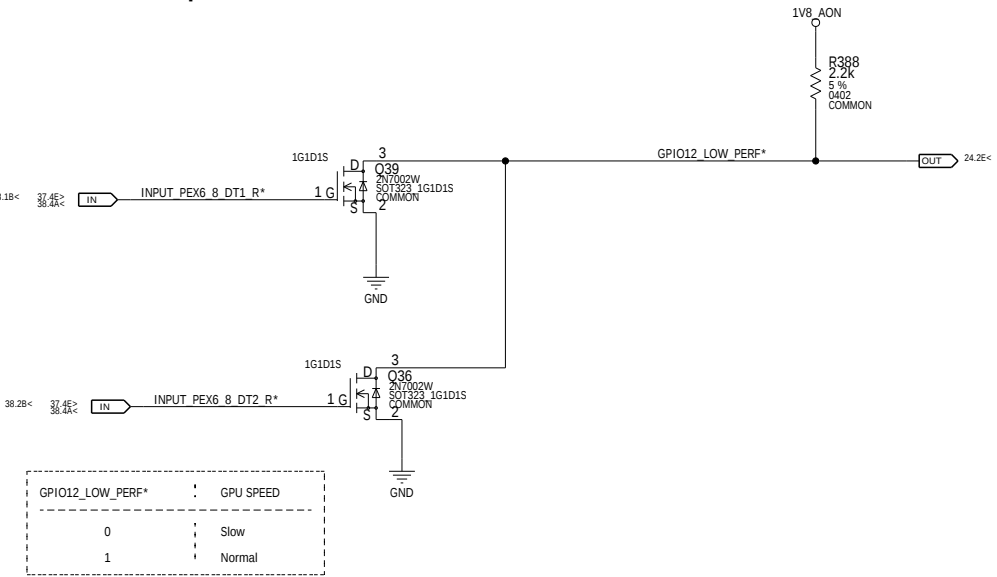


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



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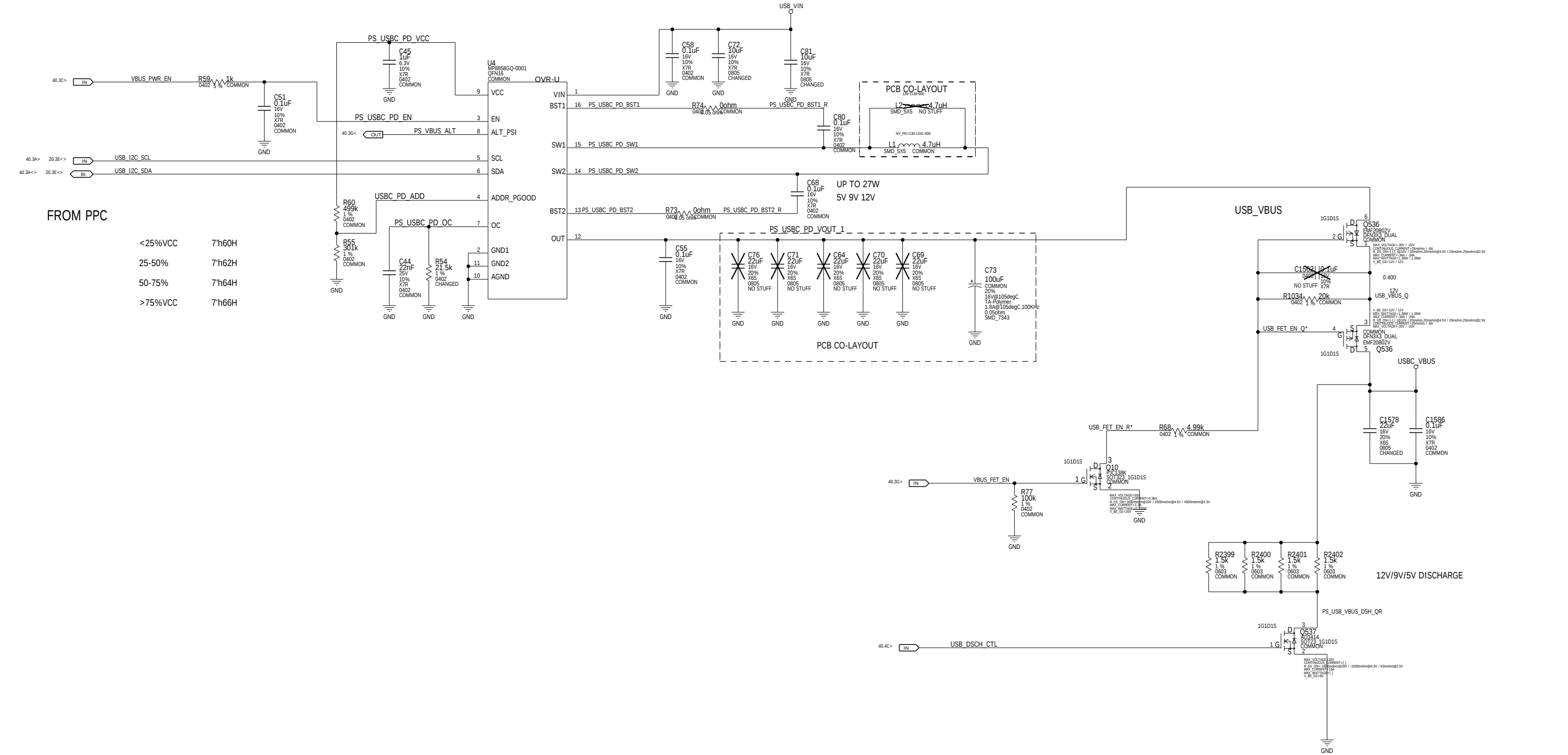
PAGE

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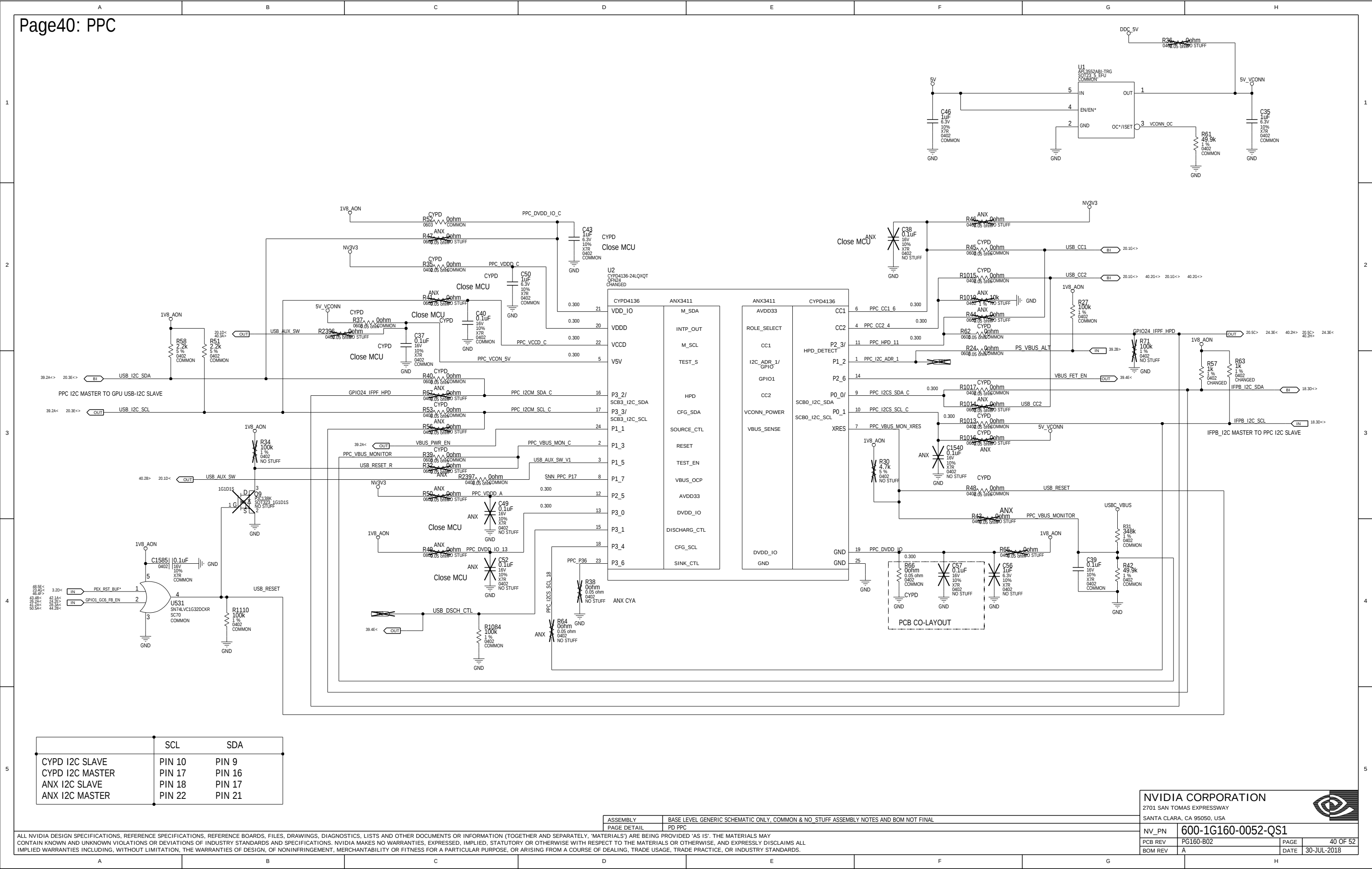
DATE

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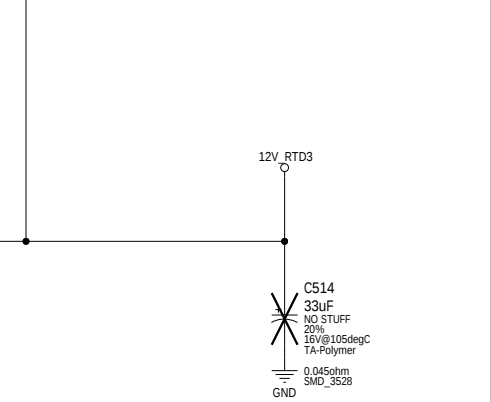
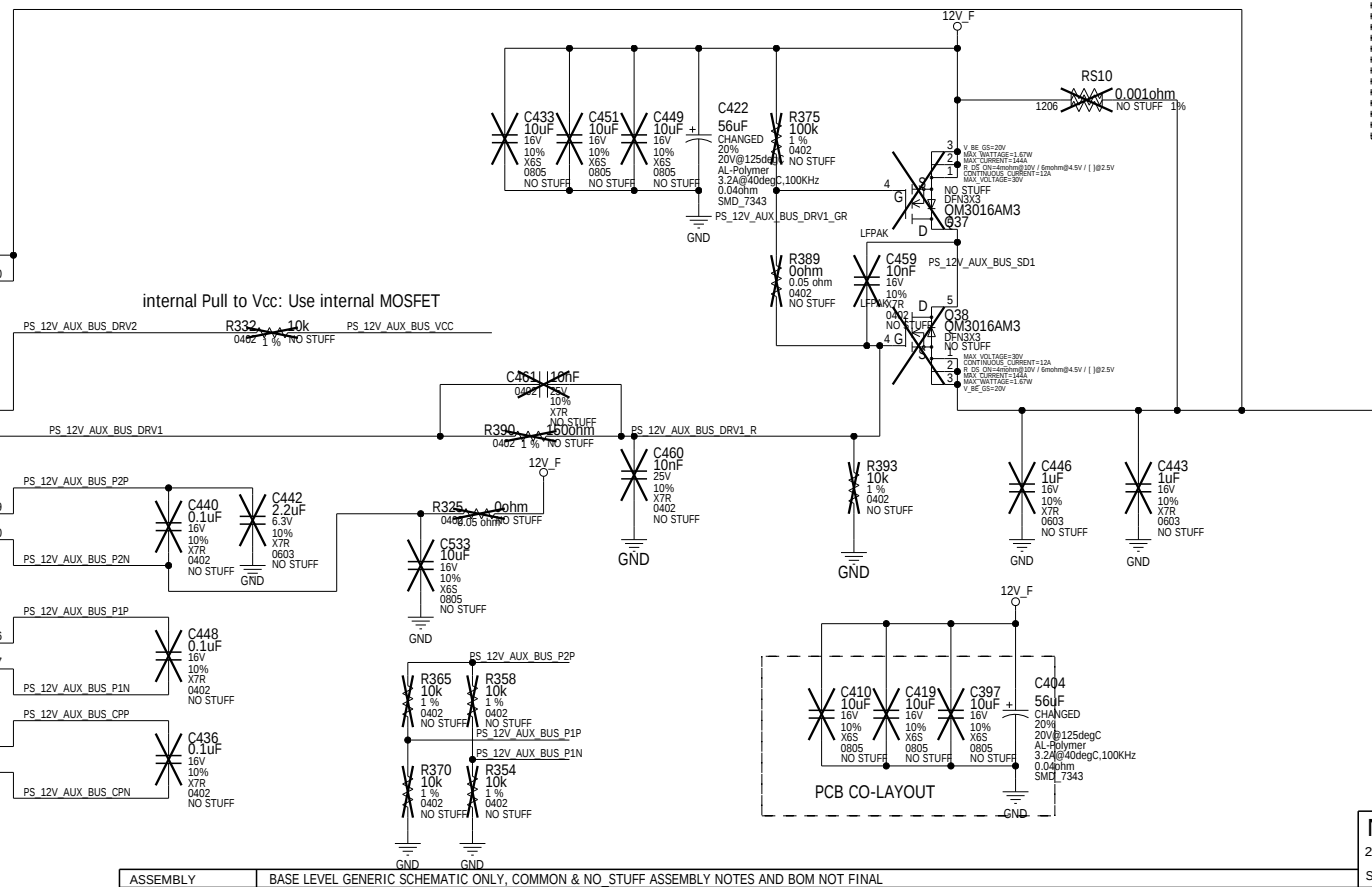
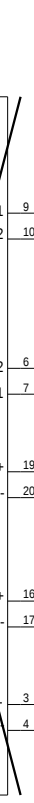
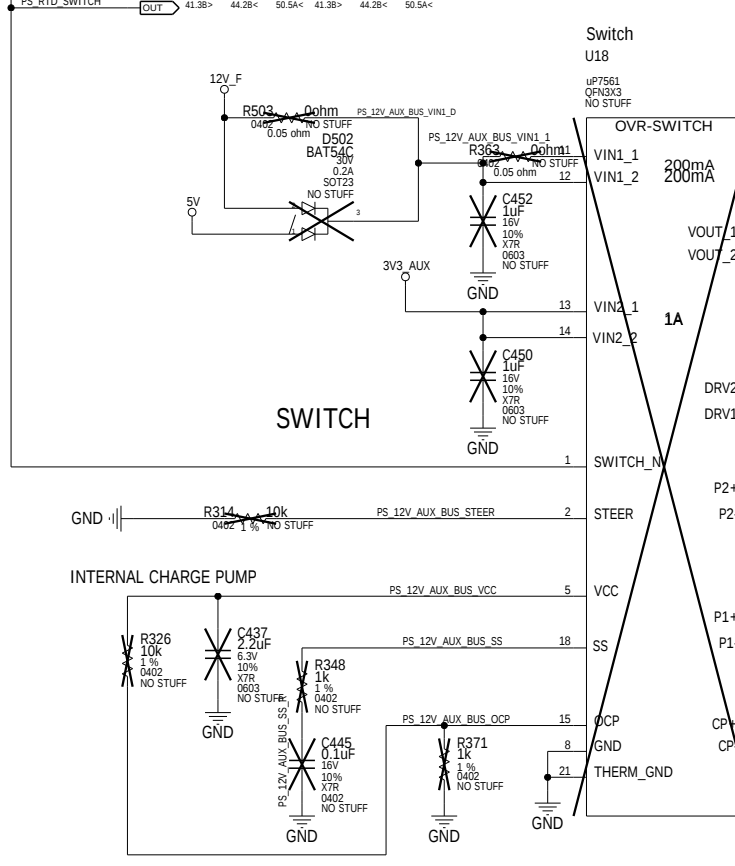
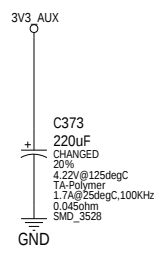
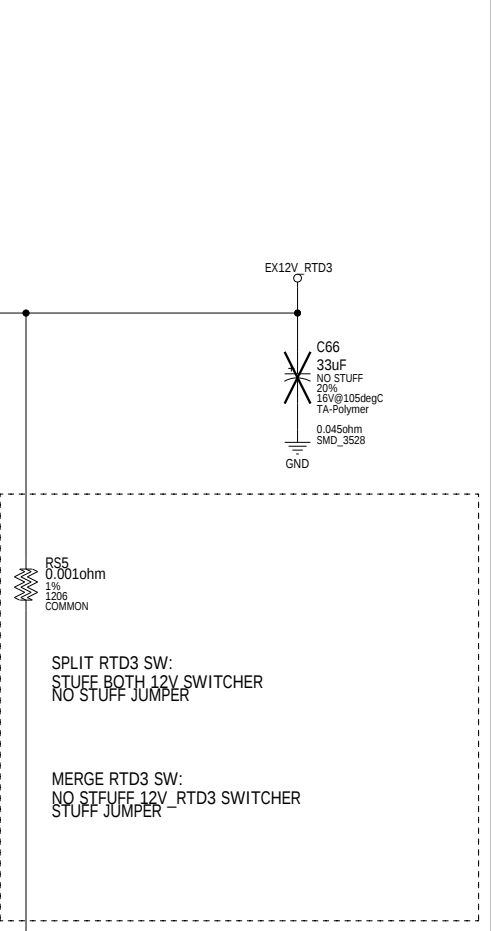
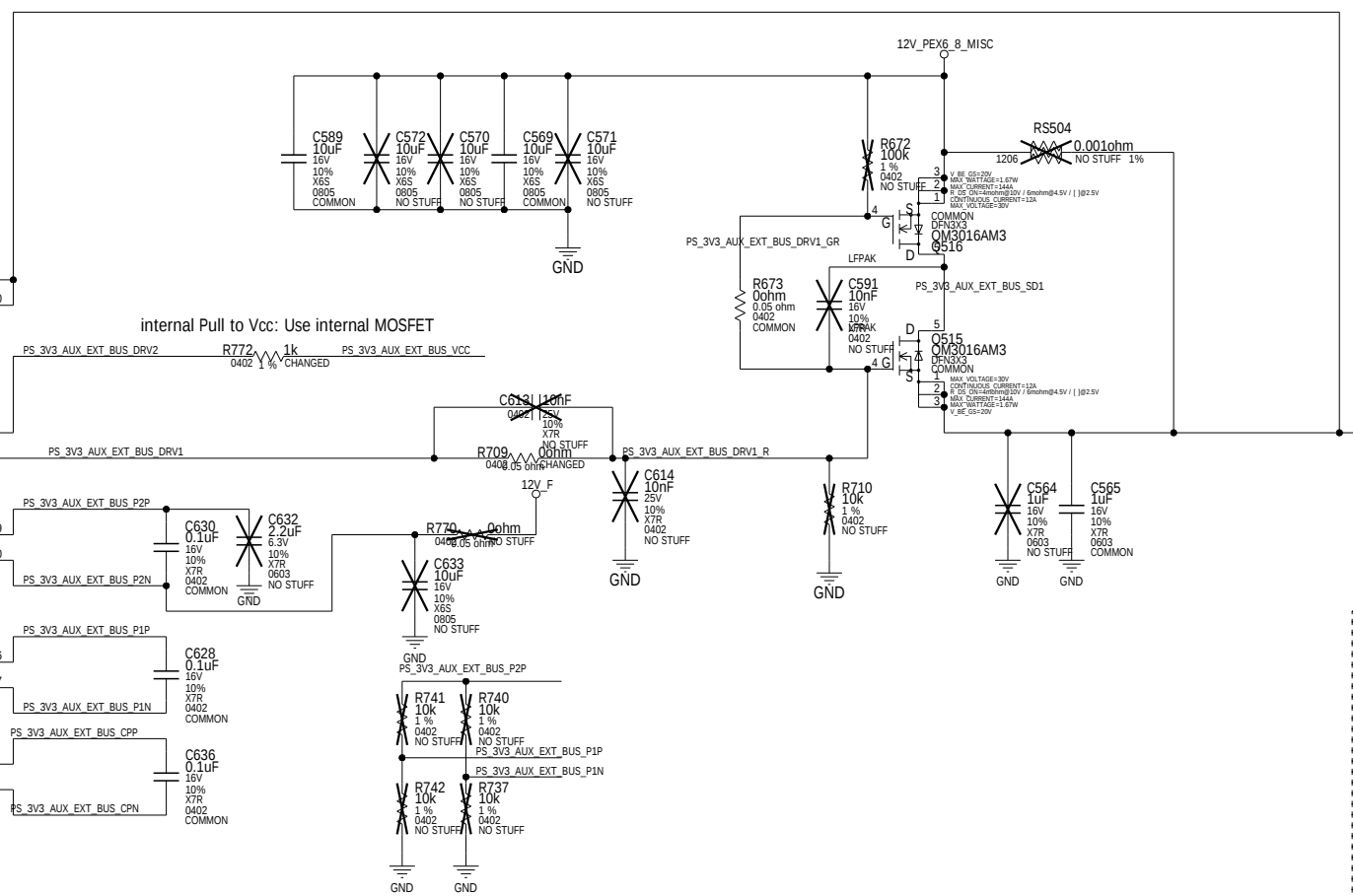
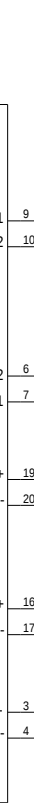
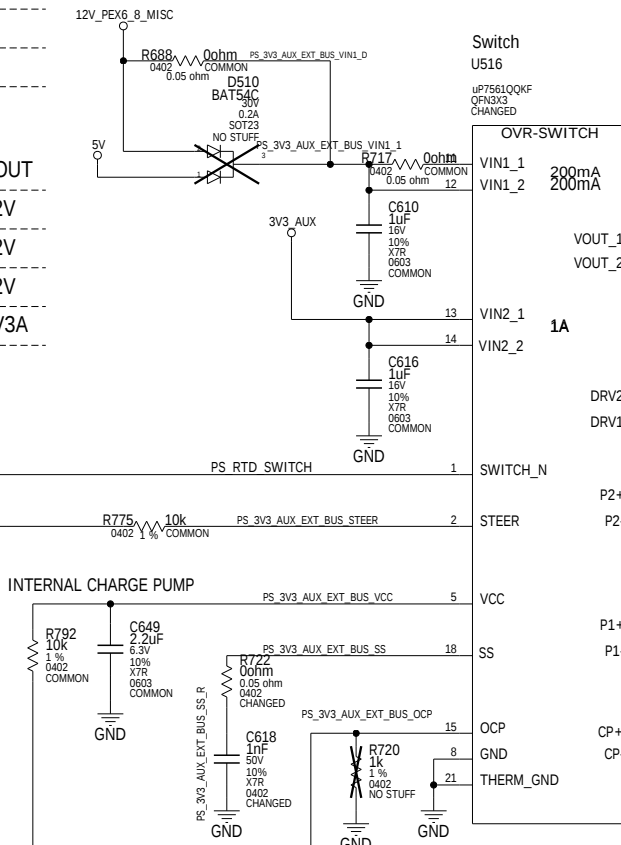
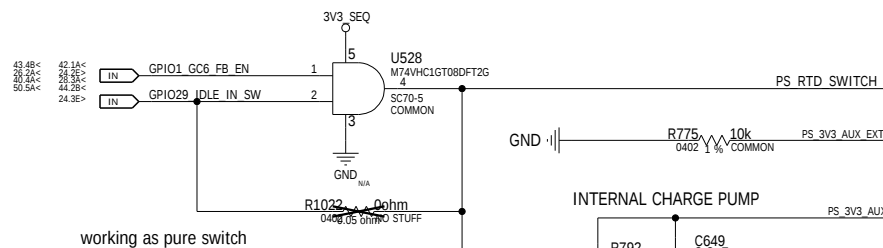
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Page41: 12V & 3V3_A SWITCHER

SWITCH	VOUT
0	VOUT = VIN1
1	VOUT = VIN2

AND GATE LOGIC			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V
0	1	0	12V
1	0	0	12V
1	1	1	3V3A



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PAGE DETAIL	PS: 12V & 3V3 A SWITCHER

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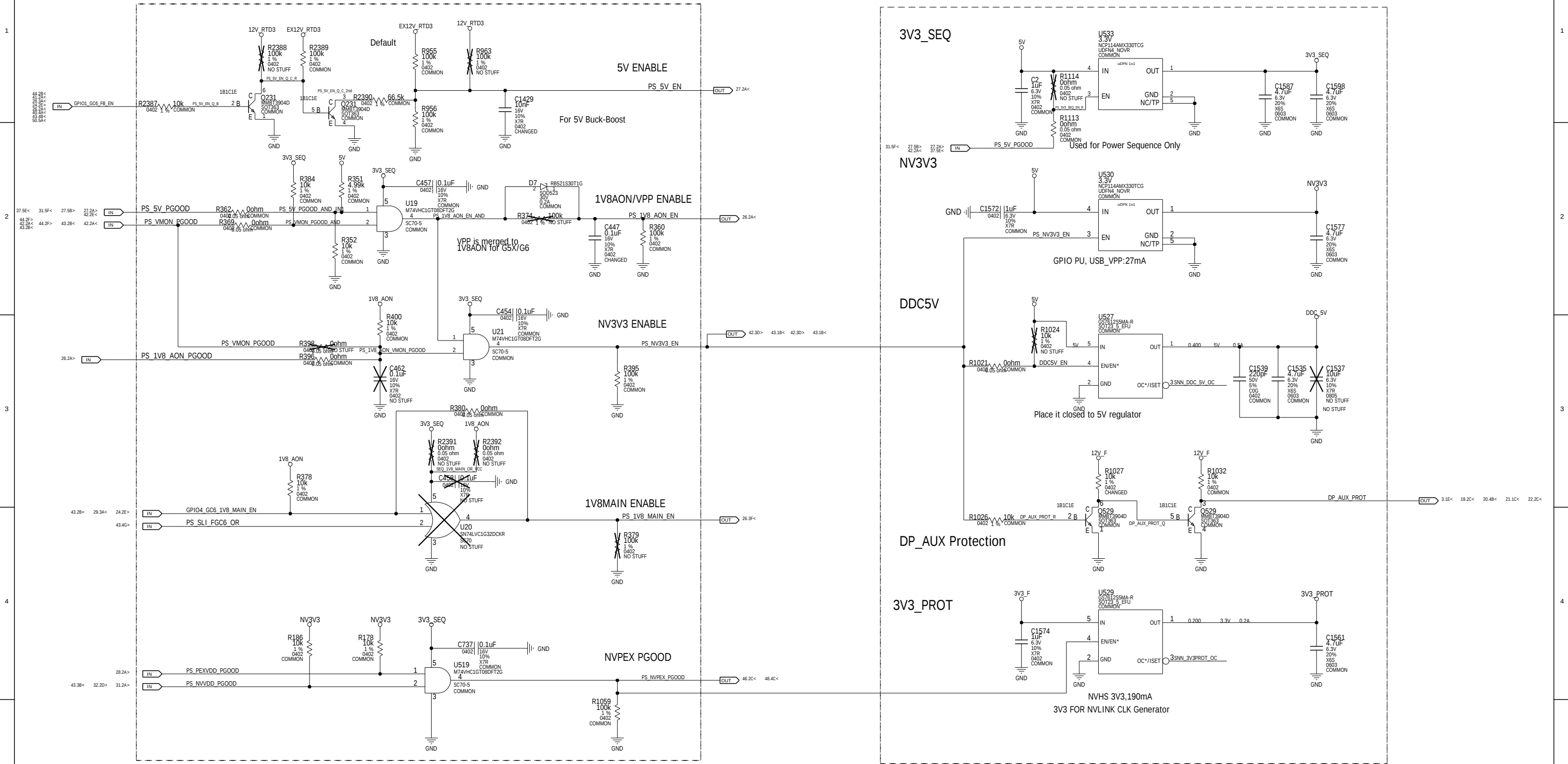
PCB REV	PG160-B02
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PAGE	41 OF 52
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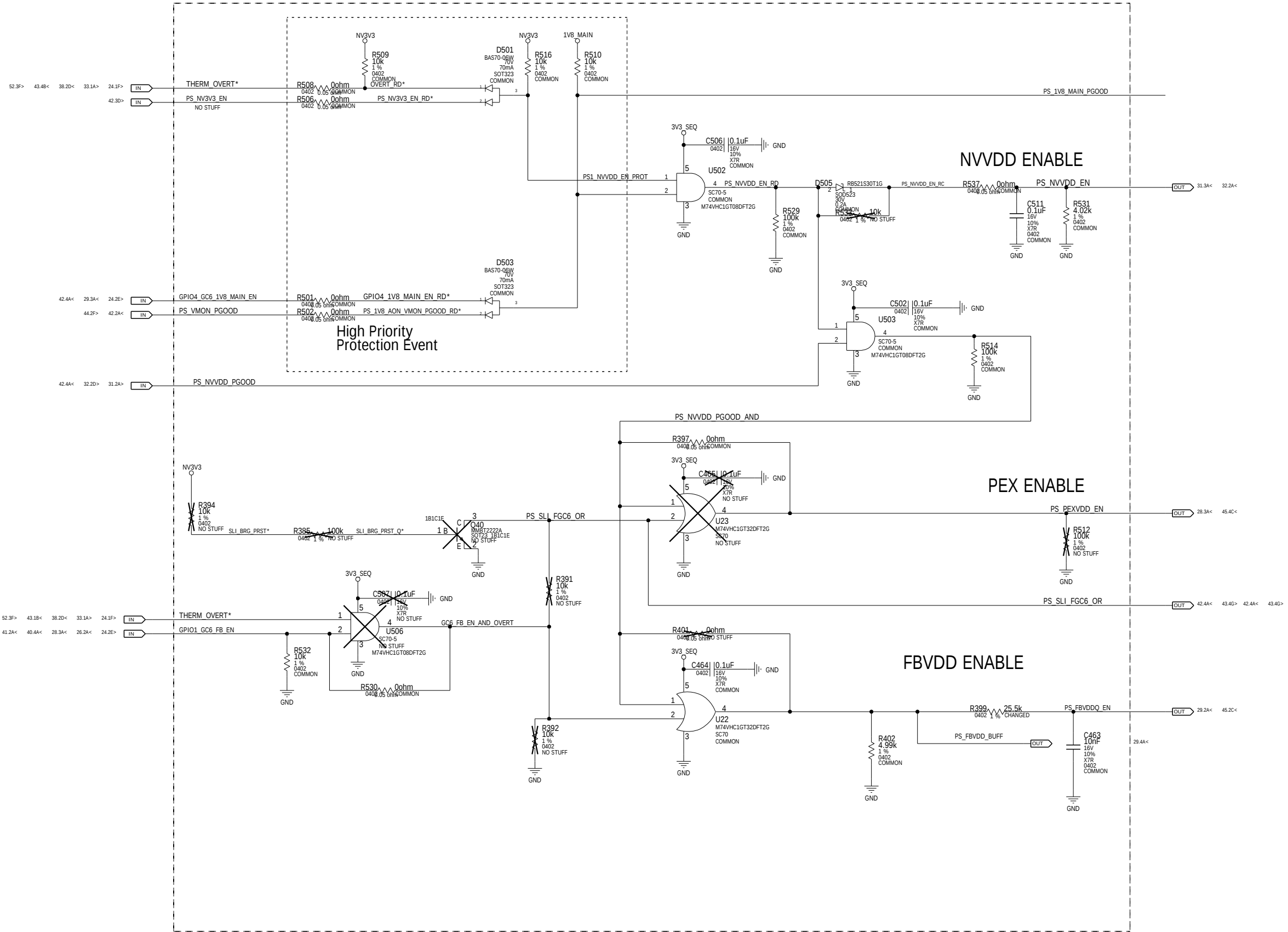
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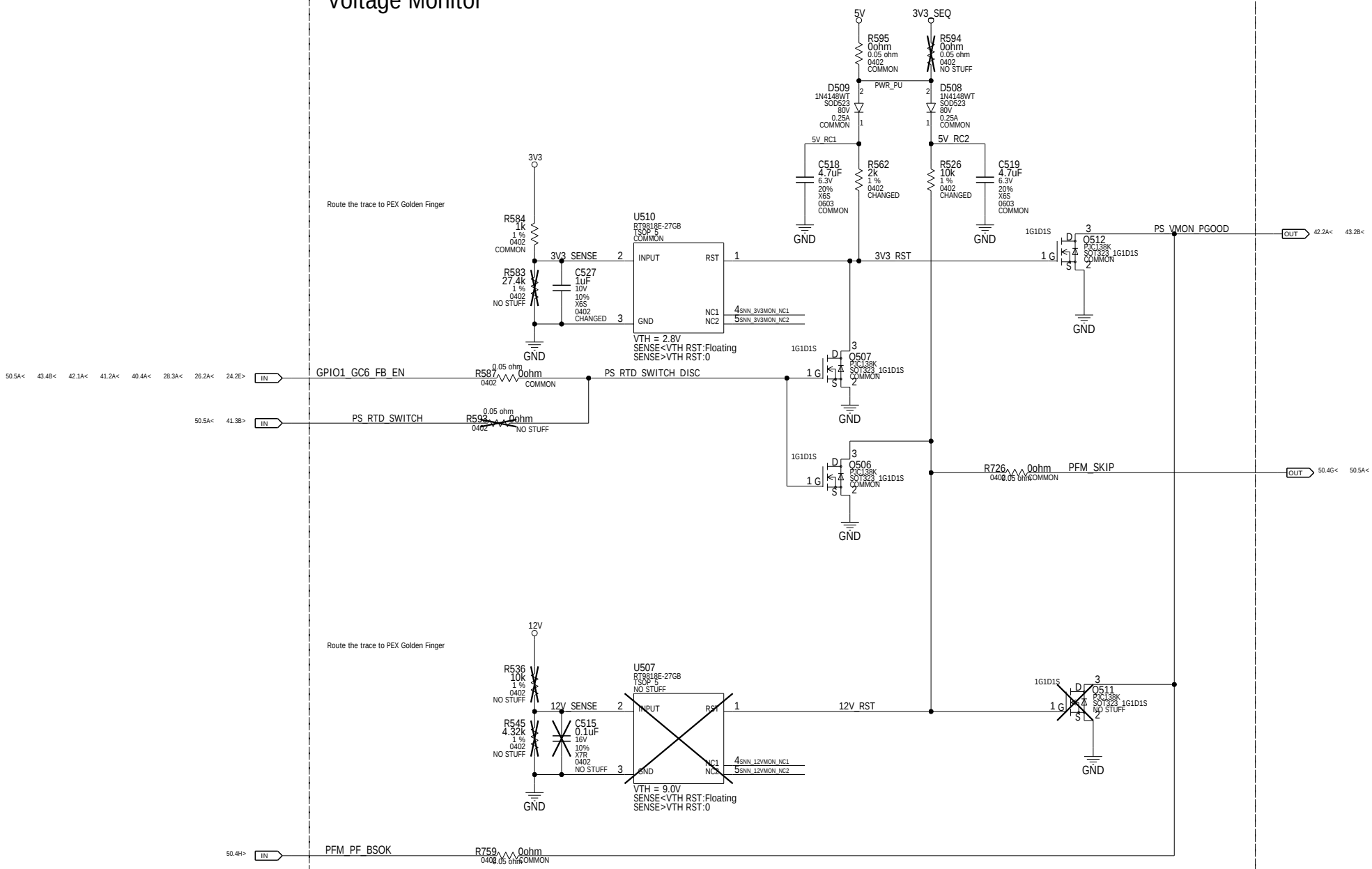
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NV_PN	600-1G160-0052-QS1		
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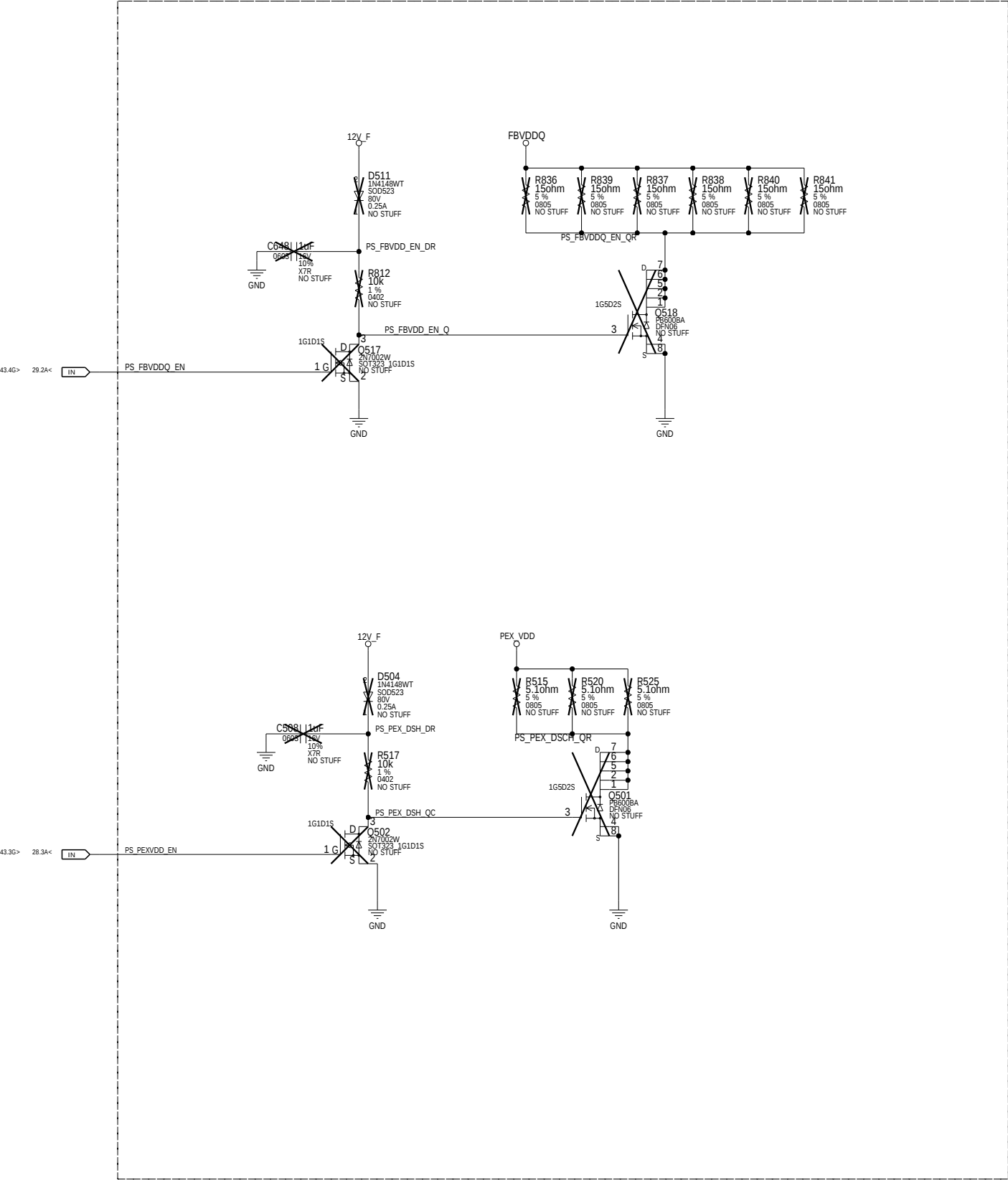
Voltage Monitor



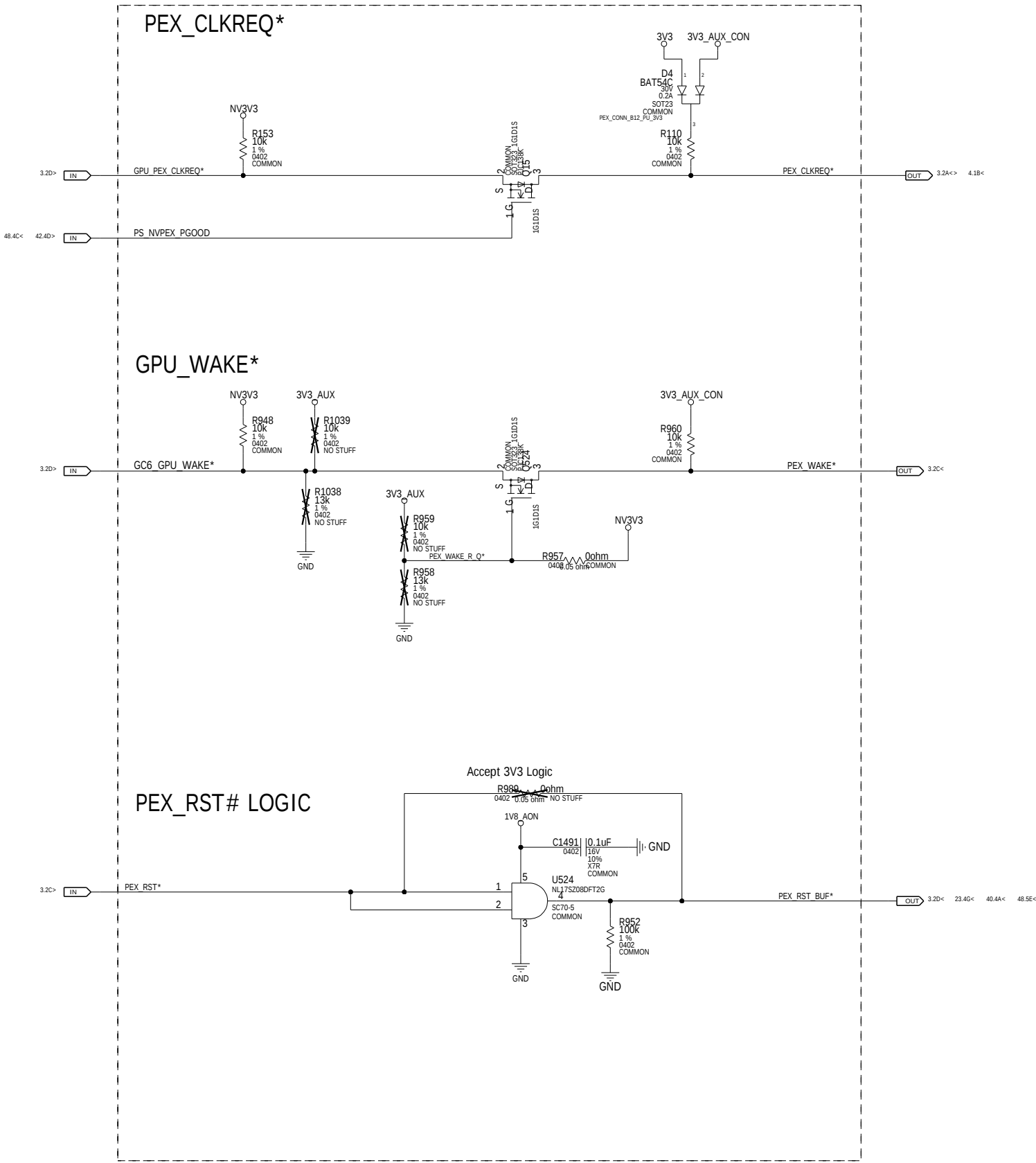
Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

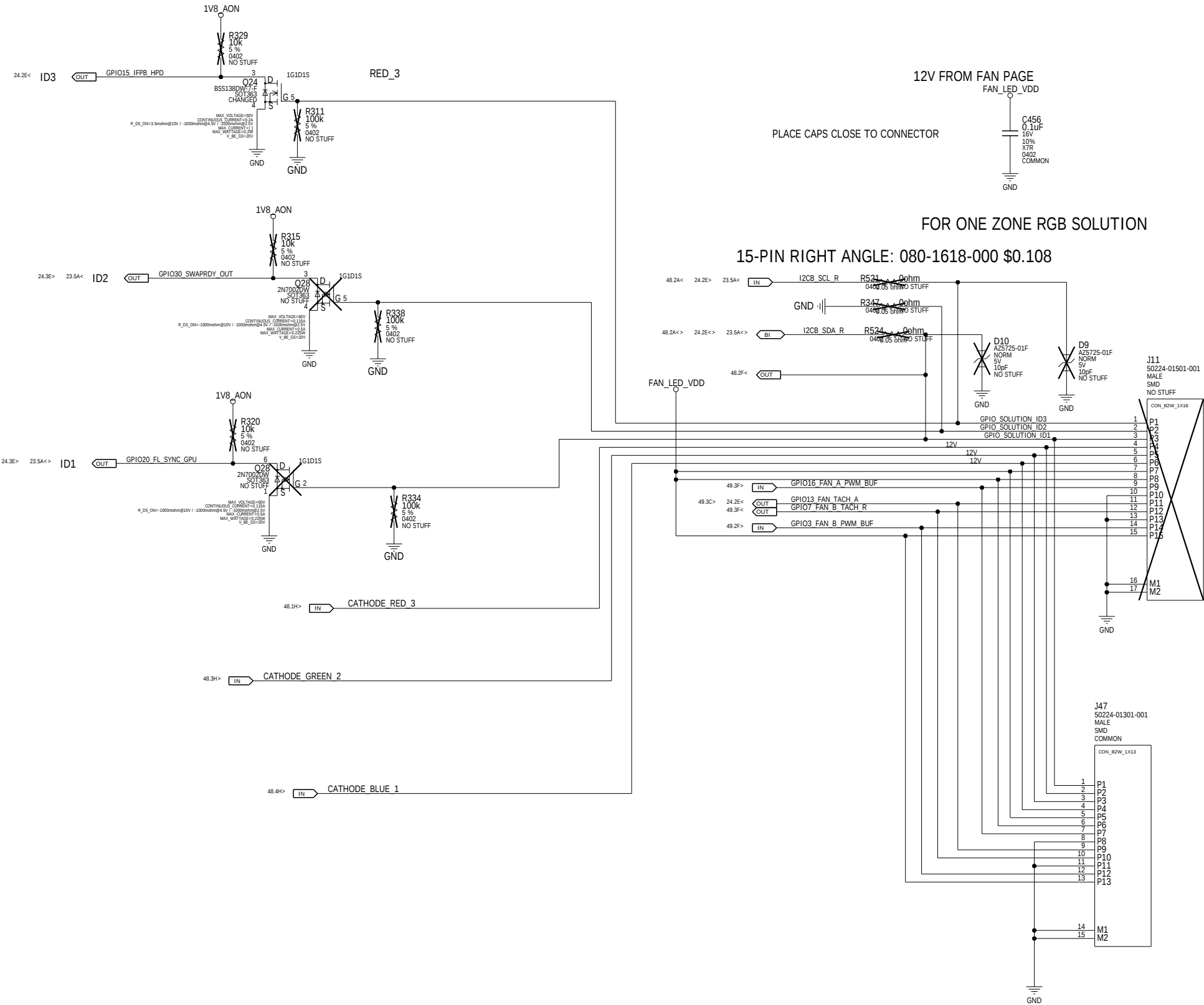


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For ONE ZONE RGB/cable	
PIN SEQ	Pin Name
1	ID3
2	ID2
3	ID1
4	DRIVE3/R
5	DRIVE2/G
6	DRIVE1/B
7	12V
8	12V
9	FAN_PWM1
10	GND
11	FAN_TACH1
12	FAN_TACH2
13	GND
14	FAN_PWM2
15	12V

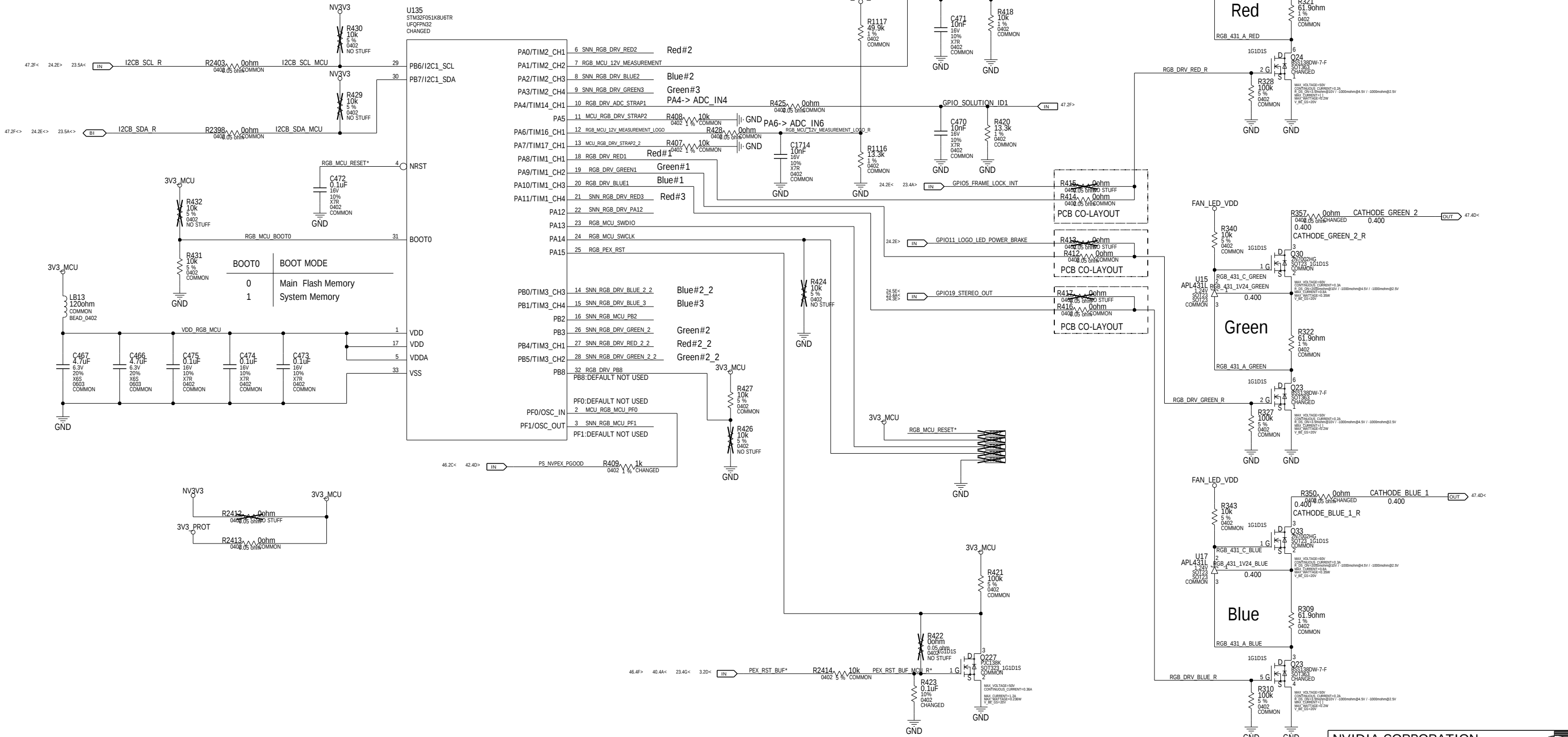


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Page48: LED DRIVER & Boost

8-bit I2C Address of MCU on GPU BOARD: 0x92

INPUT LEAKAGE CURRENT OF ADC_INx PINS: -0.2uA~0.2uA(max)



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PAGE DETAIL	LED DRIVER & BOOST

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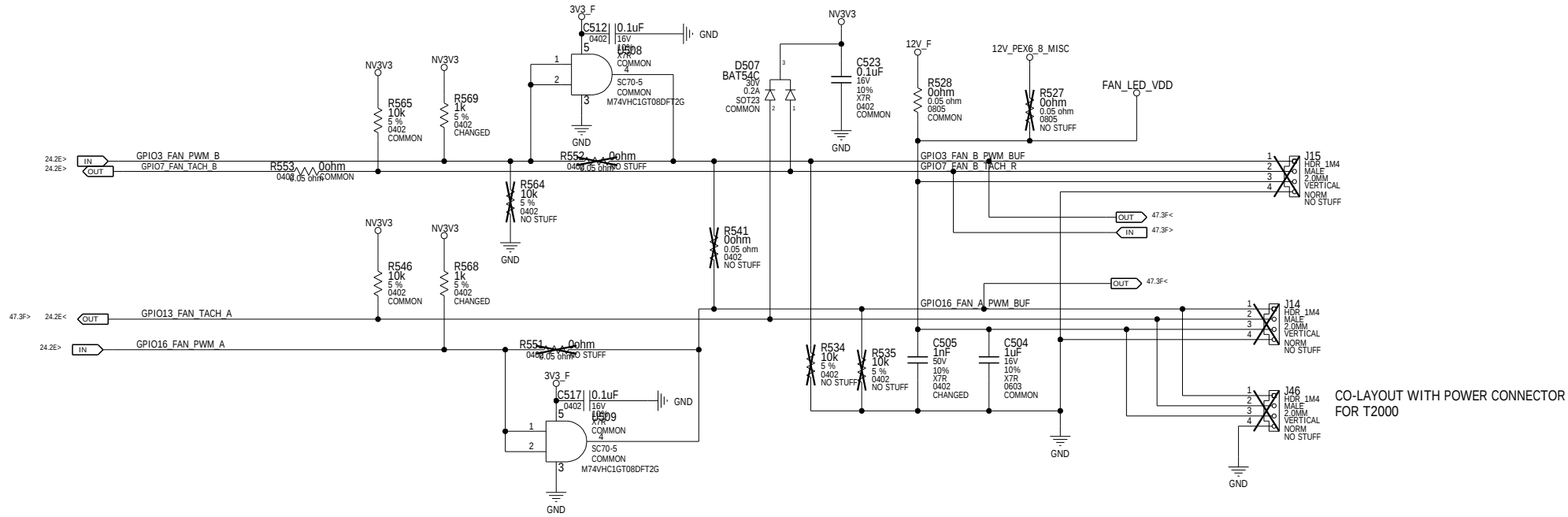
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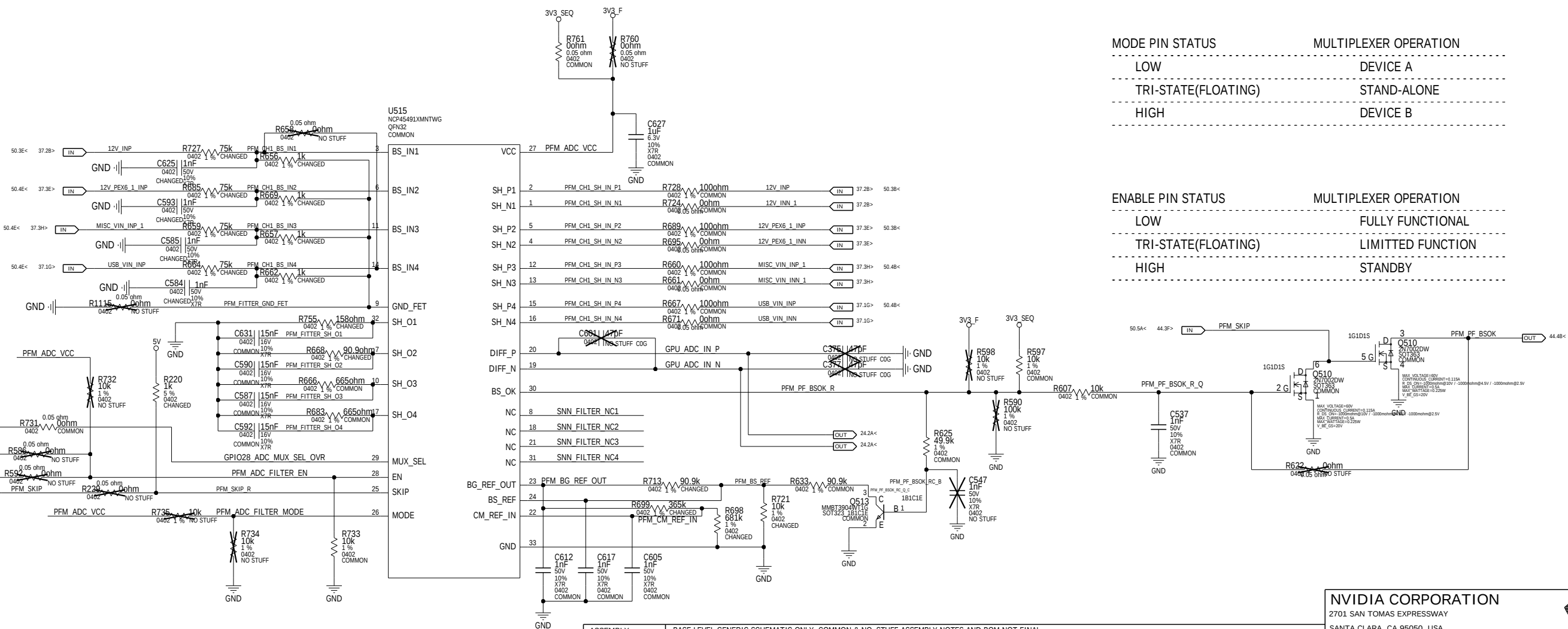
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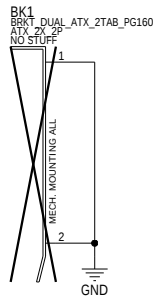


MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

Brackets:



MOUNTING HOLES FOR HS:

