

PG160-B02

8GB GDDR6, 256b, X16

Tall DVI-D + USBC/DP + DP + HDMI/DP + DP

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NV_PN

600-1G160-BASE-300

PCB REV

PG160-B02

BOM REV

A

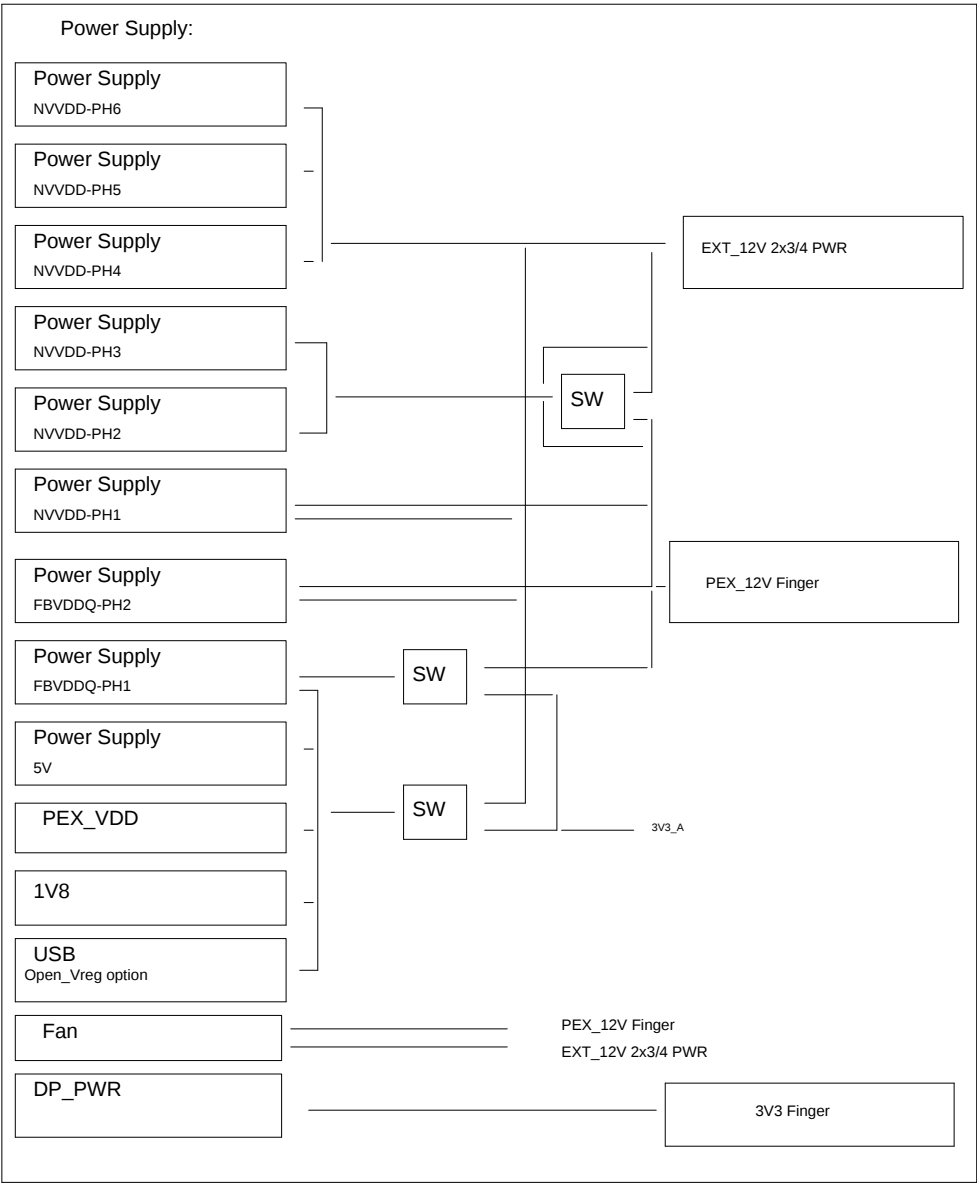
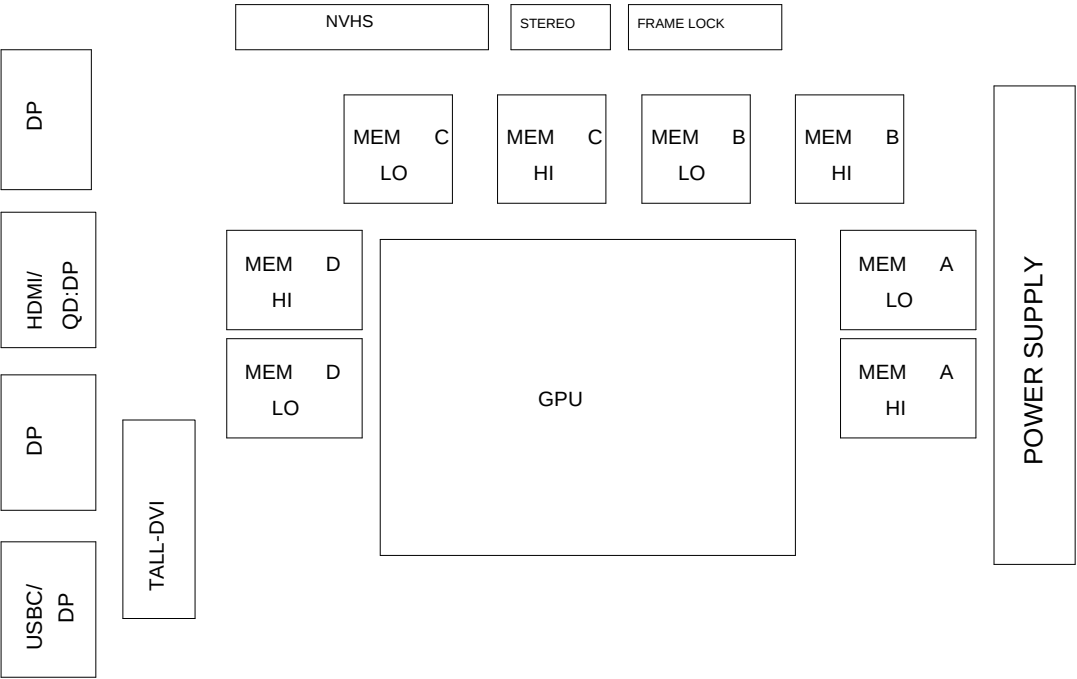
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DATE

21-JUN-2018

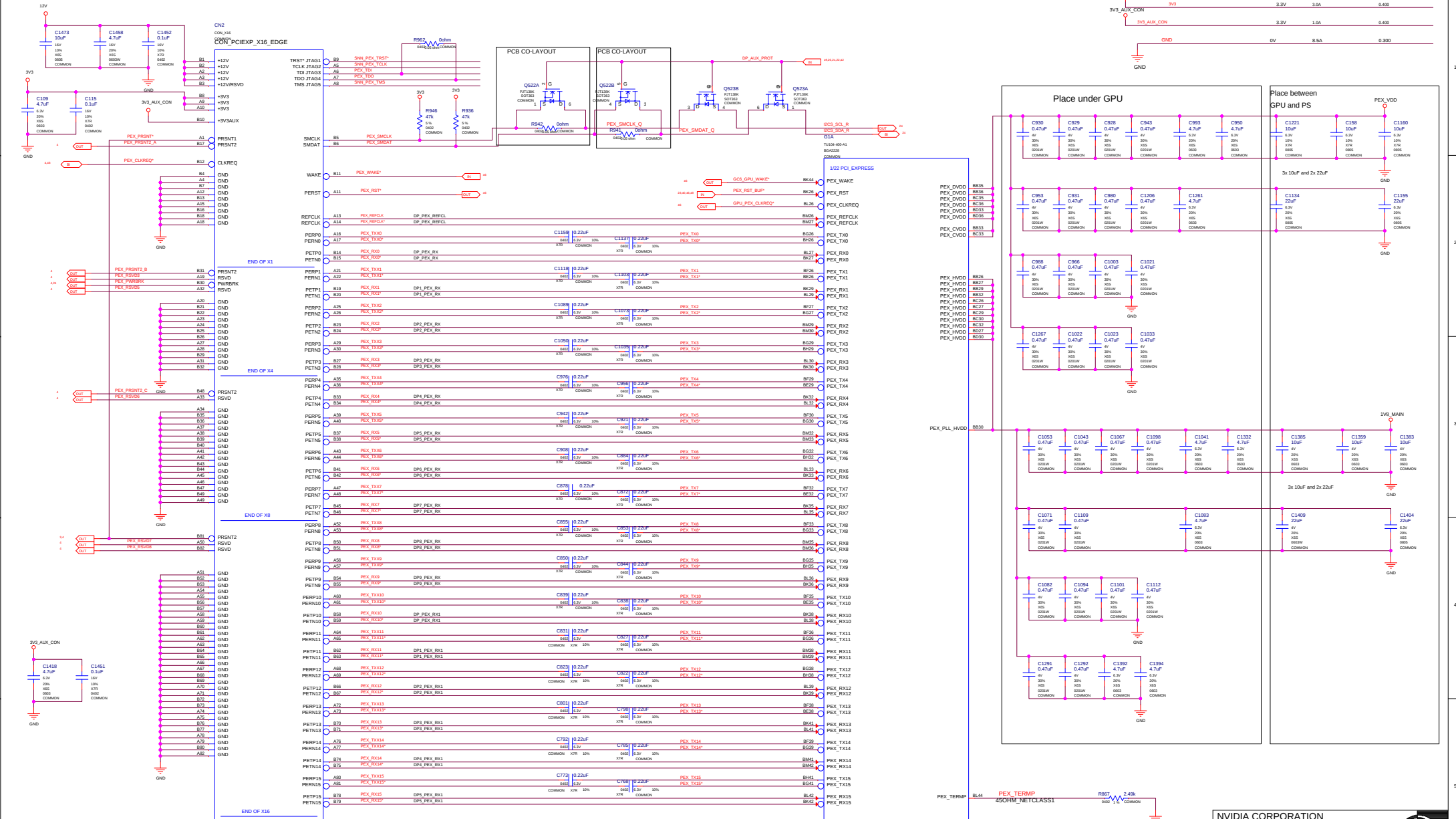




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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	Block Diagram

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NV_PN	600-1G160-BASE-300	PAGE	2 OF 52
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BCM REV	A		

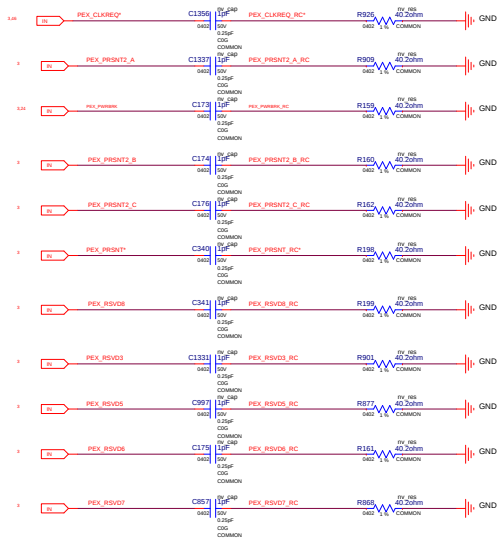


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PAGE DETAIL	PCI Express

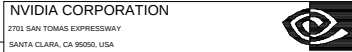
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BOM REV		A		DATE 21-JUN-2018

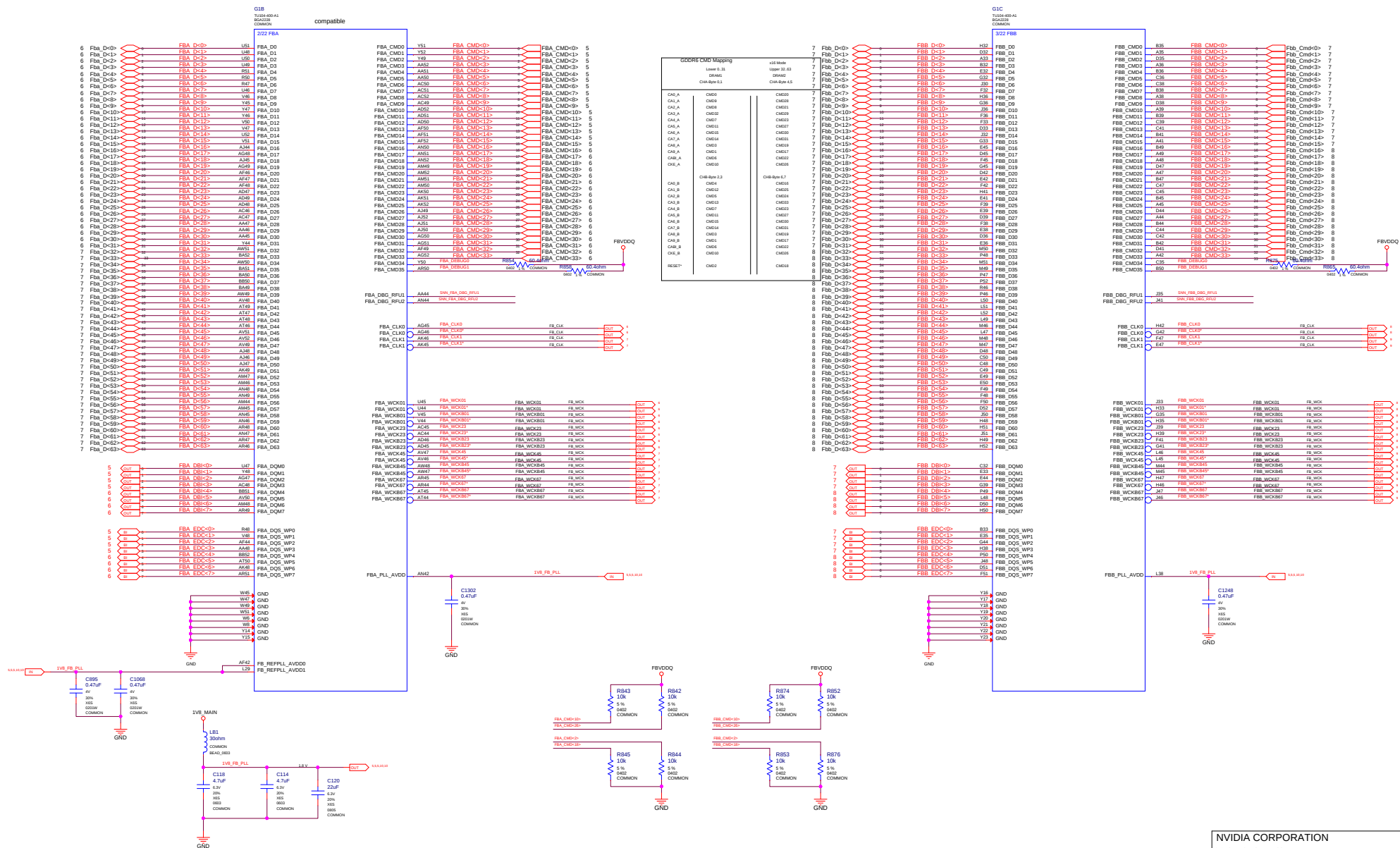




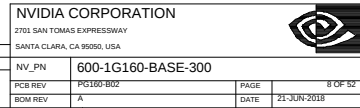
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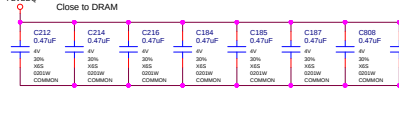
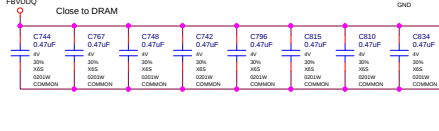
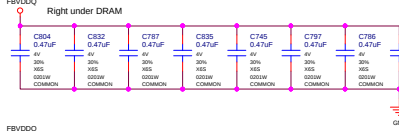
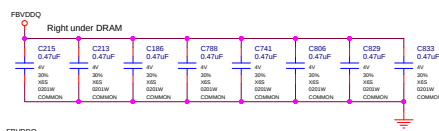
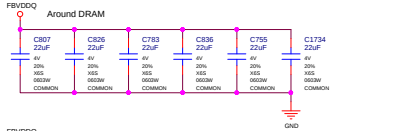
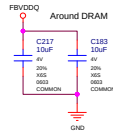
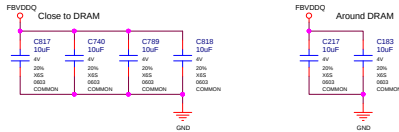
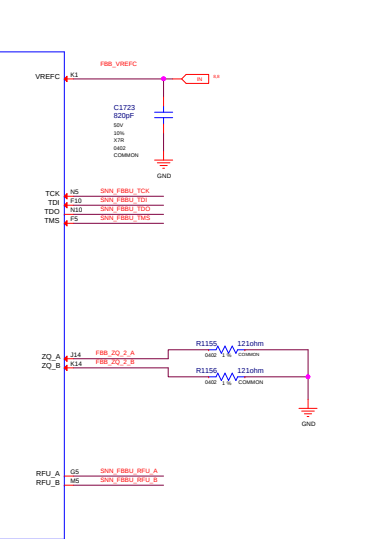
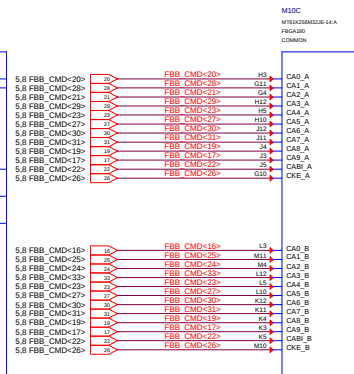
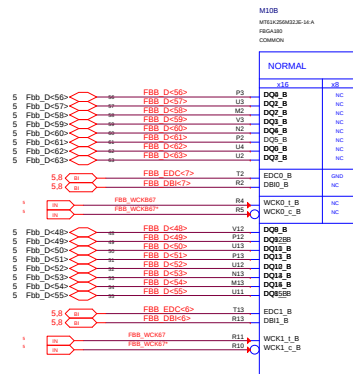
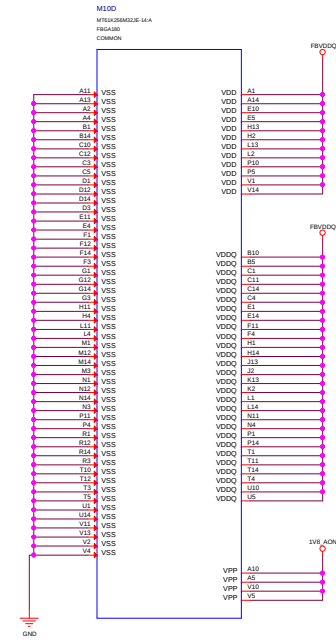


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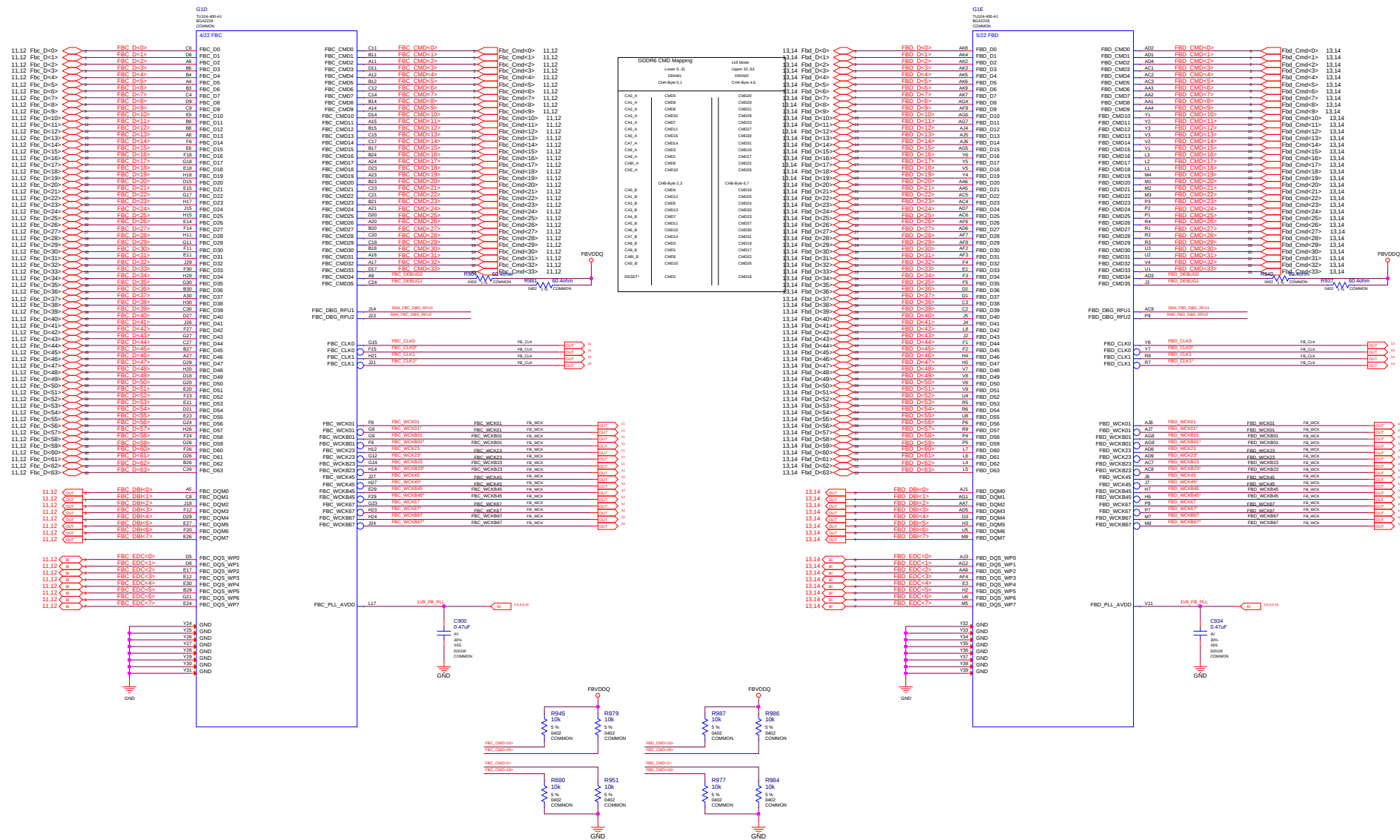


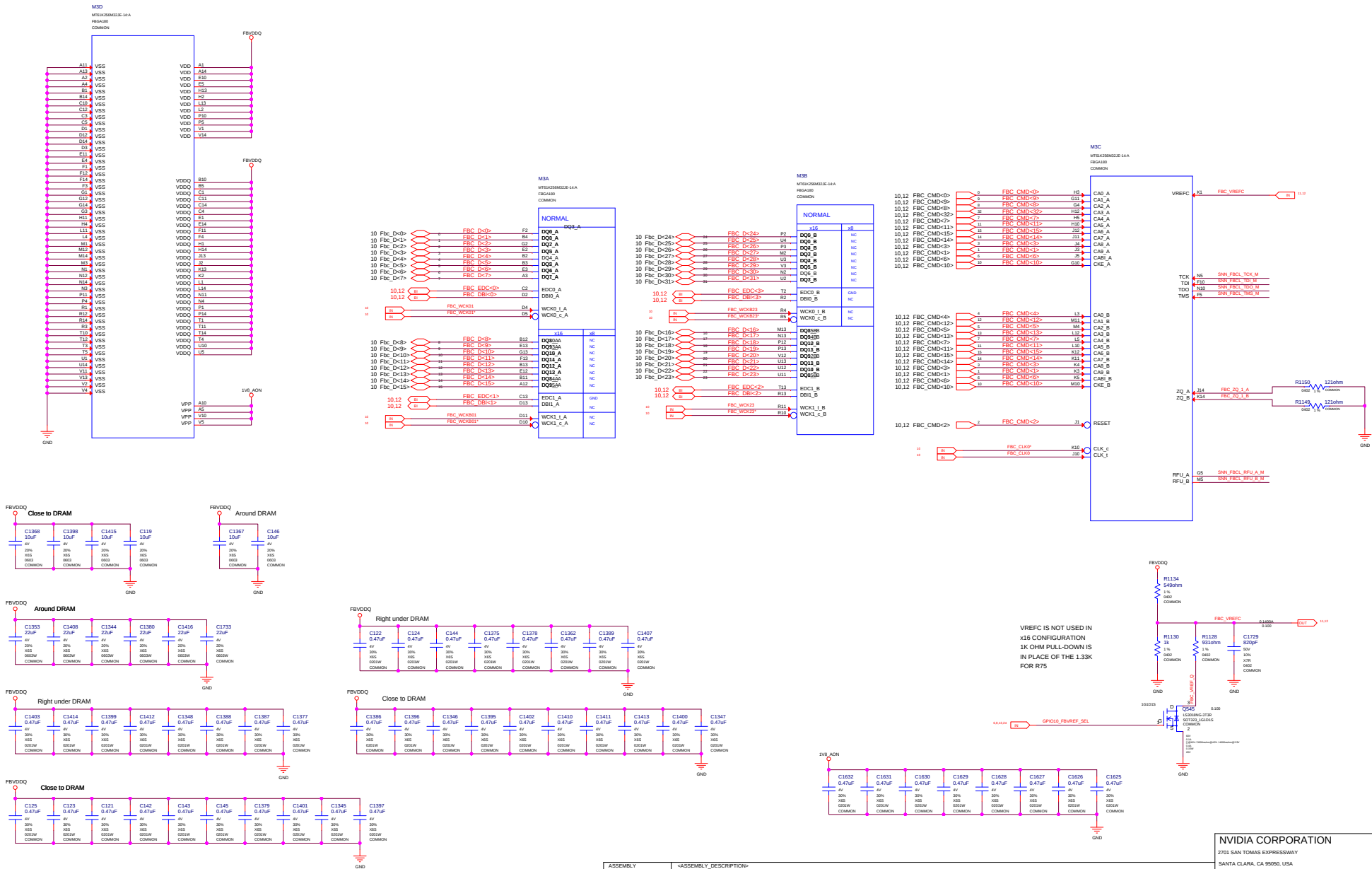
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ASSEMBLY	<ASSEMBLY DESCRIPTION>
PAGE DETAIL	MEMORY: FBB[63..32]

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INV_PN	600-1G160-BASE-300		
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PAGE DETAIL	MEMORY: FBC[31:0]

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NV_PN	600-1G160-BASE-300
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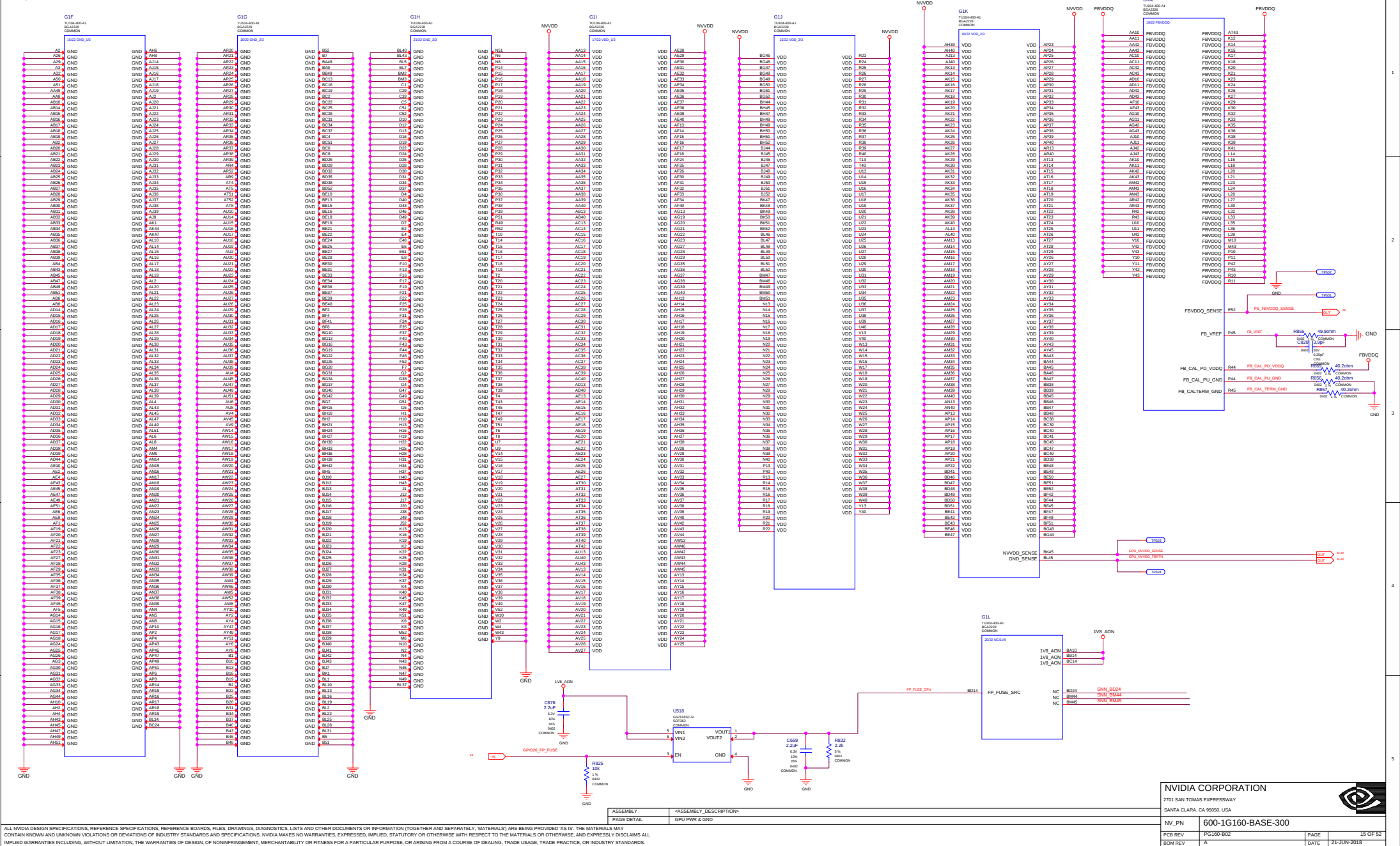
VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R62

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PCB REV	PG160-B02
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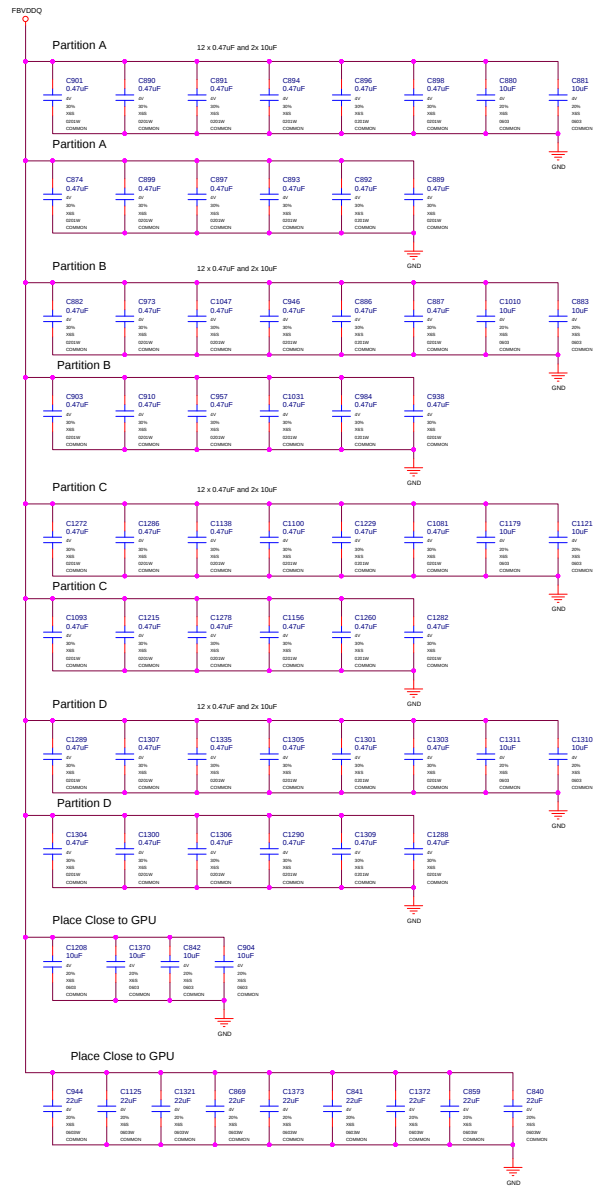
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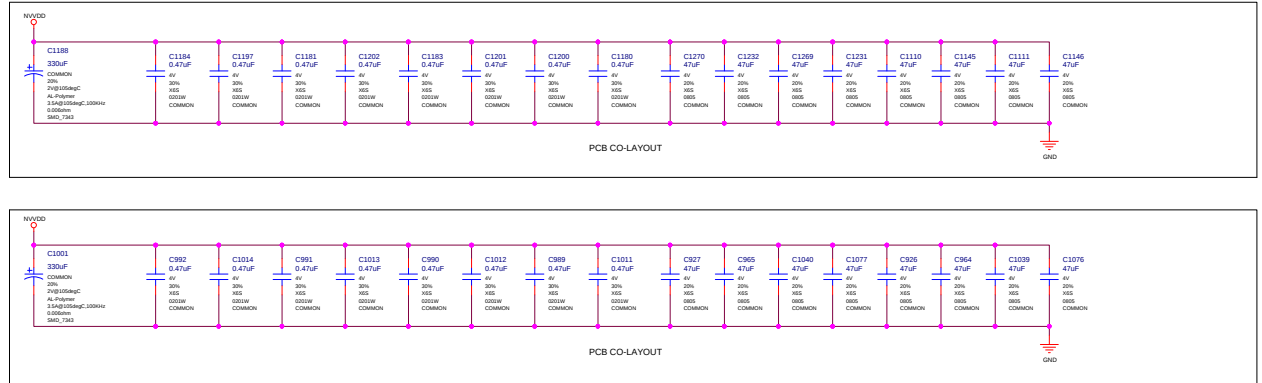


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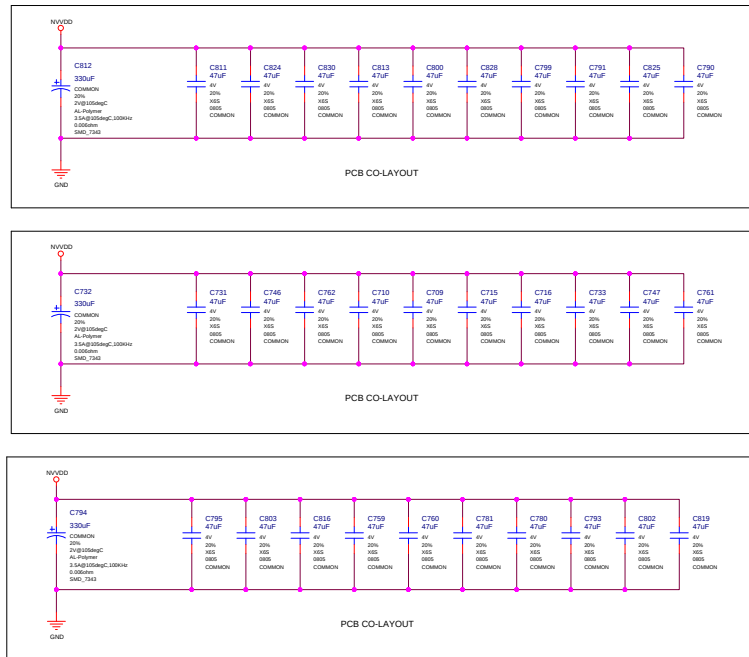
FBVDDQ



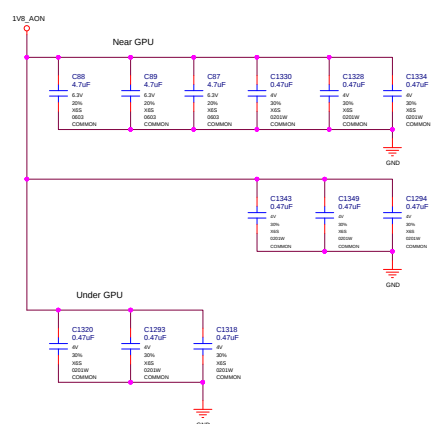
Under GPU



Near GPU



1V8_AON



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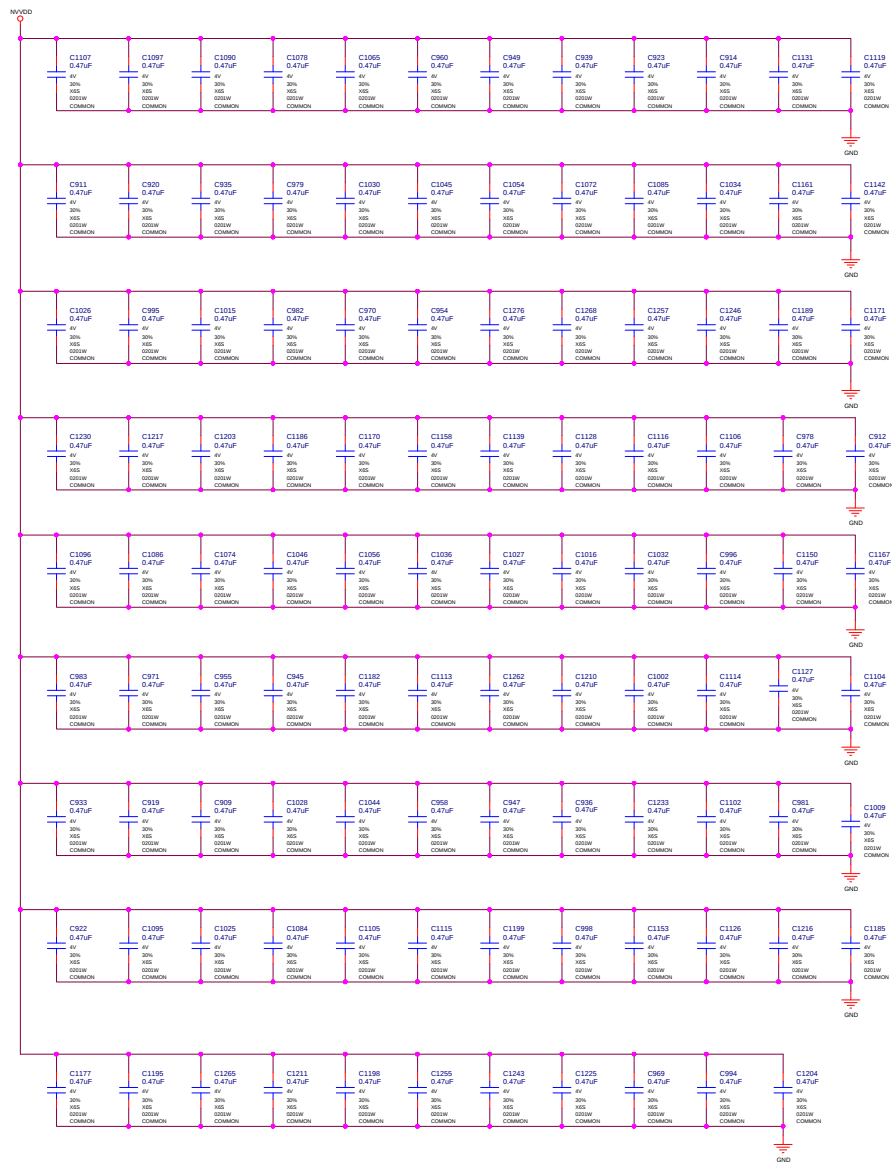
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PAGE DETAIL	GPU Decoupling

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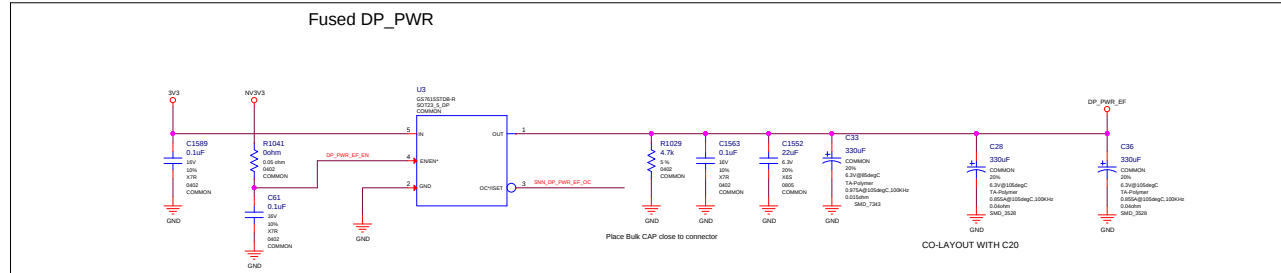
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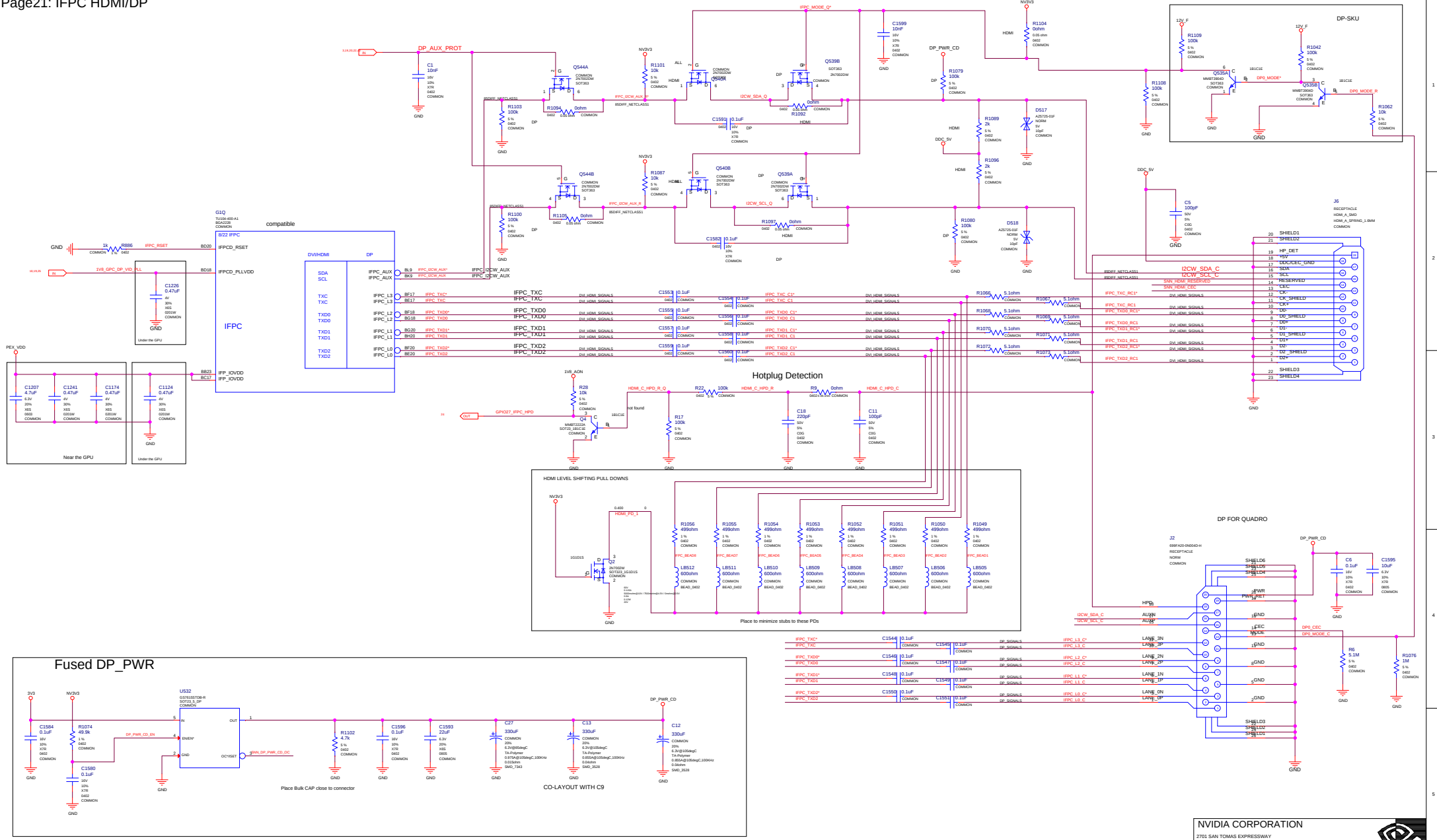
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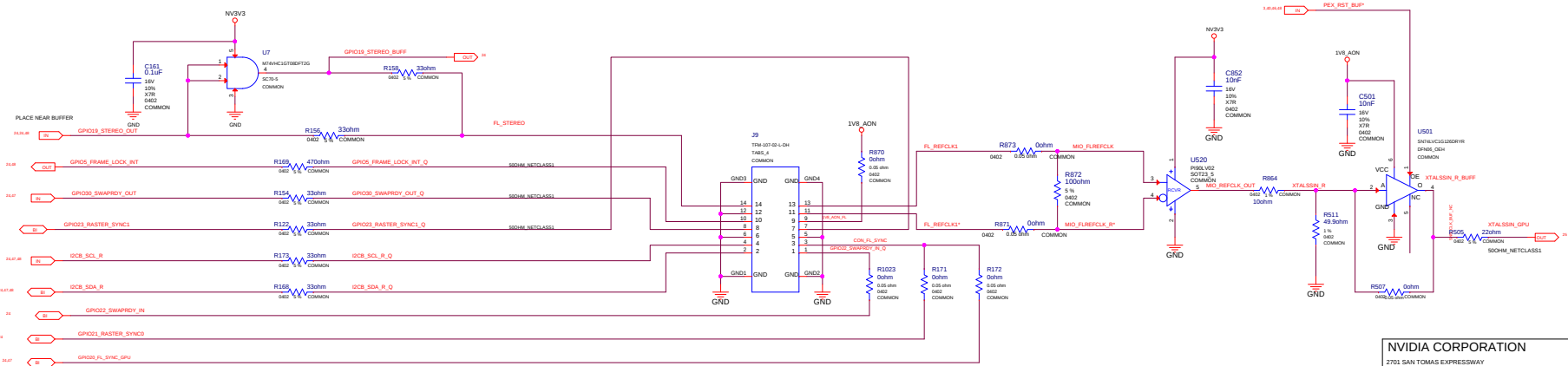
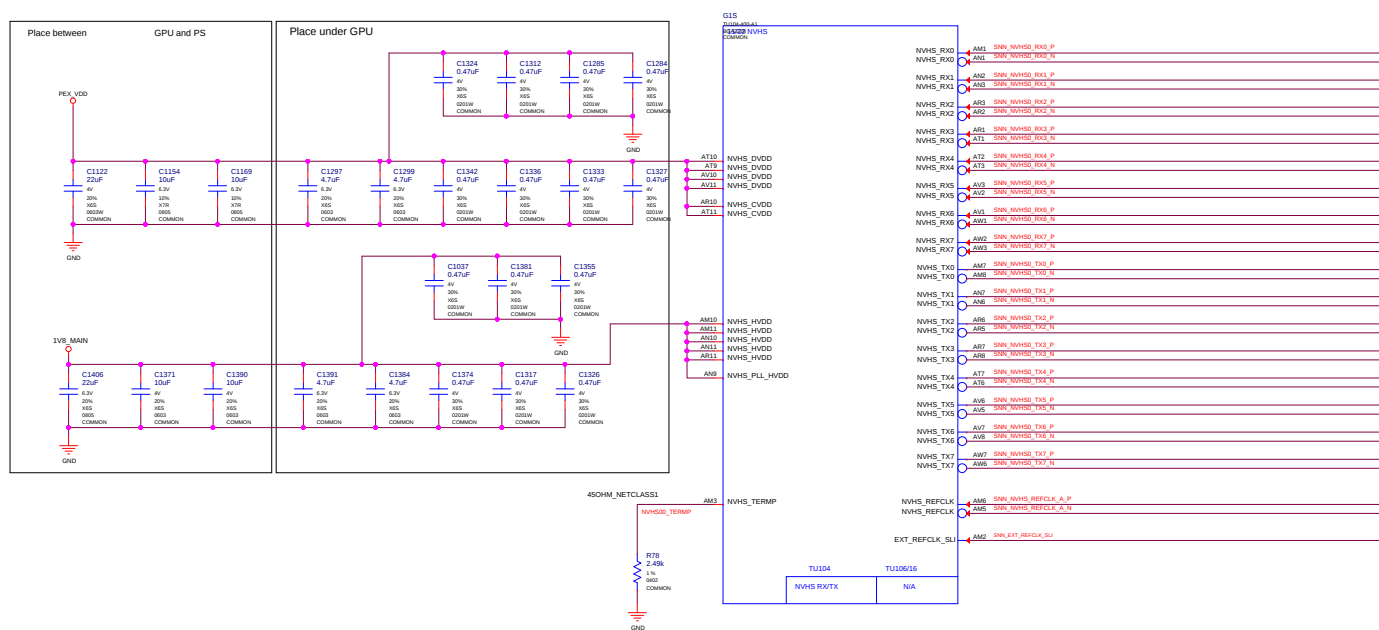


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PAGE DETAIL	IO: IFPE DP

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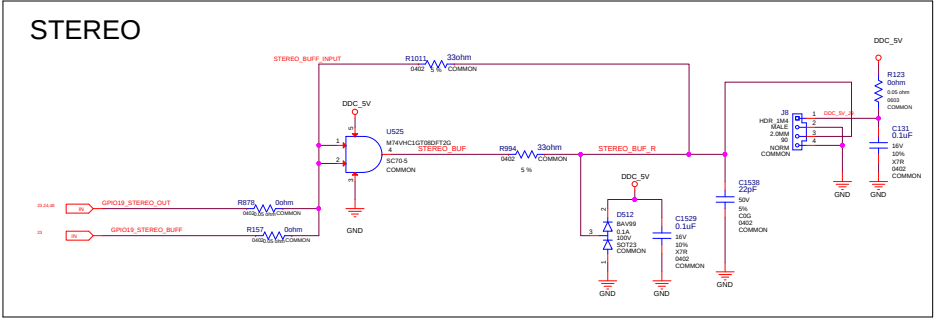
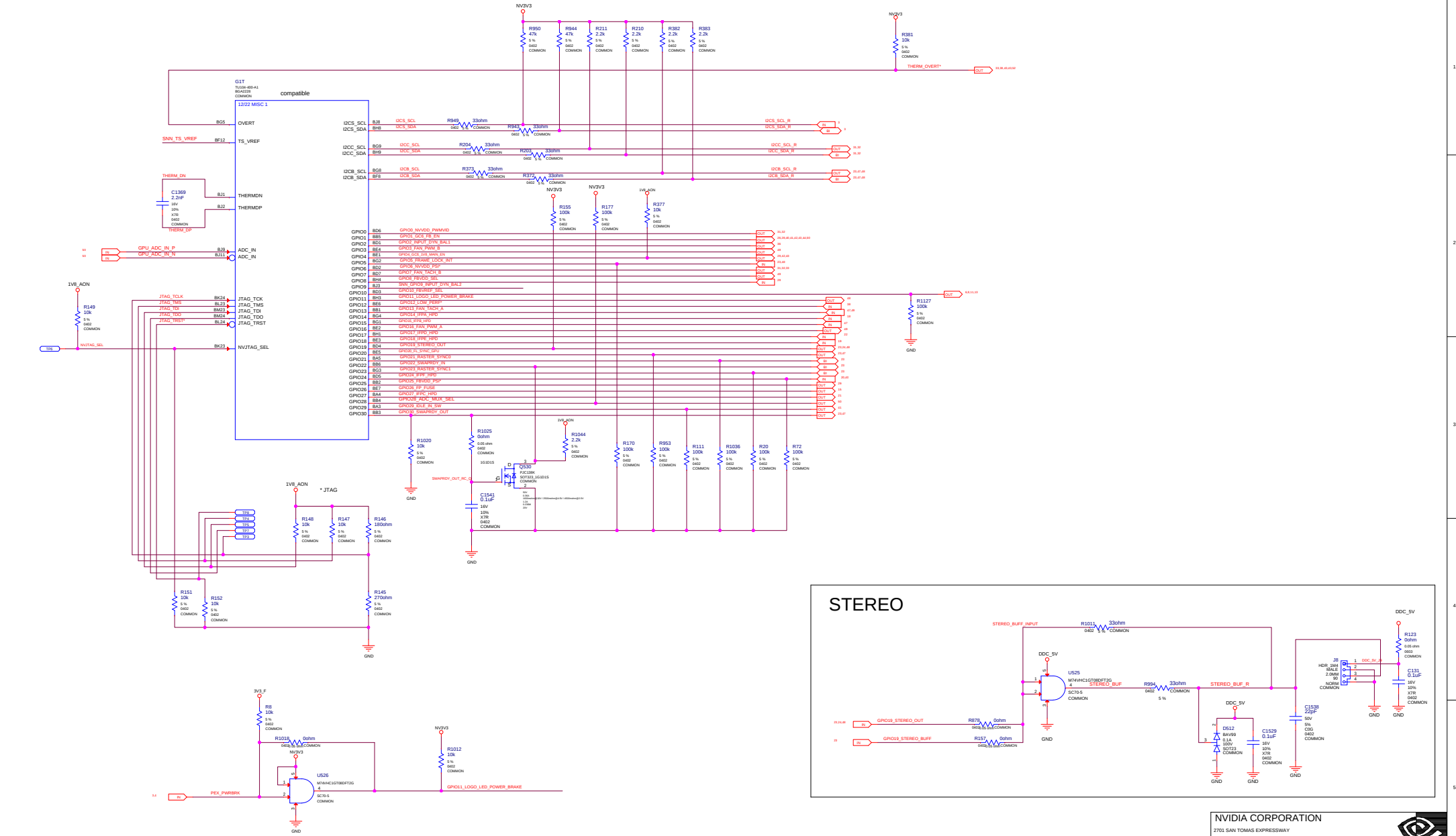
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: NVHS Interface and Frame Lock

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e25: MISC2: ROM, XTAL, Straps			
STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	H	L	00110
H	H	H	00111
L	L	M	01000

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR	DIE
00000	8Gb	256-bit	Samsung	C
00001	8Gb	256-bit	Micron	A
00010	8Gb	256-bit	Hynix	M
00011	8Gb	256-bit	Samsung	C
00100	8Gb	256-bit	Micron	A
00101	8Gb	256-bit	Hynix	M
00110	16Gb	256-bit	Samsung	M
00111				

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]_FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

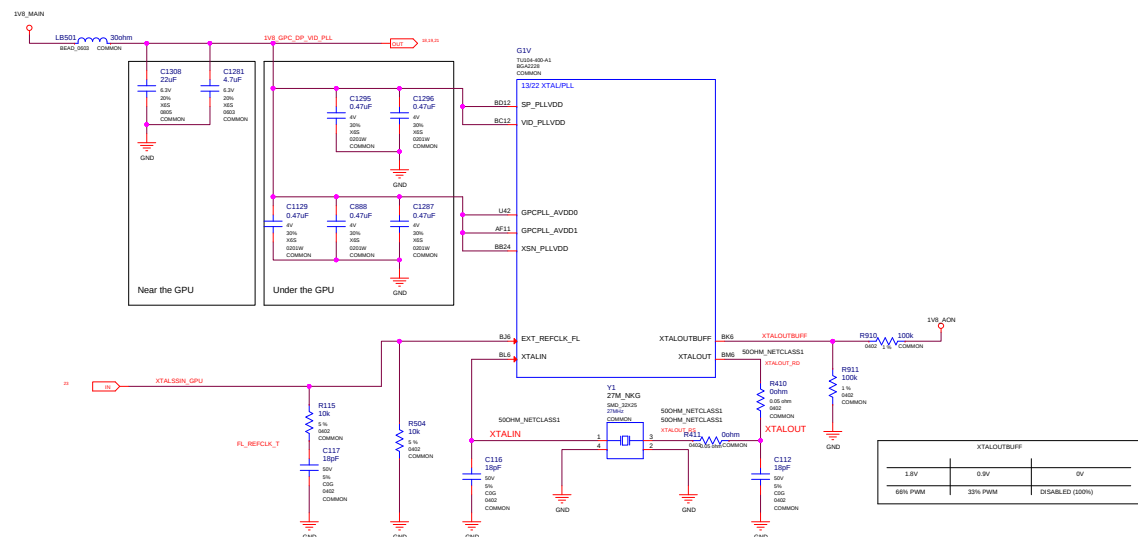
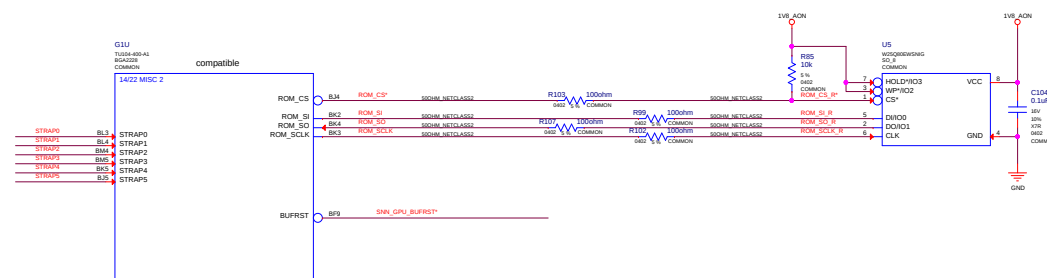
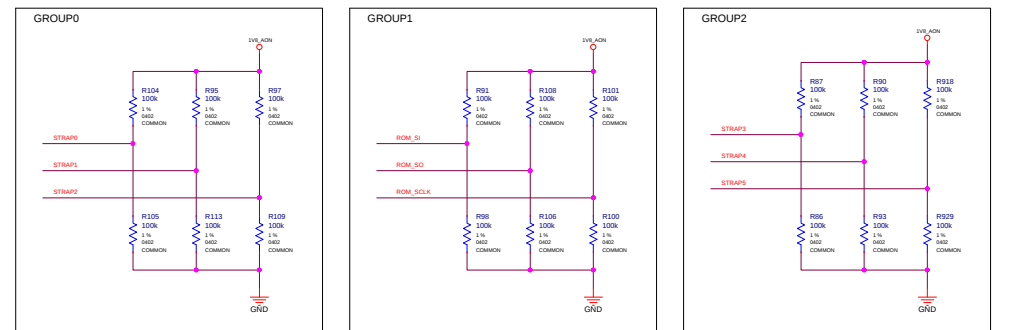
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



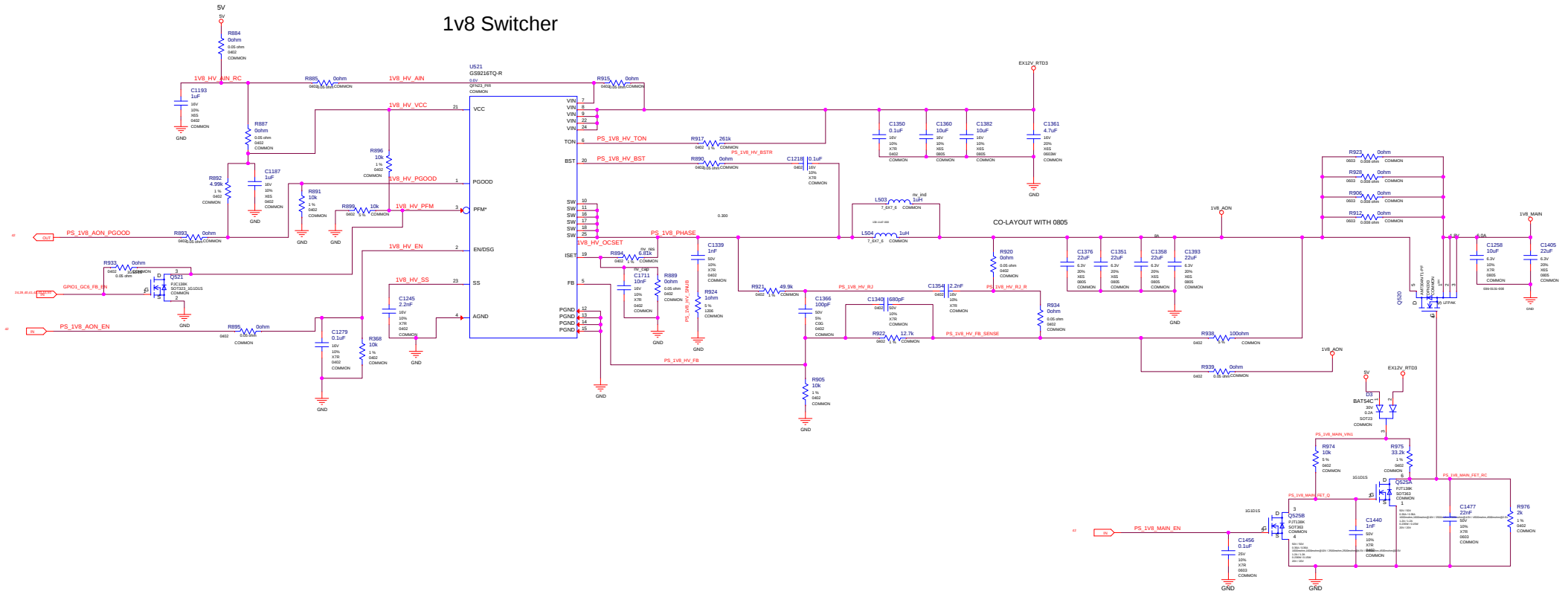
XTALOUTBUFF		
1.8V	0.9V	0V
66% PWM	33% PWM	DISABLED (100%)

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: ROM, XTAL, STRAPS

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NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN PCB REV BOM REV	600-1G160-BASE-300 PG160-B02 A	PAGE DATE	25 OF 52 21-JUN-2018





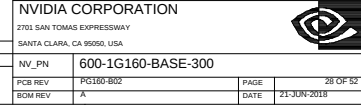
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NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
NV_PN		600-1G160-BASE-300		
PCB REV	PG160-802	PAGE	26 OF 52	
BOM REV	A	DATE	21-JUN-2018	

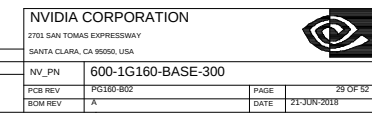


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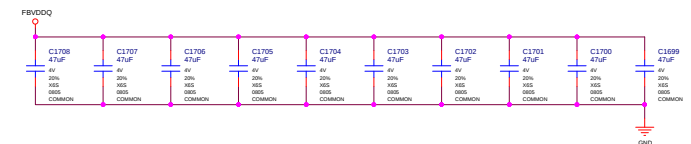
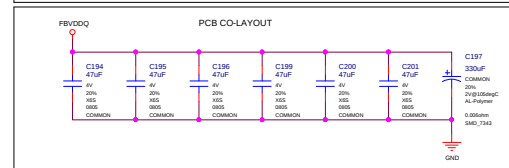
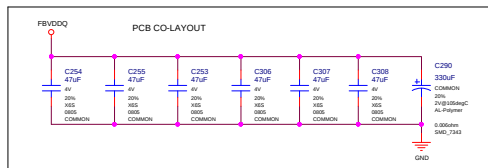
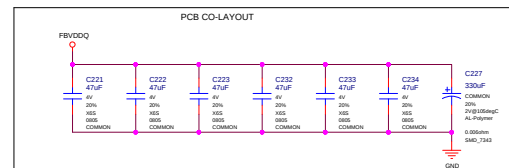
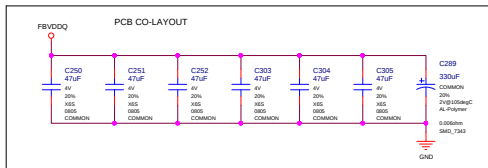
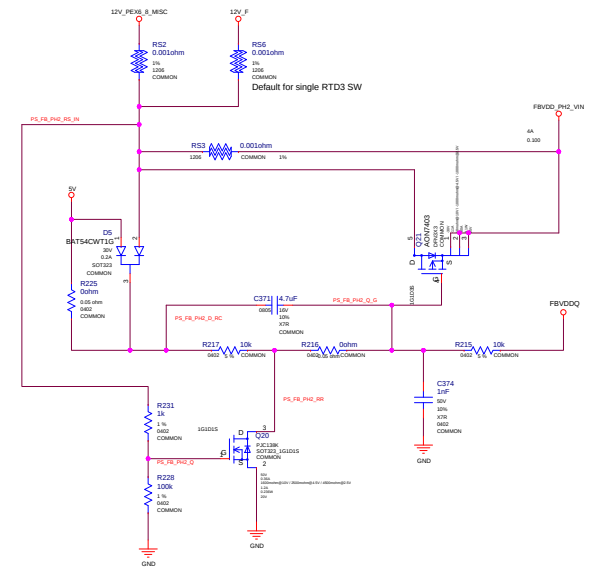
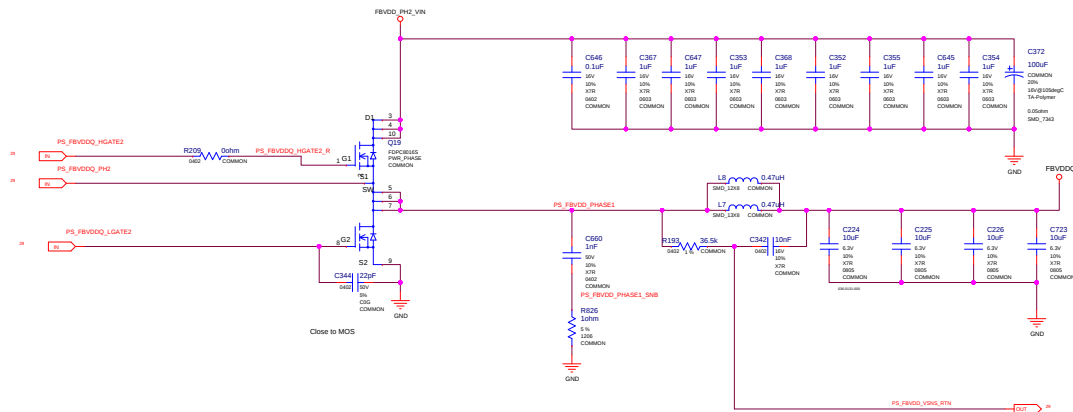
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
NV_PN		600-1G160-BASE-300		
PCB REV	A160-B02	PAGE	27 OF 52	
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ASSEMBLY		<ASSEMBLY_DESCRIPTION>		SANTA CLARA, CA 95050, USA	
PAGE DETAIL		PS: PEYVDD		NV_PN 600-1G160-BASE-300	
SALES MAY EXPRESSLY DISCLAIMS ALL INDUSTRY STANDARDS.				PCB REV PG160-802	PAGE 28 OF 52
				BOM REV A	DATE 21-JUN-2019

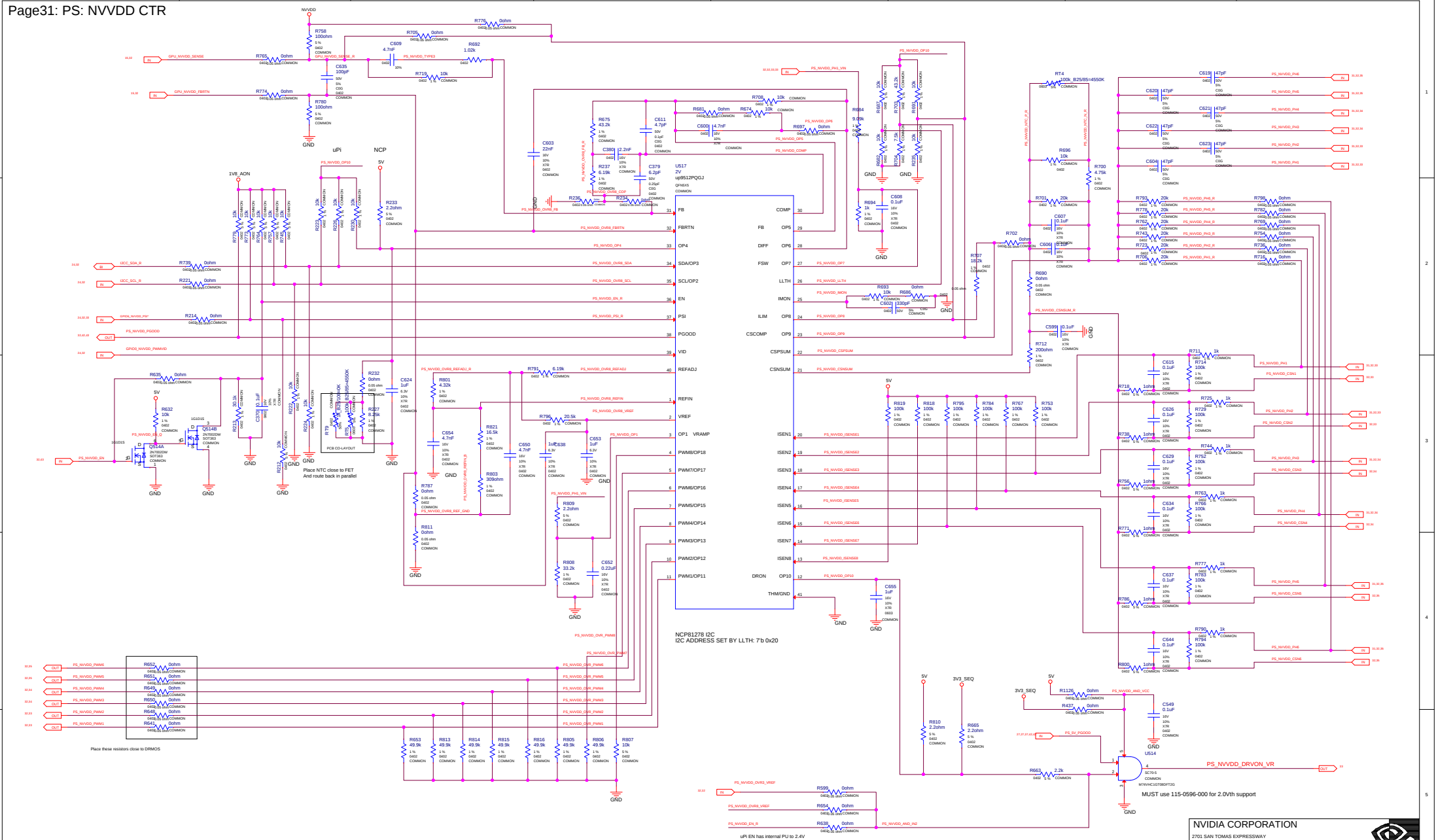


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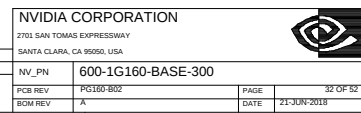


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Controller

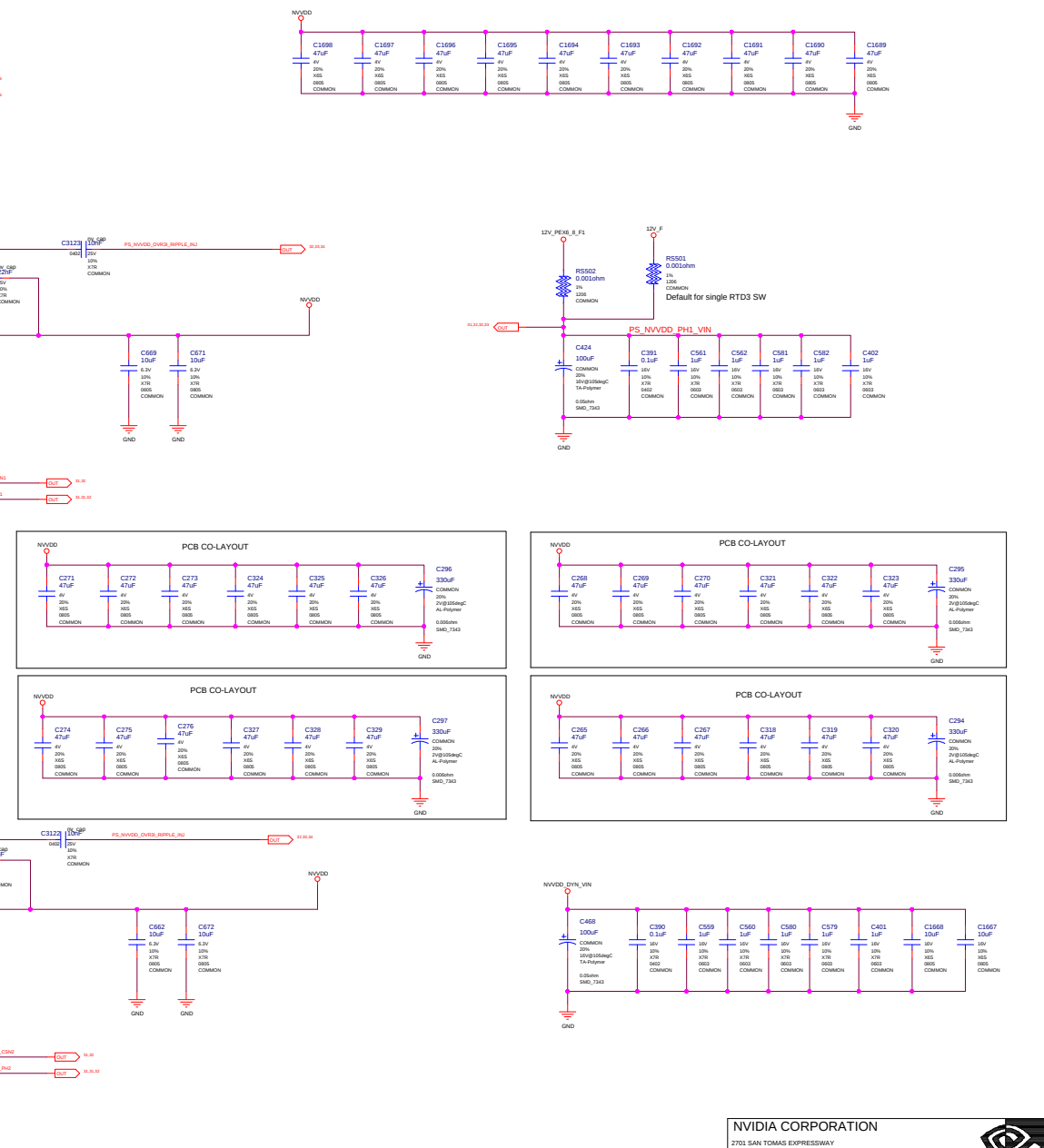
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NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
NV_PN		600-1G160-BASE-300		
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ASSEMBLY		<ASSEMBLY_DESCRIPTION>		SANTA CLARA, CA 95050, USA													
PAGE DETAIL		PS: NVDD Controller (VR3)		<table border="1"> <tr> <td>NV_PN</td> <td colspan="5">600-1G160-BASE-300</td> </tr> </table>		NV_PN	600-1G160-BASE-300										
NV_PN	600-1G160-BASE-300																
SALES MAY EXPRESSLY DISCLAIMS ALL LIABILITY STANDARDS.				<table border="1"> <tr> <td>PCB REV</td> <td>PG160-802</td> <td>PAGE</td> <td colspan="3">32 OF 52</td> </tr> <tr> <td>BOM REV</td> <td>A</td> <td>DATE</td> <td colspan="3">21-JUN-2019</td> </tr> </table>		PCB REV	PG160-802	PAGE	32 OF 52			BOM REV	A	DATE	21-JUN-2019		
PCB REV	PG160-802	PAGE	32 OF 52														
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NV_PN	600-1G160-BASE-300		
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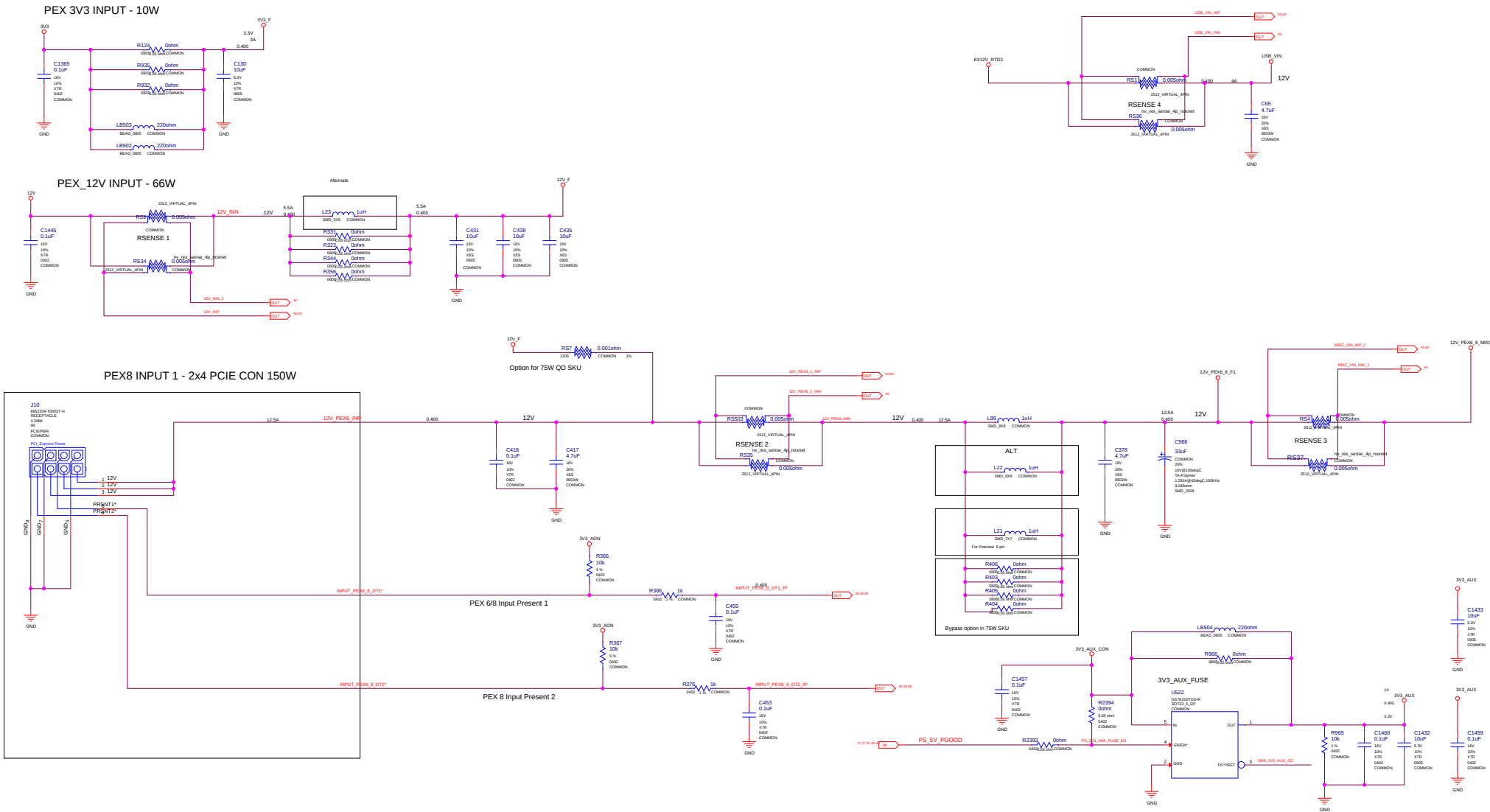
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NV_PN	600-1G160-BASE-300		
PCB REV	PG160-B02	PAGE	34 OF 52
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Input, Filtering, and Monitoring

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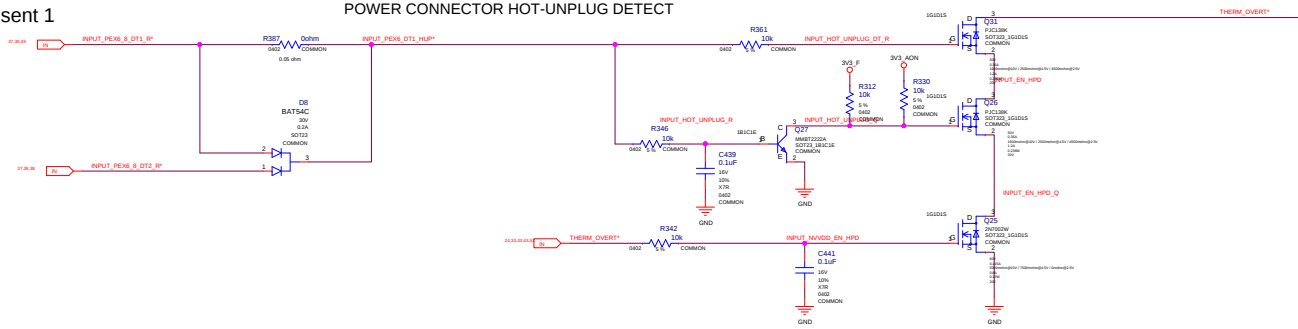
7701 SAN TOMAS EXPRESSWAY
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NV_PN	600-1G160-BASE-300
PCB REV	PG160-802
BOB REV	A
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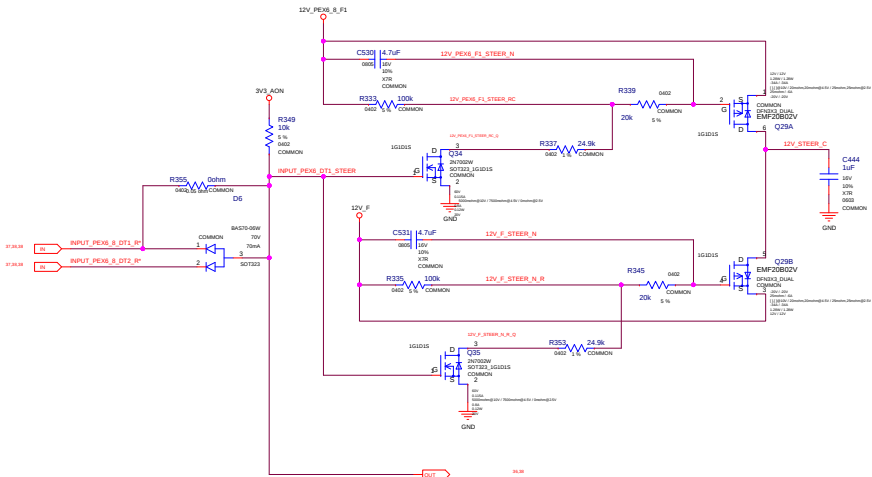
PEX Input Present 1

POWER CONNECTOR HOT-UNPLUG DETECT

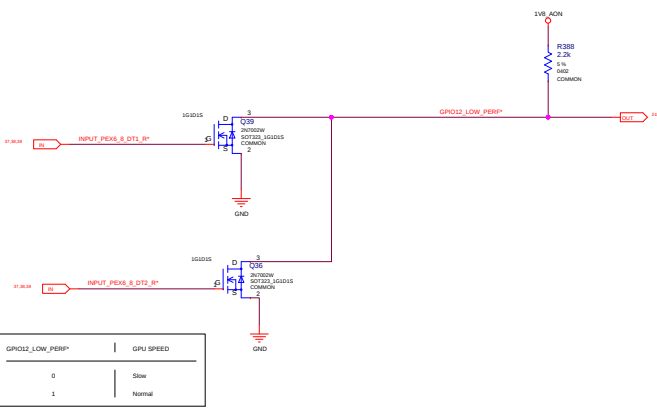


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA



PEX Input - Power Level/PSI* Control



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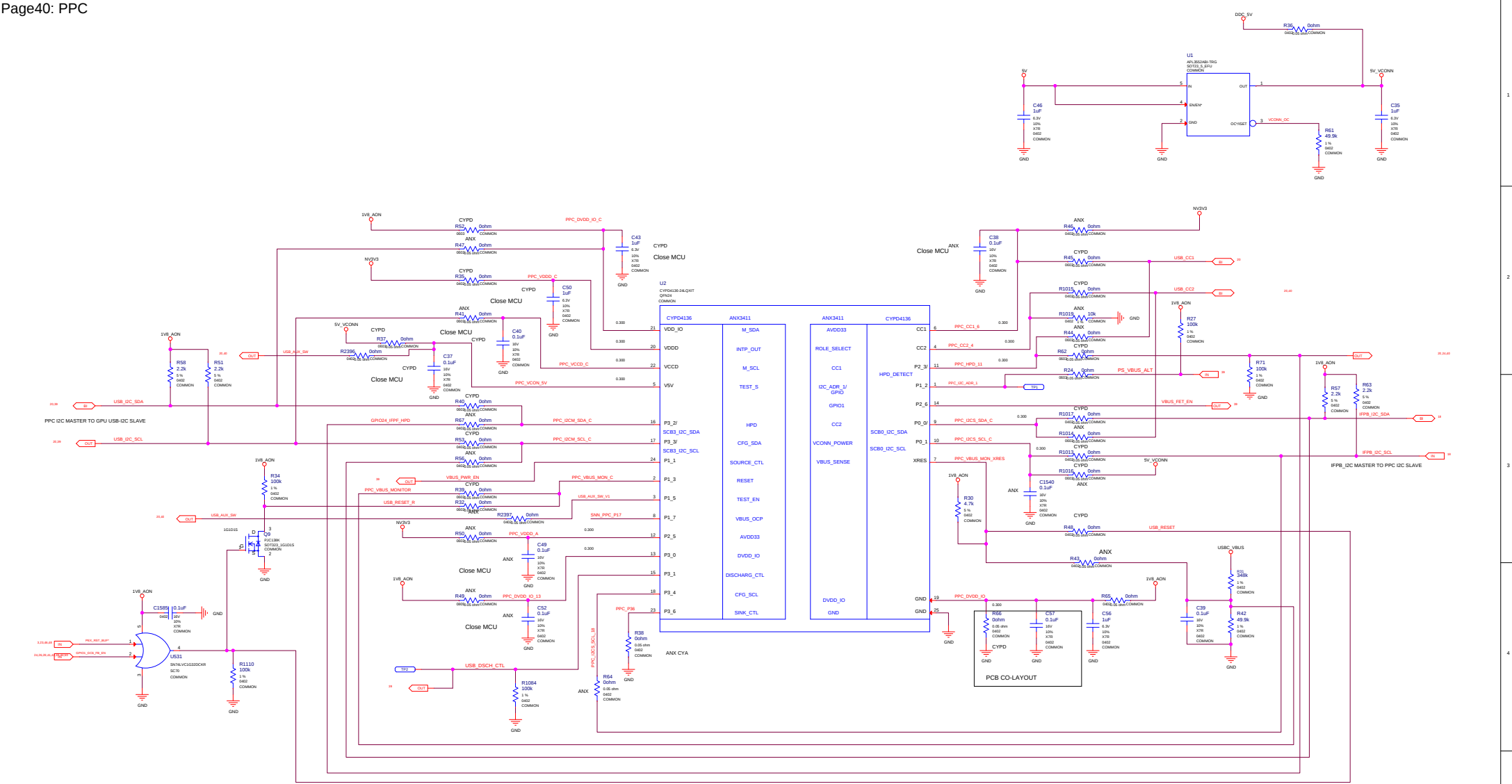
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PAGE DETAIL	PS: STEERING, UPB & HOT-UNPLUG

NV_PN	600-1G160-BASE-300
PCB REV	PG100-802
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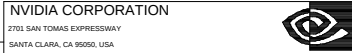
NV_PN	600-1G160-BASE-300		
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	SCL	SDA
CYPD I2C SLAVE	PIN 10	PIN 9
CYPD I2C MASTER	PIN 17	PIN 16
ANX I2C SLAVE	PIN 18	PIN 17
ANX I2C MASTER	PIN 22	PIN 21

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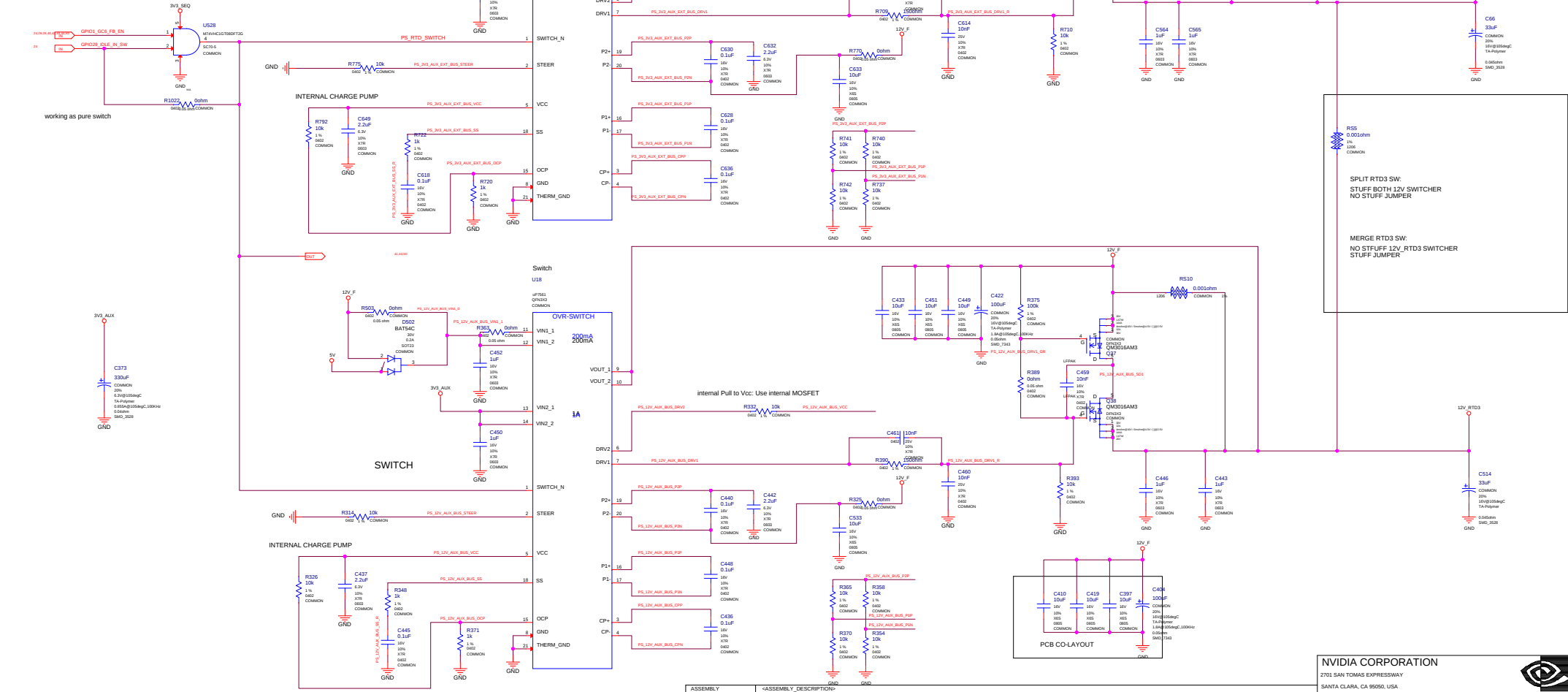
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PAGE DETAIL	PD PPC



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PCB REV	PG100-802
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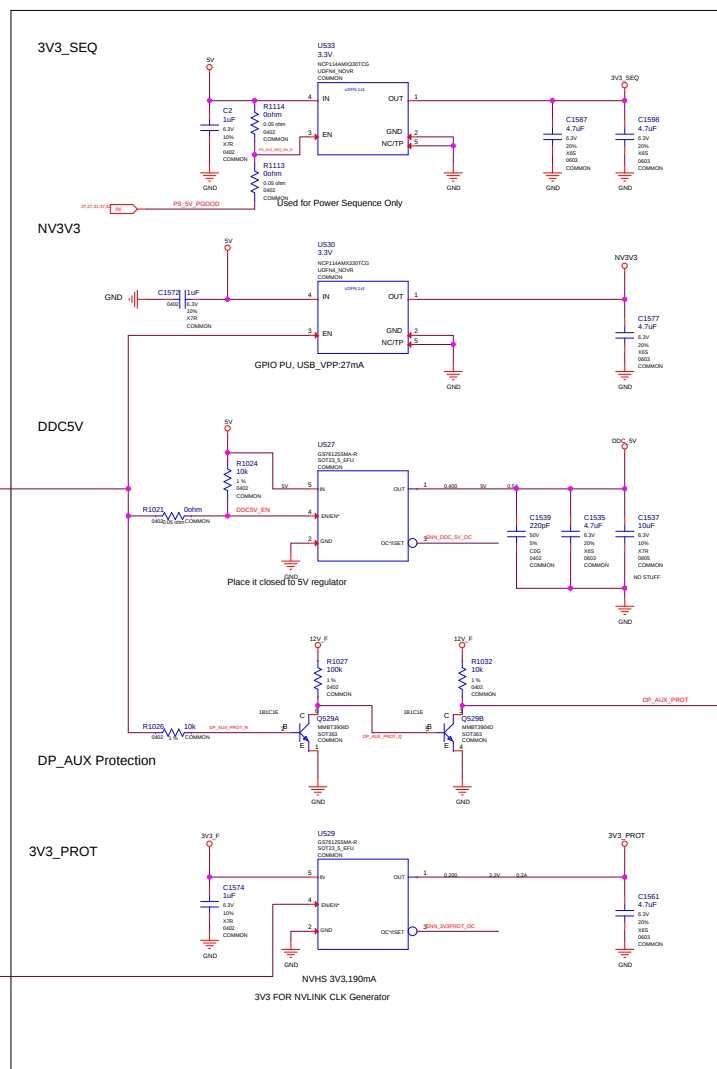
SWITCH		VOUT	
0		VOUT = VIN1	
1		VOUT = VIN2	

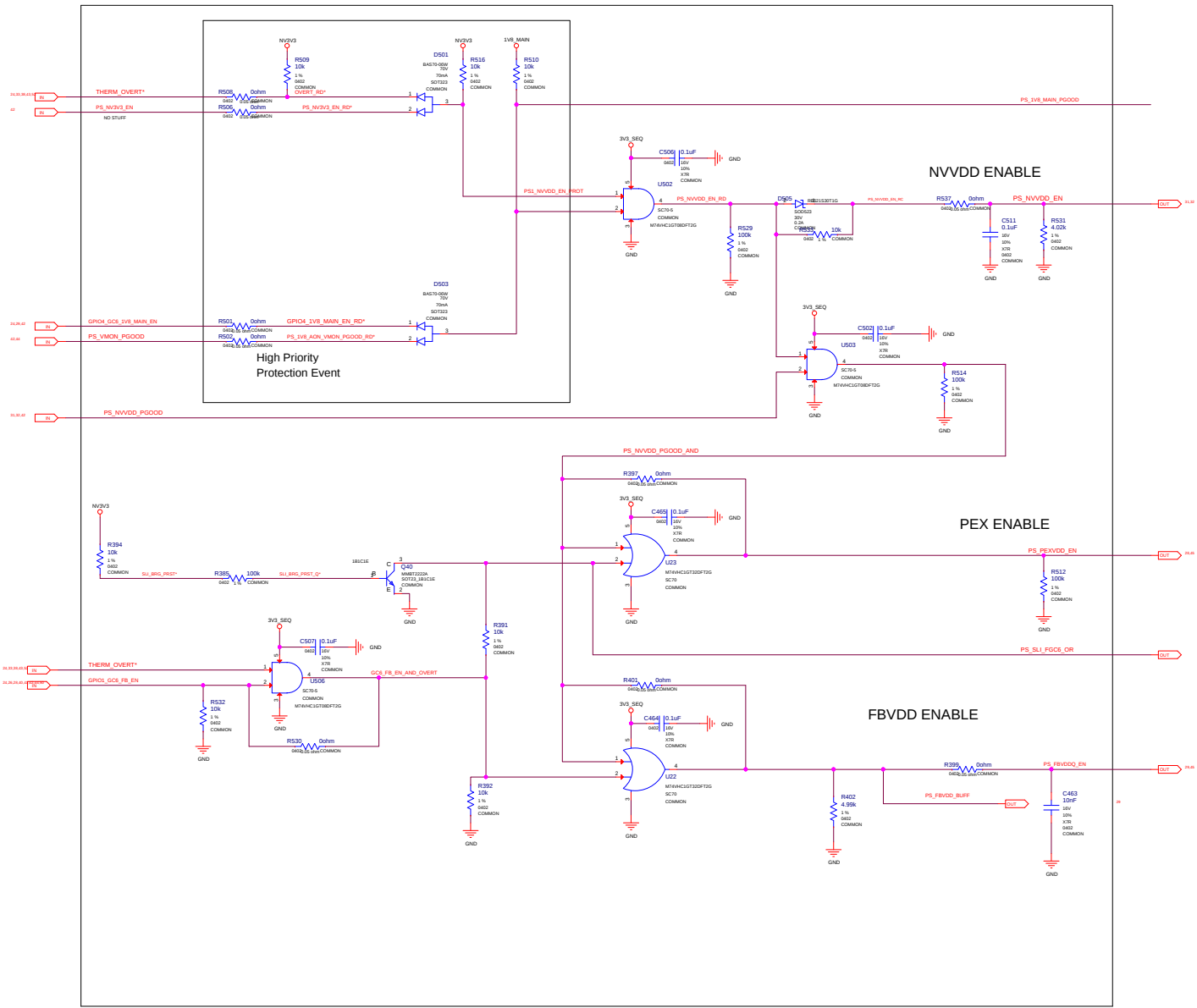
AND GATE LOGIC			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V
0	1	0	12V
1	0	0	12V
1	1	1	3V3A



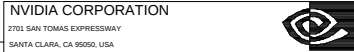
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NV_PN	600-1G160-BASE-300
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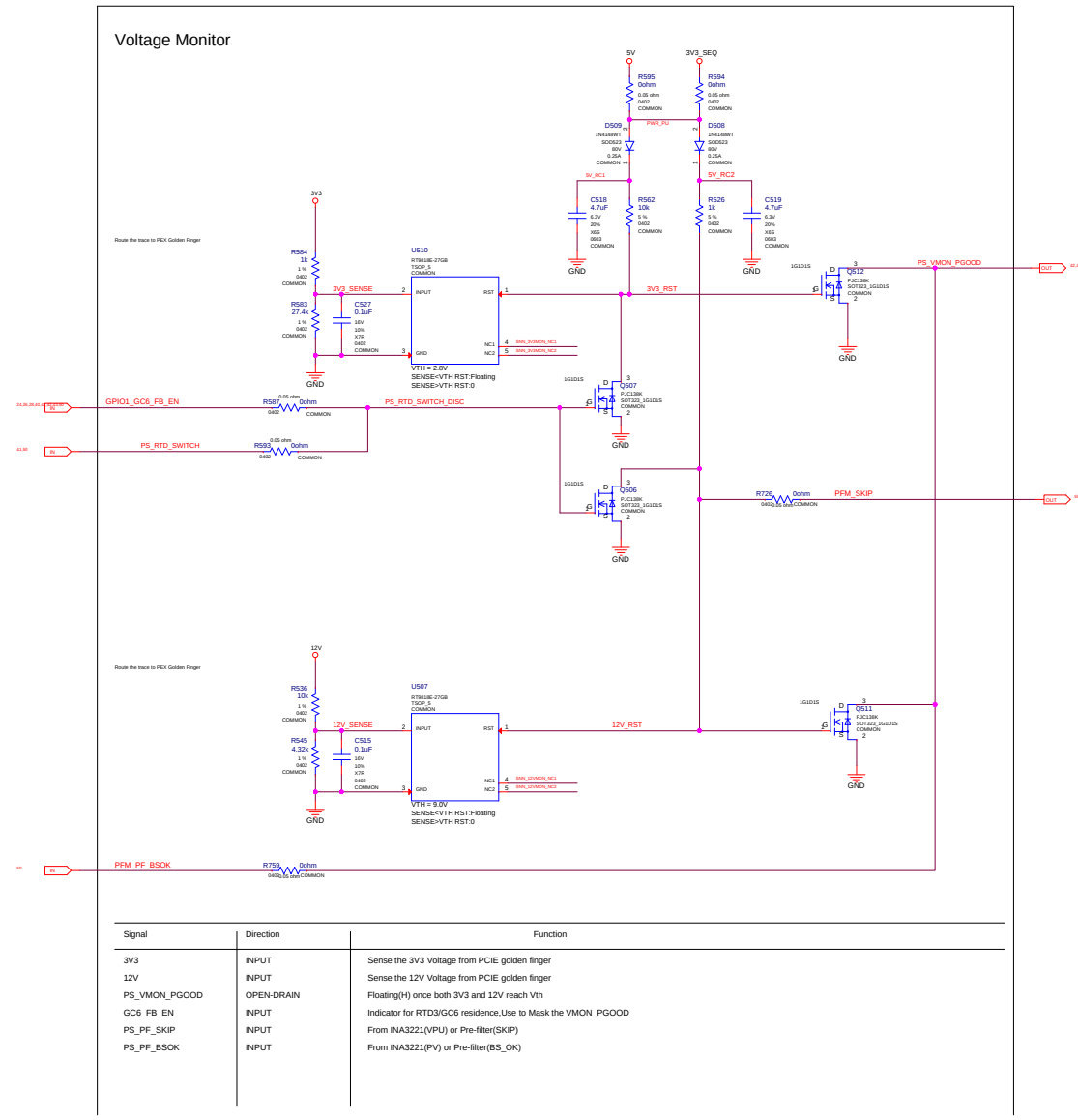




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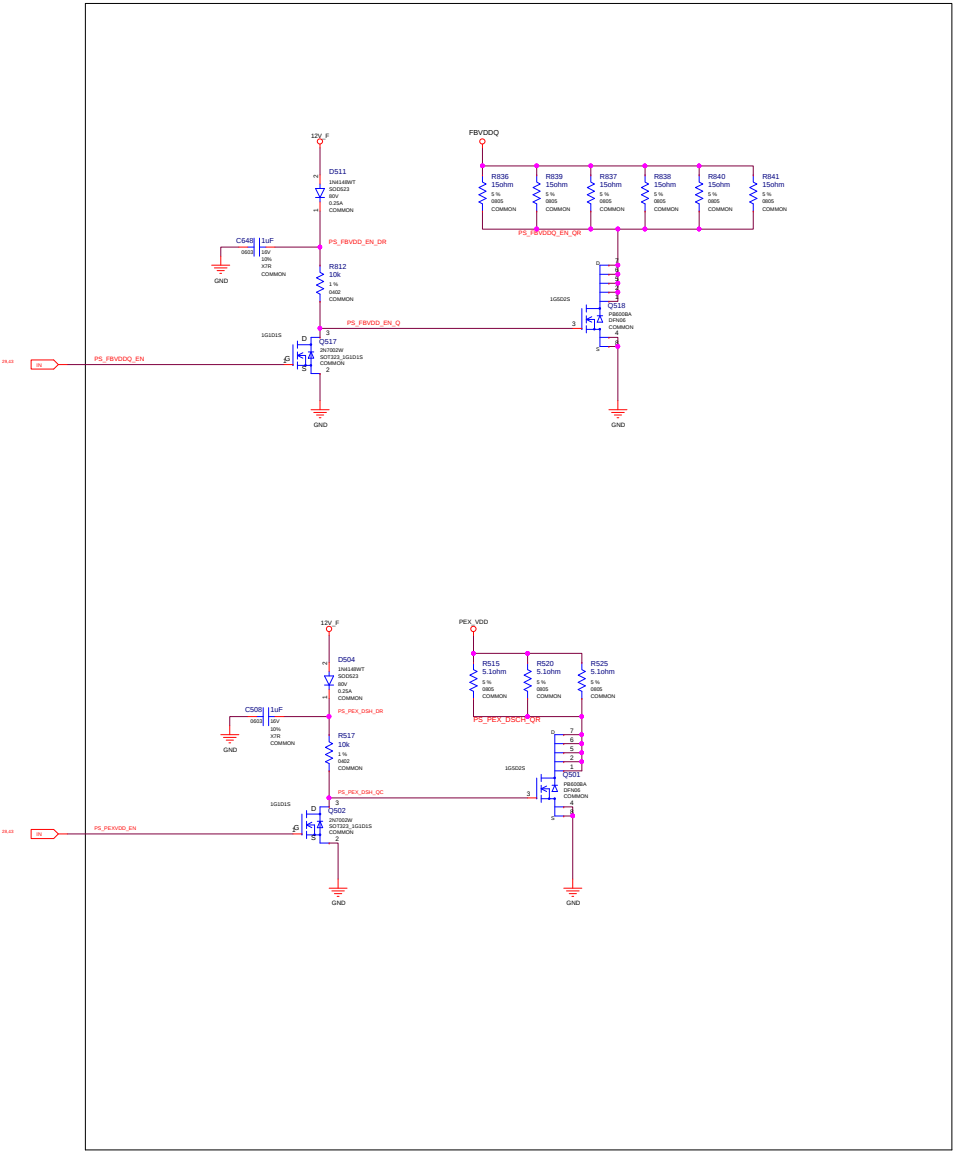


BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter	Pre-Filter	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence, Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSK0	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

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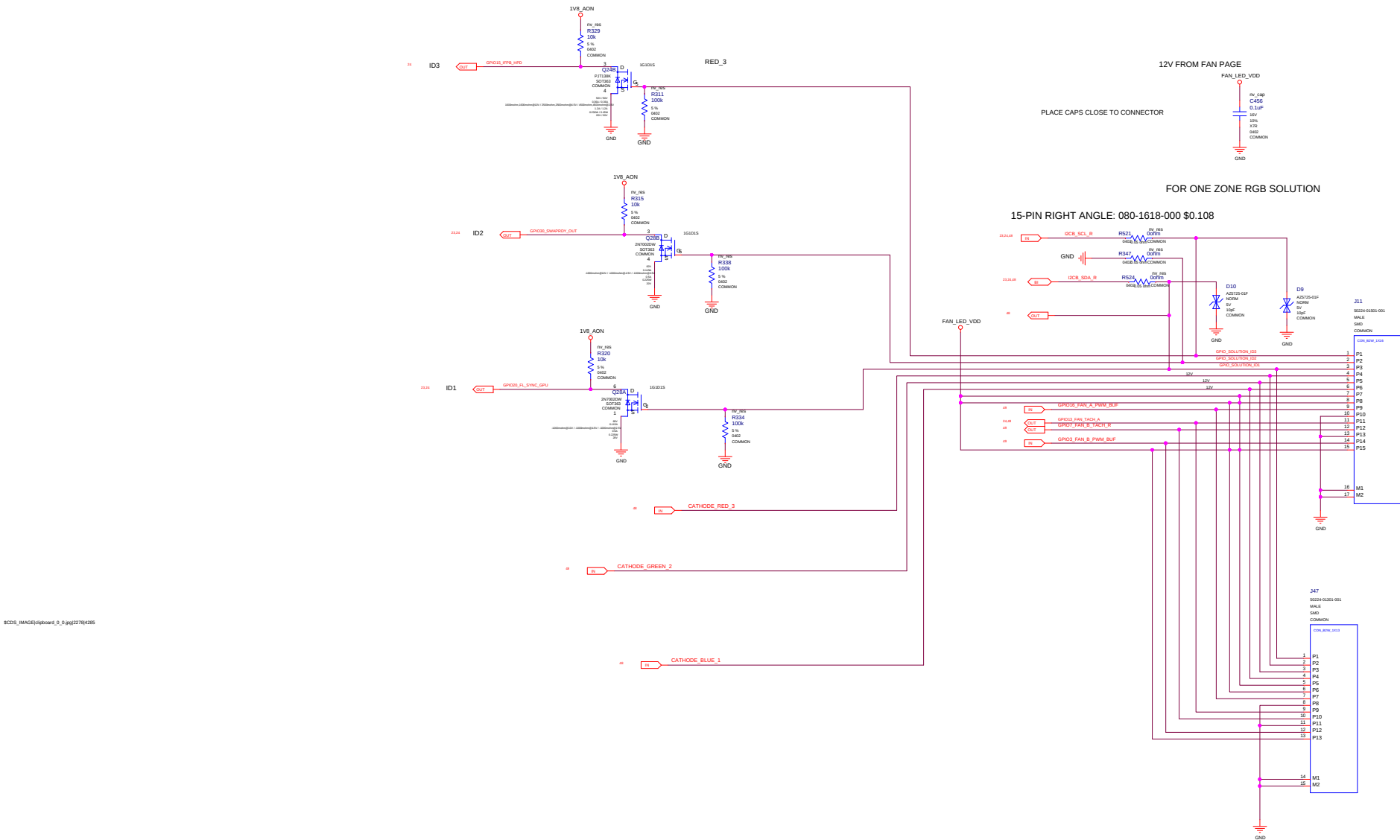
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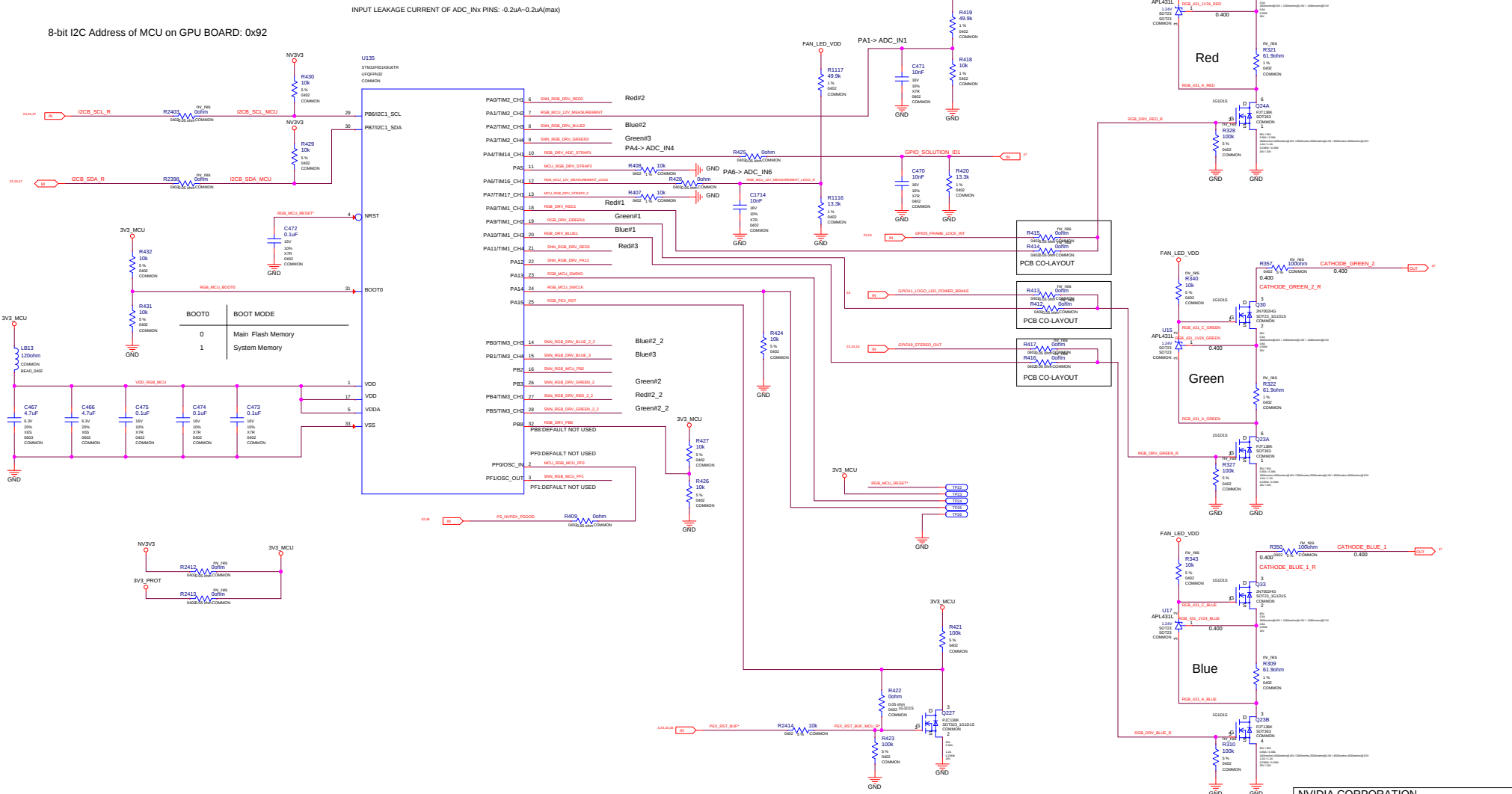
NV_PN	600-1G160-BASE-300		
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NV_PN	600-1G160-BASE-300		
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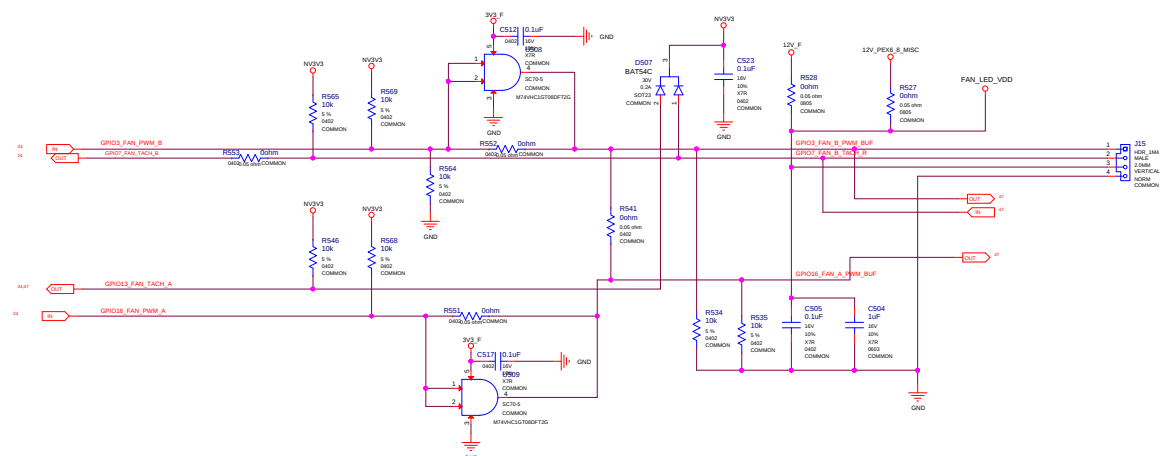


SCD3_IMAGE@sgboard_0_0.ppt2784295



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	LED DRIVER & BOOST

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	DUAL FAN

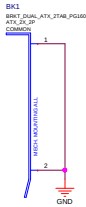
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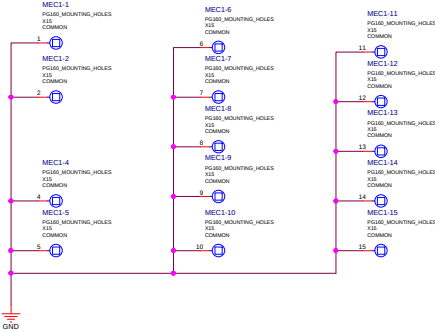
ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITED FUNCTION
HIGH	STANDBY

NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
NV_PN	600-1G160-BASE-300		
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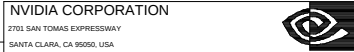
Brackets:



MOUNTING HOLES FOR HS:



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ASSEMBLY		<ASSEMBLY_DESCRIPTION>	
PAGE DETAIL		MECH	
NV_PN		600-1G160-BASE-300	
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