PG186-A00

256b GDDR6 x16
DP + DP + DP + HDMI/DP

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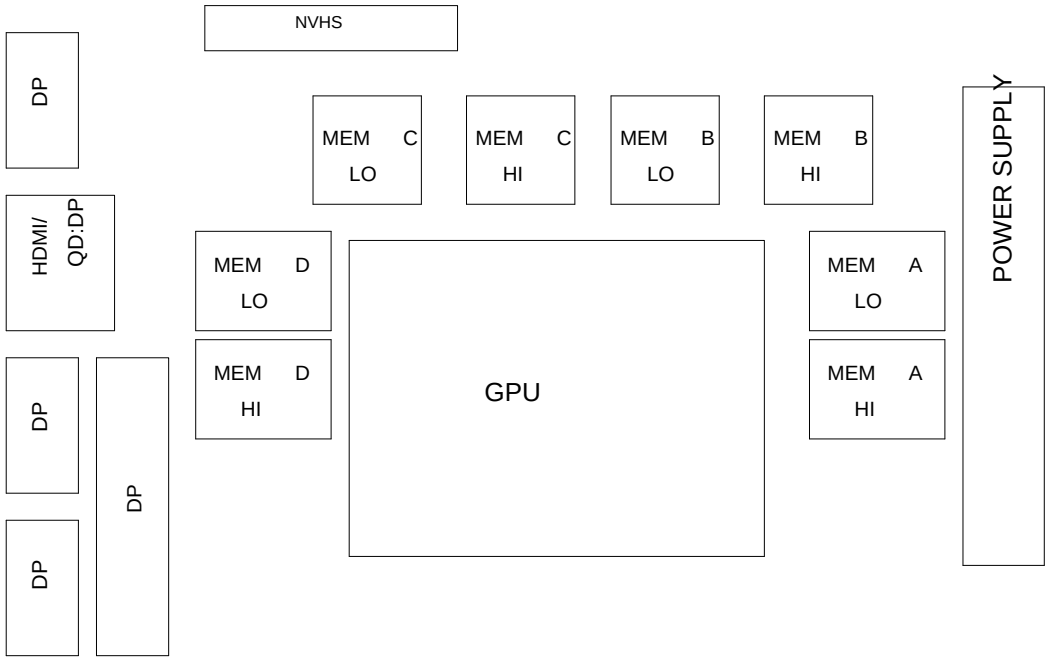
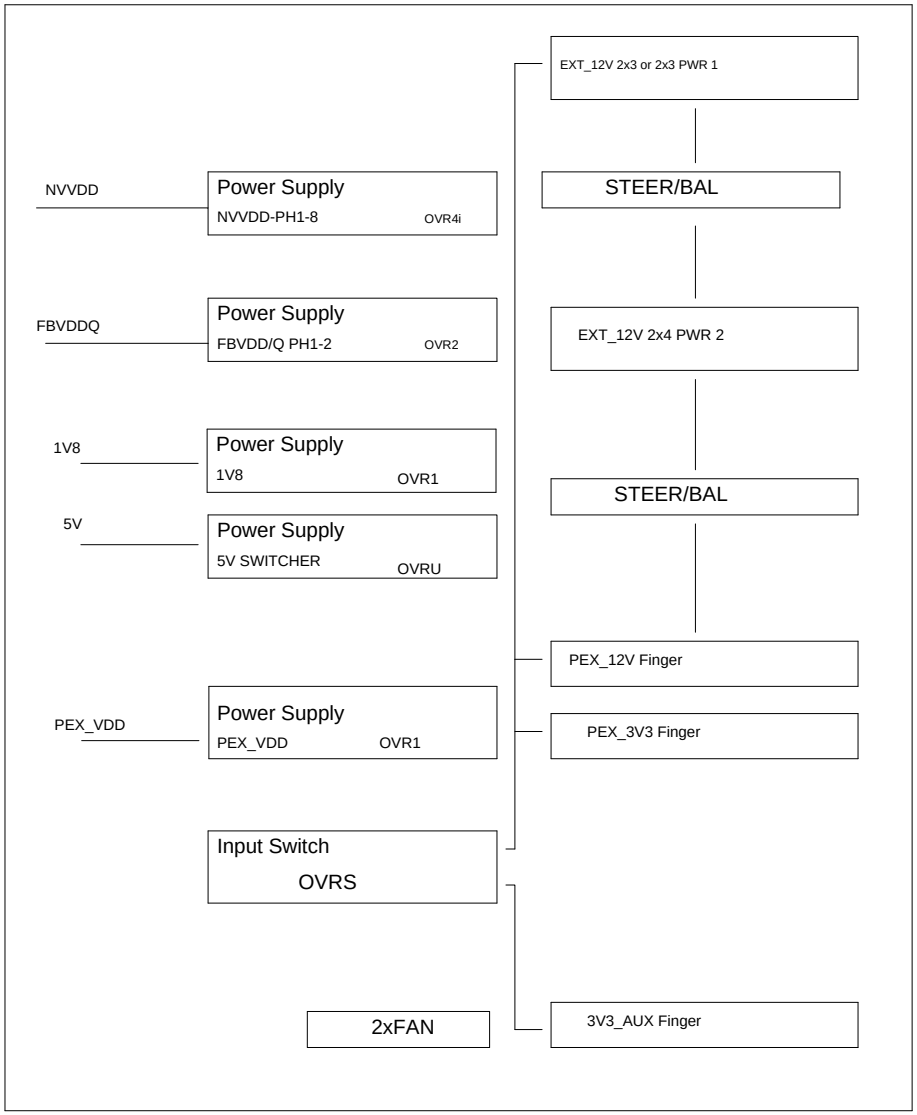
Page2: Block Diagram





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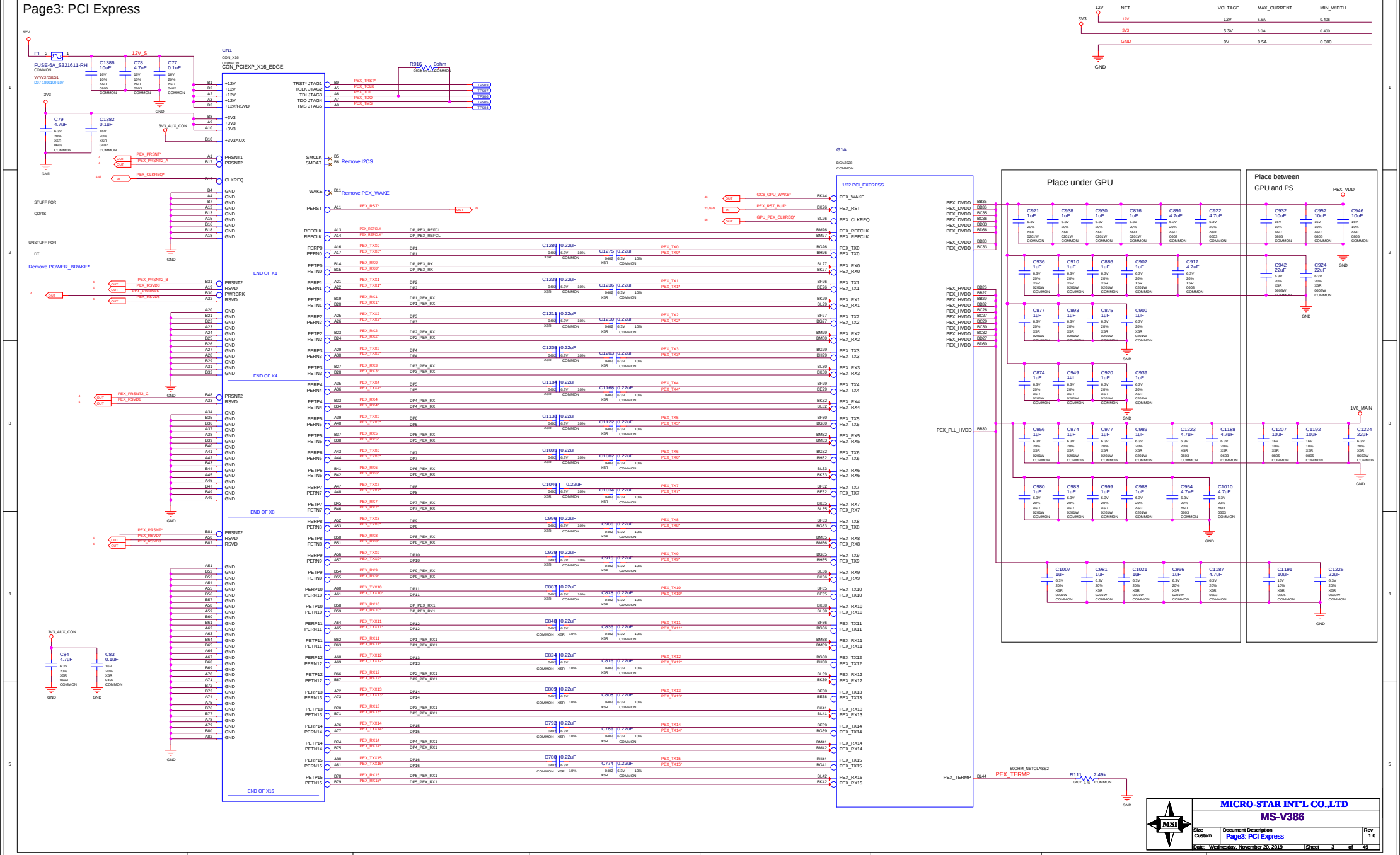
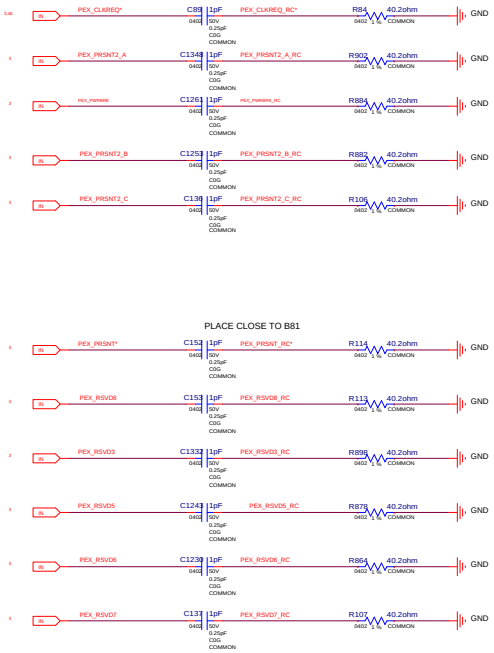
Page3: PCI Express



Page4: PCI Termination



PLACE CLOSE TO B81

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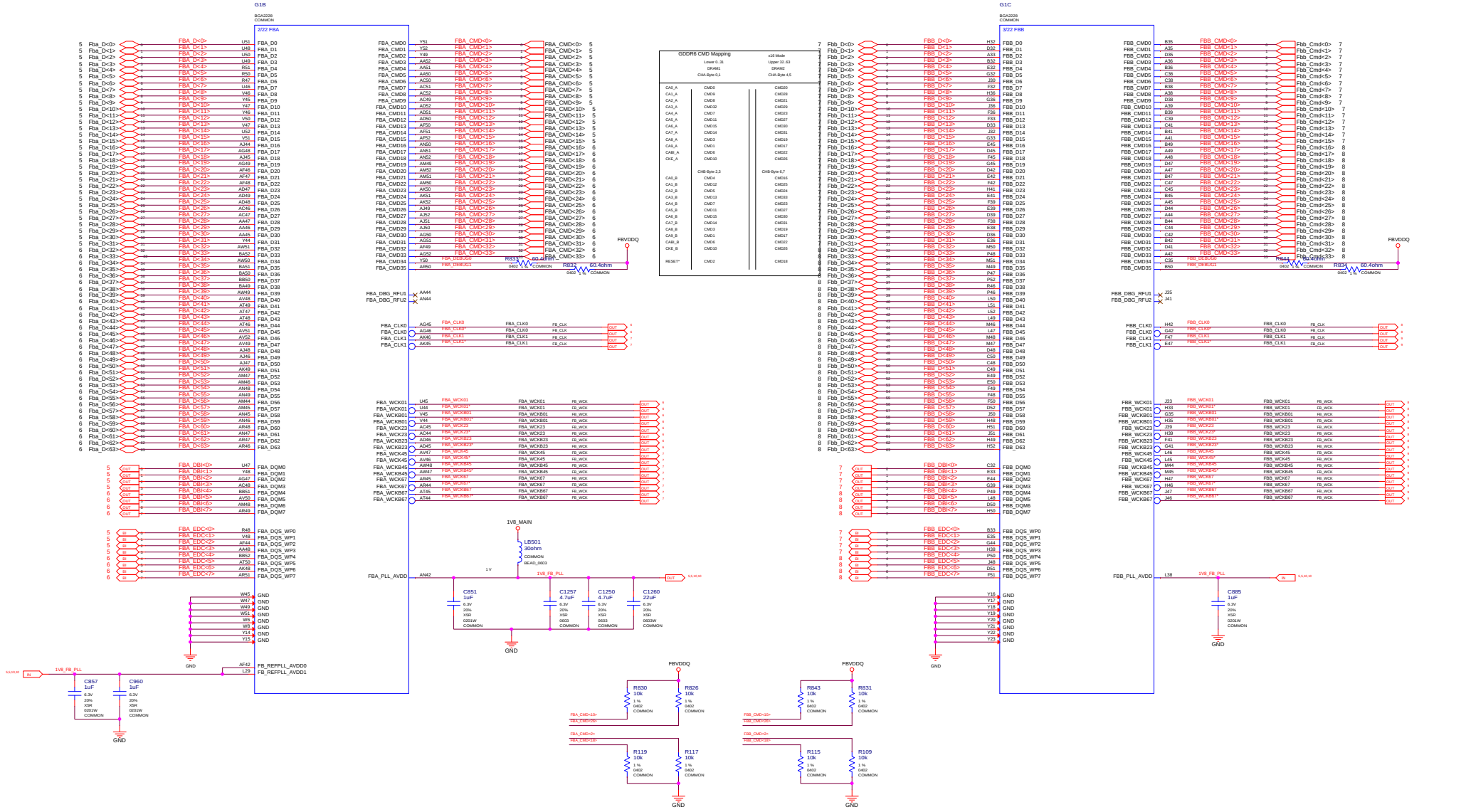
Page5: MEMORY: GPU Partition A/B



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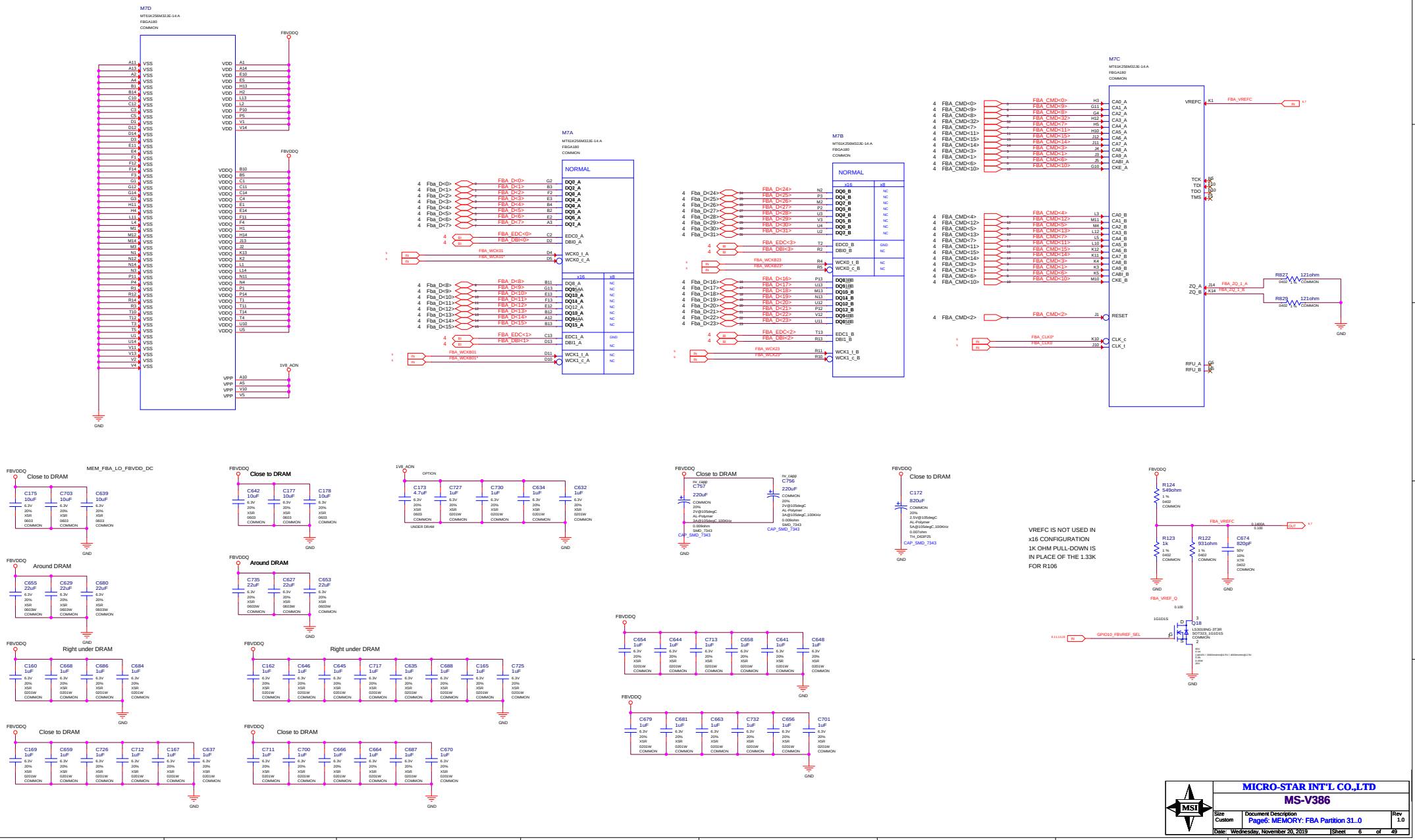
Page6: MEMORY: FBA Partition 31..0



VREFC IS NOT USED IN
x16 CONFIGURATION
1K OHM PULL-DOWN IS
IN PLACE OF THE 1.33K
FOR R106

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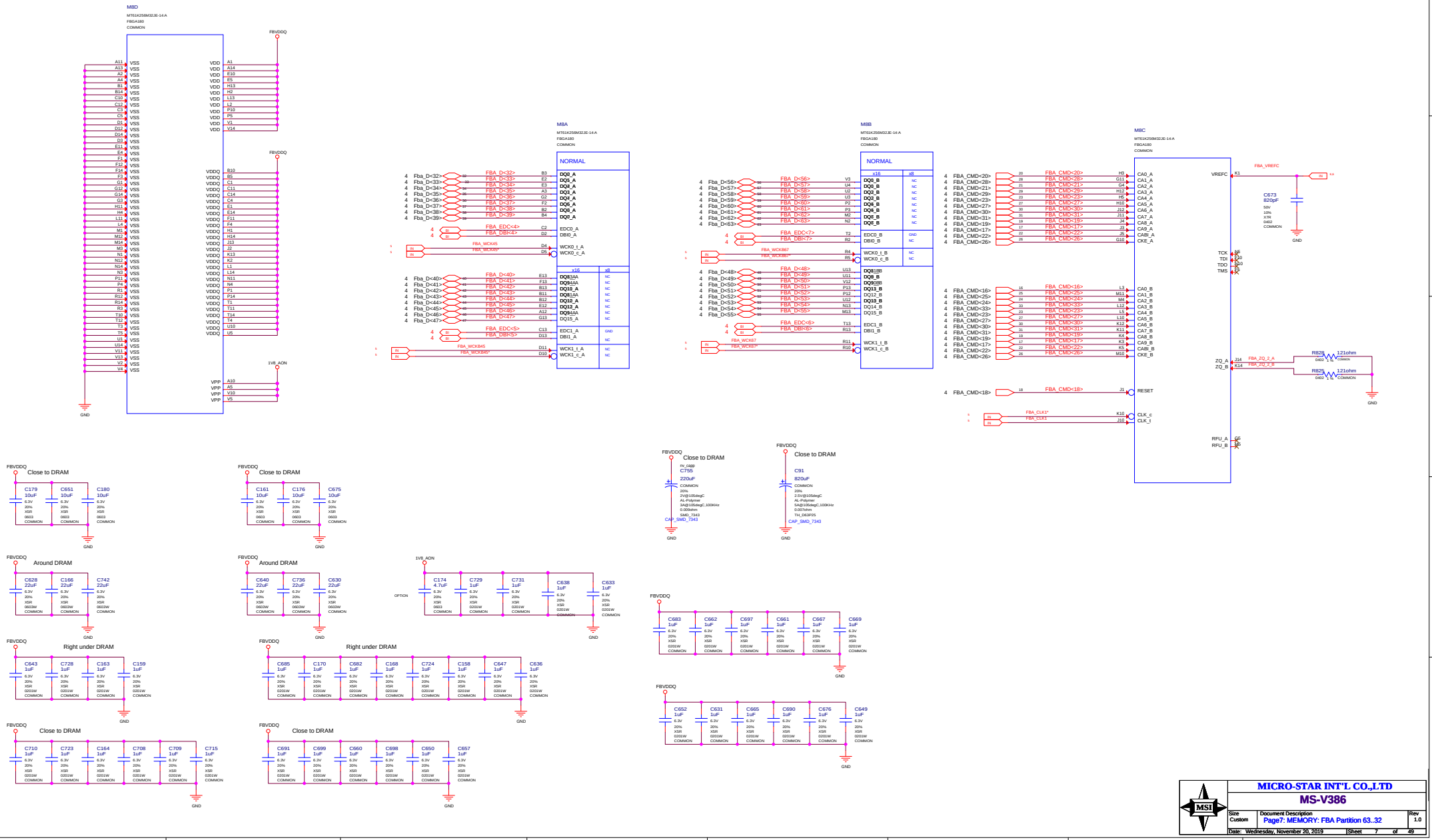
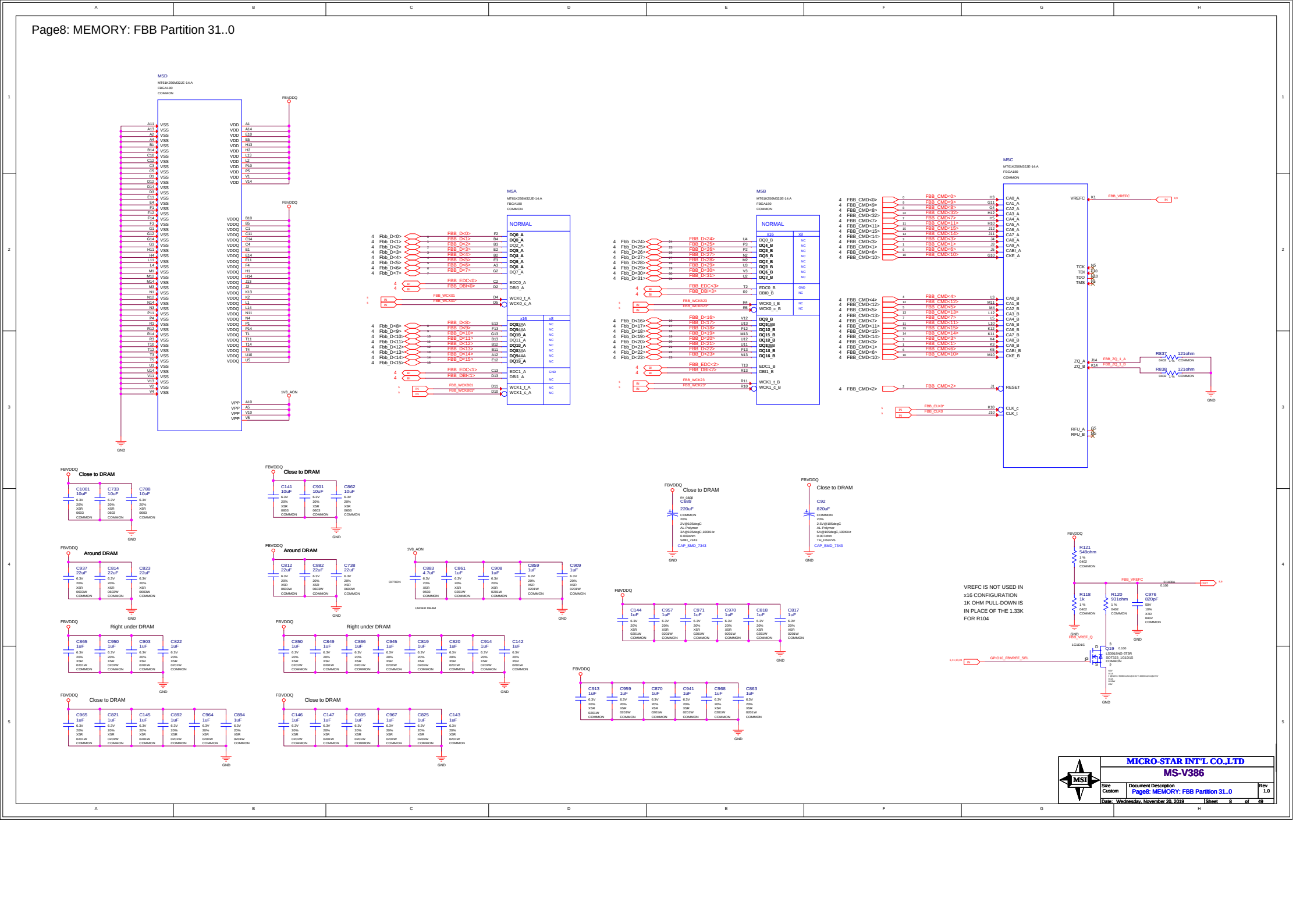
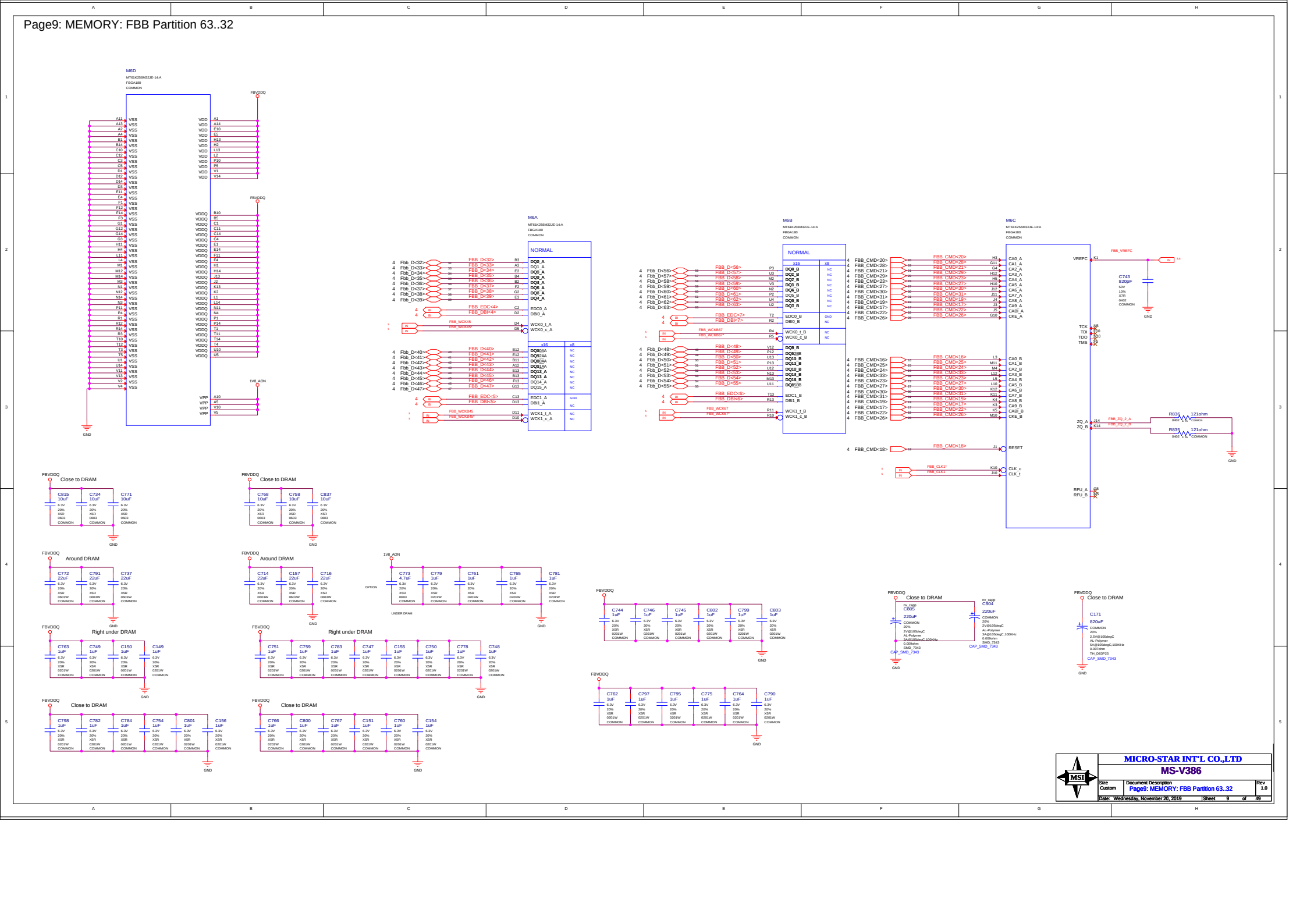
Page7: MEMORY: FBA Partition 63..32



Page8: MEMORY: FBB Partition 31..0




M6D
MT61K256M32JE-14:A
FBGA180
COMMON
FBVDDQ
1V8_AON
M6A
M6B
M6C
NORMAL
Close to DRAM
Around DRAM
Right under DRAM
GND
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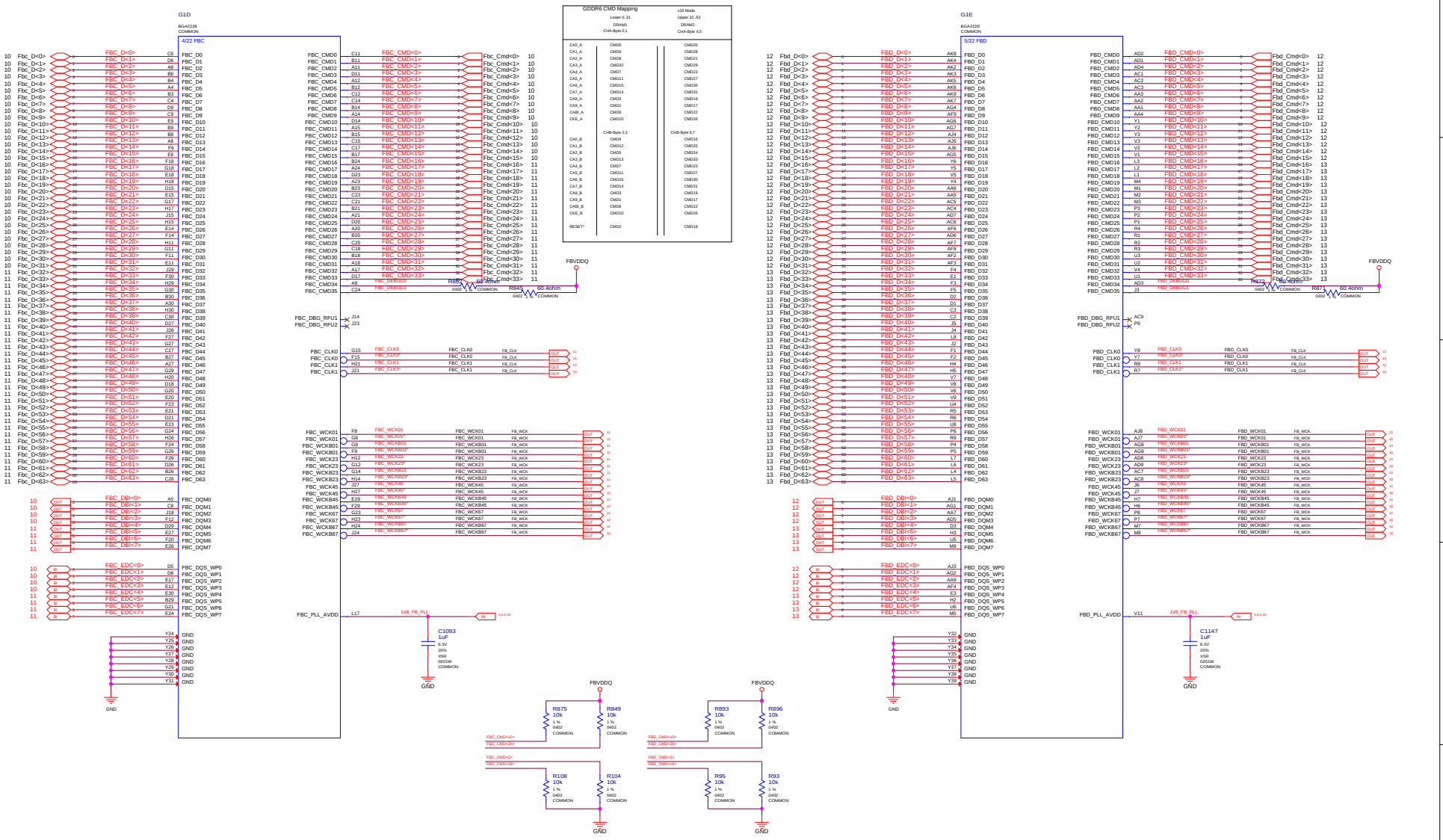
Page10: MEMORY: GPU Partition C/D



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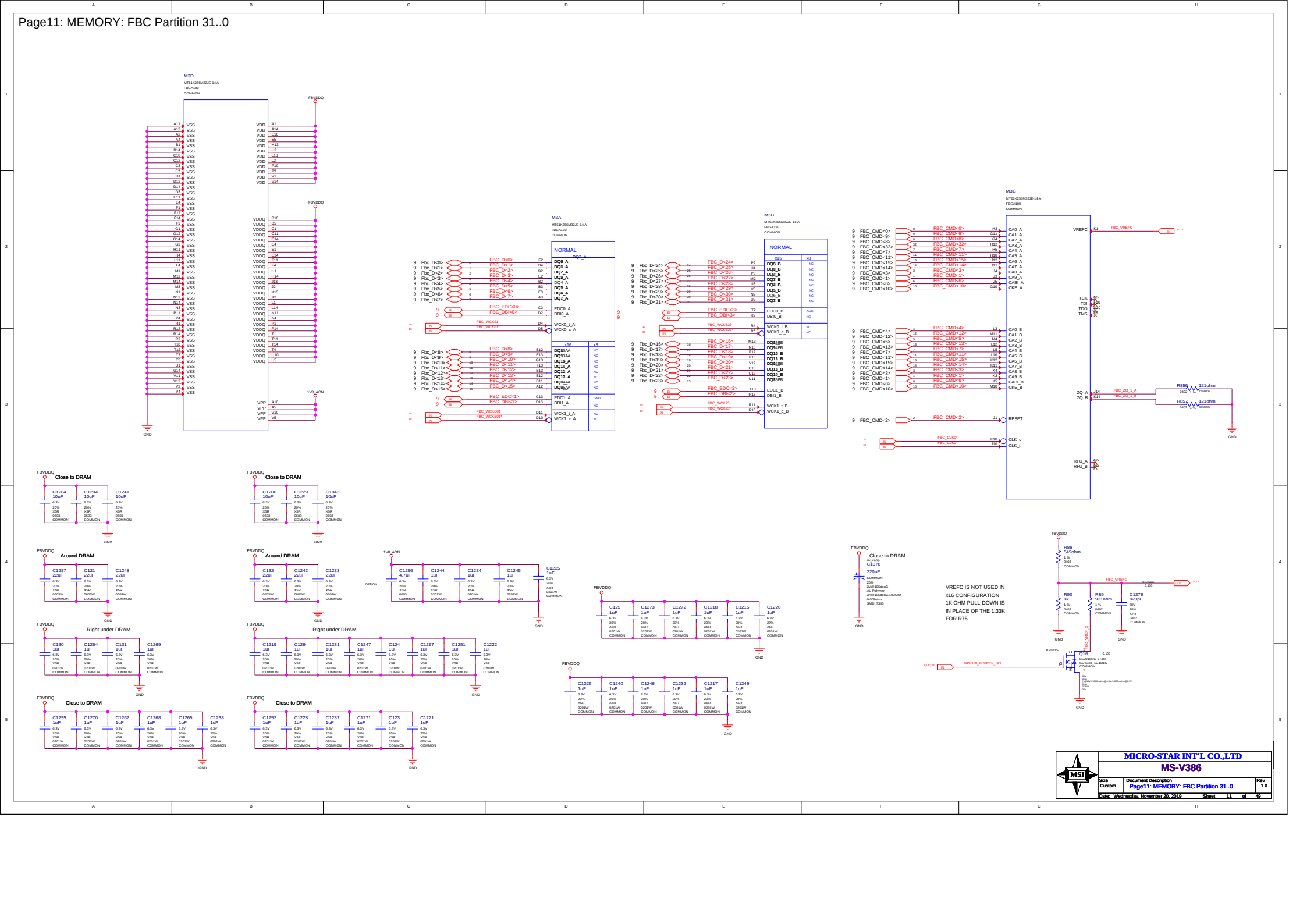
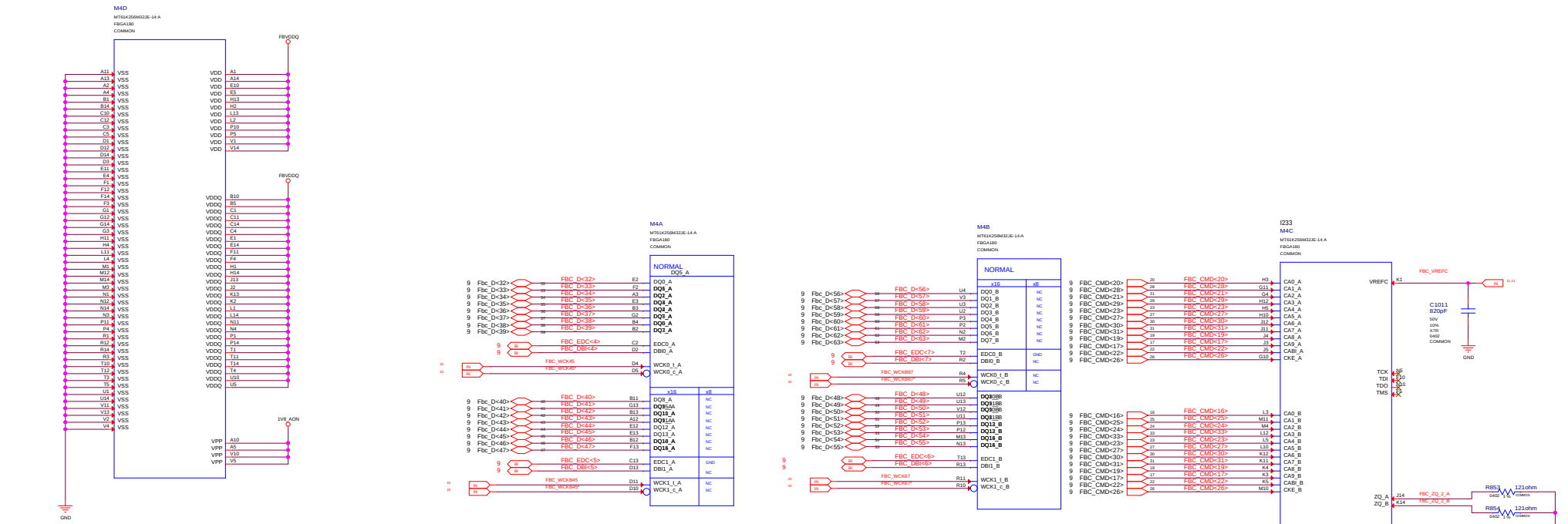
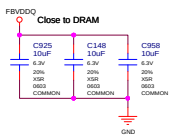
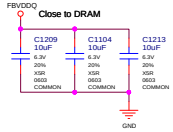
Page11: MEMORY: FBC Partition 31..0

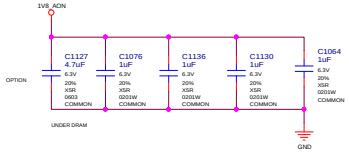


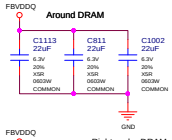
Page12: MEMORY: FBC Partition 63..32

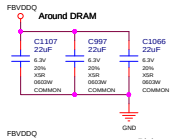


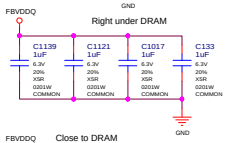


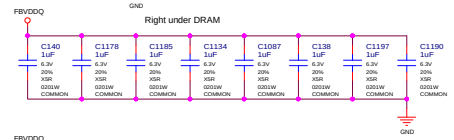


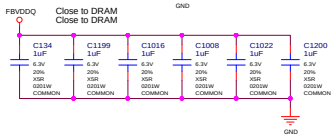


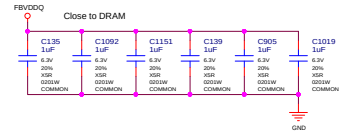


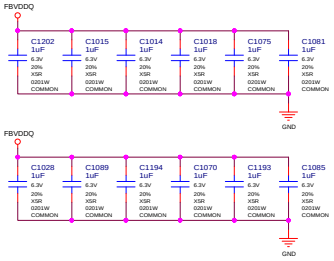


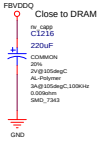


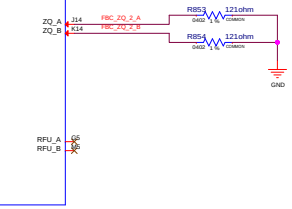












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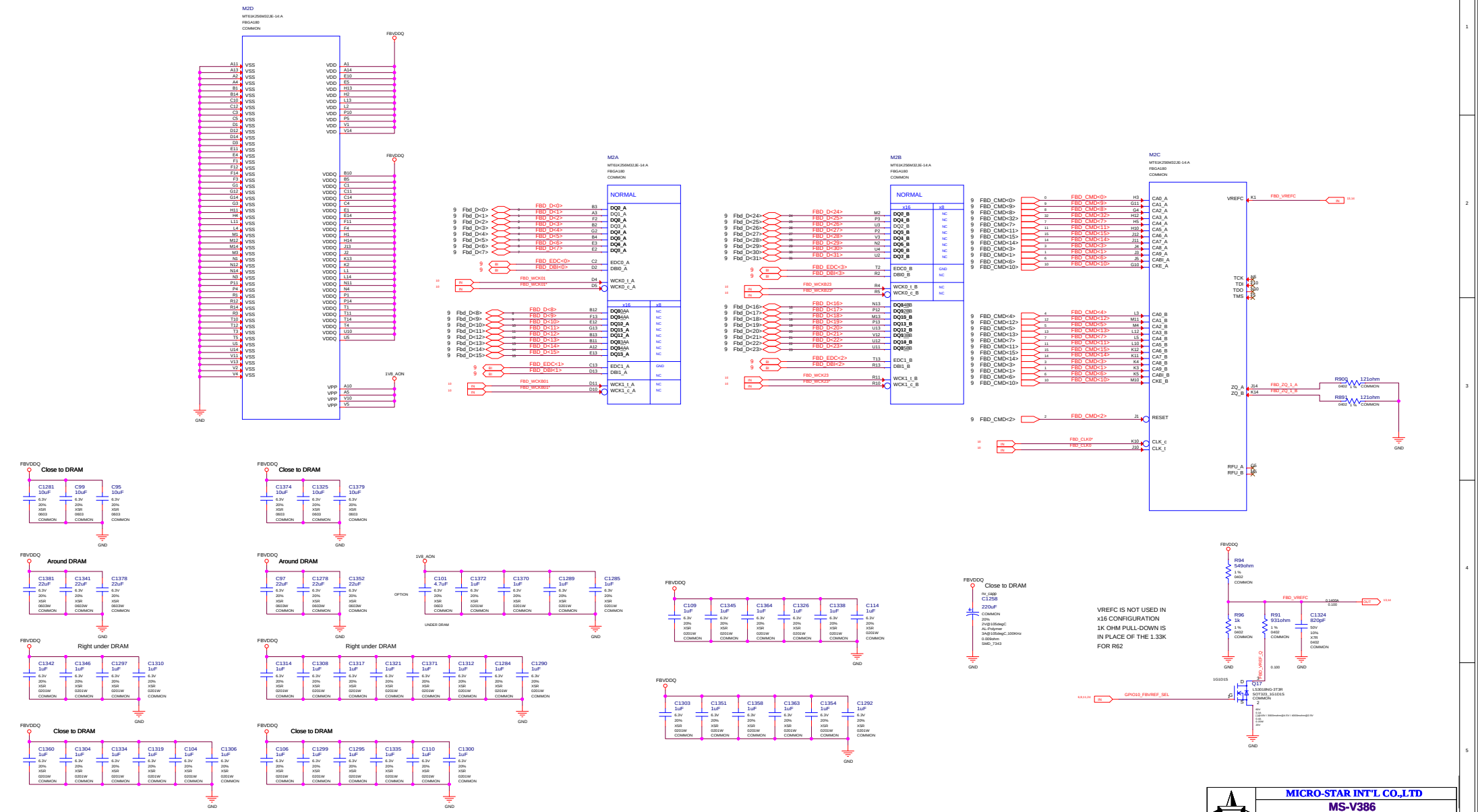

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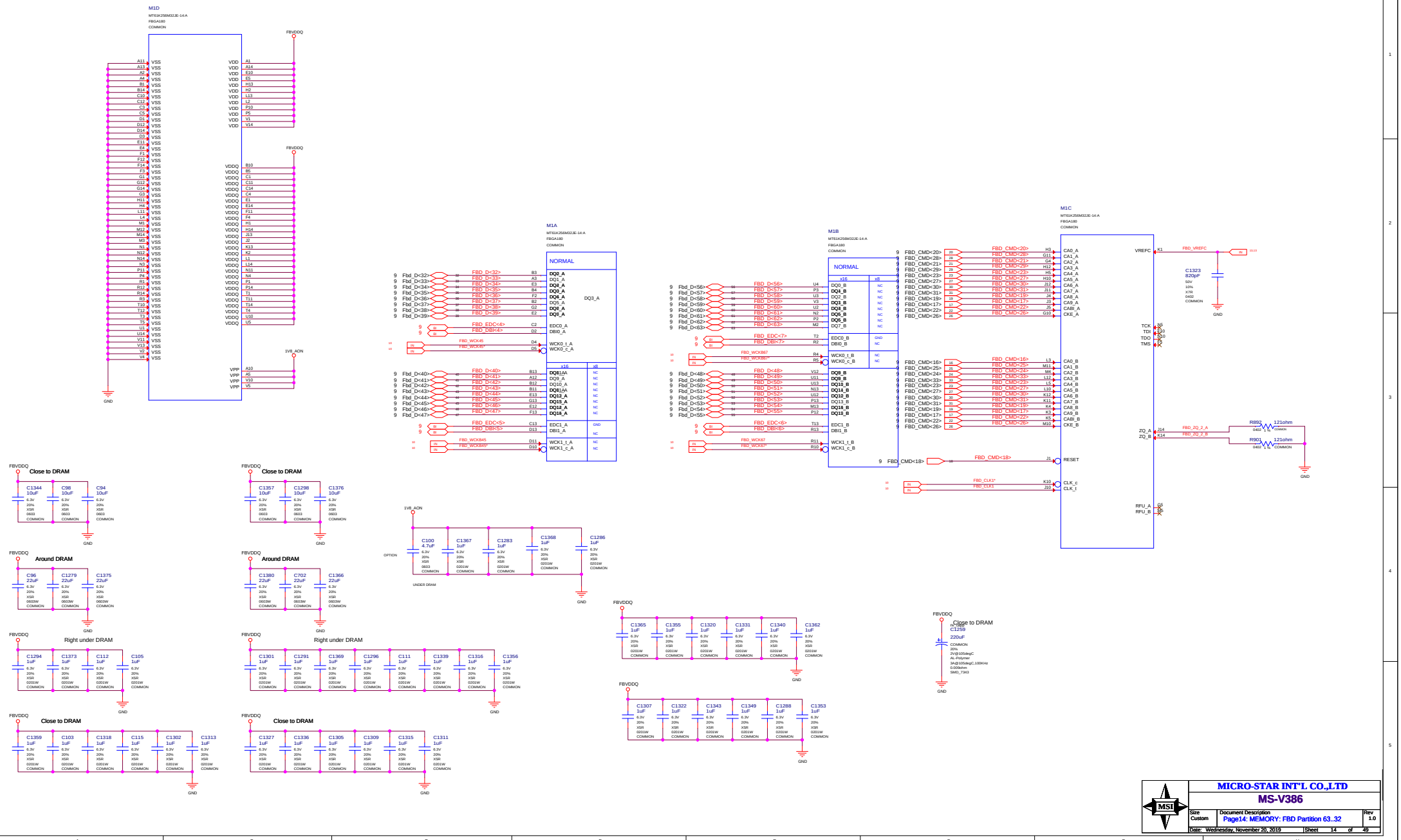

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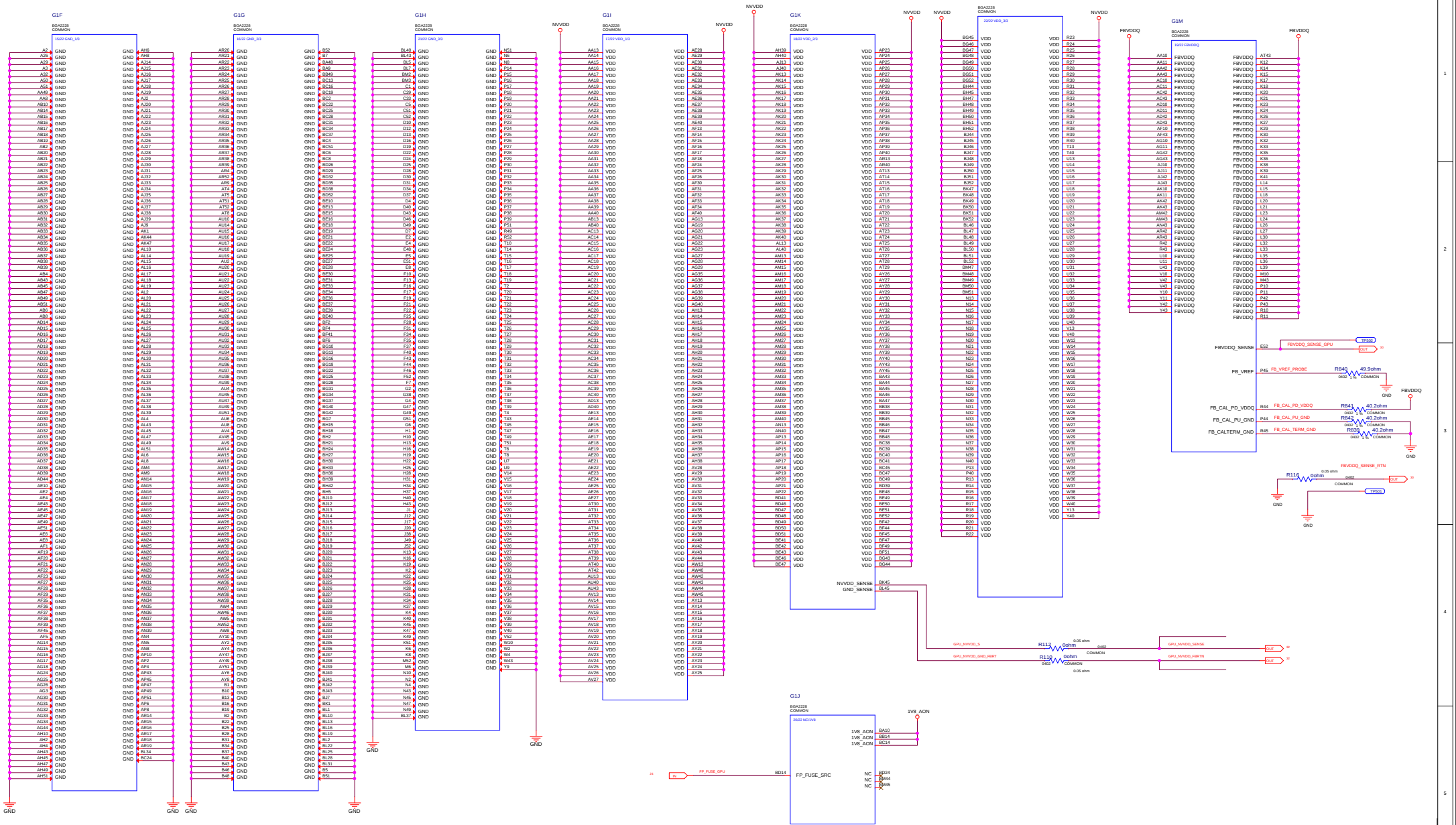
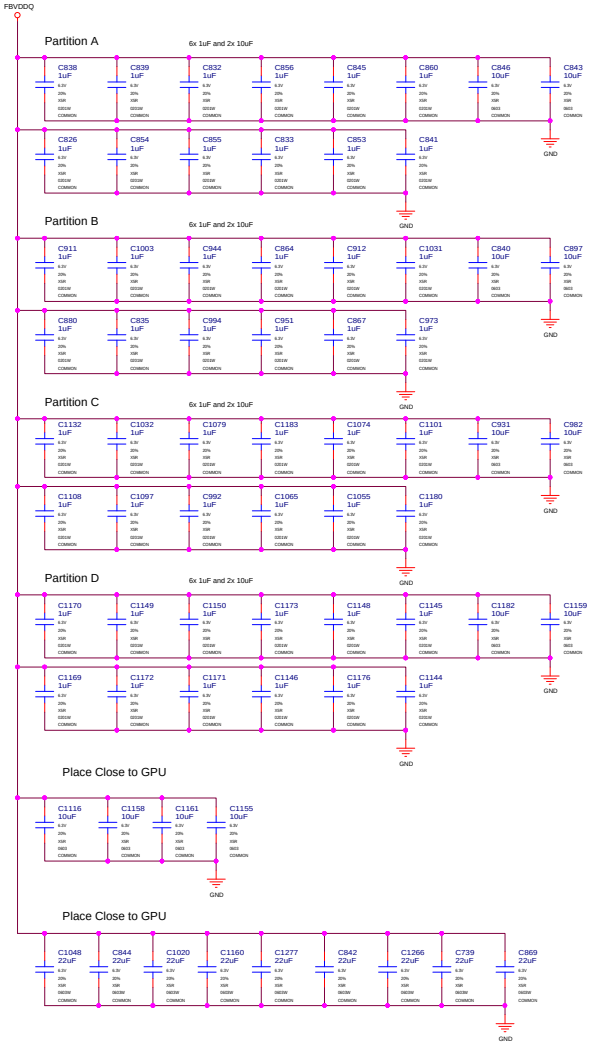
Page15: GPU PWR and GND

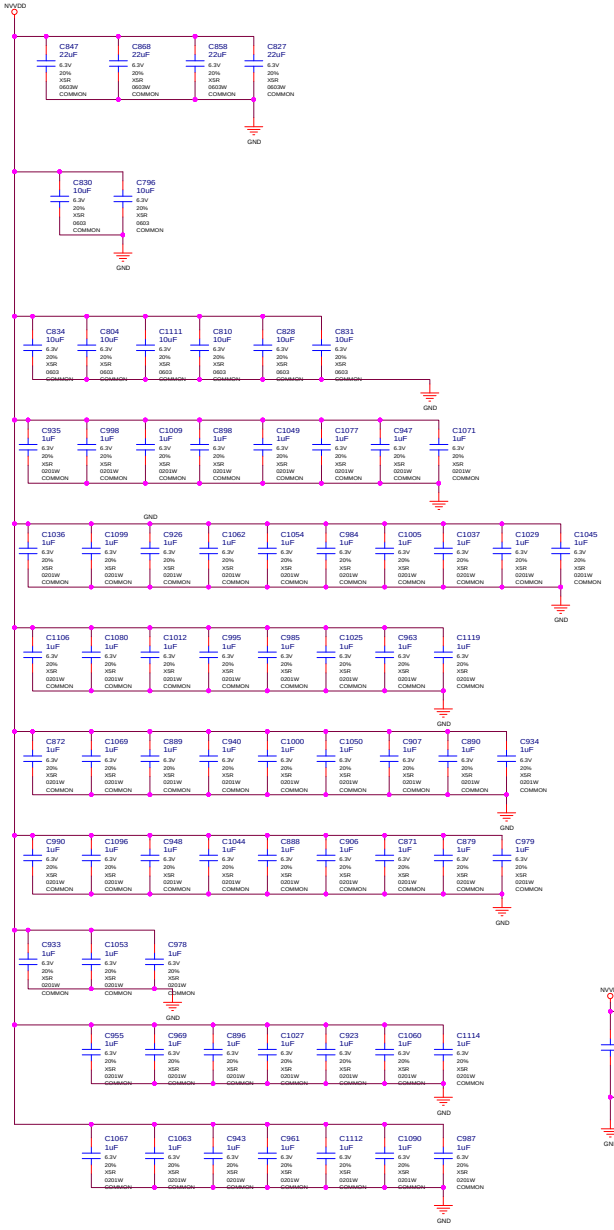


Page16: GPU Decoupling

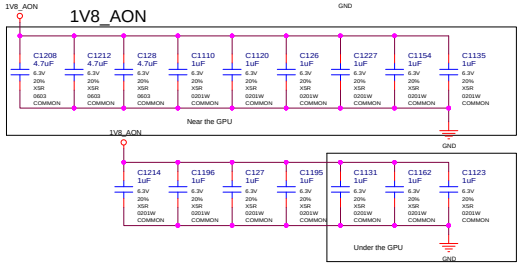
FBVDDQ



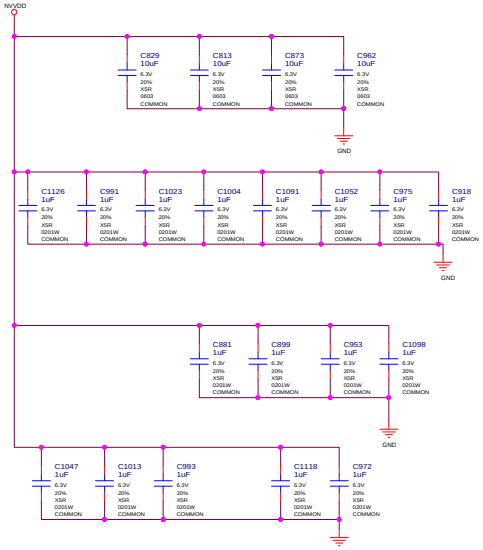
NVVDD

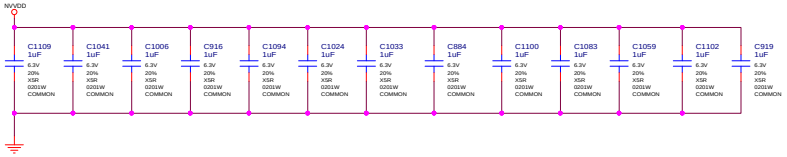


1V8_AON



NVVDD





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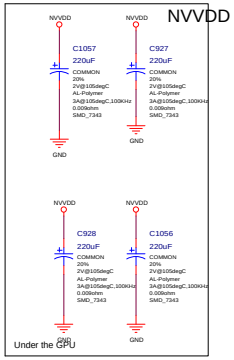

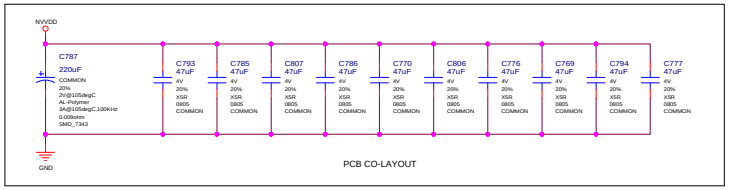

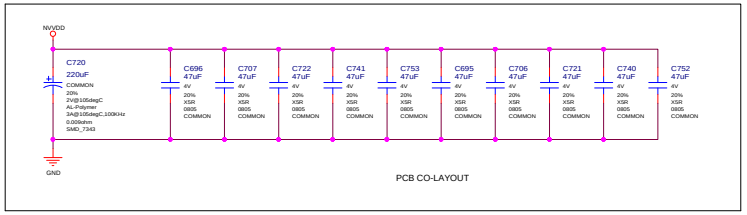

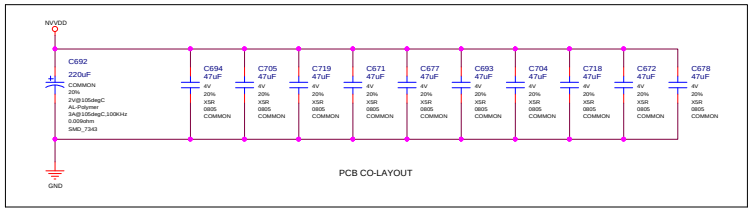

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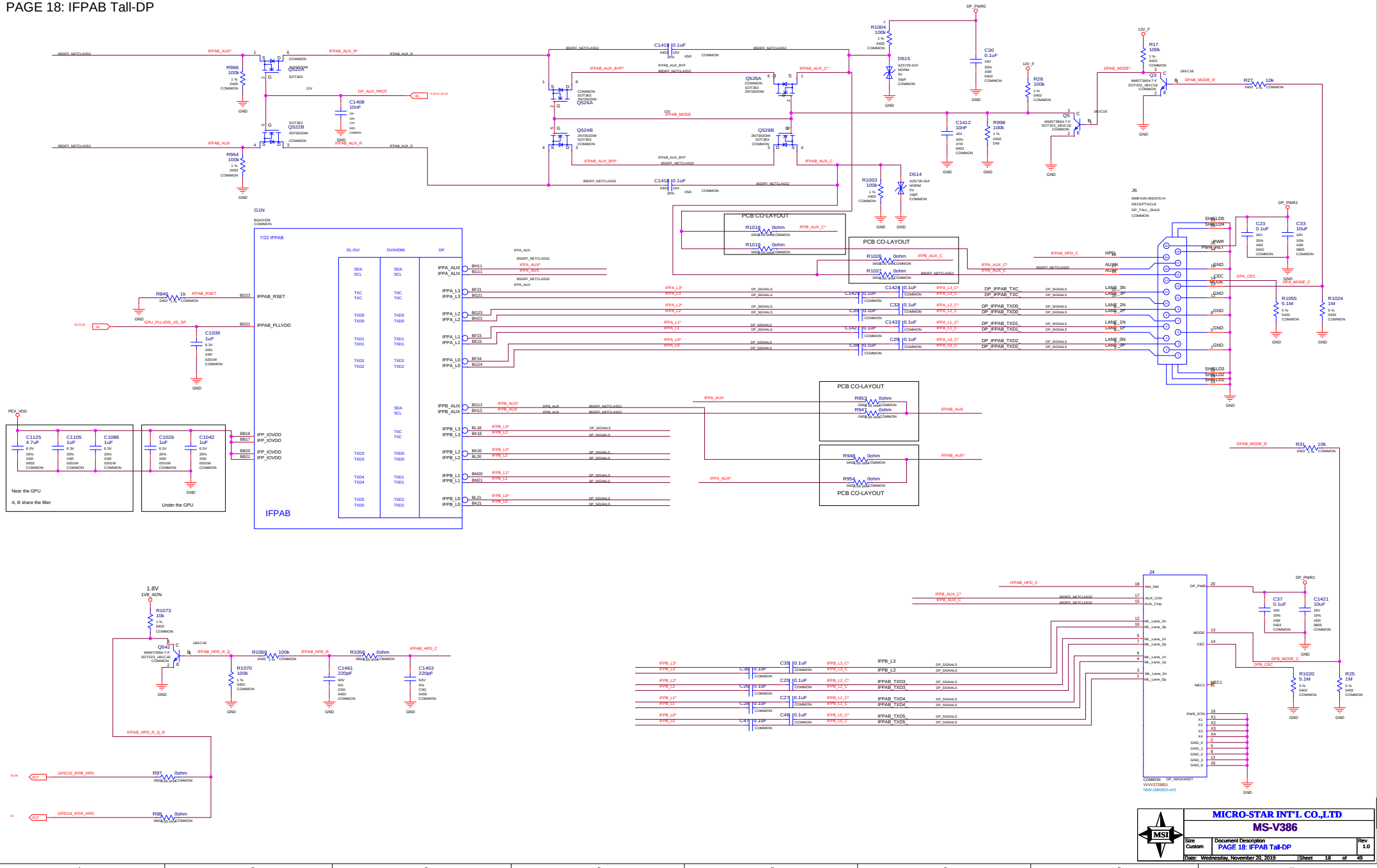
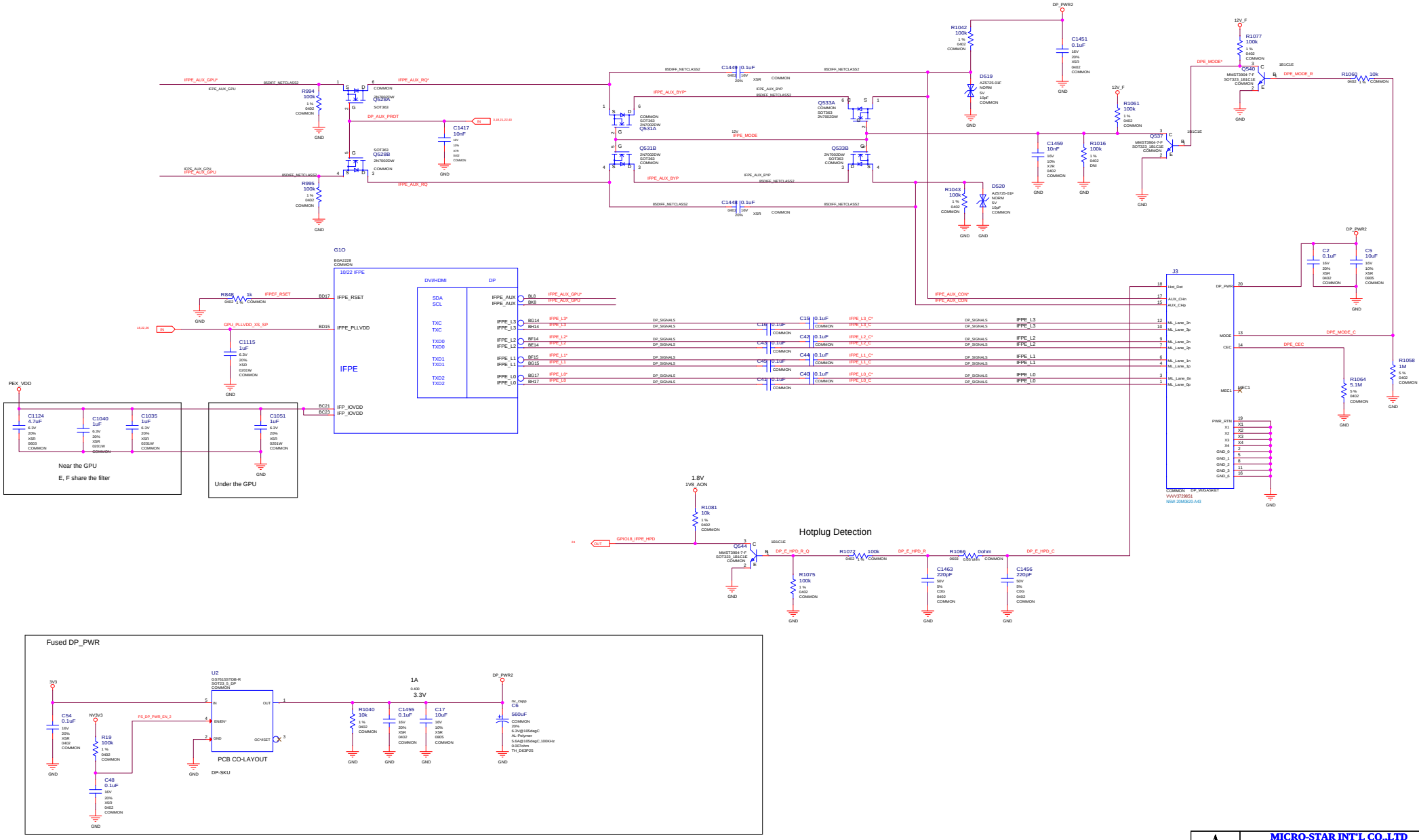
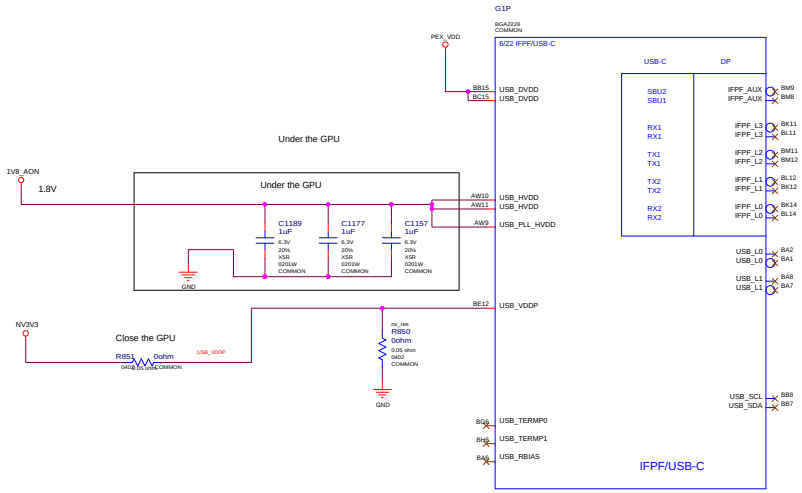
PAGE 18: IFPAB Tall-DP



PAGE 19: IFPE DP



PAGE 20: IFPF USBC



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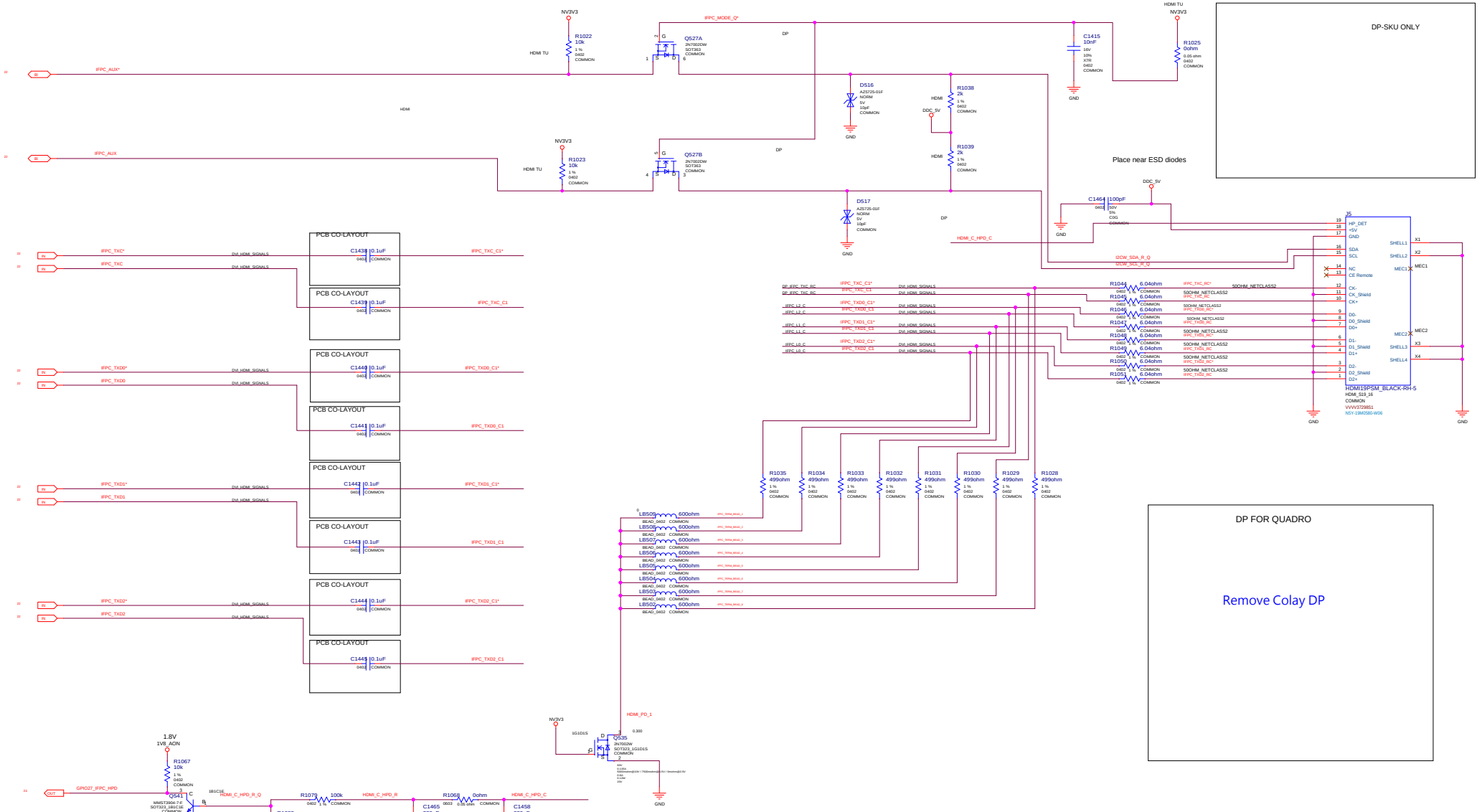
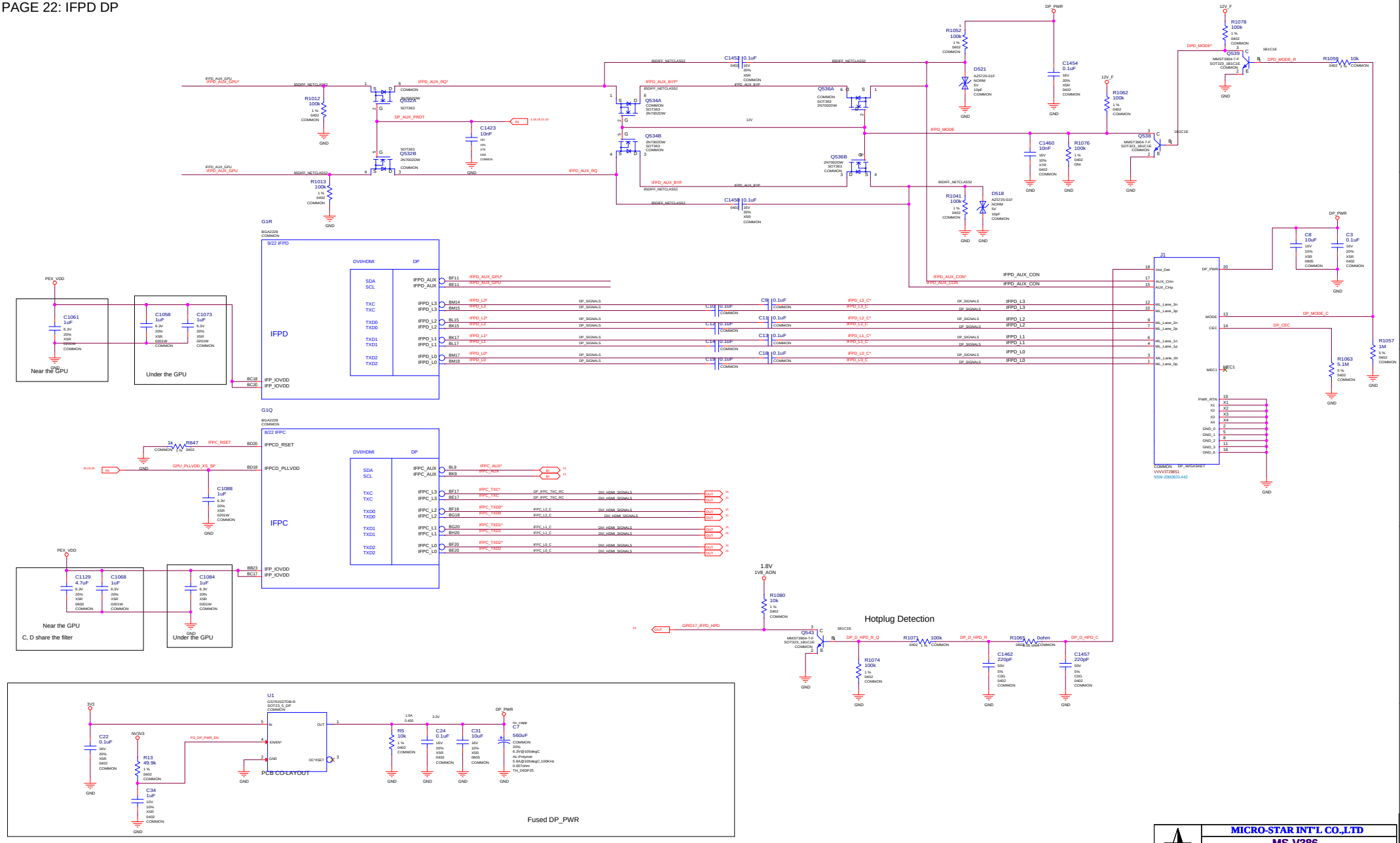
PAGE 21:IFPC HDMI 2.0/DP



PAGE 22: IFPD DP



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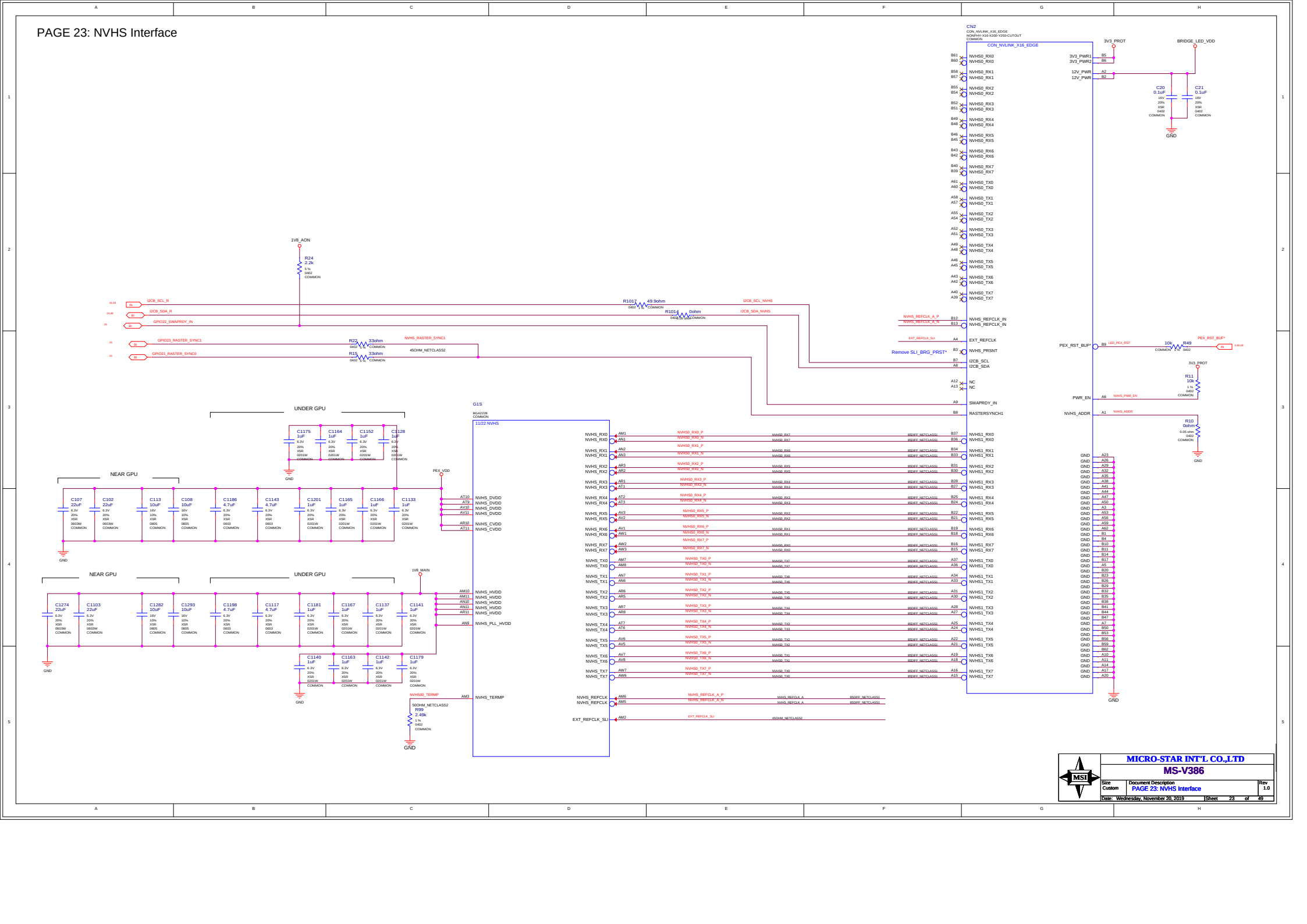
PAGE 23: NVHS Interface



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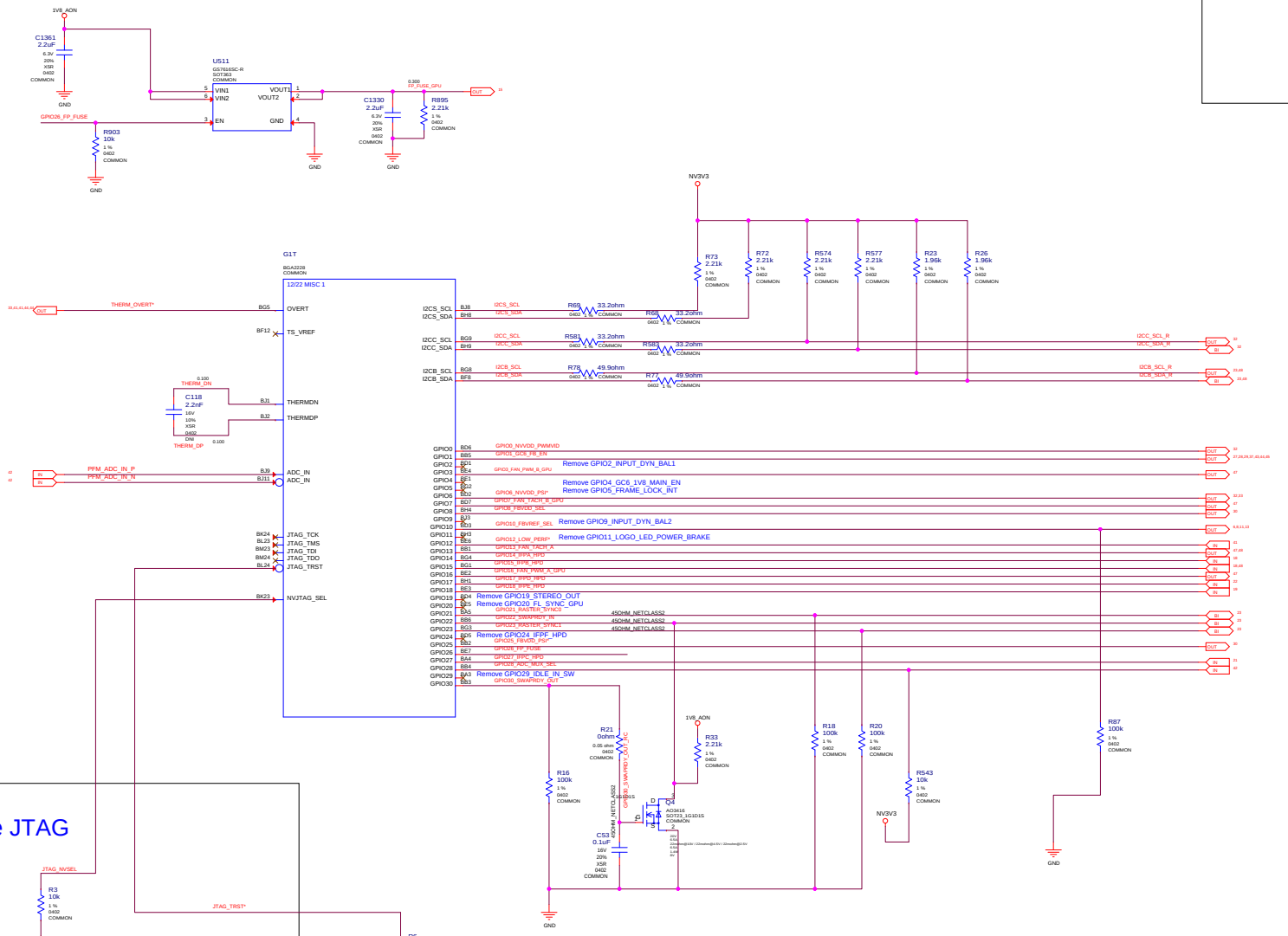
Remove POWER_BRAKE*



Remove JTAG

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PAGE 25: MISC: ROM, Straps

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]		
L	L	L	00000	RAMCFG TBD	
L	L	H	00001	RAMCFG TBD	DEFAULT
L	H	L	00010	RAMCFG TBD	
L	H	H	00011	RAMCFG TBD	
H	H	L	00110	RAMCFG TBD	
H	H	H	00111	RAMCFG TBD	

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

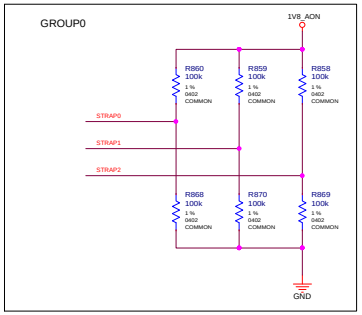
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

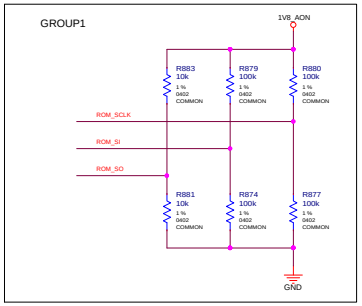
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

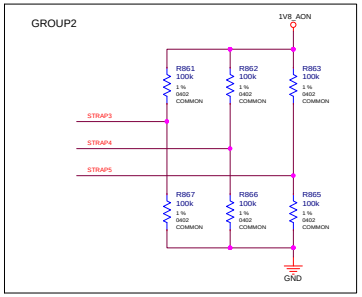
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

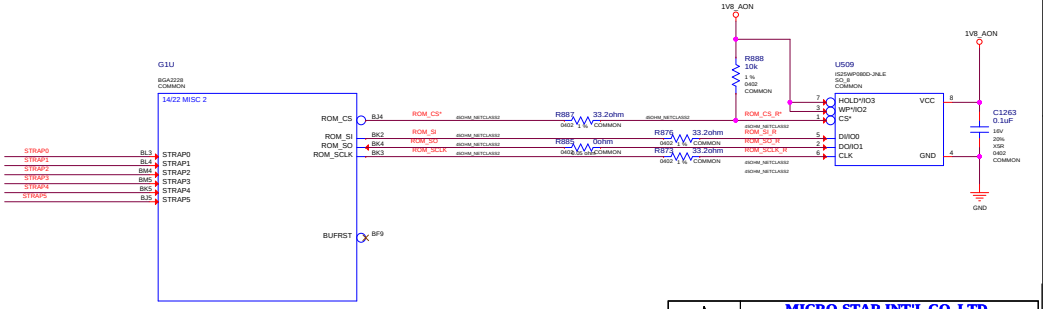
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

Default









MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V386	
Size: Custom	Document Description: PAGE 25: MISC: ROM, Straps	Rev: 1.0
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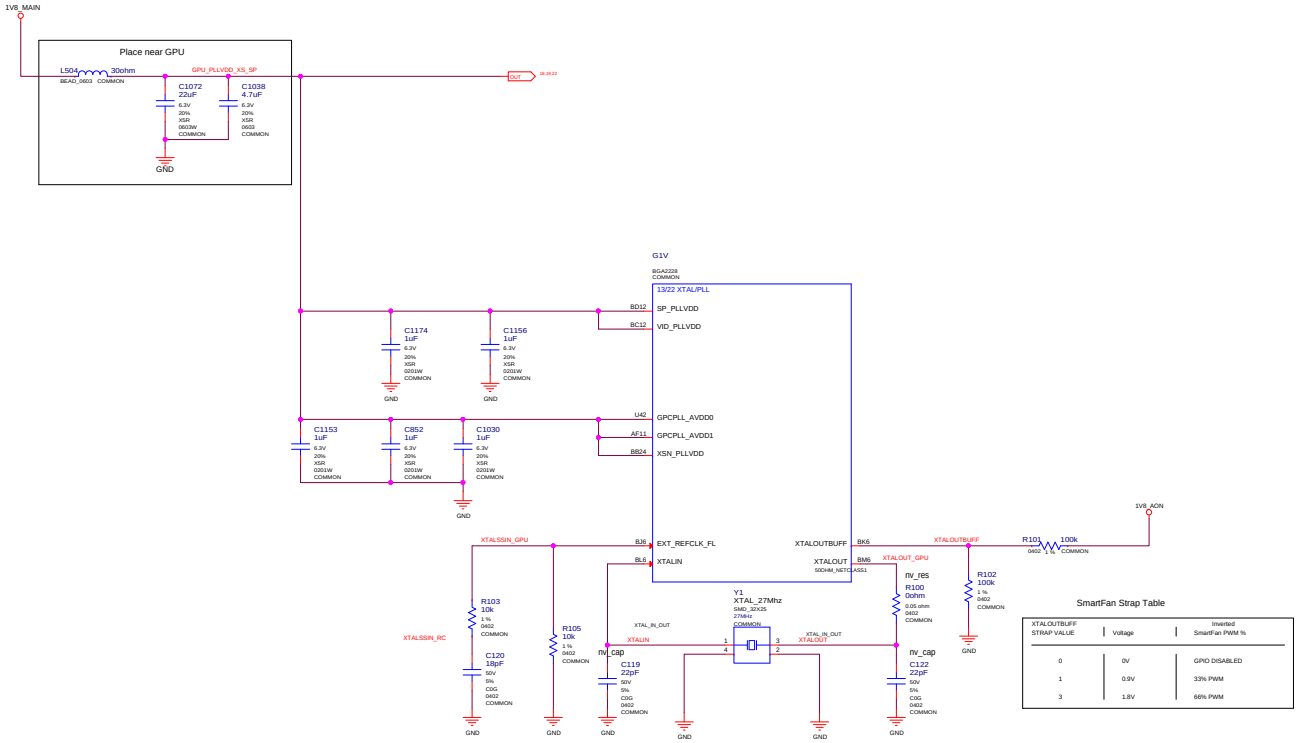
PAGE 26: MISC: XTAL. PLL



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V386	
Size: Custom	Document Description: PAGE 26: MISC: XTAL. PLL	Rev: 1.0
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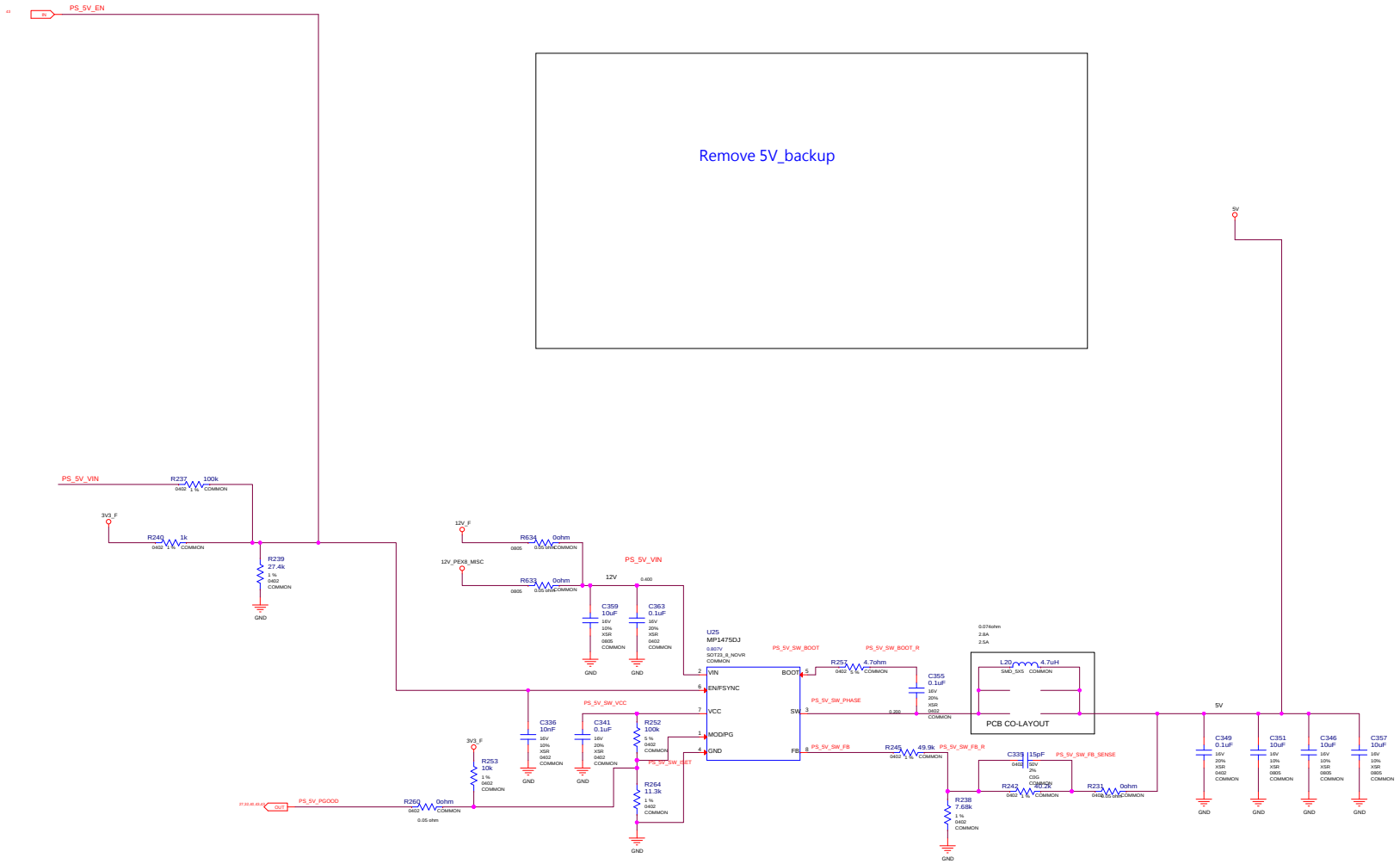
PAGE 27: PS: 5V, 5V_BACKUP



0.8V*(1+40.2K/7.68K)=4.9875V

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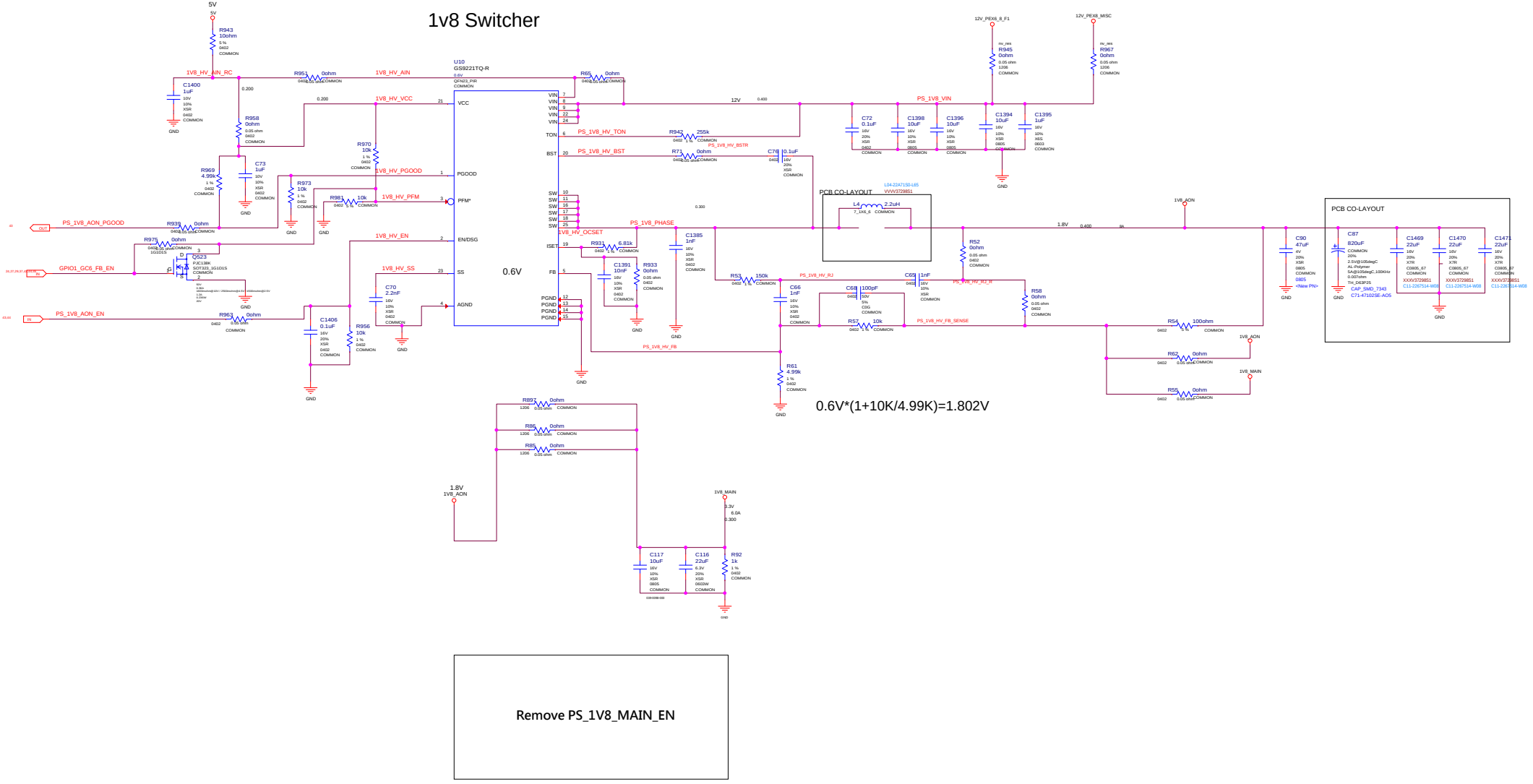
PAGE 28: PS: 1V8

1v8 Switcher



Remove PS_1V8_MAIN_EN

MICRO-STAR INT'L CO.,LTD	
MS-V386	
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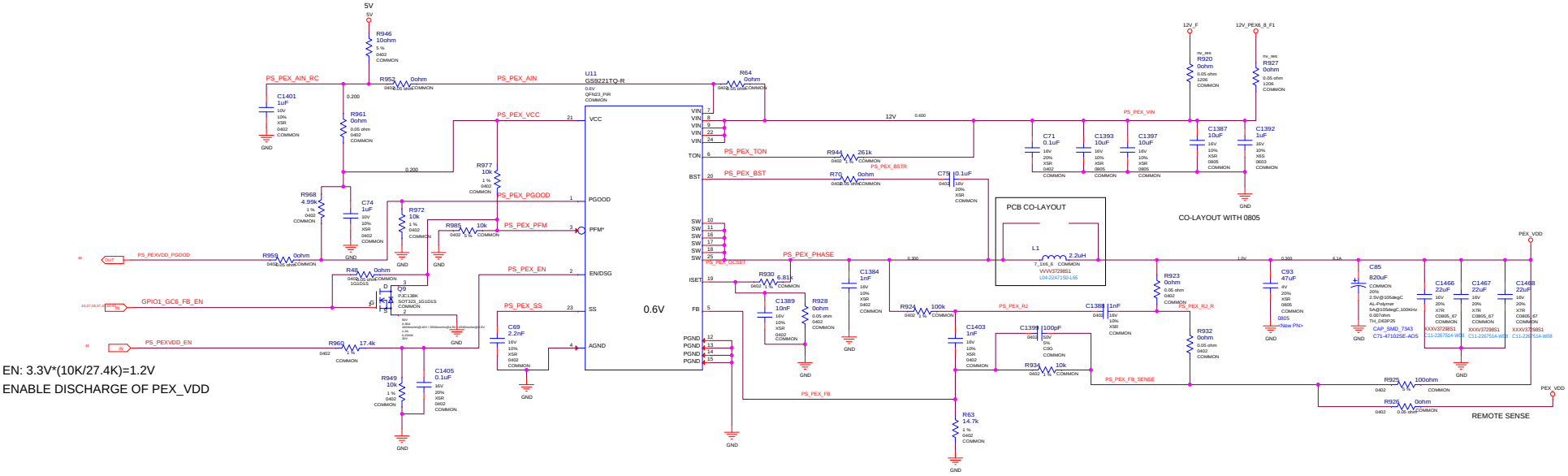
PEX Switcher



EN: 3.3V*(10K/27.4K)=1.2V

ENABLE DISCHARGE OF PEX_VDD

0.6V*(1+10K/14.7K)=1.008V

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MS-V386		
Size: Custom	Document Description: PAGE 29: PS: PEXVDD	Rev: 1.0
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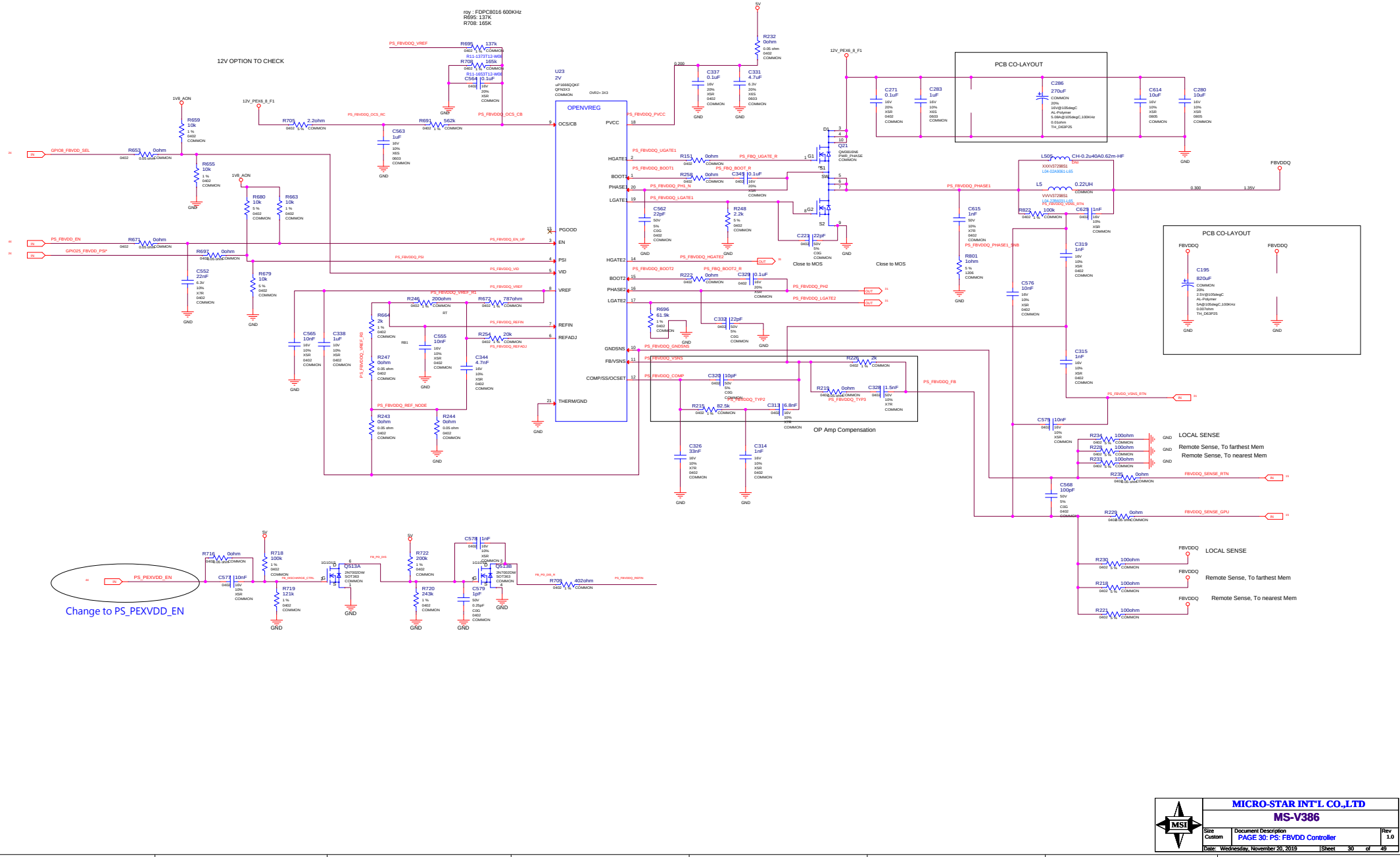
PAGE 30: PS: FBVDD Controller



MICRO-STAR INT'L CO.,LTD	
MS-V386	
Size: Custom	Document Description: PAGE 30: PS: FBVDD Controller
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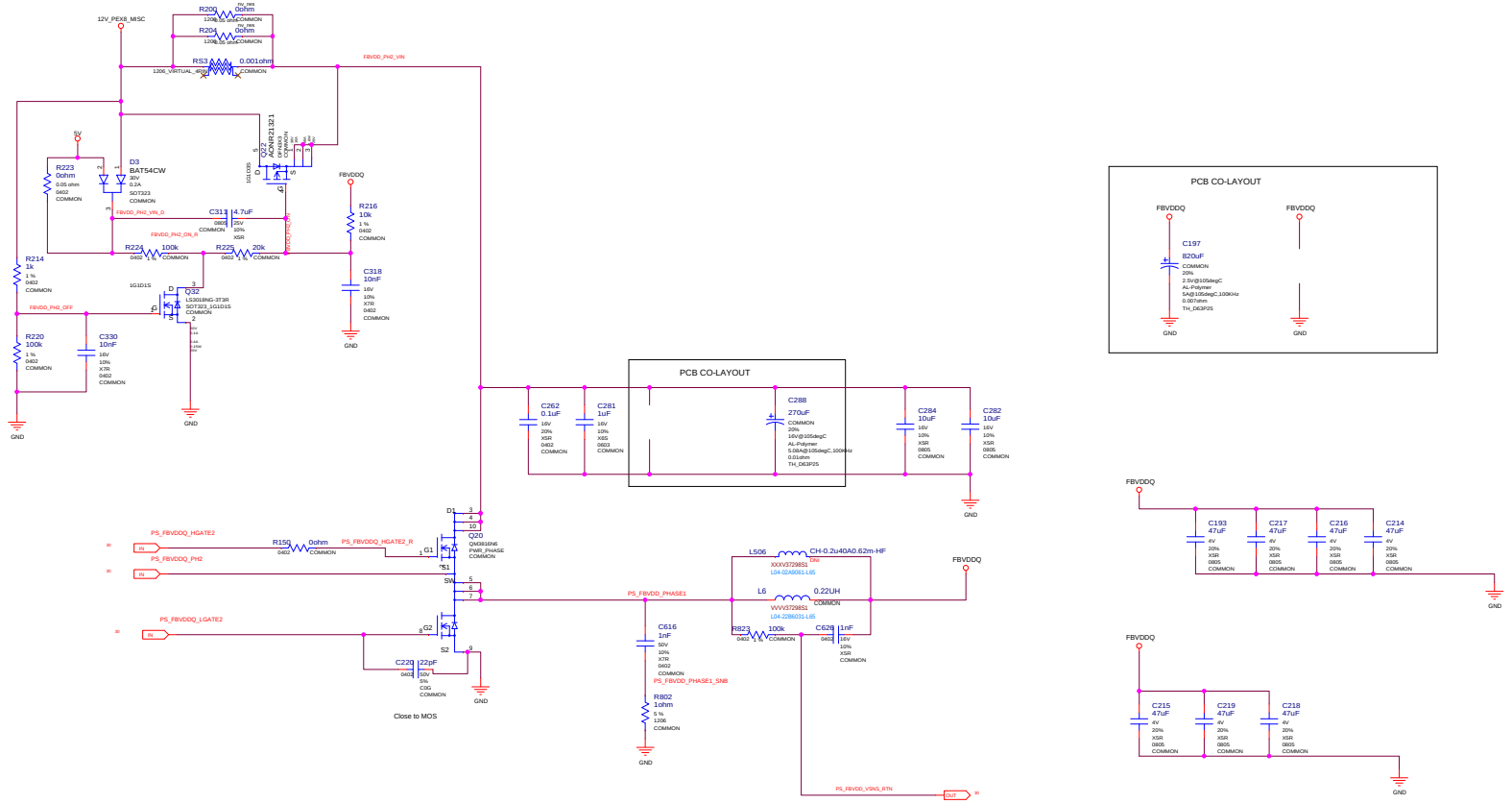
PAGE 31: PS: FBVDD Phase 1, 2



MICRO-STAR INT'L CO.,LTD		
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Size: Custom	Document Description: PAGE 31: PS: FBVDD Phase 1, 2	Rev: 1.0
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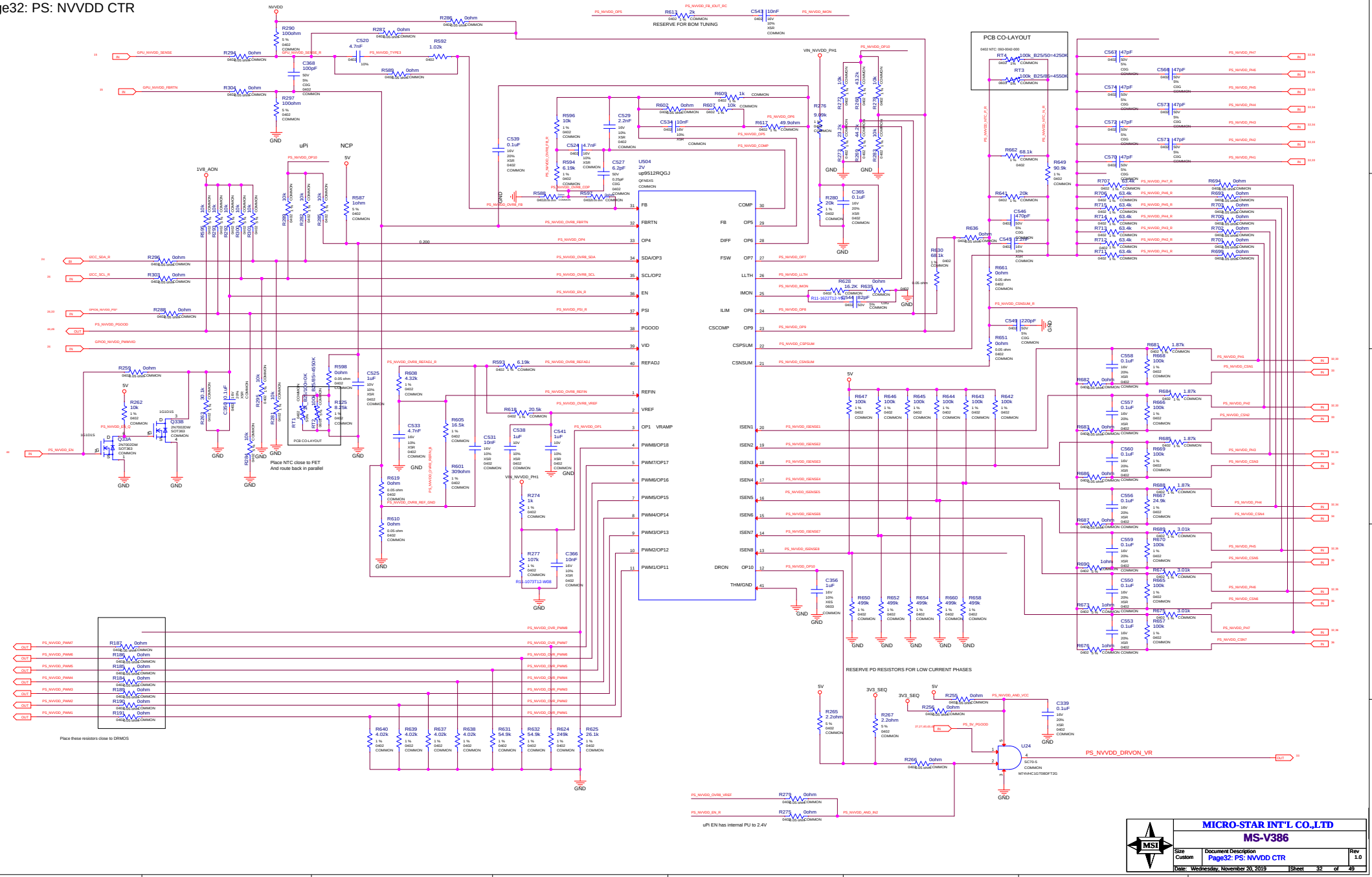
Page32: PS: NVVDD CTR



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Size	Document Description	Rev
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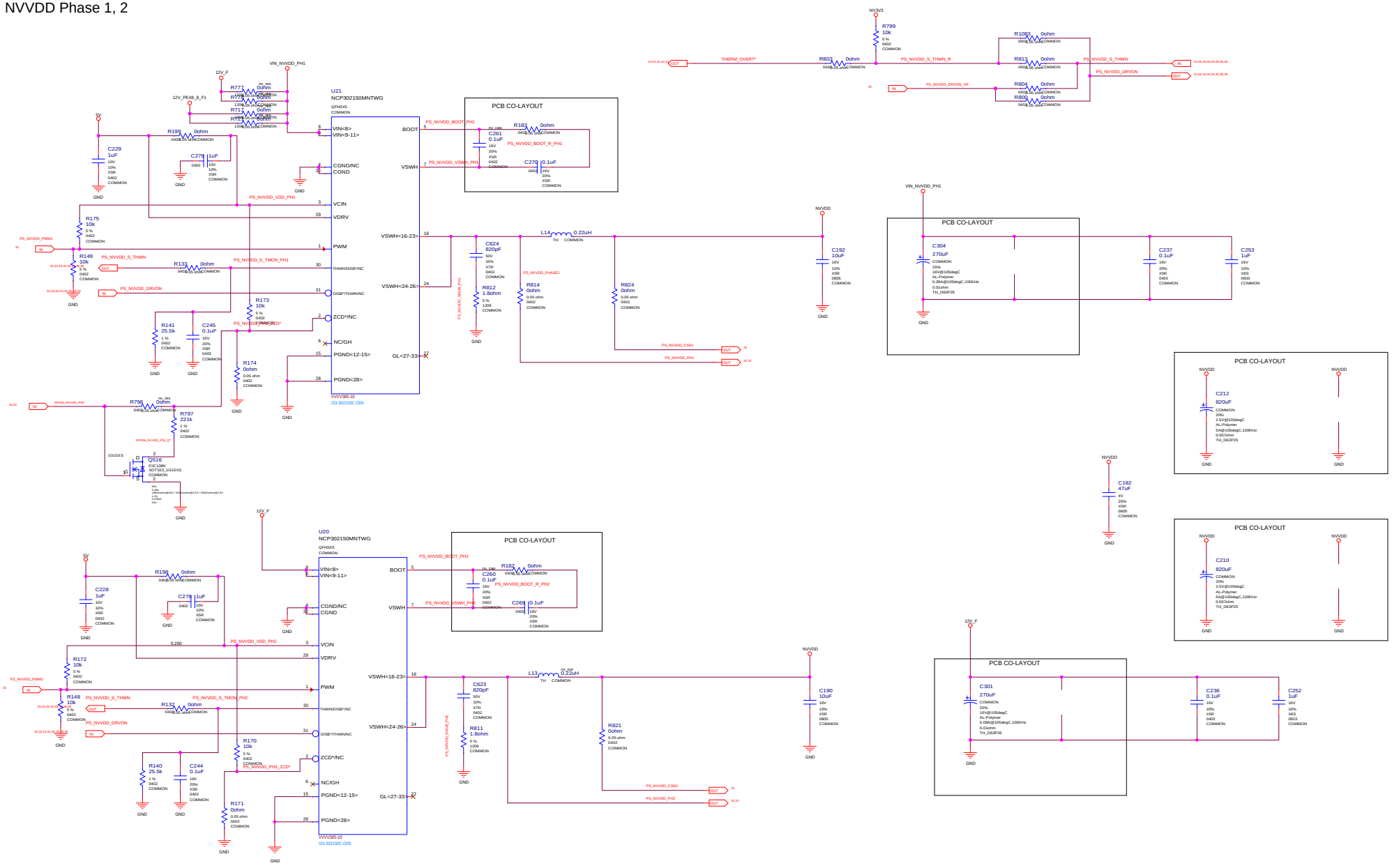
PAGE 33: PS: NVVDD Phase 1, 2



MICRO-STAR INT'L CO.,LTD	
MS-V386	
Size: Custom	Document Description: PAGE 33: PS: NVVDD Phase 1, 2
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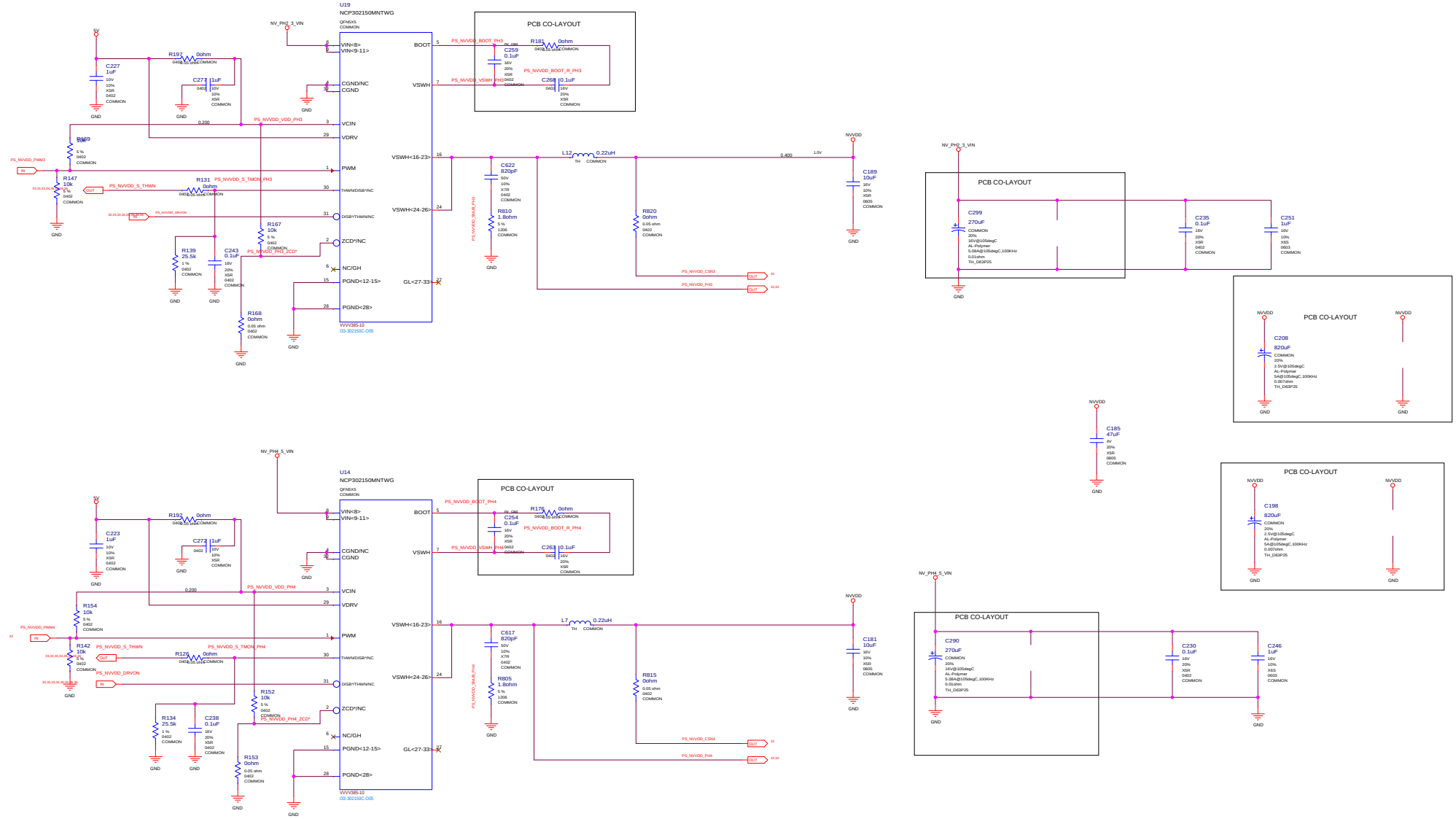
PAGE 34: PS: NVVDD Phase 3, 4



MICRO-STAR INT'L CO.,LTD	
MS-V386	
Size: Custom	Document Description: PAGE 34: PS: NVVDD Phase 3, 4
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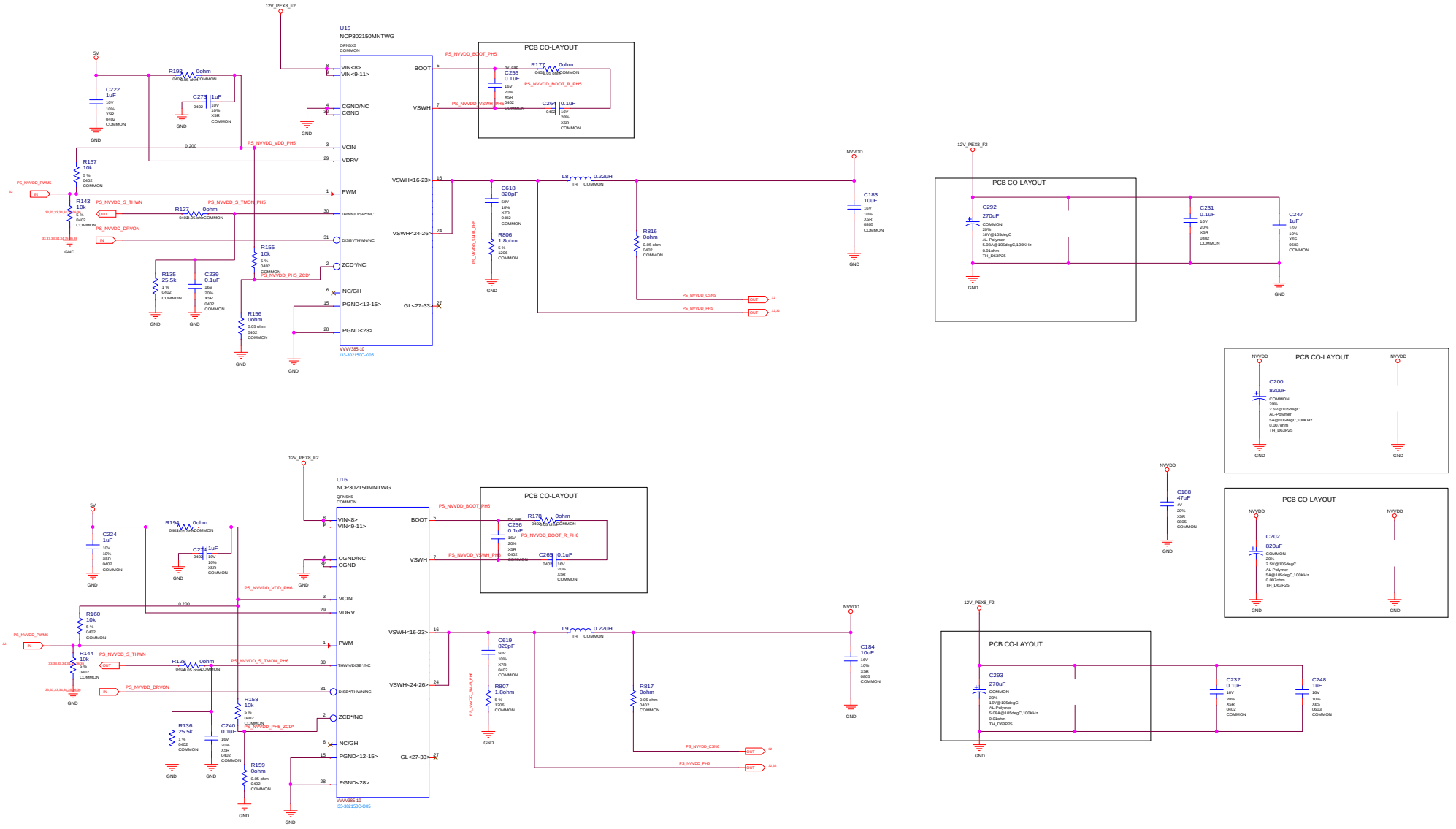
PAGE 35: PS: NVVDD Phase 5, 6



MICRO-STAR INT'L CO.,LTD	
MS-V386	
Size: Custom	Document Description: PAGE 35: PS: NVVDD Phase 5, 6
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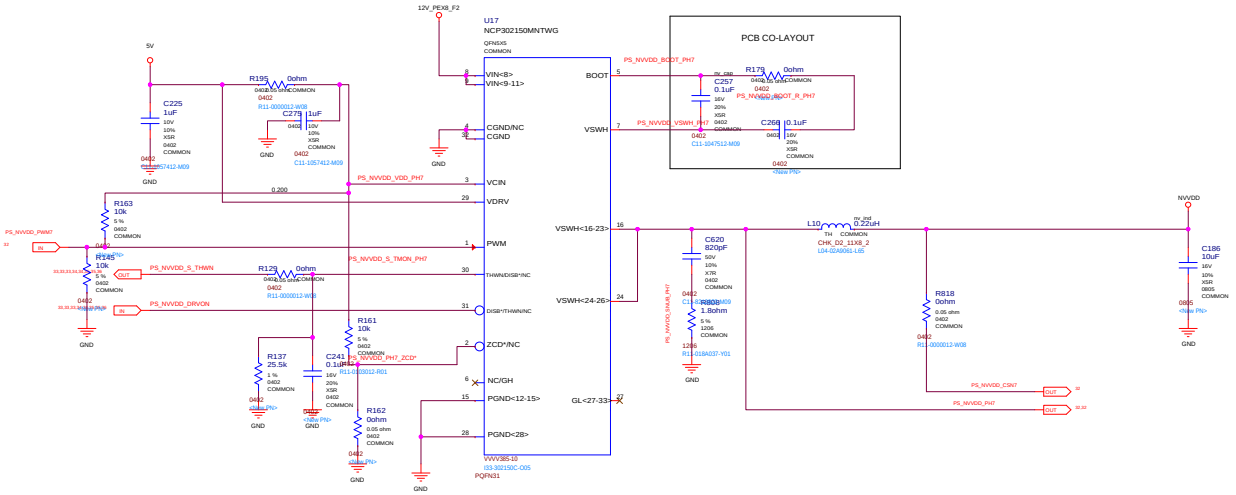
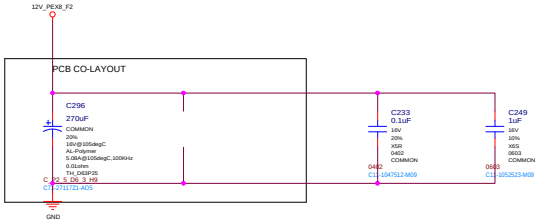
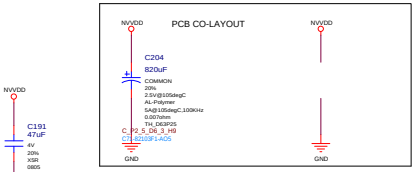
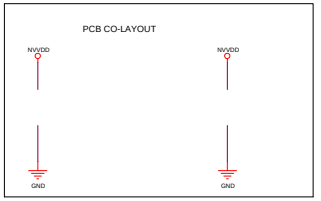
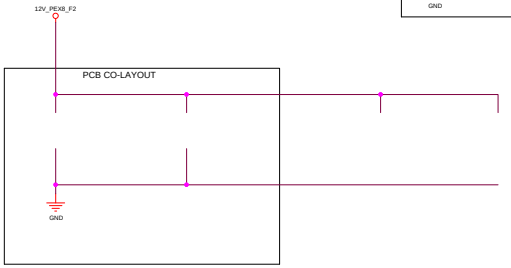
PAGE 36: PS:NVVDD Phase 7, 8











Remove Phase 8

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MS-V386		
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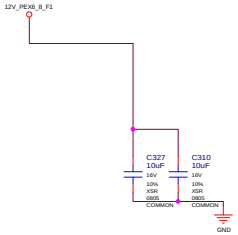
PAGE 37: PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

Remove RTD3



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Custom	PAGE 37: PS: INPUT SWITCH RTD3	1.0

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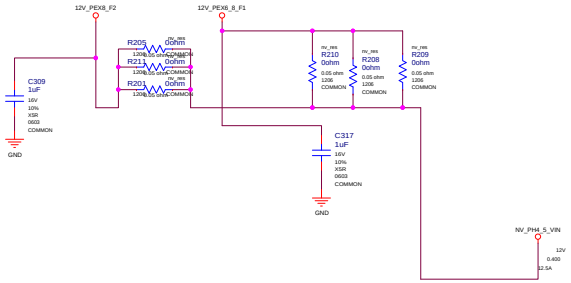
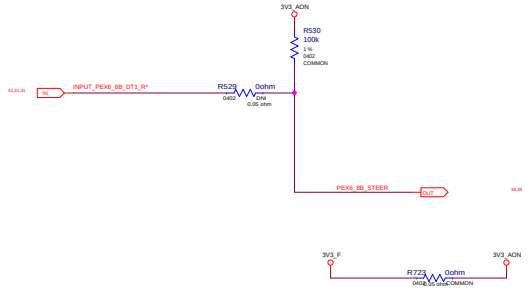
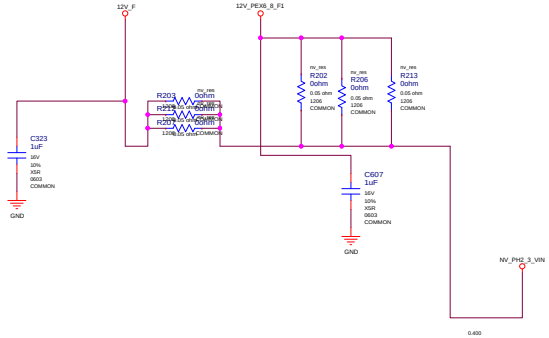
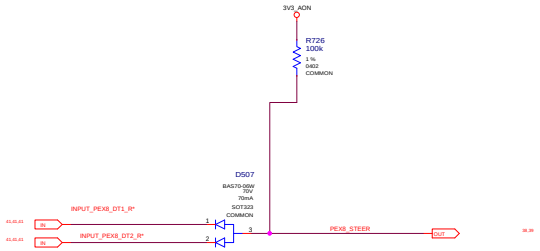
PAGE 38: PS: INPUT SWITCH Rail Balance



Remove POWER Balance







MICRO-STAR INT'L CO.,LTD		
MS-V386		
Size: Custom	Document Description: PAGE 38: PS: INPUT SWITCH Rail Balance	Rev: 1.0
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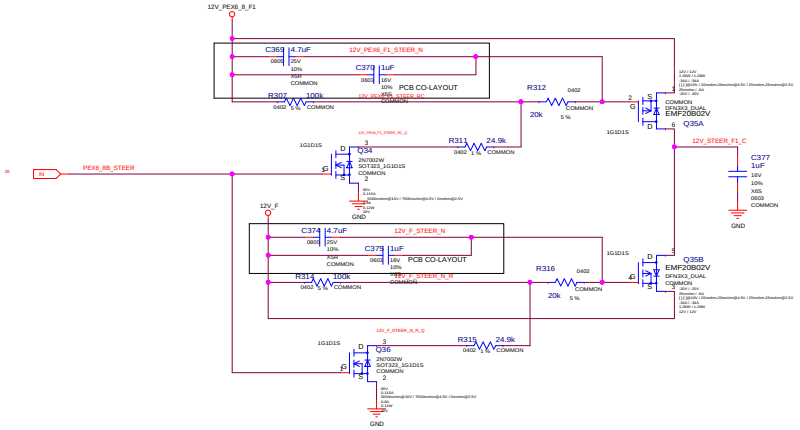
PAGE 39: PS: 12V CURRENT STEERING

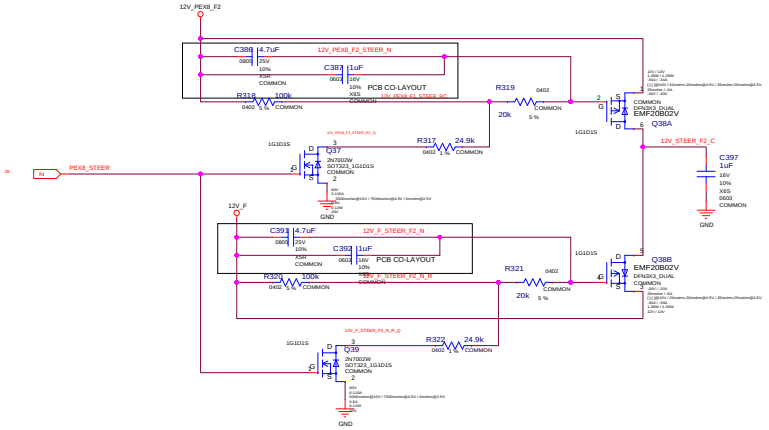
12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



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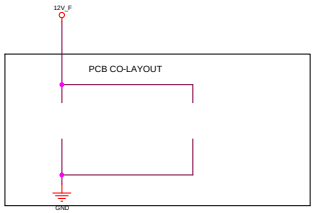
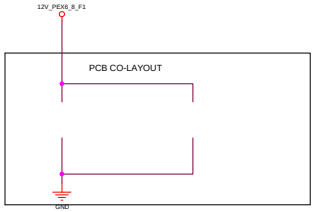
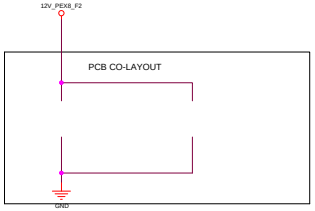
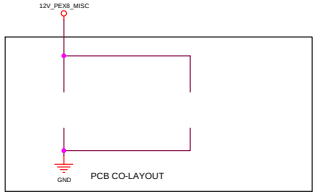
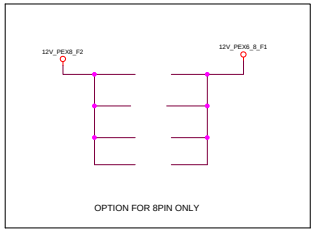
PAGE 40: PS: Inputs, Filtering, and Monitoring











PEX6 INPUT 1 - 2x3 PCIE CON 75W

Remove 3V3_AUX_FUSE

PEX8 INPUT 2 - 2x4 PCIE CON 150W

PEX 3V3 INPUT - 10W

PEX_12V INPUT - 66W

MICRO-STAR INT'L CO.,LTD			
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Size: Custom	Document Description: PAGE 40: PS: Inputs, Filtering, and Monitoring		Rev: 1.0
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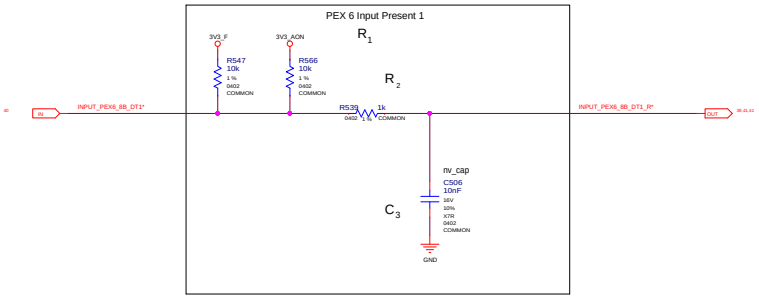
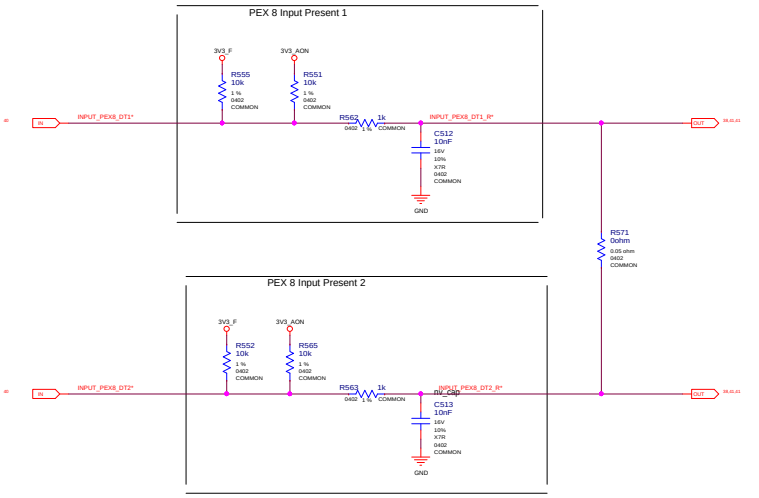
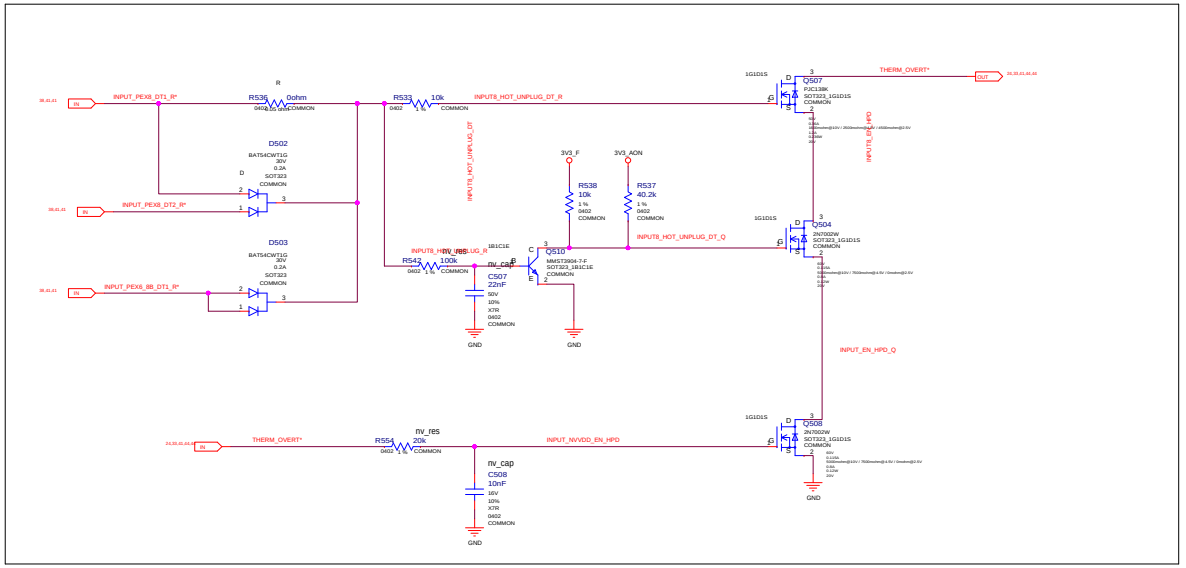
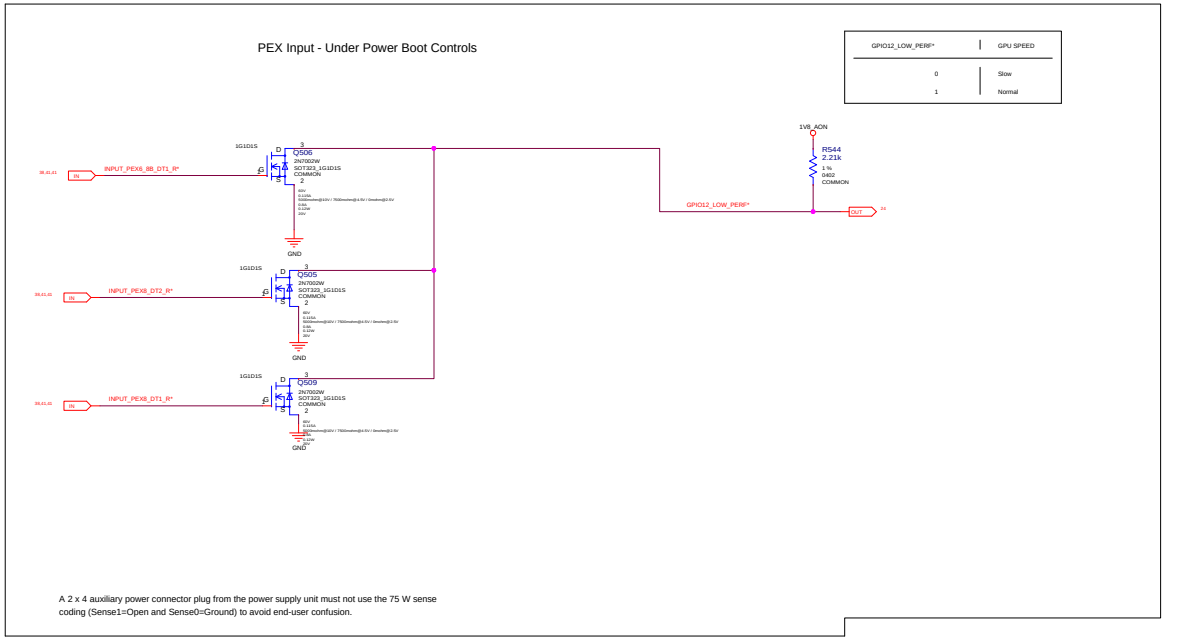
PAGE 41: PS: Current Steering, Hot Unplug Detect









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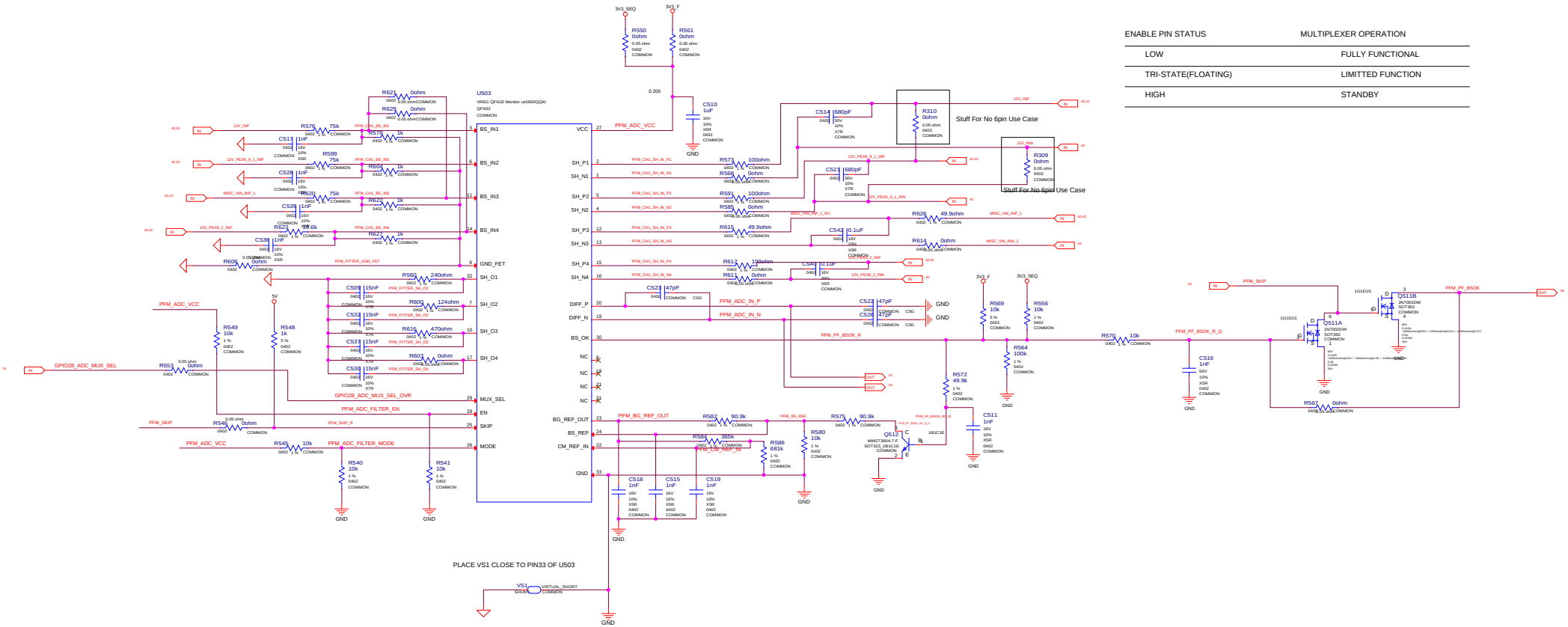
MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY



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Size: Custom	Document Description: PAGE42; PS: Pre-Filter	Rev: 1.0
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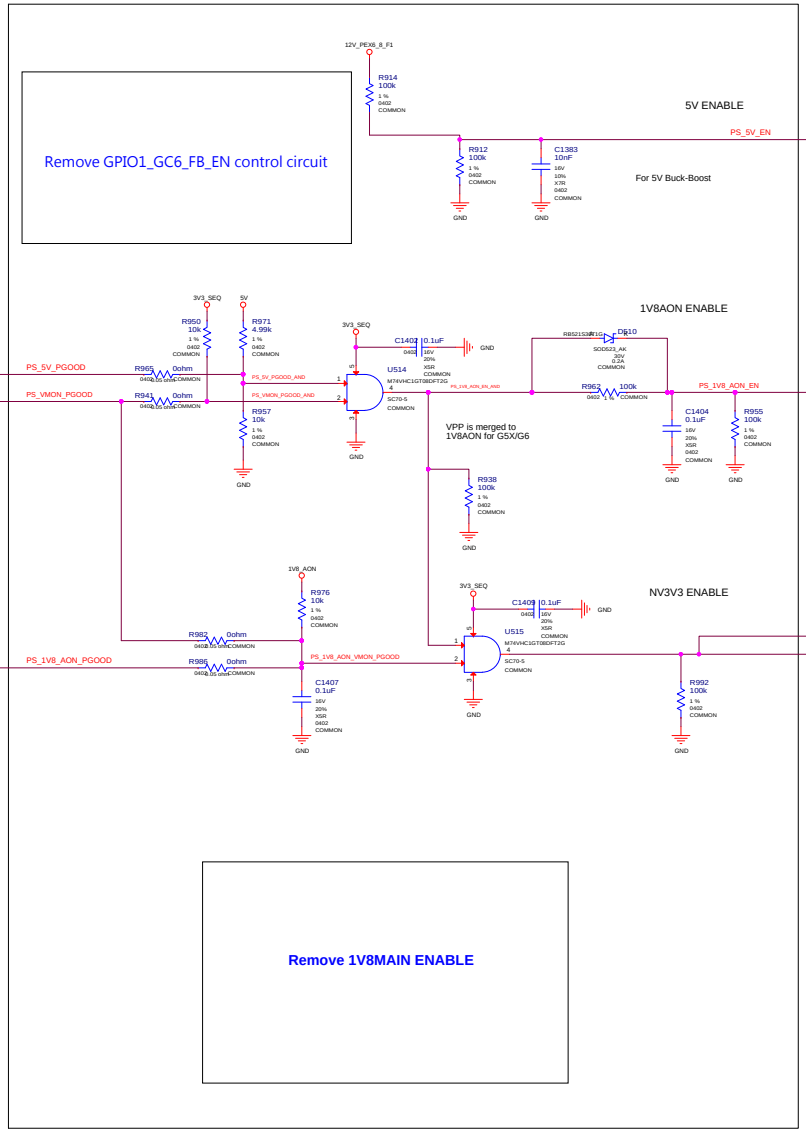
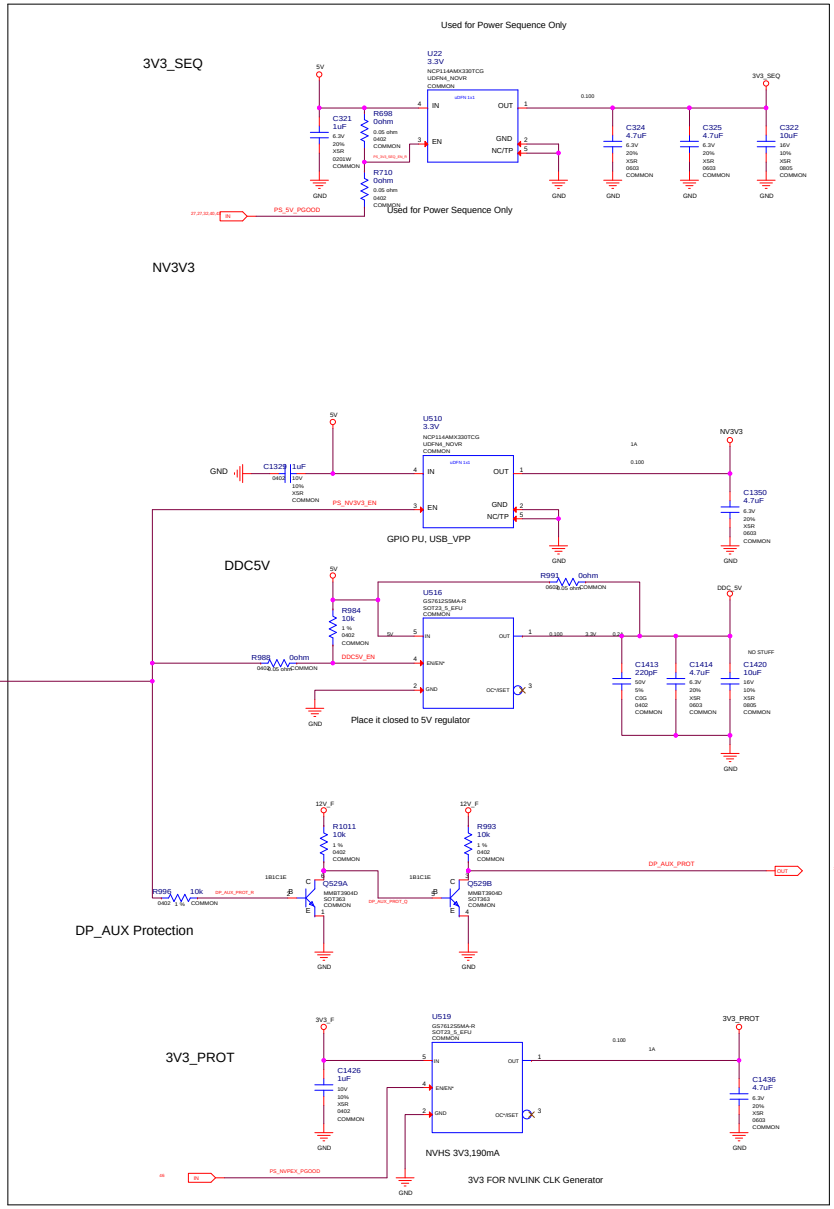
PAGE 43: SEQUENCE:5V,1V8,NV3V3 ENABLE





MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V386	
Size: Custom	Document Description: PAGE 43: SEQUENCE:5V,1V8,NV3V3 ENABLE	Rev: 1.0
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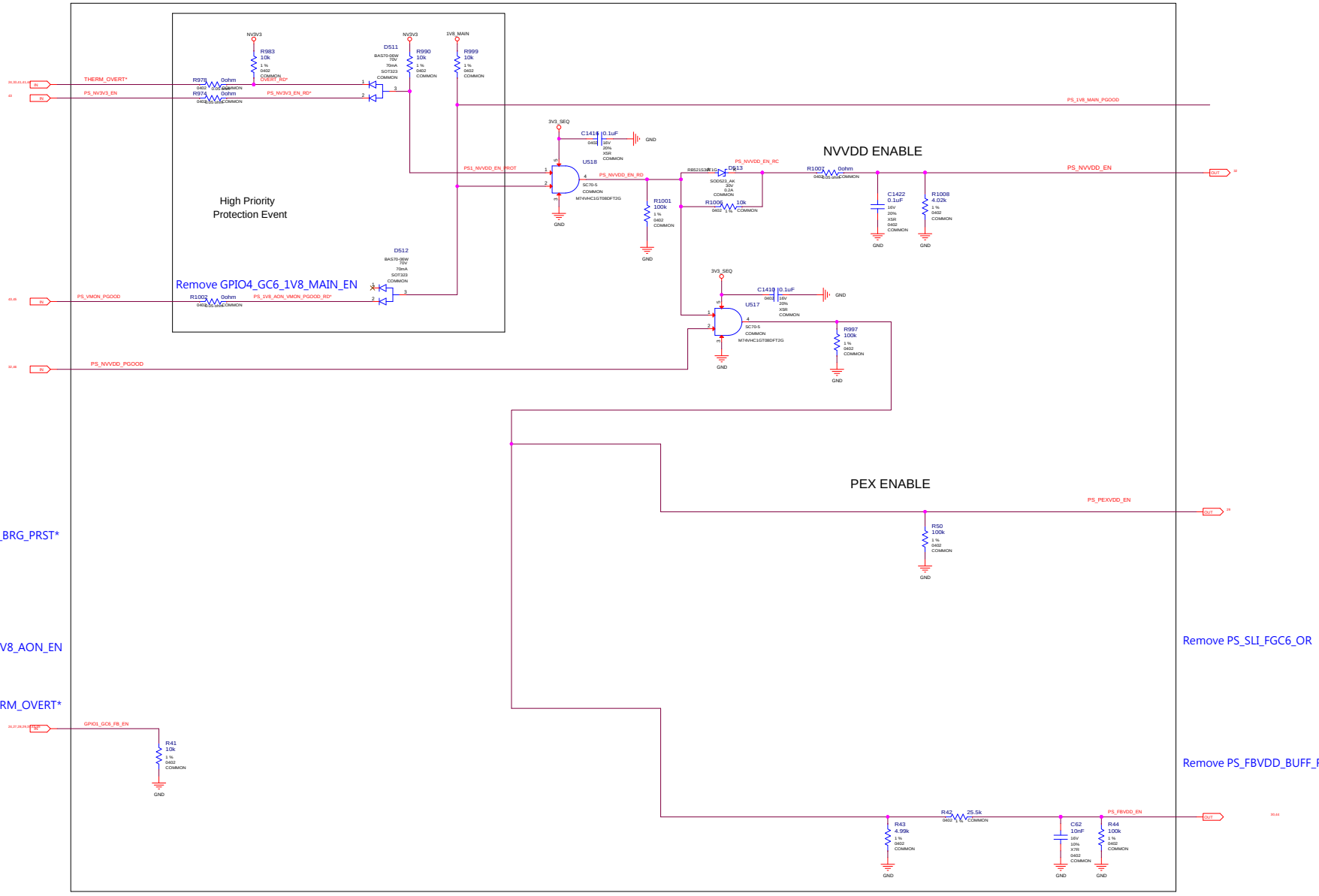
PAGE 44: SEQUENCE:NV,PEX,FB ENABLE



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Size: Custom	Document Description: PAGE 44: SEQUENCE:NV,PEX,FB ENABLE	Rev: 1.0
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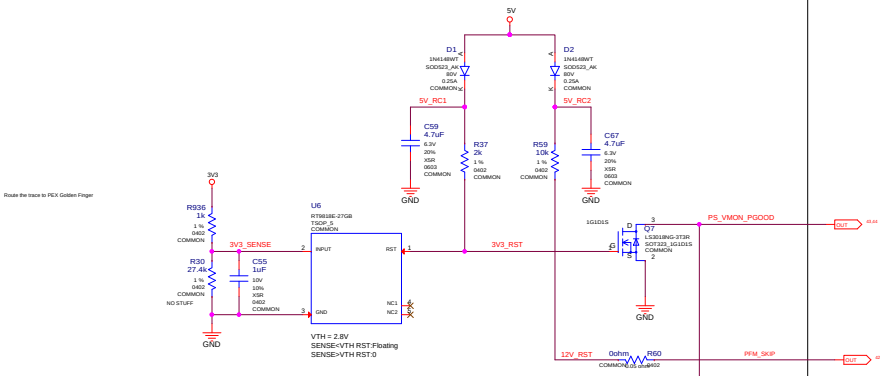
PAGE 45: SEQUENCE:PCIE VOLTAGE MONITOR

PCIE Voltage Monitor



Remove :

1.GPIO1_GC6_FB_EN

2.12V Voltage Moniton

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX

and All Input 12Vs

MICRO-STAR INT'L CO.,LTD

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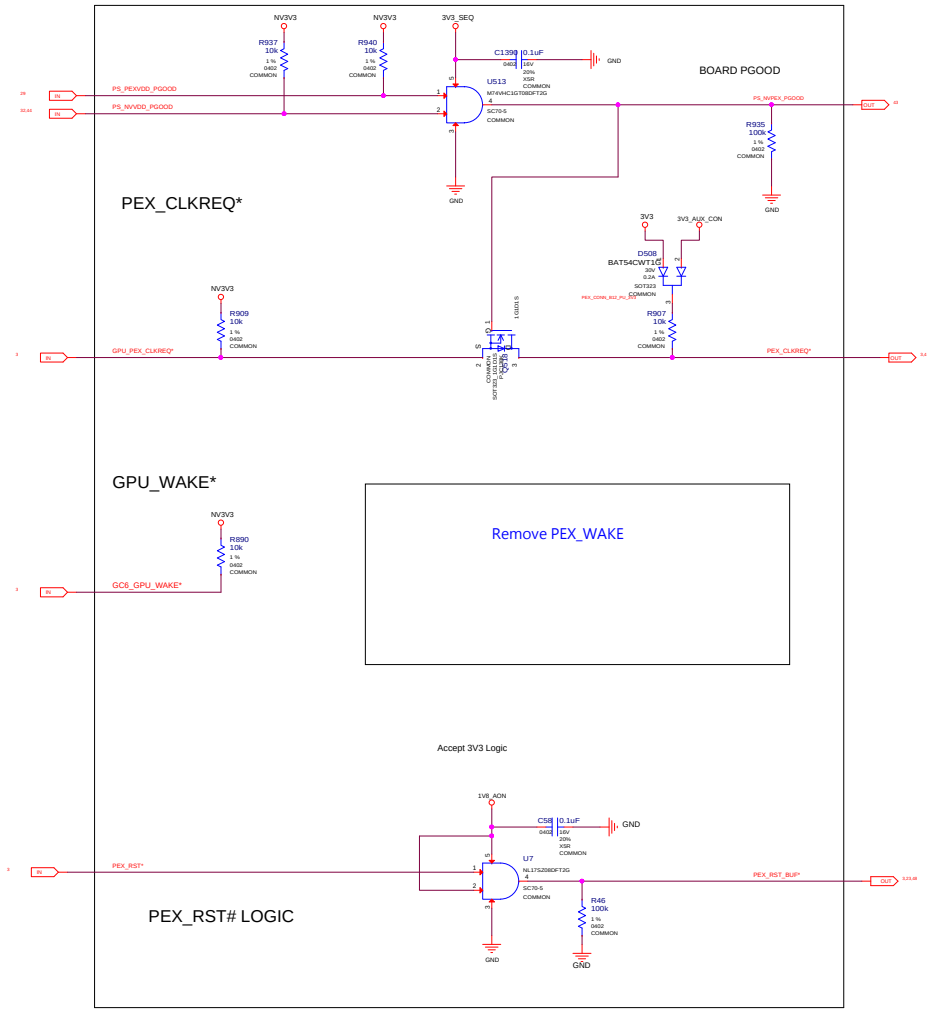

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Size: Custom	Document Description: PAGE 46: SEQUENCE:MISC	Rev: 1.0
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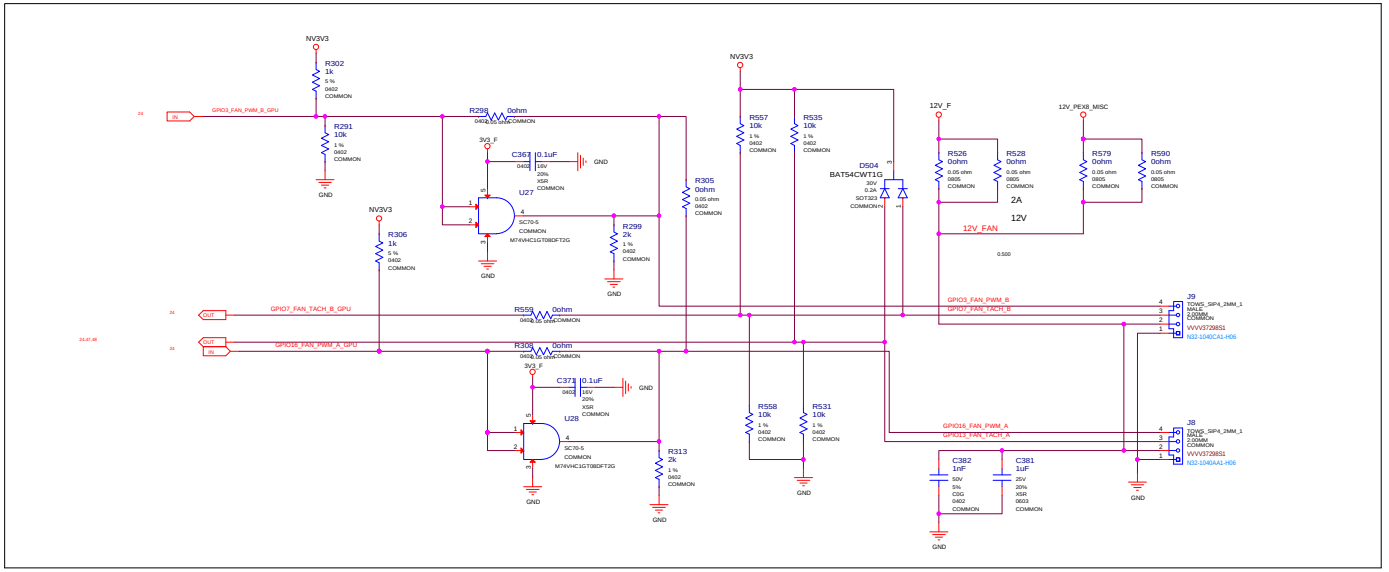
PAGE 47: LED & FAN HEADERS

Remvoe LED



Remove LED BOOST

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Remove LED2

PAGE 49:MECHANICAL;BRACKET/THERMAL SOLUTION

Brackets:

BKT1
BRACKET
ATX_2X_2P
COMMON

MECH MOUNTING ALL

GND

Bracket Screw

1

MEC4
PH_M2.5X4.5X10MM_SCREW
STEEL
COMMON

new LF screw --335-00001-000.
ROHS screw --154-0003-700.

HDMI_FEE

HDMI
$$$$$$

HDMI_FEE
COMMON
VVVV386-10
YGL-RHDM003-000

PCB

PCB

109-GN982-00A

COMMON
VVVV386-10
PS0-SV3B110-E48

BKTSCREW1

SCREW

VVVV386-10
E41-1304010-H75

BKTSCREW2

SCREW

VVVV386-10
E41-1304010-H75

HDMISCREW1

SCREW

VVVV386-10
E43-1303012-H75

EMI CLIPs

GND

BOARD STIFFENER

No connected mounting pins

MEC501
NOPIN
COMMON

STIFFENER

GPU Mounting holes

MEC2-1
MEC2-2
MEC2-3
MEC2-4
MEC2-5
MEC2-6
MEC2-7
MEC2-8

XB
COMMON

GND

Mechanical Holes Symbol

MEC10
MEC11
MEC12
MEC13
MEC14
MEC15
MEC16
MEC18

H_R220D125

DNI

XXXV3729BS1
<New PN>

GND

GPU Socket Symbol

BGA SOCKET ASSY

12 connected mounting pins

MEC3
128PIN
COMMON

GND

FM1 FM2 FM3 FM4 FM5 FM6 FM7 FM8

OPT
F_PAD_X
XXXV3729BS1
<New PN>

J18
J19

3 1
4 2

impedence

XXXV3729BS1
<New PN>

J17

X_PIN1*2

XXXV3729BS1
<New PN>

J16

X_PIN1*2

XXXV3729BS1
<New PN>

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MS-V386

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