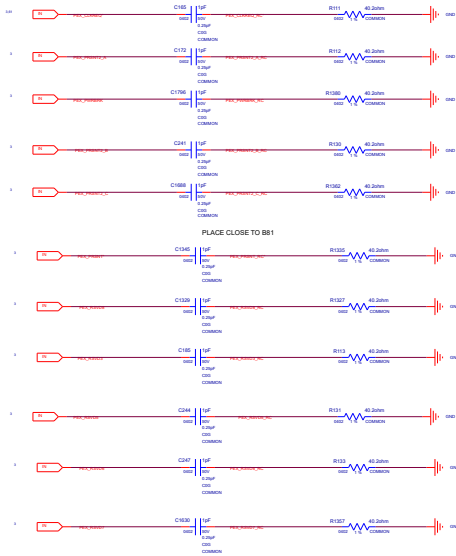
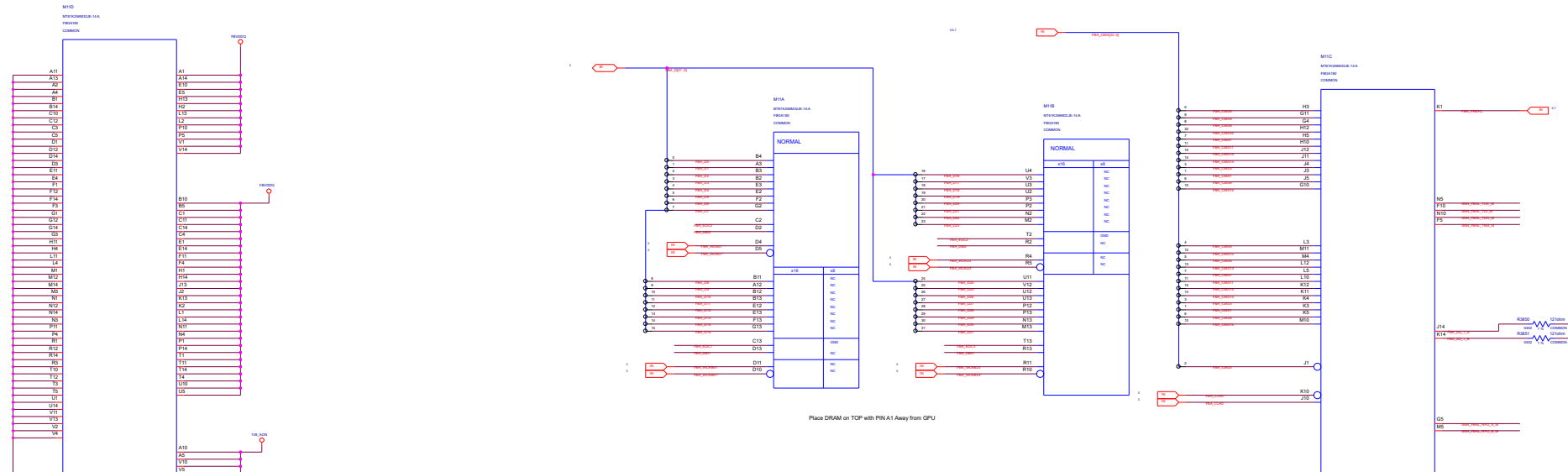


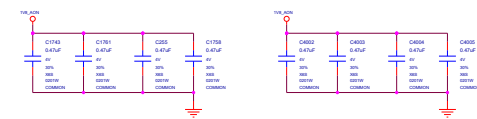
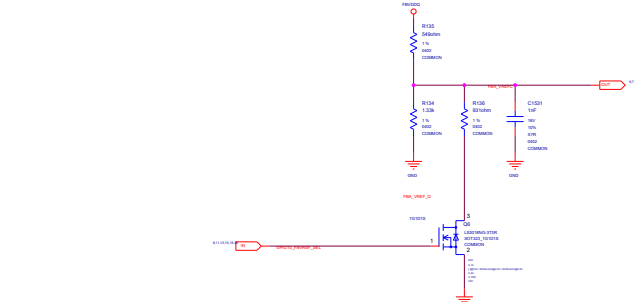
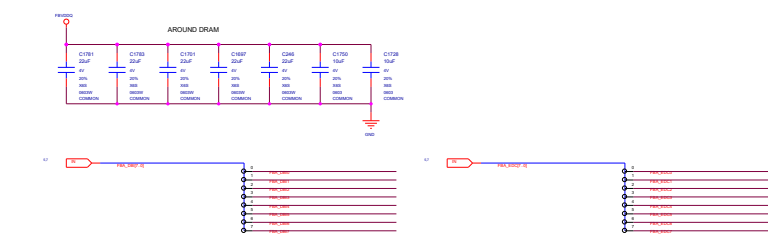
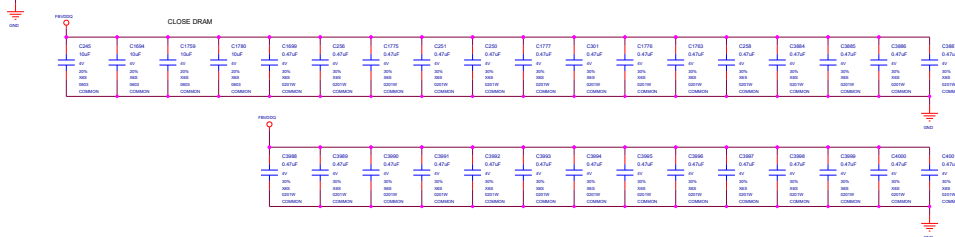
PCI TERM



MEMORY: FBA Partition 31..0



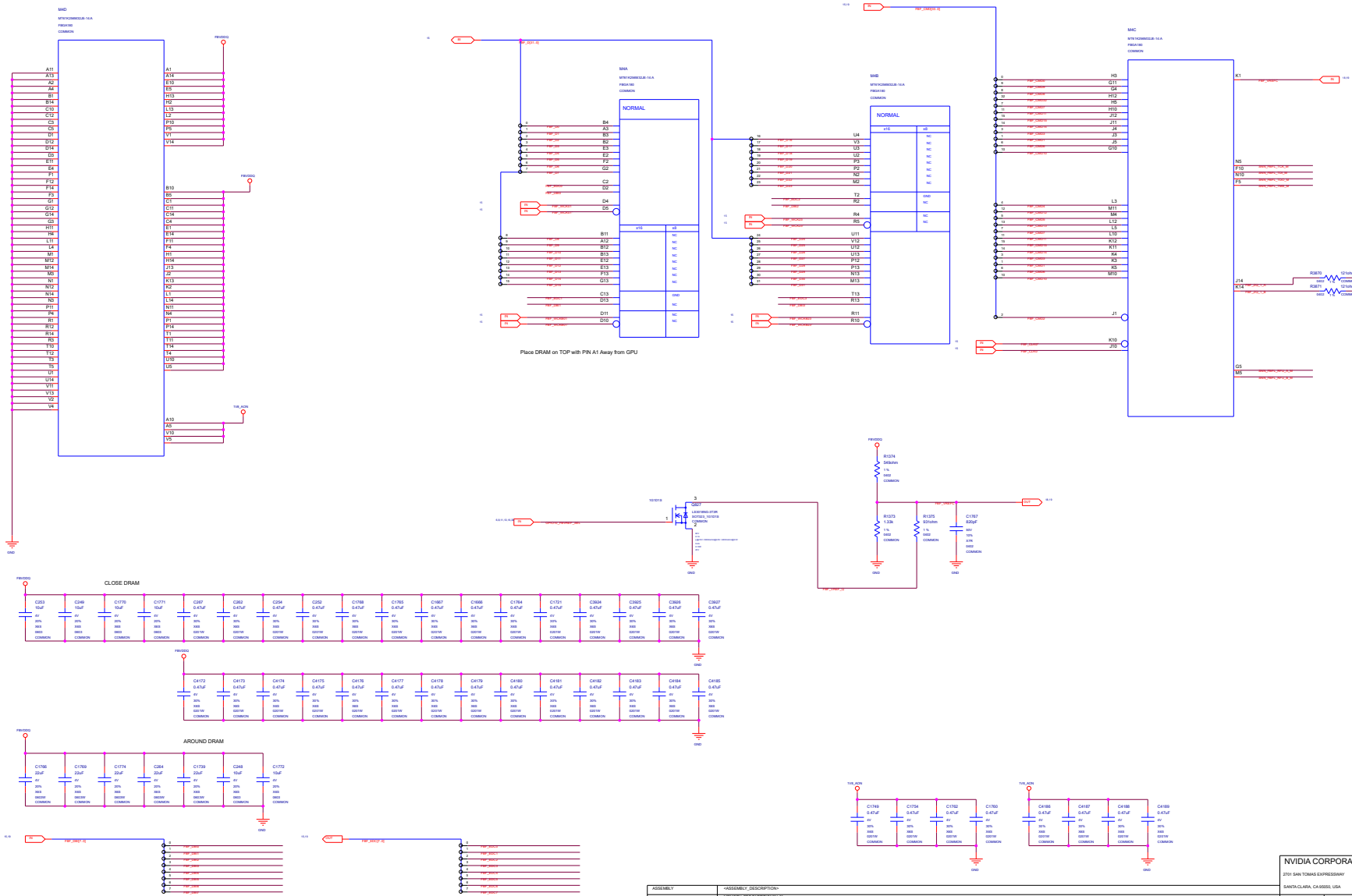
Place DRAM on TOP with PIN A1 Away from GPU



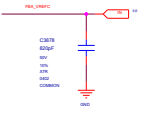
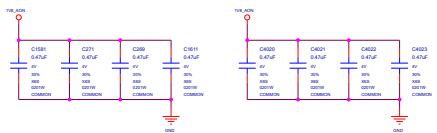
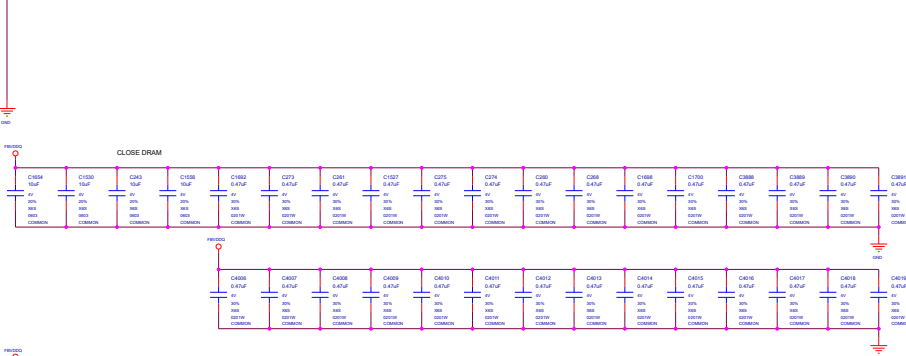
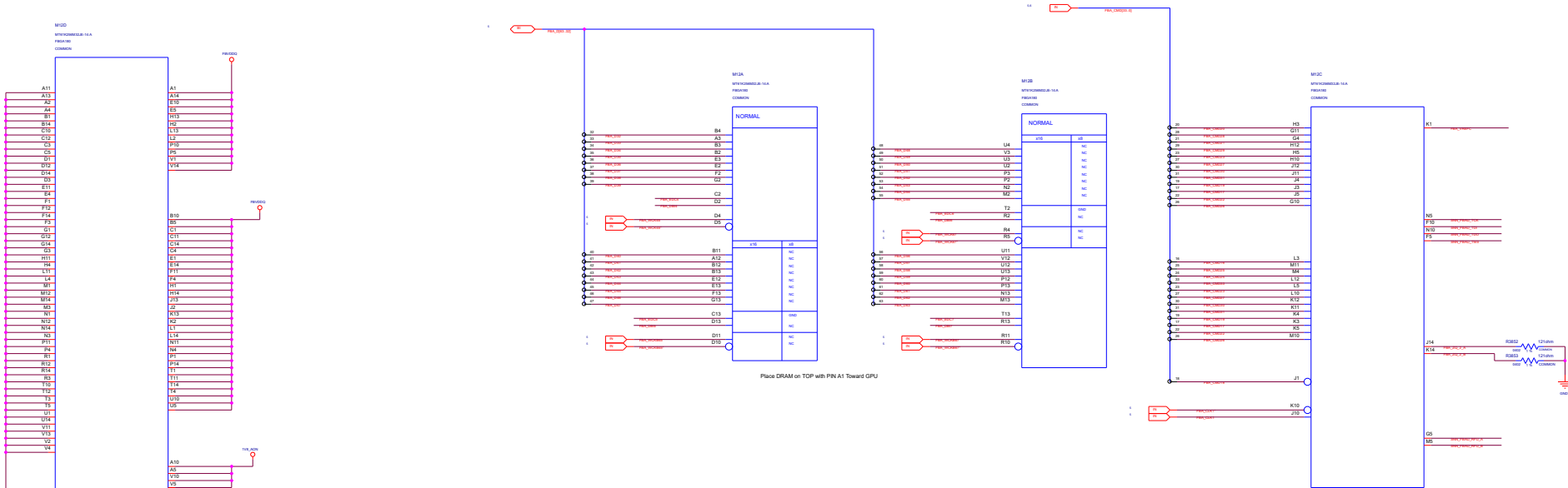
ASSEMBLY		ASSEMBLY DESCRIPTION	
FILE: 31..0		MEMORY: FBA PARTITION 31..0	

NVIDIA CORPORATION		© 2016 NVIDIA CORPORATION	
SANTA CLARA, CA 95050, USA		SANTA CLARA, CA 95050, USA	
PNV_PN	800-1G150-BASE-403	PNV_PN	8 OF 86
PCB REV	PCB150-003	PNV_PN	
DATE	16-JUL-2016	DATE	

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

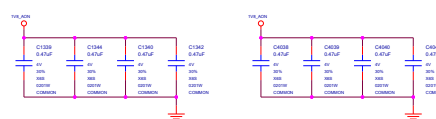


ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, EXCLUSIVE OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.



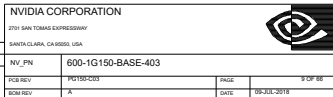
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, EXCLUSIVE OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

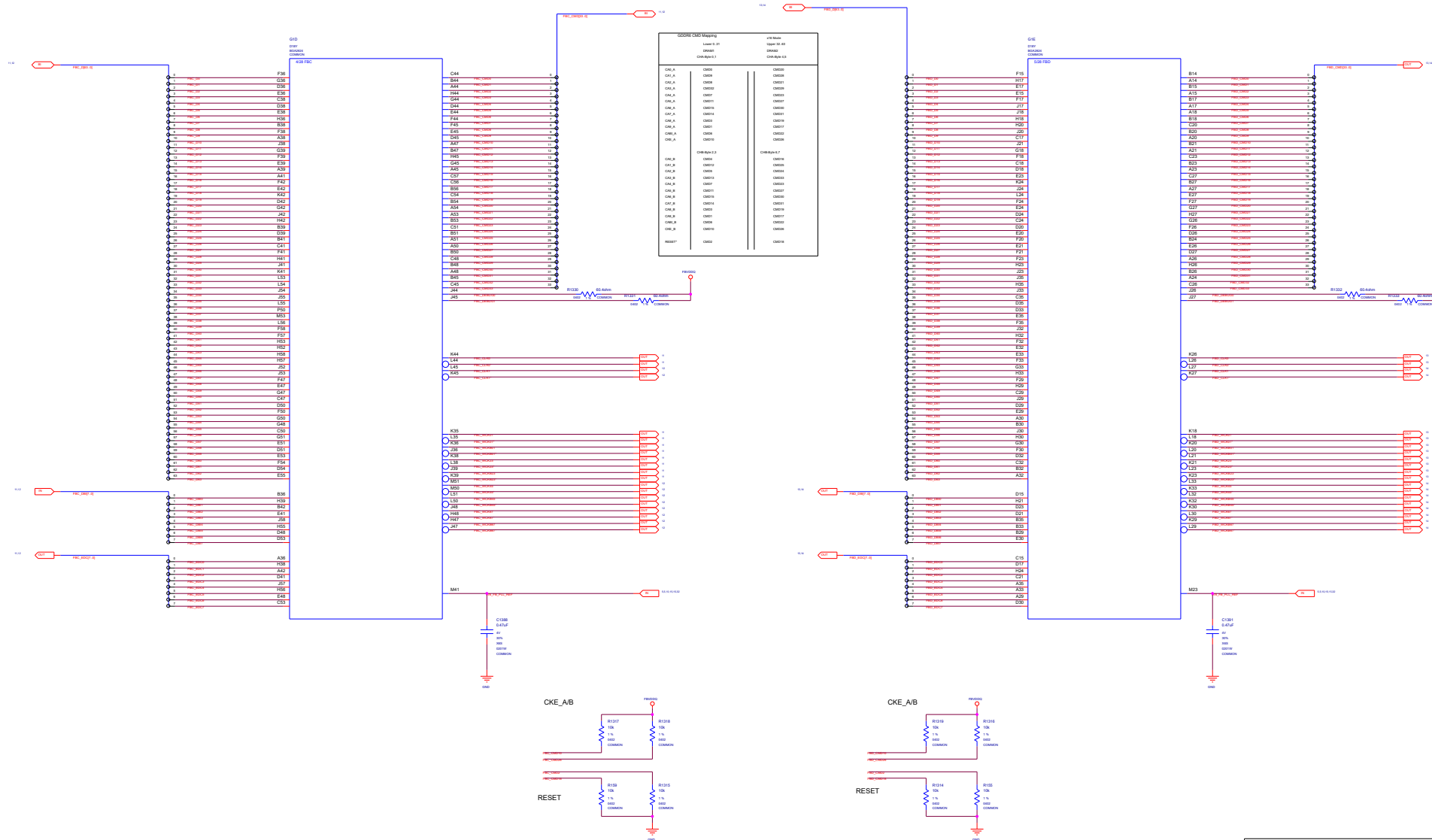
ASSEMBLY	ASSEMBLY DESCRIPTION
FRONT SIDE	MEMORY (FRONT SIDE)

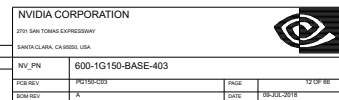


NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
NV_PN		600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	8 OF 66	
BOM REV	A	DATE	09-JUL-2018	

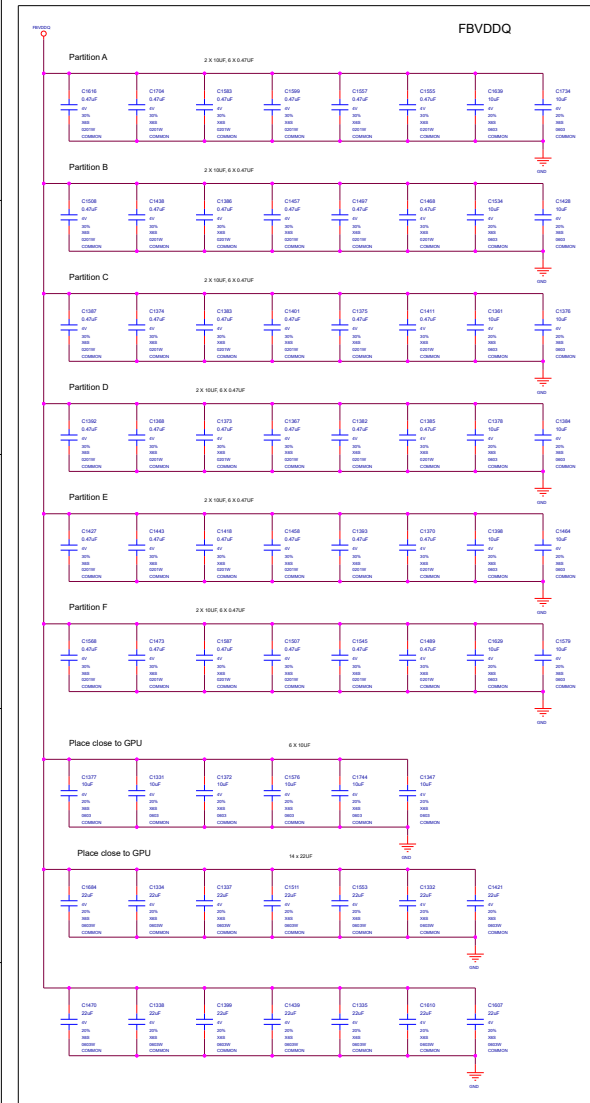




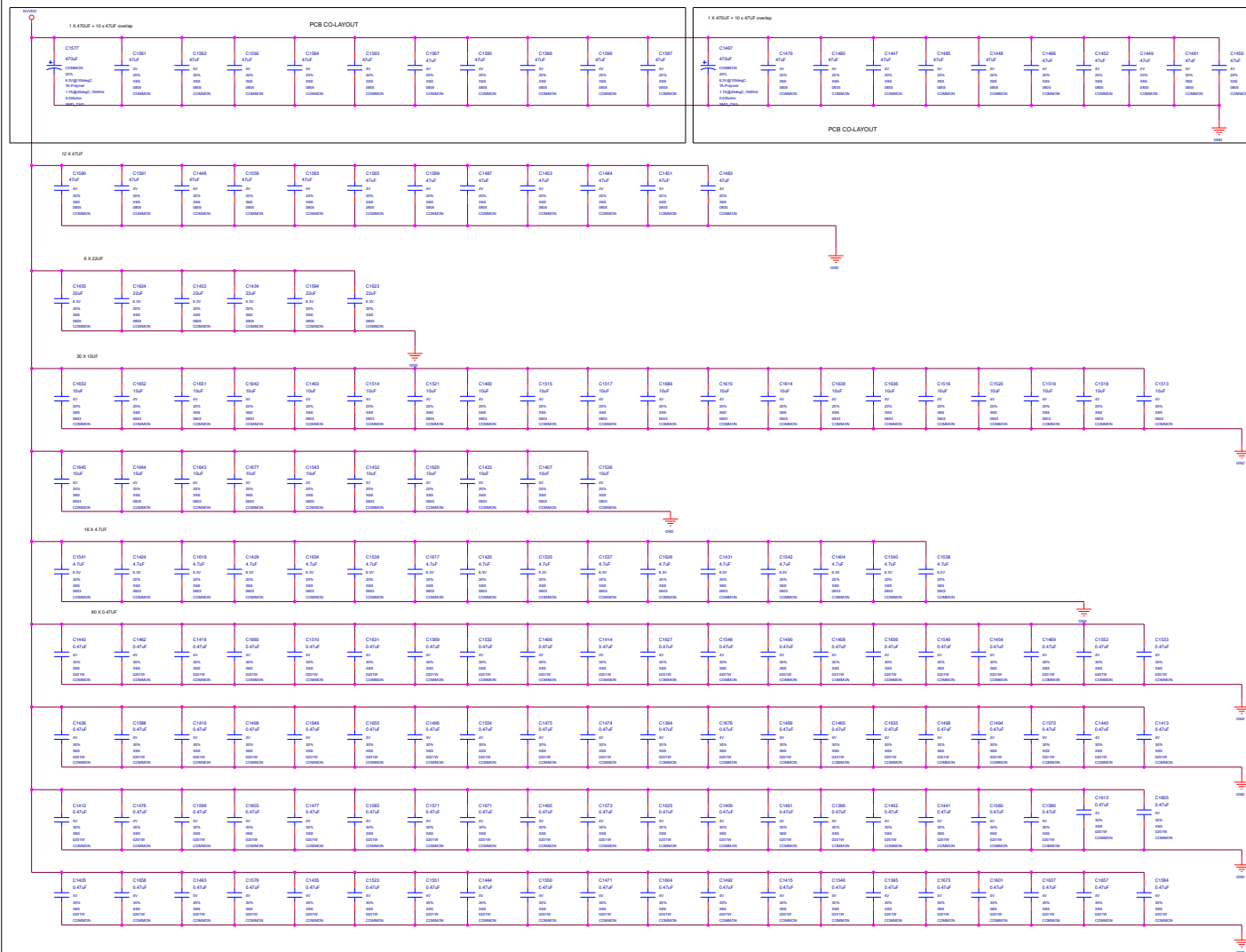




GPU Decoupling



NVDD



NVIDIA CORPORATION

©2016 NVIDIA CORPORATION

SAN JOSE, CALIFORNIA, USA

ASSEMBLY
PAGE 22 OF 24ASSEMBLY DESCRIPTION
DATE: 08-03-2016

NV_P/N 600-1G150-BASE-403

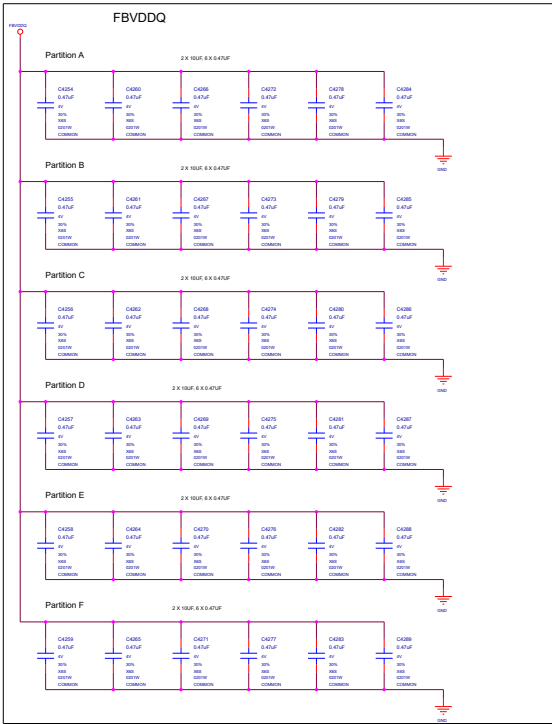
PCB REV: PCH150-003

BOX REV: A

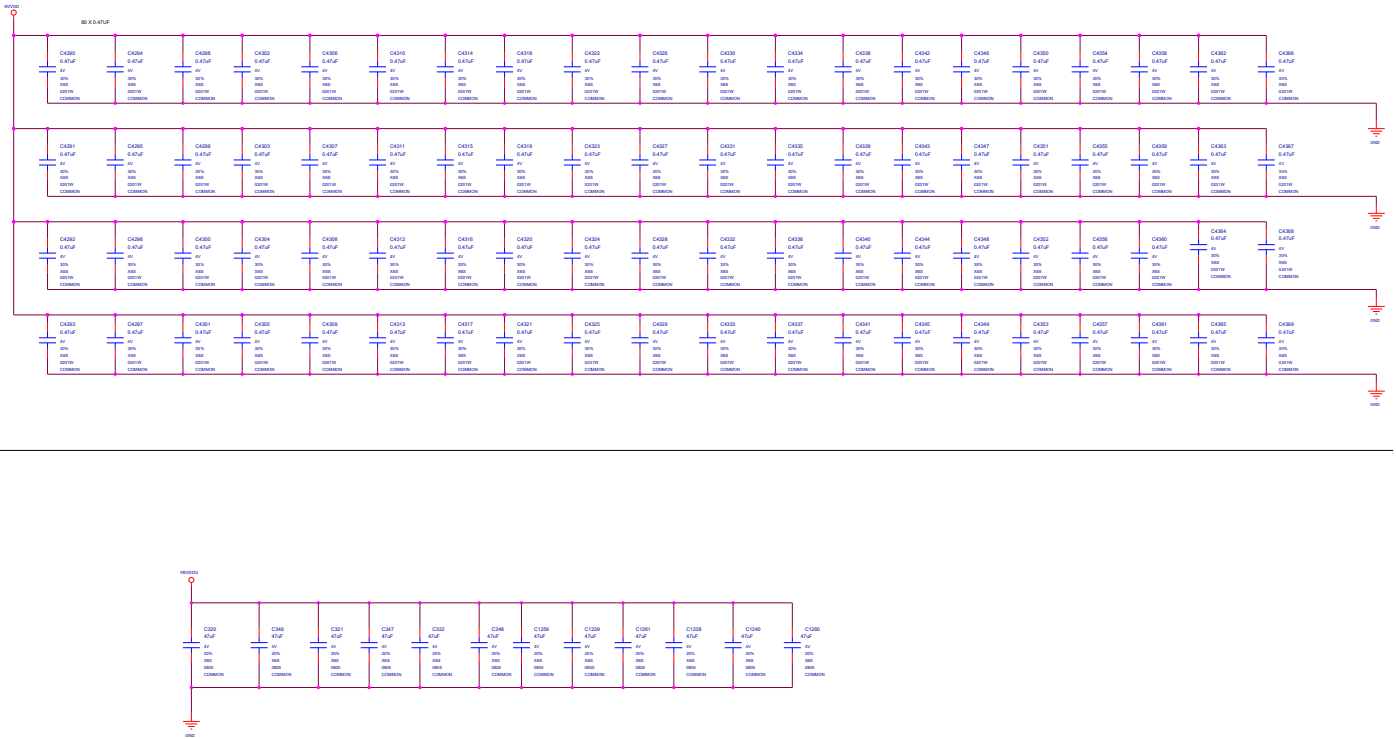
PAGE 22 OF 86

DATE: 08-03-2016

GPU Decoupling



NVDD



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	ASSEMBLY DESCRIPTION
FBVDDQ	GPU DECOUPLING F

NVIDIA CORPORATION

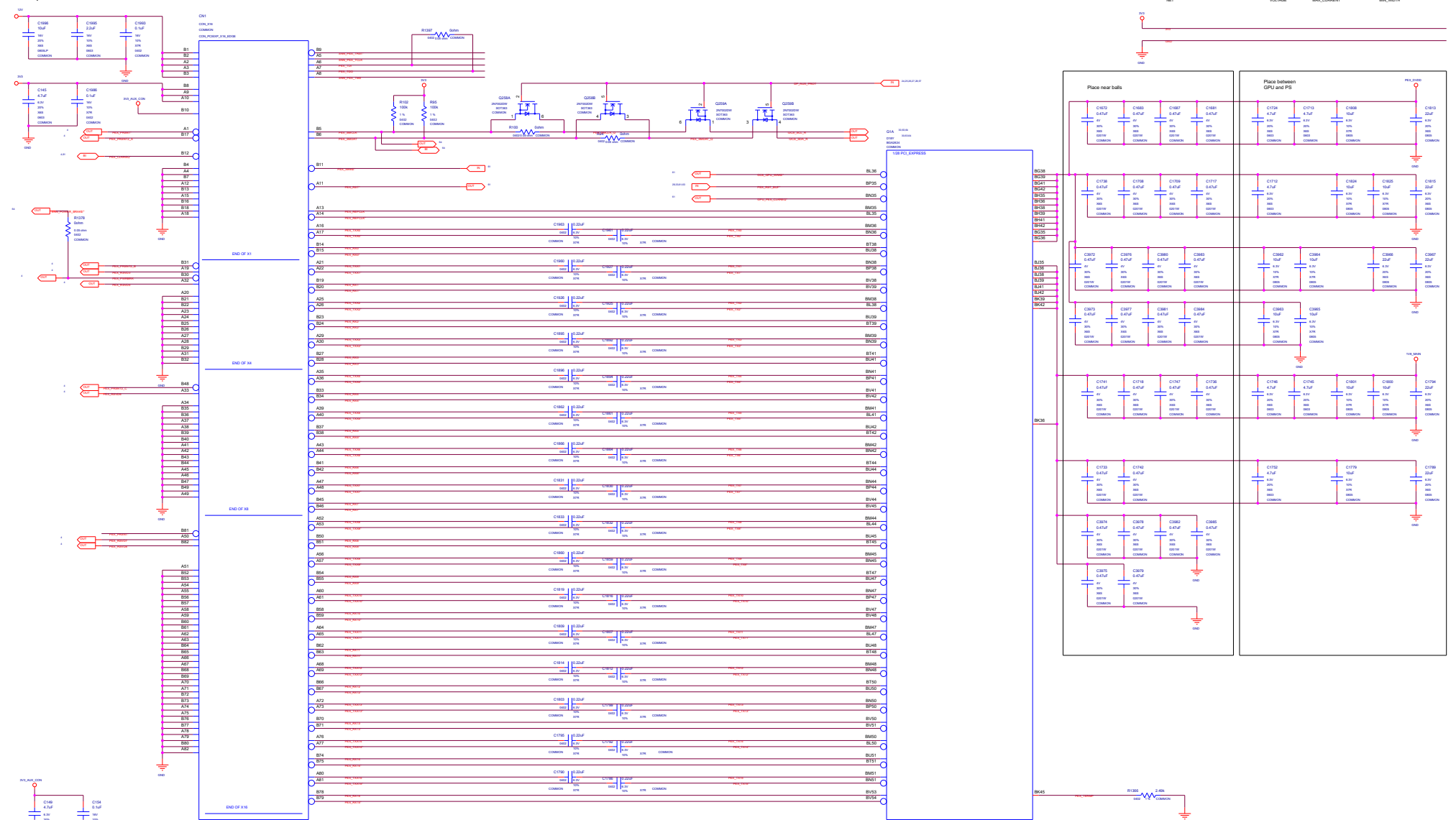
2701 SAN TOME AVE
SAN JOSE, CA 95134, USA



NV_PN 800-1G150-BASE-403

PCB REV	PC105P-023	PAGE	25 OF 86
BOARD REV	A	DATE	06-JUL-2018

PCI Express



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	ASSEMBLY DESCRIPTION
PCB LAYOUT	PCI EXPRESS

NVIDIA CORPORATION

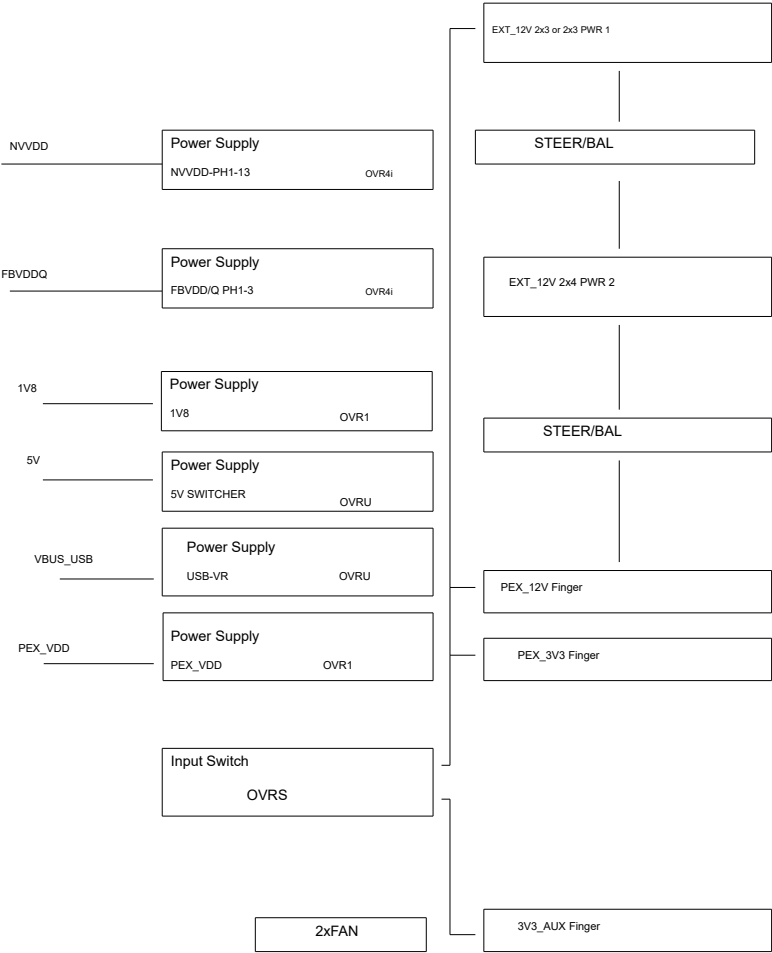
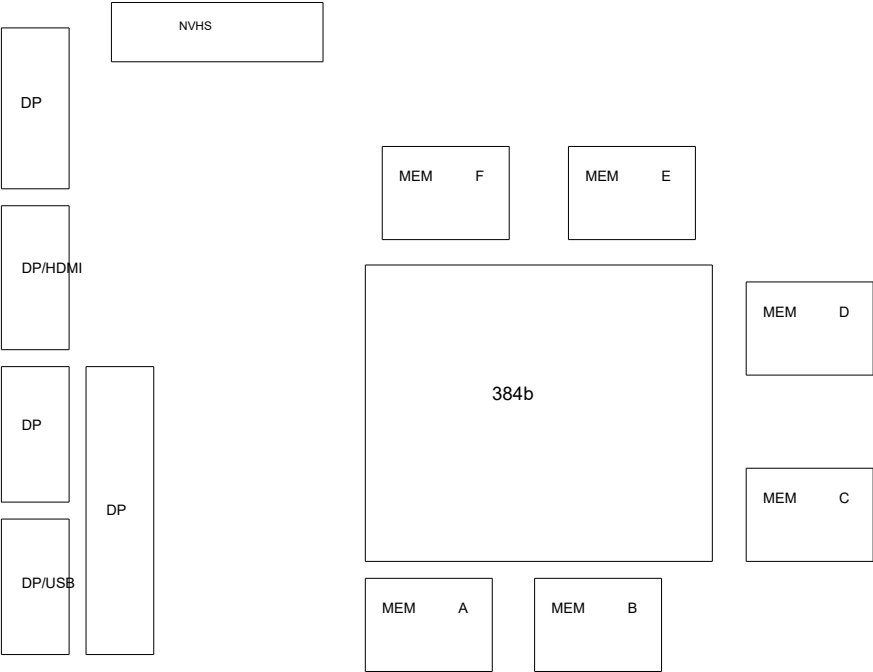
2700 SAN TOME AVE, SANTA CLARA, CA 95050, USA

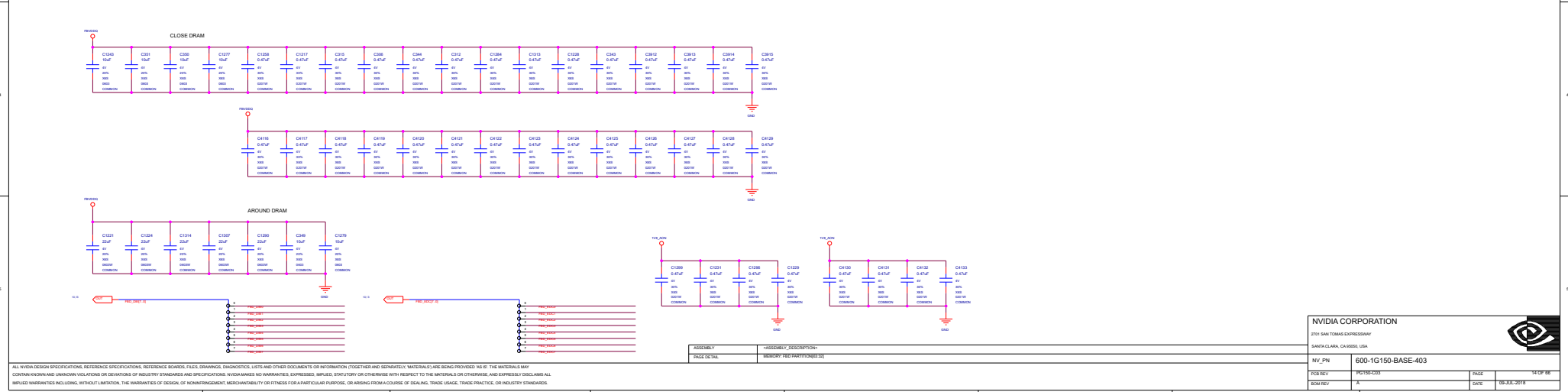
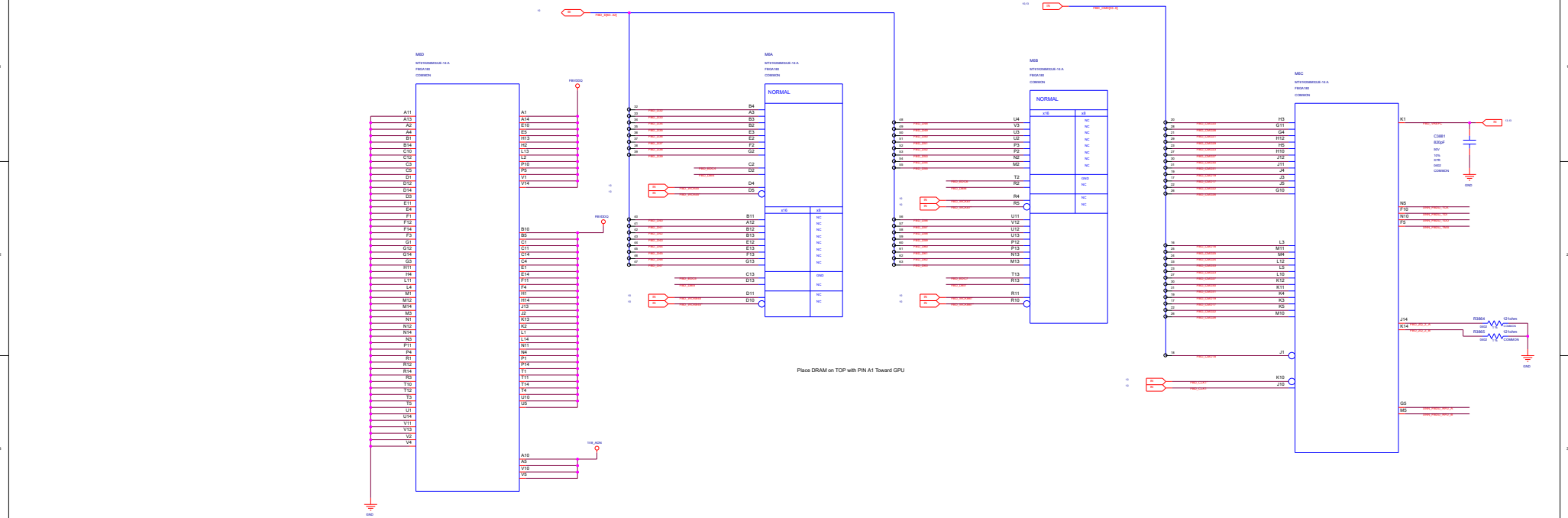


INV_FPN 600-1G150-BASE-403

PCB REV	PCB DESCRIPTION	PAGE	3 OF 86
REV 001	1	DATE	06-JUL-2018

Block Diagram





ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, EXPLICIT OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

PG150-C03

384b GDDR6 x16

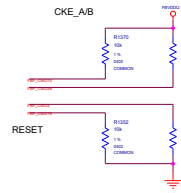
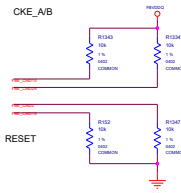
TALL DP + DP + DP + HDMI/DP + USB

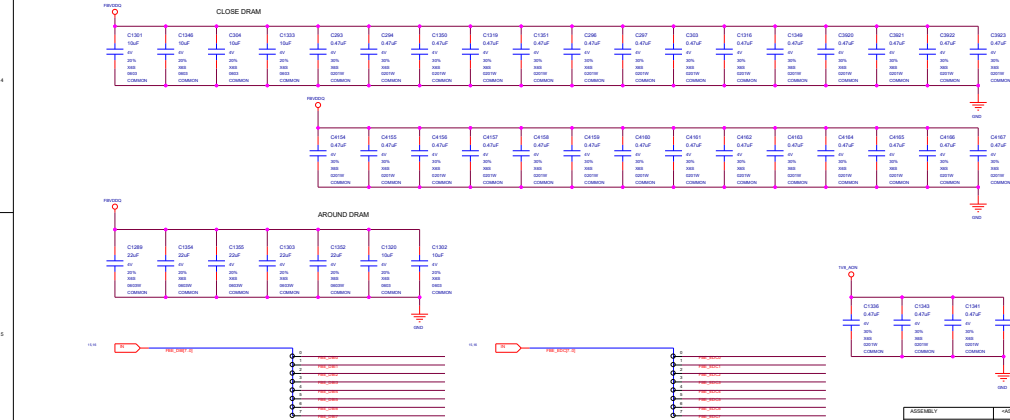
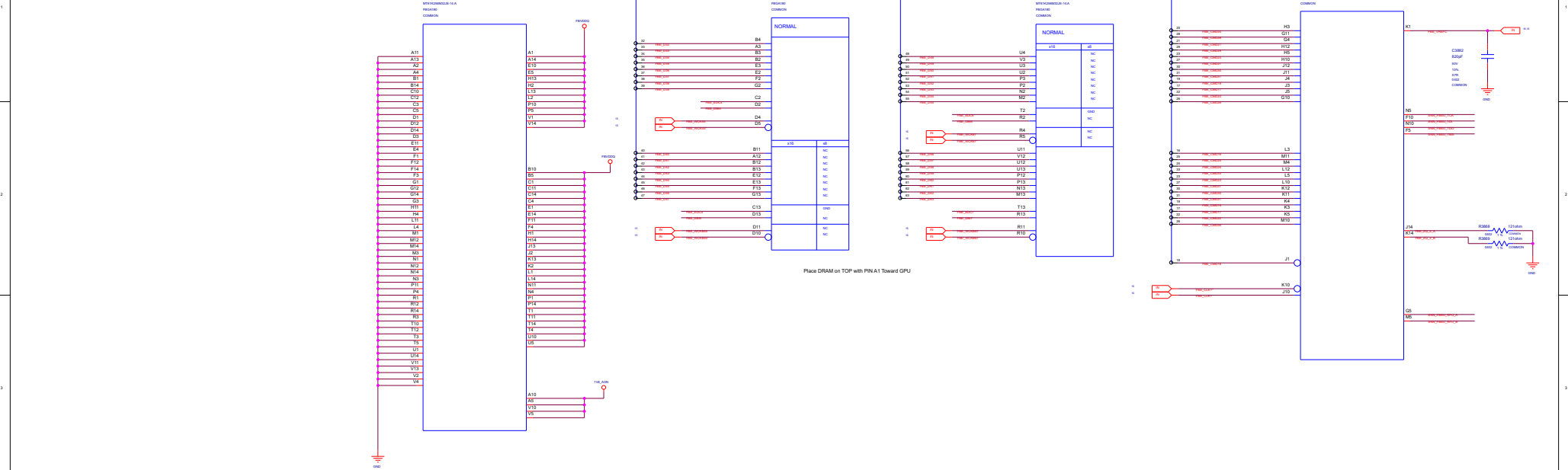
TABLE OF CONTENTS

Page	Description
1	Table of Contents
2	BLOCK DIAGRAM
3	PCI EXPRESS
4	PCI-E TERM
5	MEMORY: GPU PARTITION A/B
6	MEMORY: FBA PARTITION[31:0]
7	MEMORY: FBA PARTITION[63:32]
8	MEMORY: FBB PARTITION[31:0]
9	MEMORY: FBB PARTITION[63:32]
10	MEMORY: GPU PARTITION C/D
11	MEMORY: FBC PARTITION[31:0]
12	MEMORY: FBC PARTITION[63:32]
13	MEMORY: FBD PARTITION[31:0]
14	MEMORY: FBD PARTITION[63:32]
15	MEMORY: GPU PARTITION E/F
16	MEMORY: FBE PARTITION[31:0]
17	MEMORY: FBE PARTITION[63:32]
18	MEMORY: FBF PARTITION[31:0]
19	MEMORY: FBF PARTITION[63:32]
20	GPU PWR AND GND
21	GPU PWR, GND and NCs
22	GPU DECOUPLING
23	GPU DECOUPLING 2
24	IFPA/B DP
25	IFPE DP

Page	Description
26	IFPF USB
27	IFPC HDMI/DP
28	IFPD DP
29	NVHS X16
30	MISC: THERMAL, JTAG, GPIO, STEREO
31	MISC: ROM, STRAPS
32	MISC: XTAL, PLL
33	MISC: USB PPC
34	PS: USB_C VR
35	PS: 5V
36	PS: PEXVDD 1V8 Rail
37	PS: FBVDD Controller
38	PS: FBVDD Controller OVR3
39	PS: FBVDD Phase 1, 2
40	PS: FBVDD Phase 3
41	PS: NVVDD Controller_OVR8
42	PS: NVVDD Phase 1
43	PS: NVVDD Phase 2
44	PS: NVVDD Phase 3, 4
45	PS: NVVDD Phase 5
46	PS: NVVDD Phase 7, 8
47	PS: NVVDD Phase 9, 10
48	PS: NVVDD Phase 11, 12
49	PS: NVVDD Phase 13, 14
50	PS: INPUT SWITCH_RTD3

Page	Description
51	PS: INPUT SWITCH_RTD3 USB
52	PS: INPUT SWITCH RAIL BALANCE
53	PS: DISCRETE STEERING
54	PS: Input, filtering, and Monitoring
55	PS: Current Steering, Hot Unplug
56	PS: Prefilter
57	Sequence: 5V, 1V8, NV3V3 EN
58	Sequence: NV, PEX, FB EN
59	Sequence: PCIe Voltage Monitor
60	Sequence: Discharge
61	Sequence: MISC
62	MISC: FAN & LED1
63	MISCL: LED 2
64	MCU ZERO POWER IDLE
65	MECH
66	VR Thermal Protection





ASSEMBLY	ASSEMBLY DESCRIPTION
FRONT SIDE	MEMORY (SEE PARTITION 63)

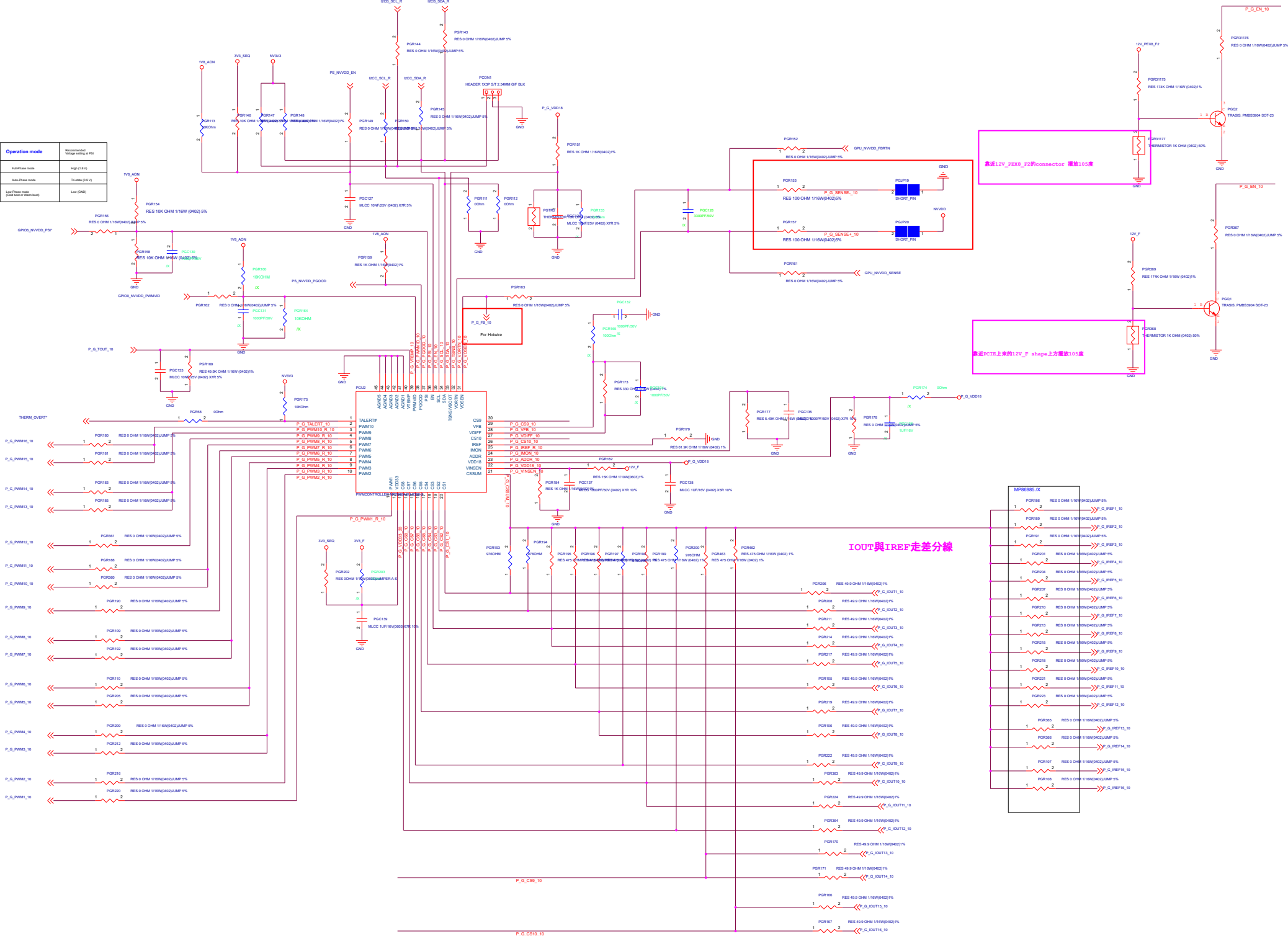
NVIDIA CORPORATION

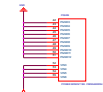
2701 SAN TOME AVE, SANTA ANA, CA 92705, USA

REV	600-1G150-BASE-403
PCB REV	PC150-003
BOX REV	1
DATE	06-JUL-2018

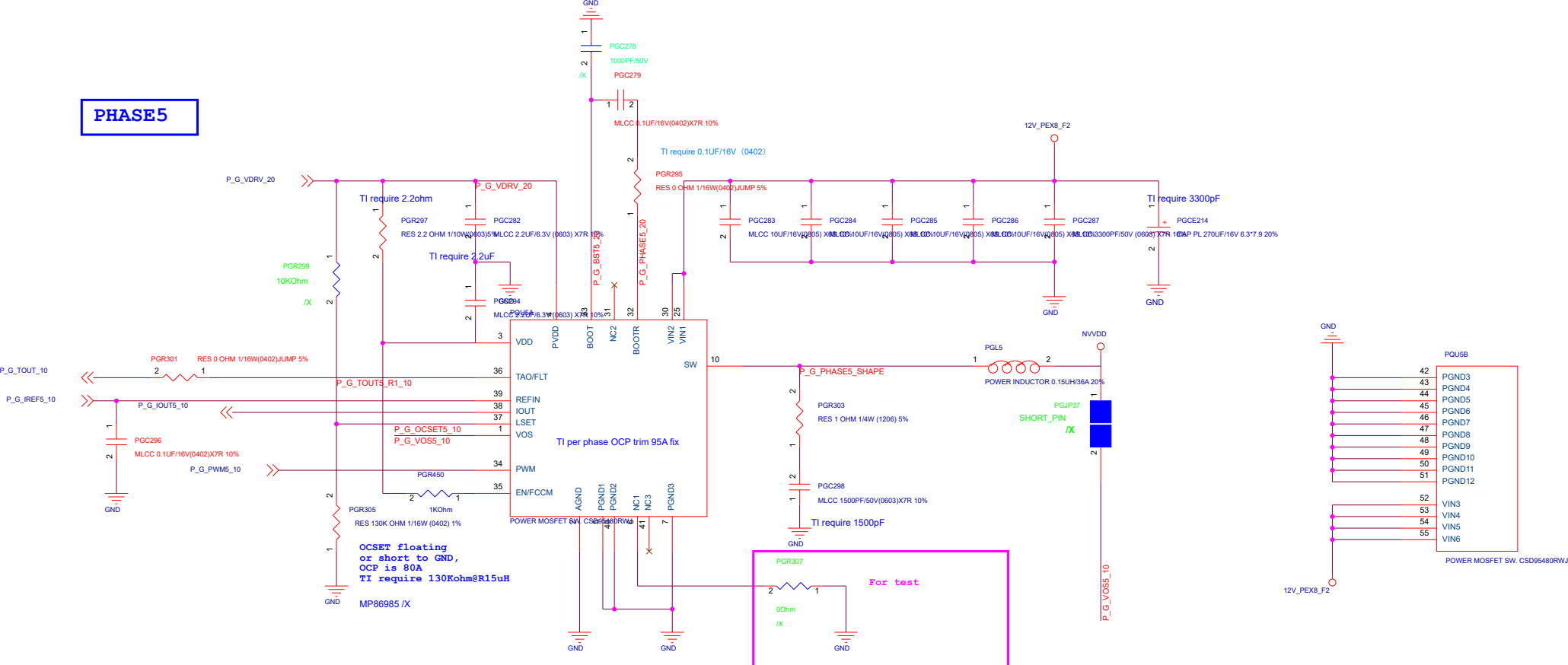
ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE. NVIDIA DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

Operation mode	Recommended storage setting at PSo
Full Phase mode	High (0.5°C)
Auto Phase mode	Trimmed (0.1°C)
Low Phase mode (Default at Sleep loss)	Low (0.0°C)

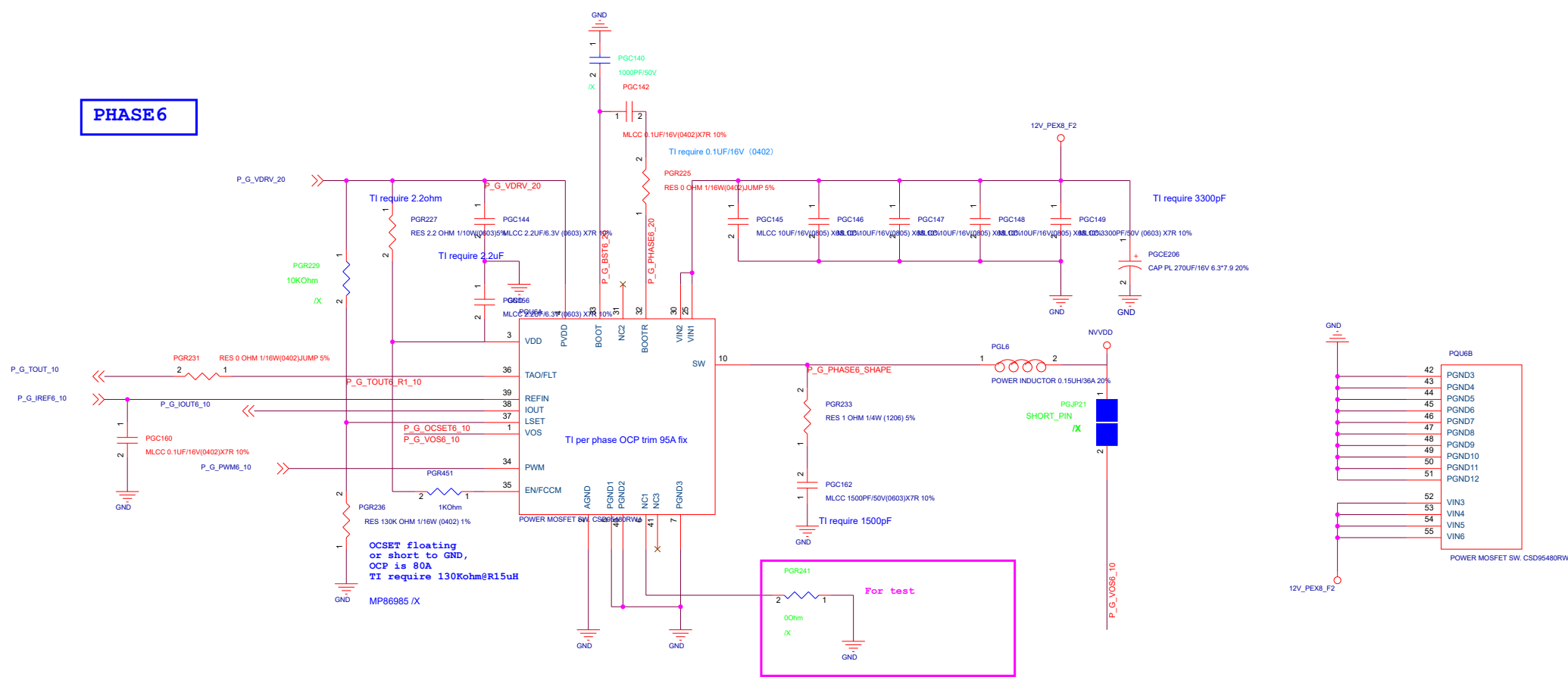




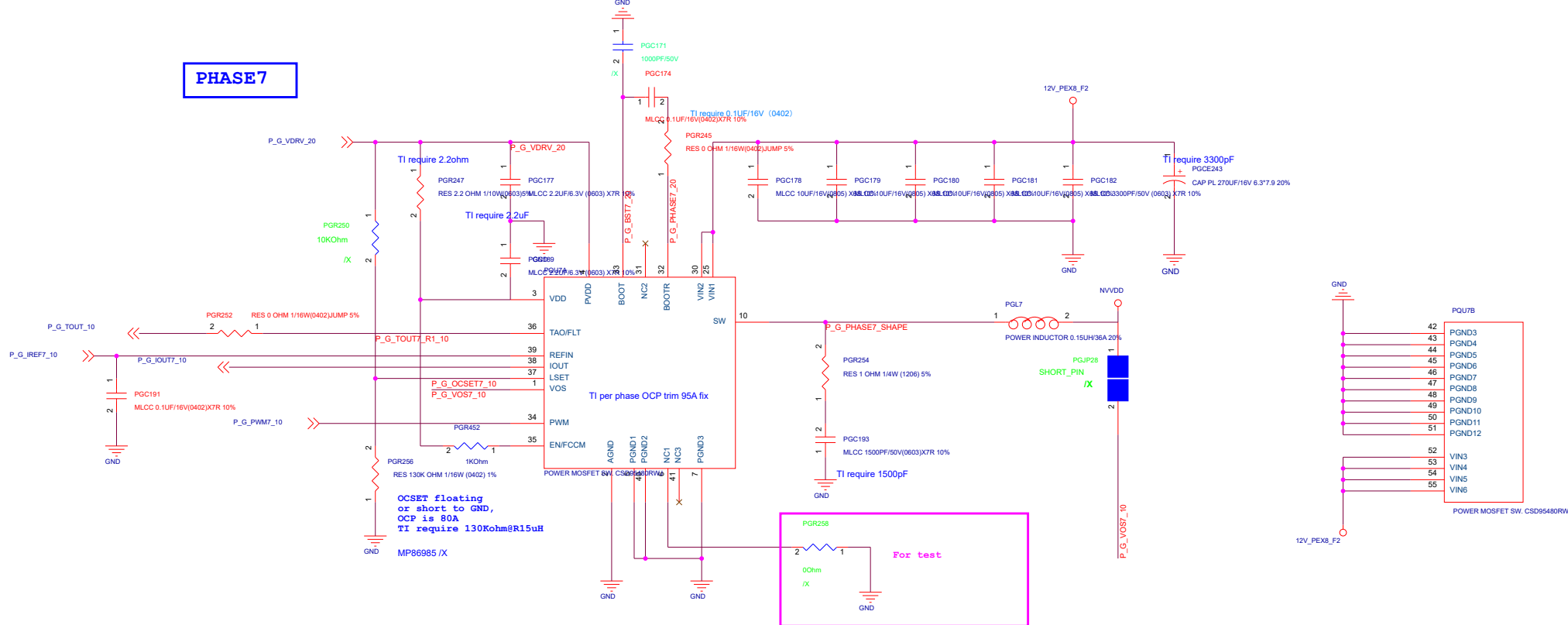
PHASE5



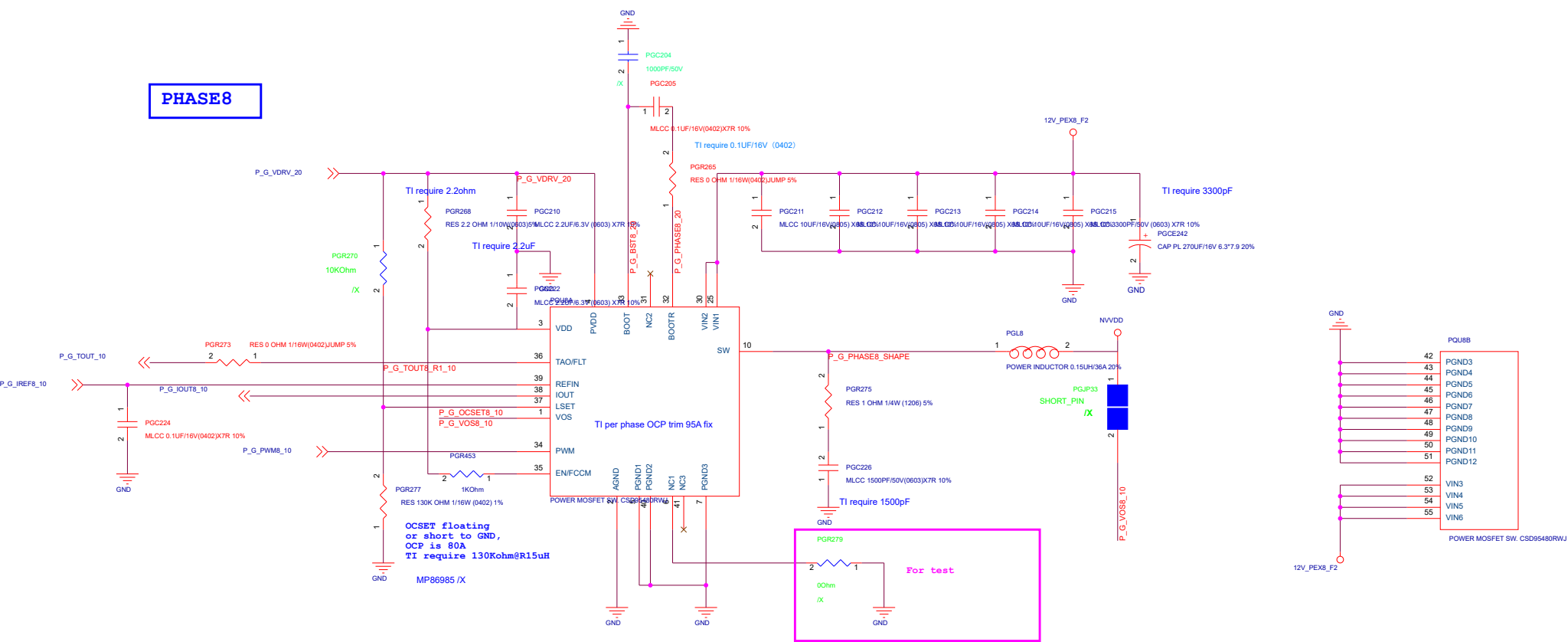
PHASE 6



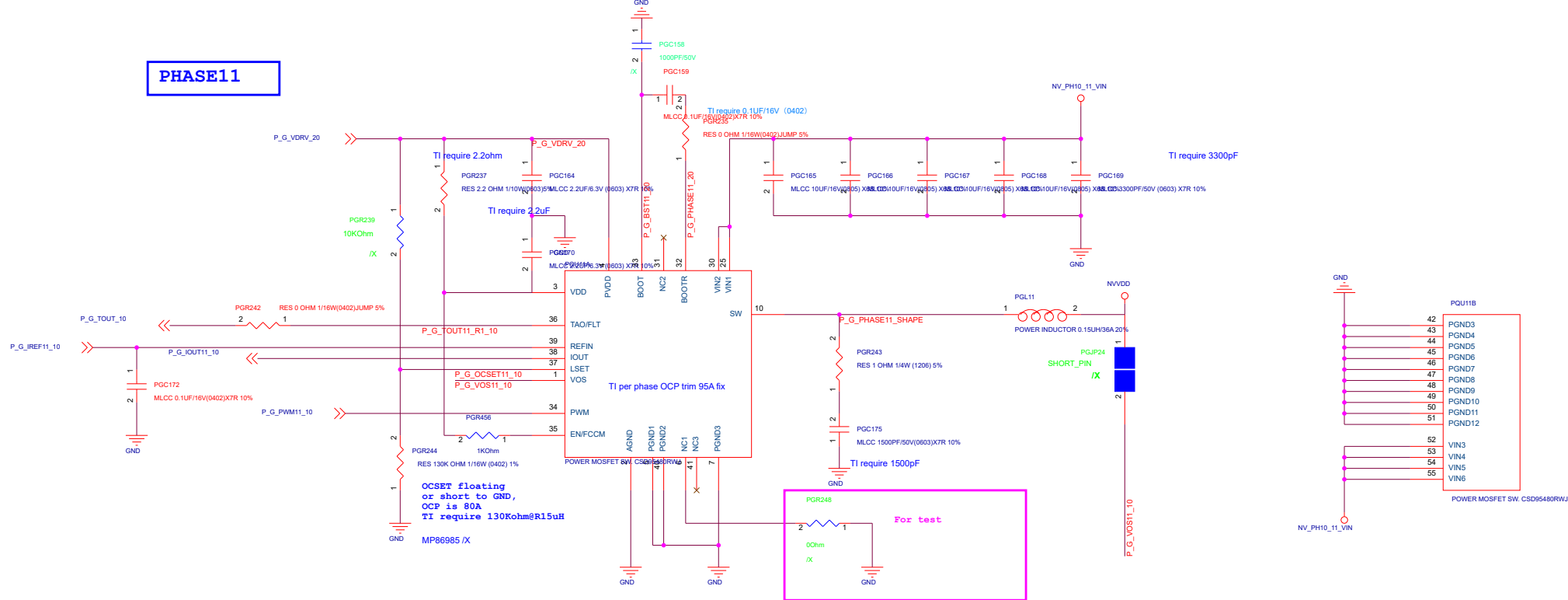
PHASE7



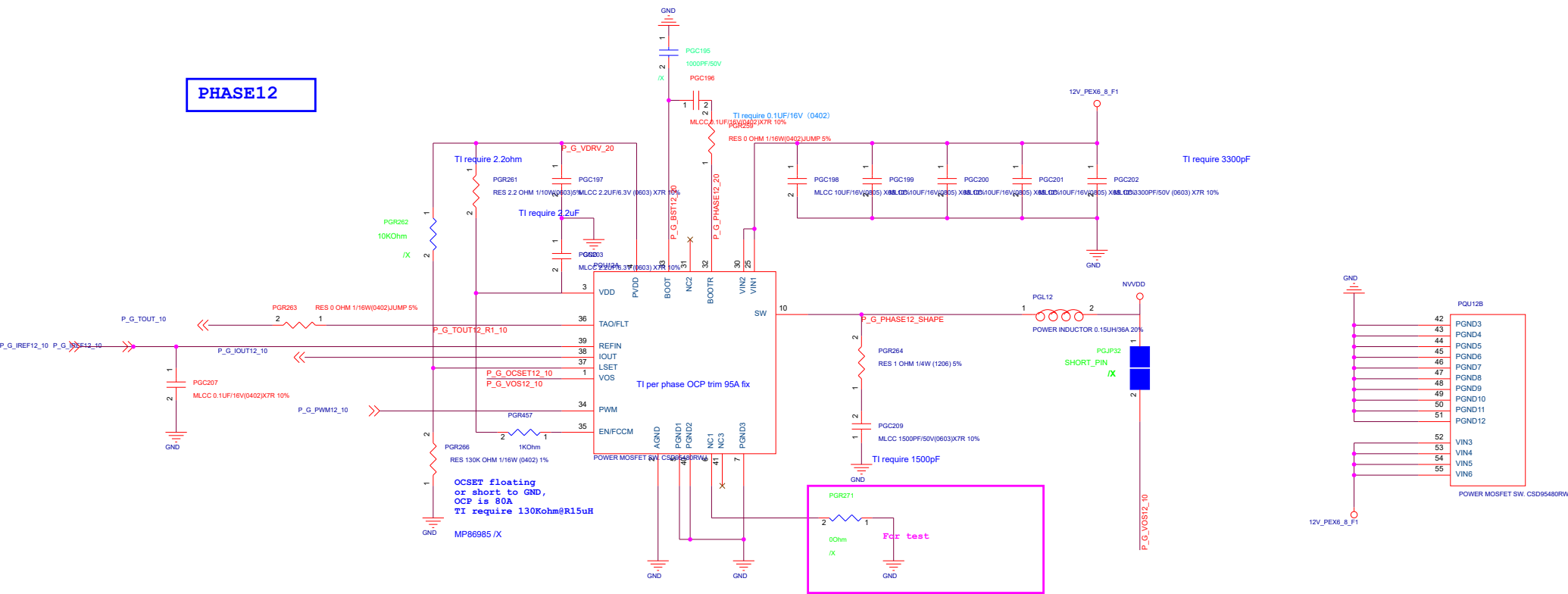
PHASE8

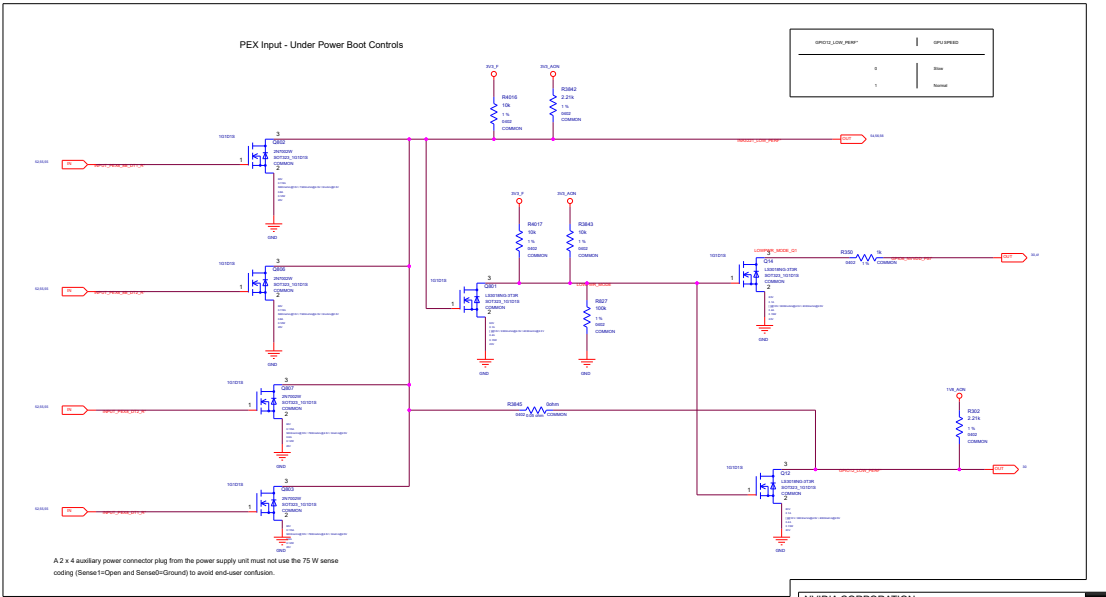
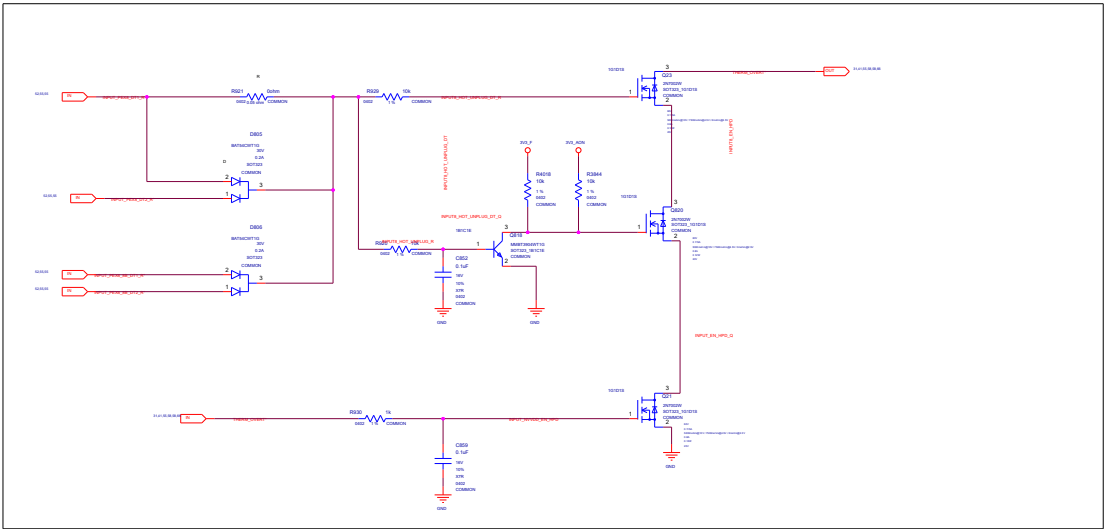
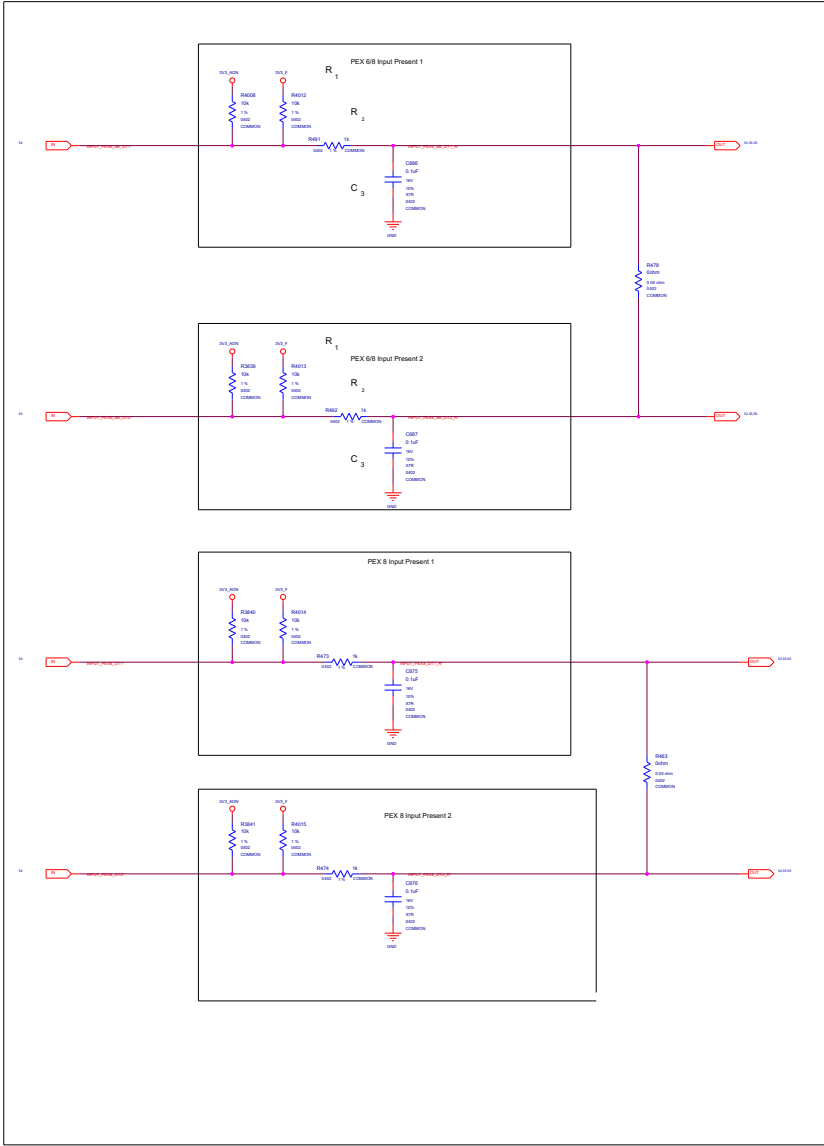


PHASE11

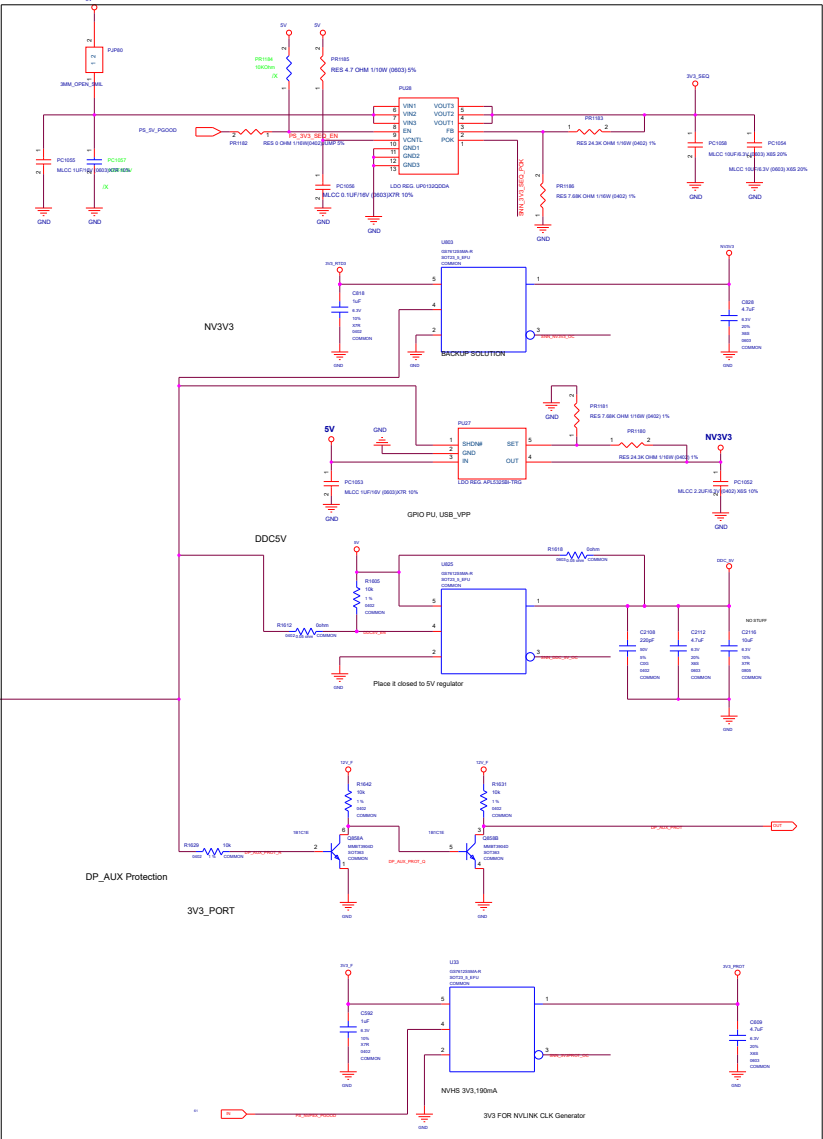
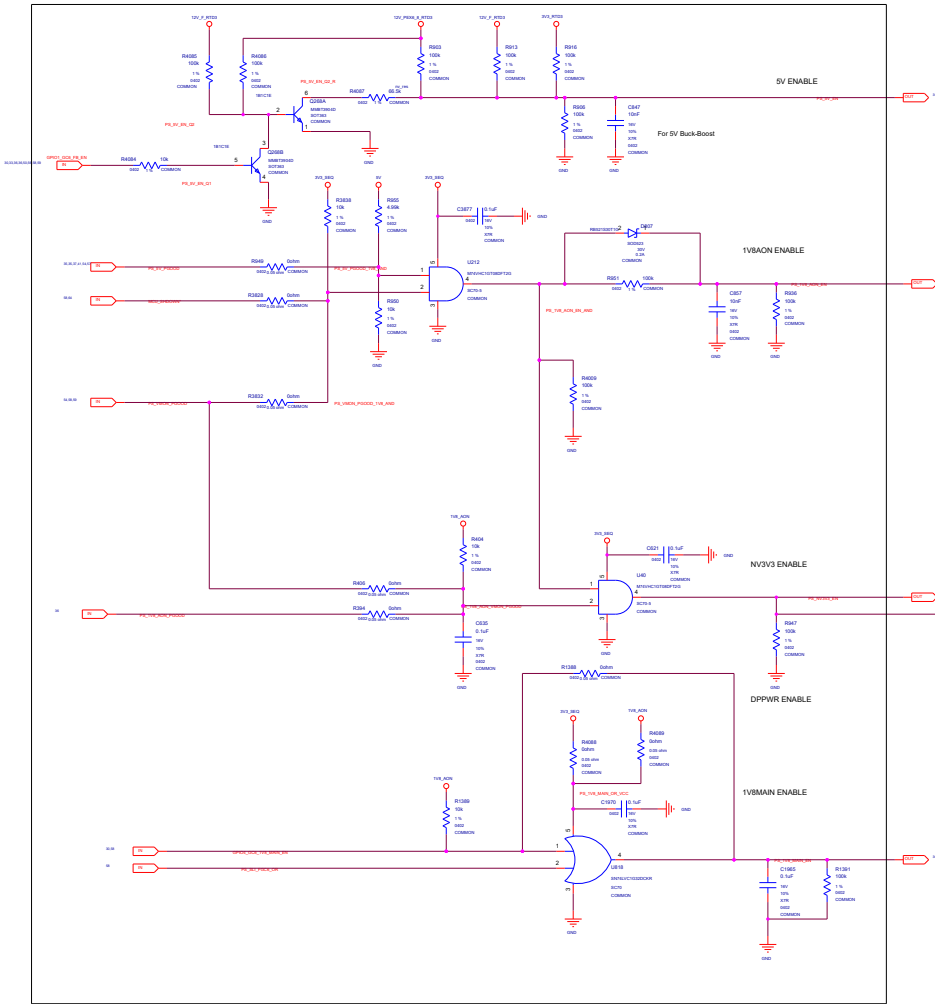


PHASE12





SEQUENCE:5V,1V8,NV3V3 ENABLE



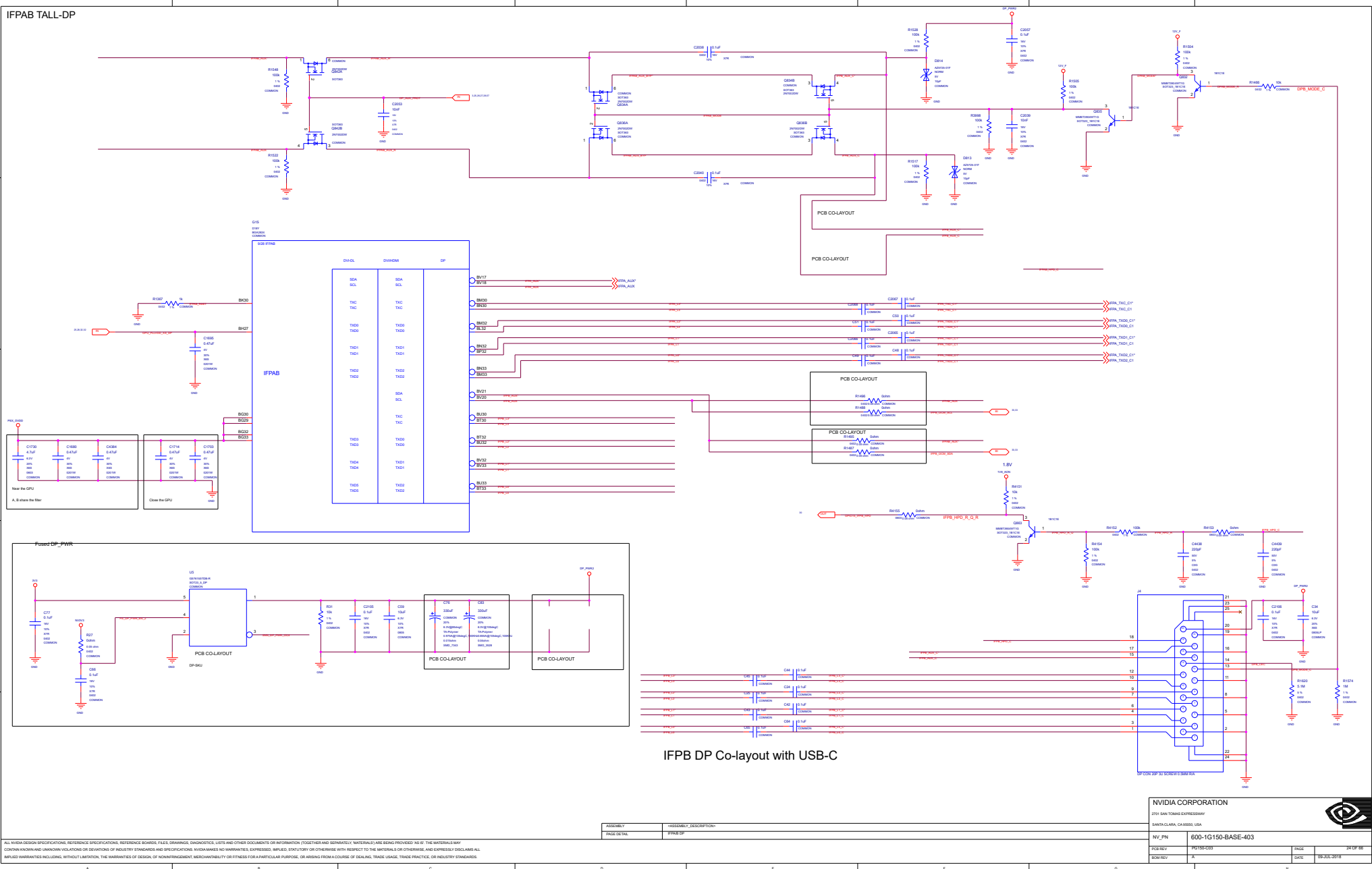
1

2

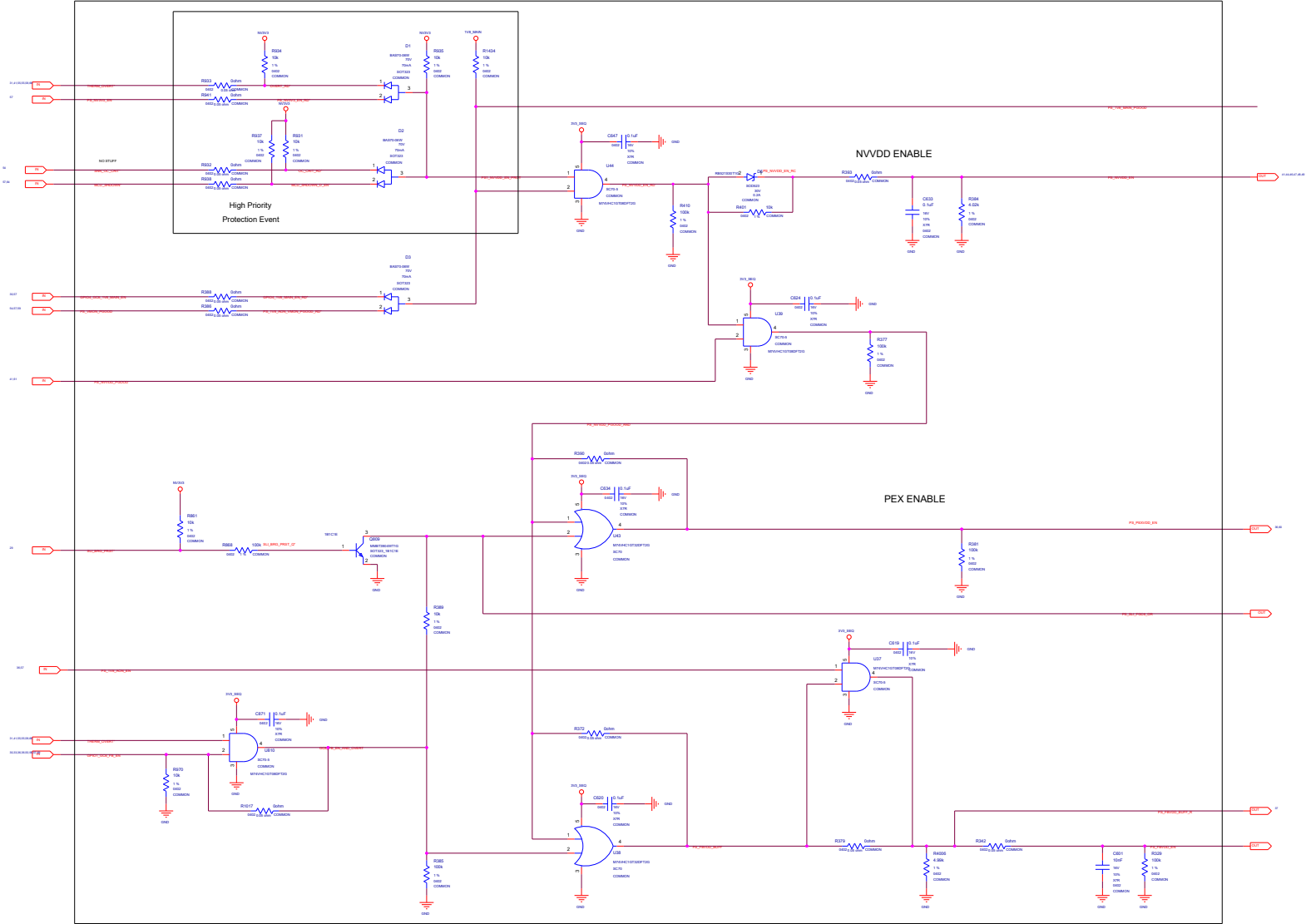
3

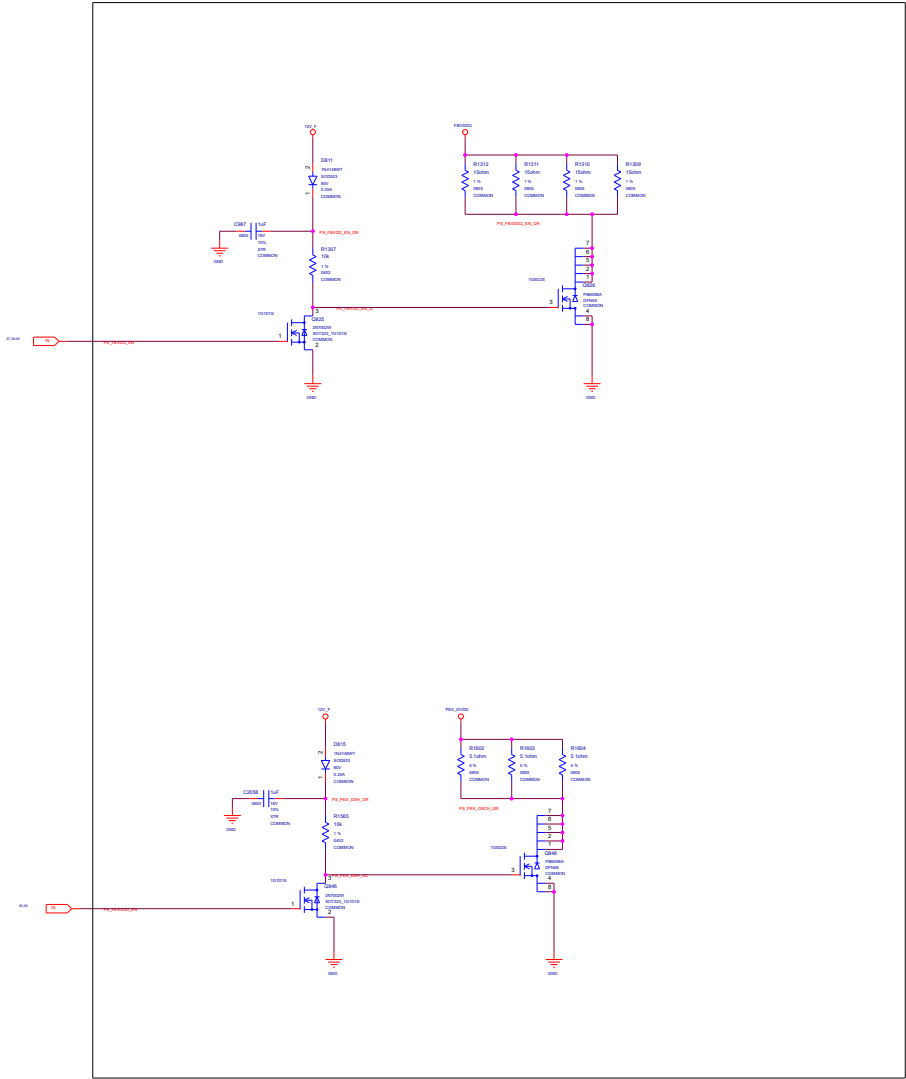
4

5

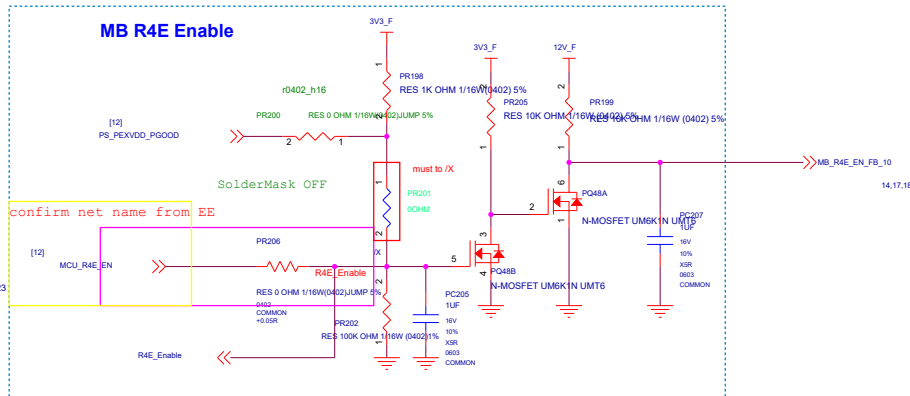
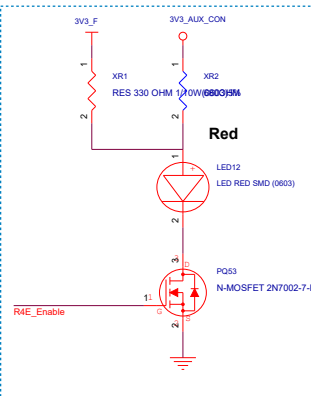


IFPAB DP Co-layout with USB-C

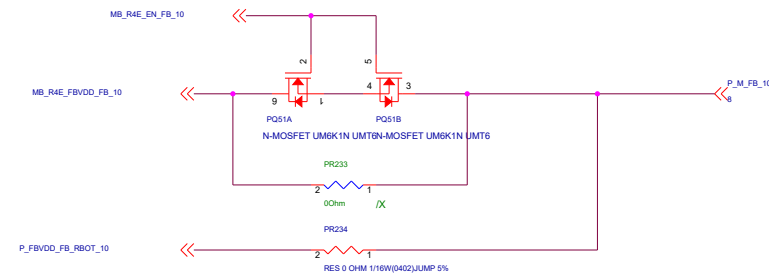
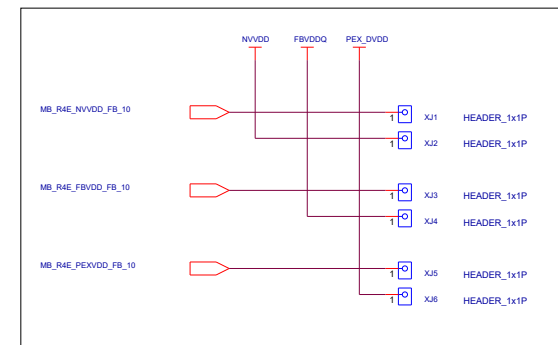




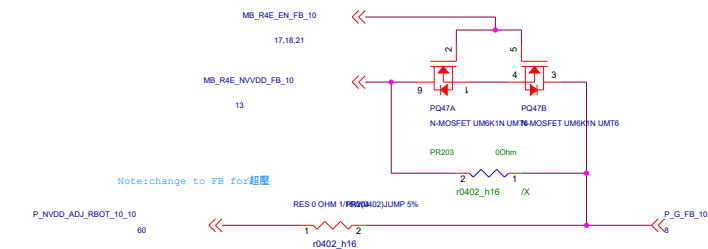
觸發信號來源需要靠整機板子最後的POWER
RAIL來決定
． 我們會先上 PEXVDD 這路的 PG 信號
． 另外預留不上 PEXVDD 這路的 PG 信號。



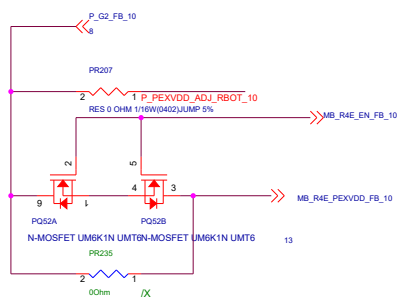
MB VGA Hotwire



For MB R4E的預留超壓電路

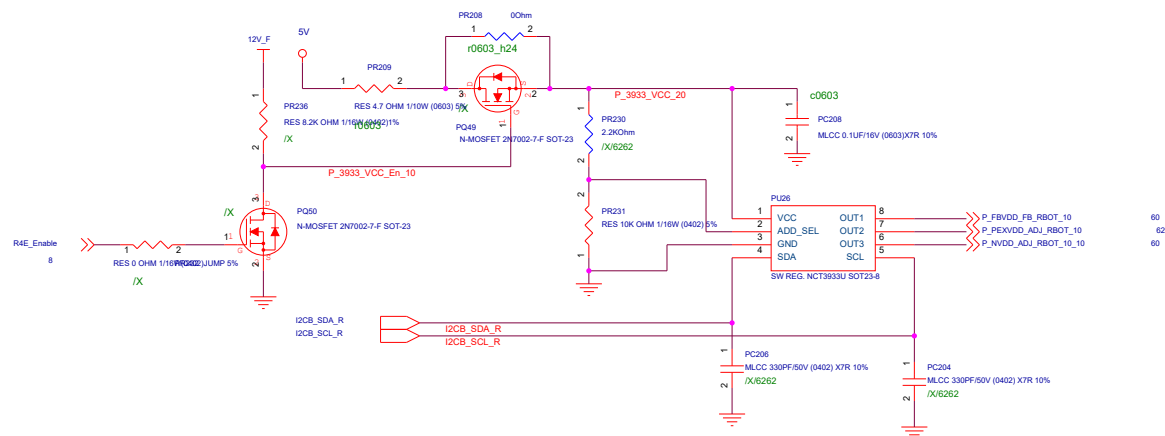


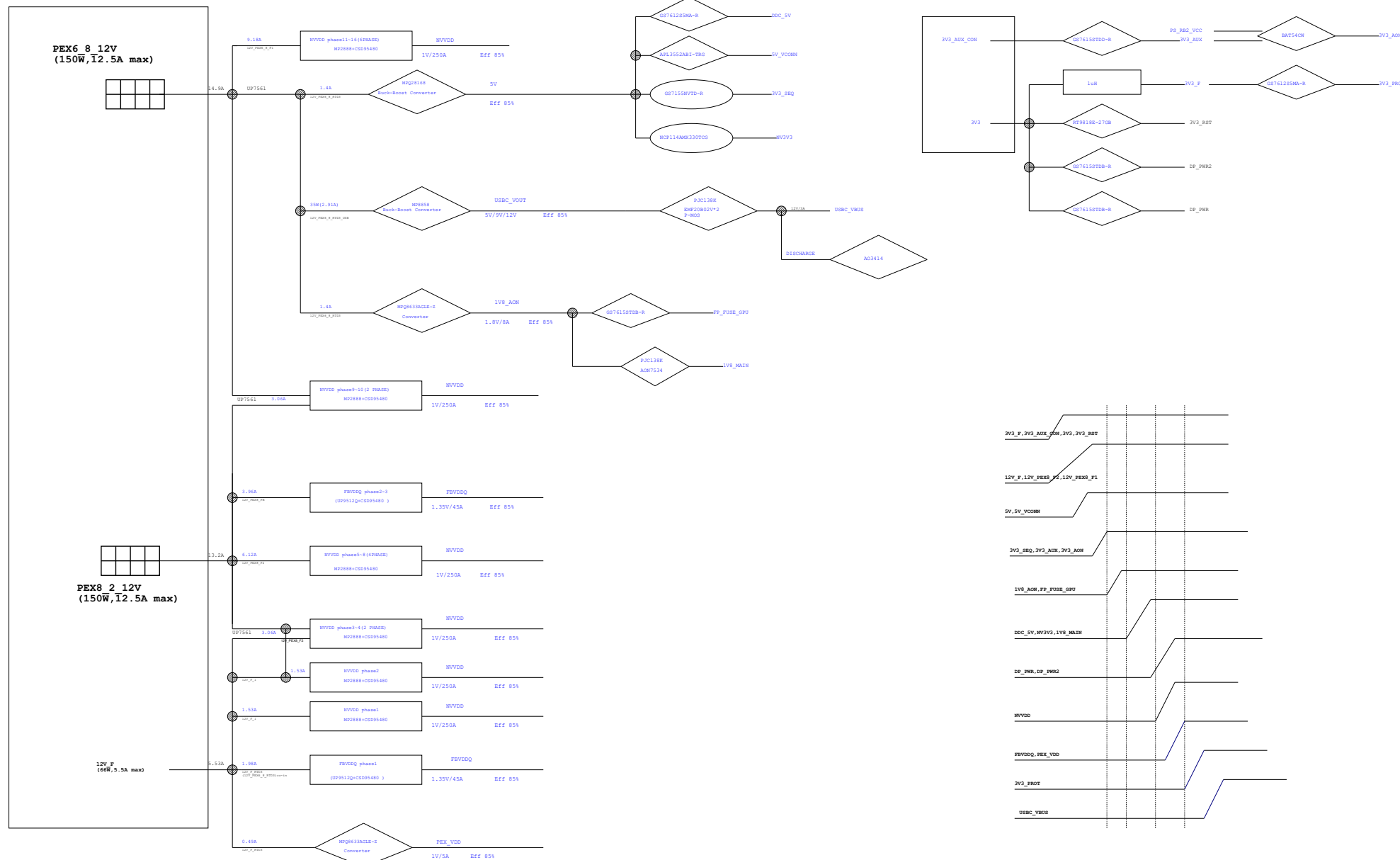
Note:change to LL for 超壓 (RESERVE)



NCT3933U Over Voltage

Address : 0x2A





ASUS VGA PCB Logo

LOG01
1
CE
/X



LOG08
1
UKRAINE
UKRAINE



LOG02
1
VCCI
/X



LOG09
1
PCB MADE IN CHINA
PCB_MADE_IN_CHINA
/X

PCB MADE IN CHINA

LOG03
1
EMI_D33005_H
EMI_D33005_H
/X



LOG10
1
MARK_L
S_MARK_L
/X



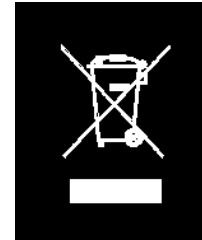
LOG04
1
FCC
FCC
/X



LOG05
1
RCM
RCM
/X



LOG011
1
WEEE_LOGO
WEEE_LOGO
/X



LOG06
1
CAN ICES-3 (B) /NMB-3 (B)
CAN_ICES_3B_NMB_3B
/X

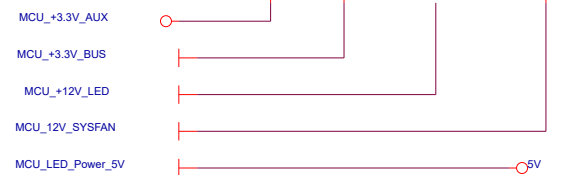
CAN ICES-3 (B) /NMB-3(B)

LOG07
1
KC_R-R-MSQ-XXXXXXXXXXXXXXX
KC_R_R_LOGO

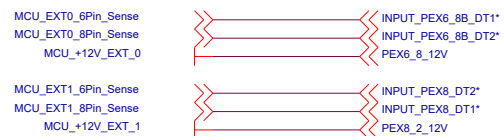


2018/06/14

Power



From PCIE 3V3_AUX (for ITE)
 From BUS 3V3 (for ITE logic判斷)
 From BUS 12V (for Cover LED/RGB Header使用, Max 2.3A)
 From 12V (for 外接式風扇使用, 任一組12V皆可)
 From 5V (for 背板LED)



From EXT 0 (外部電源第一組)

From EXT 1 (外部電源第二組)

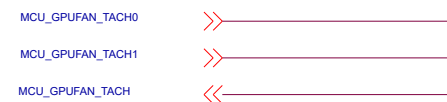
若僅有使用一組, 請拉EXT0組

I2C

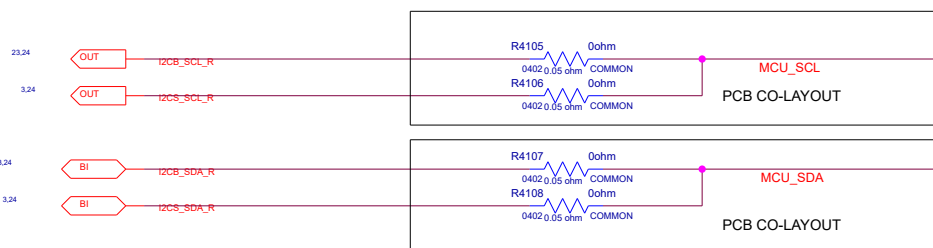
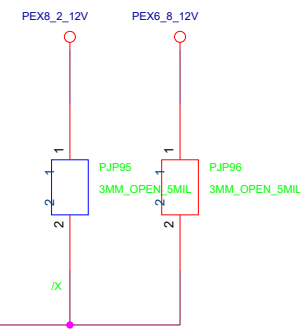


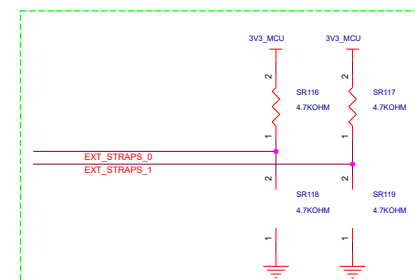
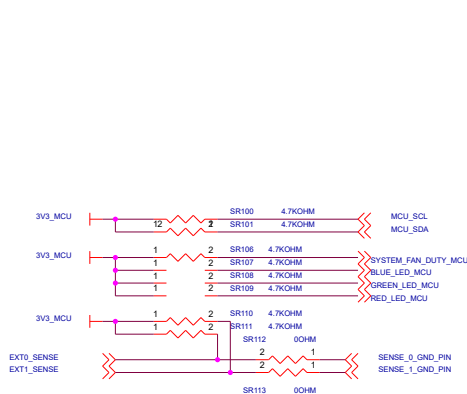
NV I2C 建議使用 I2CB_SDA & I2CB_SCL
 Layout前請再與AMD/NV EE Leader or AMD/NV AE 確認

GPUFAN

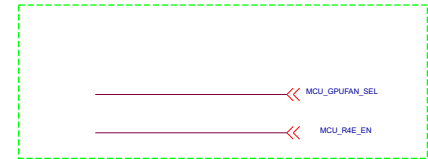
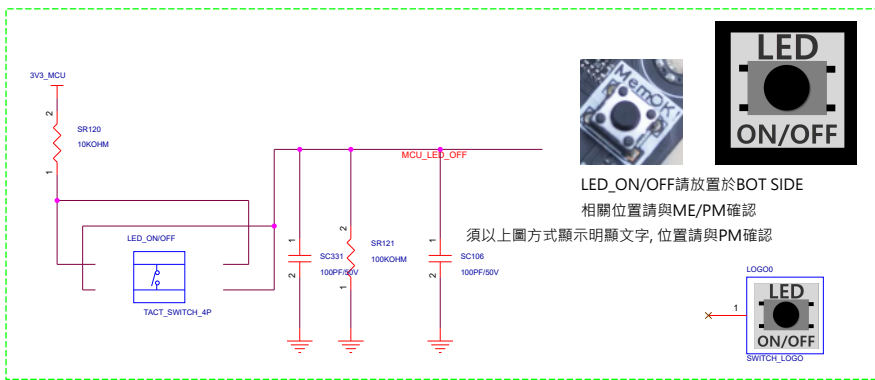
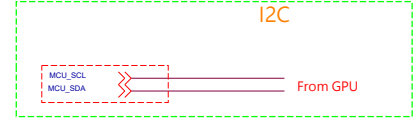
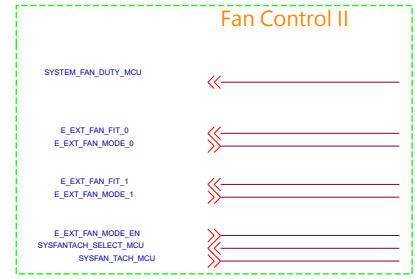
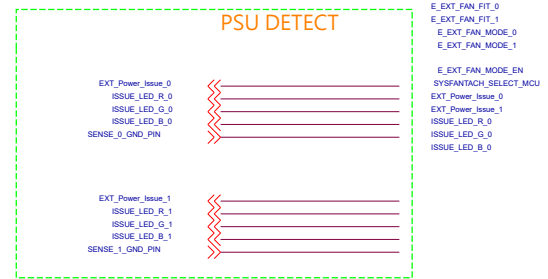
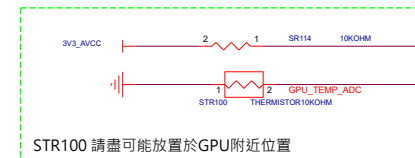


VGA HOTWIRE





11: 兩組EXT Power;
10 or 01: 一組EXT Power[EXT0];
00: 無EXT Power

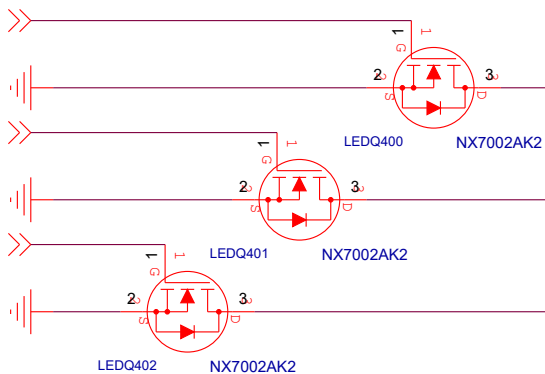


S0003 RGB LED

BLUE_LED_MCU

RED_LED_MCU

GREEN_LED_MCU



BLUE_CATHODE

RED_CATHODE

GREEN_CATHODE

LED BOARD

VF 3.2V BLUE 1206 1/4W 1% 169ohm x3pcs

VF 1.95V RED 1206 1/4W 1% 324ohm x4pcs

VF 3.2V GREEN 1206 1/4W 1% 169ohm x3pcs

MCU_+12V_LED

MCU_+12V_LED

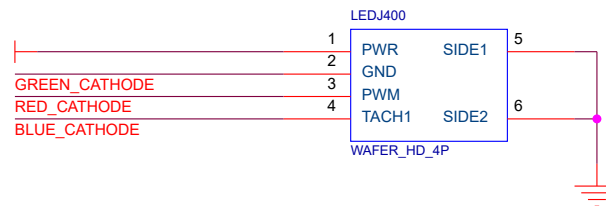
MCU_+12V_LED

Power

MCU_+12V_LED

From BUS 12V

MCU_+12V_LED





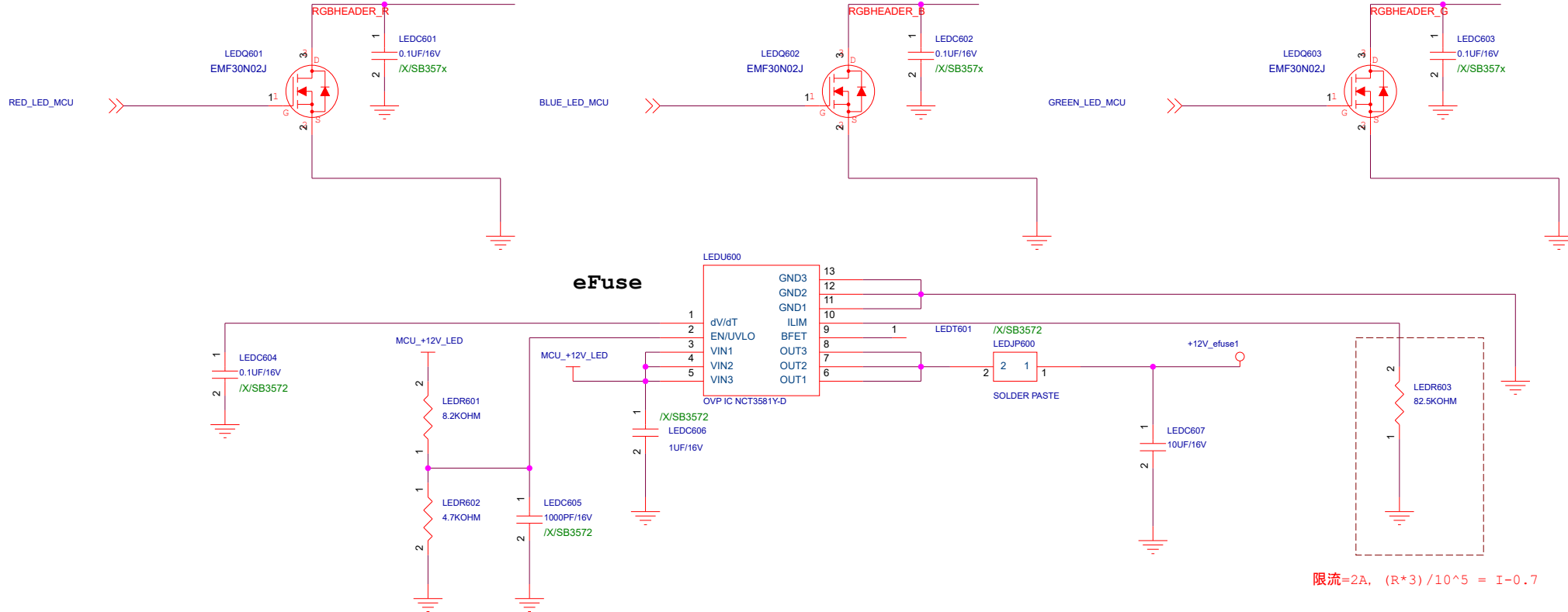
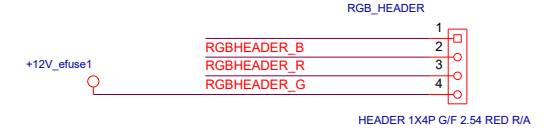


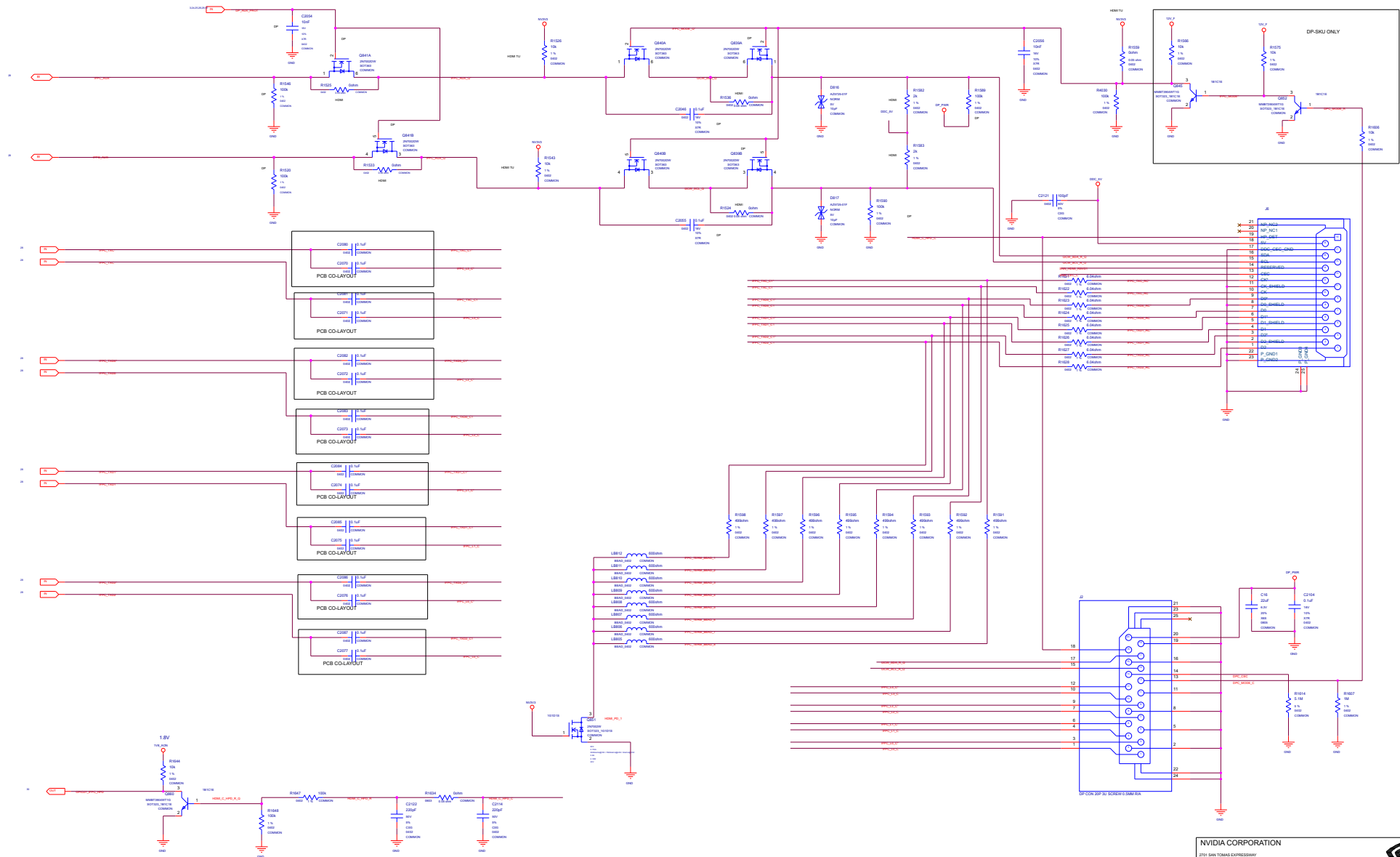
示意圖

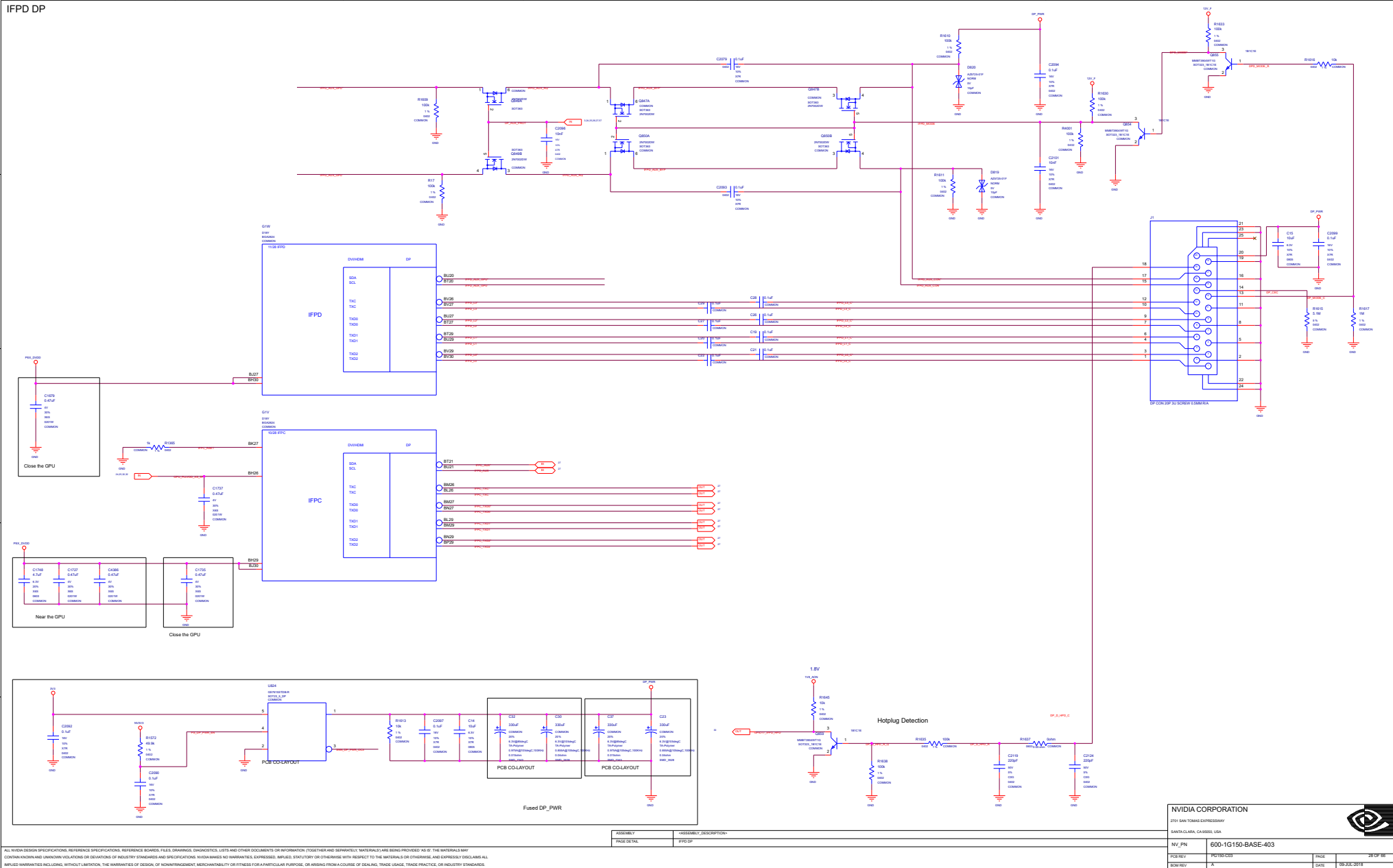


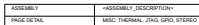
連接座旁請註明 12V G R B

RGB Header









MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	L	L	00100
H	L	H	00101
H	H	L	00110
H	H	H	00111
L	L	M	01000
L	M	L	01001

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]FS_OVERT	1=ENABLE 0=DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	H	XXXX	FS_OVERT DISABLE

DEFAULT

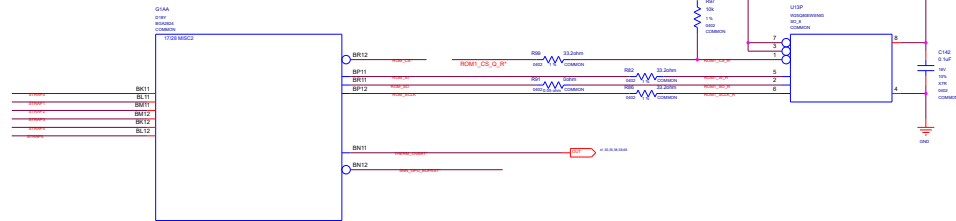
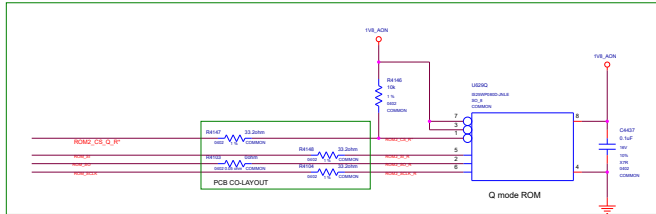
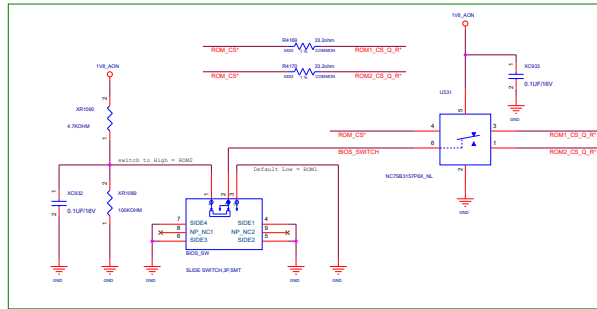
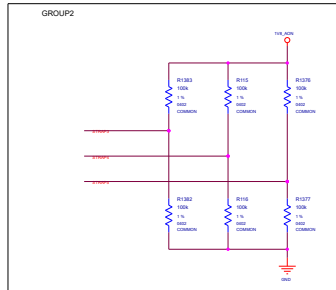
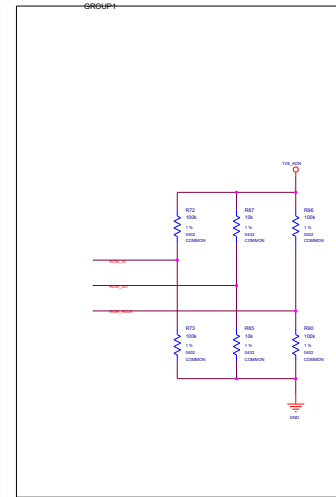
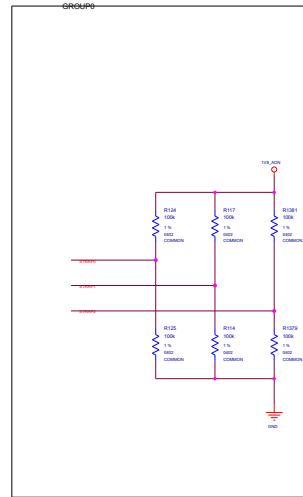
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

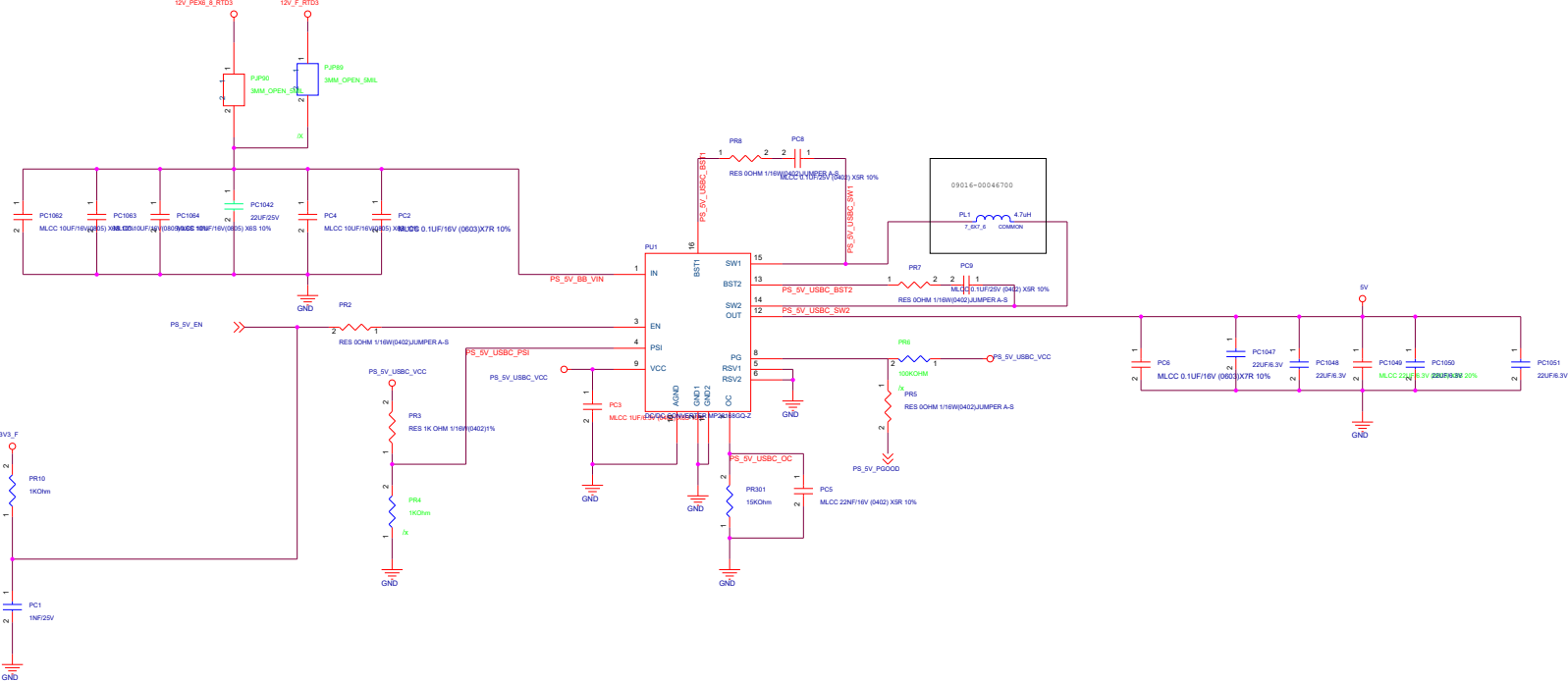
Default

SKU 200

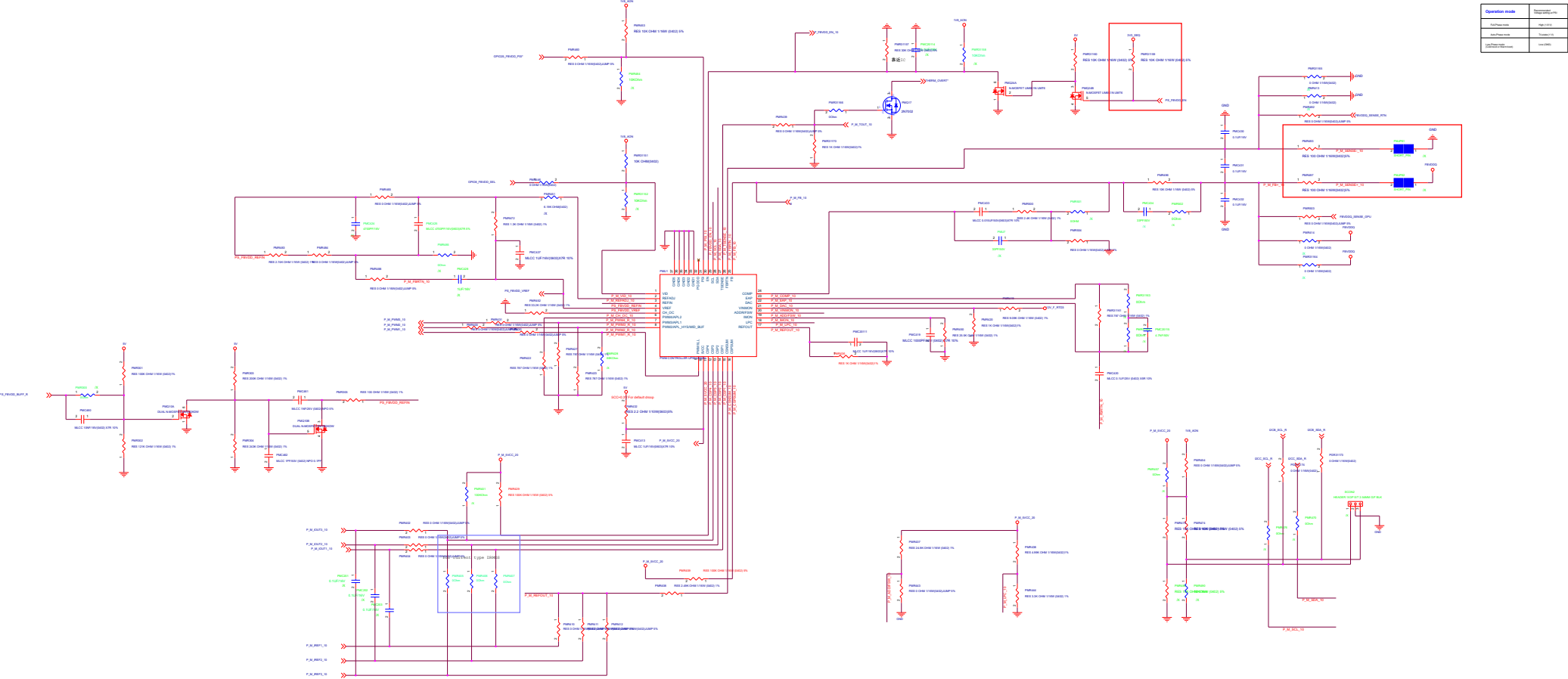
H=High :Tied to 1.8V
M=Middle Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORGNAL
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE





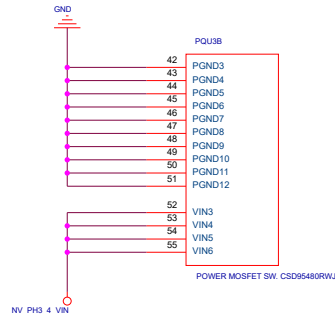
Operation mode	Temperature
Normal	25°C
High Power	75°C
Low Power	100°C



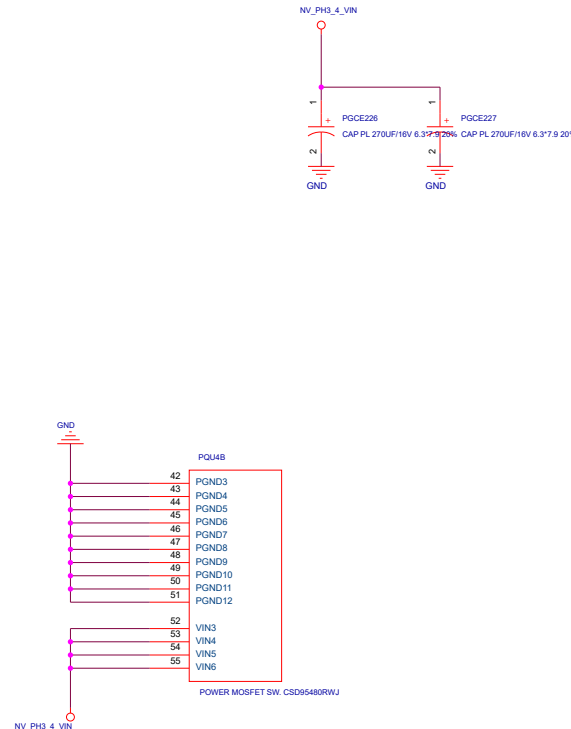
		R15 (09016-00360500) L=0.15uH DCR=0.82mohm	R30 (09016-00130800) L=0.30uH DCR=0.78mohm
RC match	Csum Rcsp	0.1uF 14.7K ohm	0.1uF 30k ohm
Total OCP (410A)	Rsum Isum	0.9K ohm 85.7uA	0.9K ohm 80uA

	Rimom	28K ohm (418A)	30K ohm (410A)
Loadline (0.3u ohm)	RLL	1.47K ohm	1.54K ohm
Loadline En threshold (101A Rn, 50A Dlx)	Rtop Rbot	124K ohm 38.3K ohm	124K ohm 39K ohm

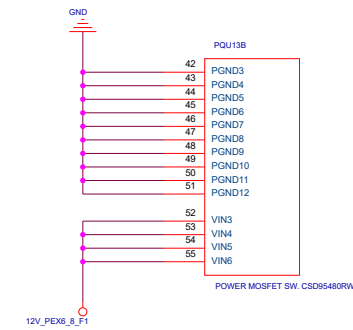
PHASE3



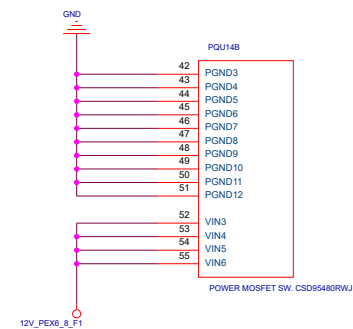
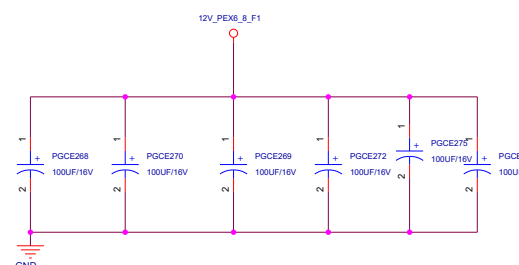
PHASE4



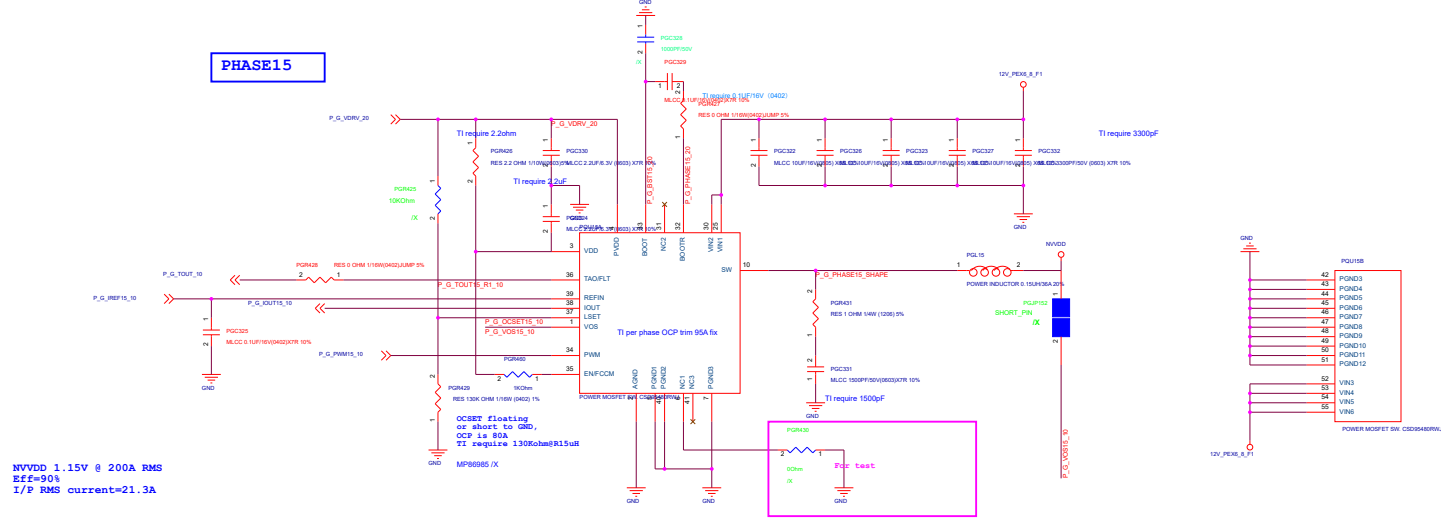
PHASE13



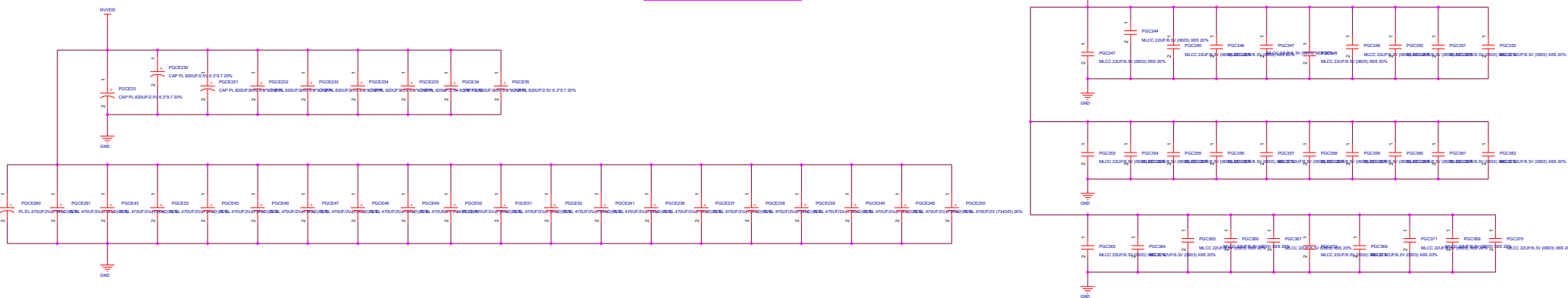
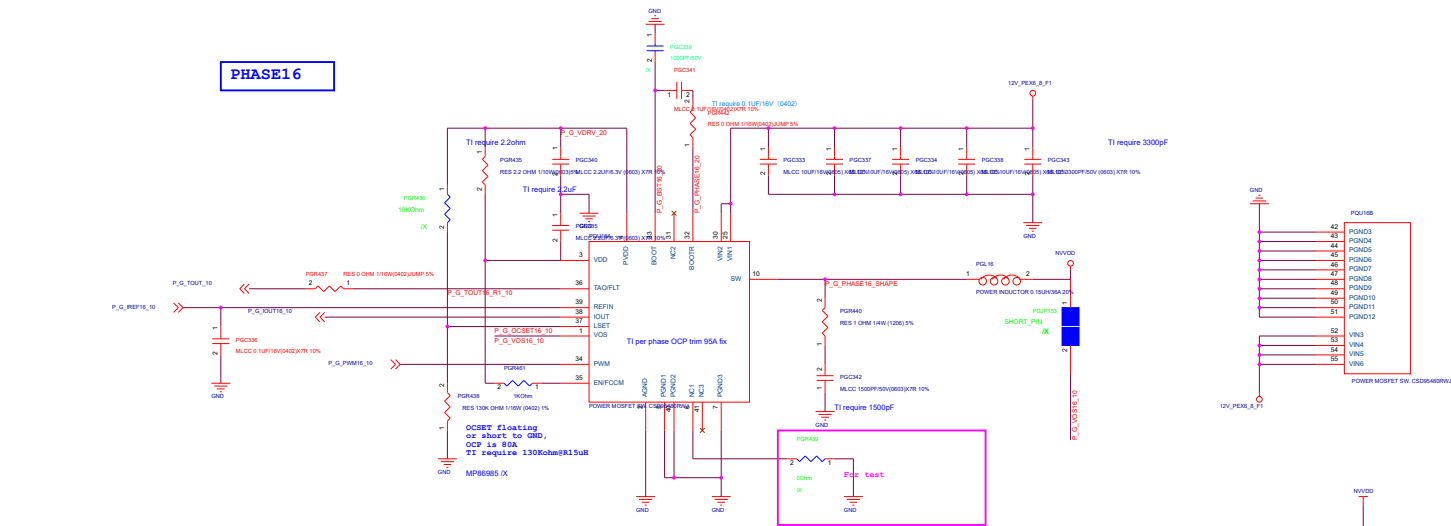
PHASE14



PHASE15



PHASE16



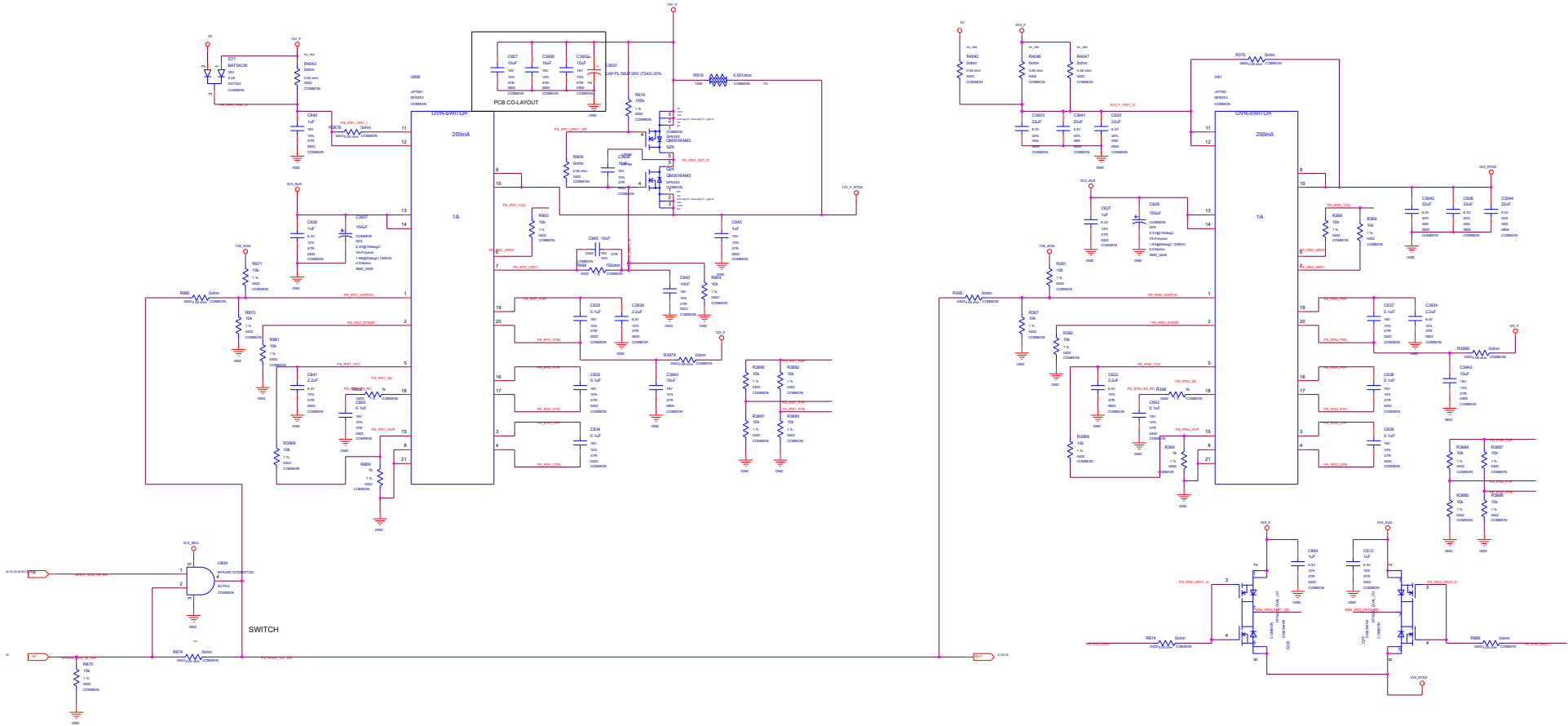
PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPI01	GPI029	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPI01	GPI029	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



NVIDIA CORPORATION

1701 S. MATEO STREET, SUITE 300

SAN JOSE, CALIFORNIA, USA 95128



PNV_PN 600-1G150-BASE-403

PCB REV: PCH150-003

DATE: 06-JUL-2018

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.



ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NONINFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.

ASSEMBLY	ASSEMBLY DESCRIPTION
PEX 6/8 PIN	PEX 6/8 PIN CURRENT STEERING

NVIDIA CORPORATION

2701 SAN TOME AVE, SUITE 5000
SANTA CLARA, CA 95050, USA



NV_PN

600-1G150-BASE-403

PCB REV

PCB150-003

BOX REV

1A

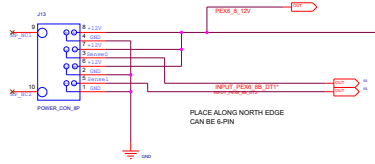
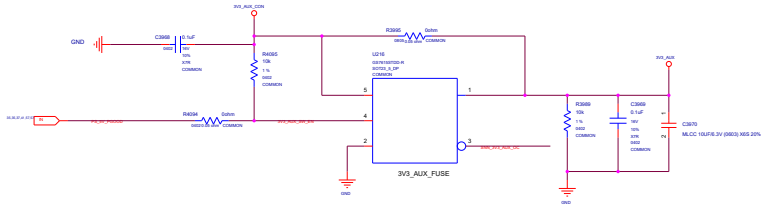
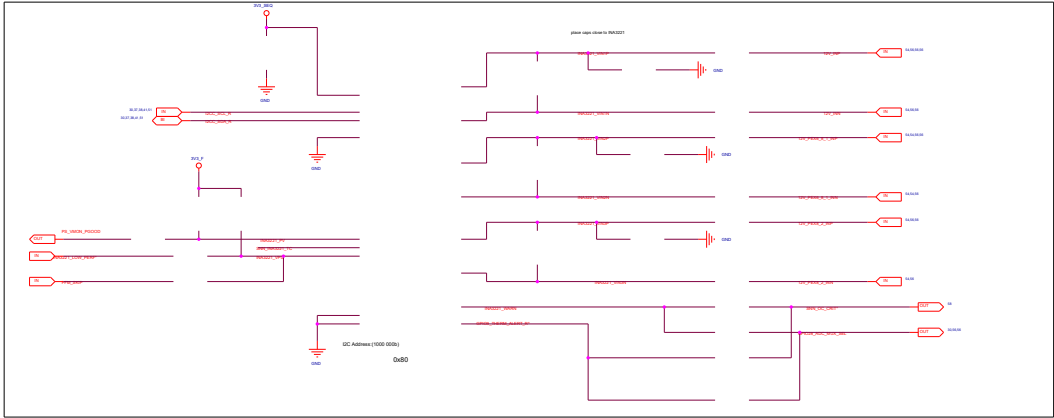
PAGE

33 OF 86

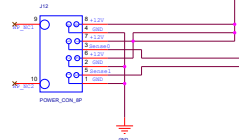
DATE

08-JUL-2018

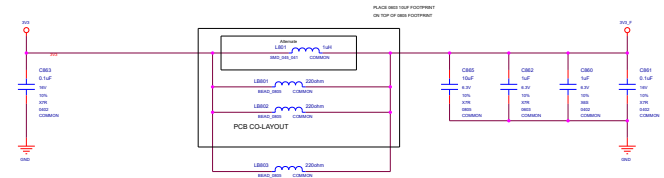
PS: Inputs, Filtering, and Monitoring



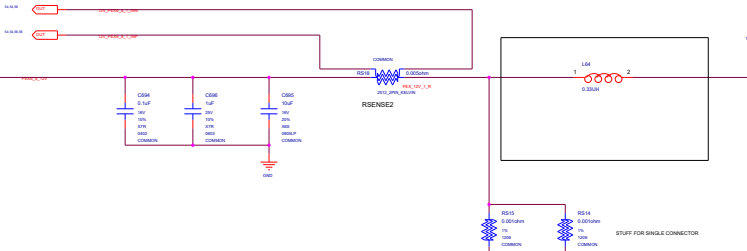
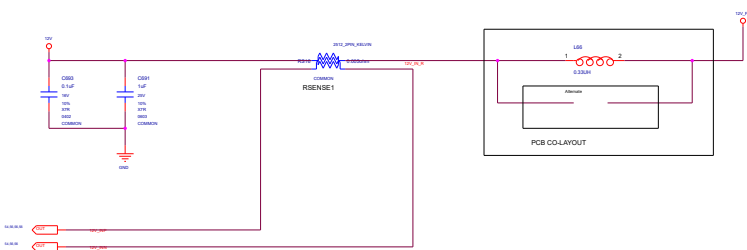
PLACE ALONG NORTH EDGE



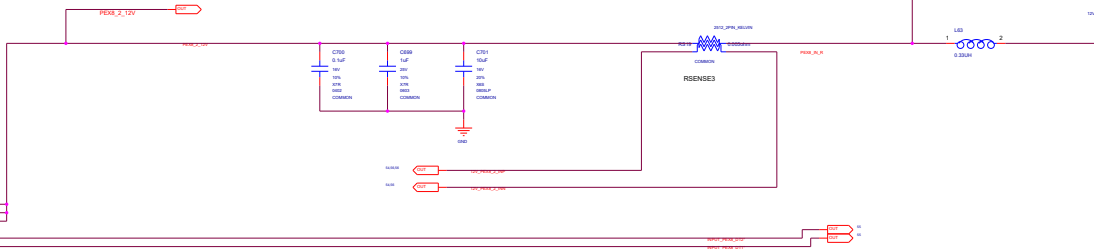
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX8 INPUT 2 - 2x4 PCIe CON 150W



NVIDIA CORPORATION

3501 SAN TOME AVE, SANTA CLARA, CA 95051, USA



REV	1.0	DATE	08-01-2018
REV	1.0	DATE	08-01-2018

PS: Pre-Filter

STUFF IF USING ZMXLX

2.7V, 5.5V
0mV, 20V
0.50A

NON-ADHESIVE
SOLDER

STUFF FOR TESA

2.7V, 5.5V
0mV, 20V
0.50A

NON-ADHESIVE
SOLDER

NVIDIA CORPORATION

2701 SAN TOME EXPRESSWAY
SANTA CLARA, CA 95050, USA



NV_PFN 600-1G150-BASE-403

PCB REV VCT150-023

BOX REV A

PAGE

38 OF 86

DATE

18-JUL-2018

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY "MATERIALS") ARE BEING PROVIDED "AS IS". THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.



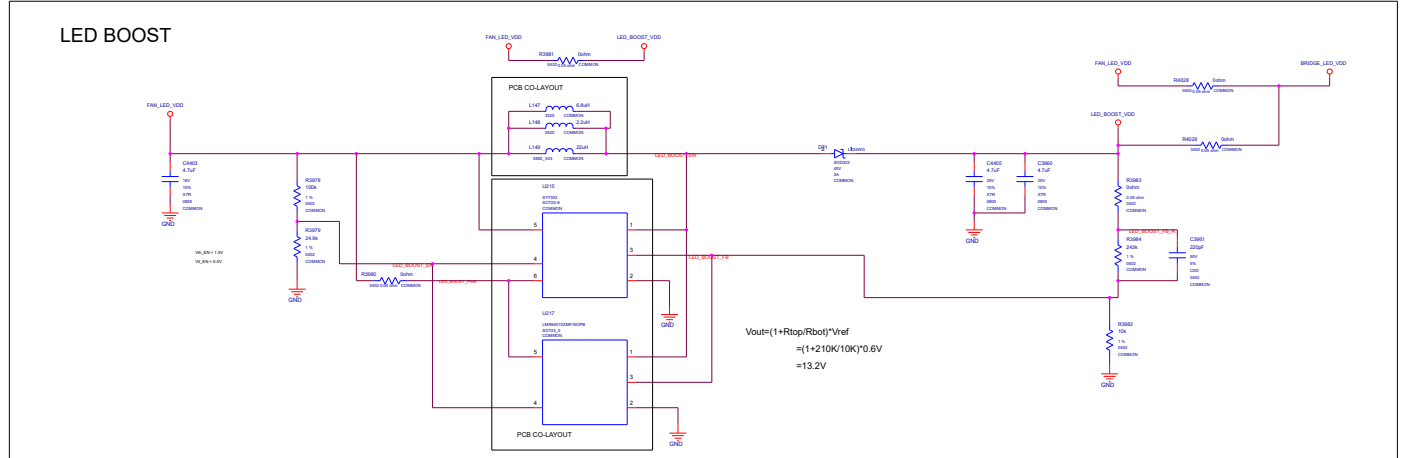
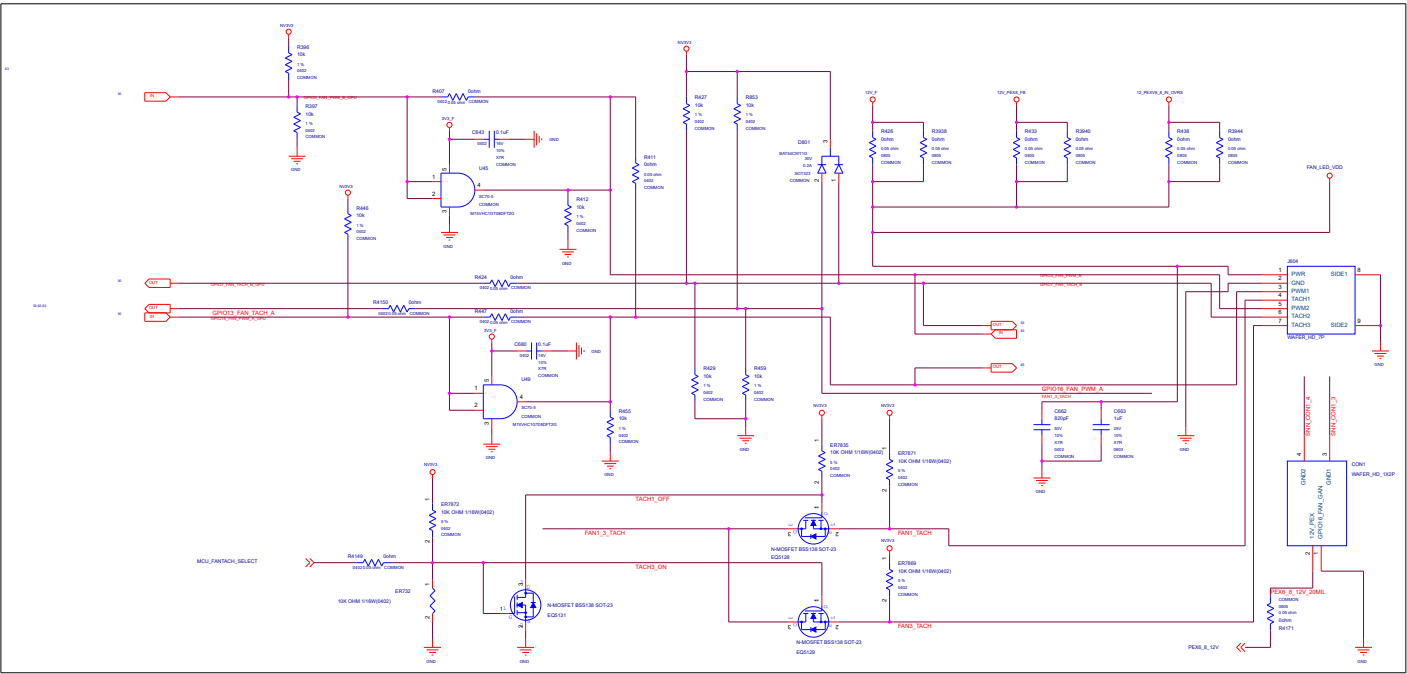
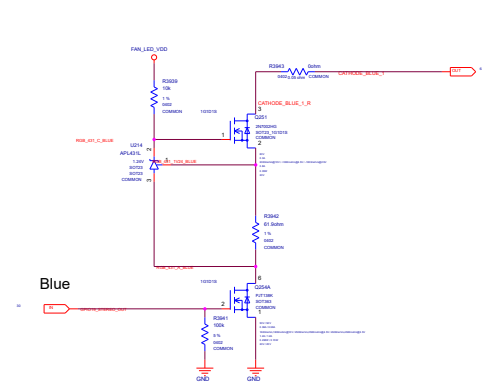
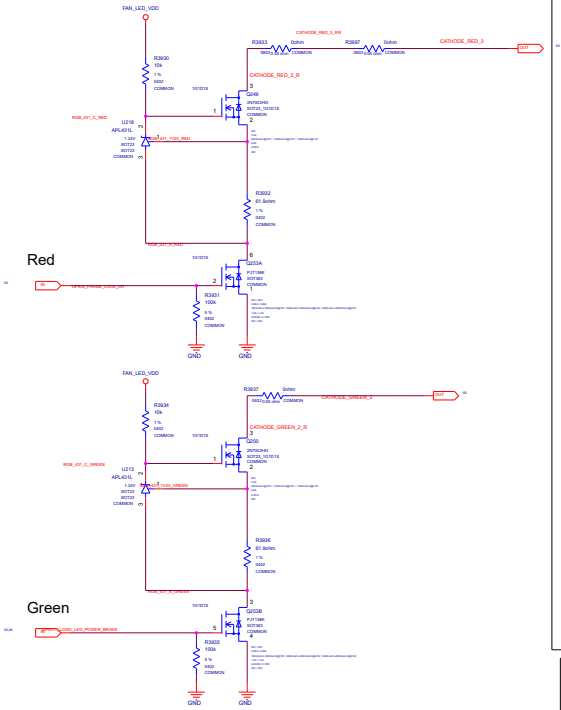
OPTIONS	PEXIOV_SENSE	PEXIOV_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3 Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

and All Input 12Vs

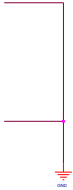
NVIDIA CORPORATION				
2701 SAN TOMAS EXPRESSWAY				
SANTA CLARA, CA 95050, USA				
NV_PN	600-1G150-BASE-403			
PCB REV	PG150-C03		PAGE	50 OF 66
BOM REV	A		DATE	08-JUL-2018



MISC: FAN & LED1



Brackets:



Bracket Screw



Back Cover



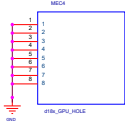
GPU Stiffner back side



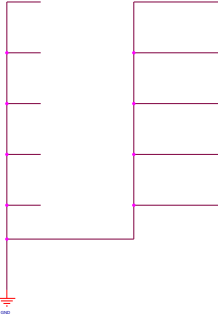
GPU Socket Symbol



GPU Mounting holes



Mechanical Holes Symbol



GPIO6_NVVDD_PSI*	PS_NVVDD_PGOOD
GPIO0_NVVDD_PWMVID	
PS_NVVDD_EN	
I2CC_SDA_R	
I2CC_SCL_R	
I2CB_SCL_R	
I2CB_SDA_R	
GPU_NVVDD_FBRTN	
GPU_NVVDD_SENSE	

GPIO25_FBVDD_PSI*	PS_FBVDD_PGOOD
GPIO8_FBVDD_SEL	
PS_FBVDD_BUFF_R	
PS_FBVDD_EN	
FBVDDQ_SENSE_RTN	
FBVDDQ_SENSE_GPU	
I2CC_SCL_R	
I2CC_SDA_R	

PS_5V_EN	PS_5V_PGOOD
----------	-------------

PS_1V8_AON_EN	PS_1V8_AON_PGOOD
GPIO1_GC6_FB_EN	PS_PEXVDD_PGOOD
PS_PEXVDD_EN	GPIO1_GC6_FB_EN
PS_1V8_MAIN_EN	

VBUS_PWR_EN	PS_USBC_ALT
VBUS_FET_EN	
USB_DSCH_CTL	
USB_I2CS_SCL	
USB_I2CS_SDA	

GPIO28_ADC_MUX_SEL	PFM_PF_BSKK
INA3221_LOW_PERF*	
PFM_SKIP	PFM_ADC_IN_P
PS_RTD3_12V_SW	PFM_ADC_IN_N
GPIO1_GC6_FB_EN	
12V_INP	
12V_INN	
12V_PEX6_8_1_INP	
12V_PEX6_8_1_INN	
12V_PEX8_2_INP	
12V_PEX8_2_INN	
12V_RTD3_PEX_INP	
12V_RTD3_PEX_INN	
12V_PEX6_8_1_OVR_INP	
12V_PEX6_8_1_OVR_INN	
12V_PEX8_1_FBP	
12V_PEX8_1_FBN	

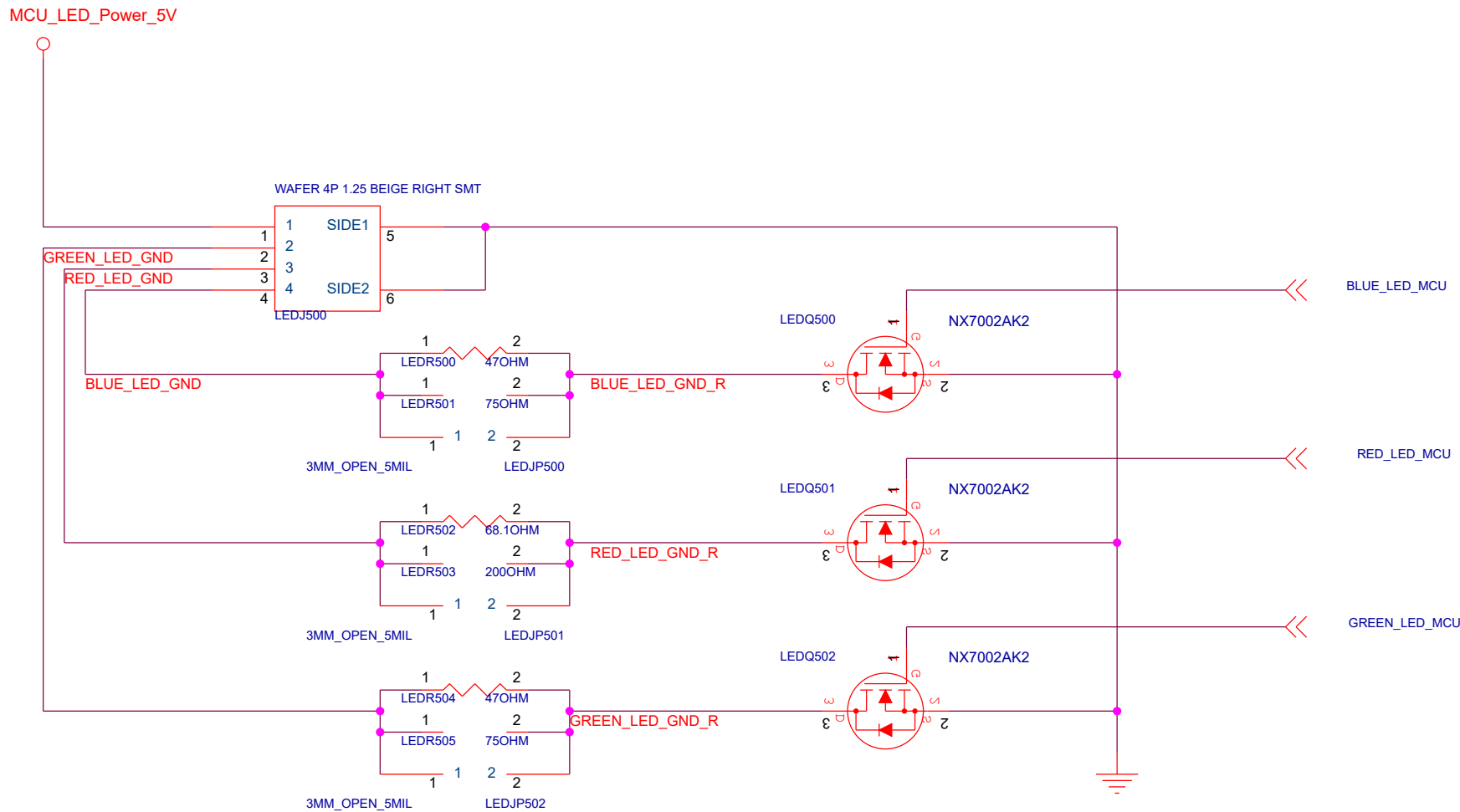
GPIO1_GC6_FB_EN	12V_PEX6_8_1_OVR_INP
GPIO29_IDLE_IN_SW	12V_PEX6_8_1_OVR_INN
PS_RTD3_12V_SW	12V_RTD3_PEX_INN
	12V_RTD3_PEX_INP

PEX_RST_BUF*	USB_I2CS_SCL
GPIO1_GC6_FB_EN	IFPB_I2CM_SDA
GPIO24_IFFP_HPD	USB_I2CS_SDA
IFPB_I2CM_SCL	GPIO24_IFFP_HPD
IFPB_I2CM_SDA	VBUS_PWR_EN
USB_CC1	PS_USBC_ALT
USB_CC2	USB_AUX_SW
	USB_CC2
	USB_AUX_SW
	USB_CC1
	USB_DSCH_CTL
	VBUS_FET_EN

PS_RB2_VCC	FP_FUSE_GPU
PS_RB2_P2P	DP_AUX_PROT
GPIO26_FF_FUSE	
PS_5V_PGOOD	
PS_NV3V3_EN	
PS_NVPEX_PGOOD	

12V_PEX8_FB	PS_VMON_PGOOD
GPIO1_GC6_FB_EN	PFM_SKIP
PS_RTD3_12V_SW	
PFM_PF_BSKK	

S0014 LIGHT BACK PLATE

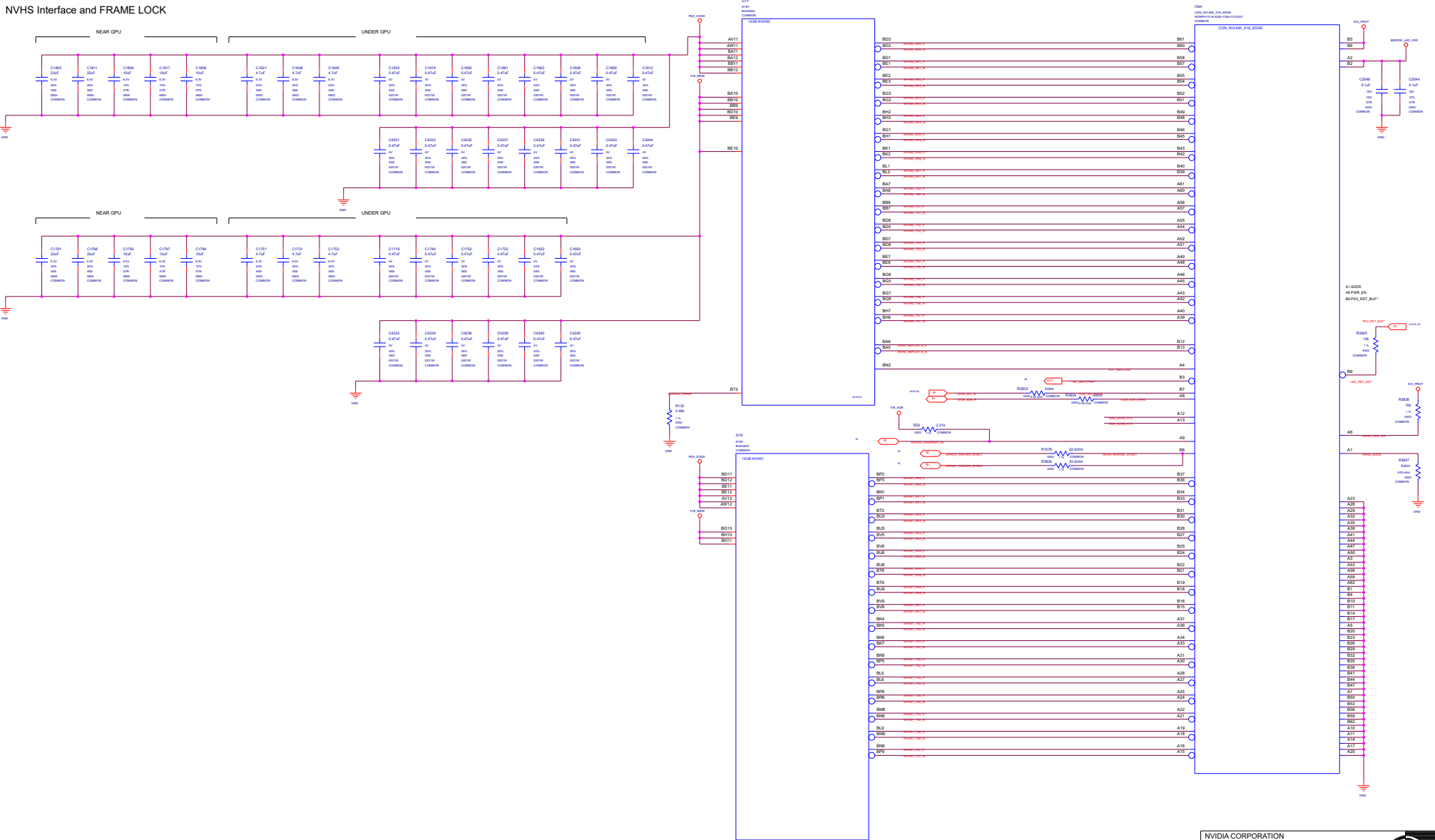


Power

MCU_LED_Power_5V

From S000

NVHS Interface and FRAME LOCK



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	NVHS X10

NVIDIA CORPORATION

2234 SAN TOMAS EXPRESSWAY

NV_PN	600-1G150-BASE-403
-------	--------------------

ALL NVIDIA DESIGN SPECIFICATIONS, REFERENCE SPECIFICATIONS, REFERENCE BOARDS, FILES, DRAWINGS, DIAGNOSTICS, LISTS AND OTHER DOCUMENTS OR INFORMATION (TOGETHER AND SEPARATELY, "MATERIALS") ARE BEING PROVIDED "AS IS." THE MATERIALS MAY CONTAIN KNOWN AND UNKNOWN VIOLATIONS OR DEVIATIONS OF INDUSTRY STANDARDS AND SPECIFICATIONS. NVIDIA MAKES NO WARRANTIES, EXPRESSED, IMPLIED, STATUTORY OR OTHERWISE WITH RESPECT TO THE MATERIALS OR OTHERWISE, AND EXPRESSLY DISCLAIMS ALL IMPLIED WARRANTIES INCLUDING, WITHOUT LIMITATION, THE WARRANTIES OF DESIGN, OF NON-INFRINGEMENT, MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE, OR ARISING FROM A COURSE OF DEALING, TRADE USAGE, TRADE PRACTICE, OR INDUSTRY STANDARDS.