PG150-C03

384b GDDR6 x16
TALL DP + DP + DP + HDMI/DP + USB

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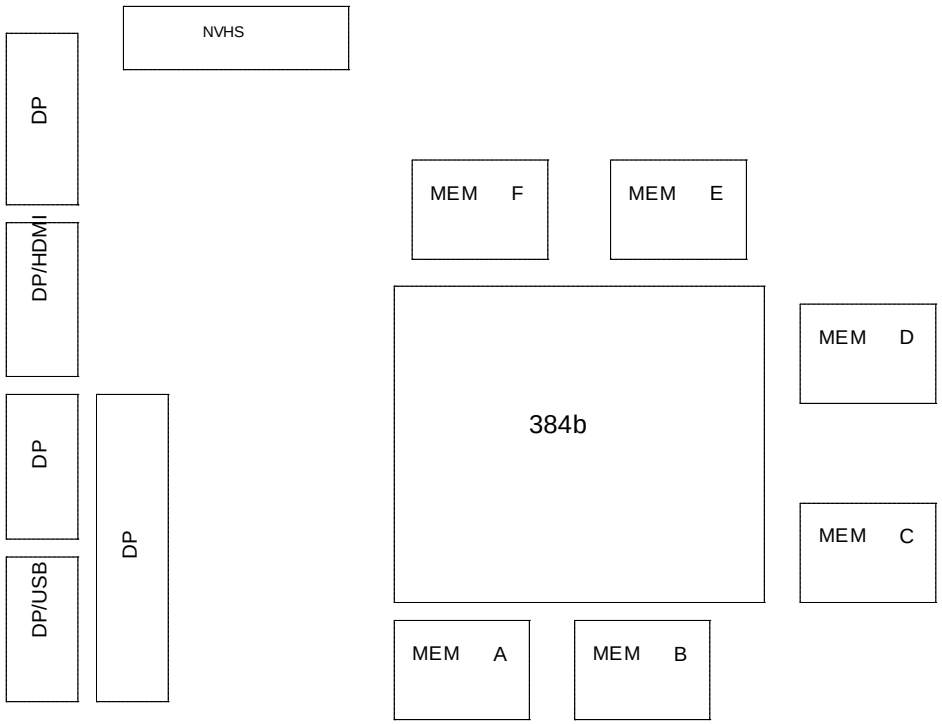

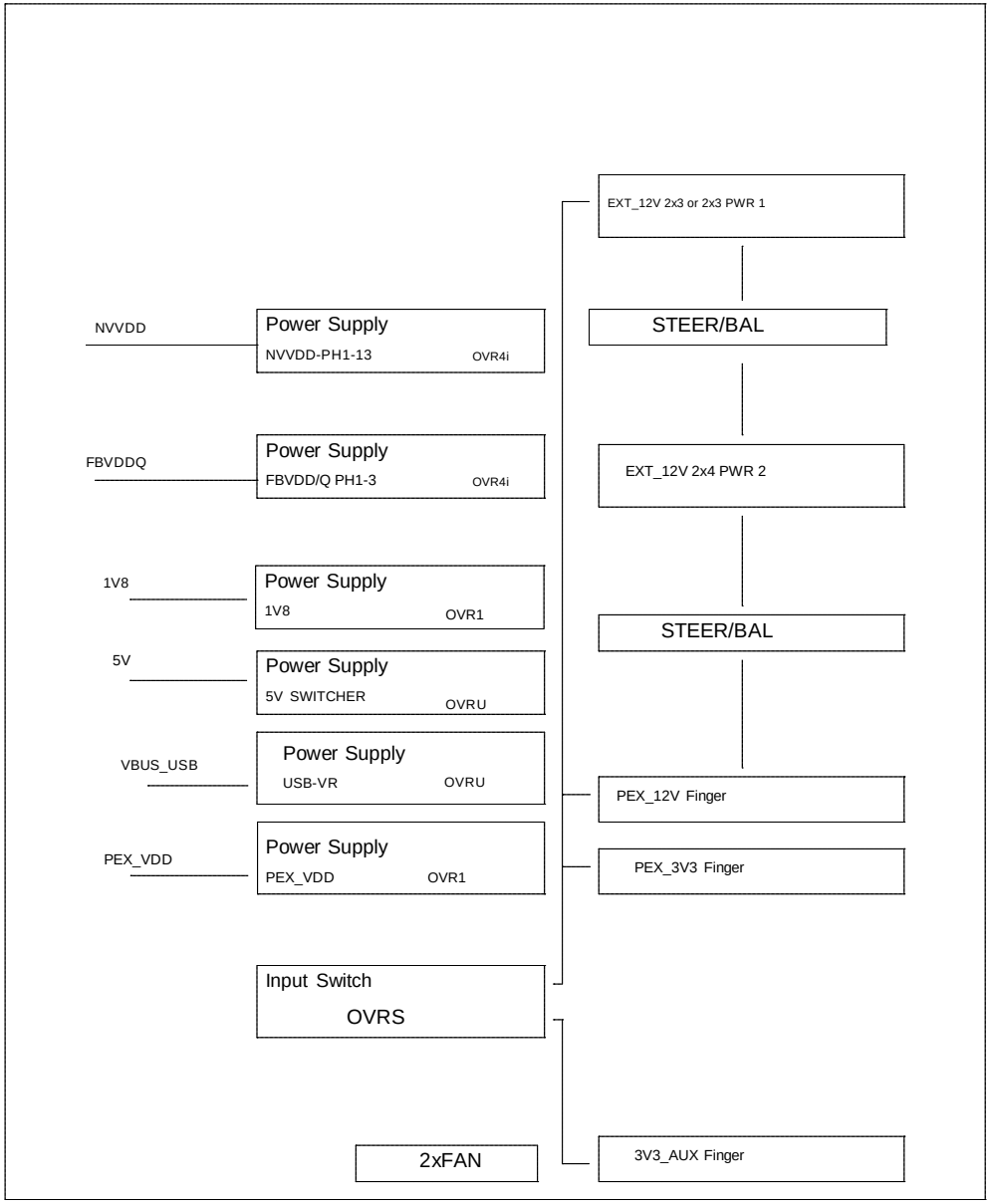

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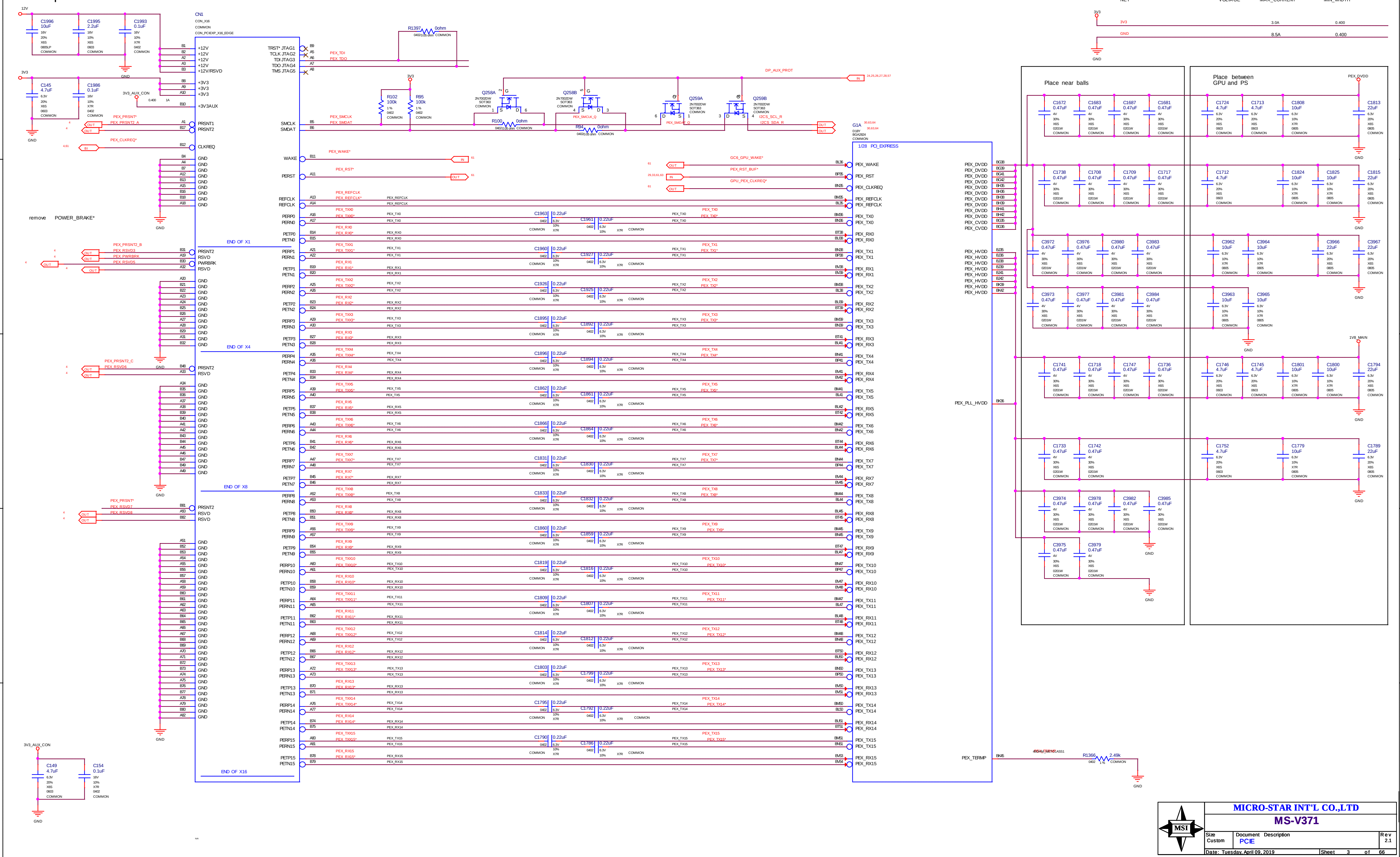
PCI Express



CN1
CON_X16
COMMON
CON_PCIEXP_X16_EDGE
12V
3V3
3V3_AUX_CON
remove POWER_BRAKE*
END OF X1
END OF X4
END OF X8
END OF X16
PEX_PRSNT*
PEX_PRSNT2_A
PEX_CLKREQ*
PEX_WAKE*
PEX_RST*
PEX_REFCLK
PEX_REFCLK*
PEX_TDI
PEX_TDO
PEX_SMCLK
PEX_SMDAT
DP_AUX_PROT
I2CS_SCL_R
I2CS_SDA_R
GC6_GPU_WAKE*
PEX_RST_BUF*
GPU_PEX_CLKREQ*
Q258A
Q258B
Q259A
Q259B
2N7002DW
SOT363
R102 100k
R95 100k
R100 0ohm
R94 0ohm
R1397 0ohm
G1A
1/28 PCI_EXPRESS
PEX_WAKE
PEX_RST
PEX_CLKREQ
PEX_REFCLK
PEX_DVDD
PEX_HVDD
PEX_PLL_HVDD
PEX_TERMP
R1366 2.49k
Place near balls
Place between GPU and PS
PEX_DVDD
1V8_MAIN
NET
VOLTAGE
MAX_CURRENT
MIN_WIDTH
3V3 3.0A 0.400
GND 8.5A 0.400
GND
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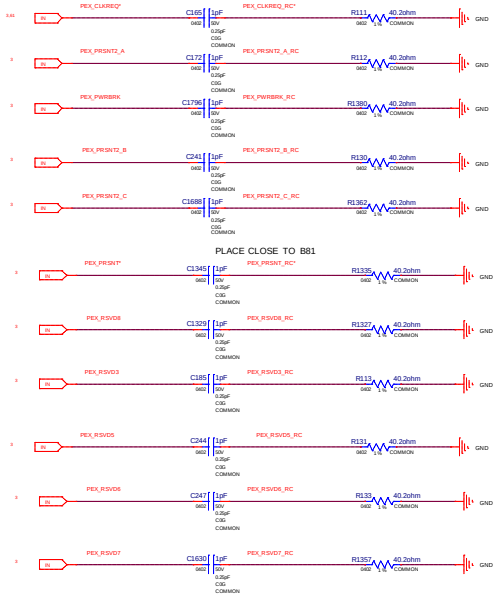
PCI TERM



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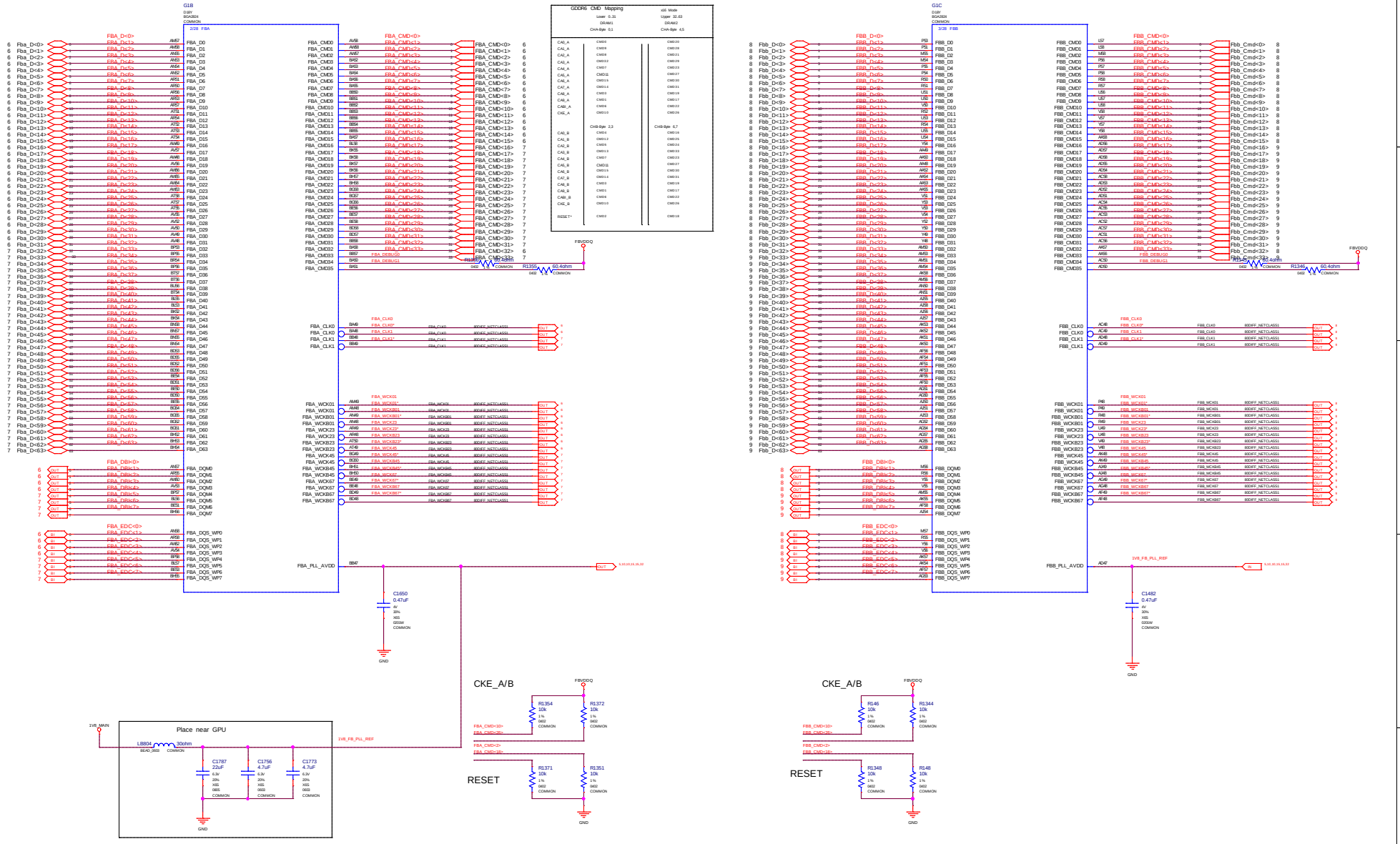
MEMORY: GPU Partition A/B



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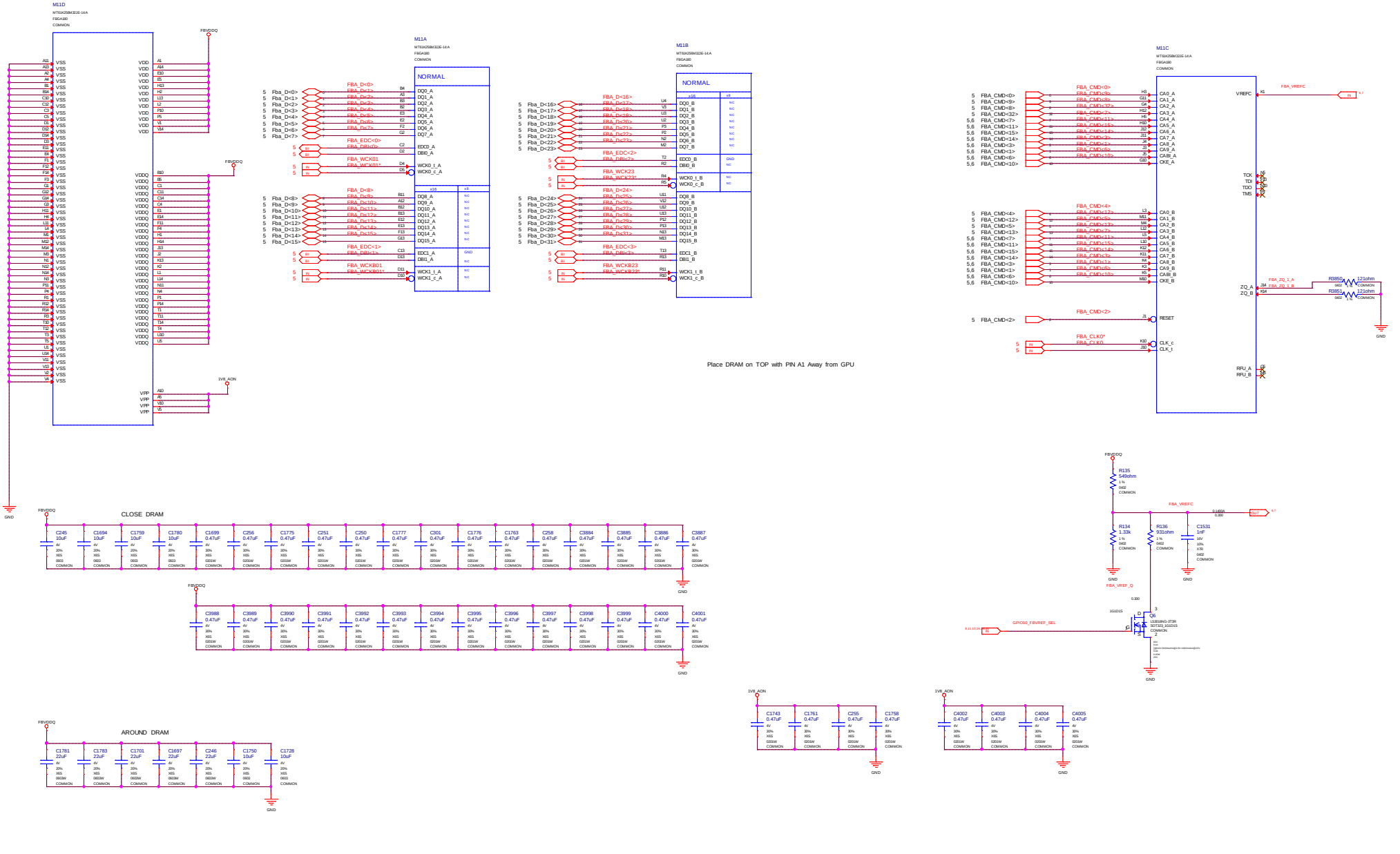
MEMORY: FBA Partition 31..0



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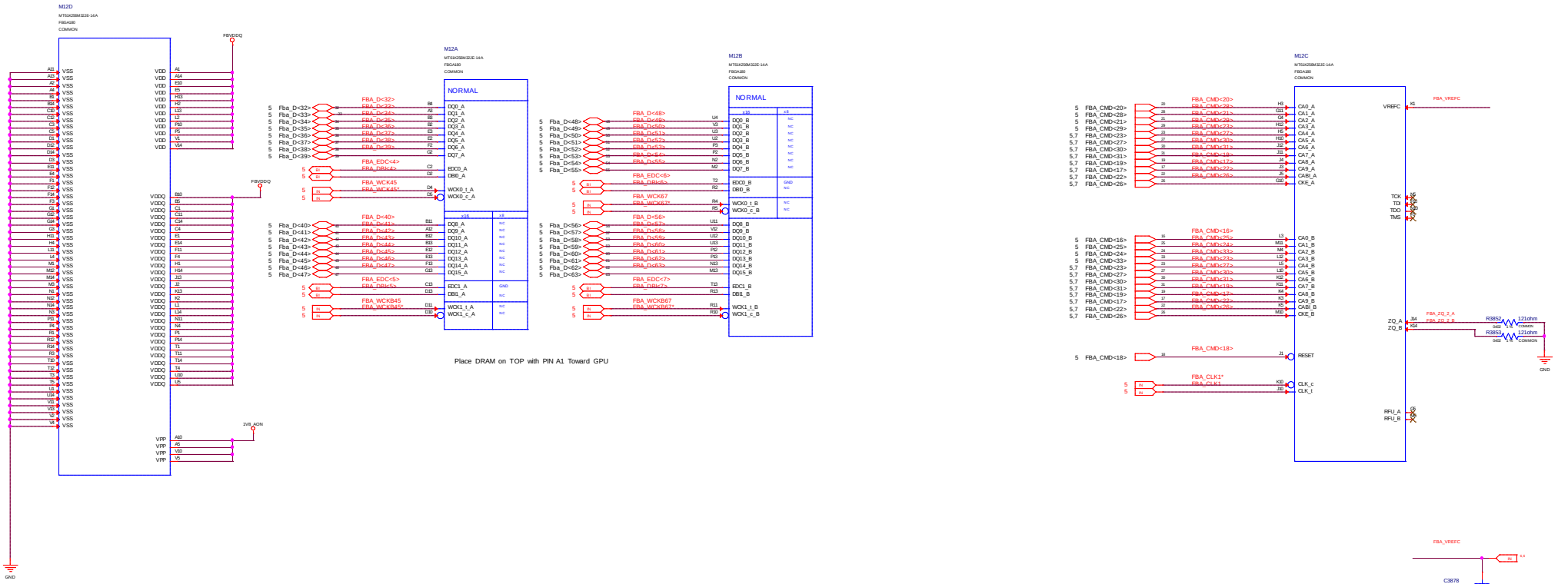
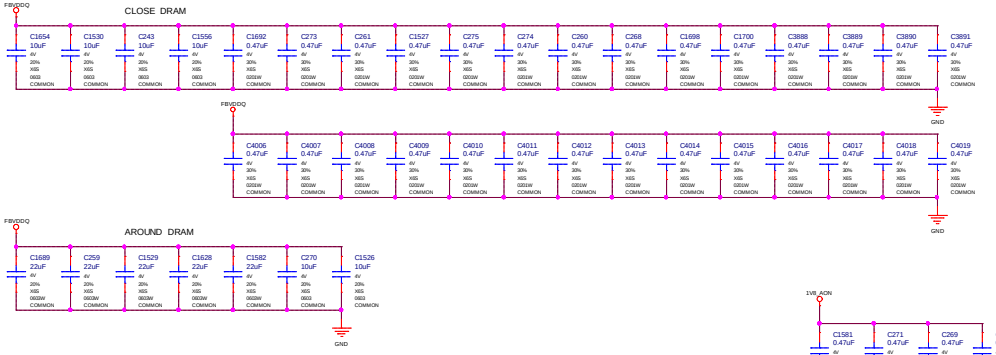
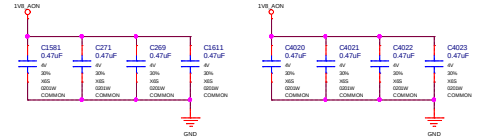
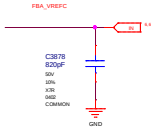
MEMORY: FBA Partition 63..32









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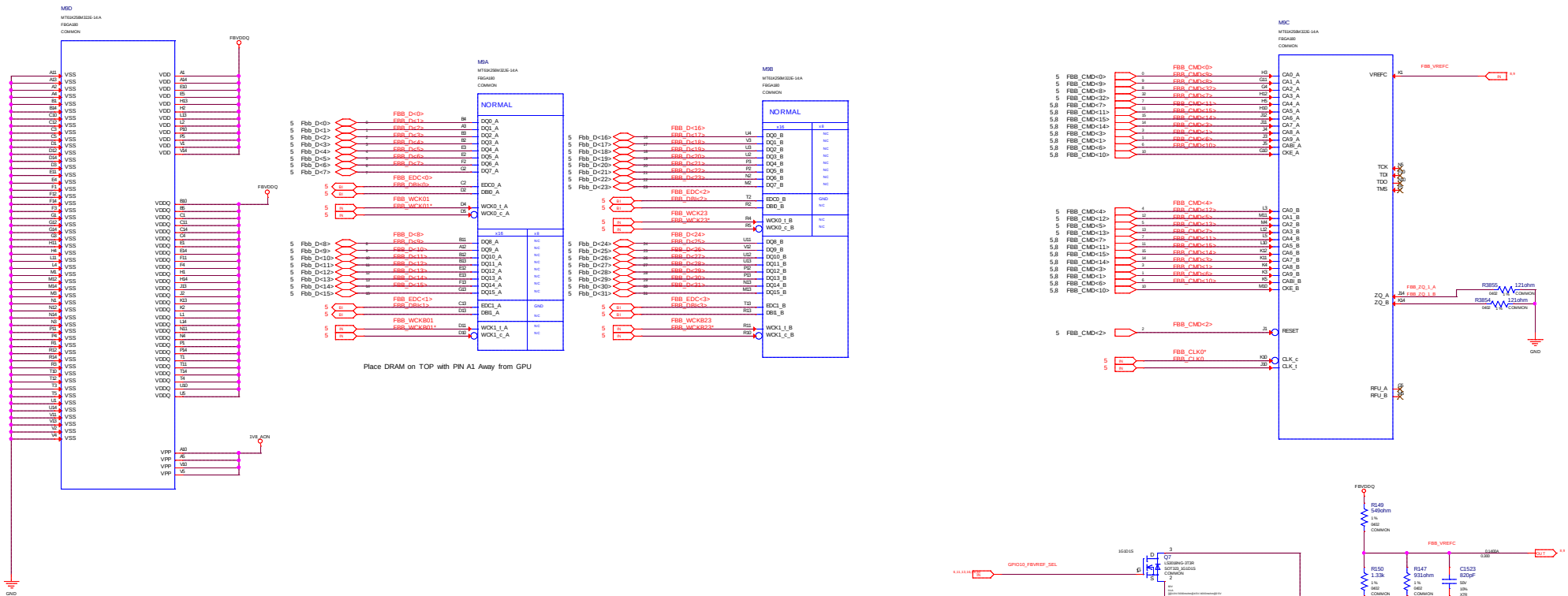
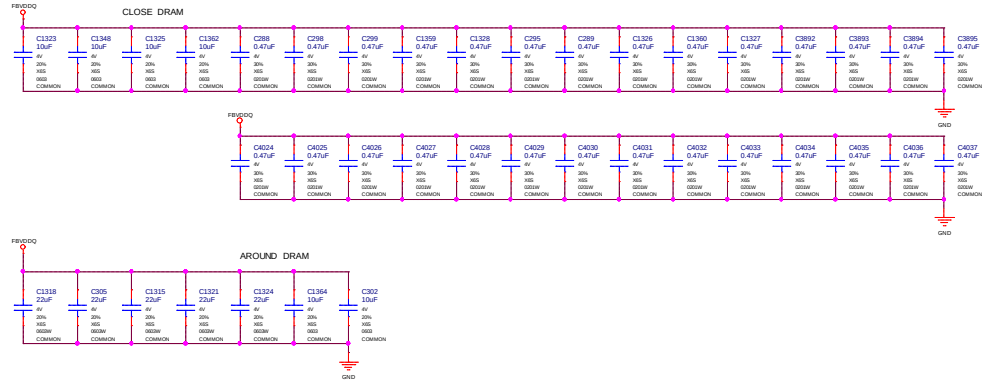
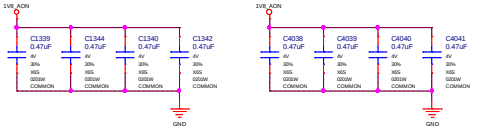
MEMORY: FBB Partition 31..0







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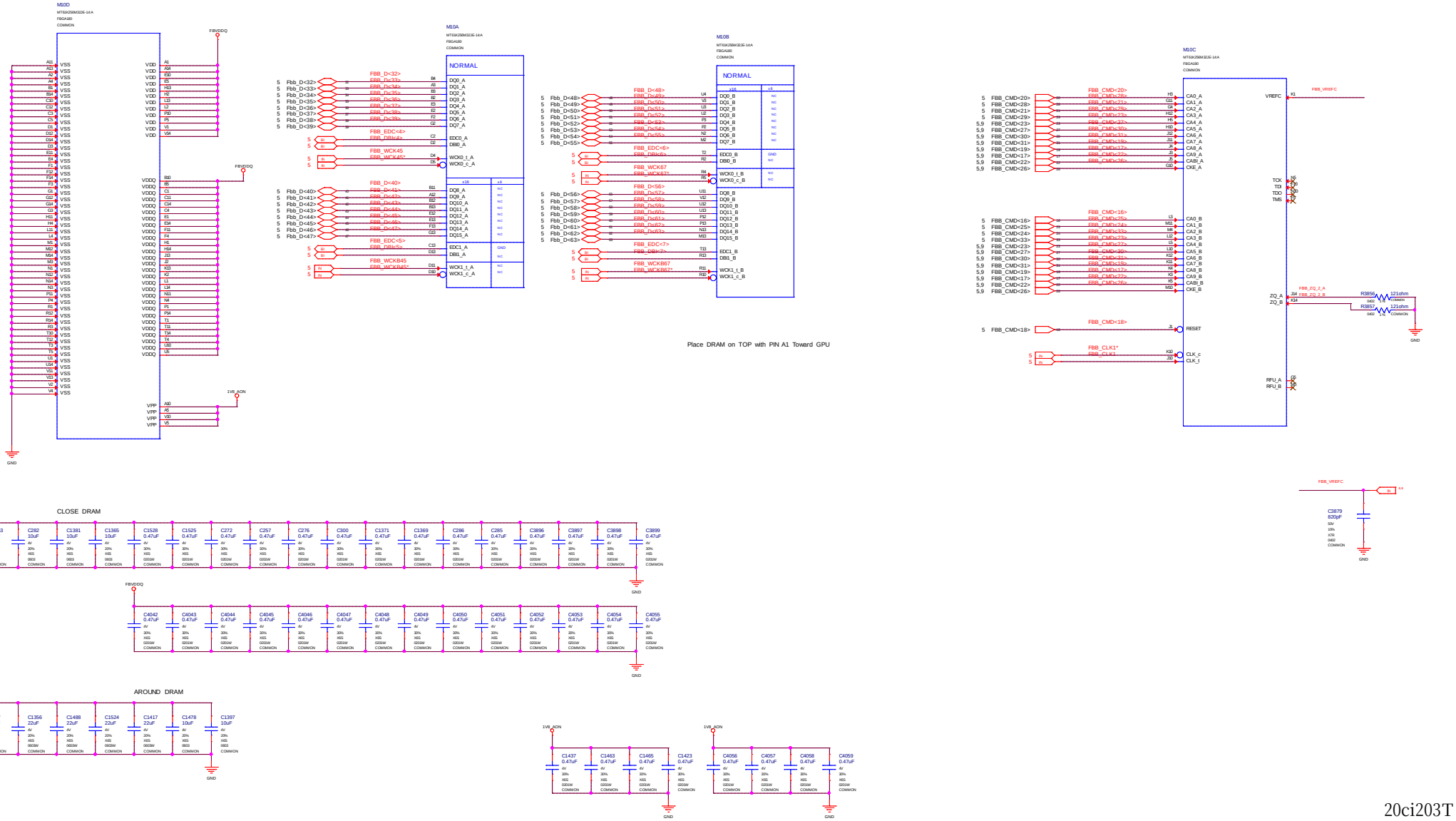
MEMORY: FBB Partition 63..32



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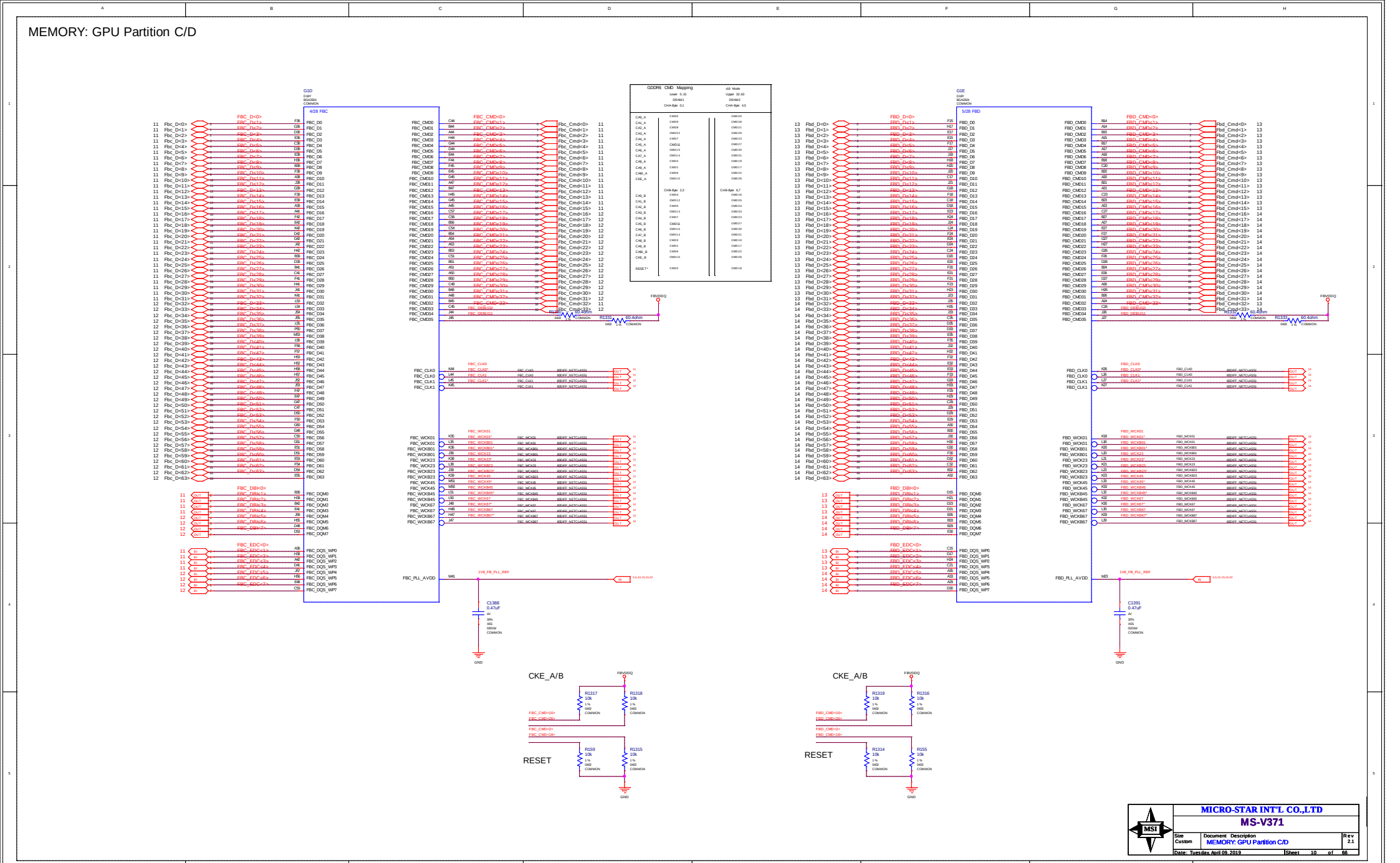
MEMORY: GPU Partition C/D



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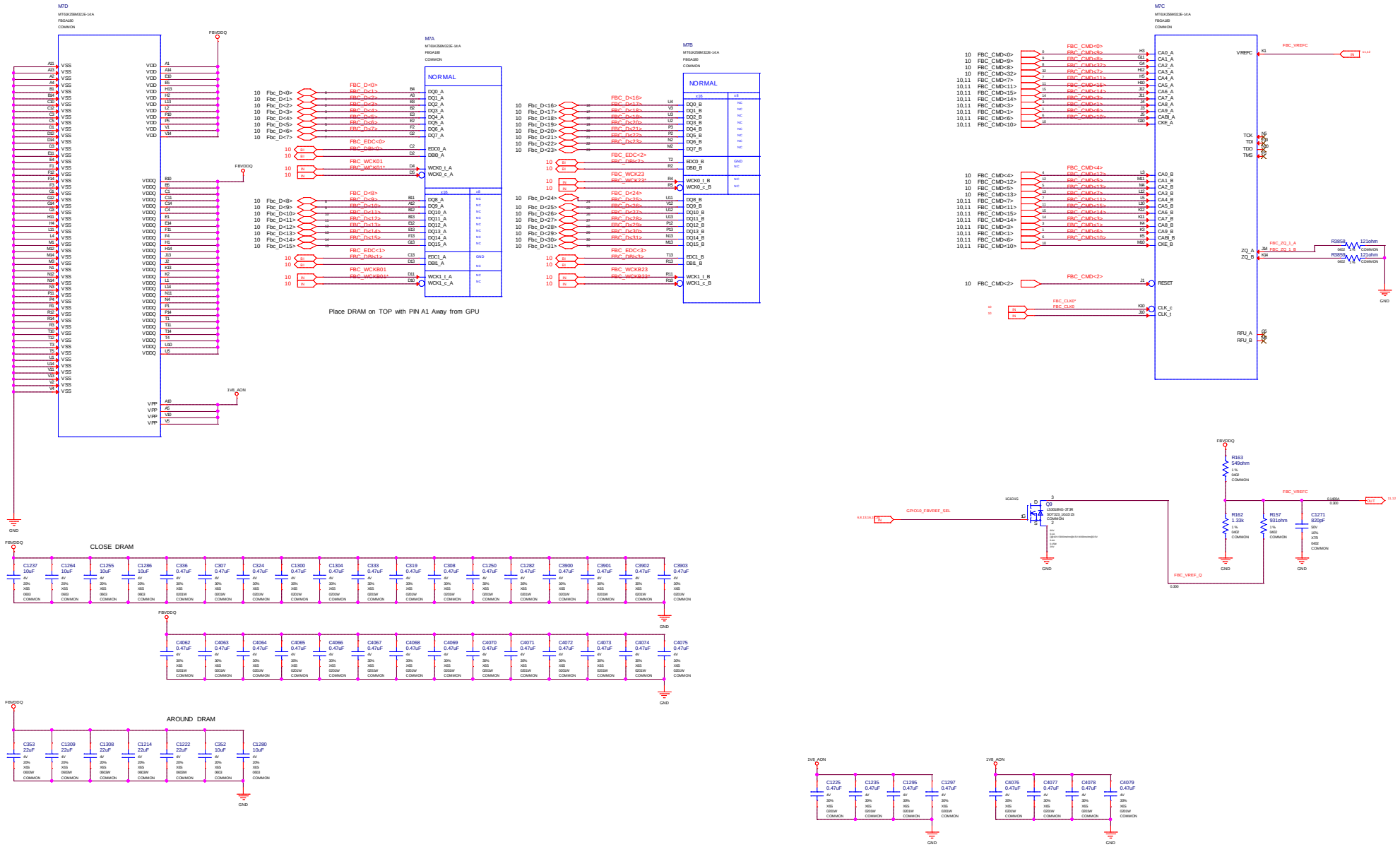
MEMORY: FBC Partition 31..0



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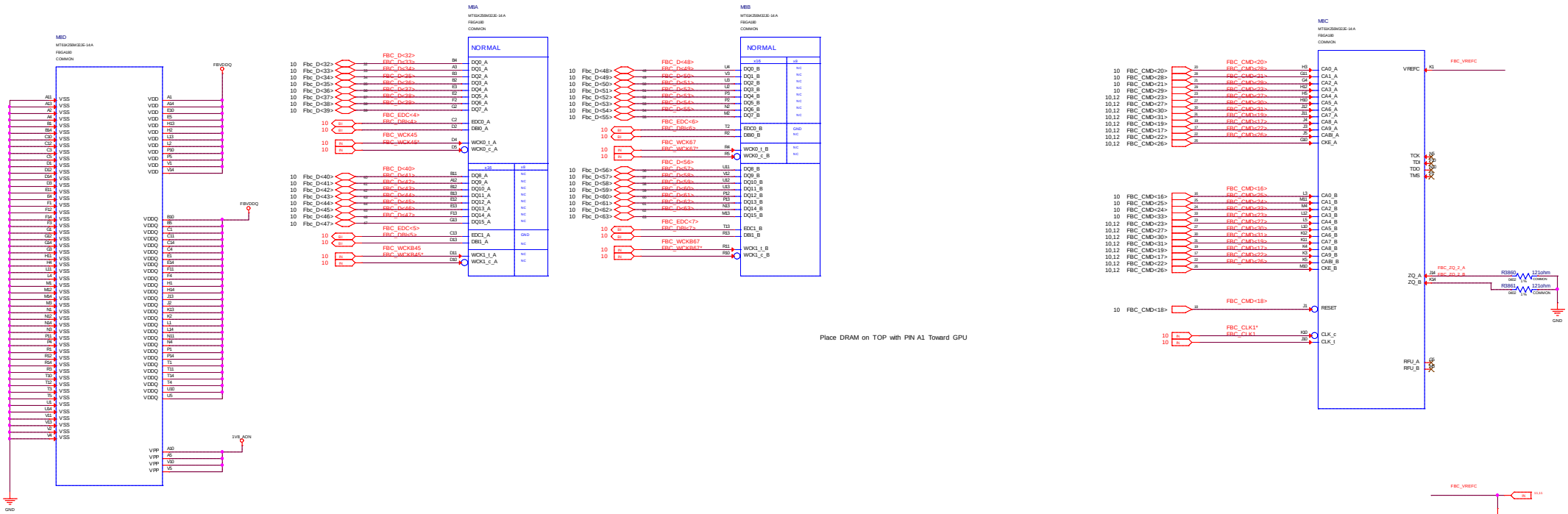
MEMORY: FBC Partition 63..32



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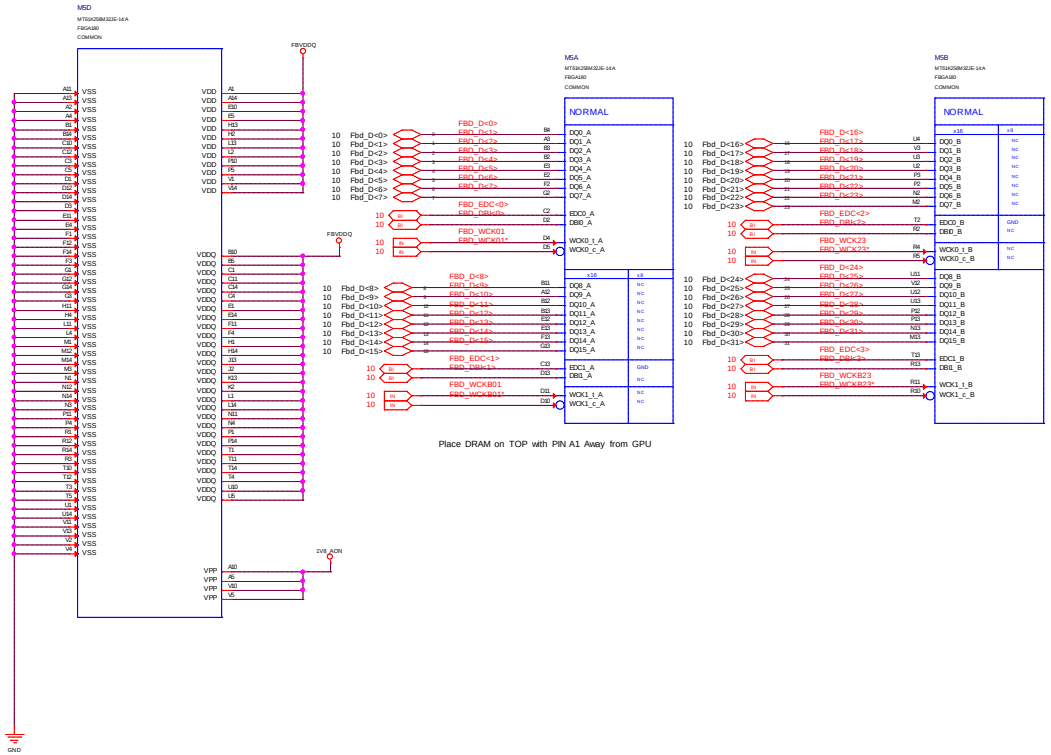
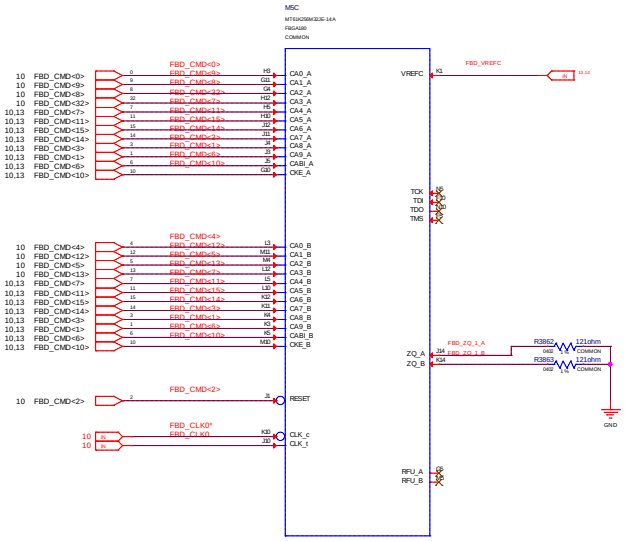
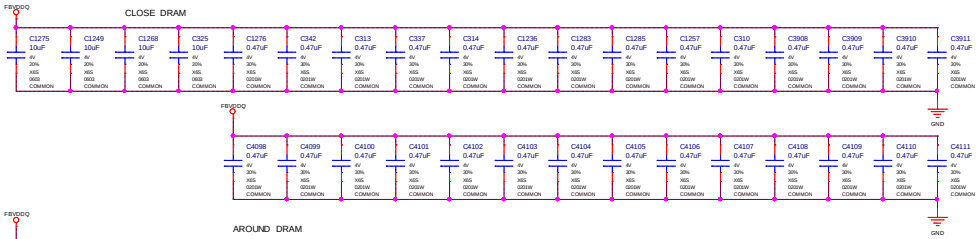
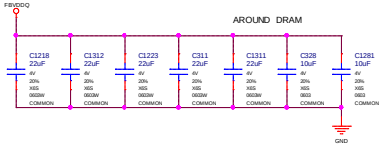
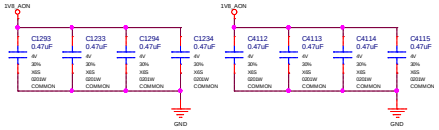
MEMORY: FBD Partition 31..0











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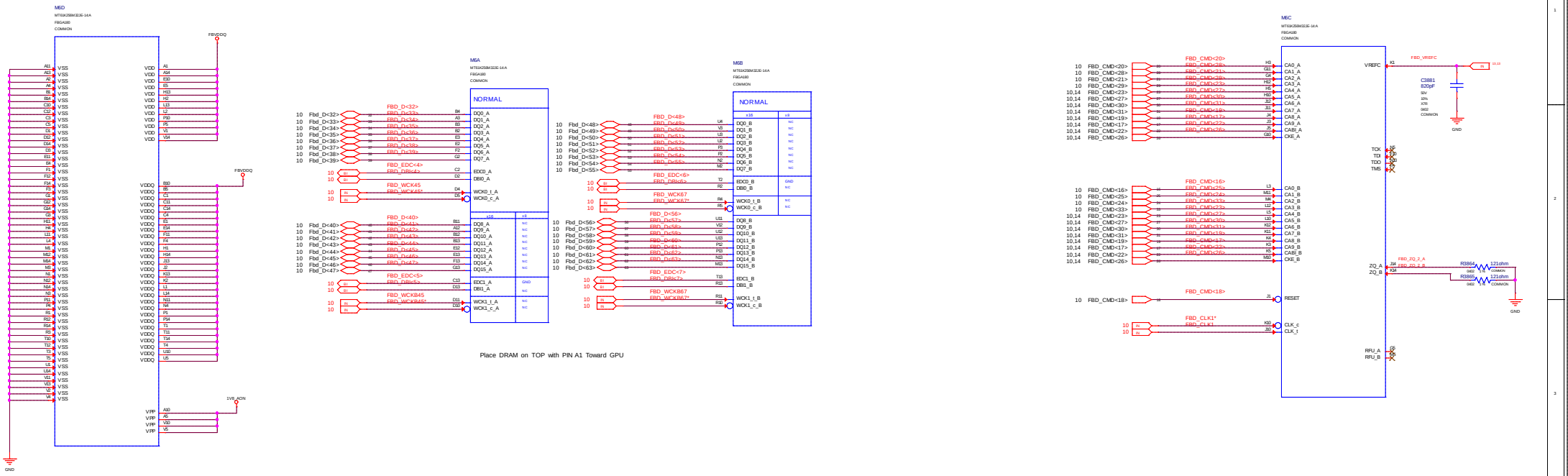
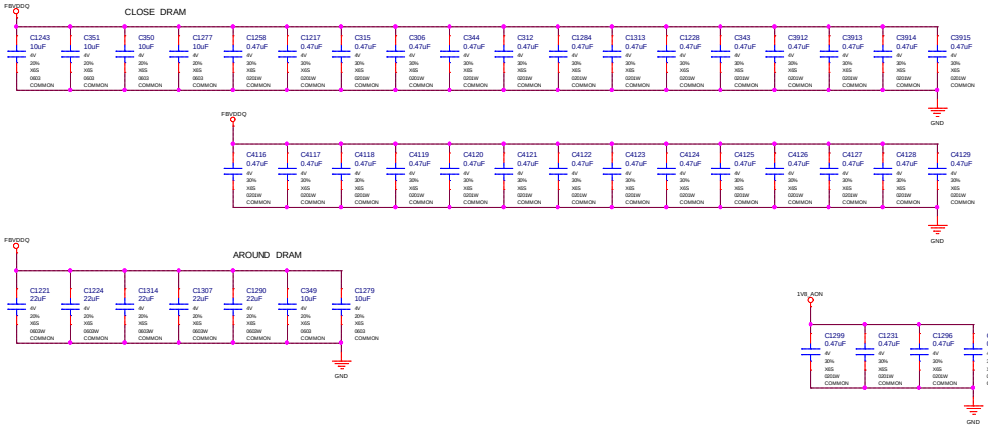
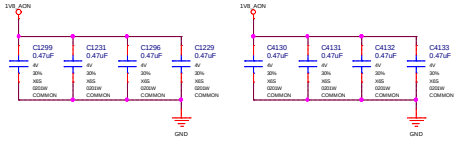
MEMORY: FBD Partition 63..32







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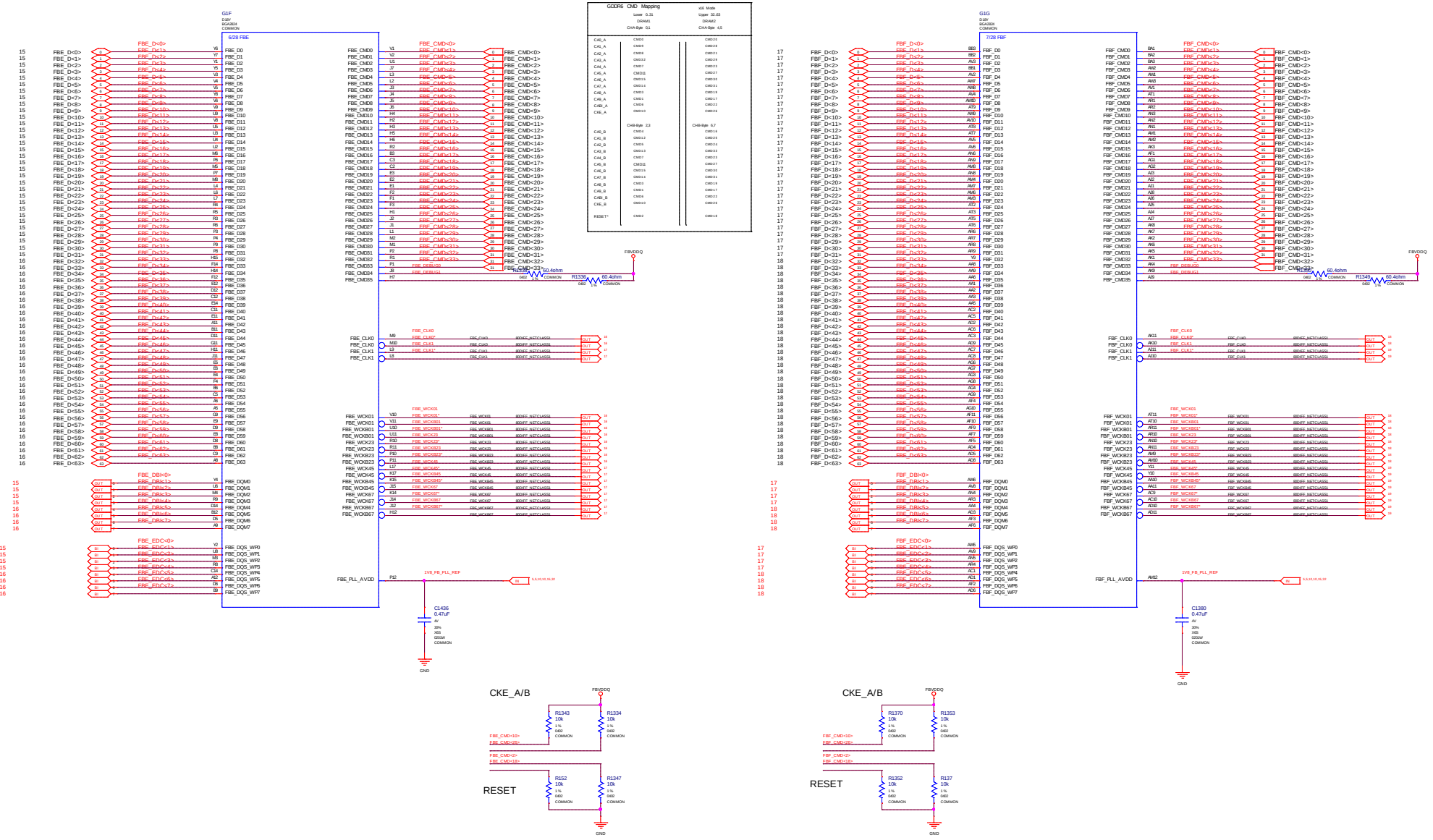
MEMORY: GPU Partition E/F



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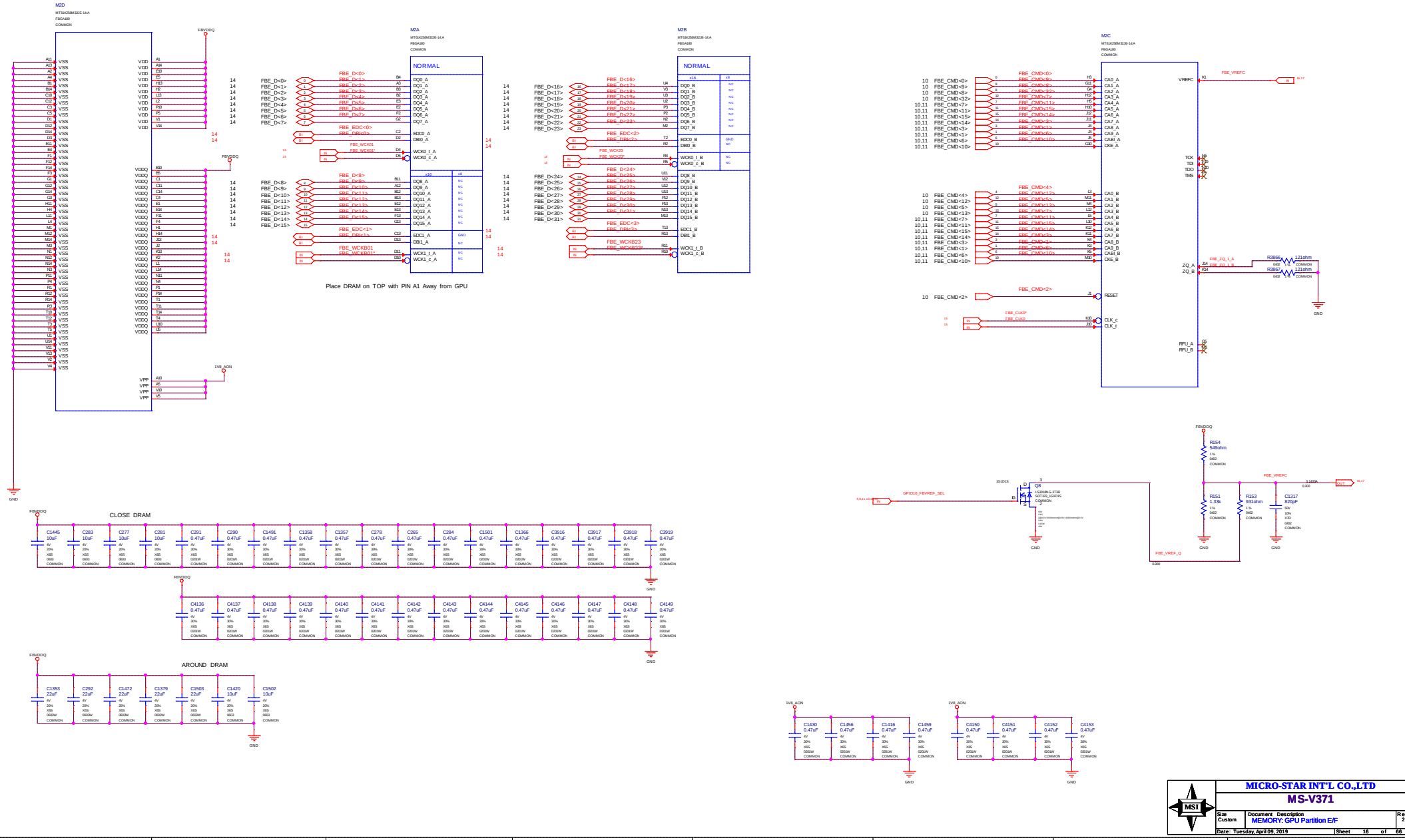
MEMORY: FBE Partition 31..0



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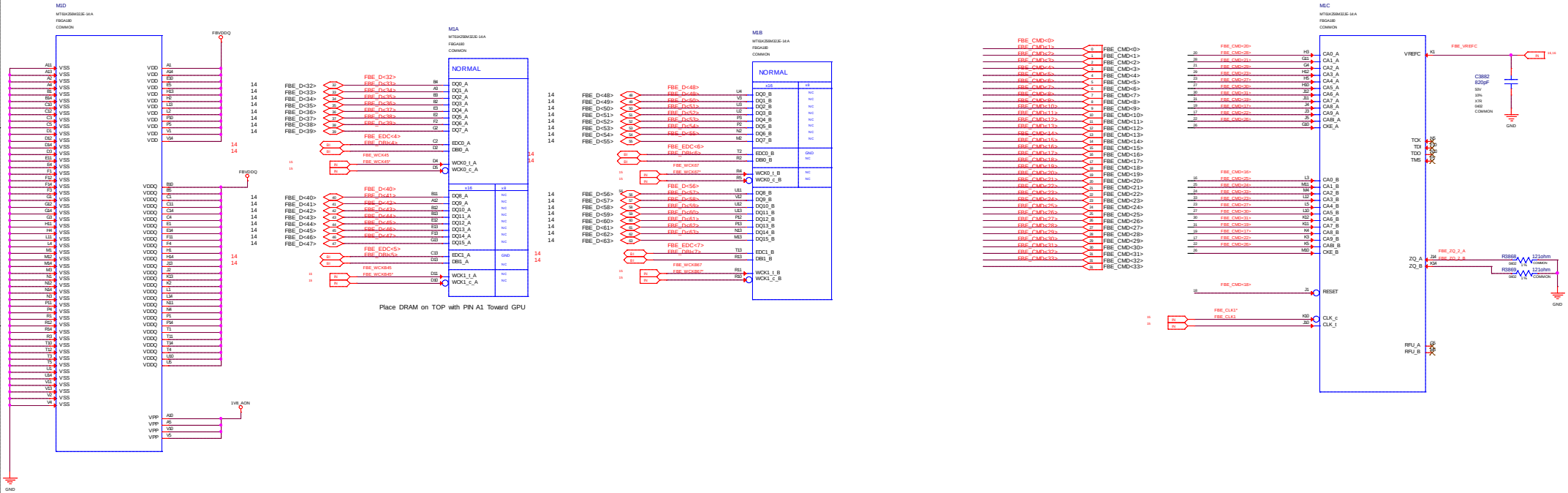

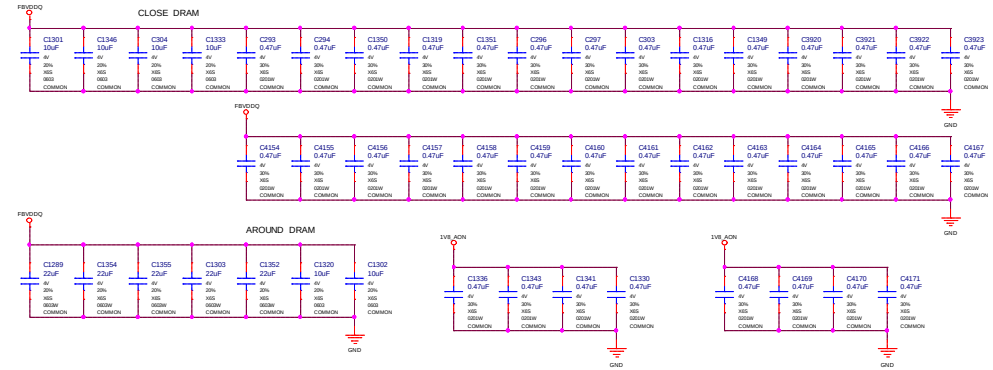

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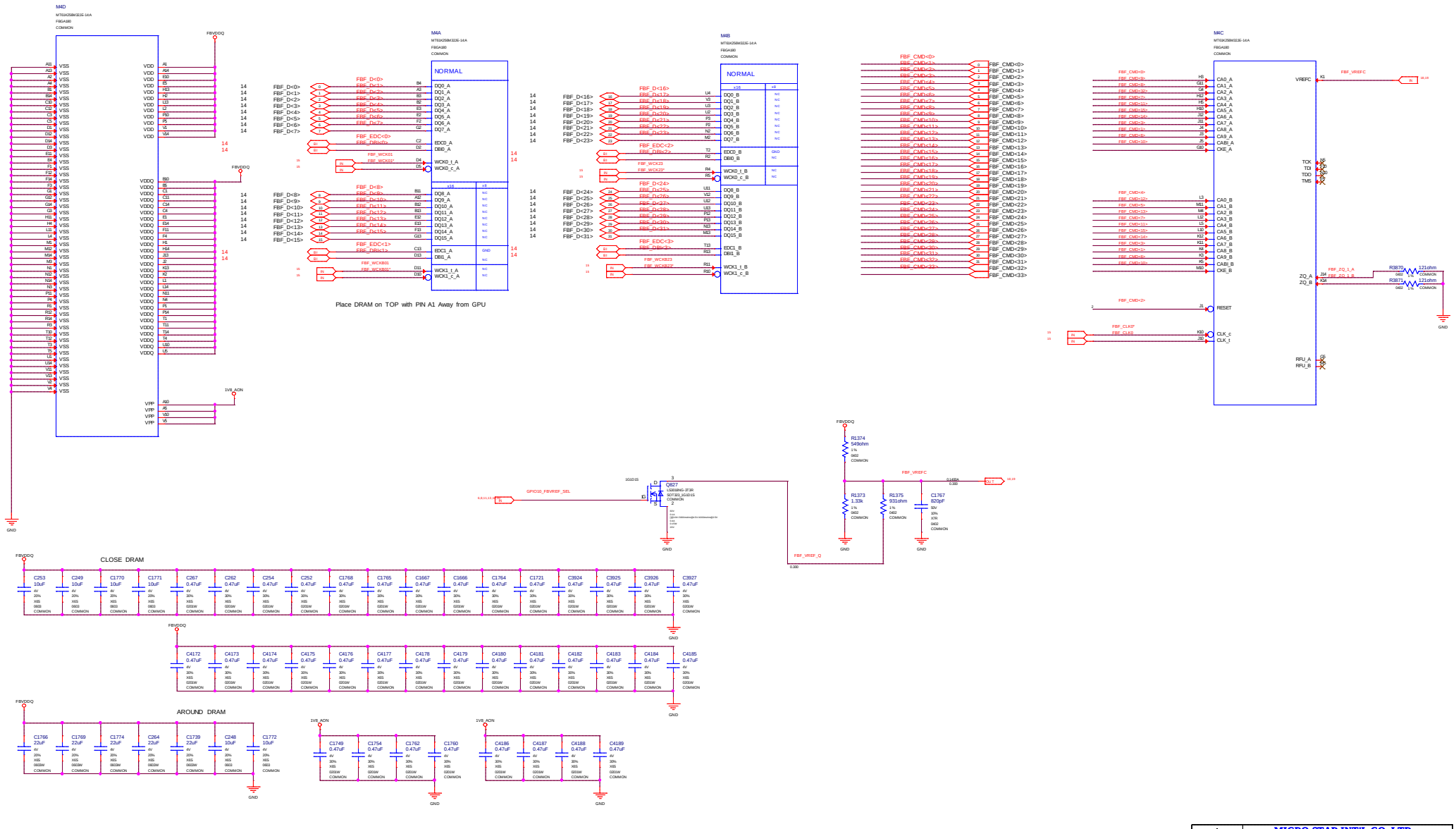
MEMORY: FBF Partition 31..0



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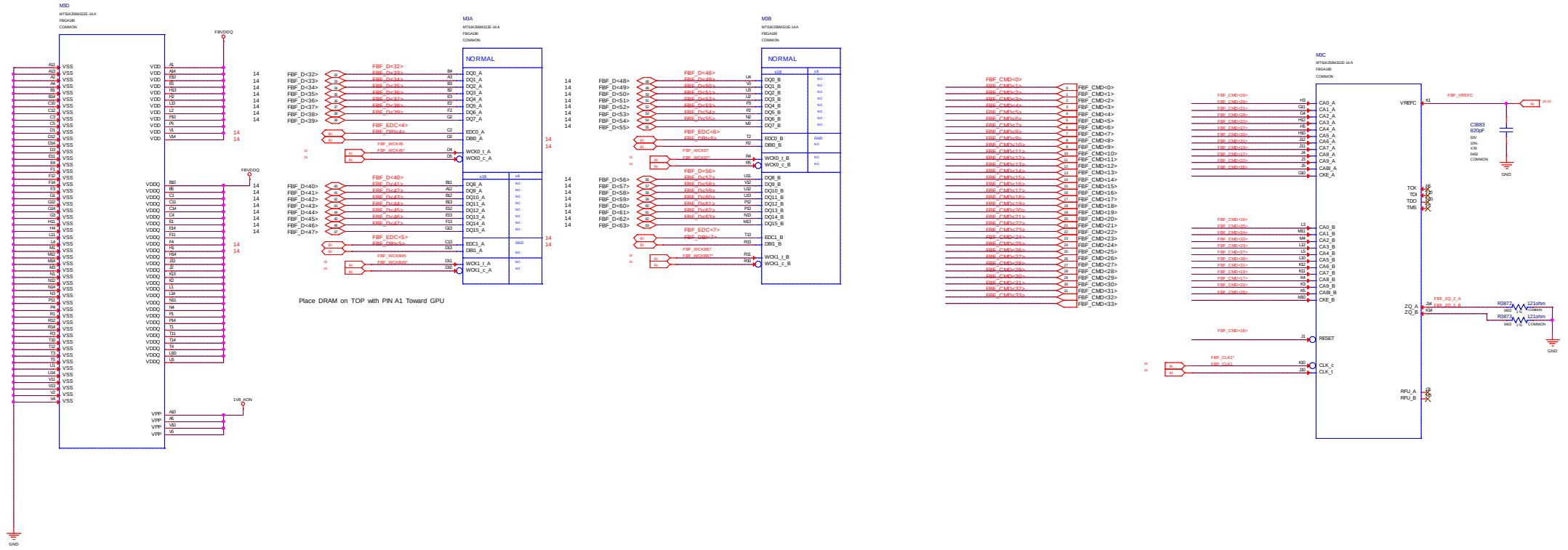

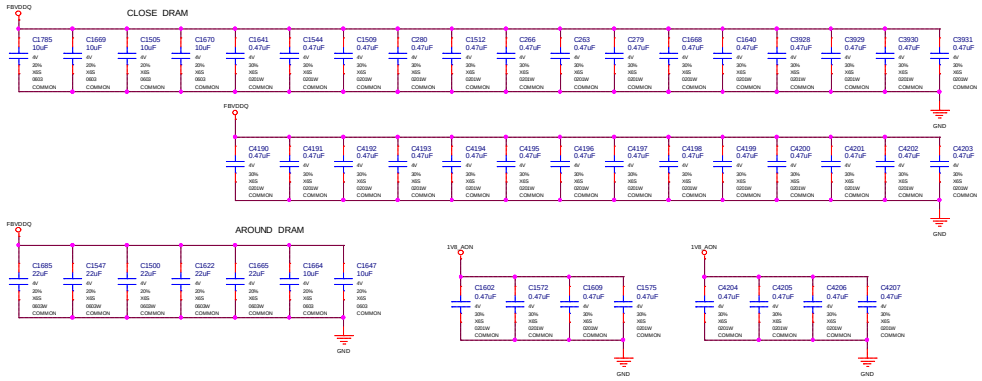

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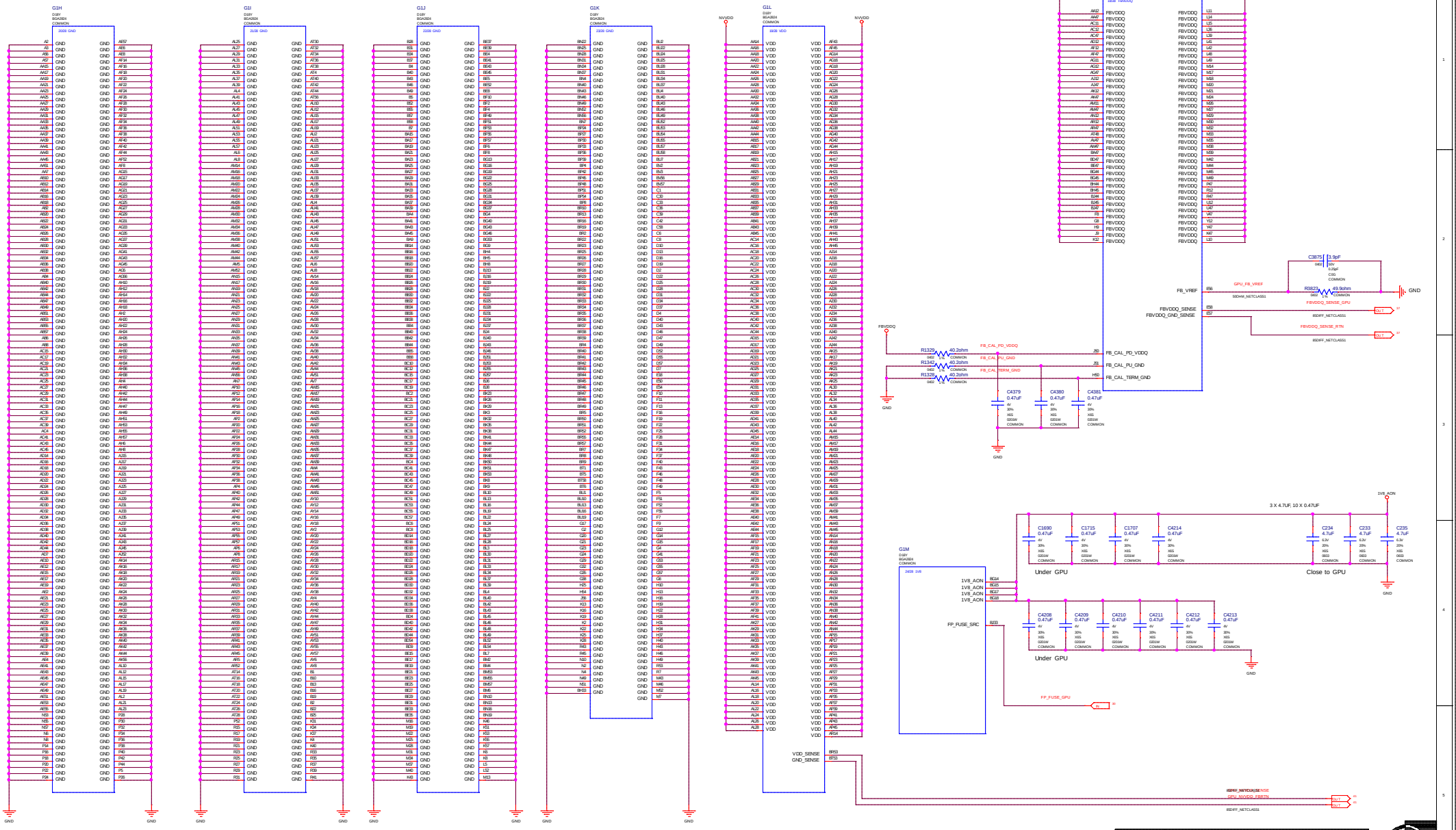
GPU PWR and GND



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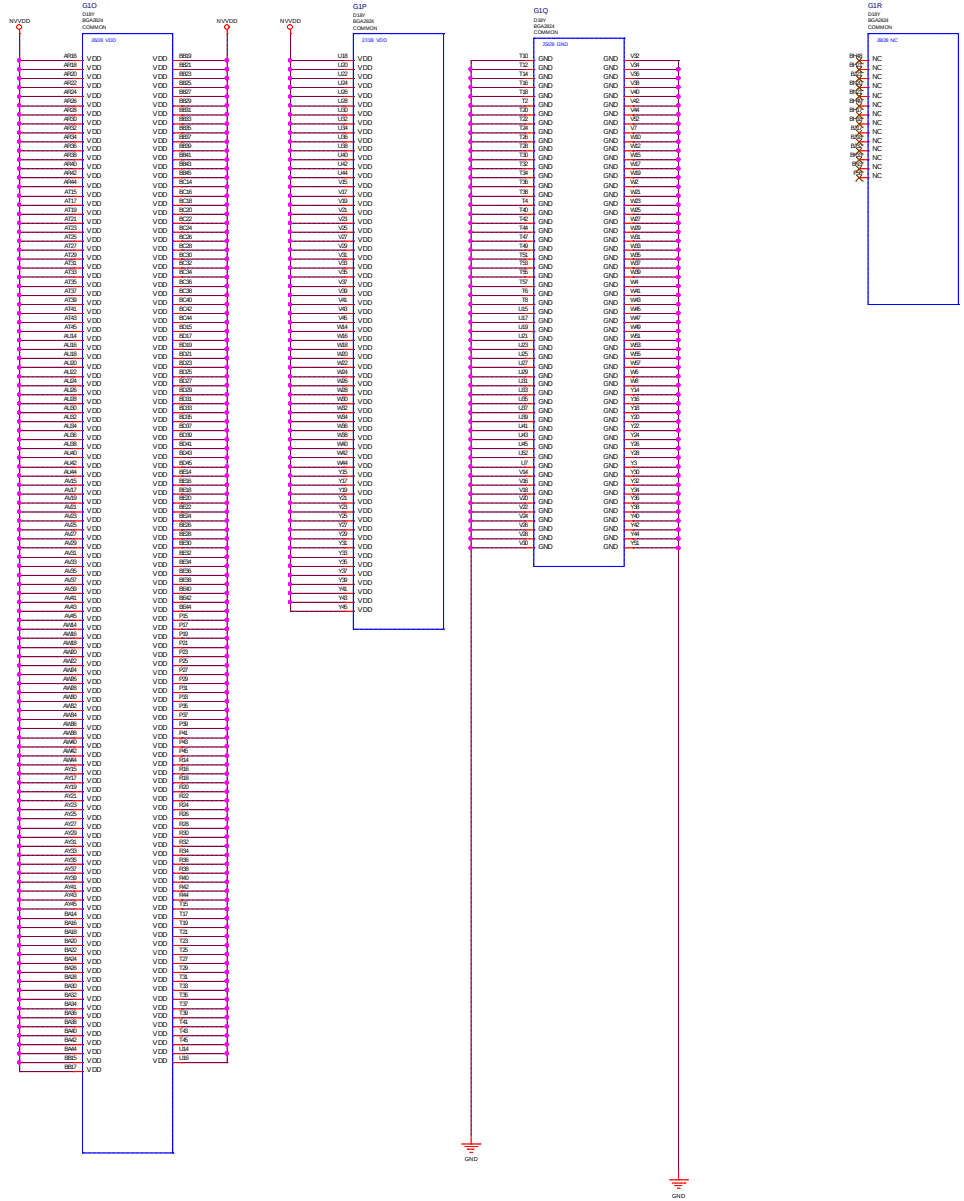
GPU PWR GND NCs



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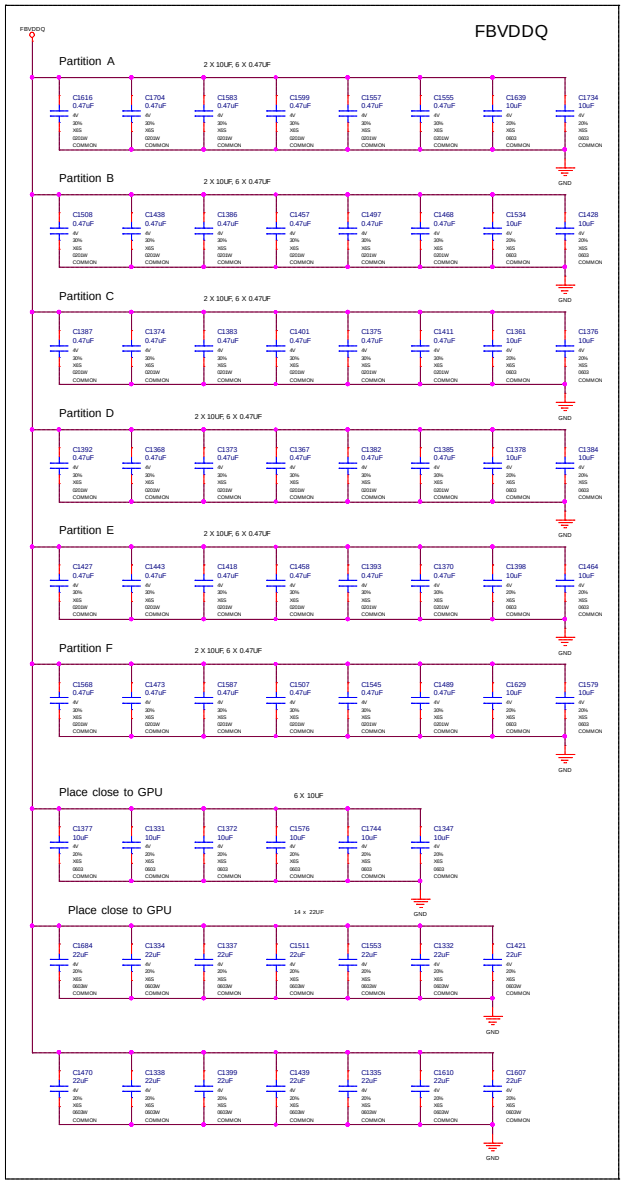
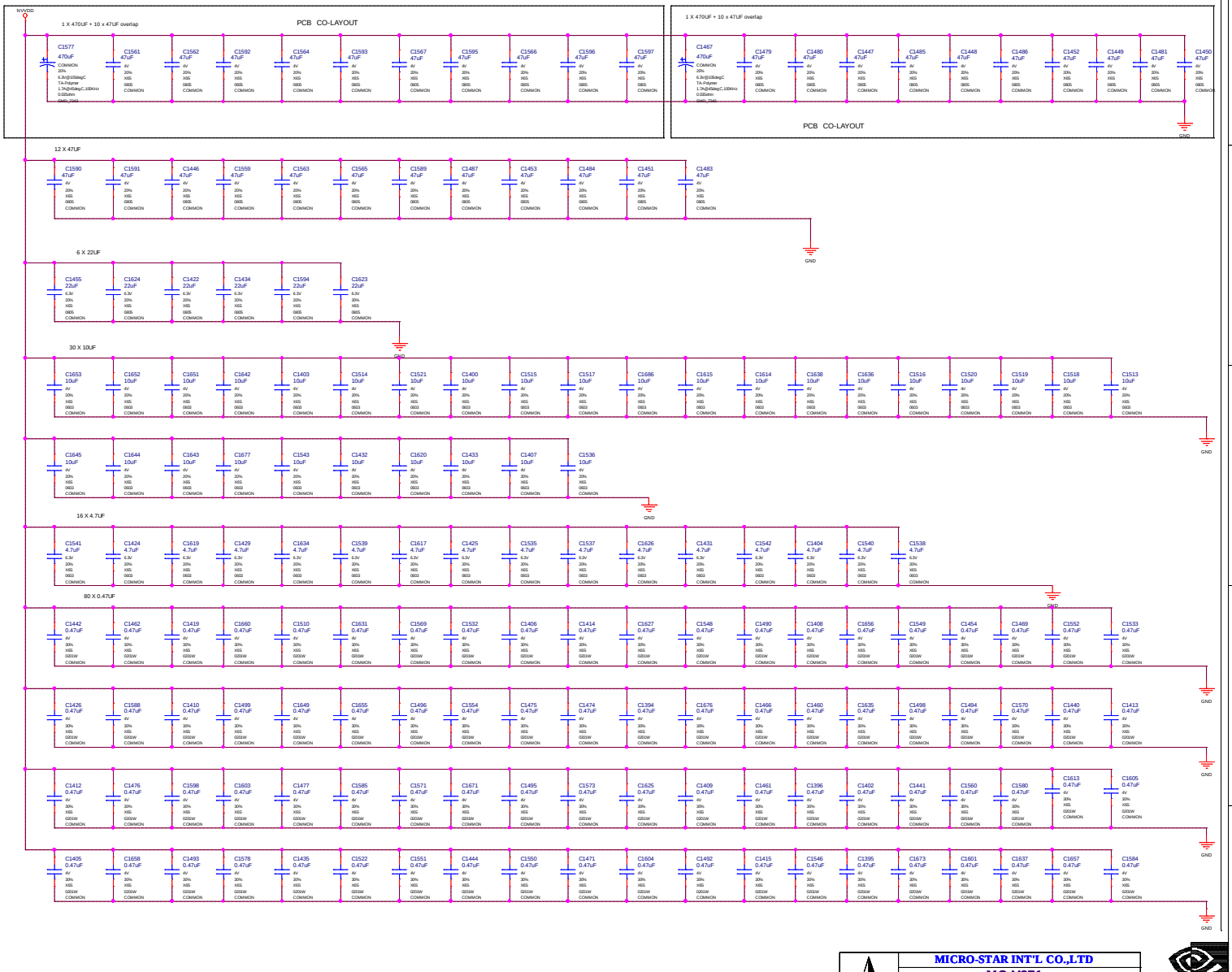
GPU Decoupling

FBVDDQ



NVVDD



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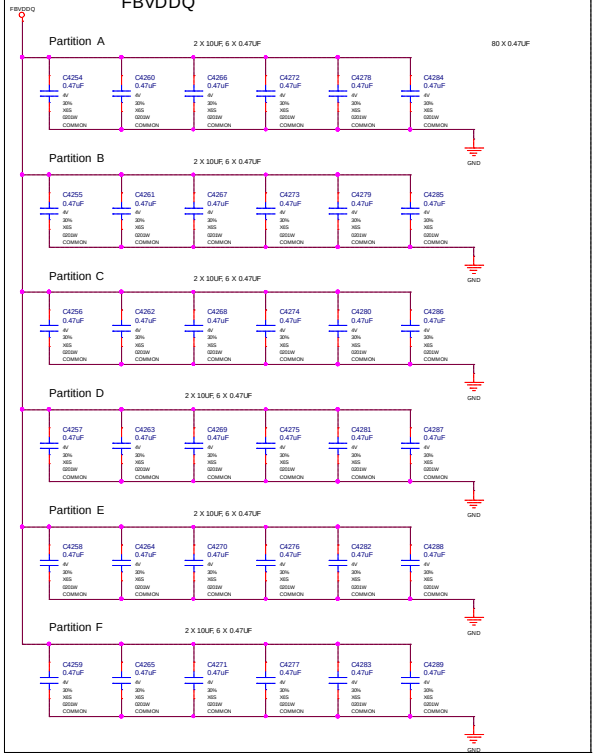
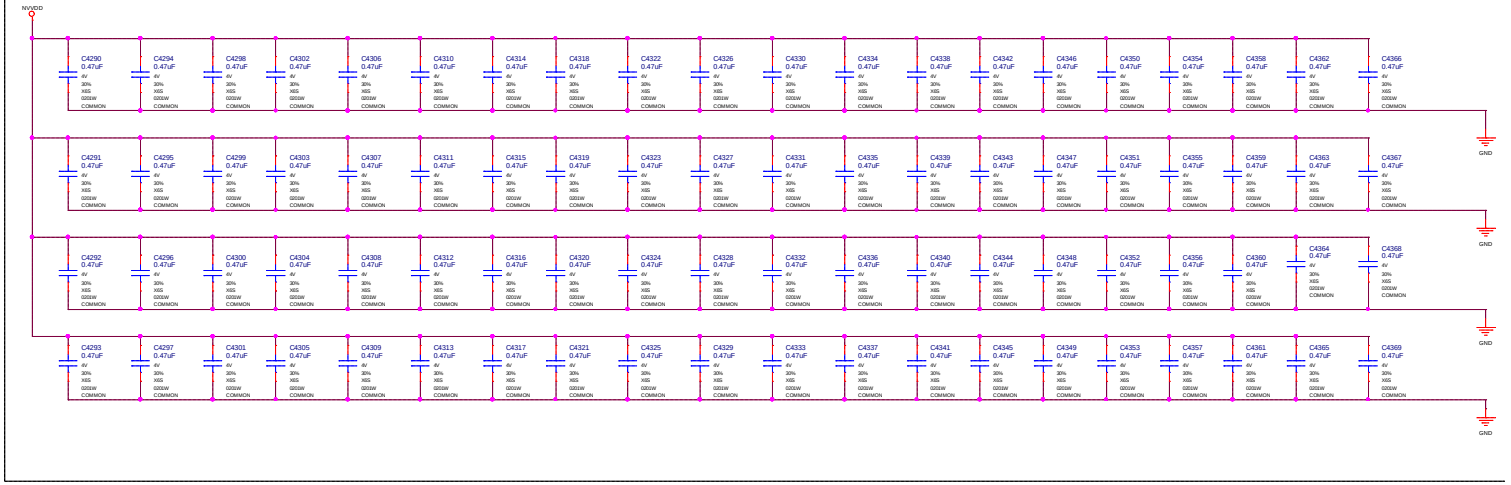
GPU Decoupling

FBVDDQ



NVVDD



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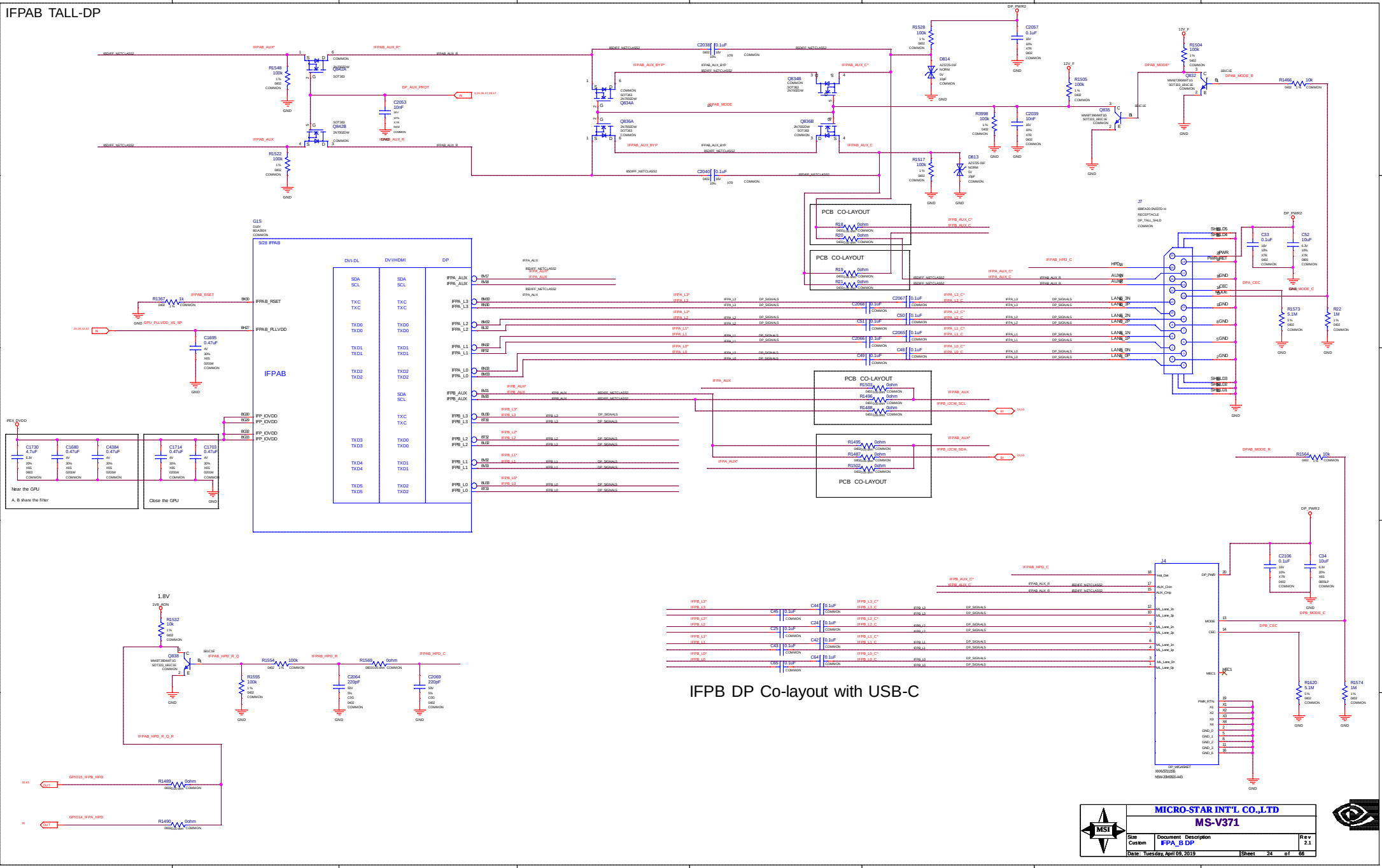
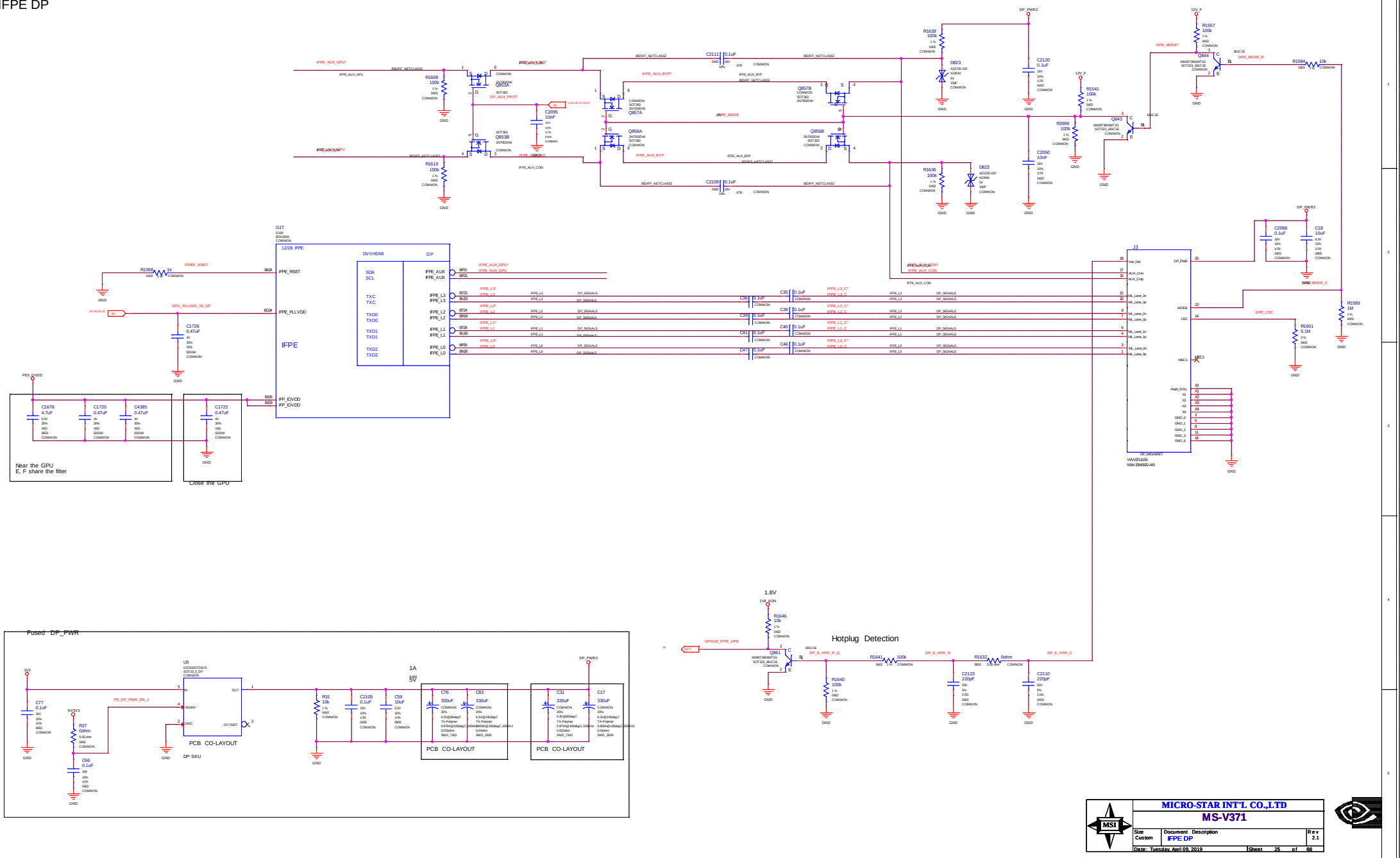
IFPAB TALL-DP



IFPB DP Co-layout with USB-C

IFPE DP


IFPE
12/28 IFPE
DVI/HDMI
DP
Near the GPU
E, F share the filter
Close the GPU
Pused DP_PWR
PCB CO-LAYOUT
DP-SKU
Hotplug Detection
1.8V
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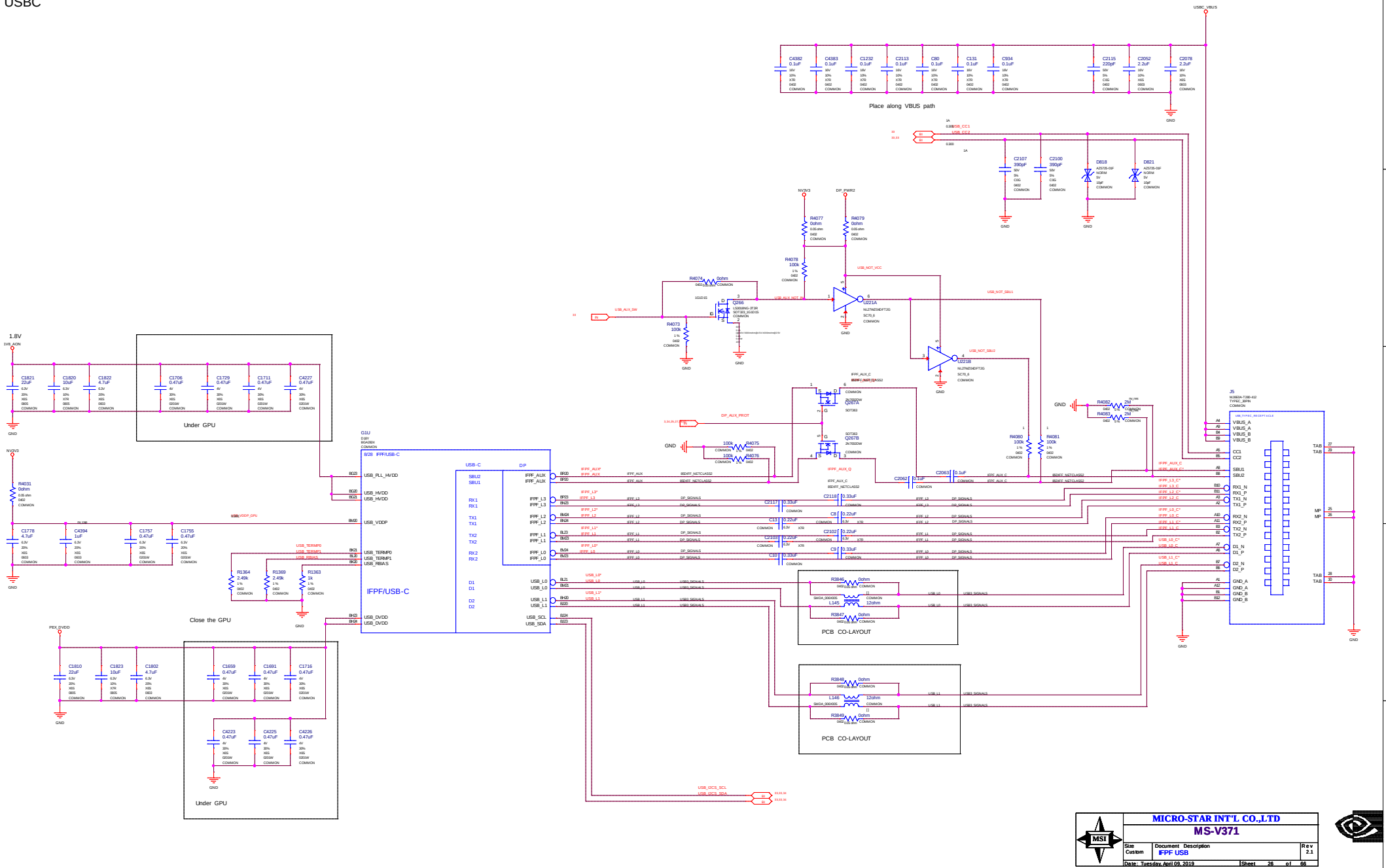
IFPF USBC



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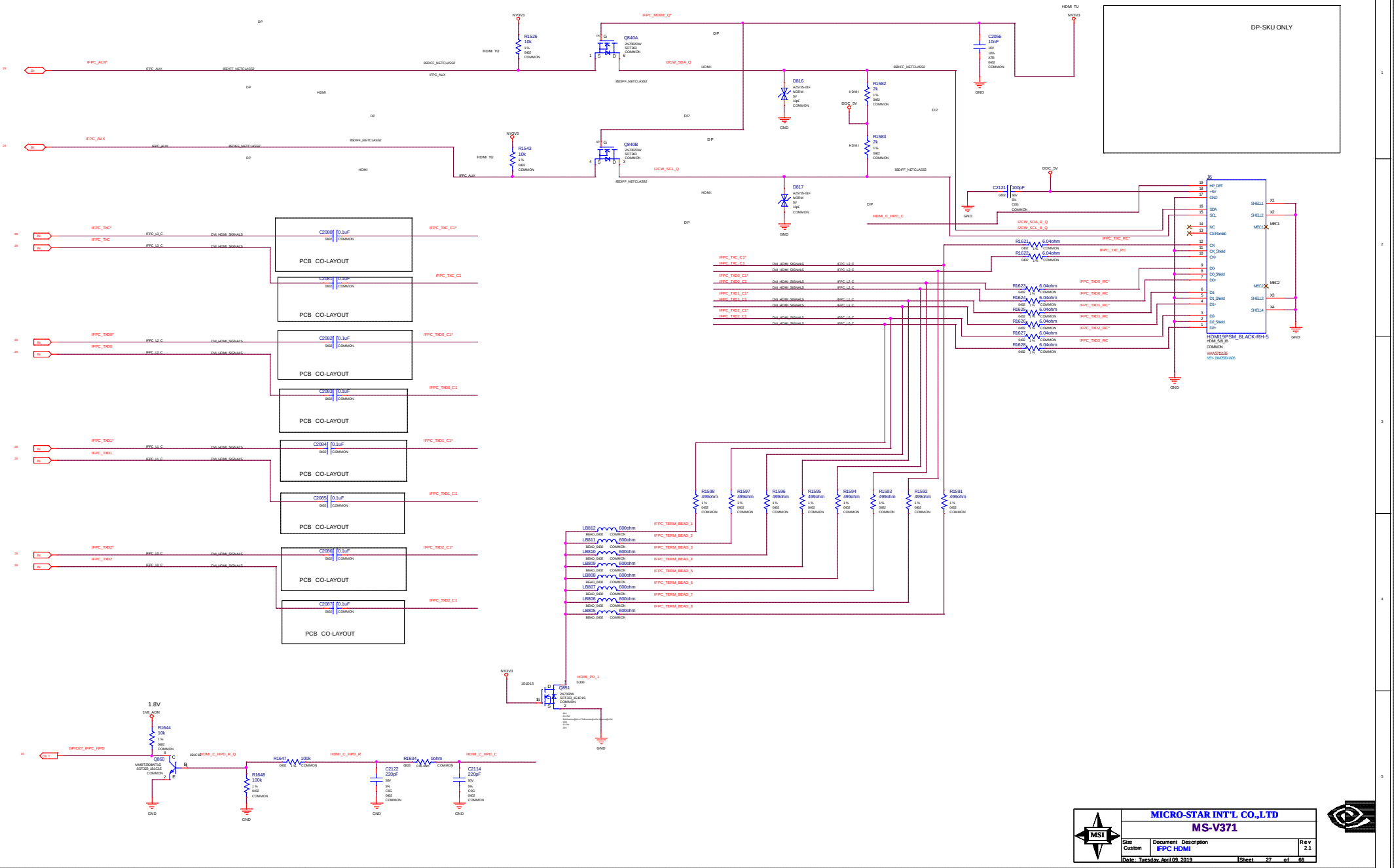
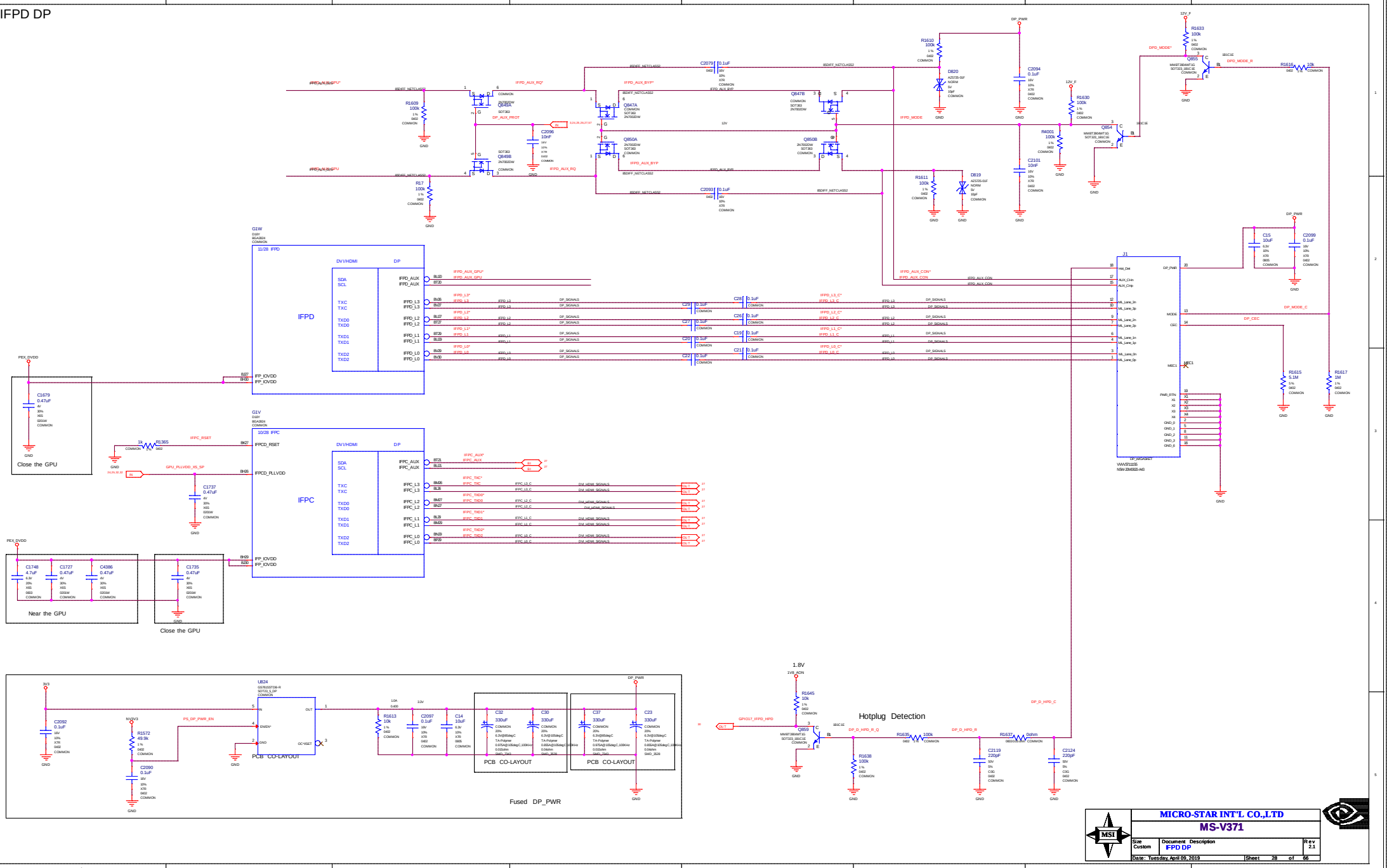
IFPC HDMI 2.0/DP



IFPD DP


IFPD
IFPC
DVI/HDMI
DP
Close the GPU
Near the GPU
Close the GPU
PCB CO-LAYOUT
PCB CO-LAYOUT
PCB CO-LAYOUT
Fused DP_PWR
Hotplug Detection
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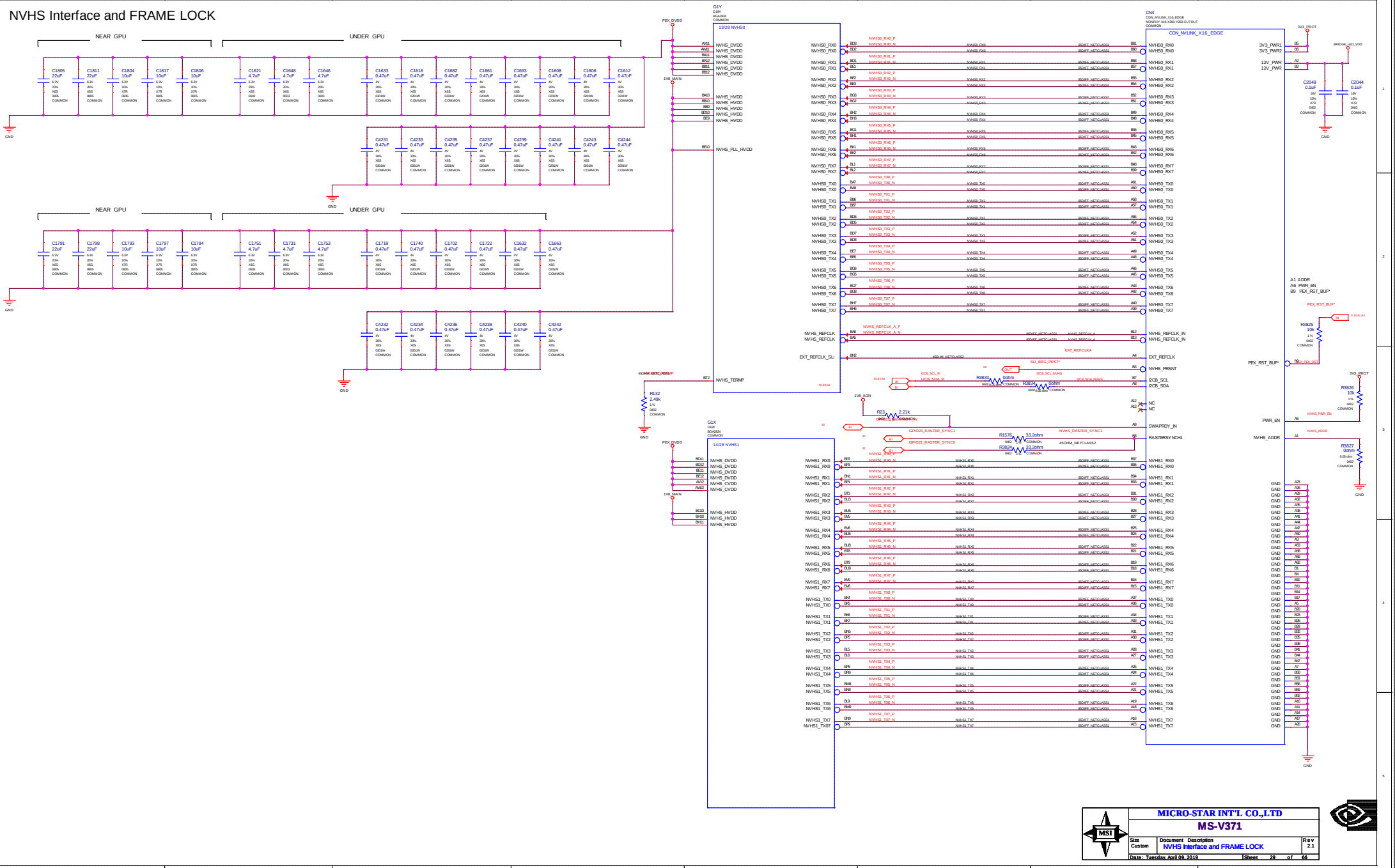
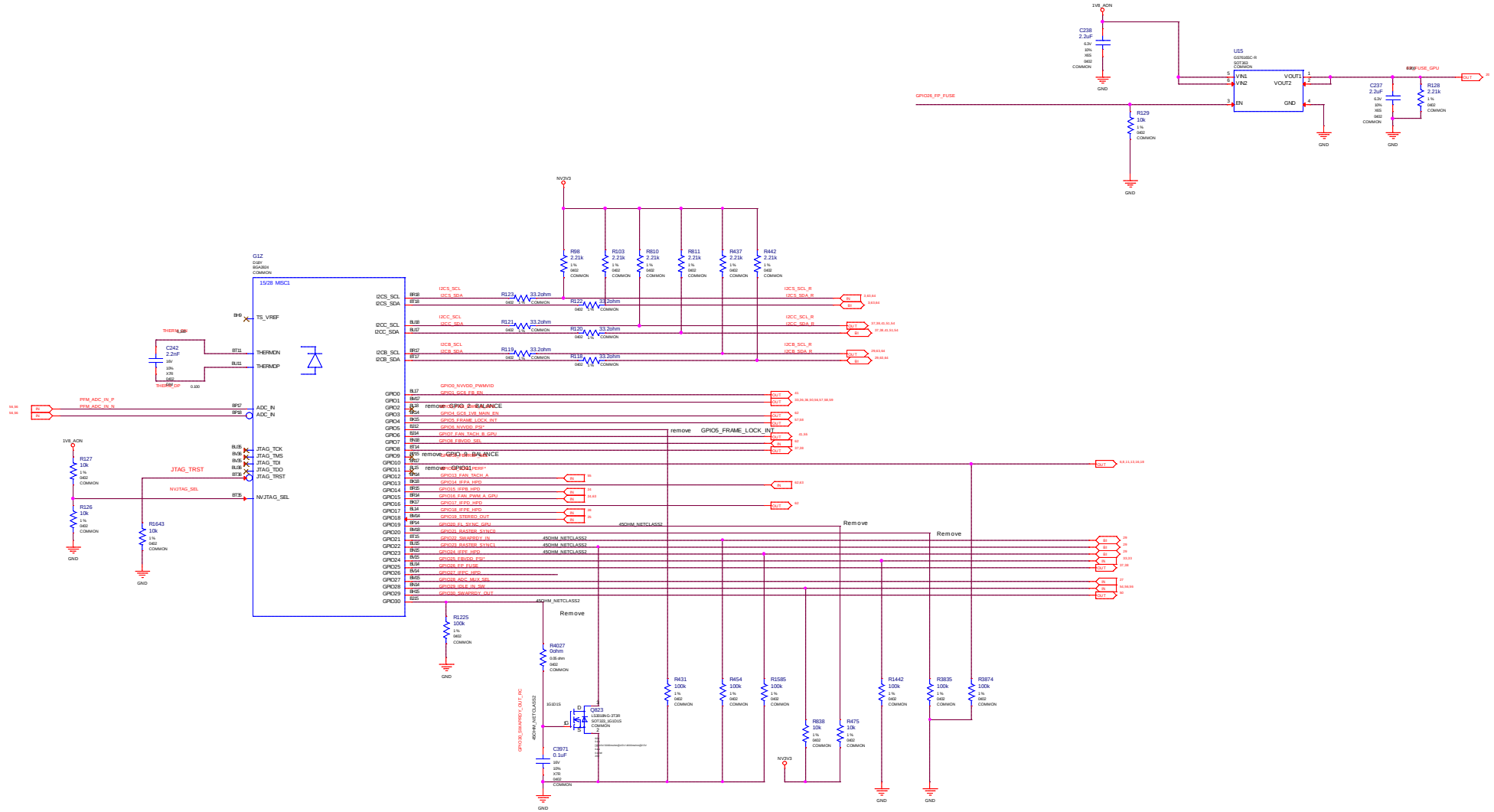
NVHS Interface and FRAME LOCK



MISC1: Fan, Thermal, JTAG, GPIO, STEREO



MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	
L	L	H	00001	DEFAULT
L	H	L	00010	
L	H	H	00011	
H	L	L	00100	
H	L	H	00101	
H	H	L	00110	
H	H	H	00111	
L	L	M	01000	
L	M	L	01001	

H=High :Tied to 1.8V

M=Middle:Tied to 0.9V

L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	H	XXX0	FS_OVERT DISABLE	

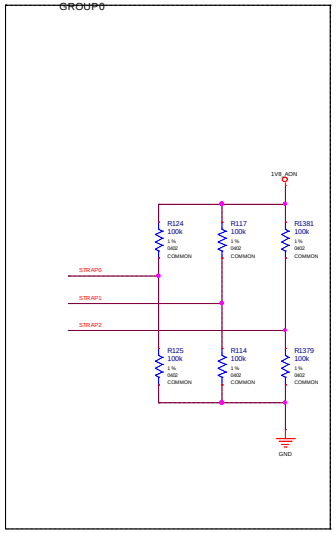
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	SKU 200

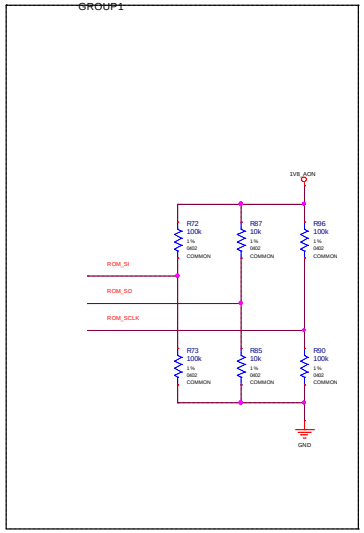
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

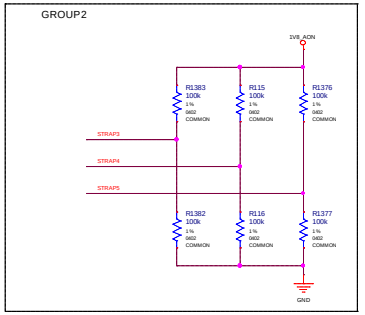
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

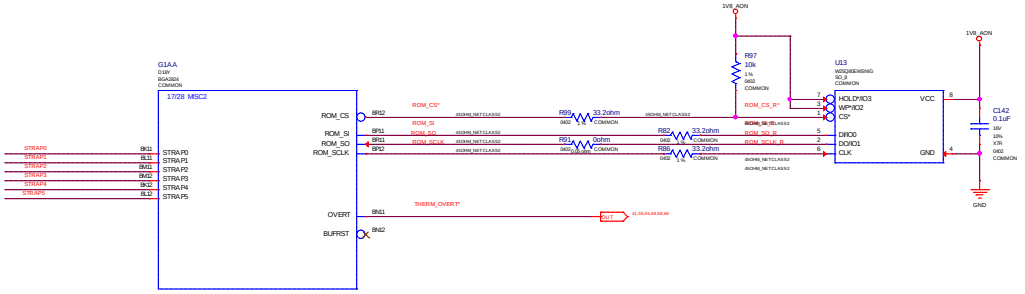
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE









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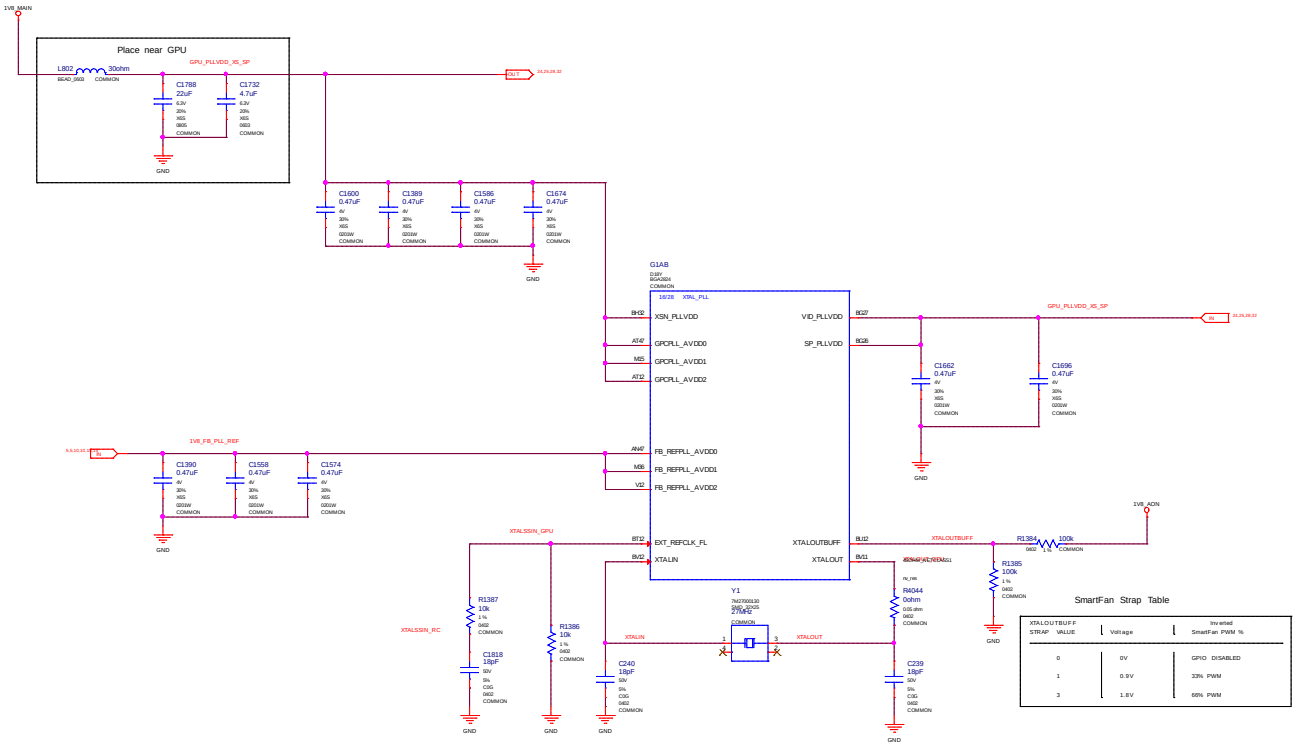
MISC2: XTAL. PLL



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MISC: USB PPC

PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN

U820 CYPD4136-24LQXIT QFN24 COMMON

CYPD4136 ANX3411 ANX3411 CYPD4136

VDD_IO M_SDA | VDDD INTP_OUT | VCCD M_SCL | V5V TEST_S | P3_2/ SCB3_I2C_SDA HPD | P3_3/ SCB3_I2C_SCL CFG_SDA | P1_1 SOURCE_CTL | P1_3 RESET | P1_5 TEST_EN | P1_7 VBUS_OCP | P2_5 AVDD33 | P3_0 DVDD_IO | P3_1 DISCHARG_CTL | P3_4 CFG_SCL | P3_6 SINK_CTL

AVDD33 | ROLE_SELECT | CC1 | I2C_ADR_1/ GPIO | GPIO1 | CC2 | VCONN_POWER | VBUS_SENSE | DVDD_IO | GND

CC1 | CC2 | P2_3/ | HPD_DETECT | P1_2 | P2_6 | P0_0/ SCB0_I2C_SDA | P0_1 SCB0_I2C_SCL | XRES | GND | GND

USB_DVDD_IO ANX

PCB CO-LAYOUT

UART RXD DEBUG PORT

Place it closed to 5V regulator

MICRO-STAR INT'L CO.,LTD

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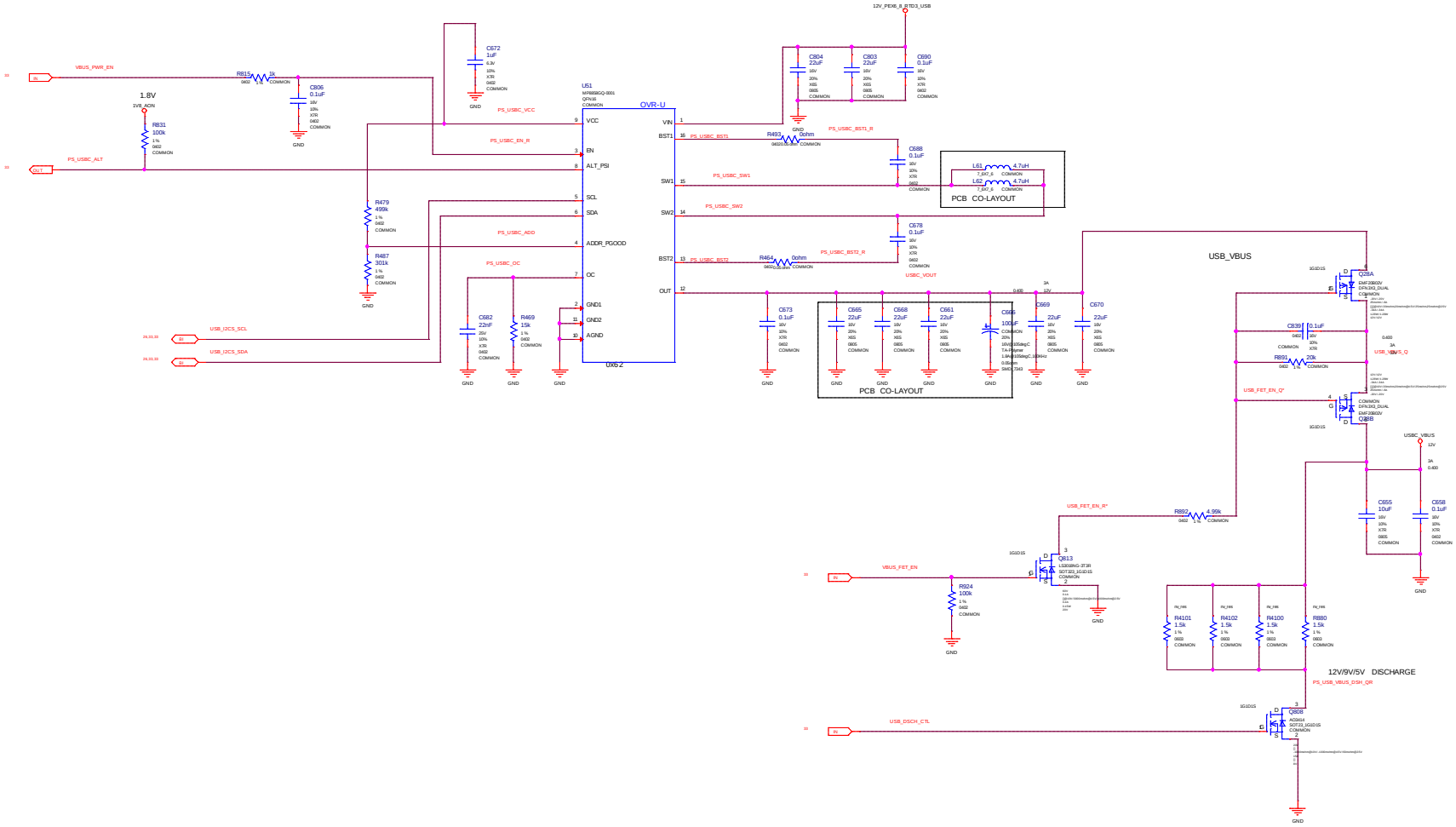
PS: USB VR



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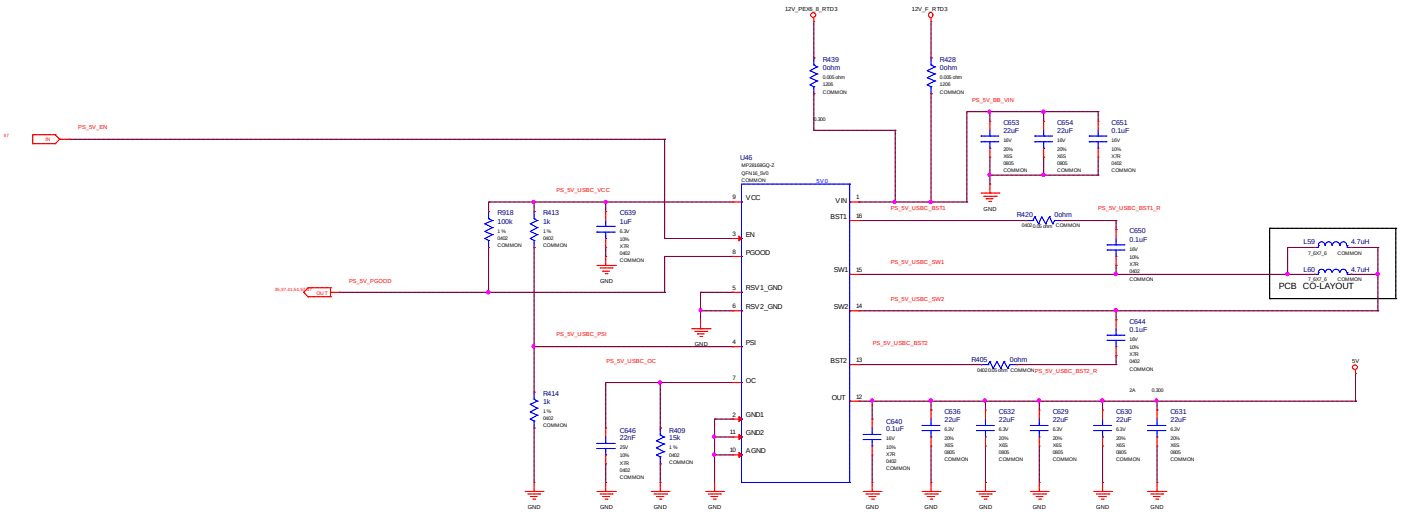
PS: 5V, 5V_BACKUP



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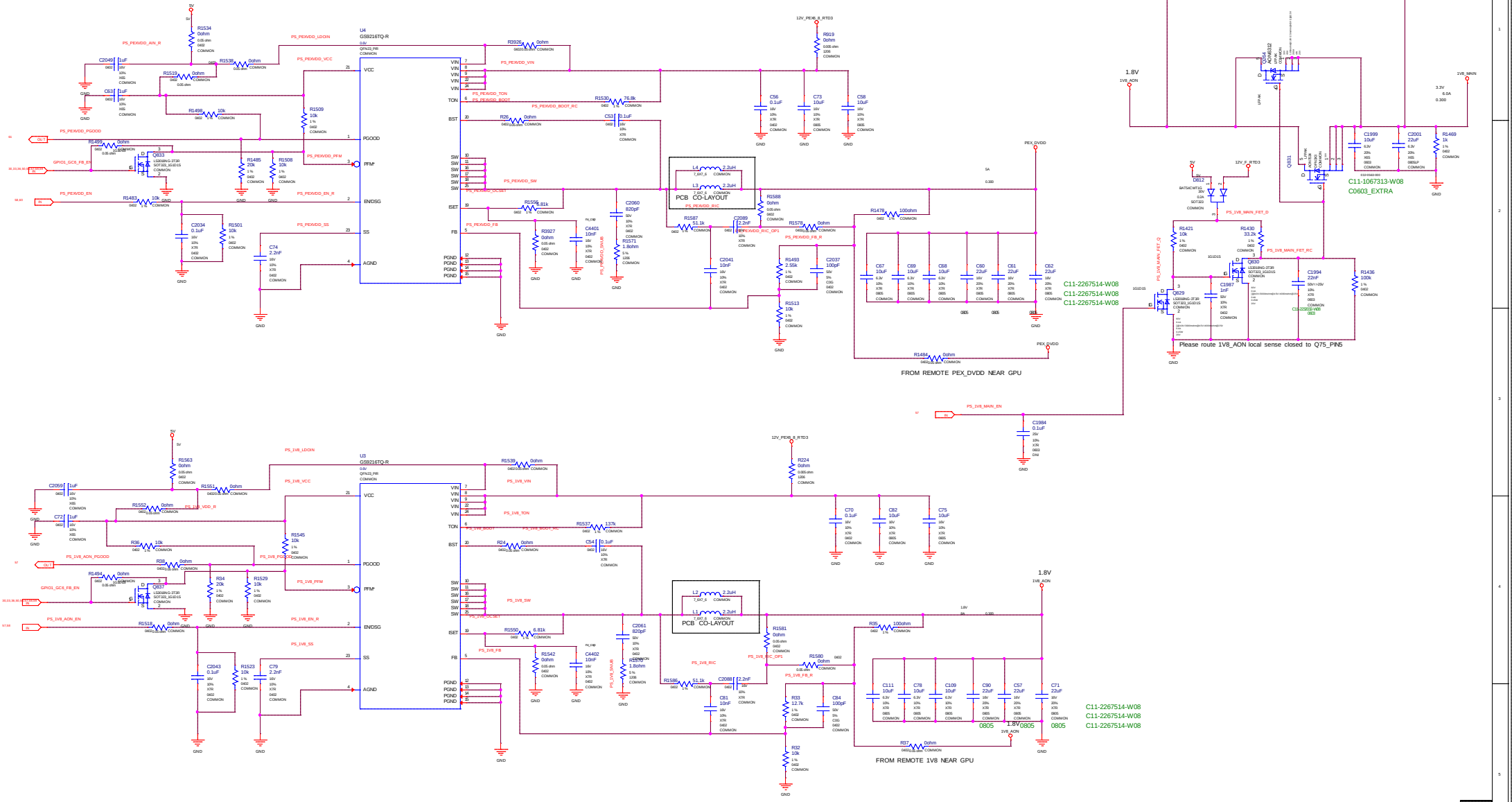
PS: PEXVDD 1V8 Rail



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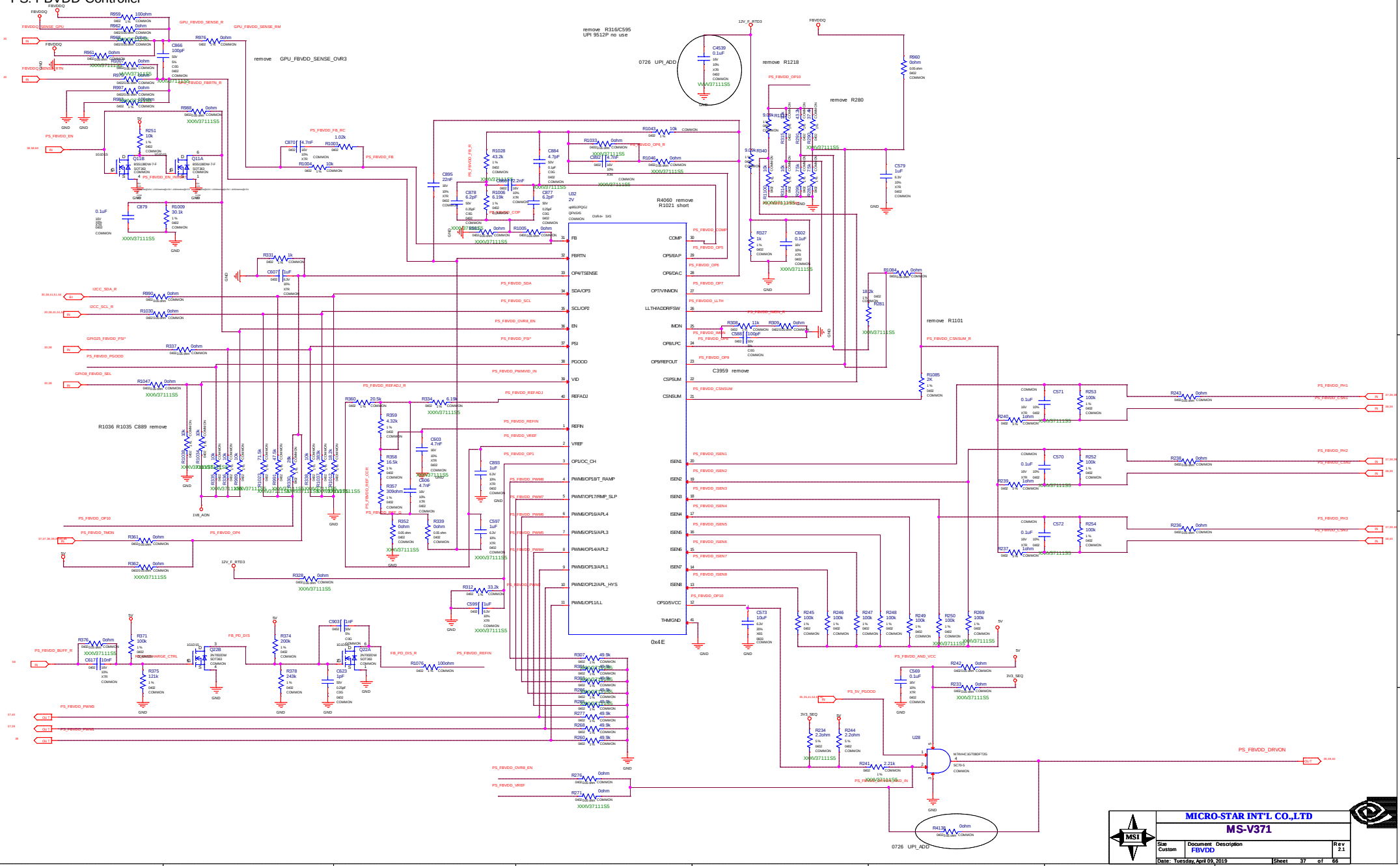
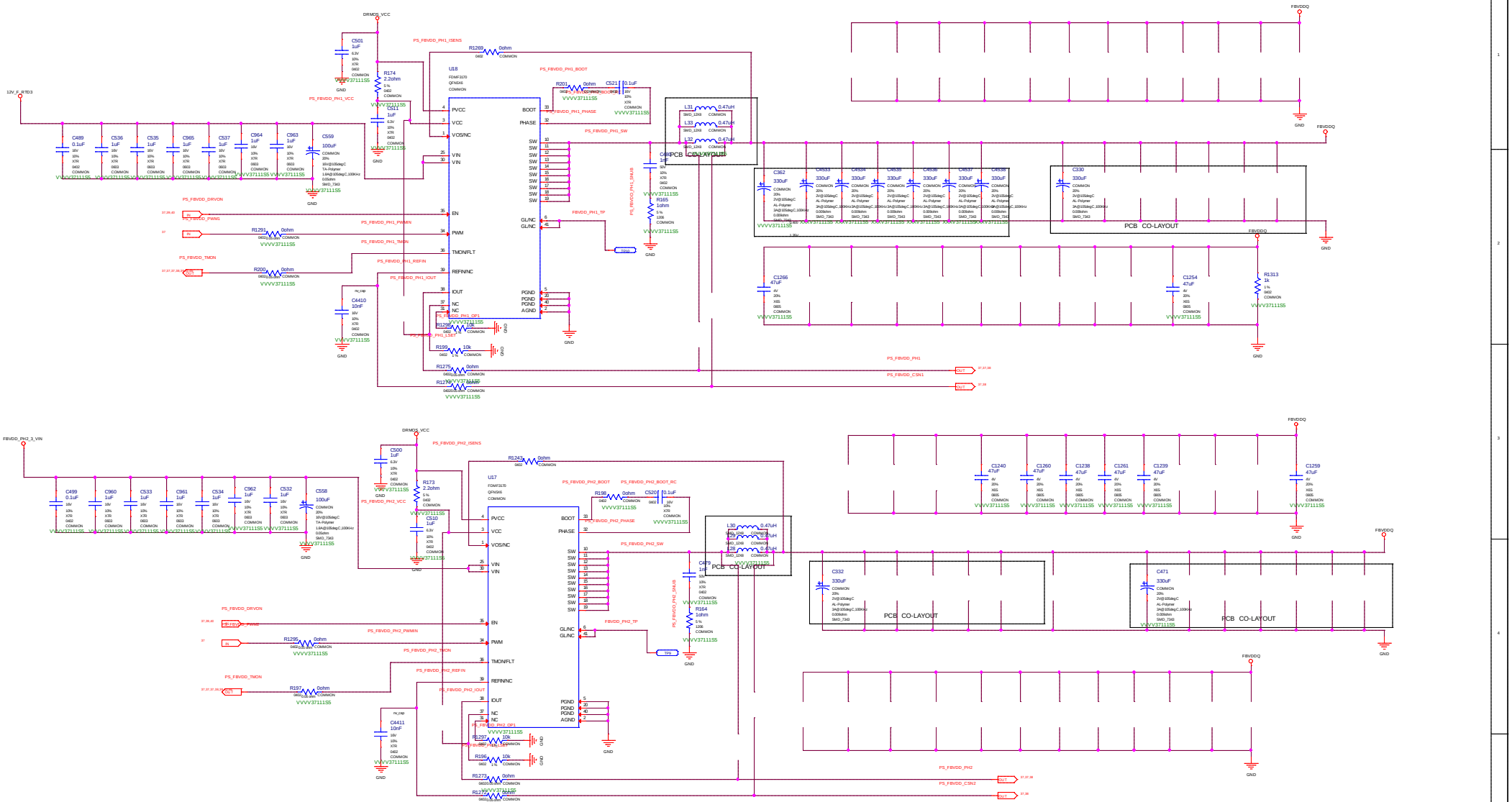
PS: FBVDD Controller



PS: FBVDD Controller OVR3

remove FBVDDQ

PS: FBVDD PH1, 2



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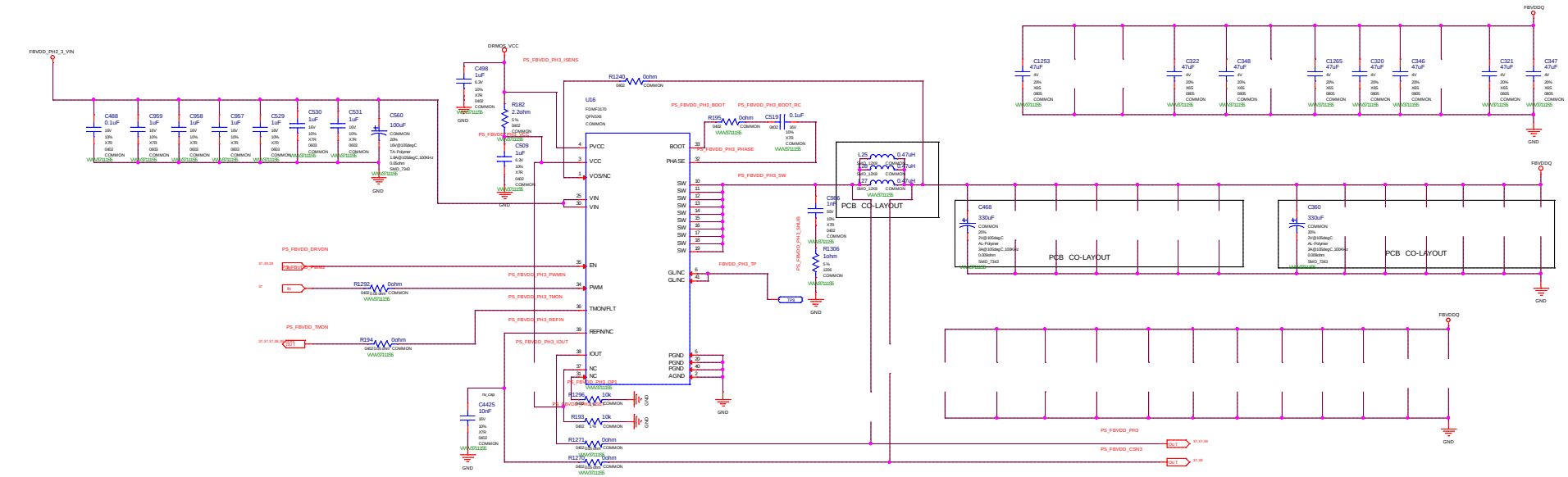
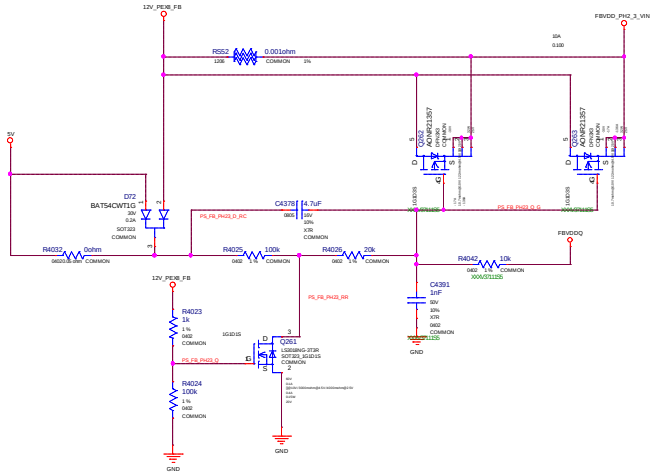
PS: FBVDD PH3





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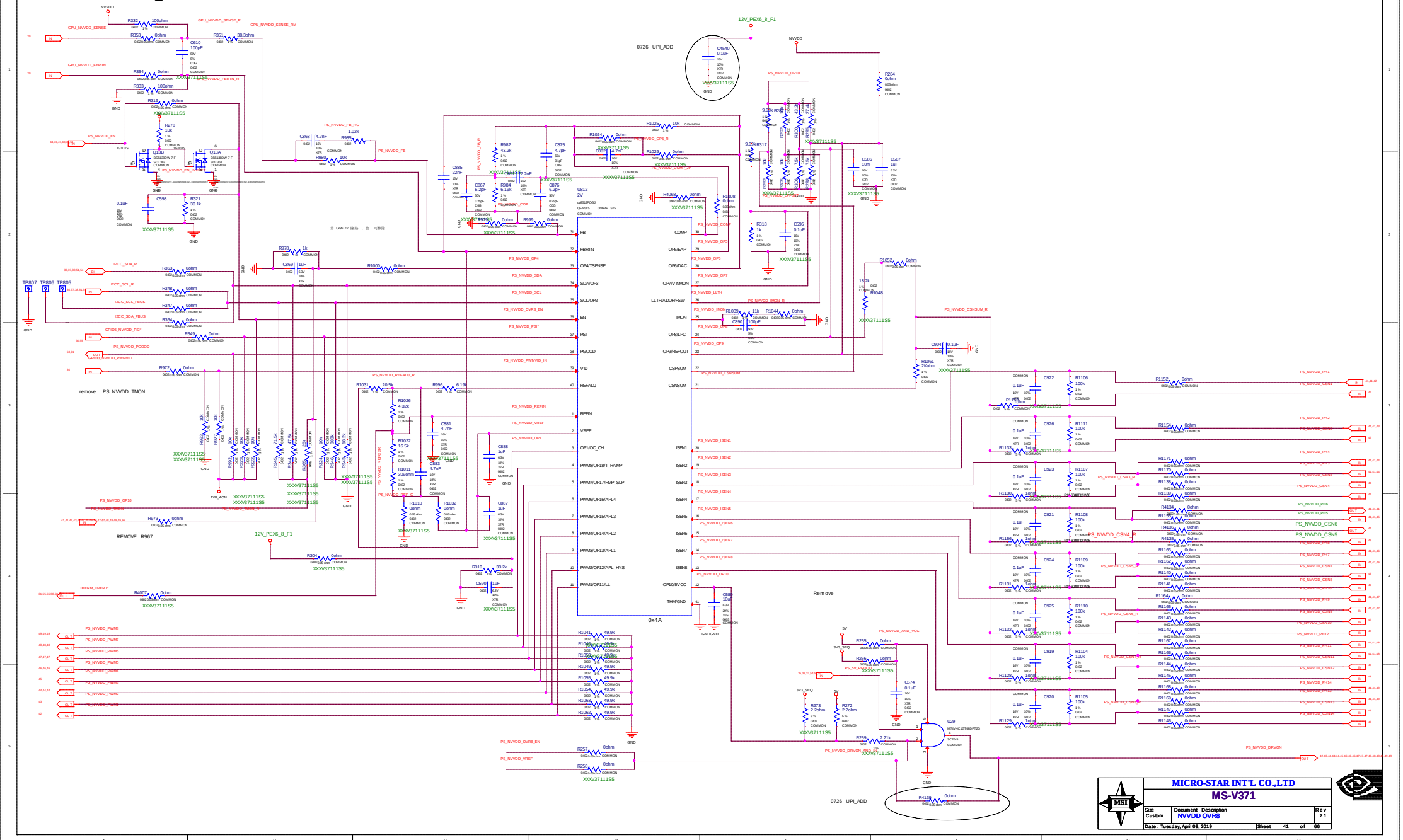
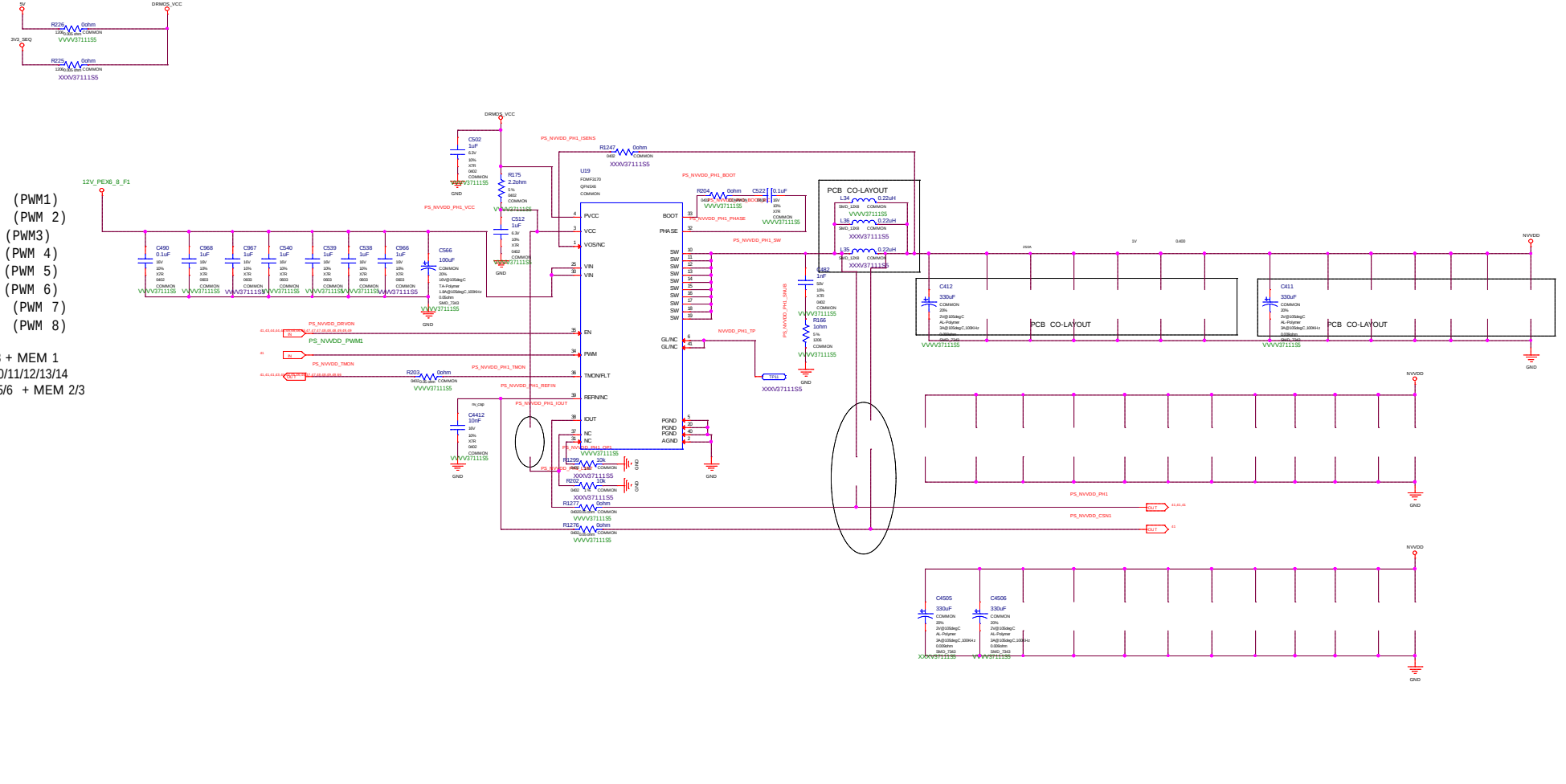
PS: NVVDD Controller_OVR8



PS: NVVDD Phase 1

1	F1	(PWM1)
2	F2	(PWM 2)
3/4	F2	(PWM3)
5/6	F2	(PWM 4)
7/8	12V_F	(PWM 5)
9/10	F1	(PWM 6)
11/12	F1	(PWM 7)
13/14	F1	(PWM 8)

12V_F NVVDD 7/8 + MEM 1
F1 NVVDD-1/9/10/11/12/13/14
F2 NVVDD-2/3/4/5/6 + MEM 2/3



Remove PS_NVVDD_TSENSE_PTC

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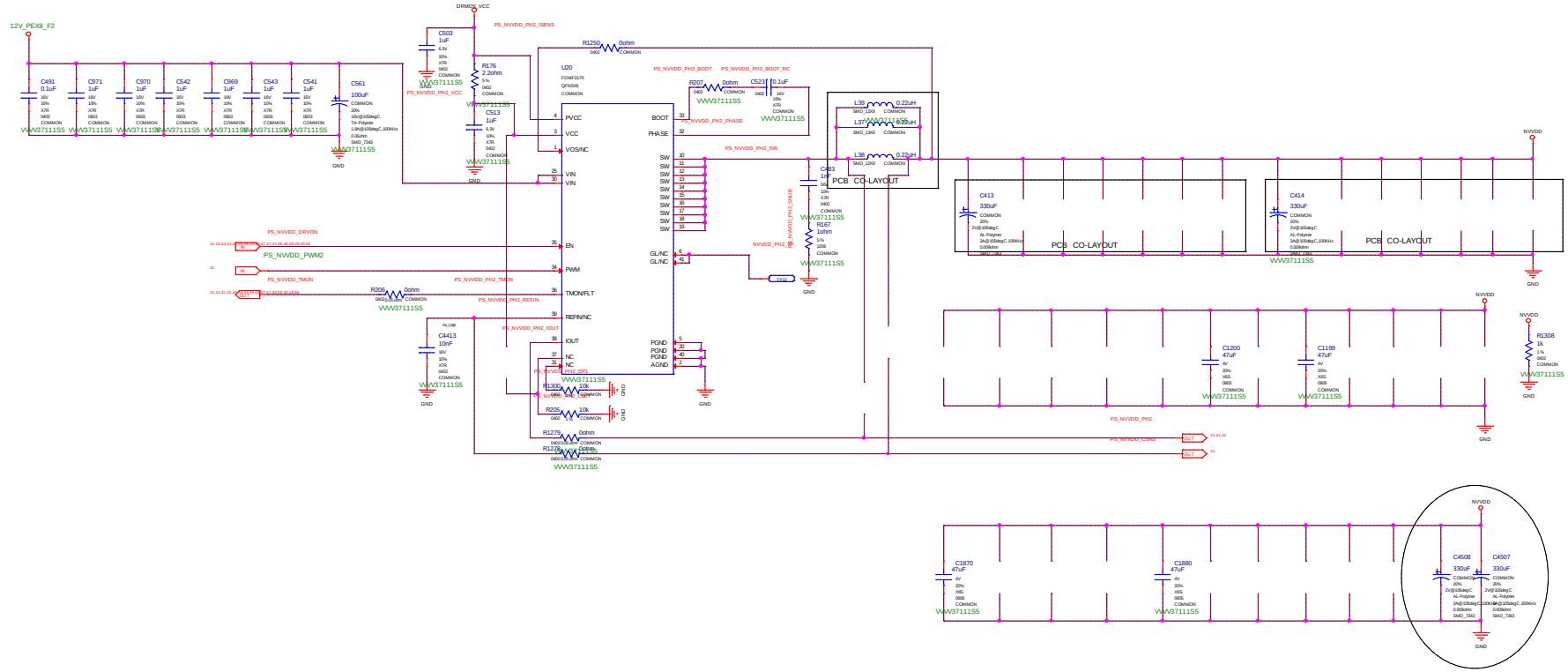
PS: NVVDD Phase 2



MICRO-STAR INT'L CO.,LTD		
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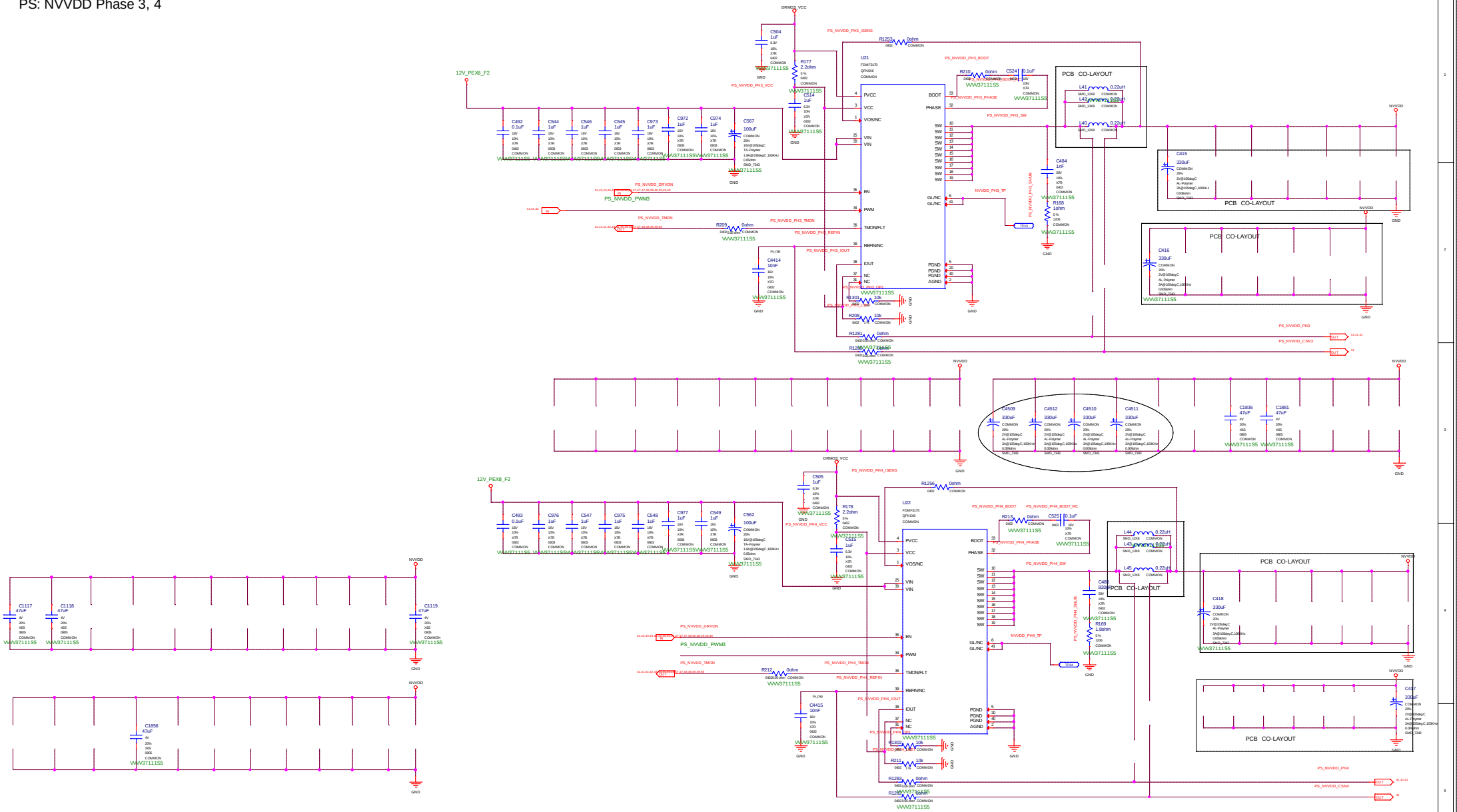
PS: NVVDD Phase 3, 4



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Size: Custom	Document Description: NVVDD PH3/4
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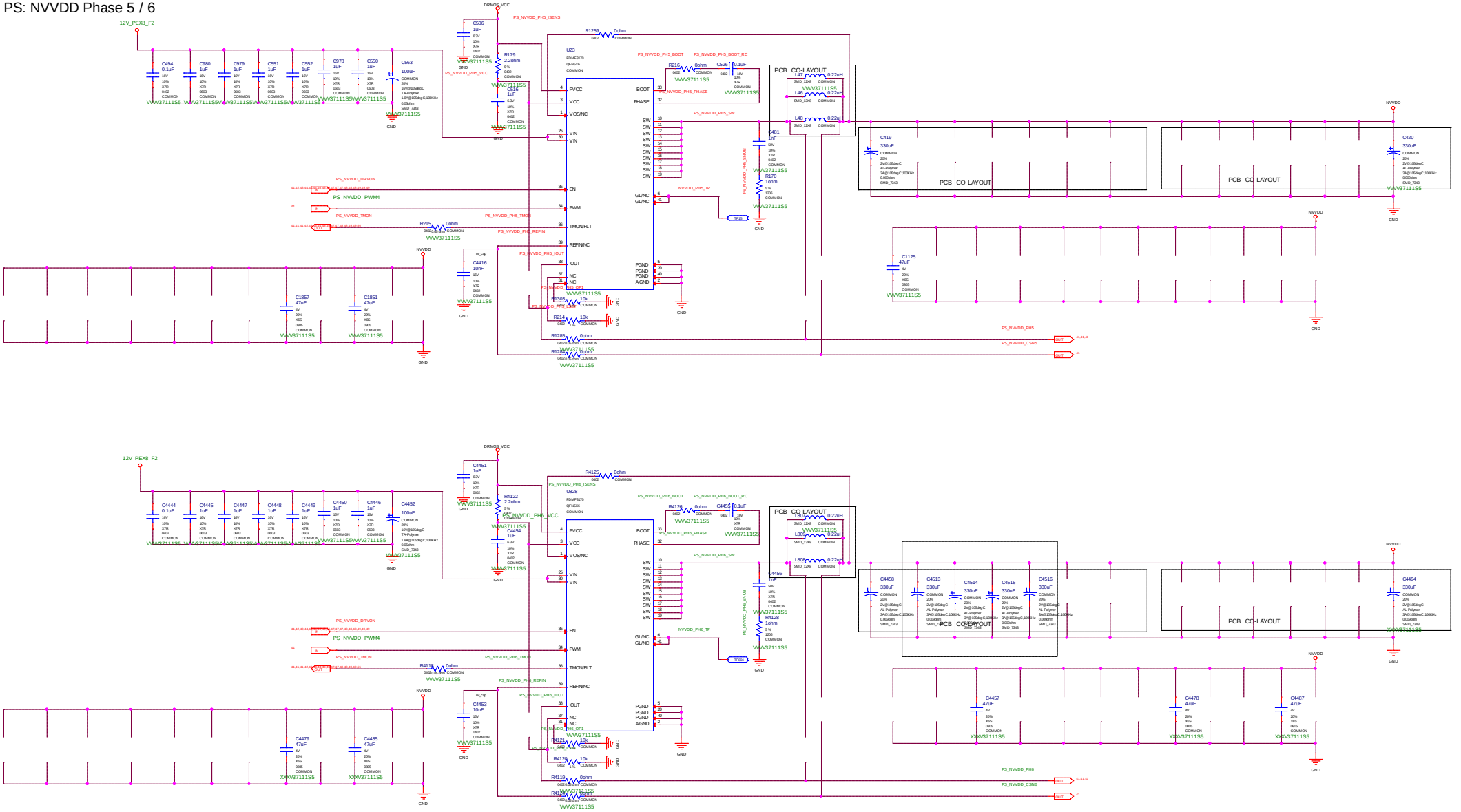
PS: NVVDD Phase 5 / 6



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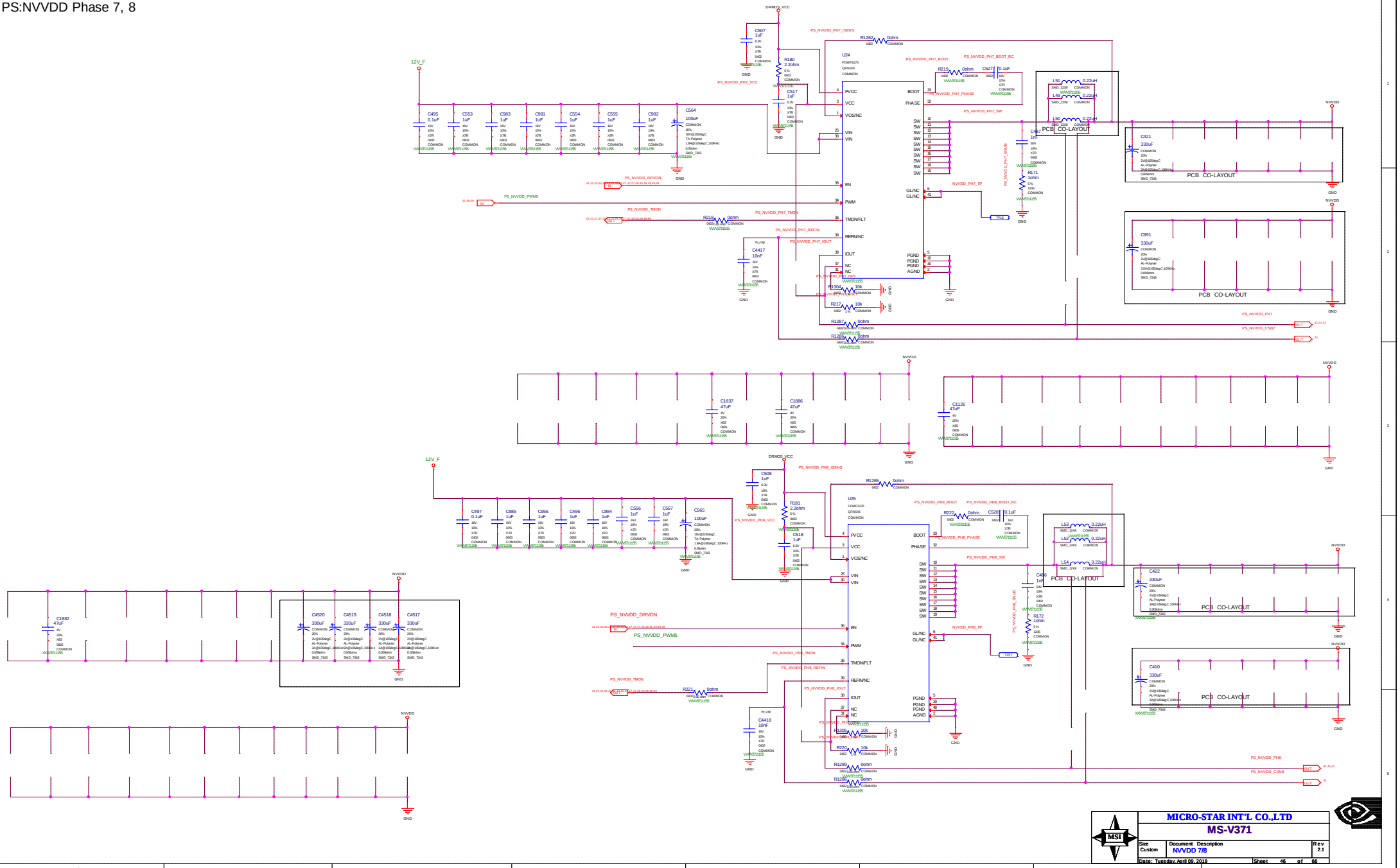
PS:NVVDD Phase 7, 8



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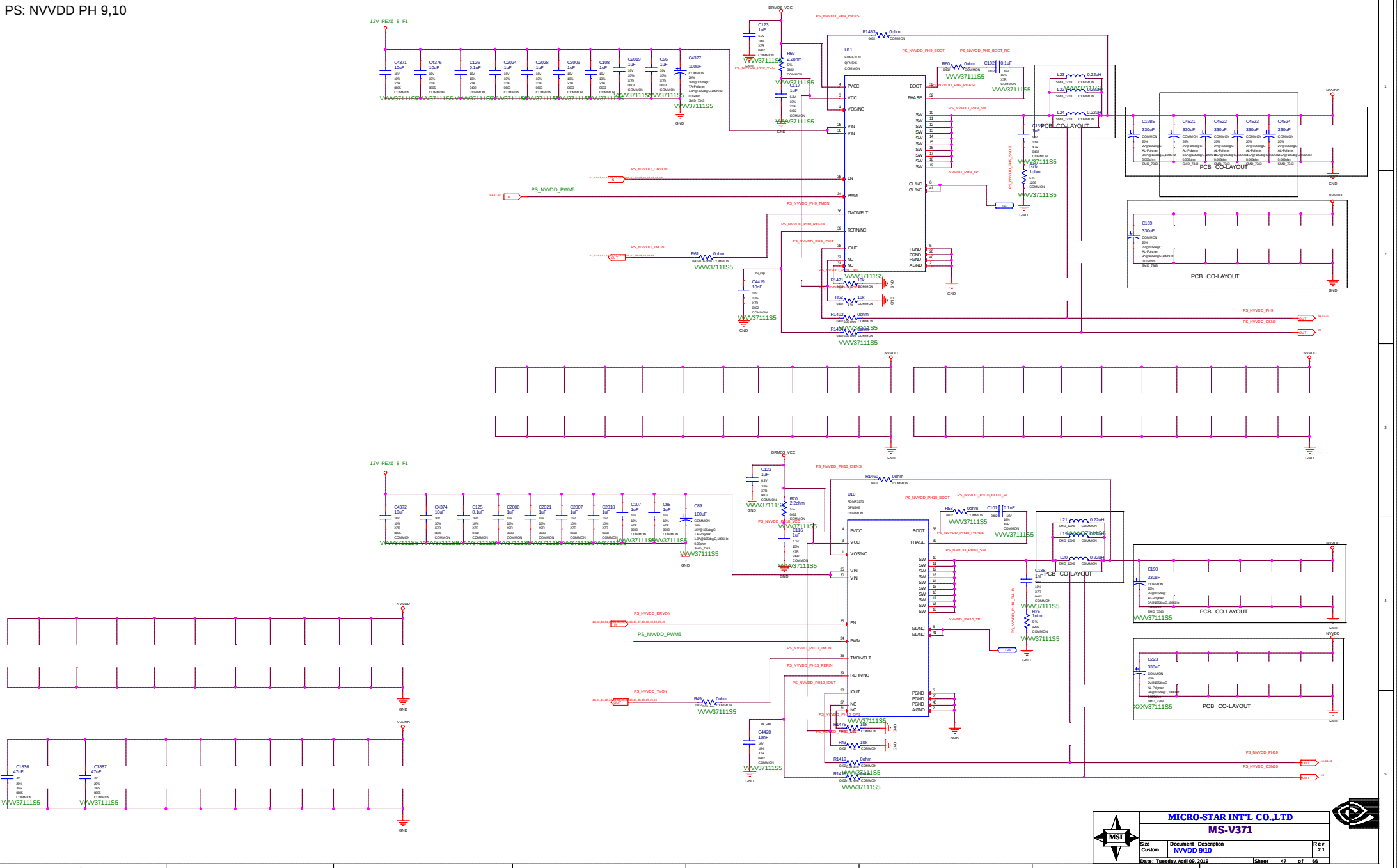
PS: NVVDD PH 9,10



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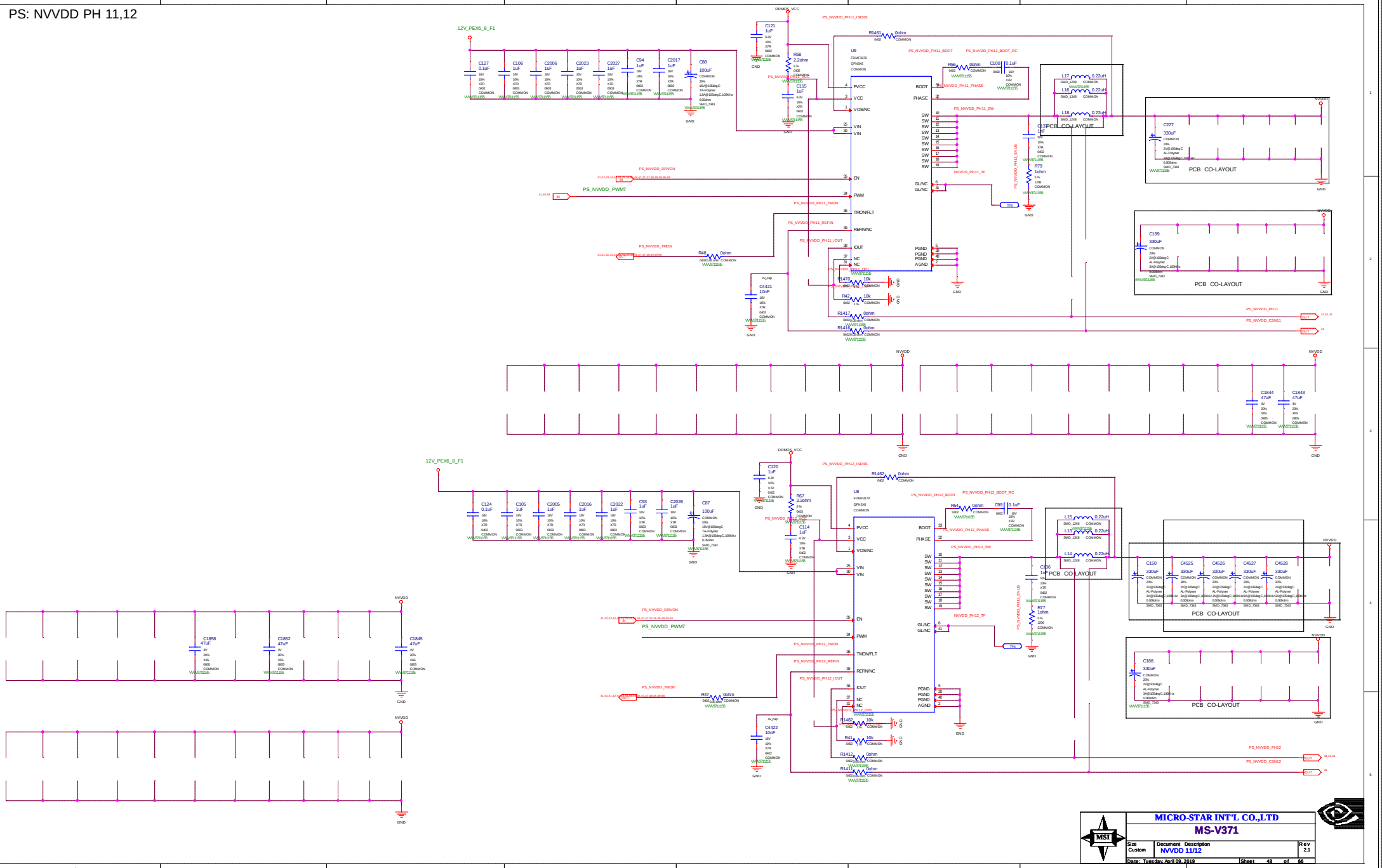
PS: NVVDD PH 11,12



MICRO-STAR INT'L CO.,LTD

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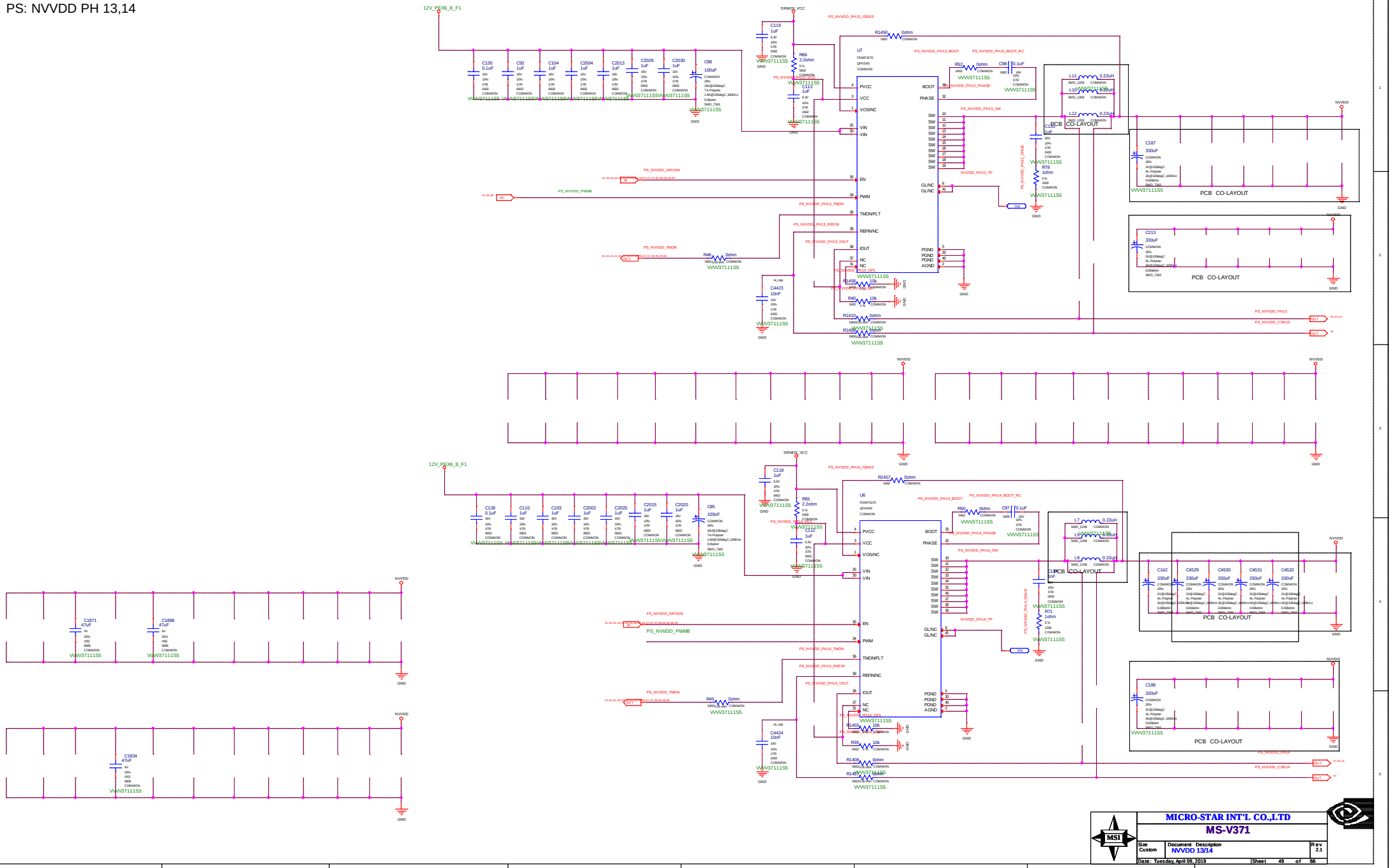
PS: NVVDD PH 13,14



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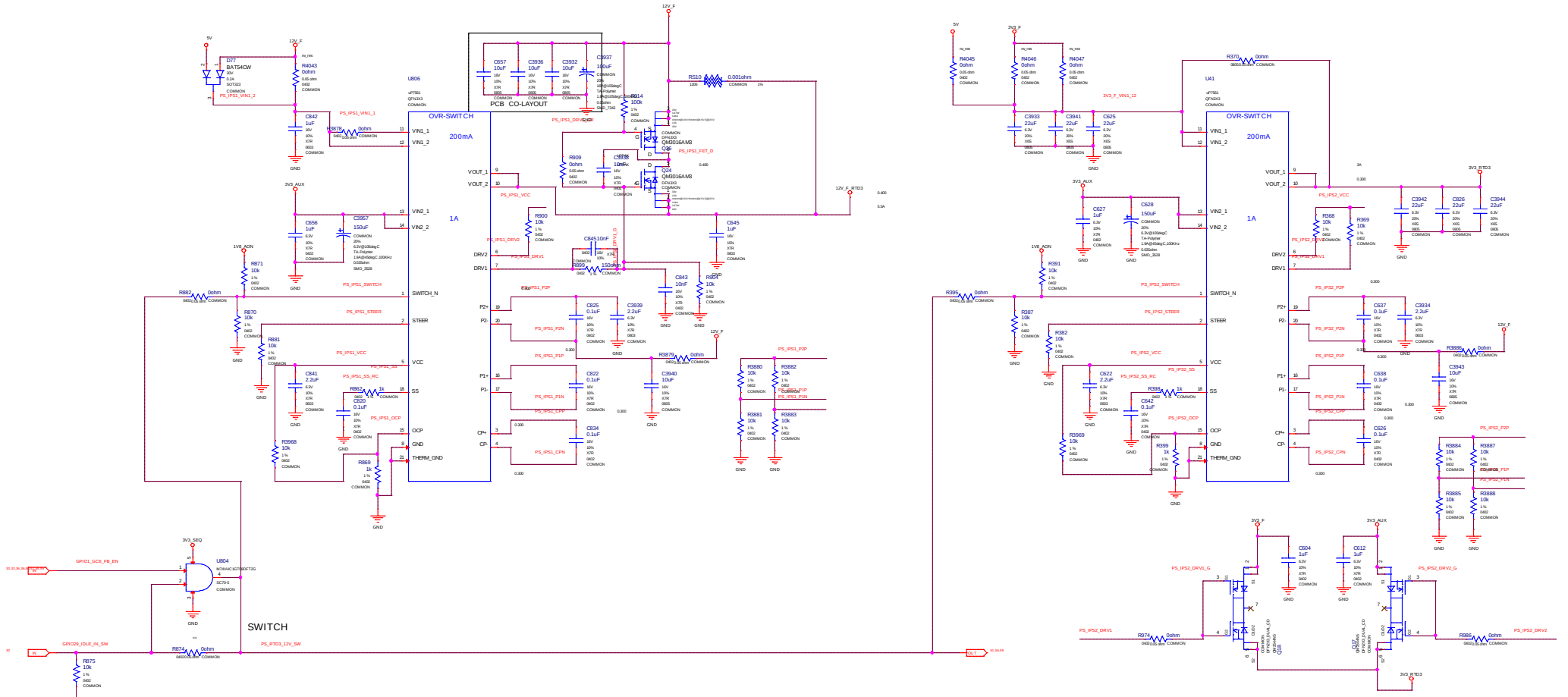
PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



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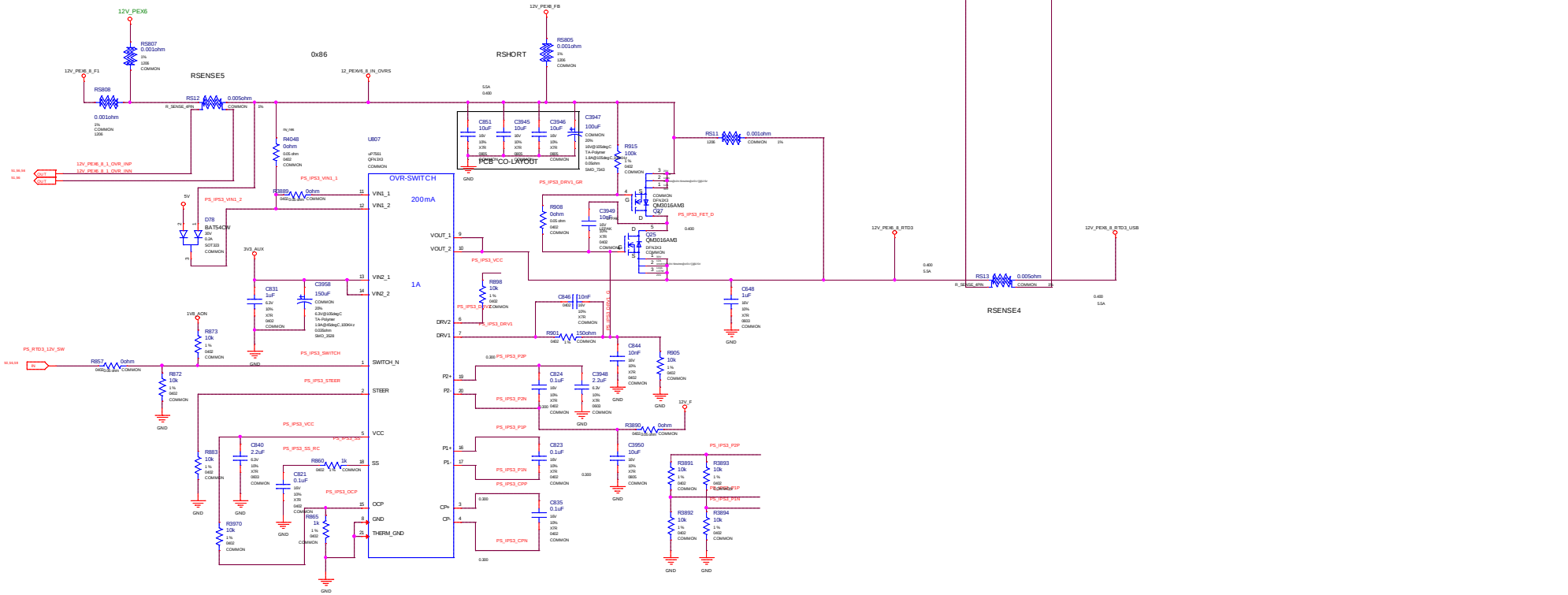

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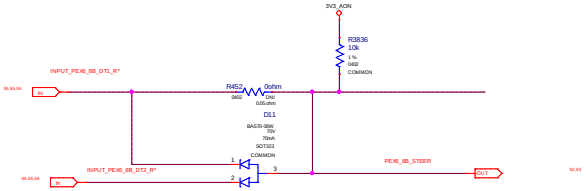
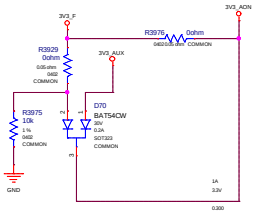
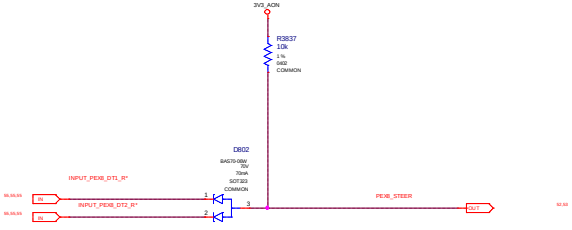
PS: Input Switch Rail Balance







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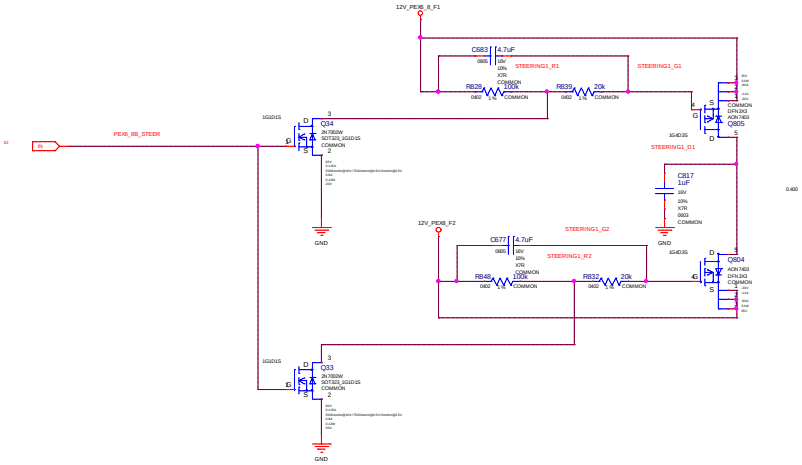
12V CURRENT STEERING (UNDER POWER BOOT):

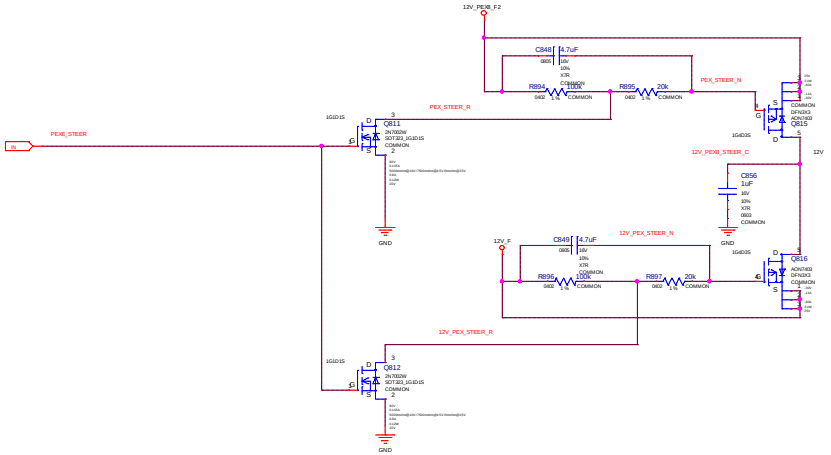
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA

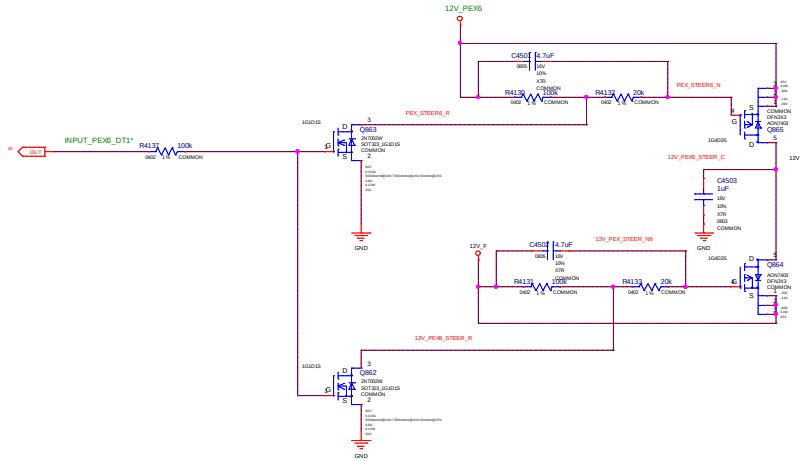


12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode





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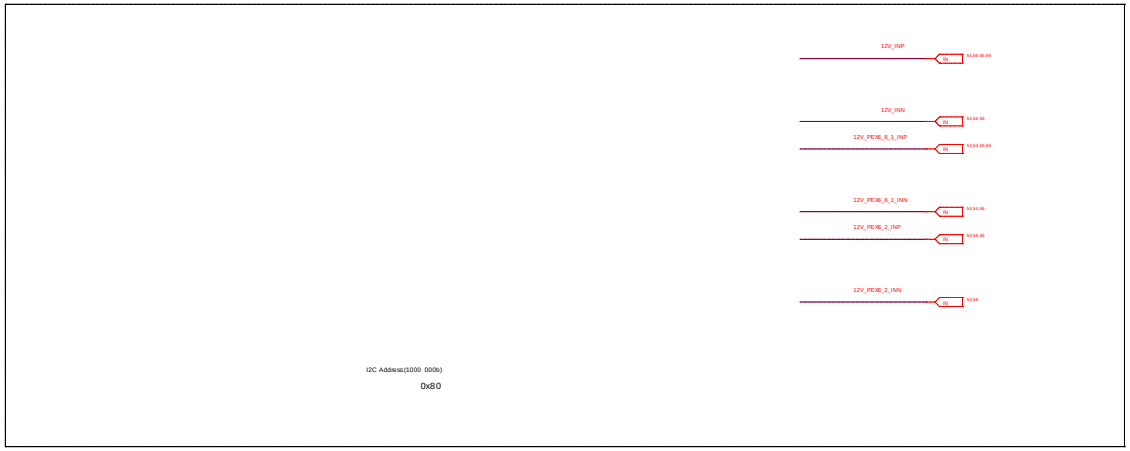
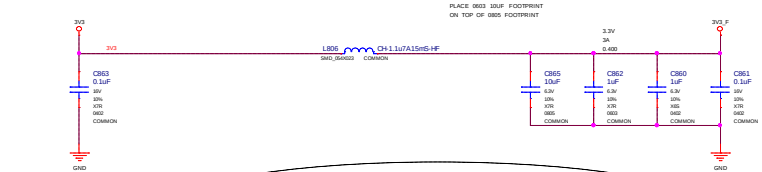
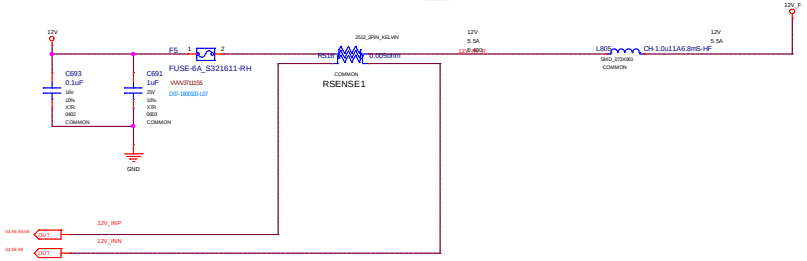
PS: Inputs, Filtering, and Monitoring

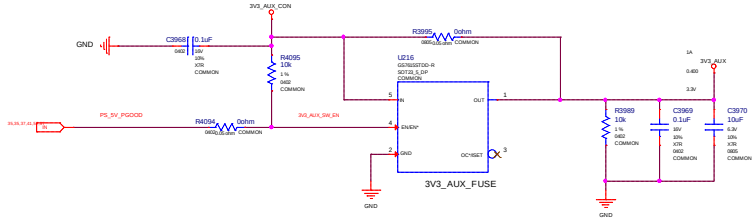


PEX 3V3 INPUT - 10W

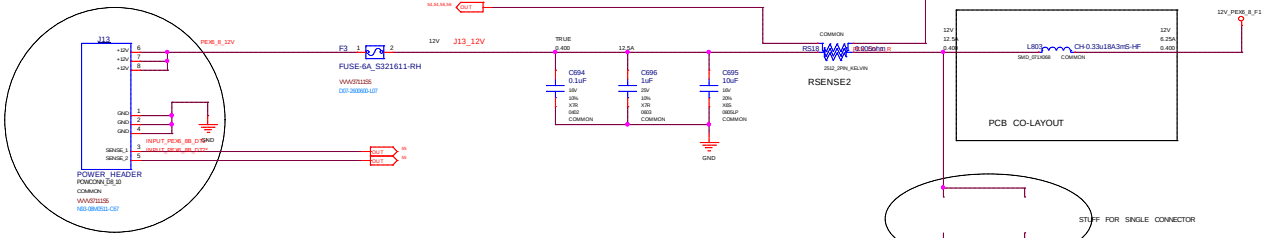


PEX_12V INPUT - 66W

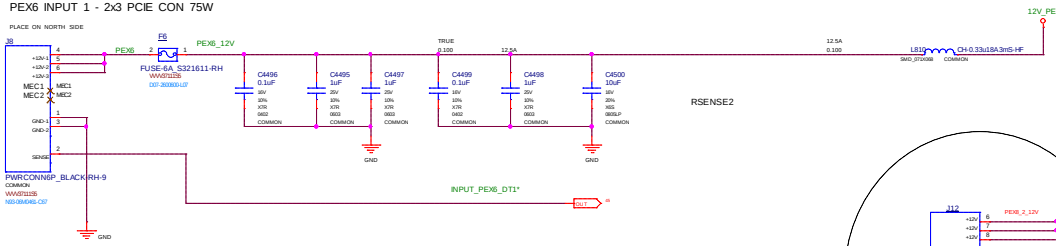




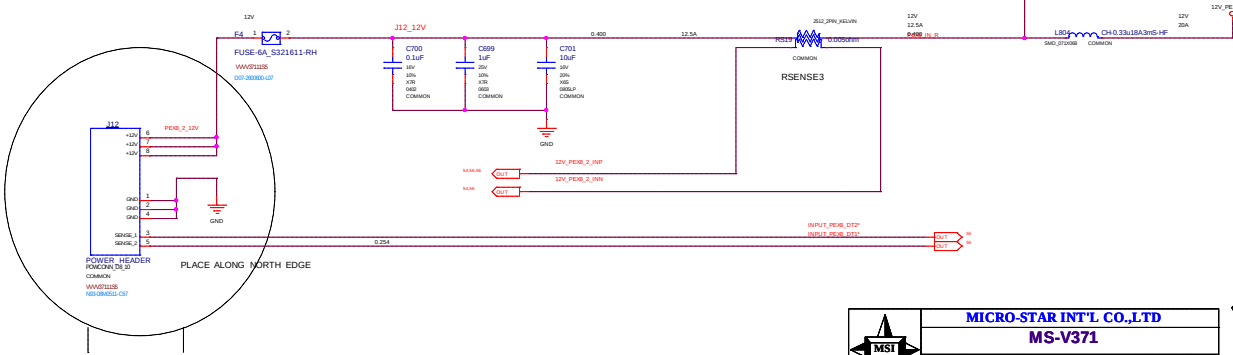
PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



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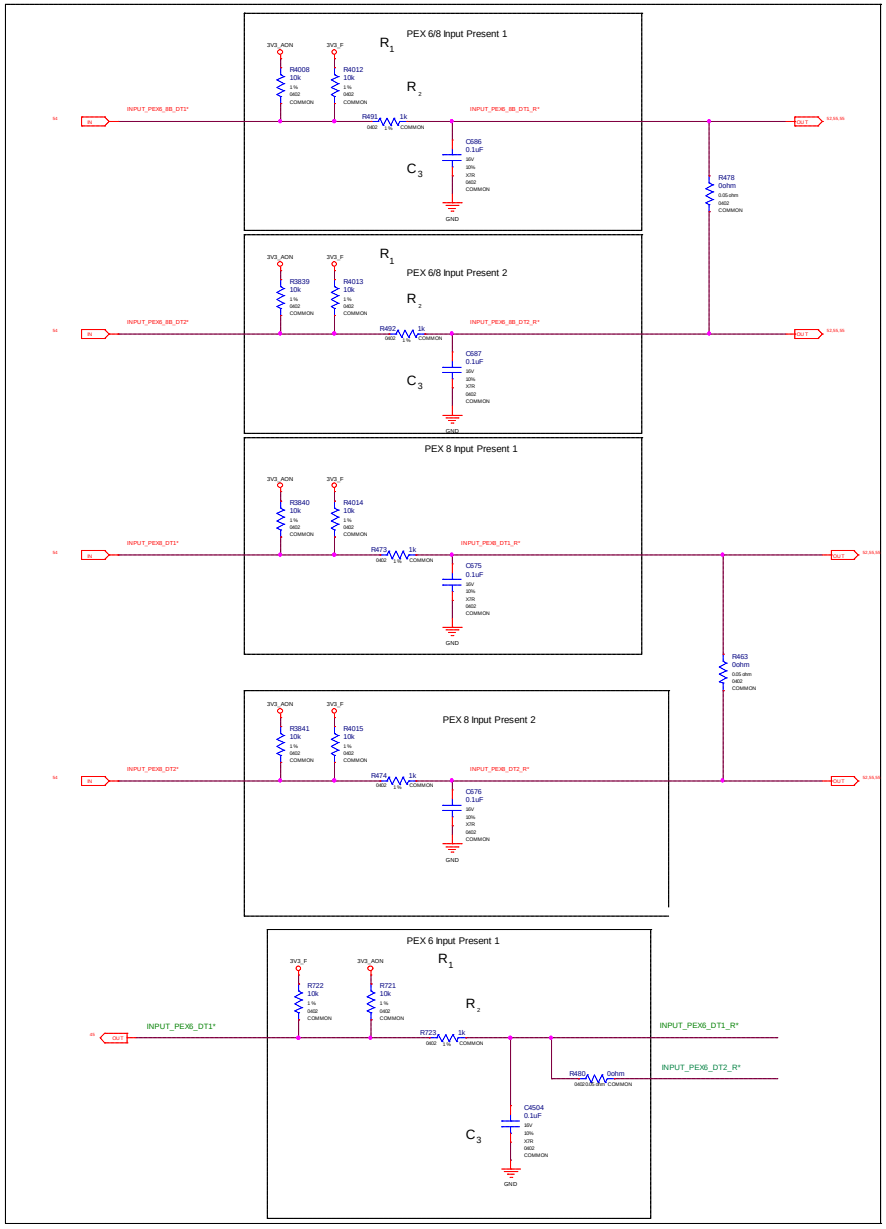
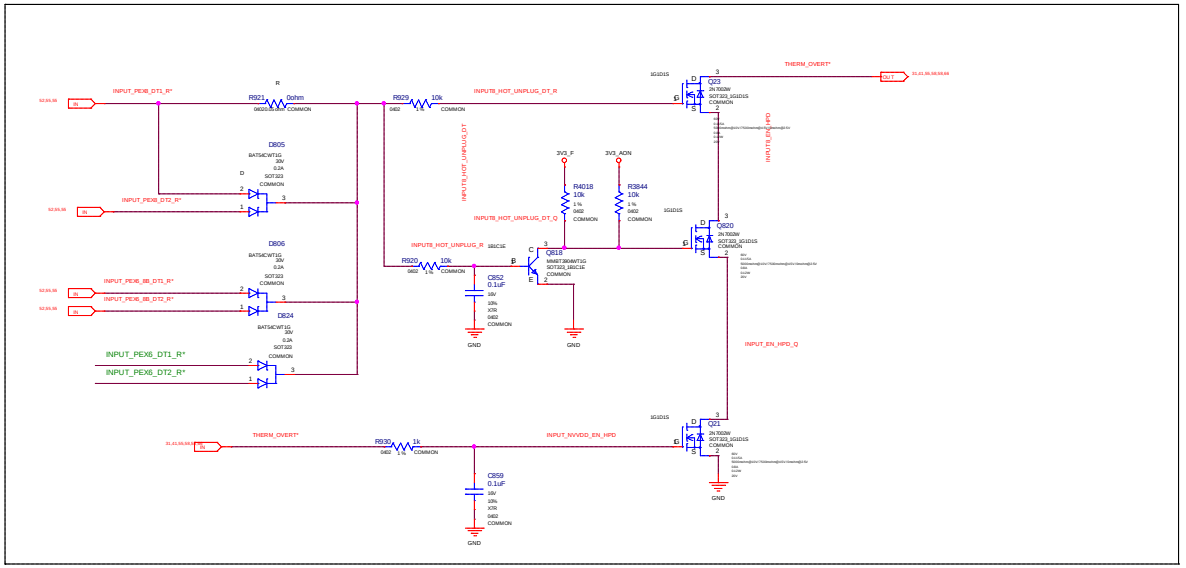
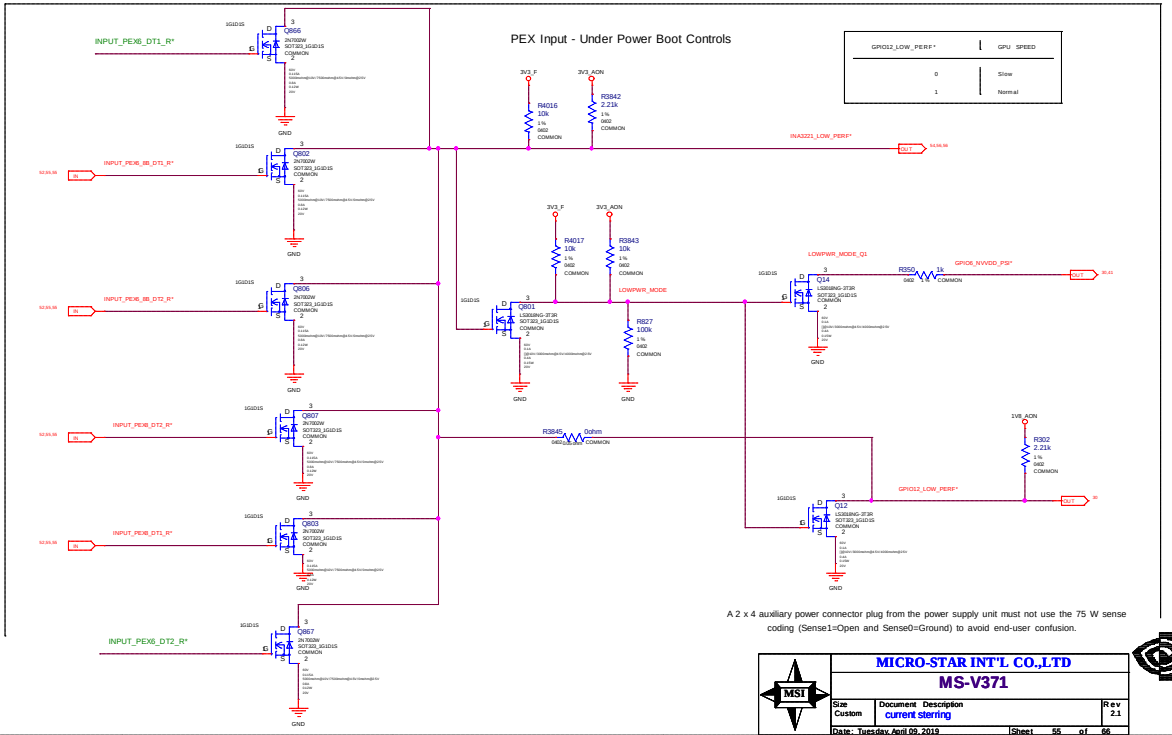
PS: 12V Current Steering & Hot Unplug Detect







A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

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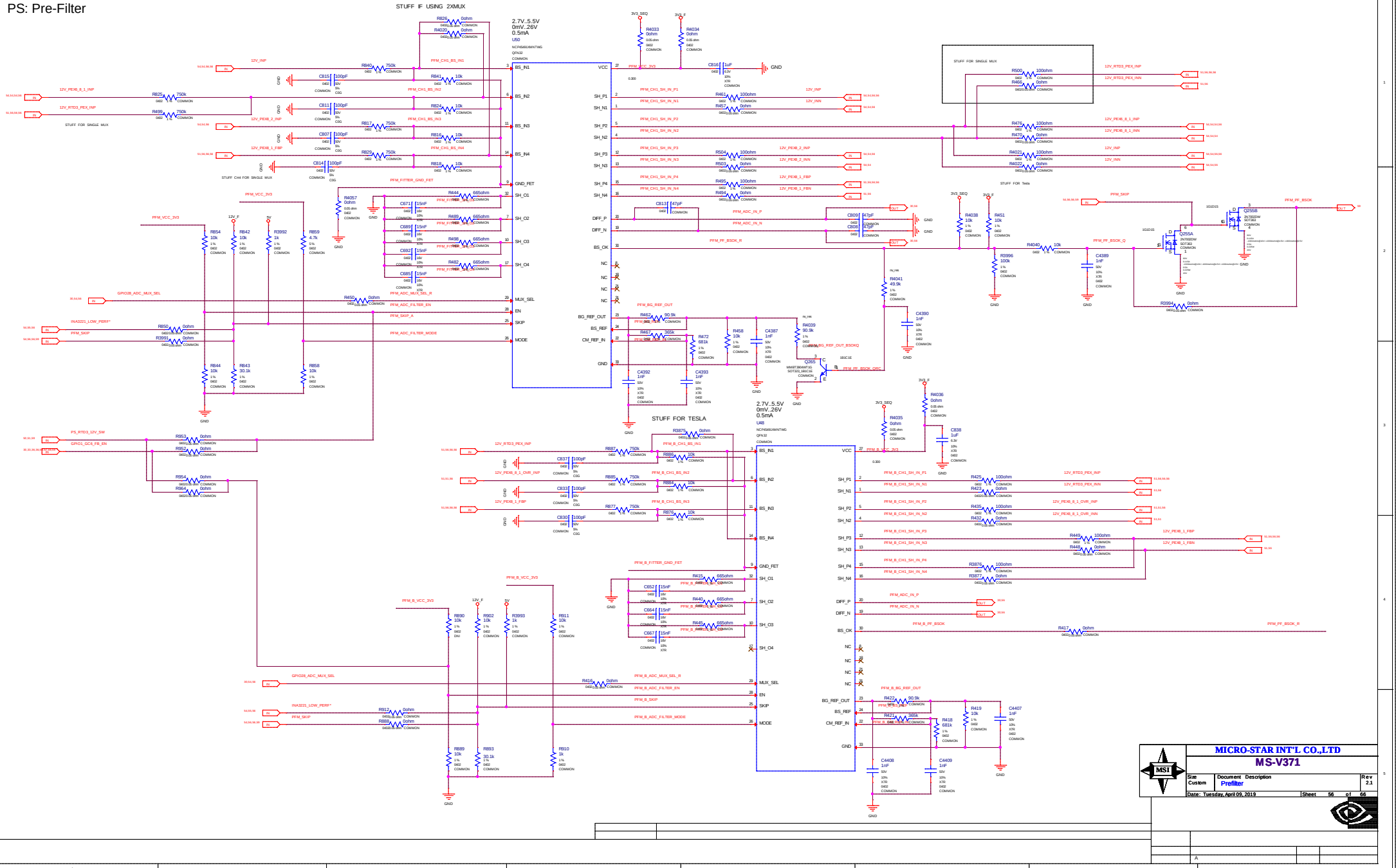
PS: Pre-Filter



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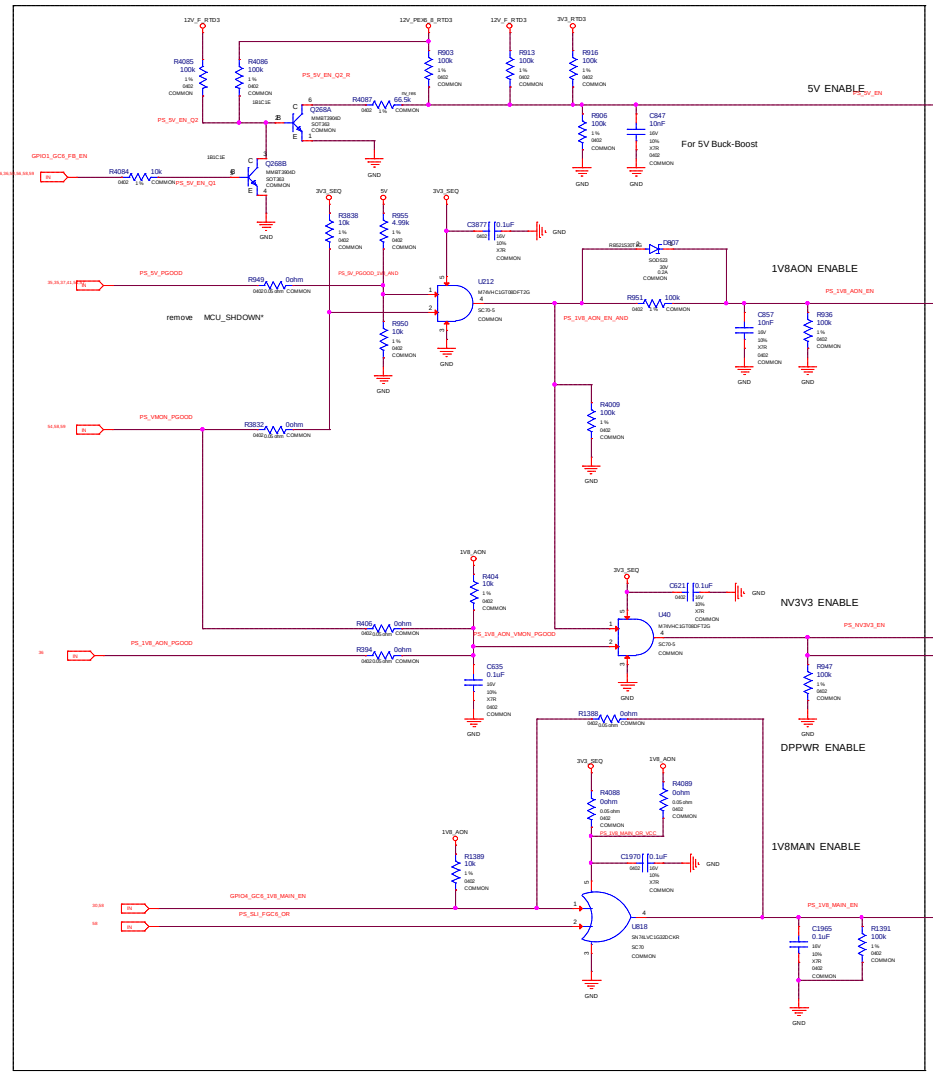
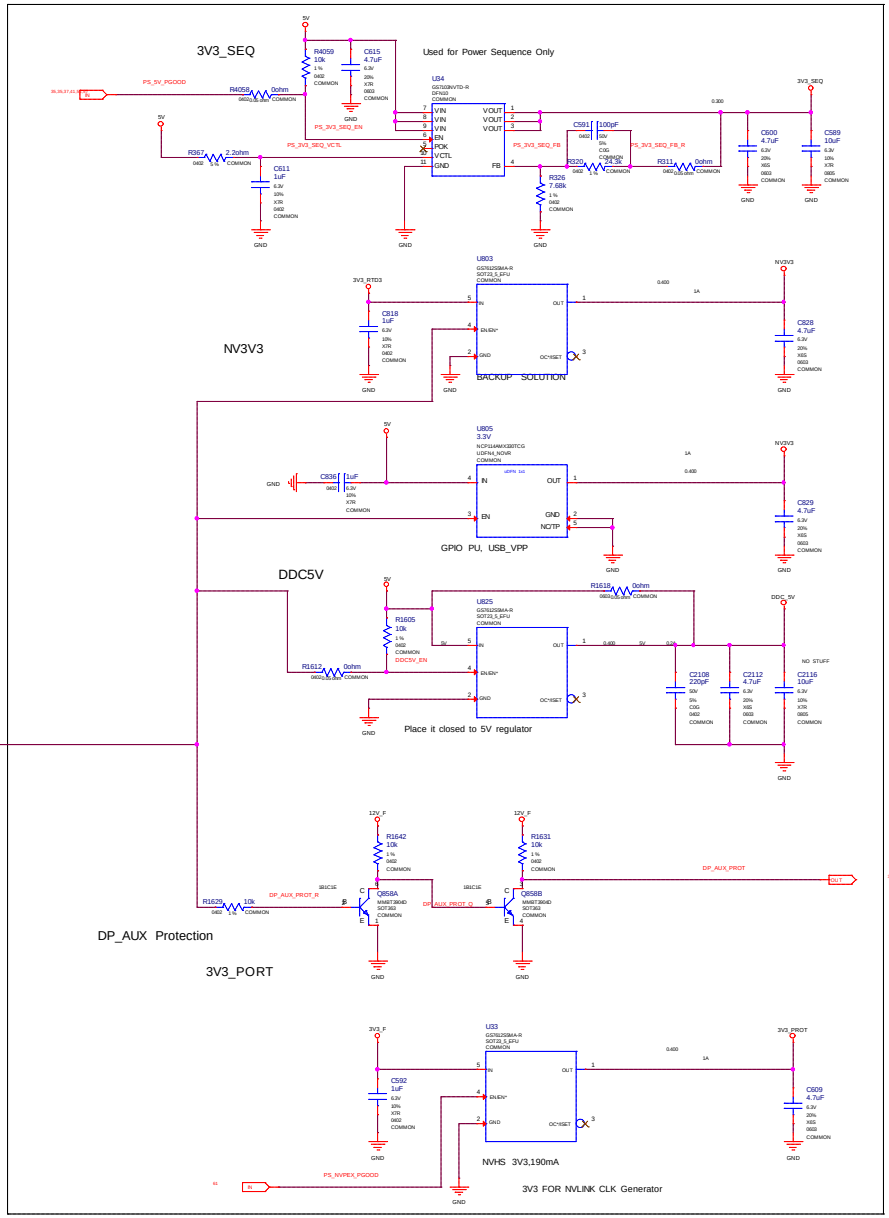
SEQUENCE:5V,1V8,NV3V3 ENABLE





ASSEMBLY
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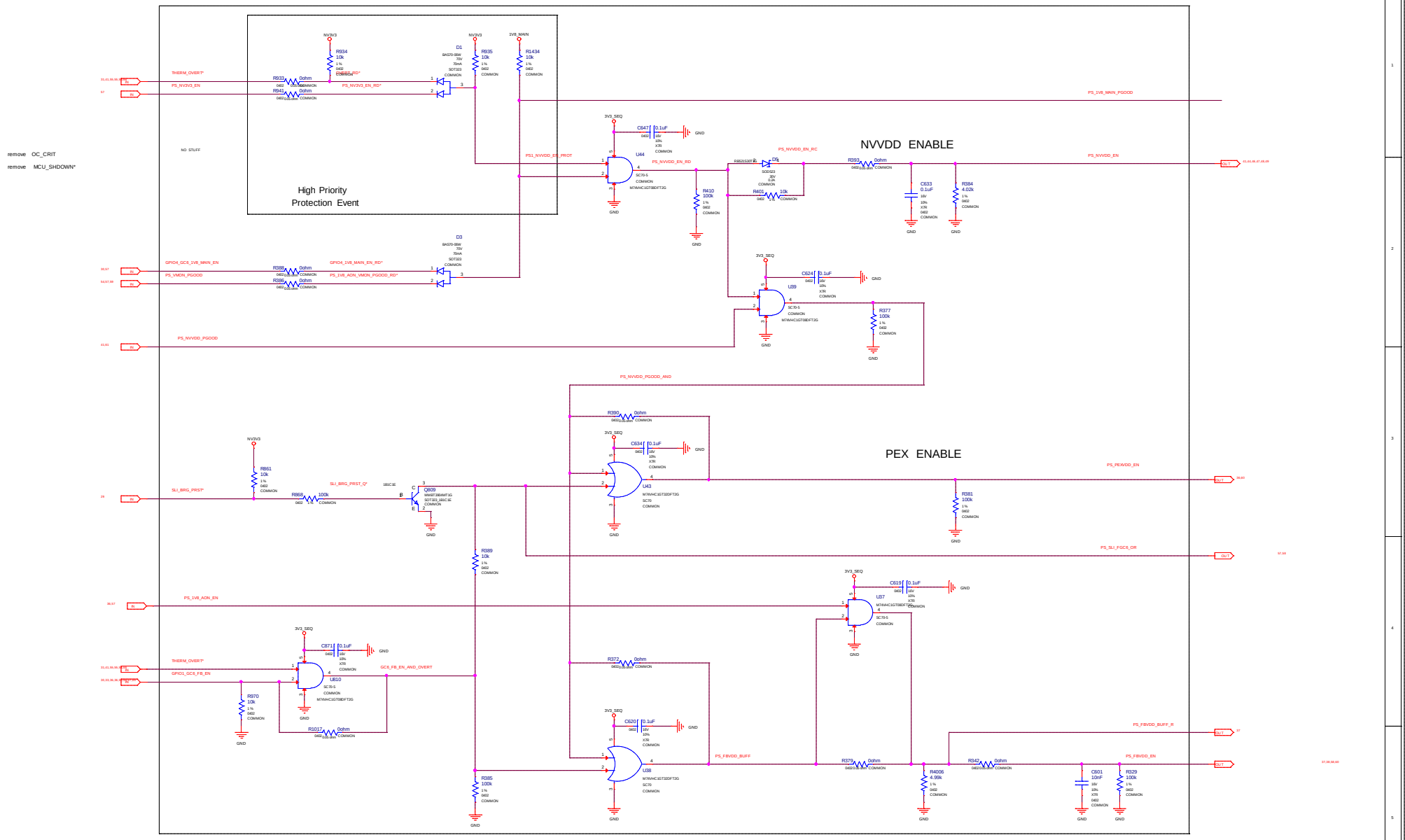
SEQUENCE:NV,PEX,FB ENABLE



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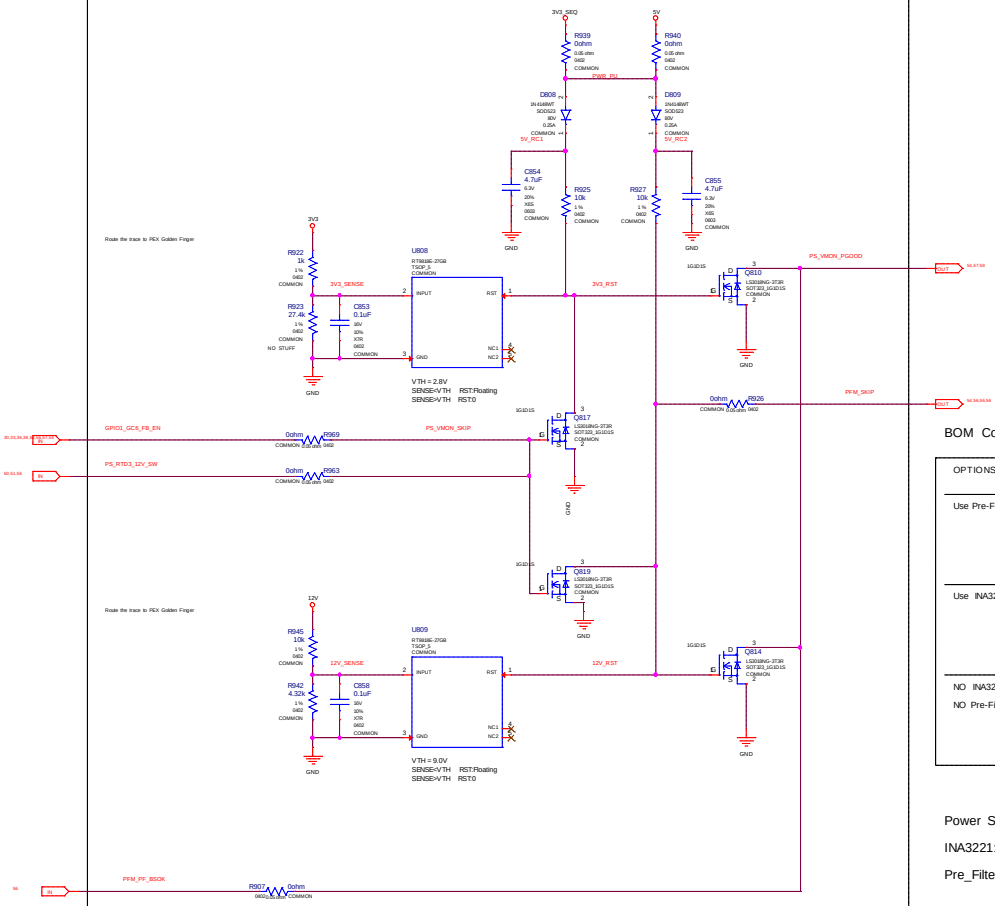
SEQUENCE:PCIE Voltage Monitor

PCIE Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX

and All Input 12Vs

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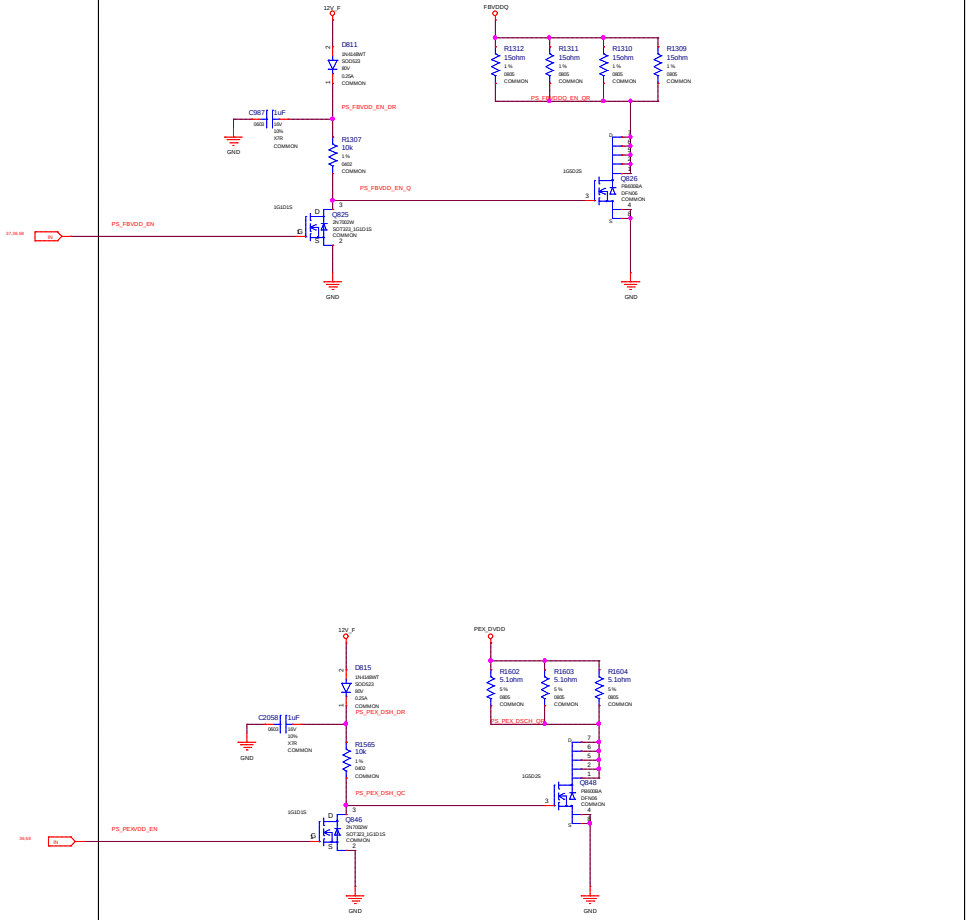
SEQUENCE:Discharge



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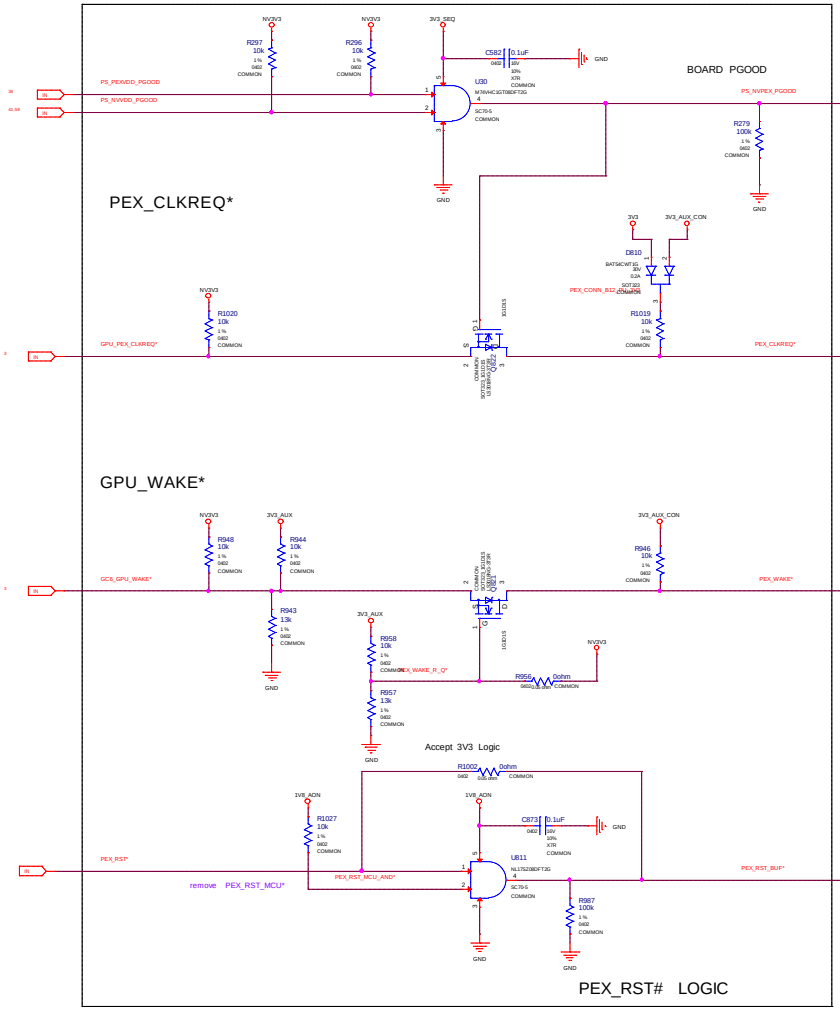
SEQUENCE:MISC



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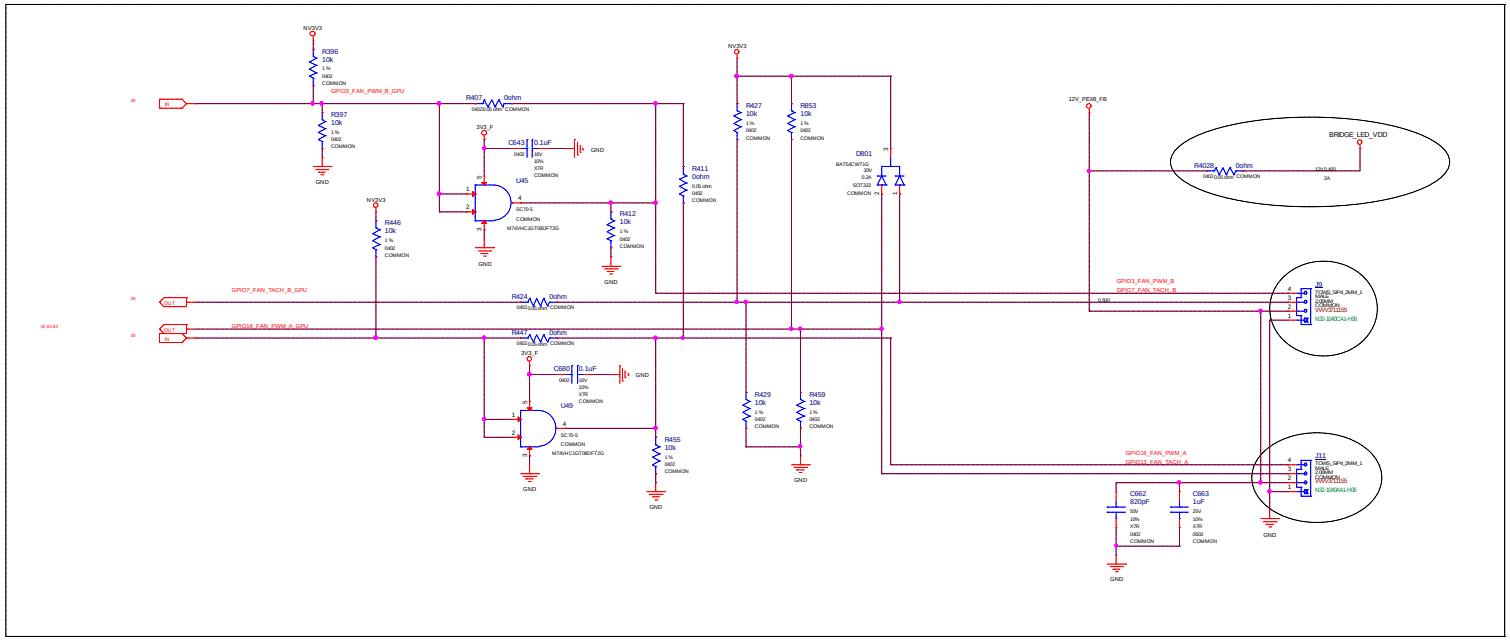
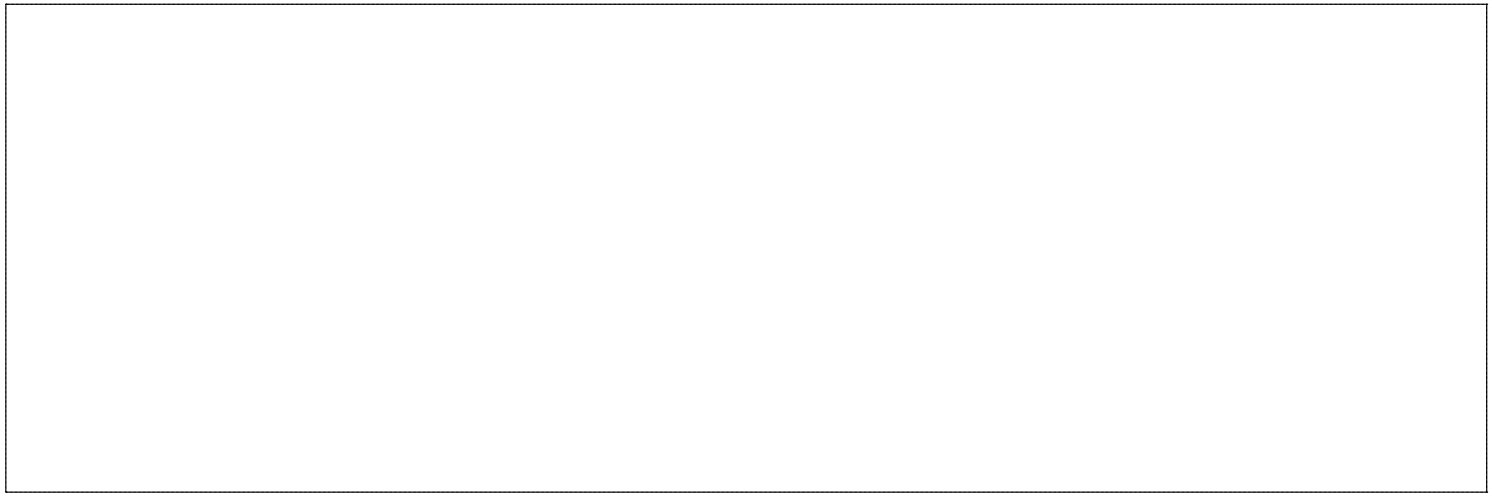
MISC: FAN & LED1





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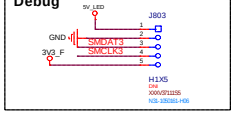
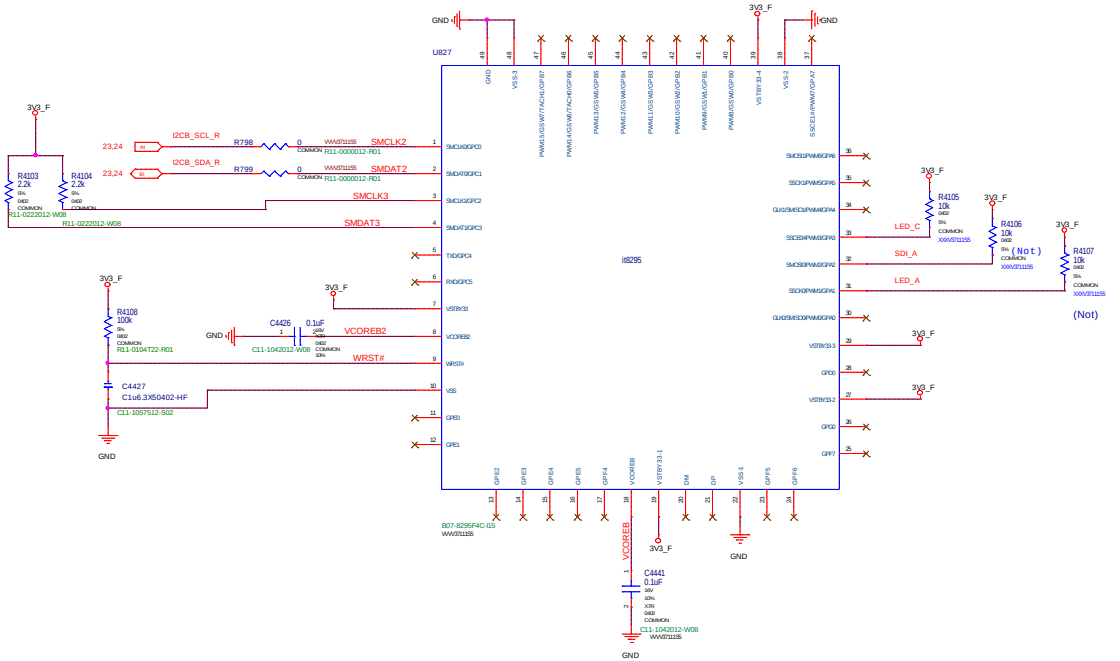
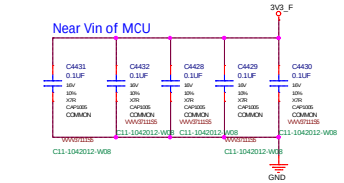
LED_CONTROLLER_IT8295

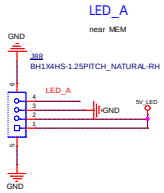
Firmware Programming

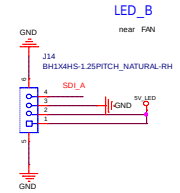
Debug

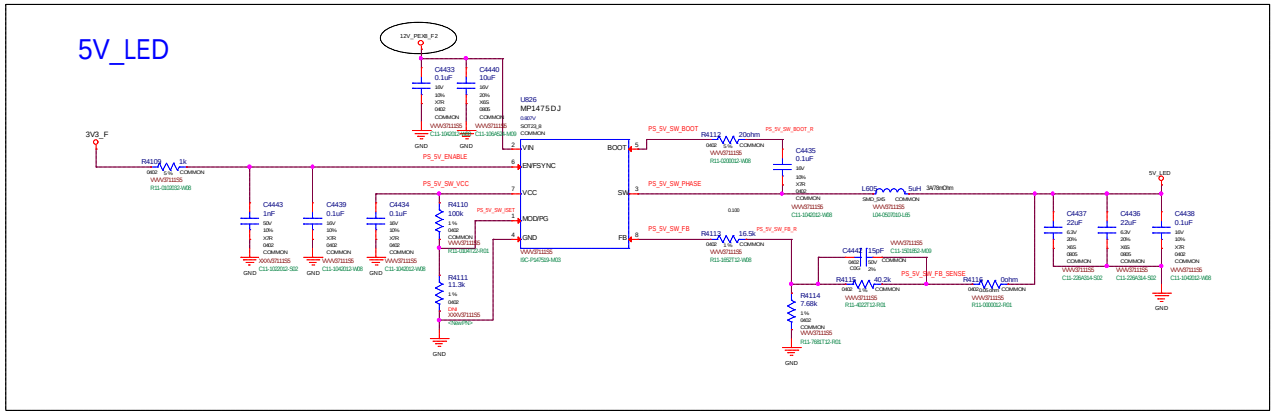


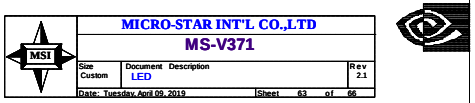












ZERO IDLE POWER MCU

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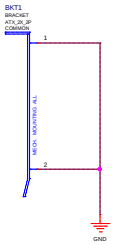
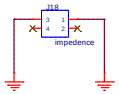
Mechanical: Bracket/Thermal Solution

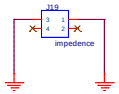
Brackets:

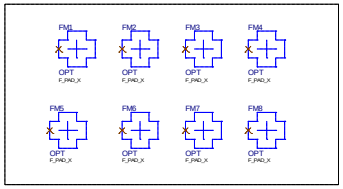


Bracket Screw

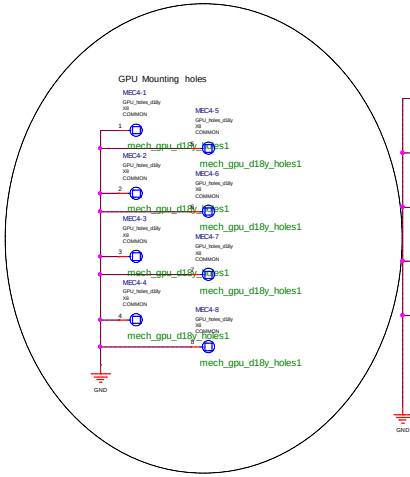
Screw



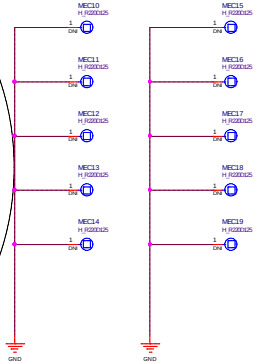




0 7 2 6 避開鉚釘點 螺絲 孔 位



Mechanical Holes Symbol



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VR THERMAL PROTECTION

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