

PG150-C03

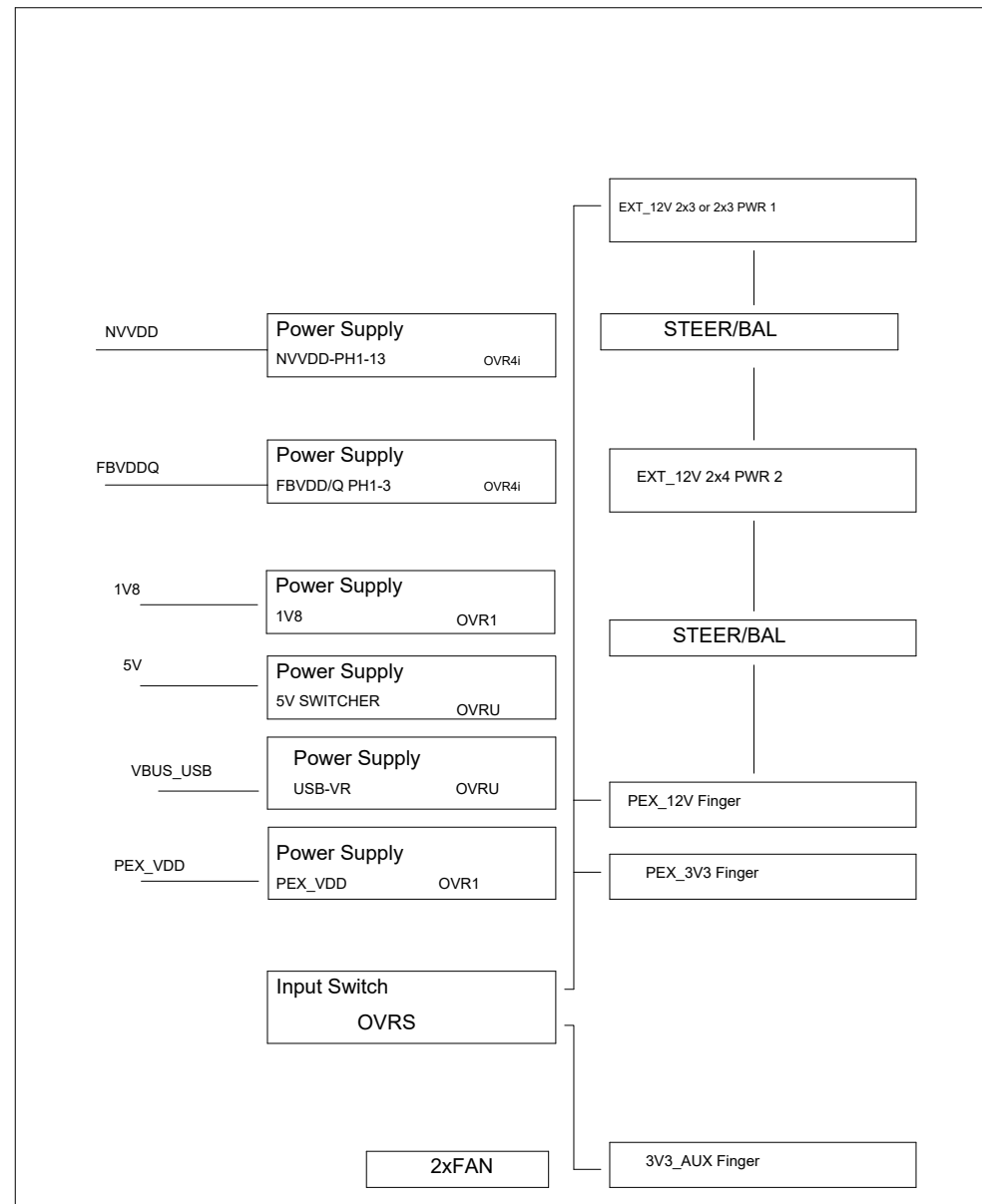
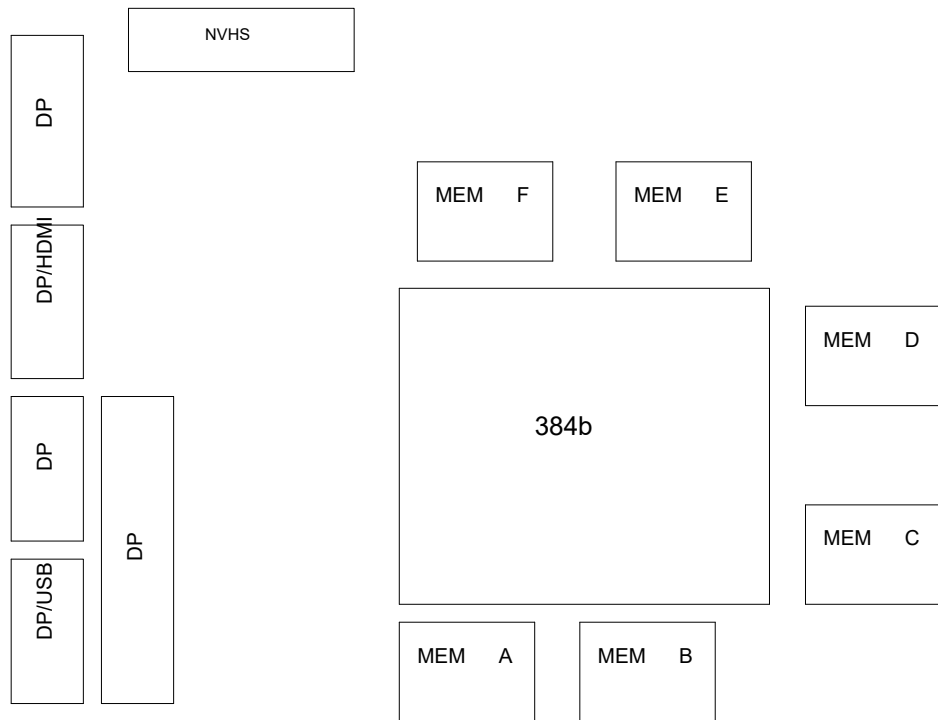
384b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

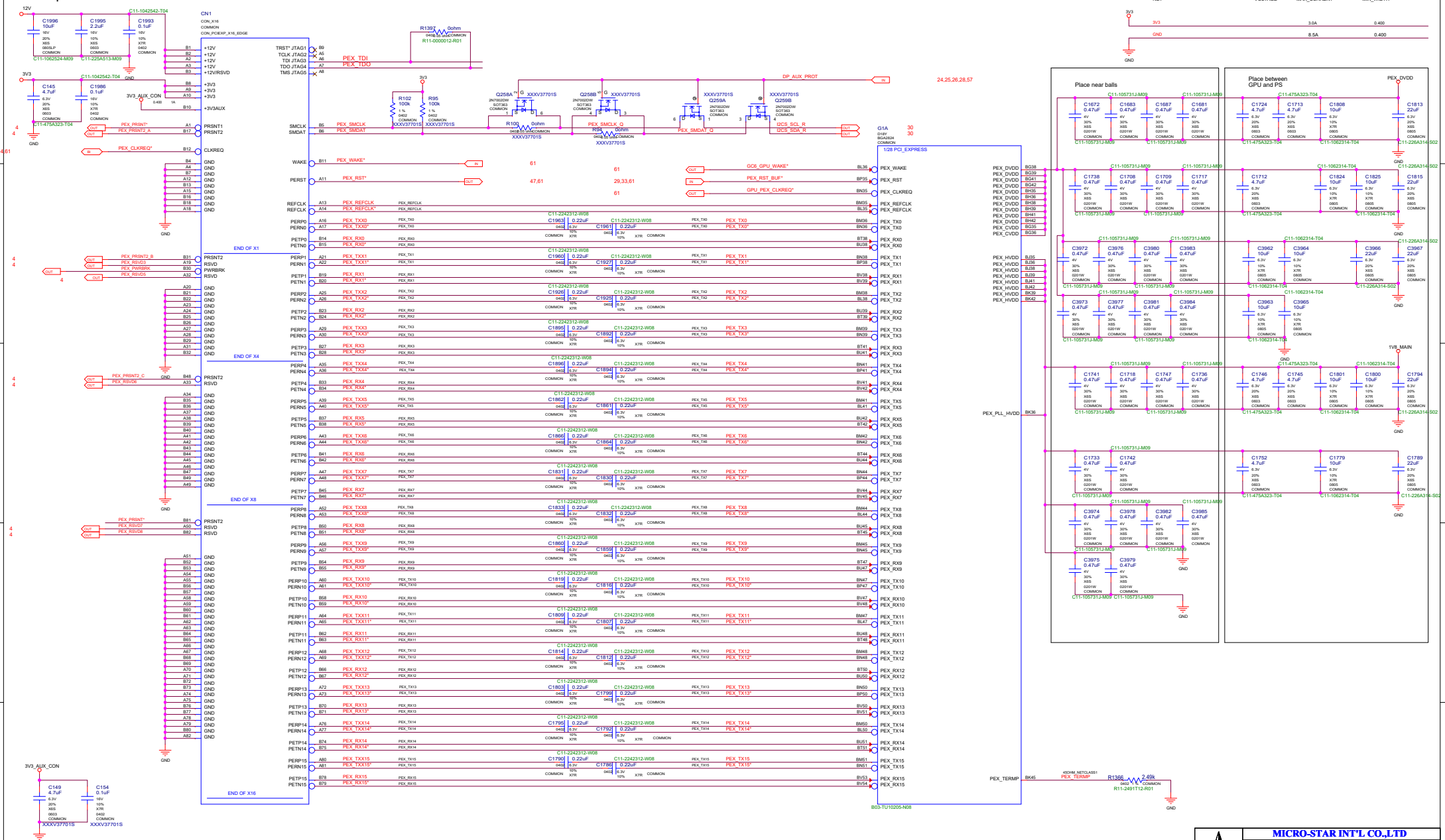
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Block Diagram



PCI Express



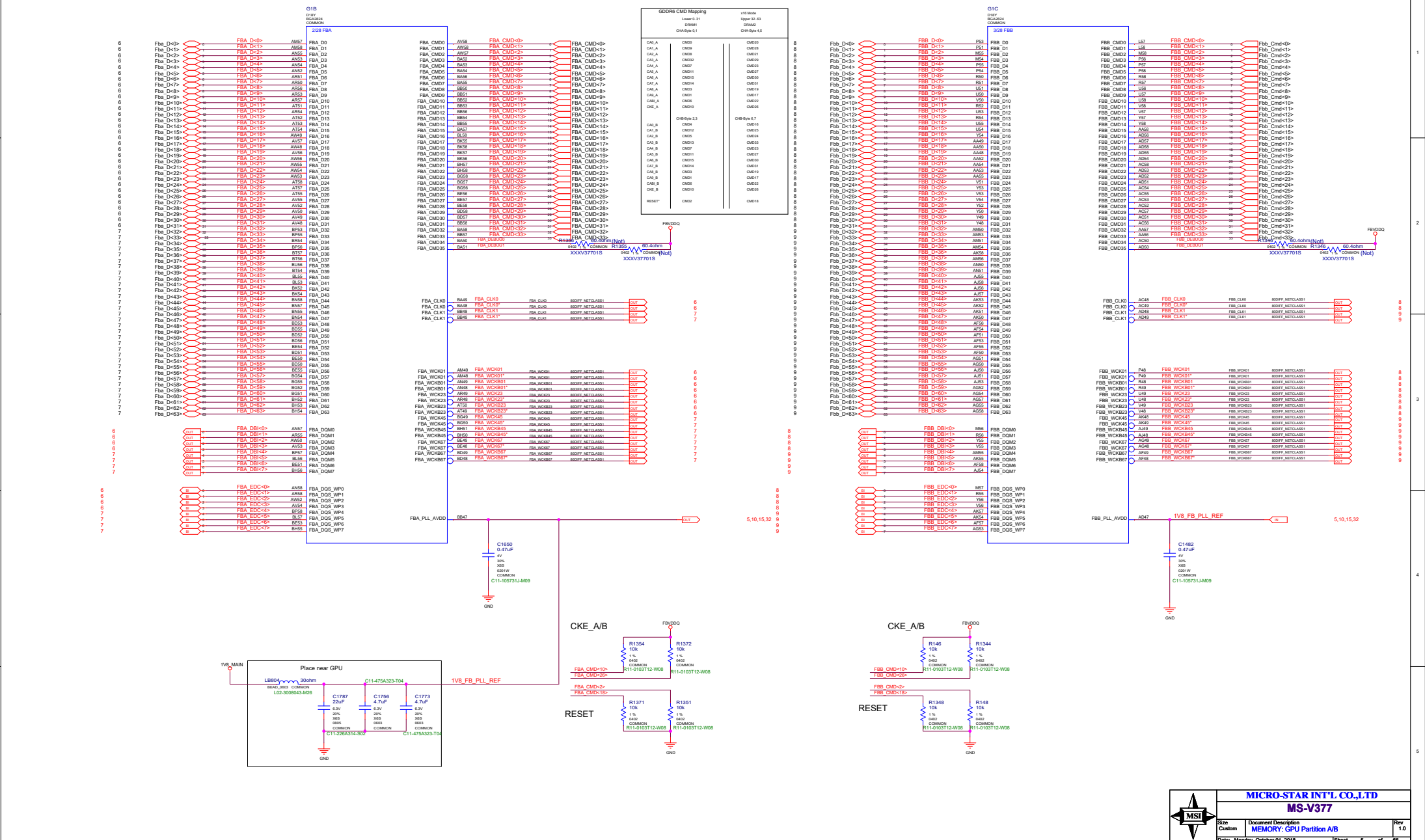
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MS-V377

Size Custom	Document Description MEMORY: GPU Partition A/B	Rev 1.0
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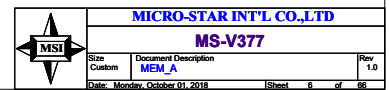
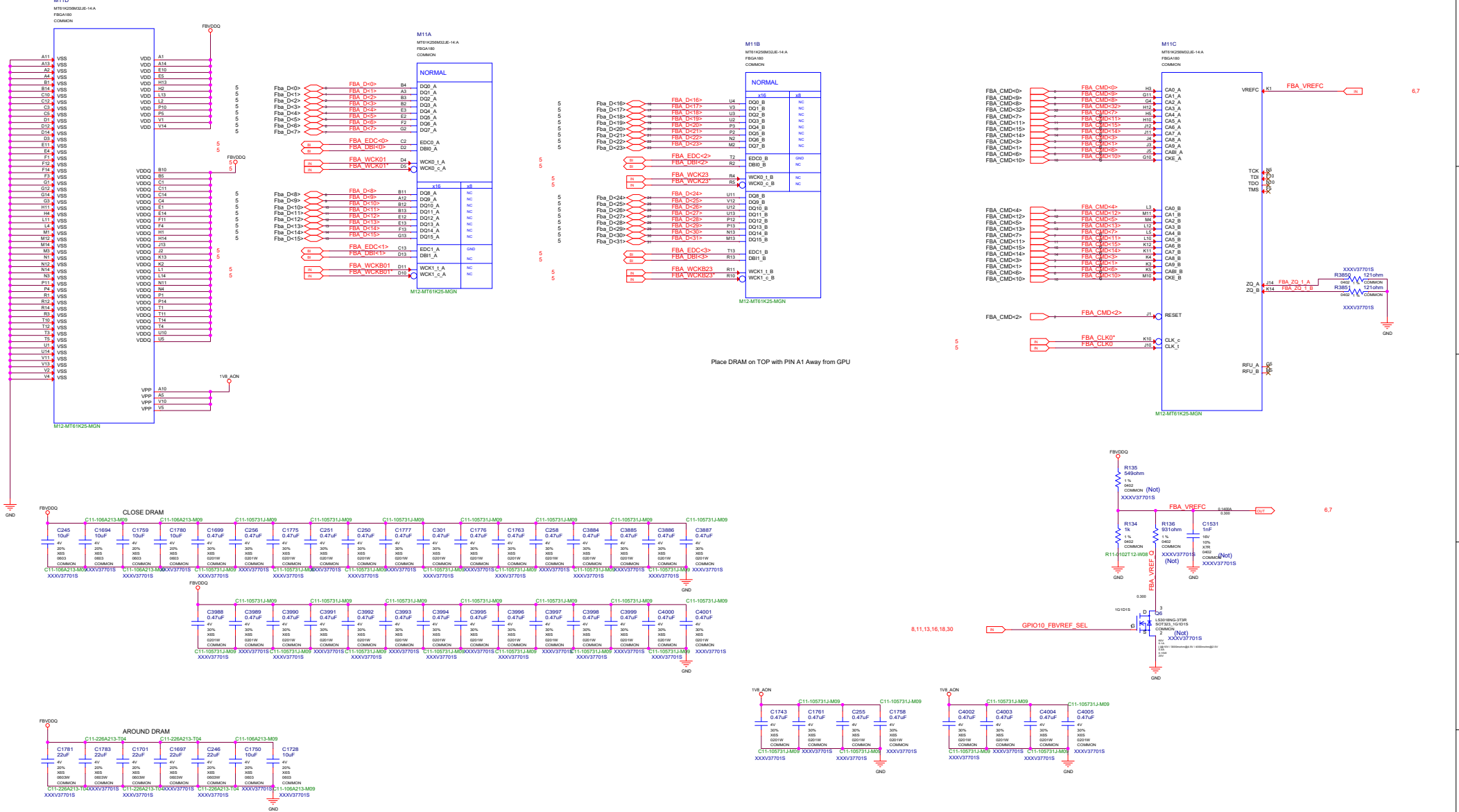
PCI TERM

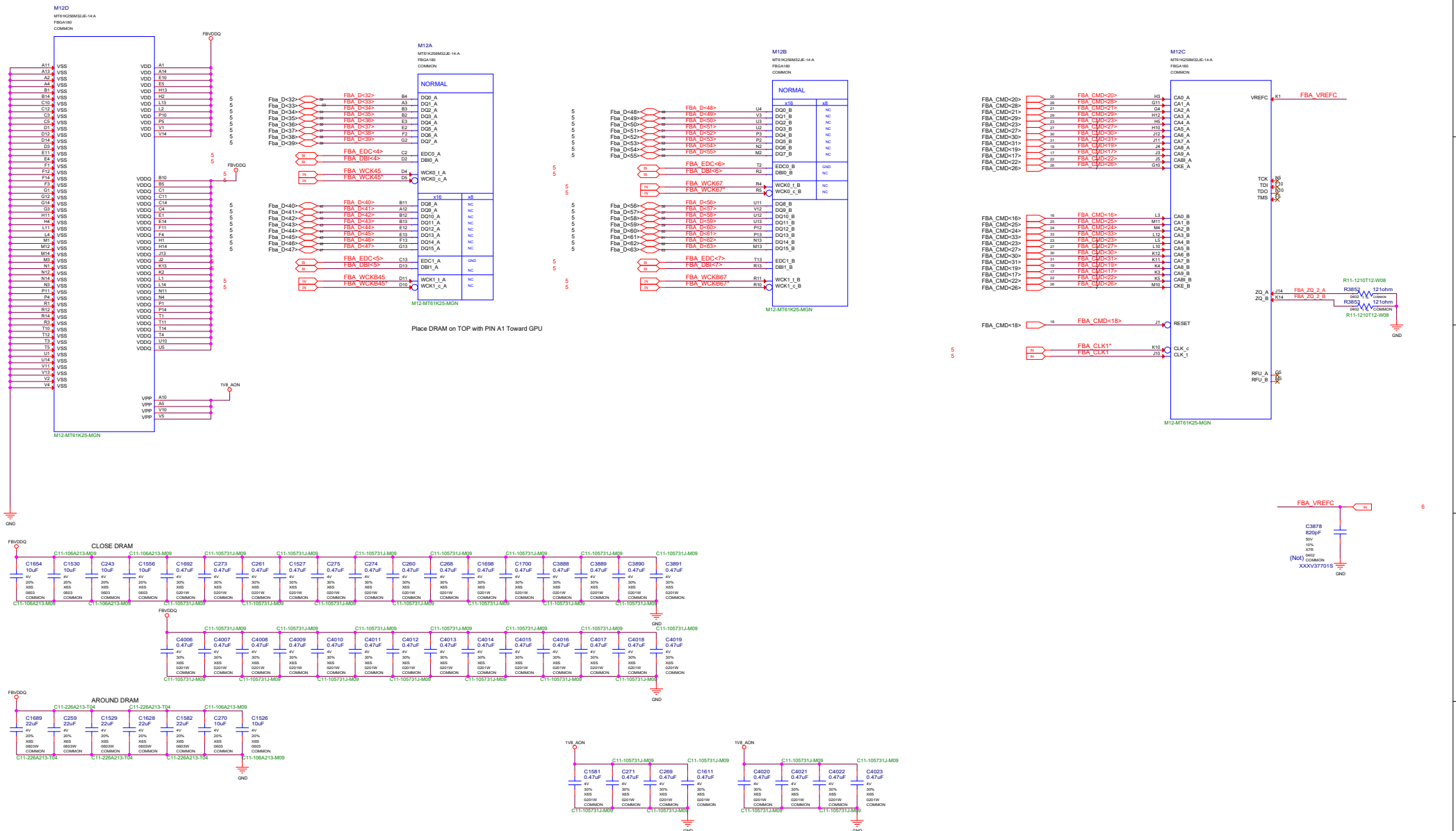


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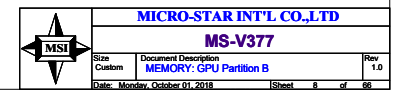
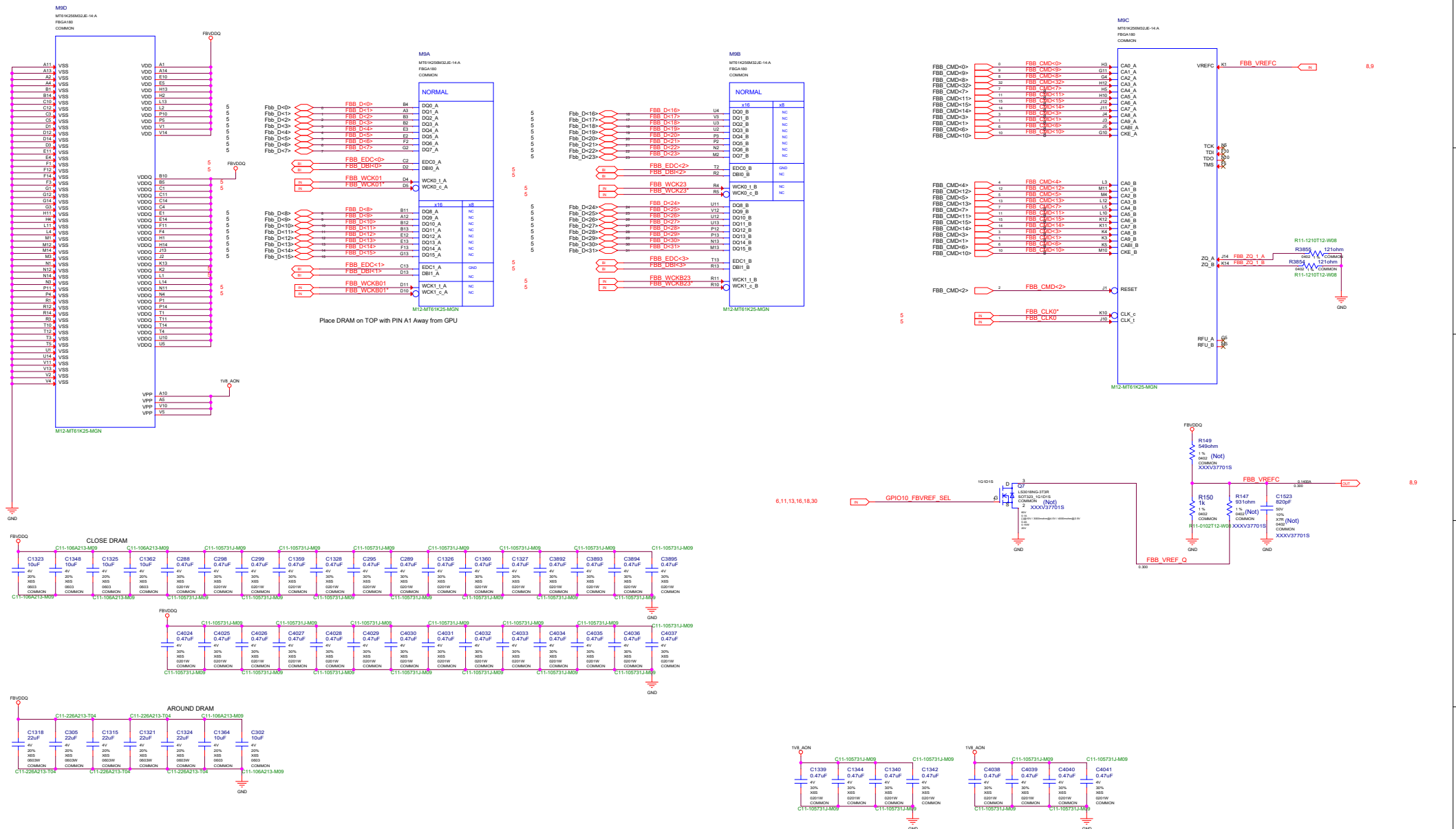


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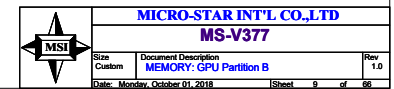
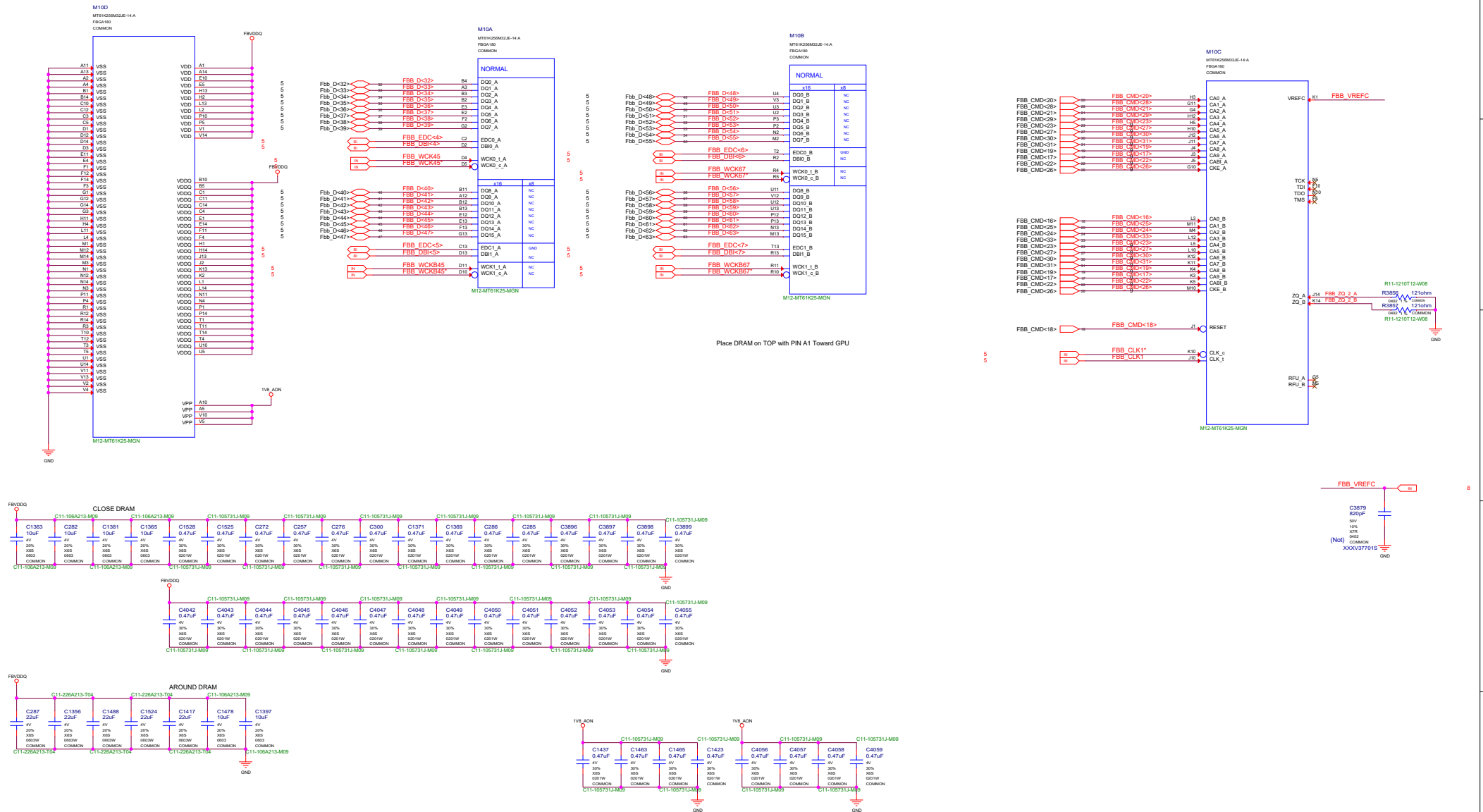




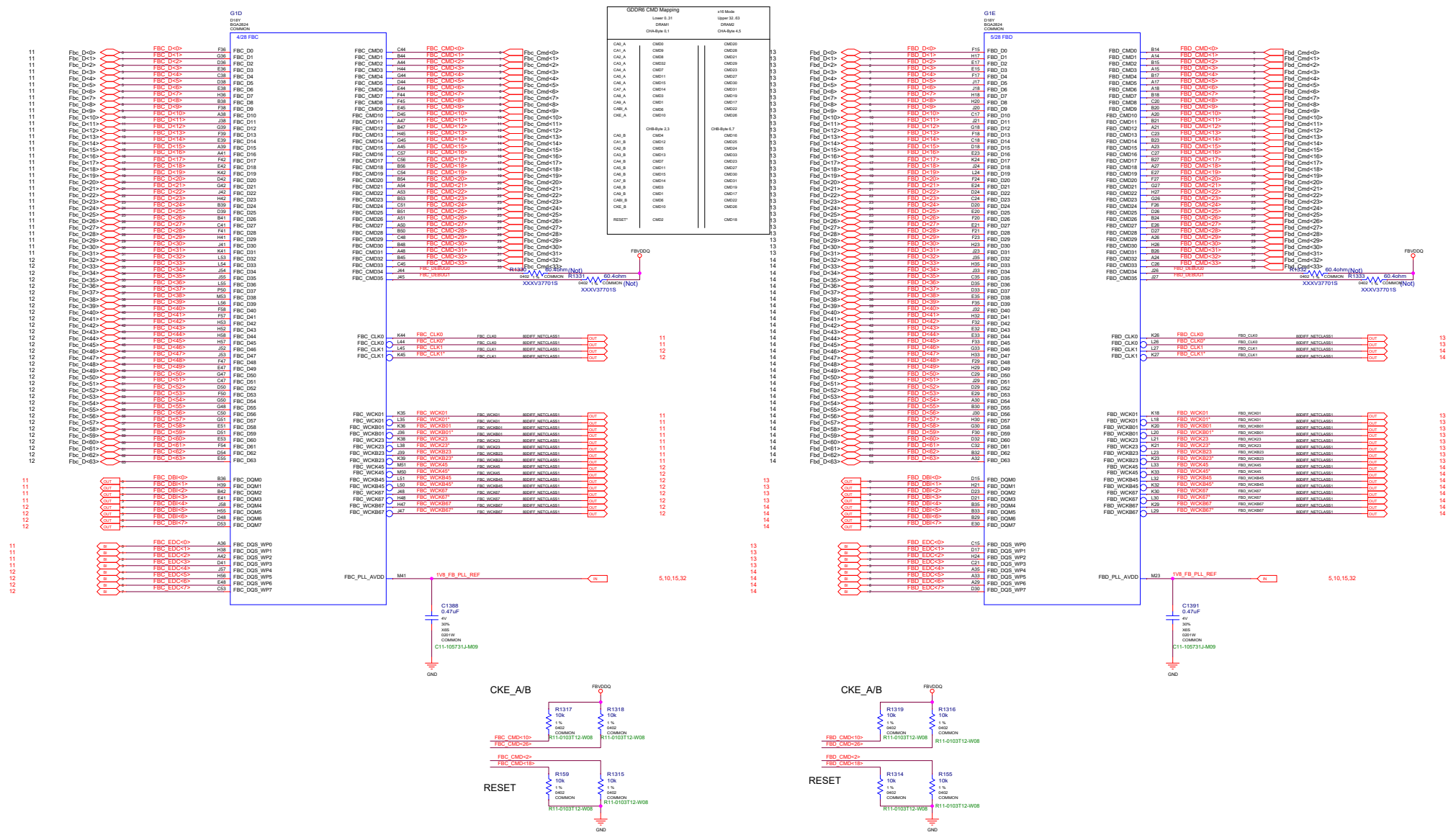
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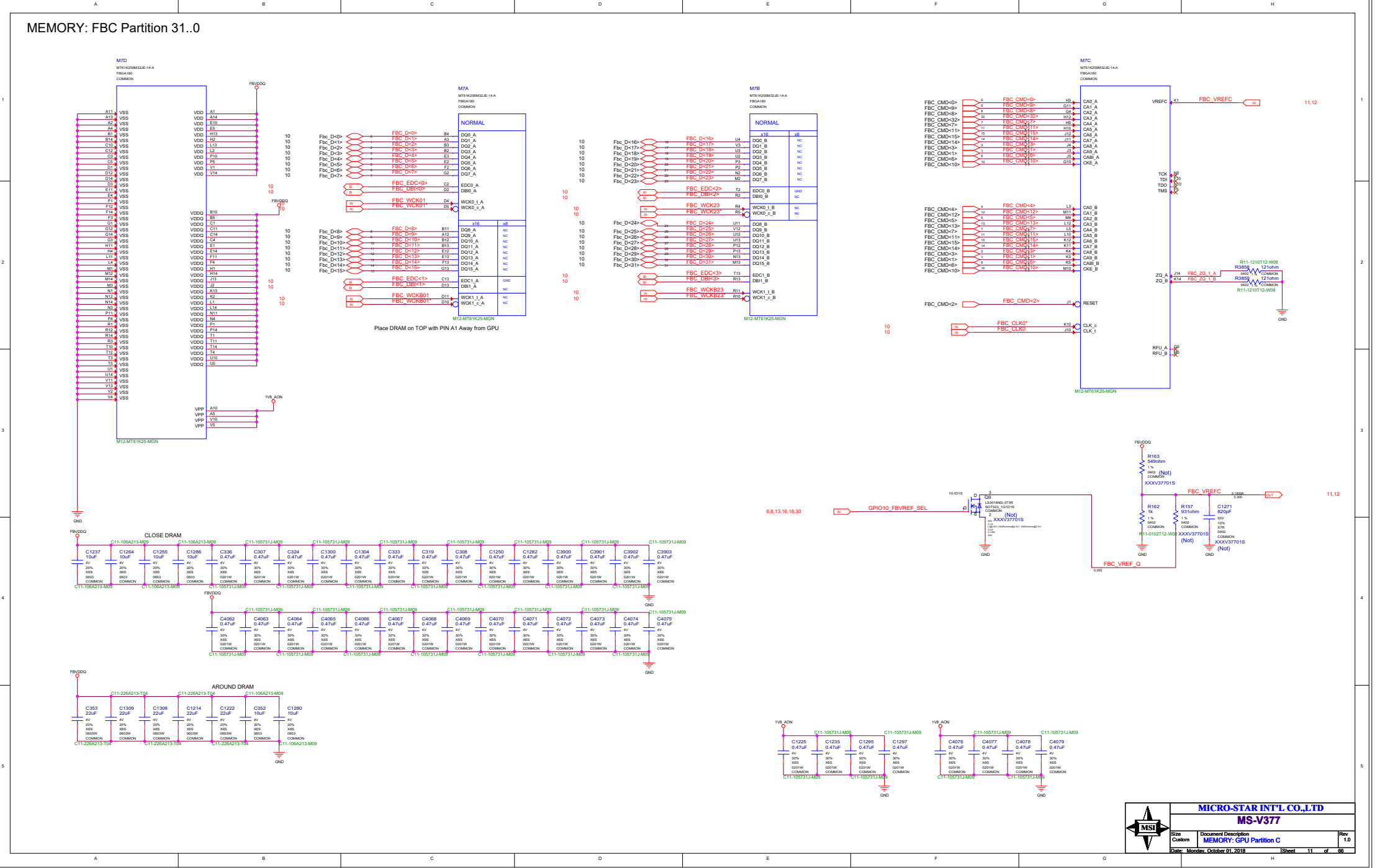
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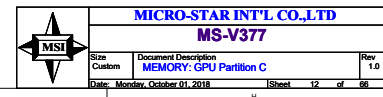
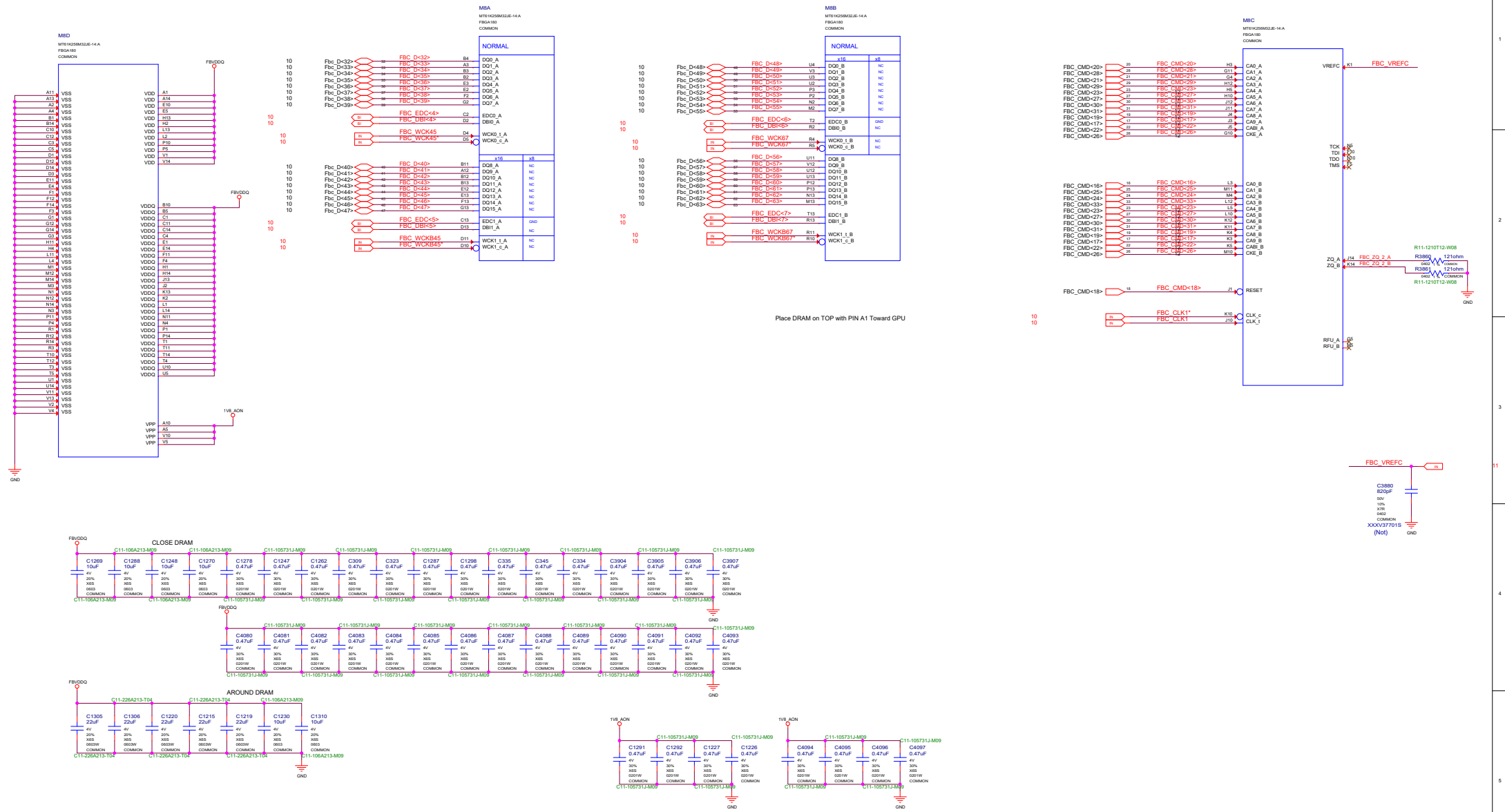


MEMORY: GPU Partition C/D

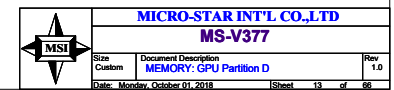
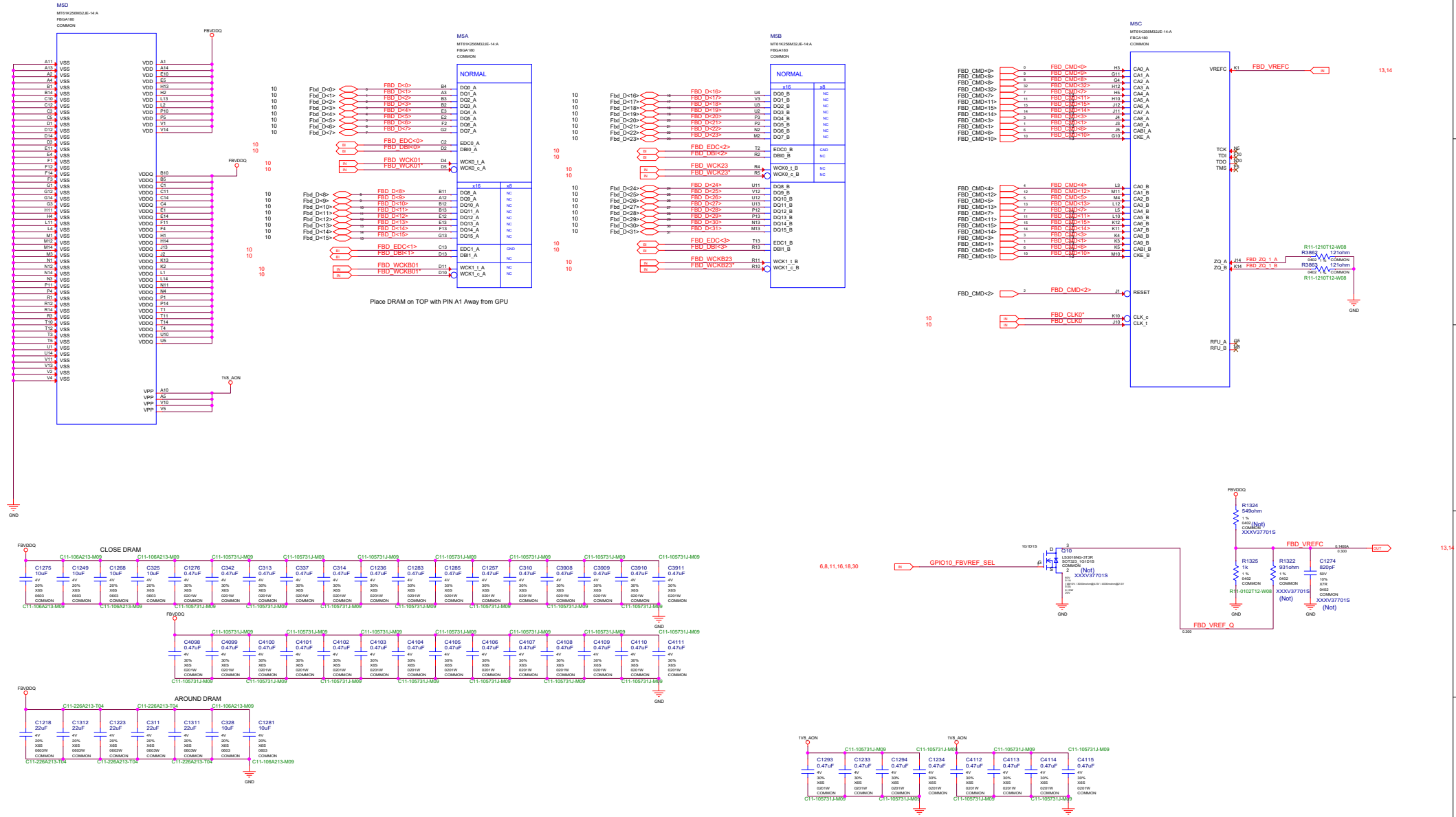


MEMORY: FBC Partition 31..0

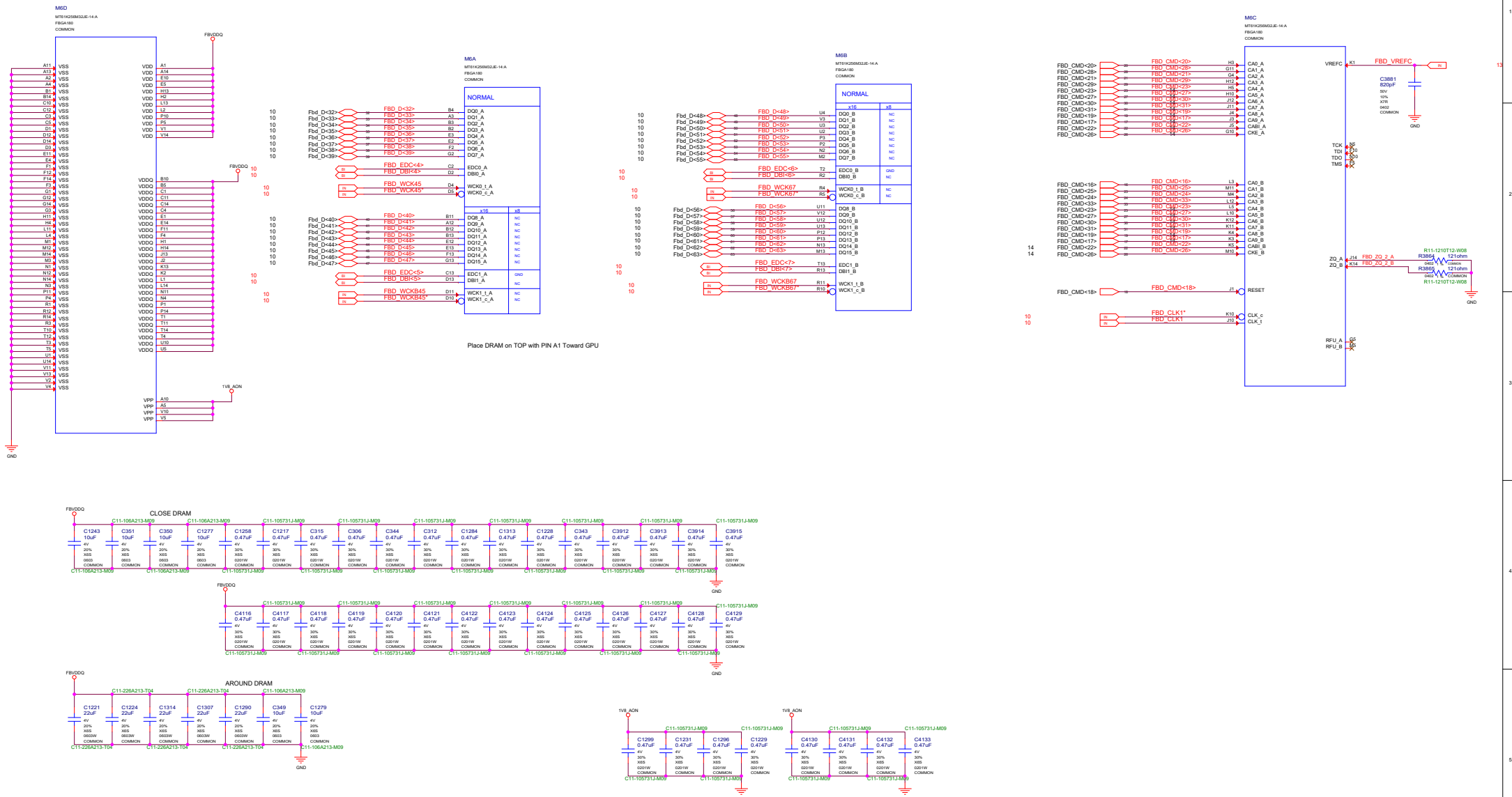


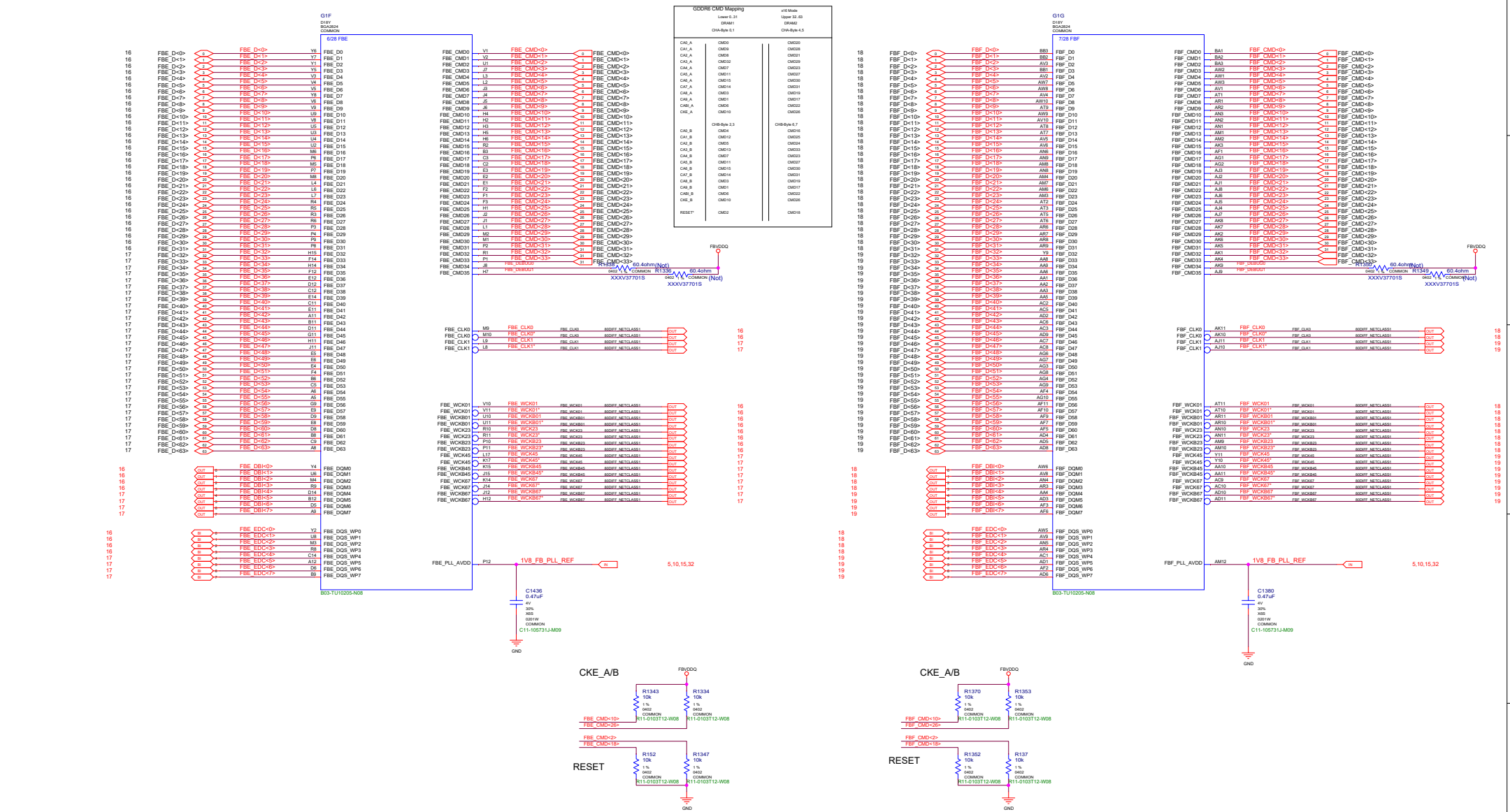


MEMORY: FBD Partition 31..0

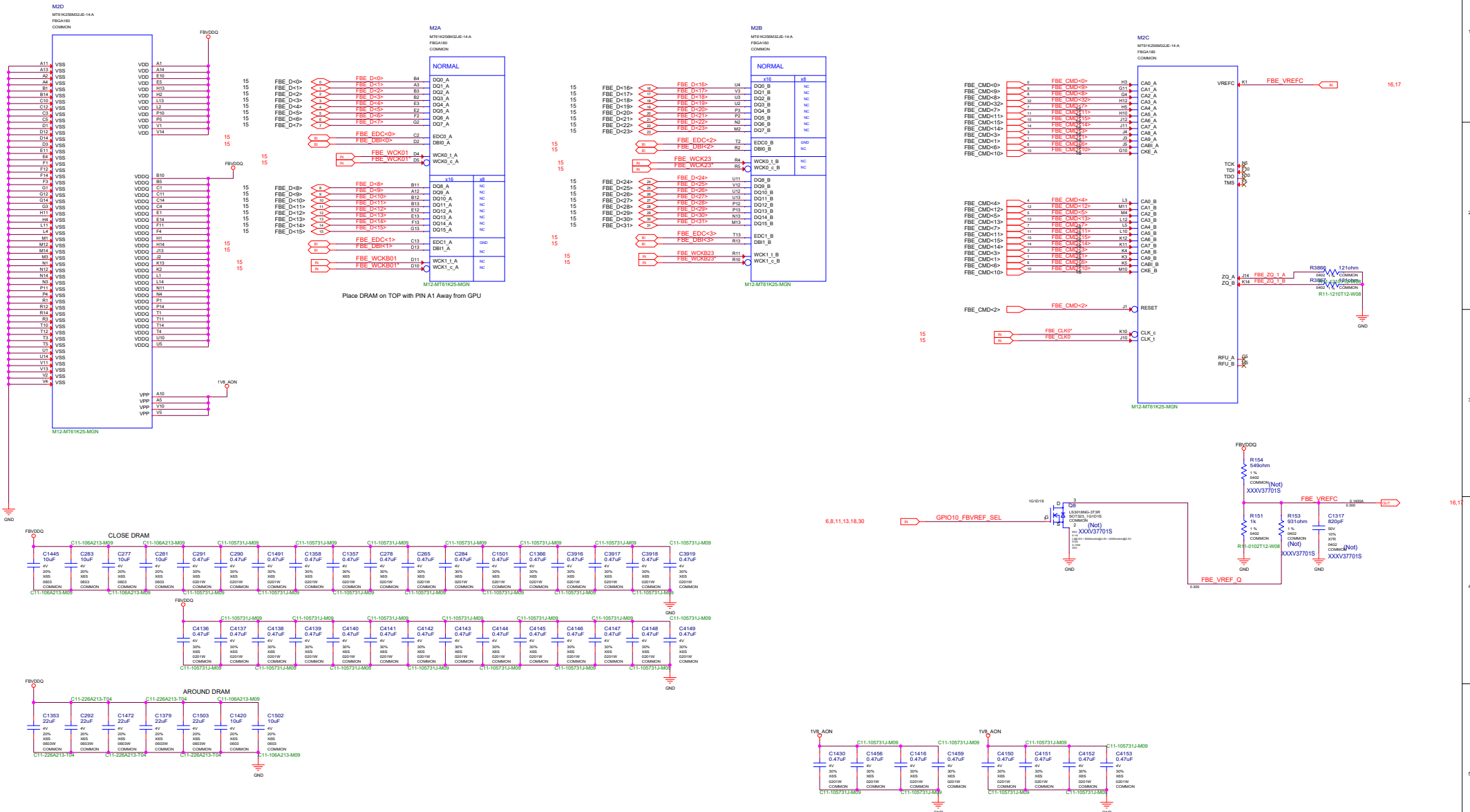


MEMORY: FBD Partition 63..32





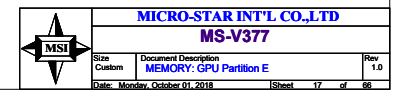
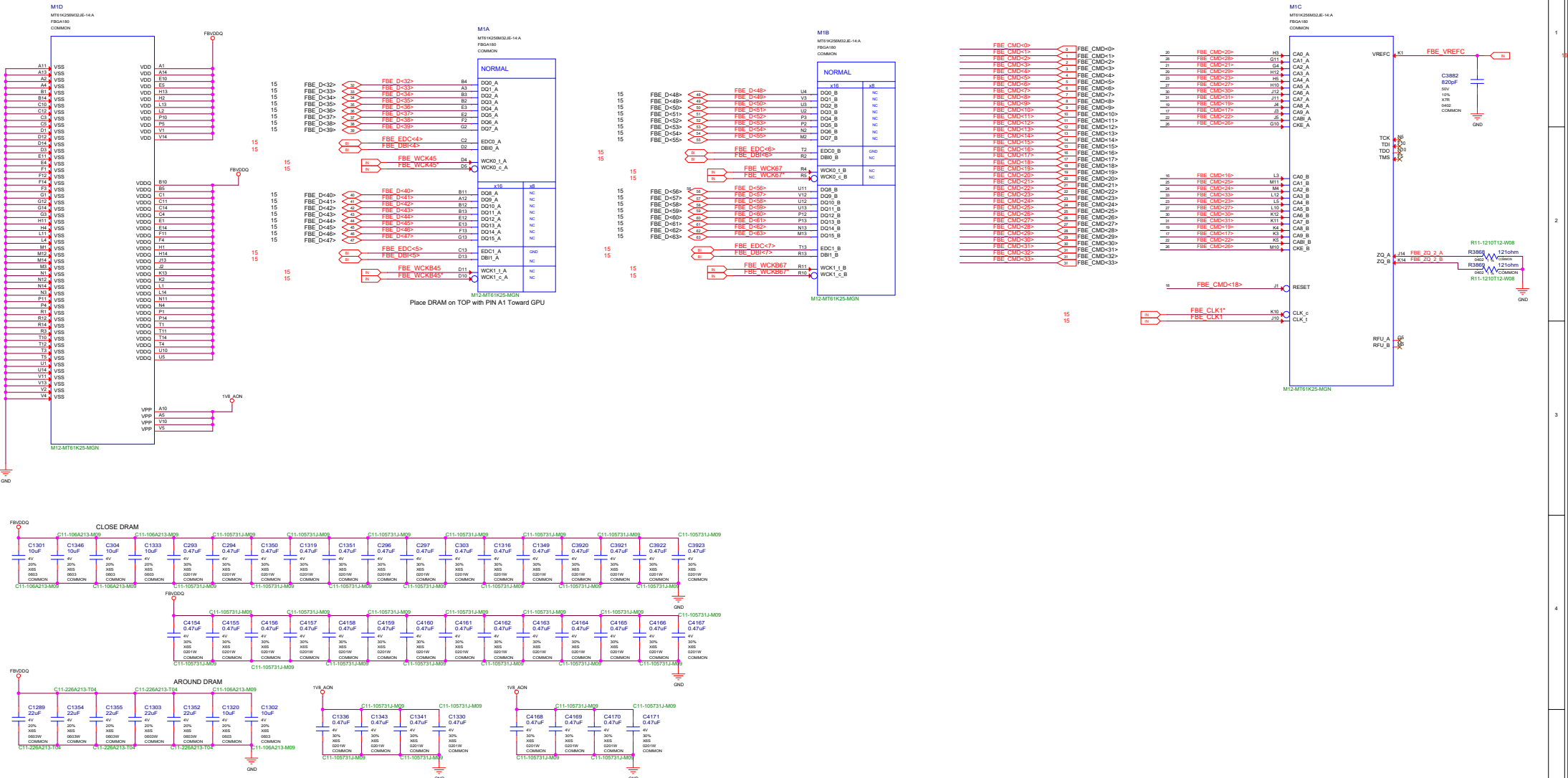
MEMORY: FBE Partition 31..0

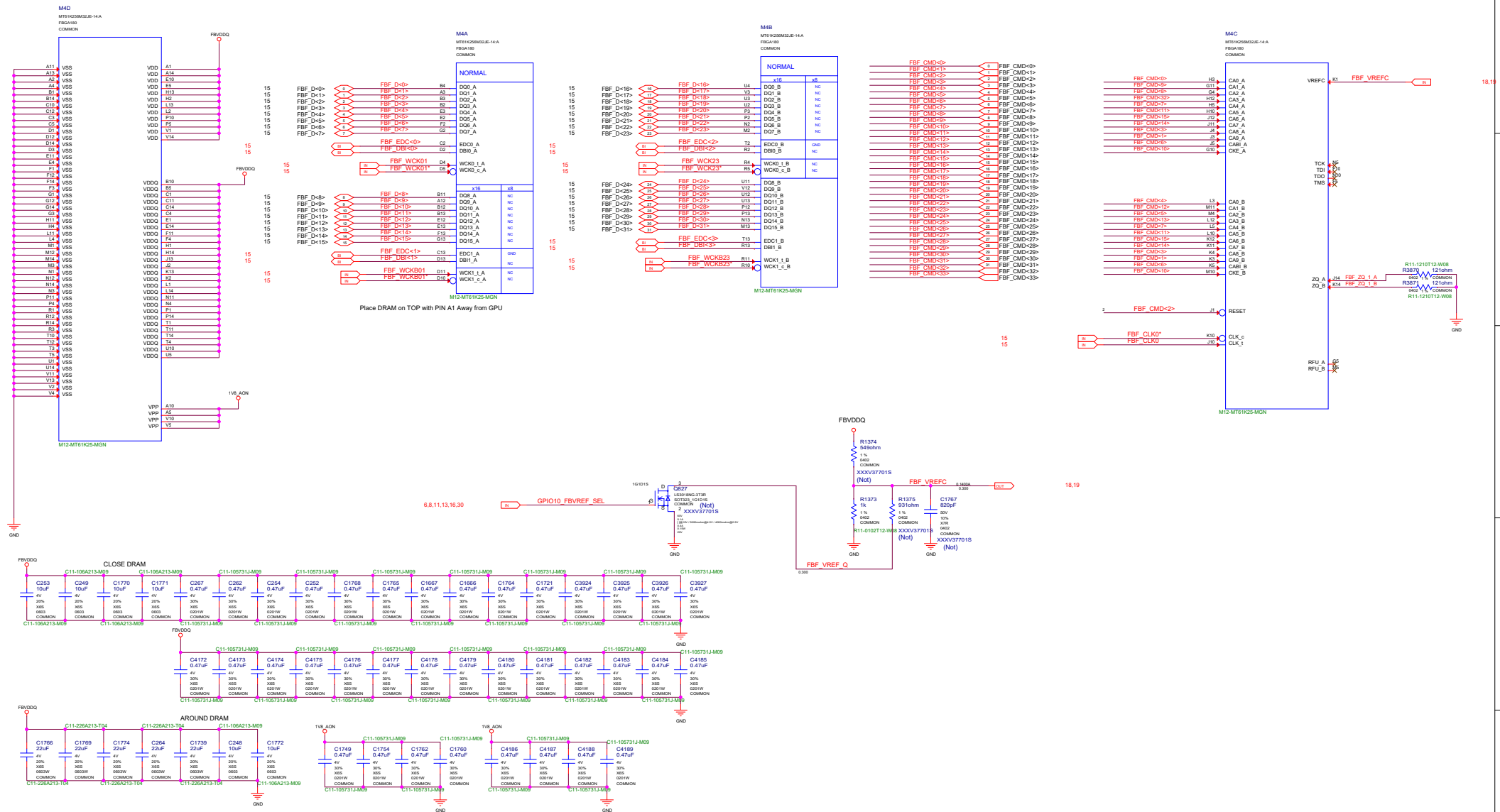


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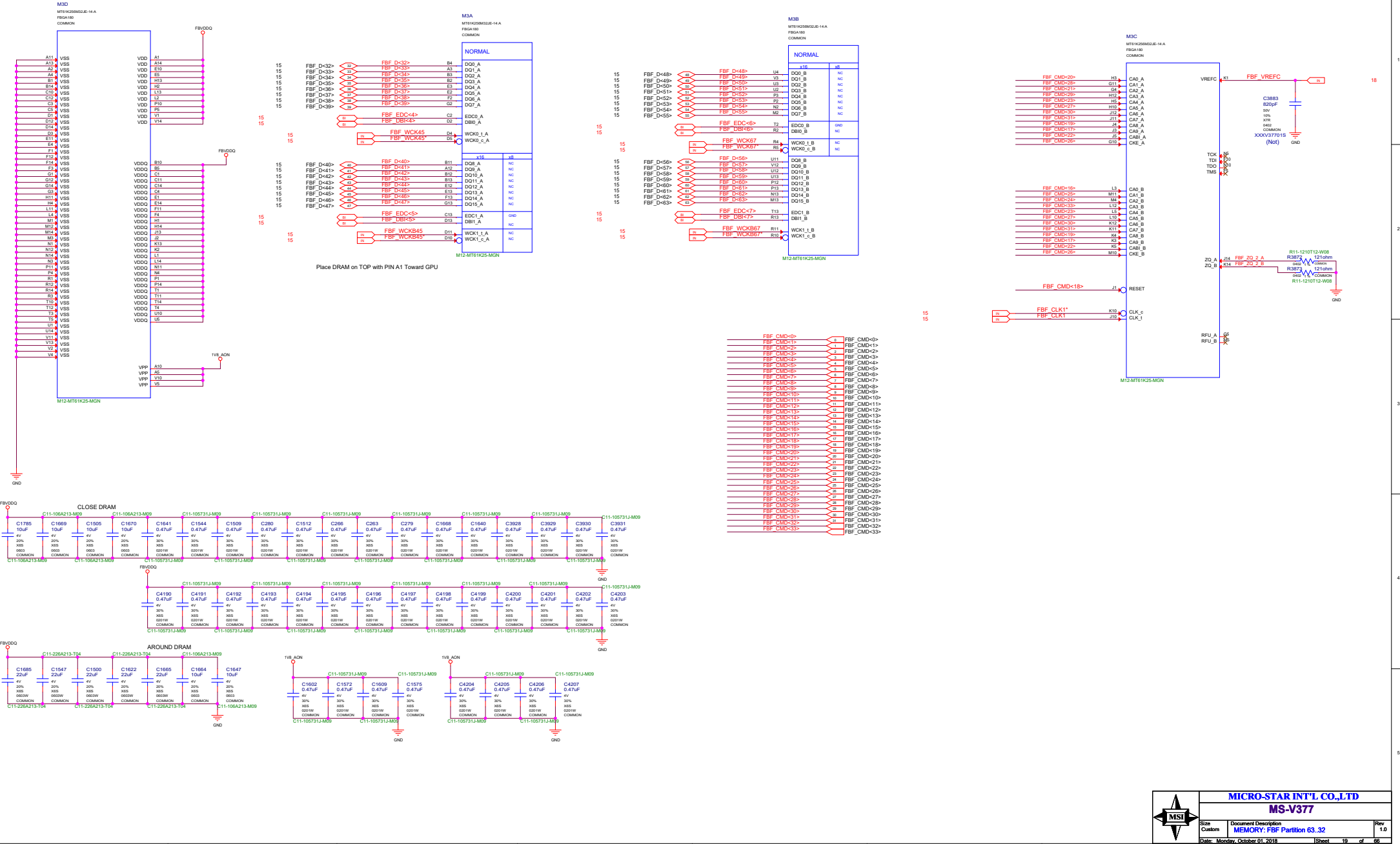
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MEMORY: FBE Partition 63..32

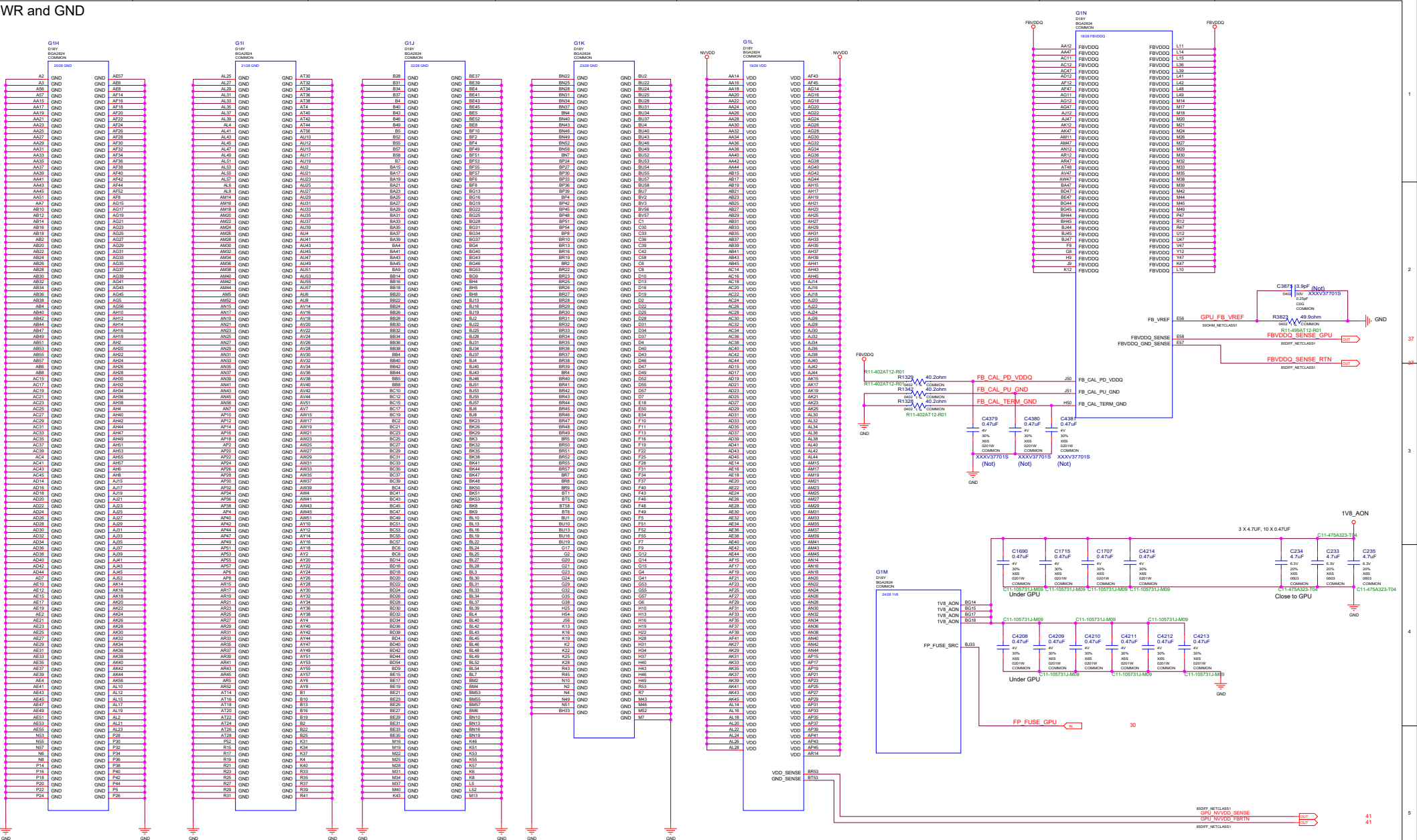




MEMORY: FBF Partition 63..32



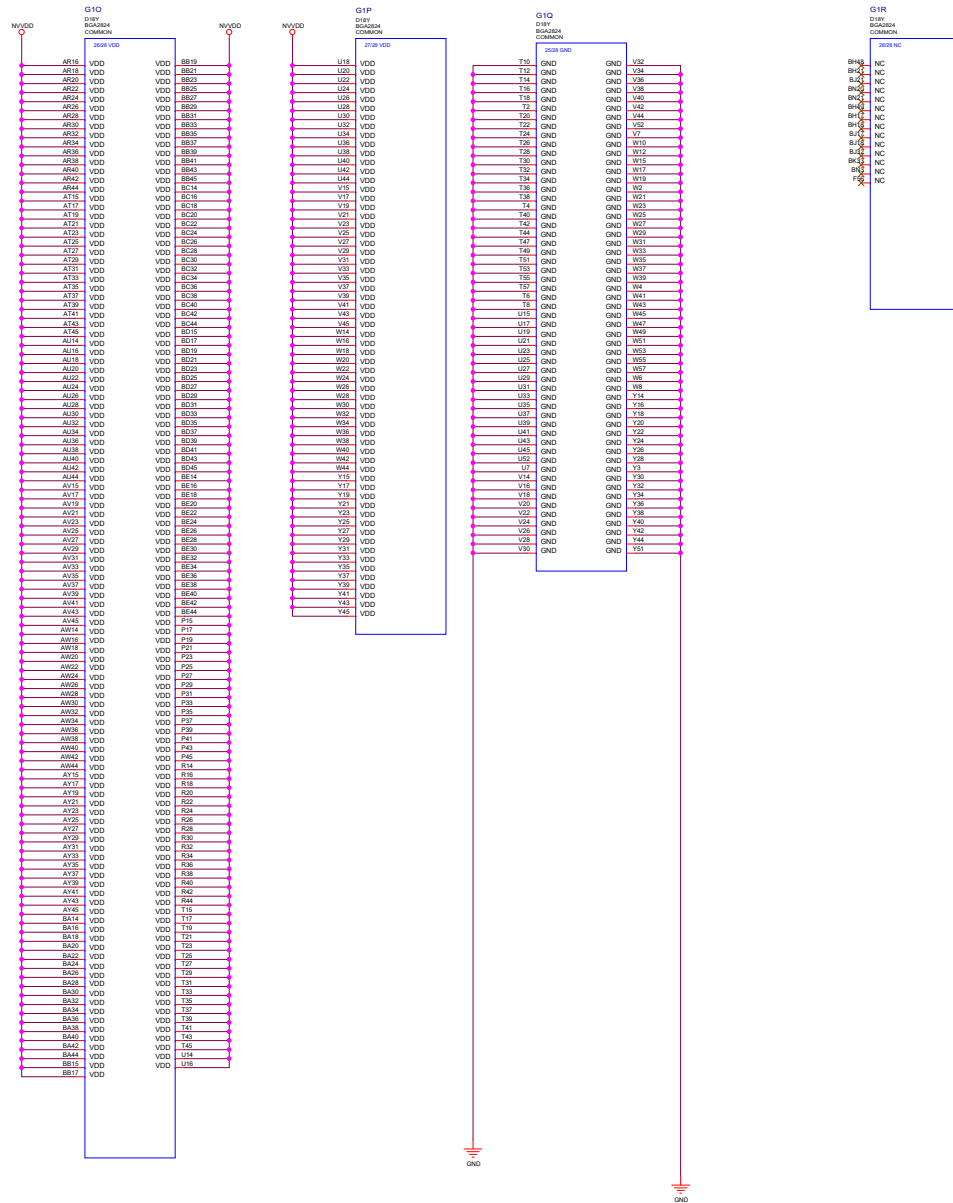
GPU PWR and GND



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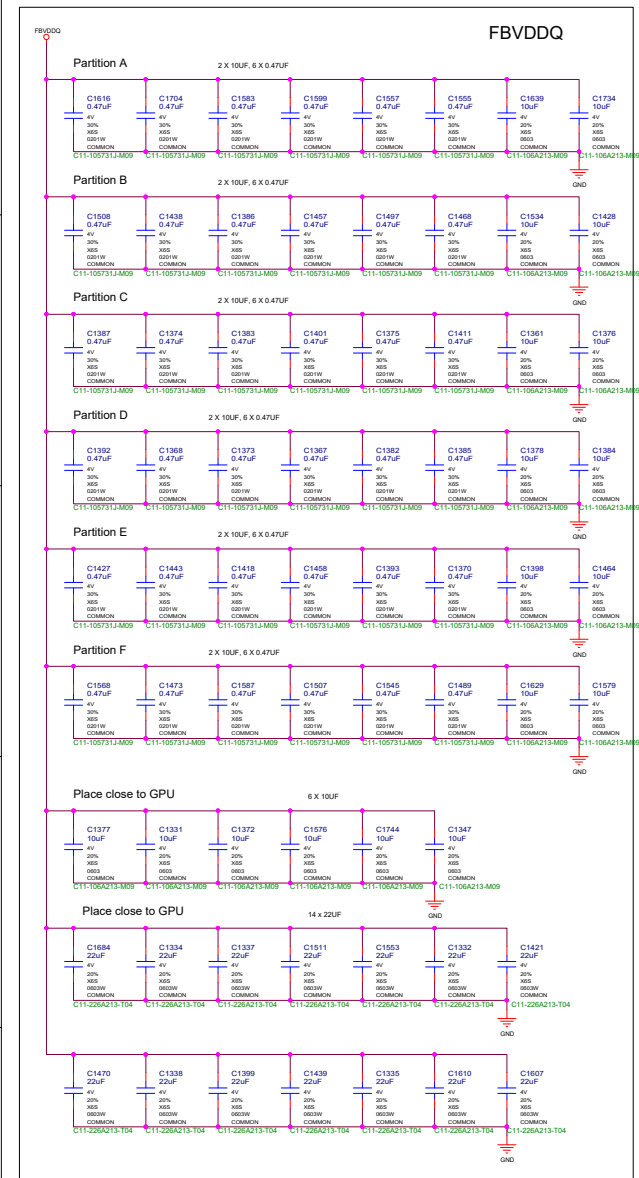
GPU PWR GND NCs



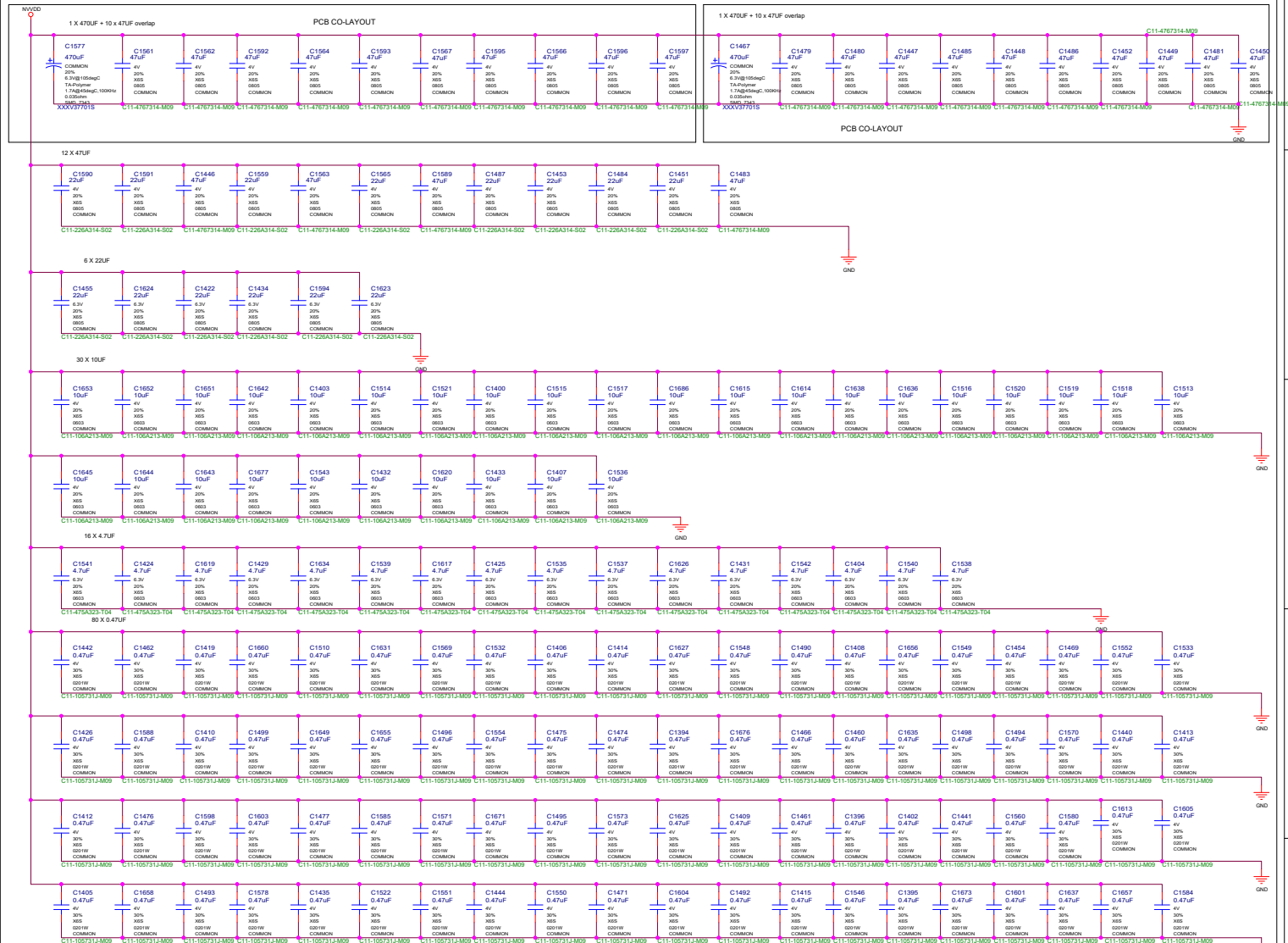
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Size Custom	Document Description GPU PWR GND NCs	Rev 1.0
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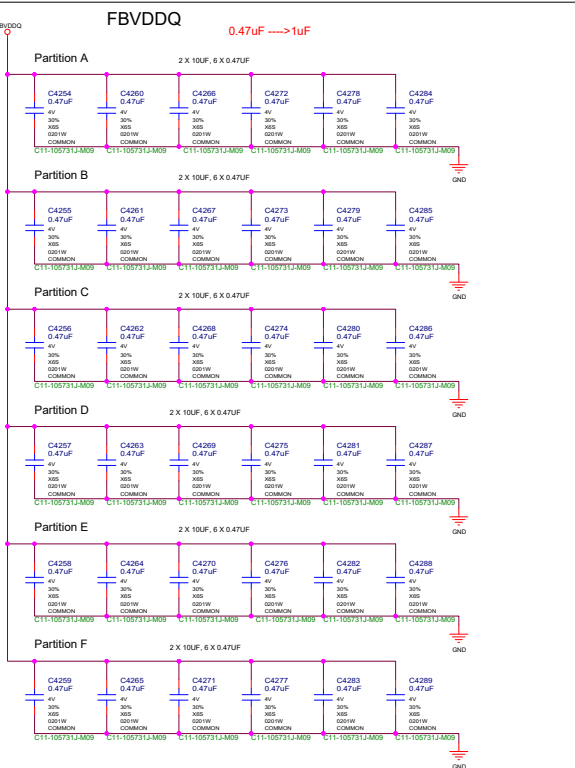
GPU Decoupling



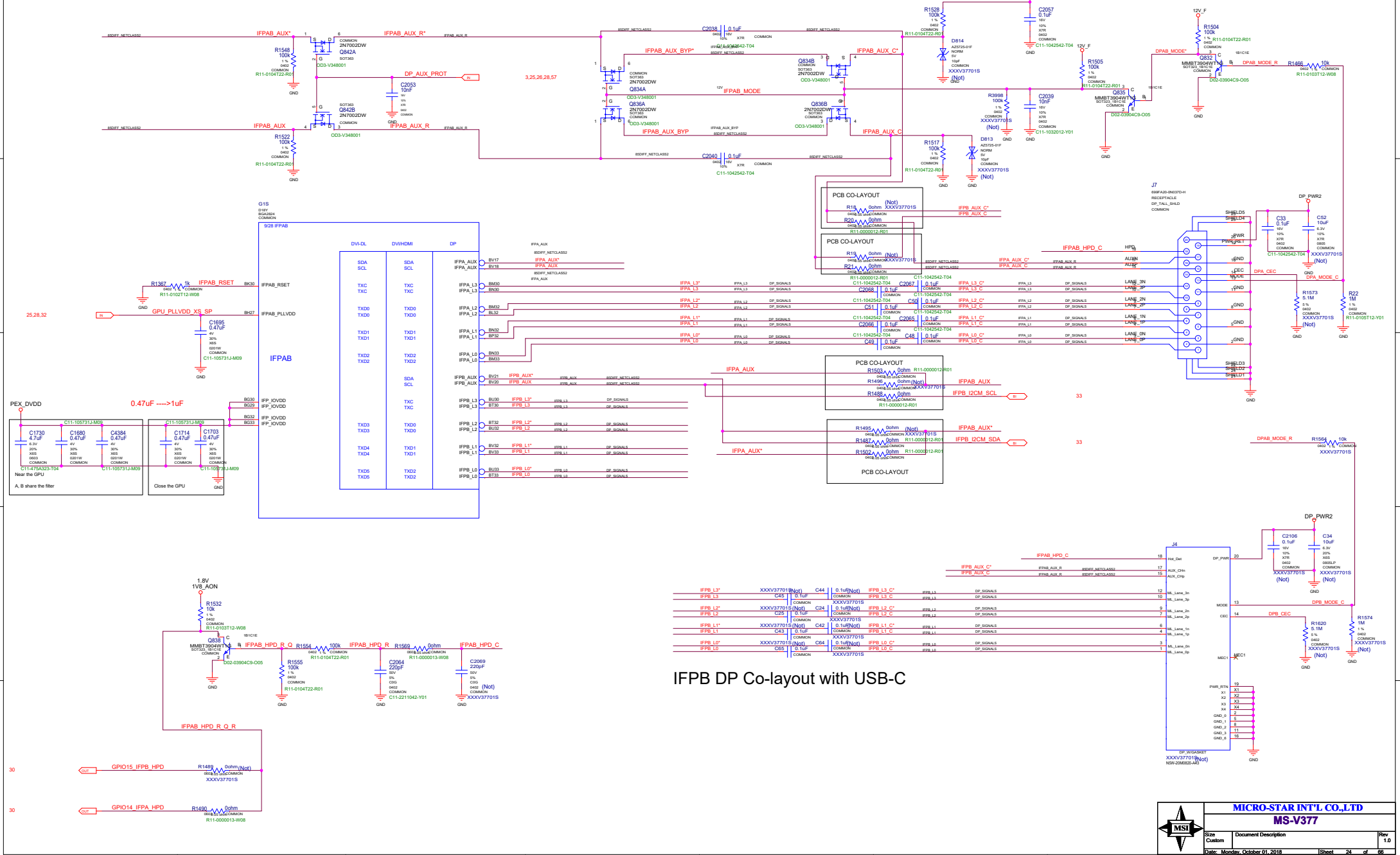
NVVDD

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GPU Decoupling

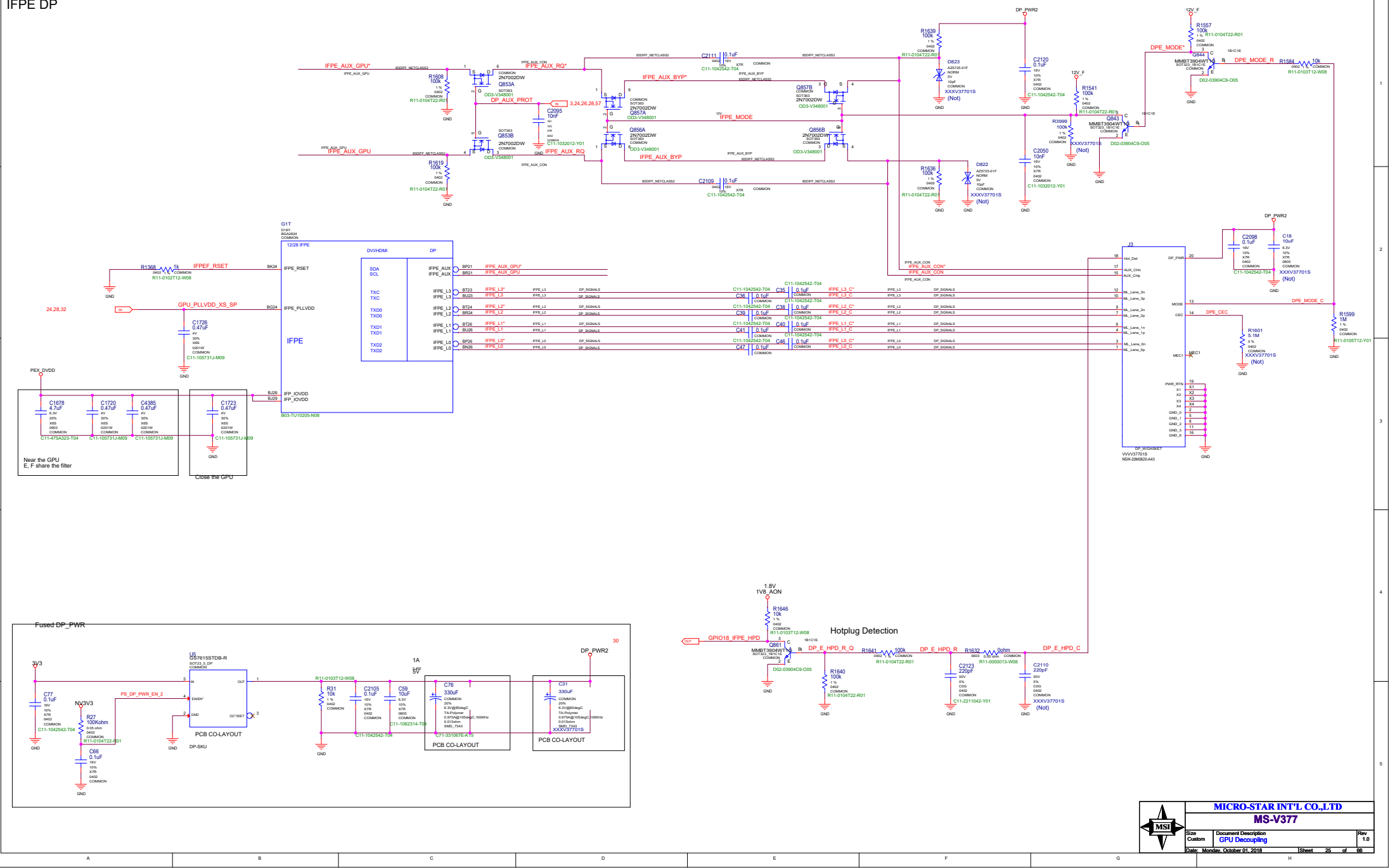


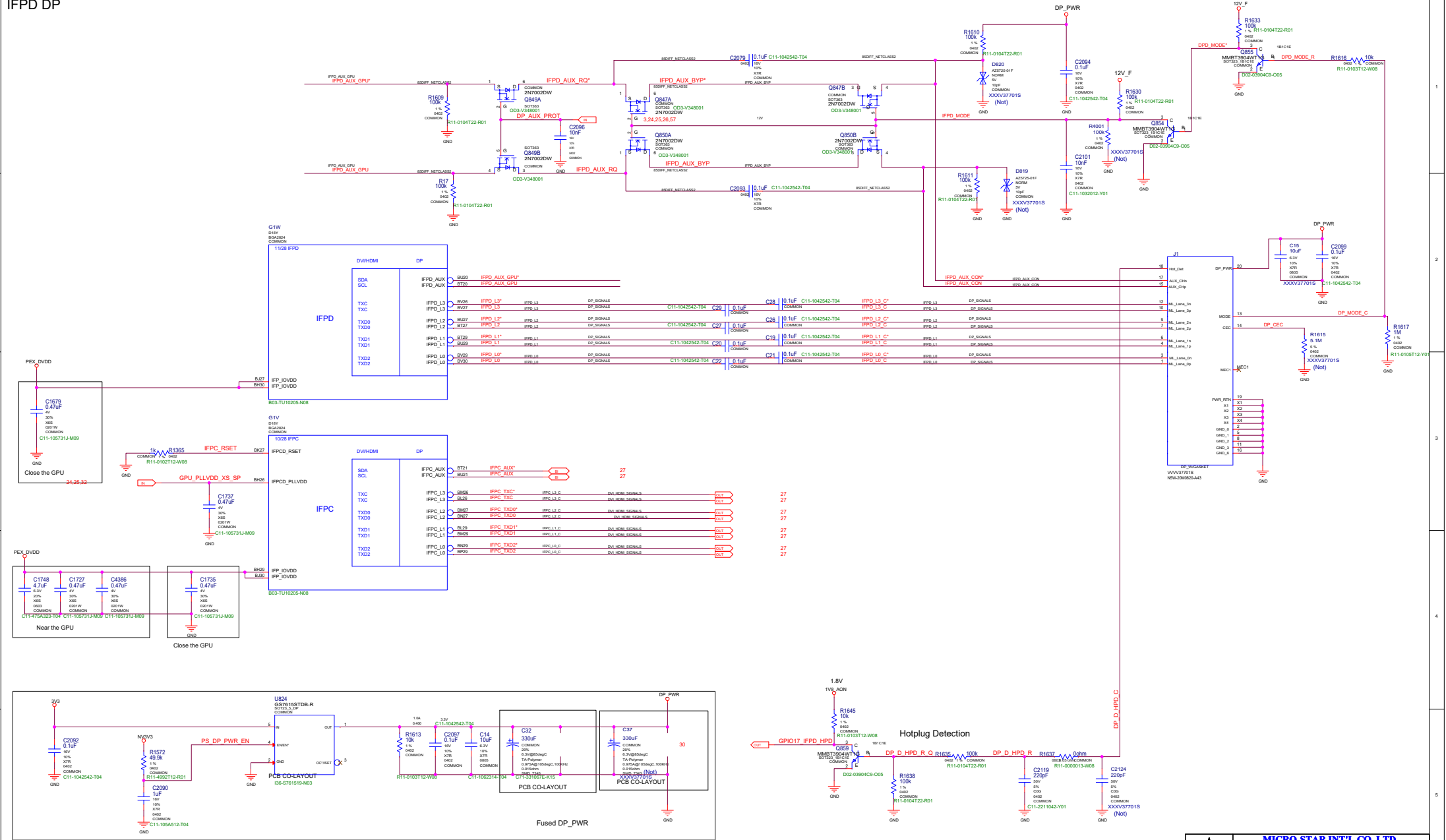
IFPAB TALL-DP



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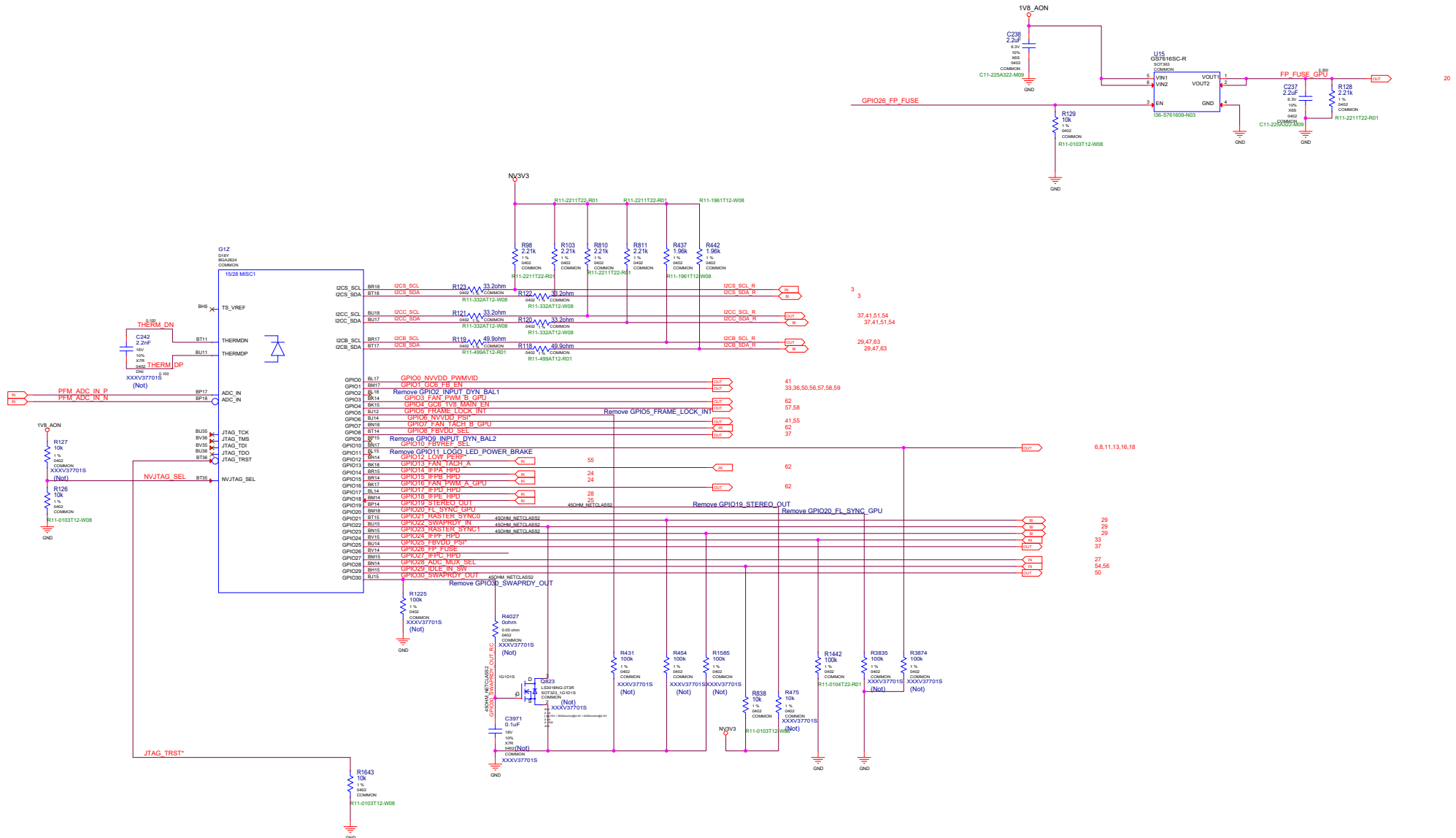
NVHS Interface and FRAME LOCK



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MISC1: Fan, Thermal, JTAG, GPIO, STEREO



MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]
L	L	L	00000
L	L	H	00001
L	H	L	00010
L	H	H	00011
H	L	L	00100
H	L	H	00101
H	H	L	00110
H	H	H	00111
L	L	M	01000
L	M	L	01001

DEFAULT

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

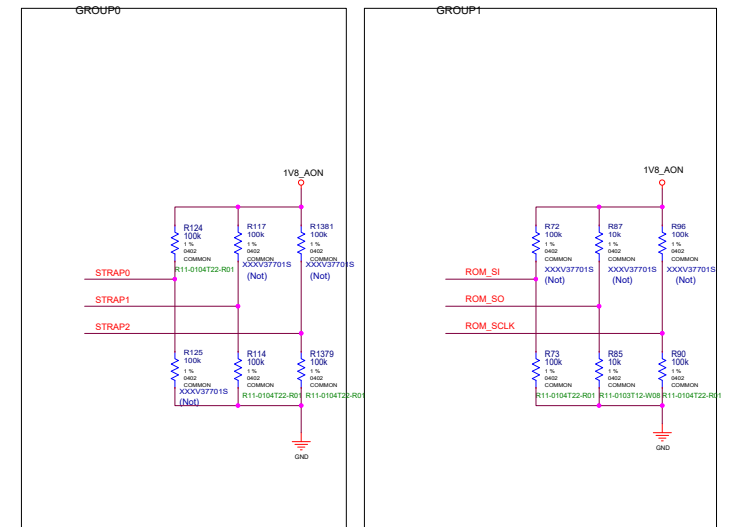
ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	H	XXX0	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

Default

SKU 200

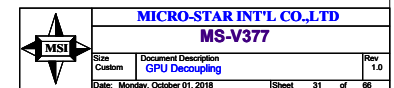
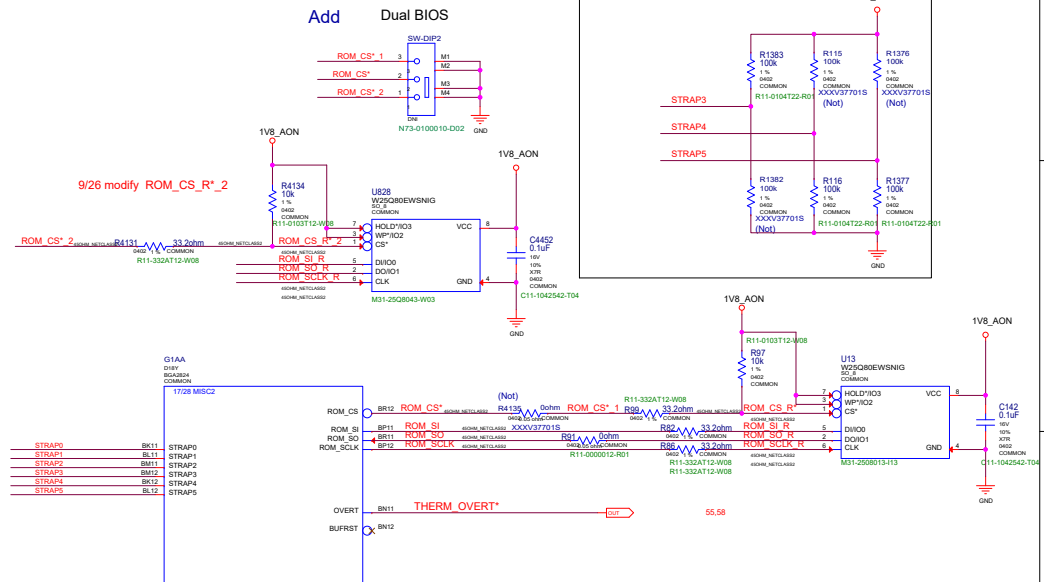


```
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

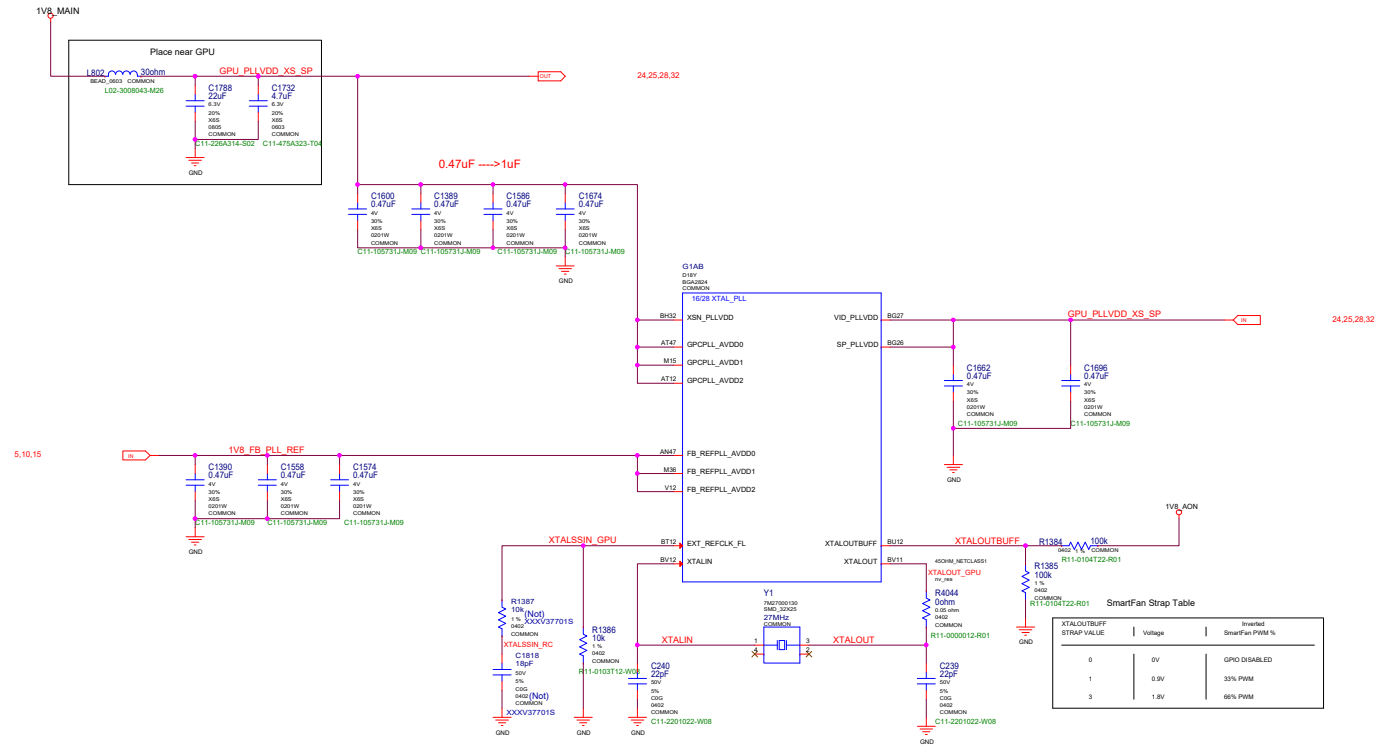
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

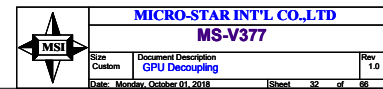
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE
```



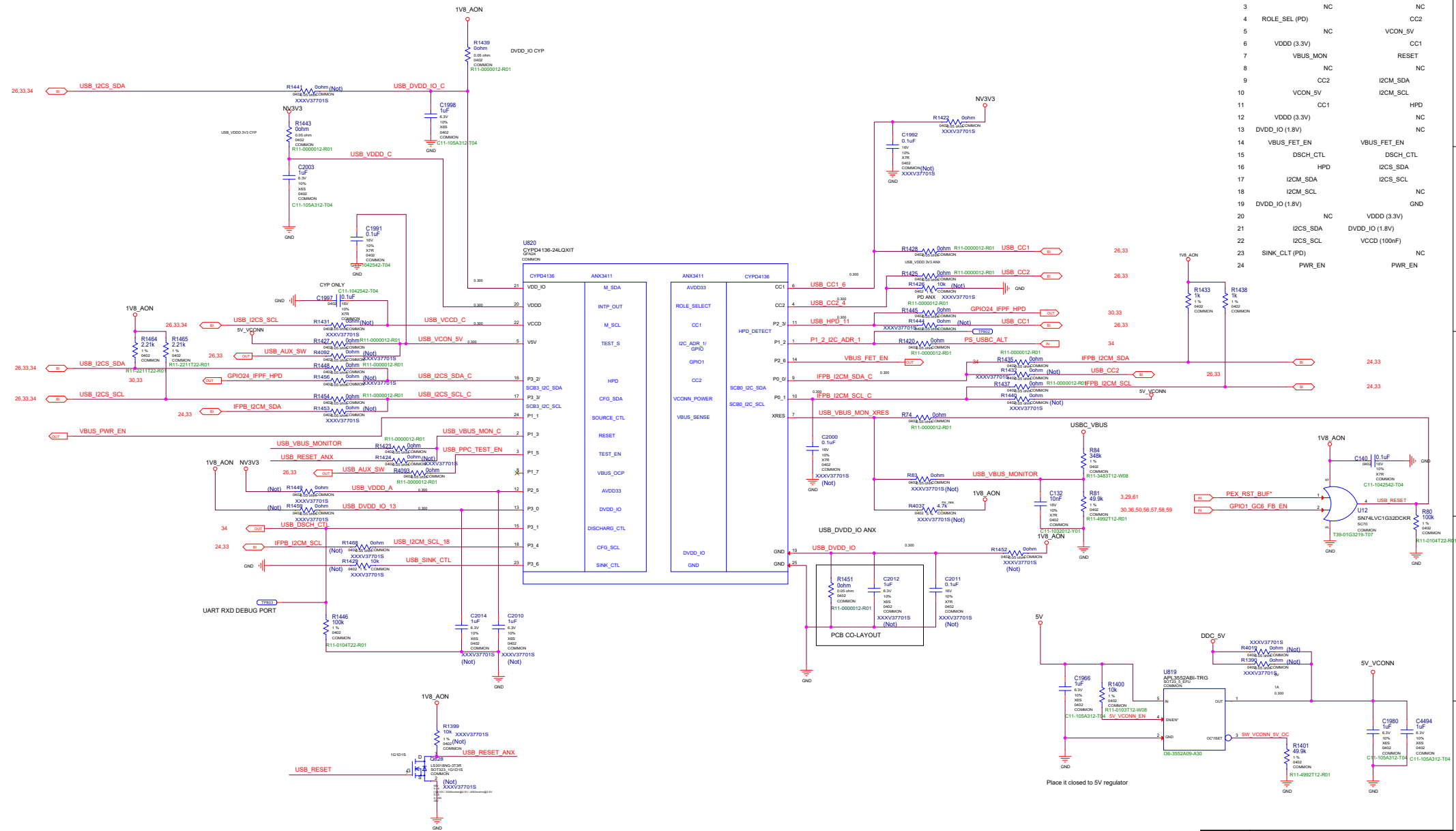
MISC2: XTAL. PLL



XTALOUTBUFF STRAP VALUE	Voltage	Inverted SmartFan PWM %
0	0V	GPIO DISABLED
1	0.9V	33% PWM
3	1.8V	66% PWM



MISC: USB PPC



PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (1000mF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN



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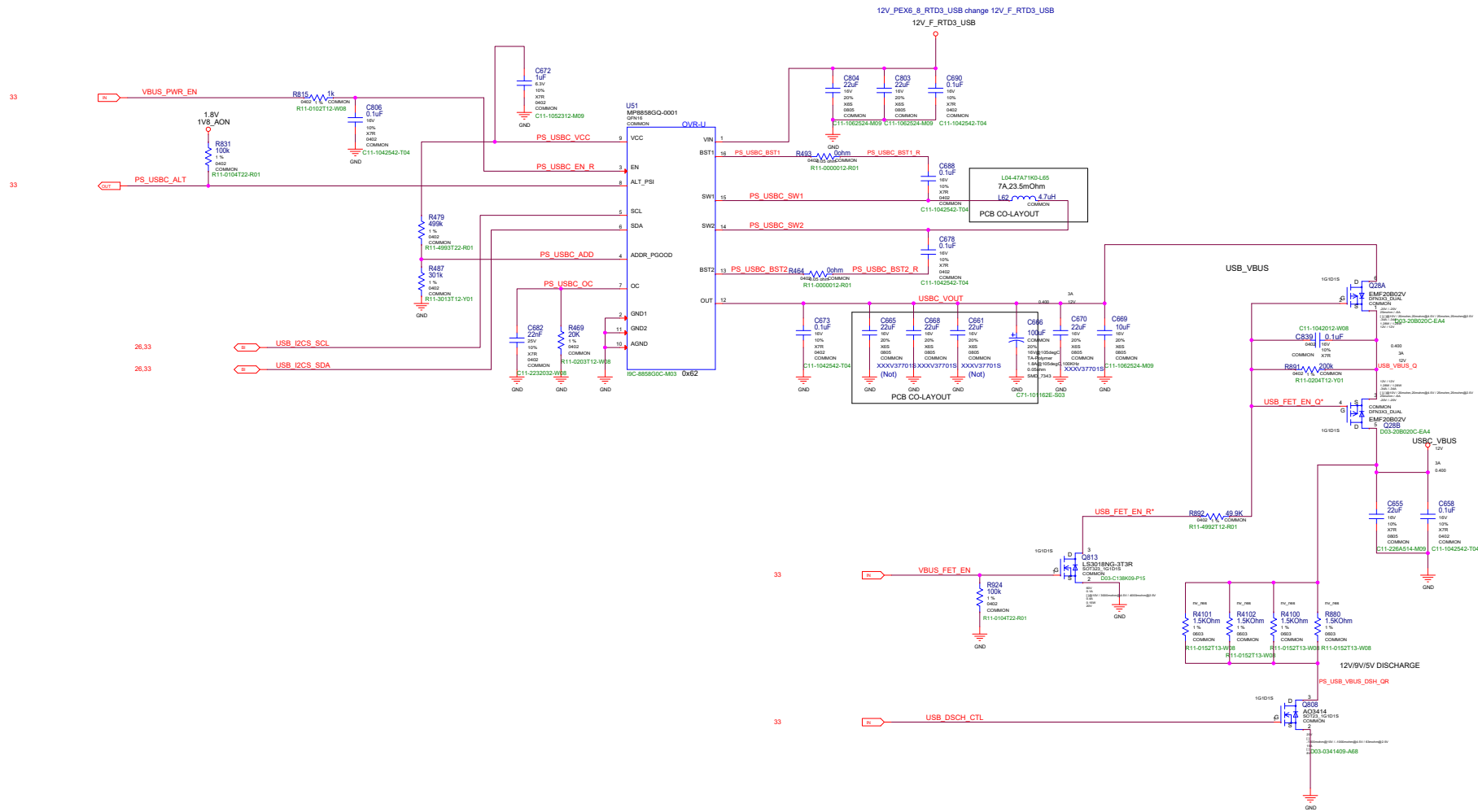
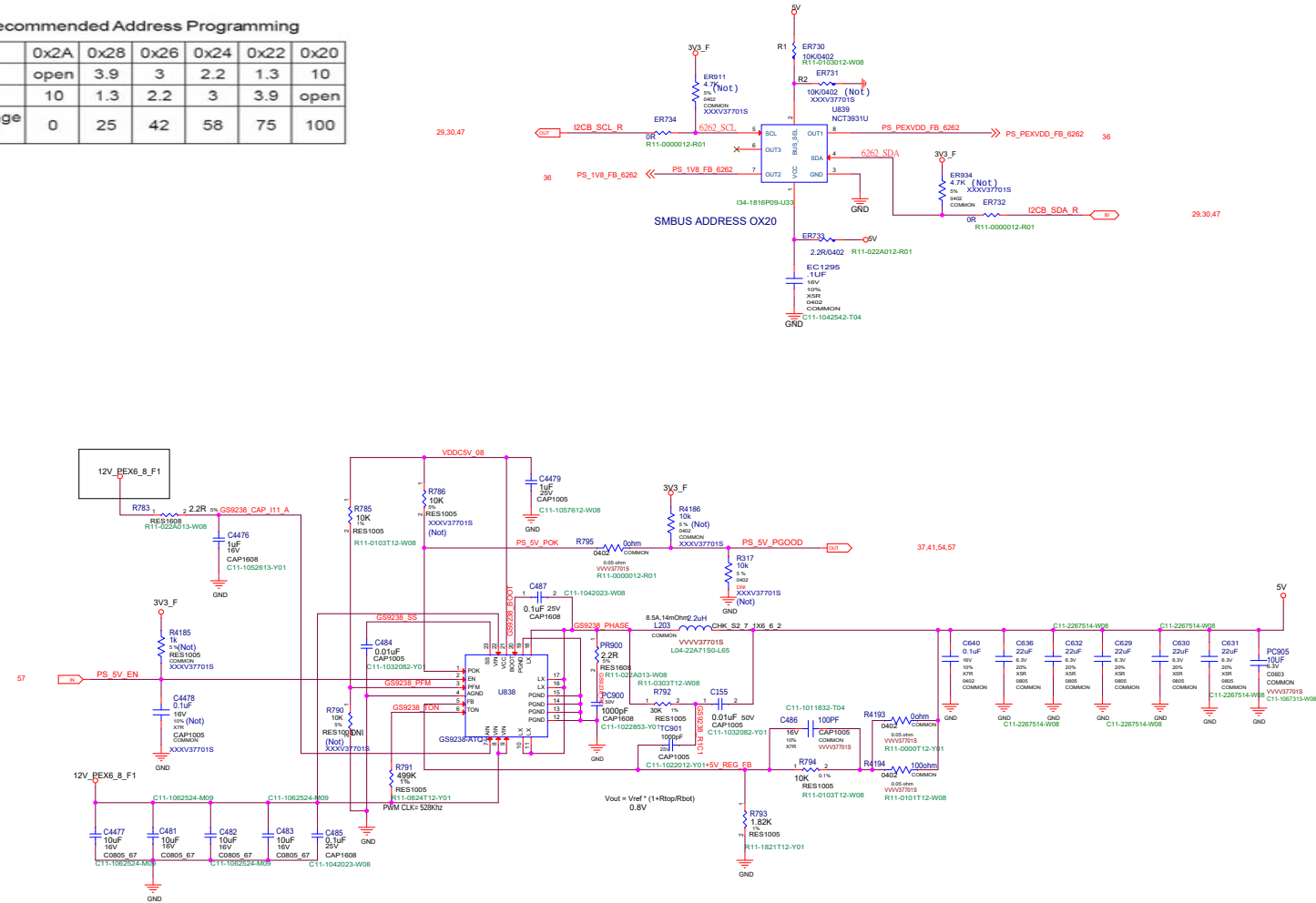


Table 1. Recommended Address Programming

Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (k Ω)	open	3.9	3	2.2	1.3	10
R2 (k Ω)	10	1.3	2.2	3	3.9	open
BUS_SEL Voltage (% of VCC)	0	25	42	58	75	100

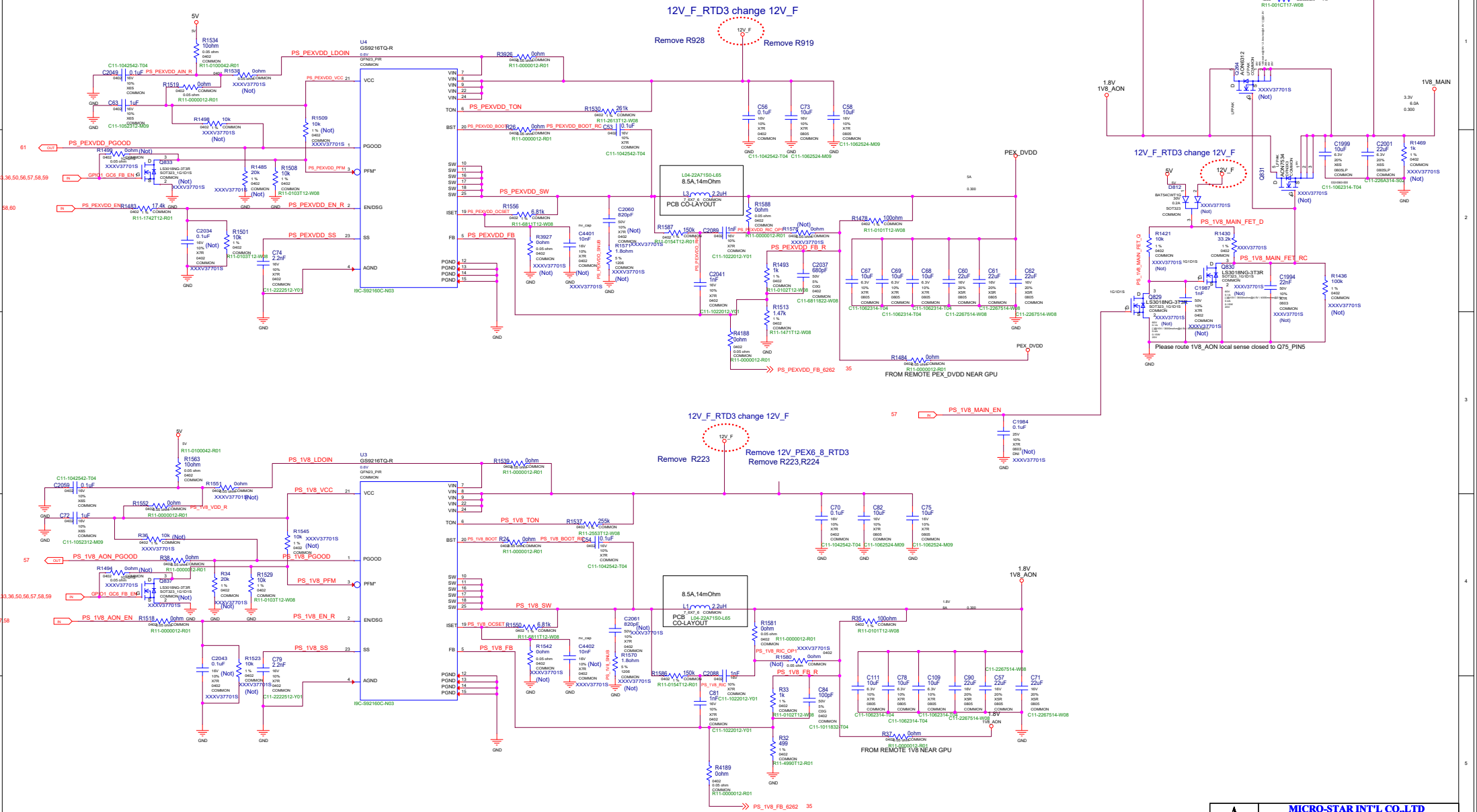


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PS: PEXVDD 1V8 Rail



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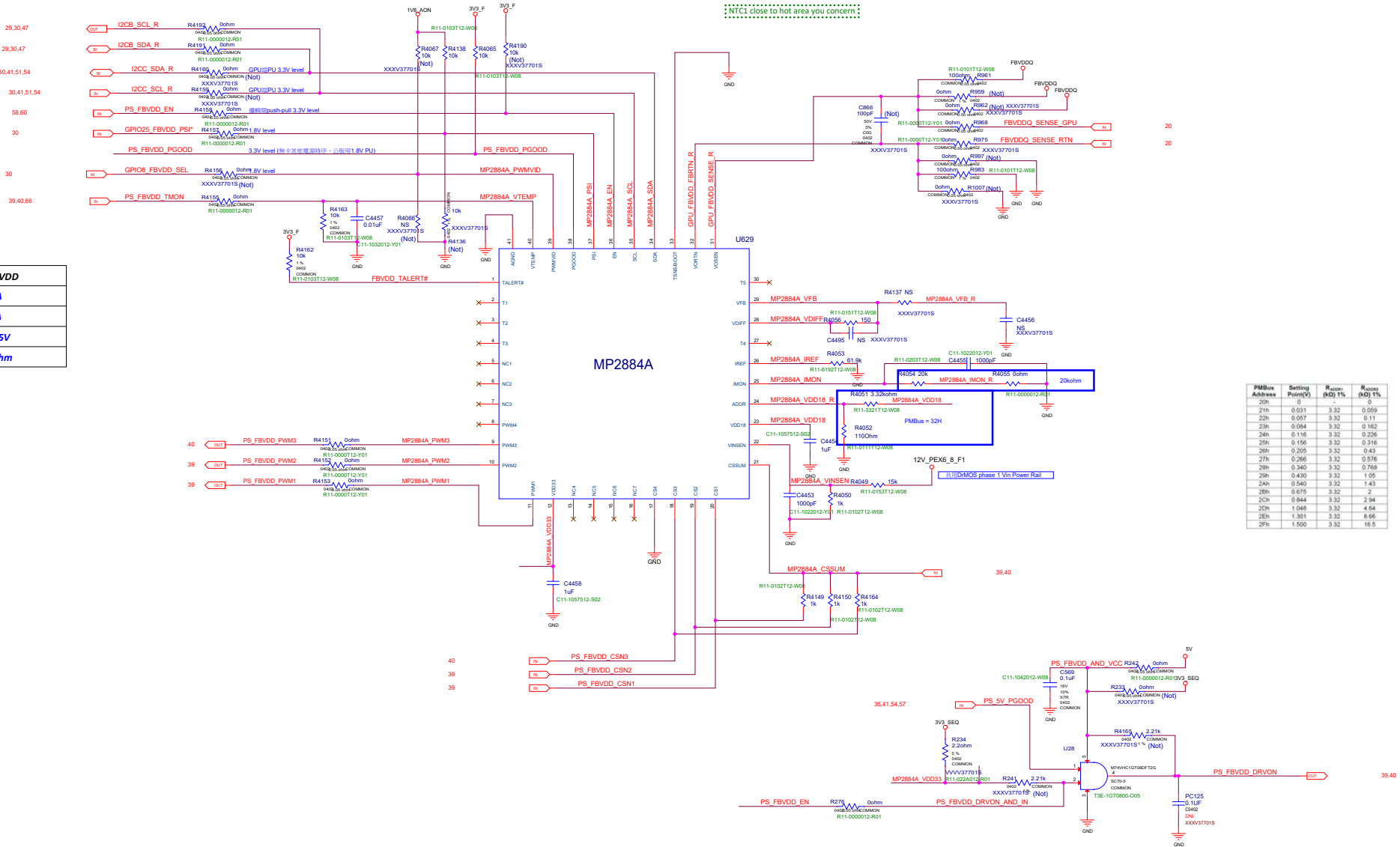
PS: FBVDD Controller

<i>EN Type</i>	<i>R3</i>
<i>Open Drain</i>	<i>10k</i>
<i>Push Pull</i>	<i>NS</i>

<i>PSI</i>	<i>Mode</i>
<i>High</i>	<i>High Phase Count</i>
<i>Hi-Z</i>	<i>Auto Power Mode</i>
<i>Low</i>	<i>Low Phase Count</i>

PWMVID	Vout
High	VID in 24h
Hi-Z	VID in 21h
Low	VID in 1fh

	+NVVDD
TDC	??A
IccMax	??A
Vboot	1.35V
Load Line	0mohm



PMBus Address	Setting Point(V)	$R_{DS(on)}$ (mΩ) 1%	$R_{DS(on)}$ (mΩ) 1%
20n	0	3.32	0.0569
21n	0.031	3.32	0.11
22n	0.057	3.32	0.162
23n	0.084	3.32	0.226
24n	0.116	3.32	0.316
25n	0.156	3.32	0.43
26n	0.205	3.32	0.576
27n	0.266	3.32	0.768
28n	0.340	3.32	1.05
29n	0.430	3.32	1.43
30n	0.540	3.32	1.94
31n	0.675	3.32	2.64
32n	0.844	3.32	4.64
20h	1.048	3.32	8.66
21h	1.301	3.32	16.5
22h	1.500	3.32	



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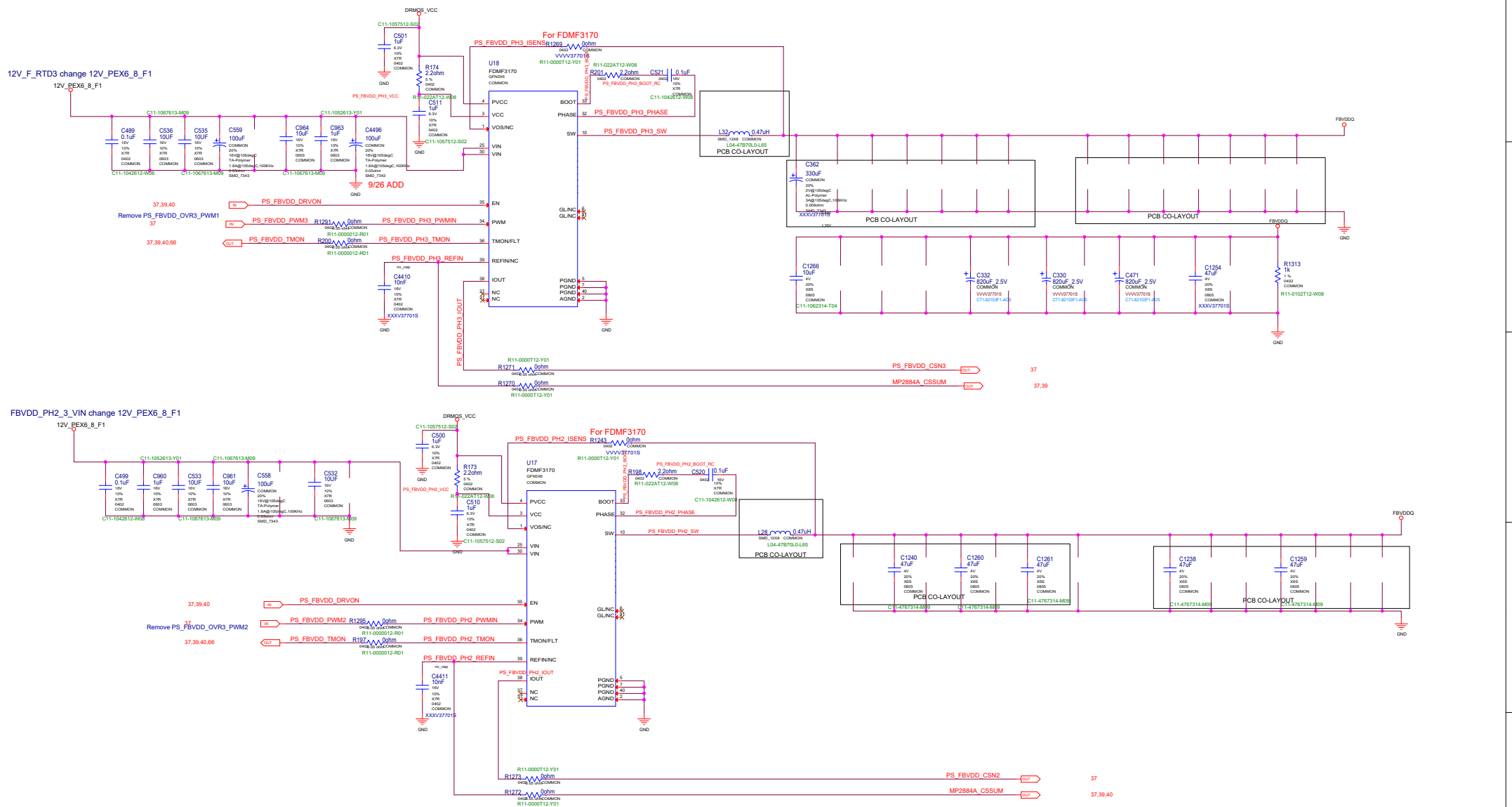
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PS: FBVDD Controller OVR3



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PS: FBVDD PH2,3

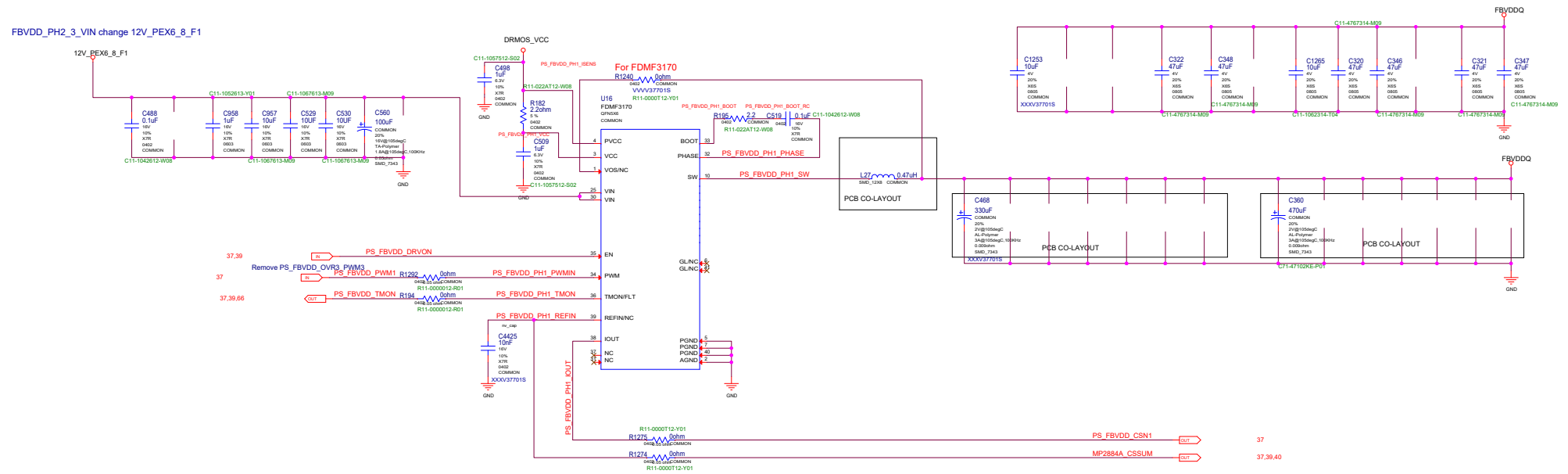


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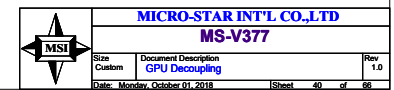
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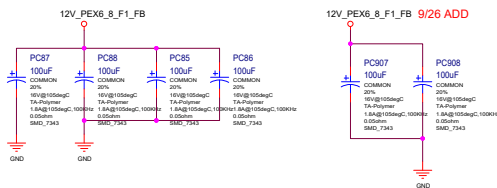
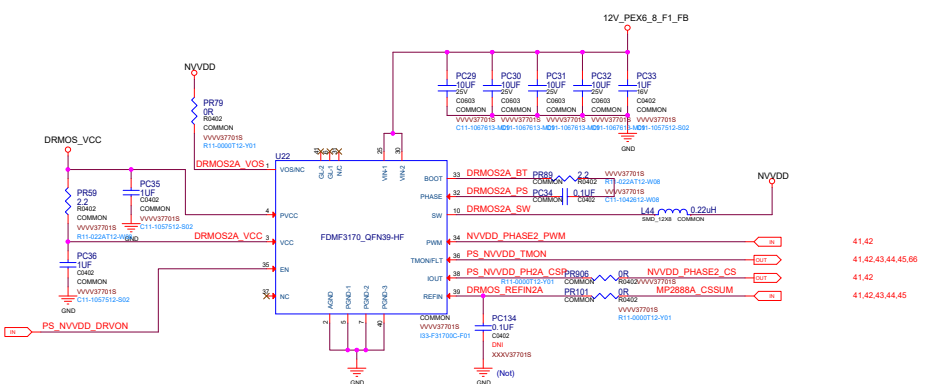
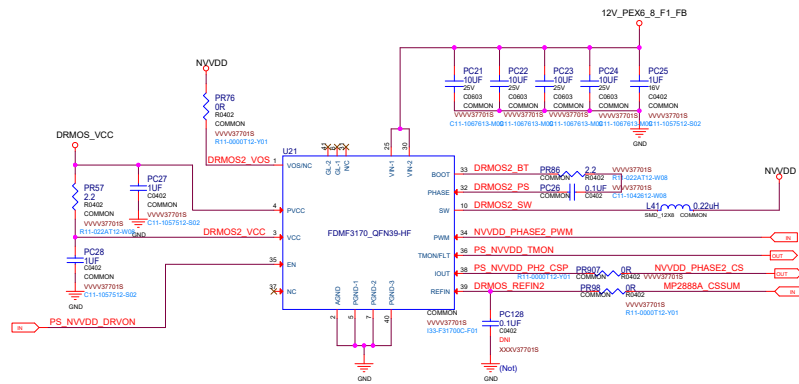
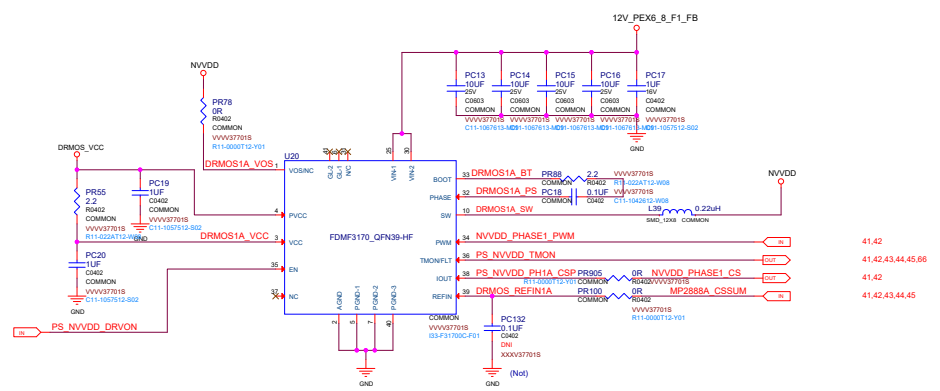
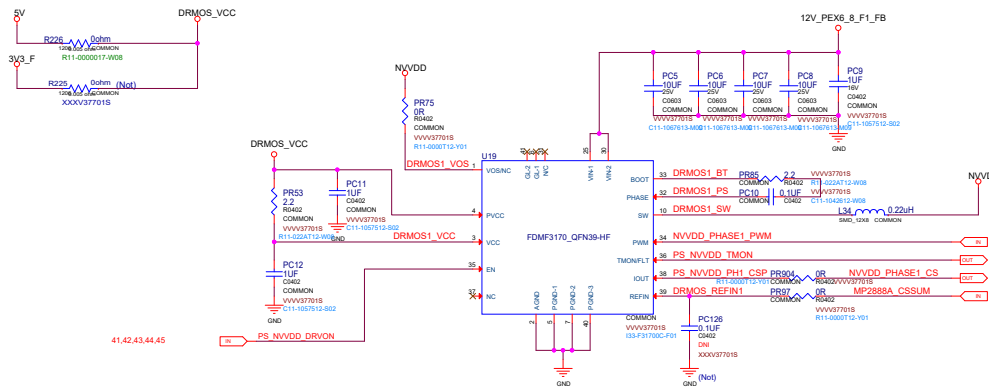
PS: FBVDD PH1



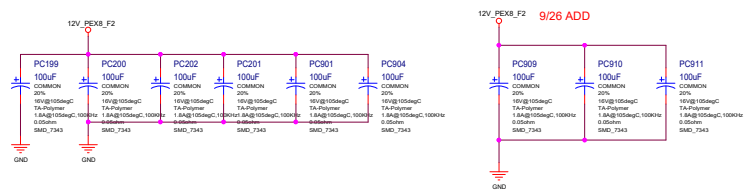
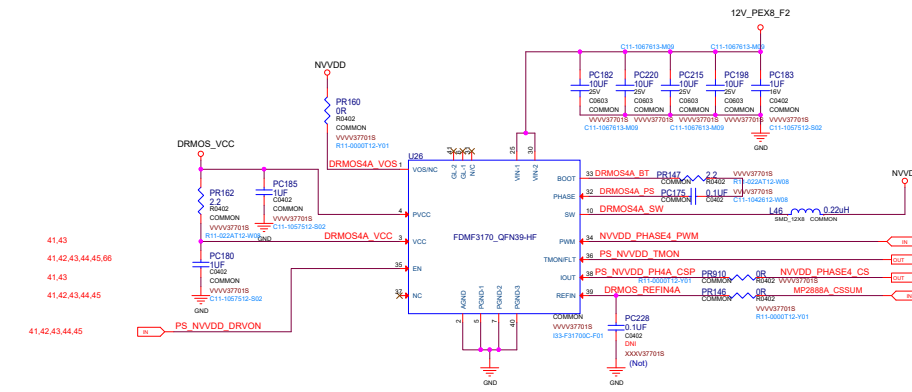
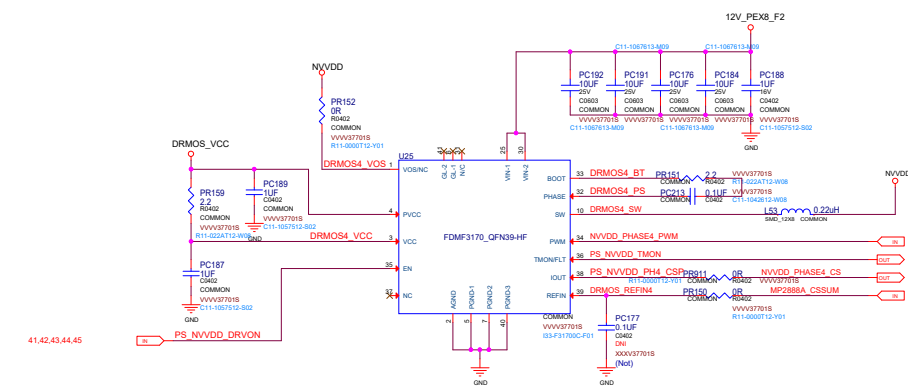
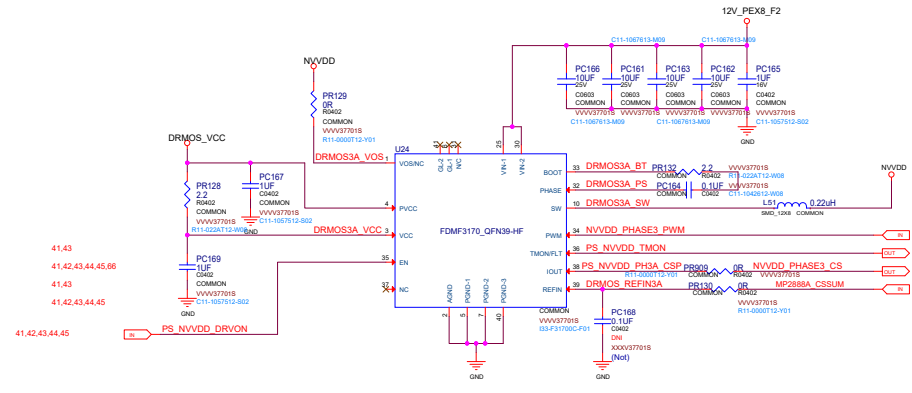
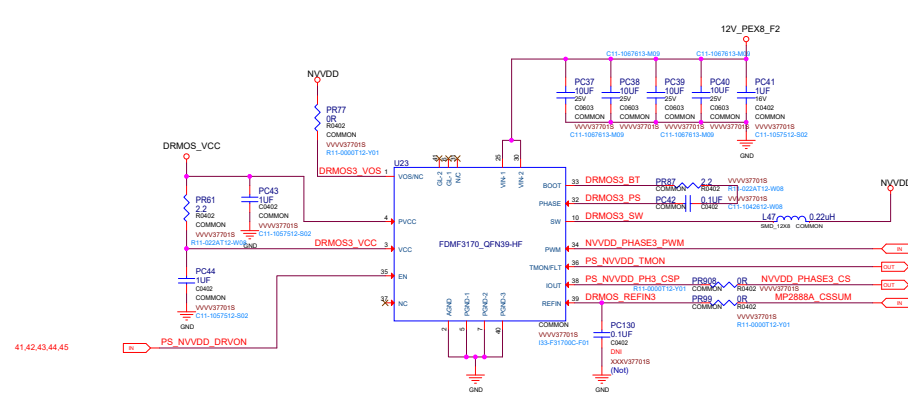
Remove 12V_PEX_FB ---->FBVDD_PH2_3_VIN circuit

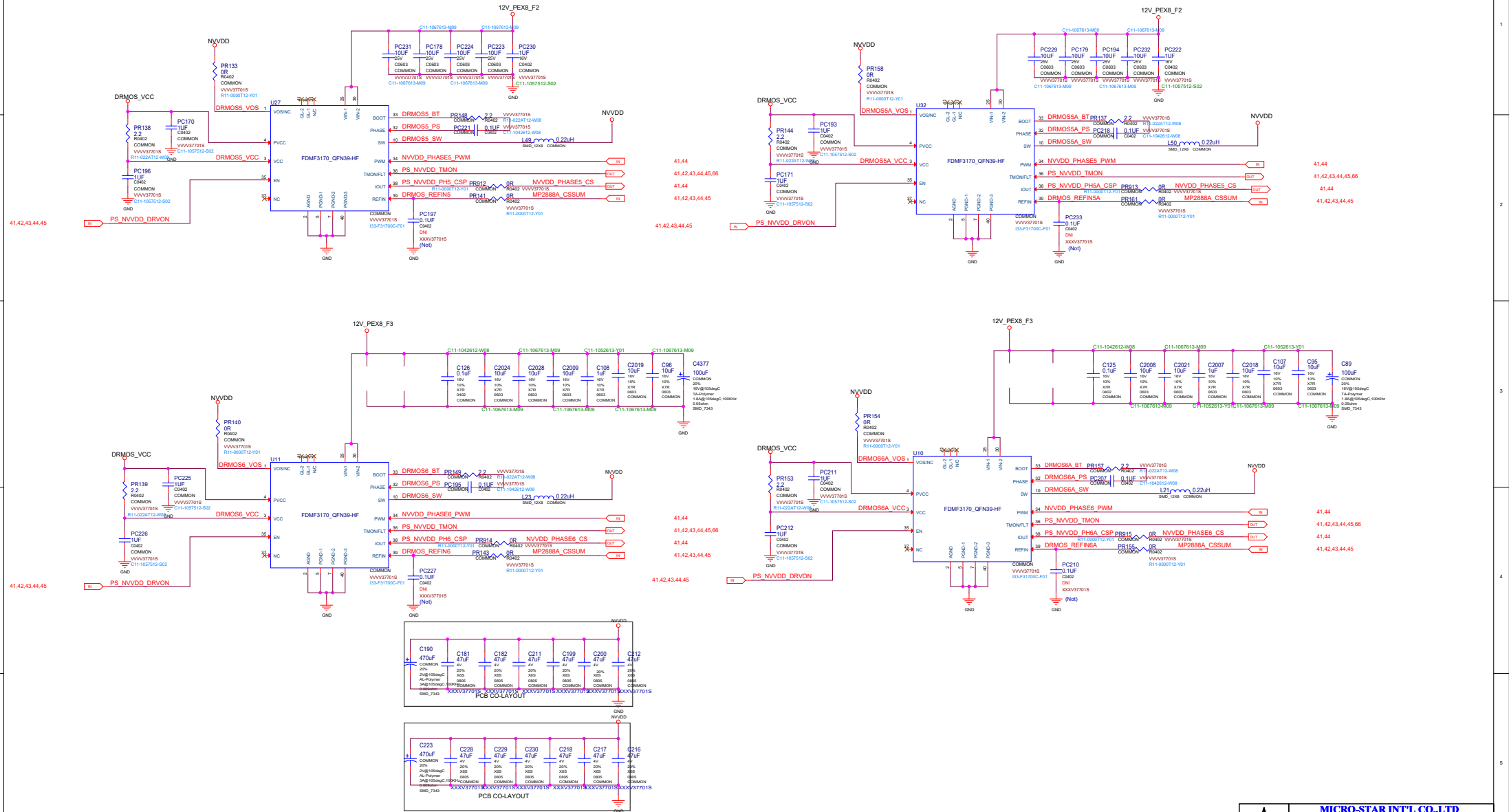


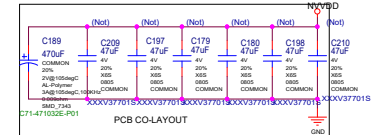
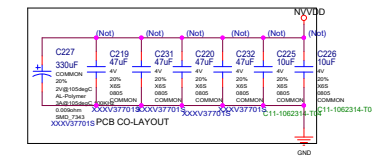
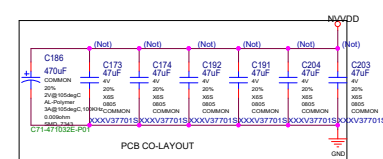
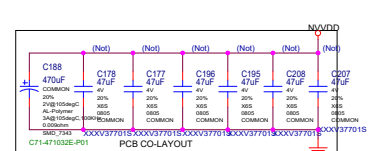
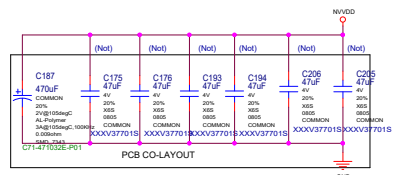
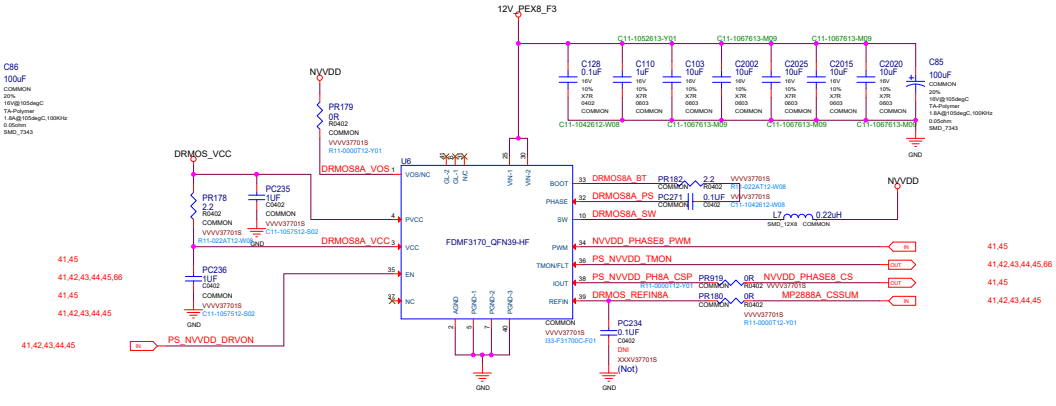
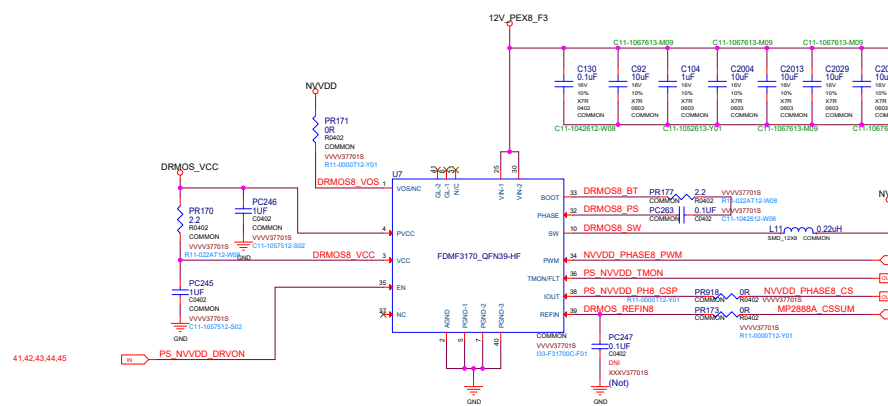
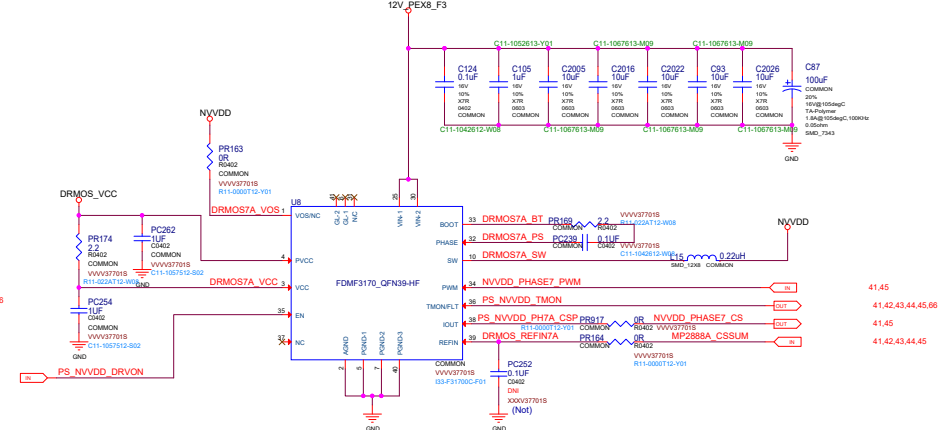
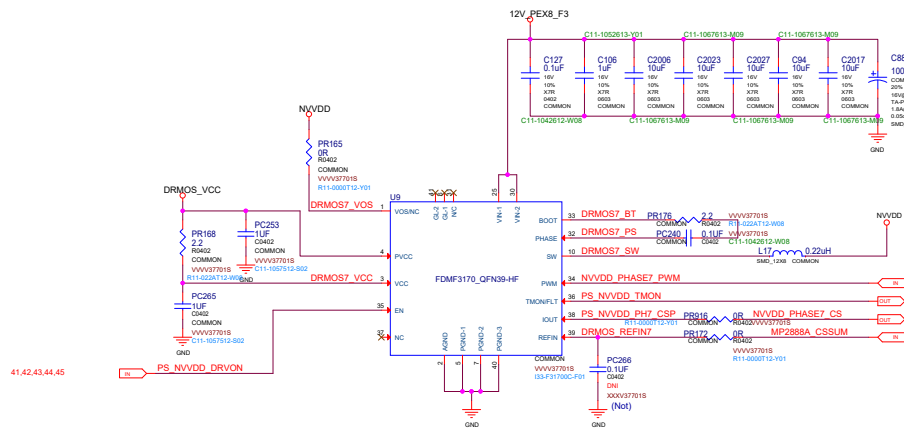
PS: NVVDD Phase 1~4

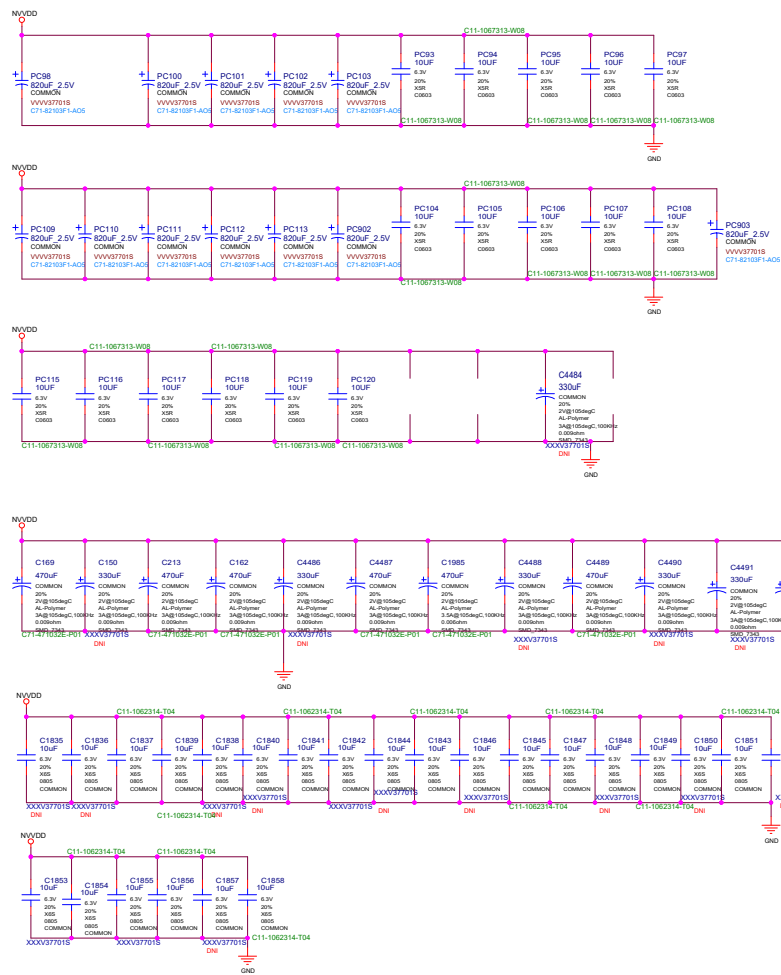


PS: NVVDD Phase 5~8





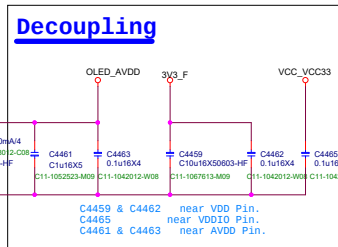
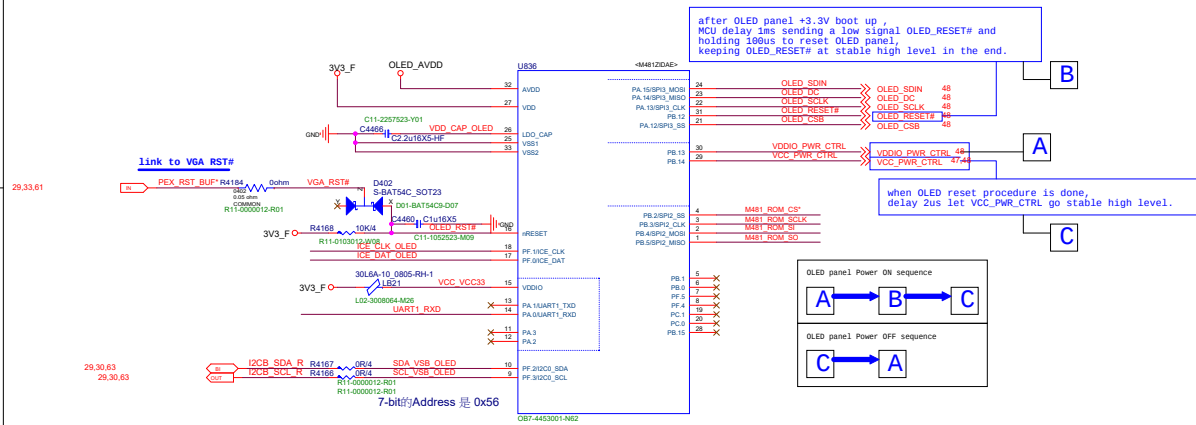




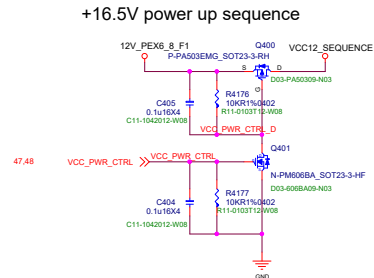
MICRO-STAR INT'L CO.,LTD

MS-V377

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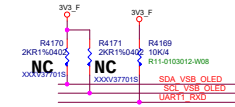
MPS1542 BUCK BOOST FOR OLED POWER 12Vin 16.5Vout



PIN FUNCTIONS

Pin #	Name	Description
1	COMP	Compensation Pin. Connect a capacitor and resistor in series to ground for loop stability.
2	FB	Feedback Input. Reference voltage is 1.25V. Connect a resistor divider to this pin.
3	EN	Regulator On/Off Control Input. A high input at EN turns on the converter, and a low input turns it off. When not used, connect EN to the input source (through a 100kΩ pull-up resistor if V_{IN} is 6V) for automatic startup. EN cannot be left floating.

I2C and UART Reserve

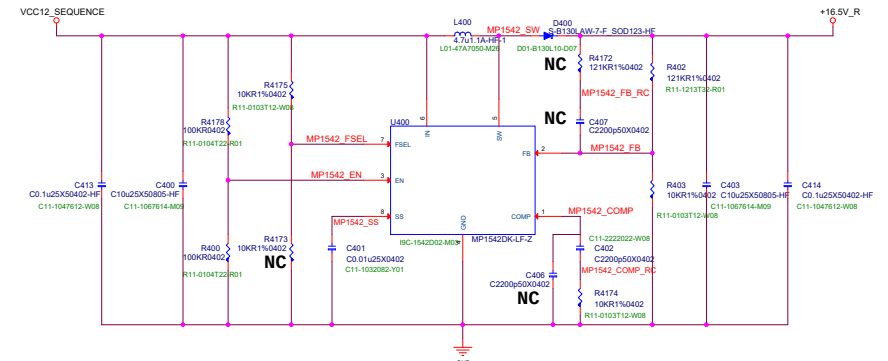
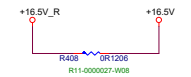
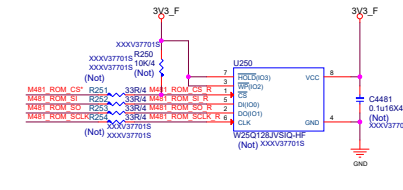


```
pull high I2C don't leave it floating,
once R23 + R24 removed
pull high UART Rx don't leave it floating
```

FW update



External 3.3V SPI ROM,128M(16Mx8bit)



[illegible]

A		B		C		D		E		F		G		H	
PS: NVVDD PH 13,14															
1															
2															
3															
4															
5															
A		B		C		D		E		F		G		H	



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PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

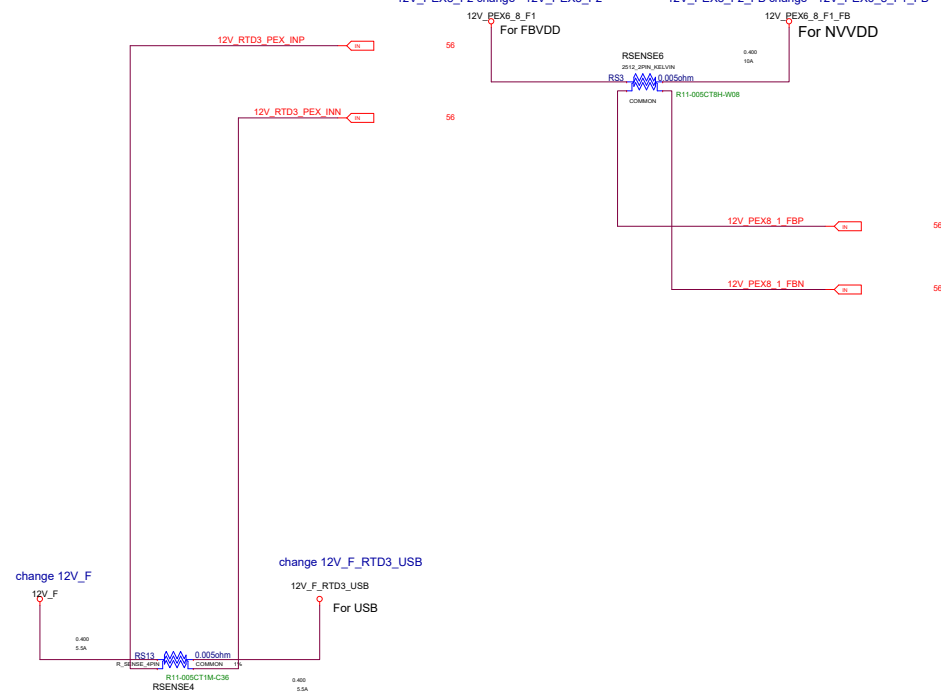
Remove 12V_F_RTD3 circuit

AND GATE LOGIC FOR P-BOARD			
GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

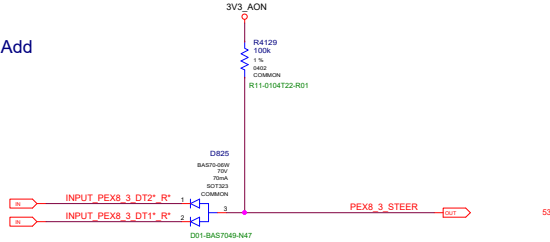
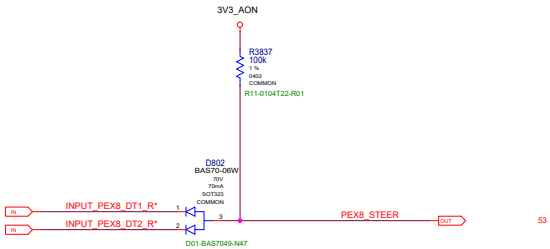
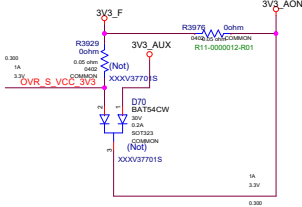
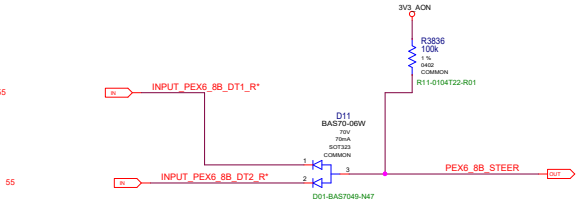
Remove 3V3_RTD3 circuit



12V_PEX8_F2 change 12V_PEX8_F2 12V_PEX8_F2_FB change 12V_PEX6_8_F1_FB



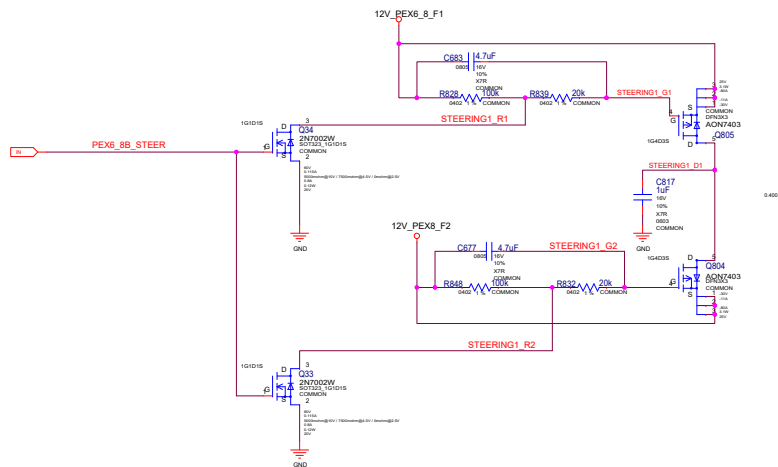
PS: Input Switch Rail Balance



Remove NVVDD VIN change circuit

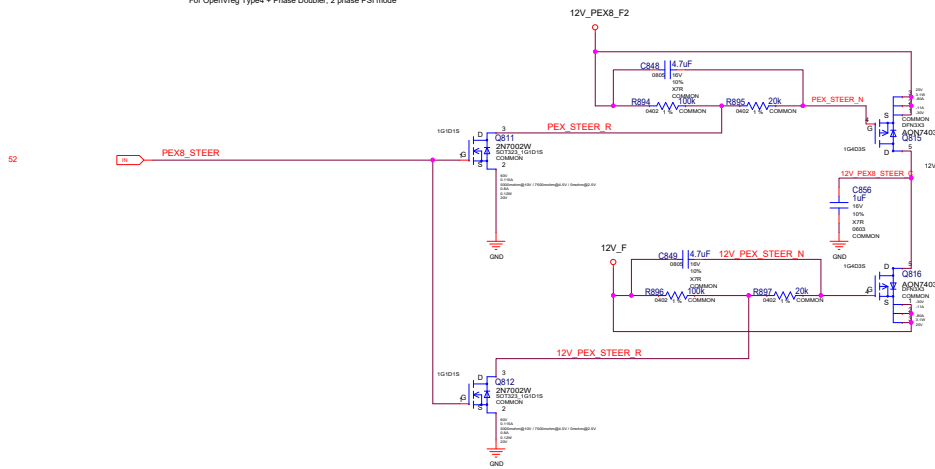
Add

12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA

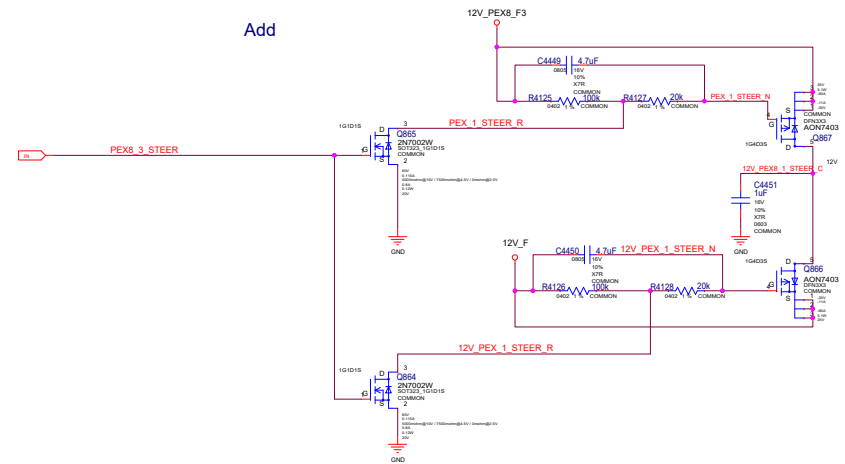


12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

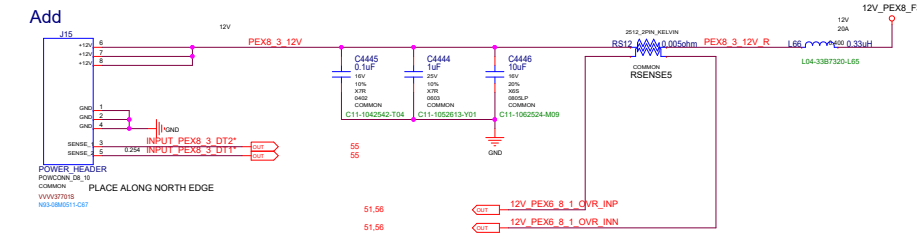
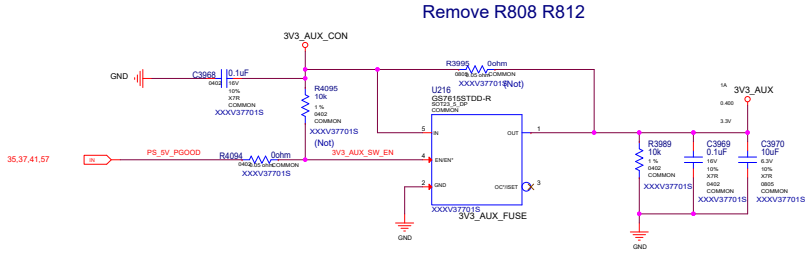
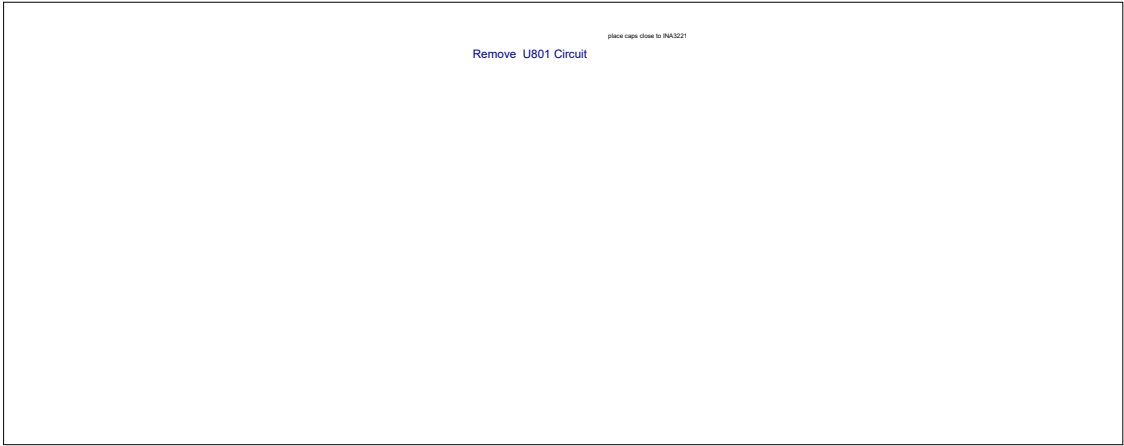
For OpenVing Type4 + Phase Doubler, 2 phase PSI mode



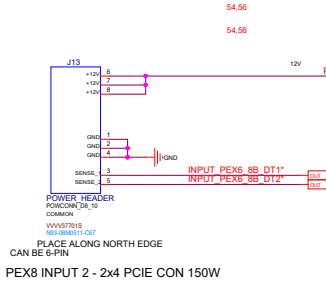
Add



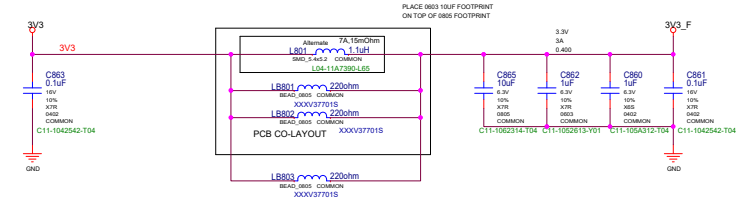
PS: Inputs, Filtering, and Monitoring



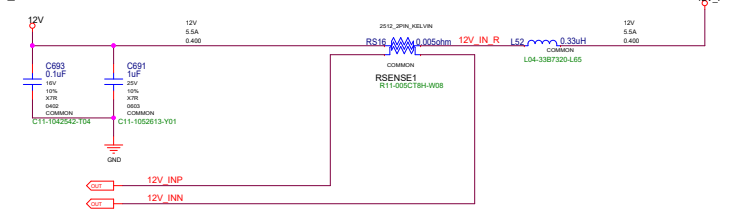
PEX8 INPUT 1 - 2x3 PCIE CON 75W



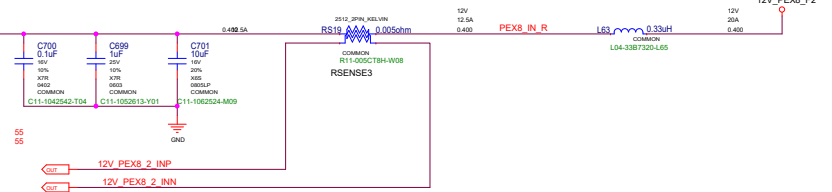
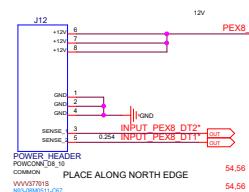
PEX 3V3 INPUT - 10W



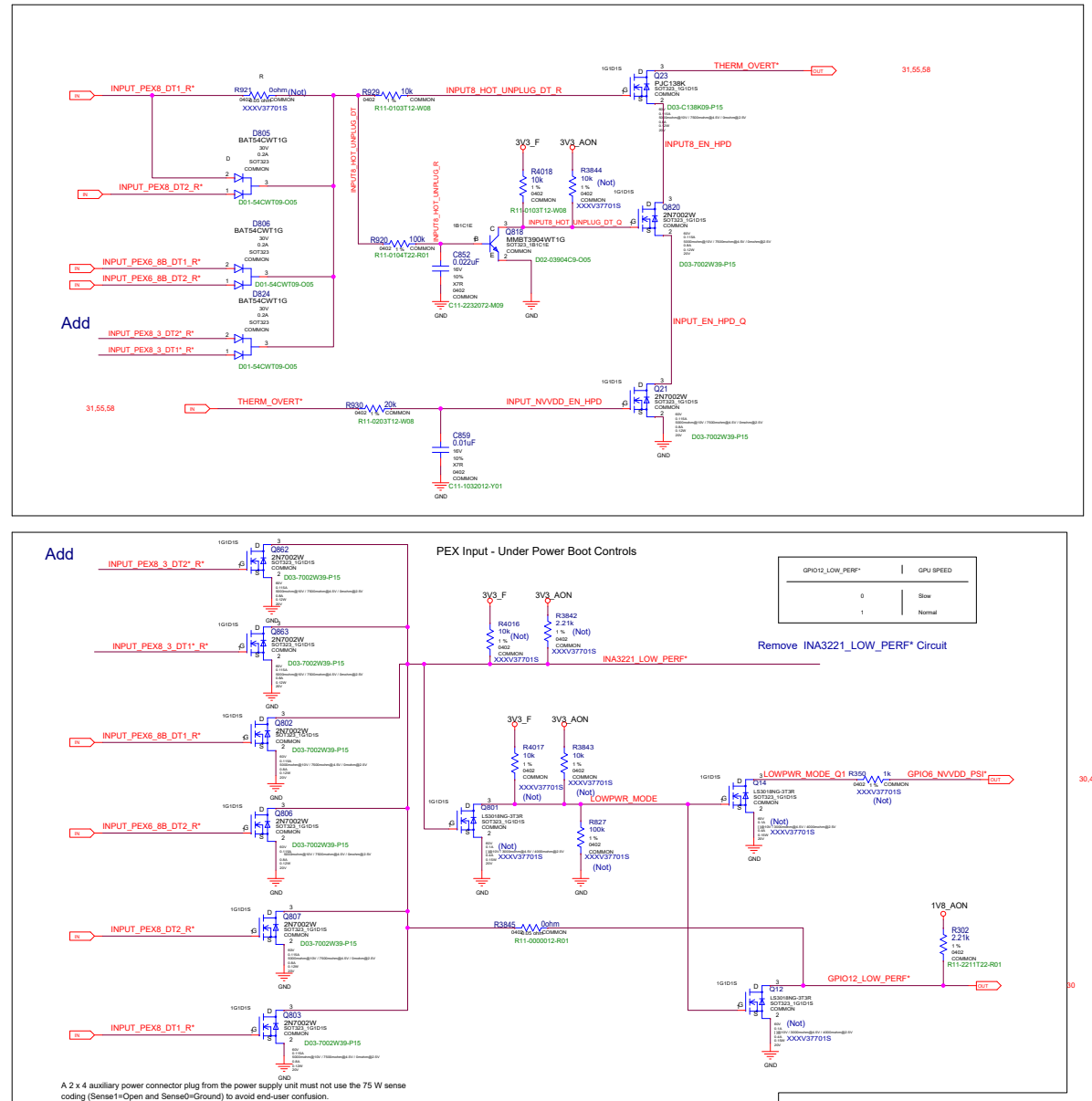
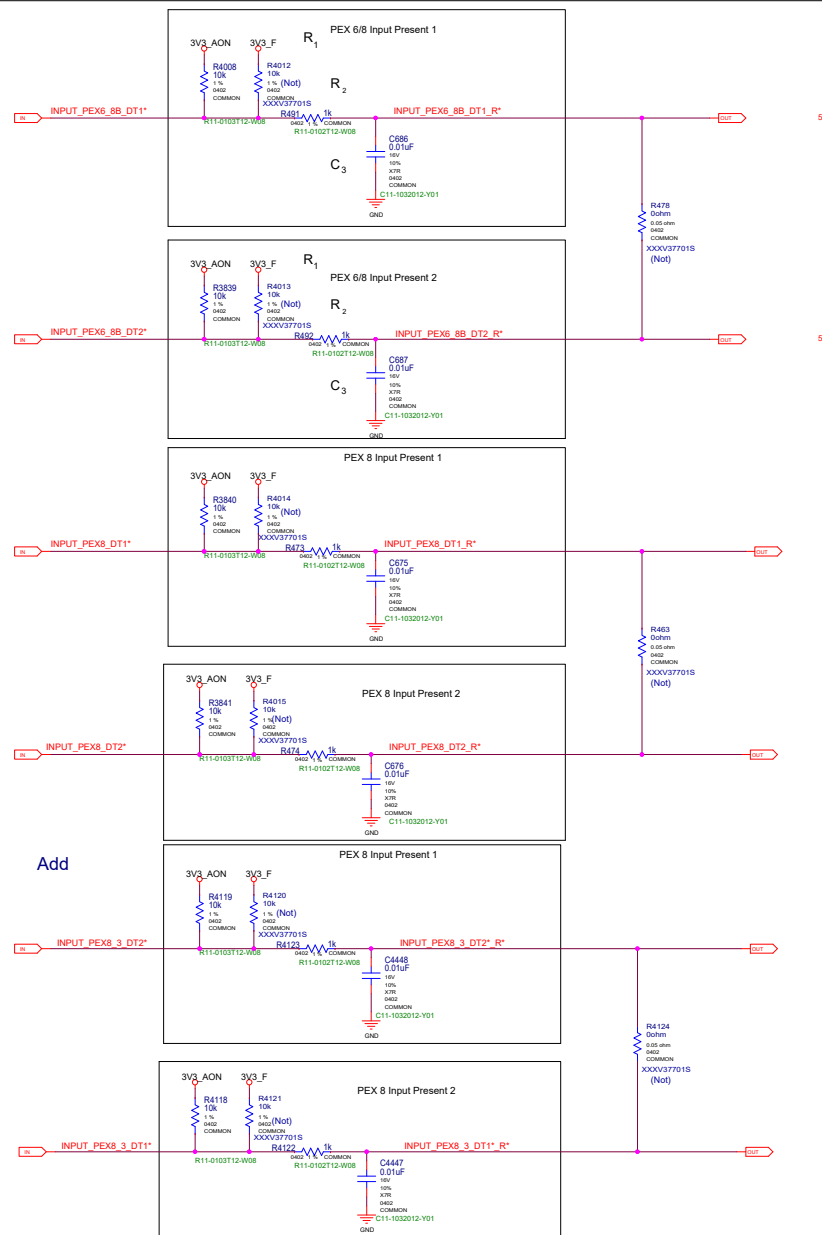
PEX 12V INPUT - 66W



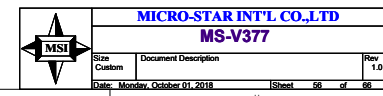
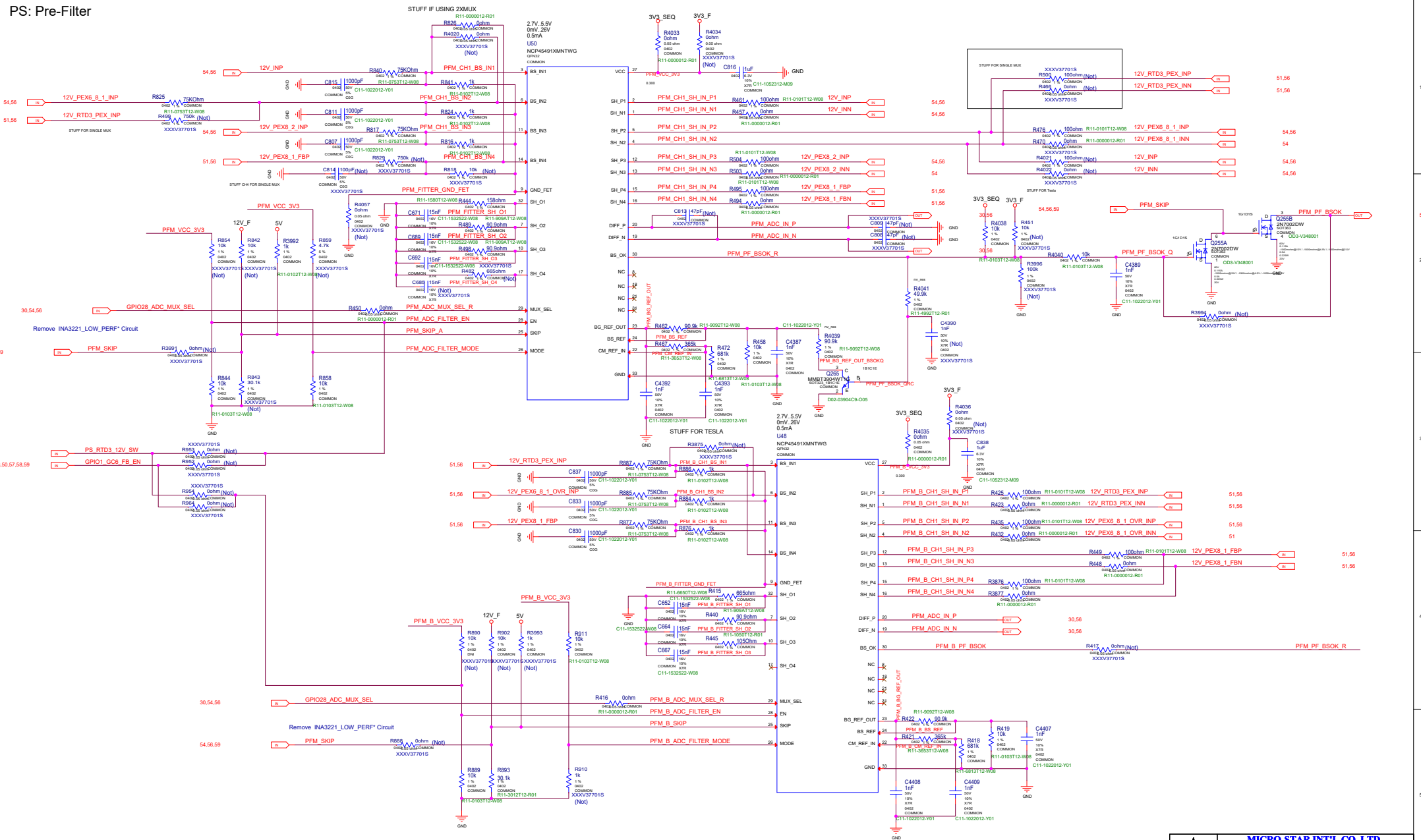
Remove RS14 RS15



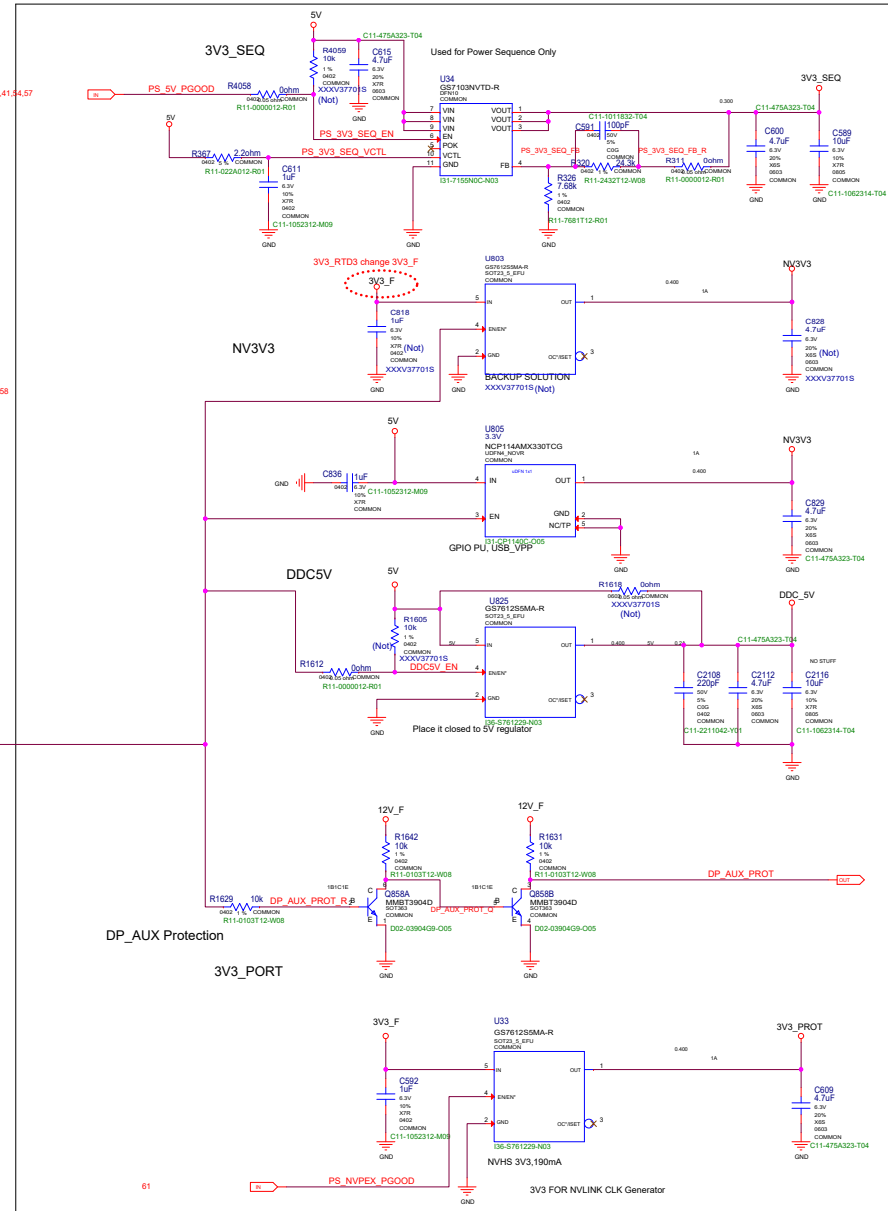
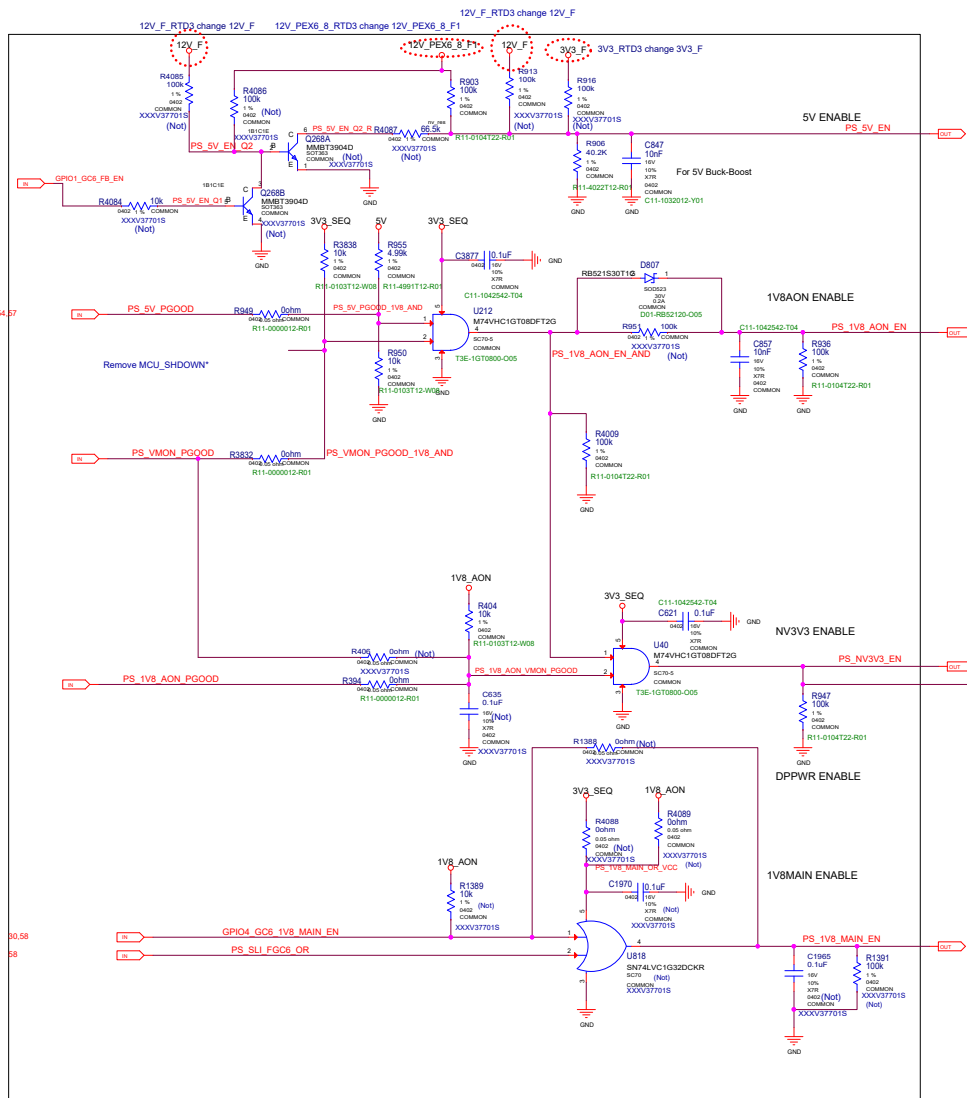
PS: 12V Current Steering & Hot Unplug Detect



PS: Pre-Filter



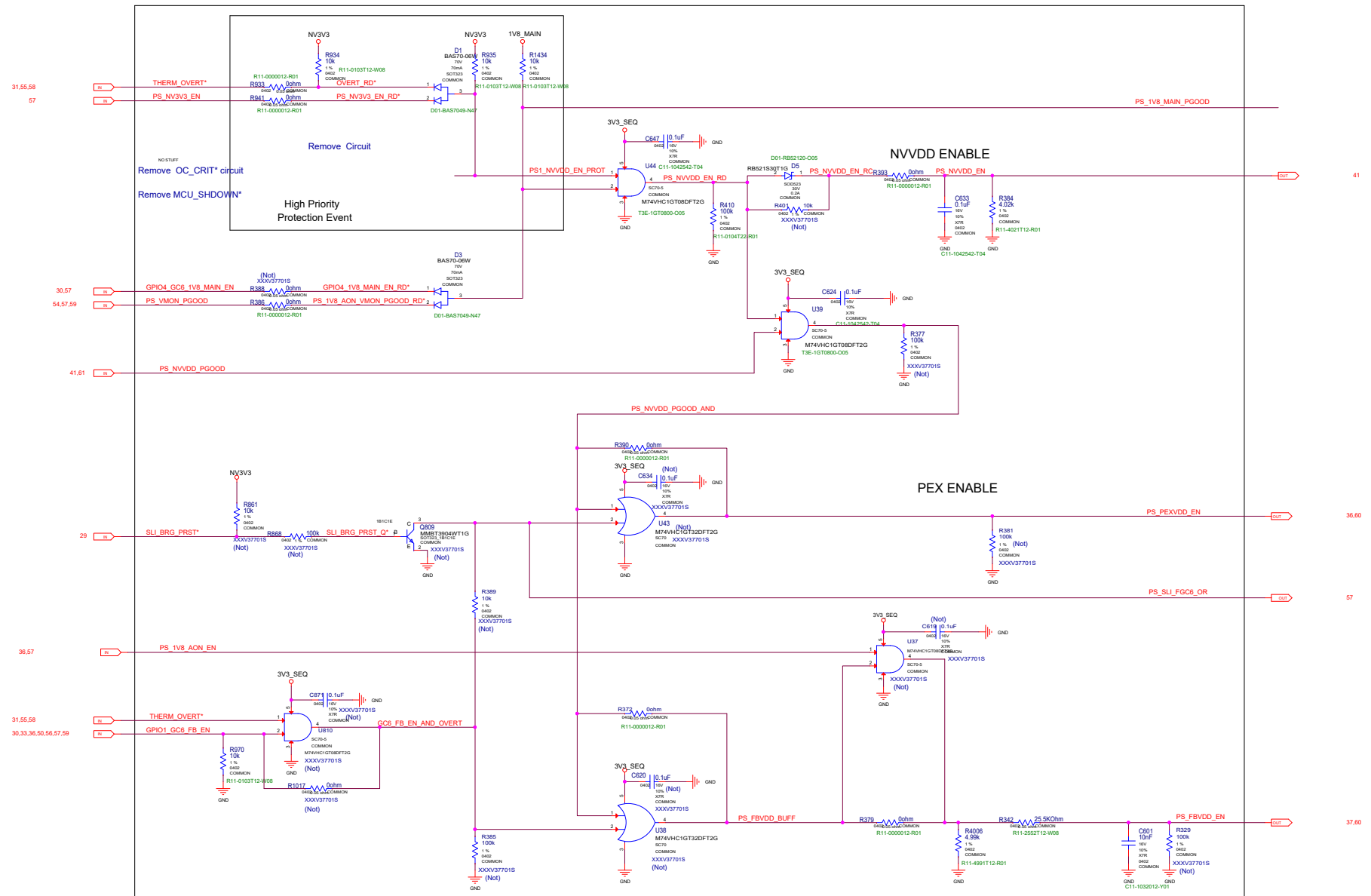
SEQUENCE:5V,1V8,NV3V3 ENABLE



MICRO-STAR INT'L CO.,LTD
MS-V377

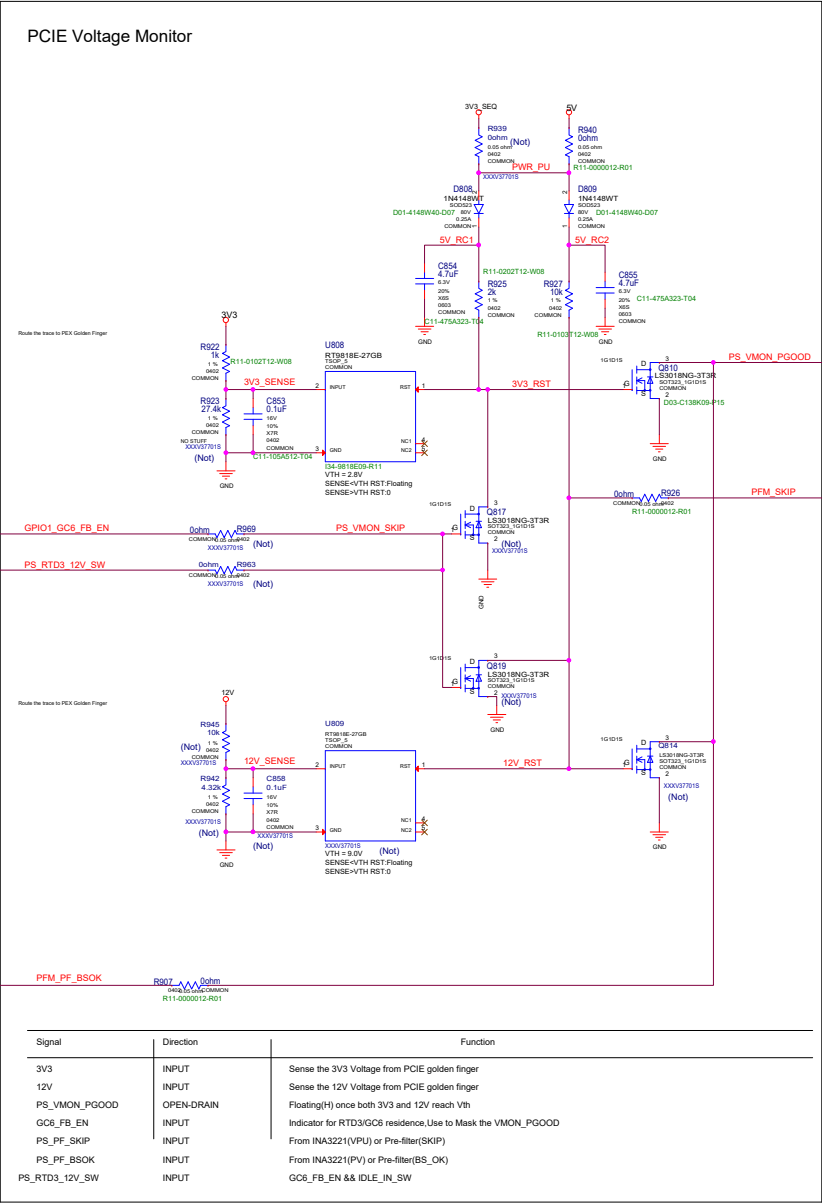
Size Custom	Document Description 5V,1V8,NV3V3 ENABLE	Rev 1.0
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SEQUENCE:NV,PEX,FB ENABLE



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BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

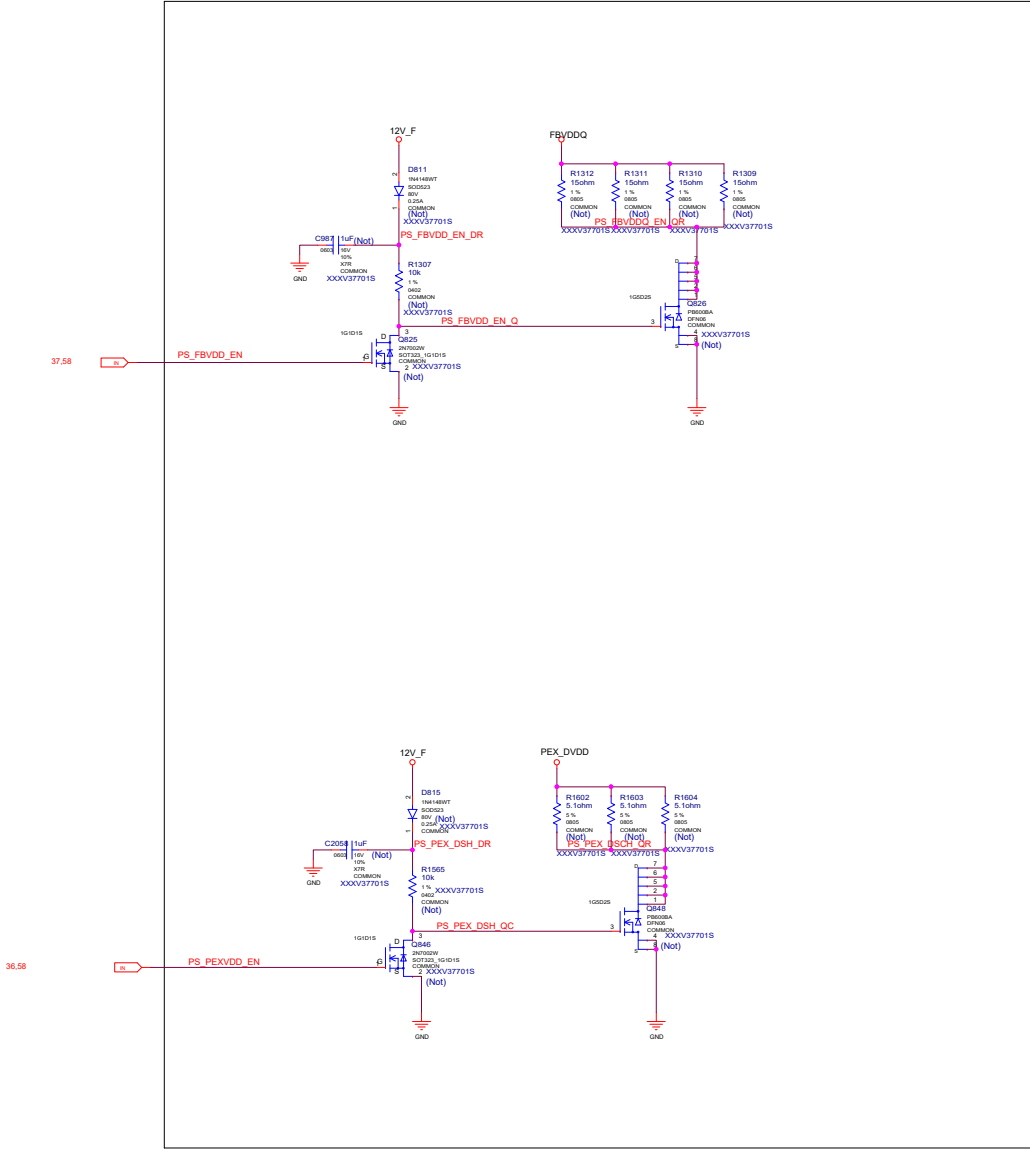
Power Supply

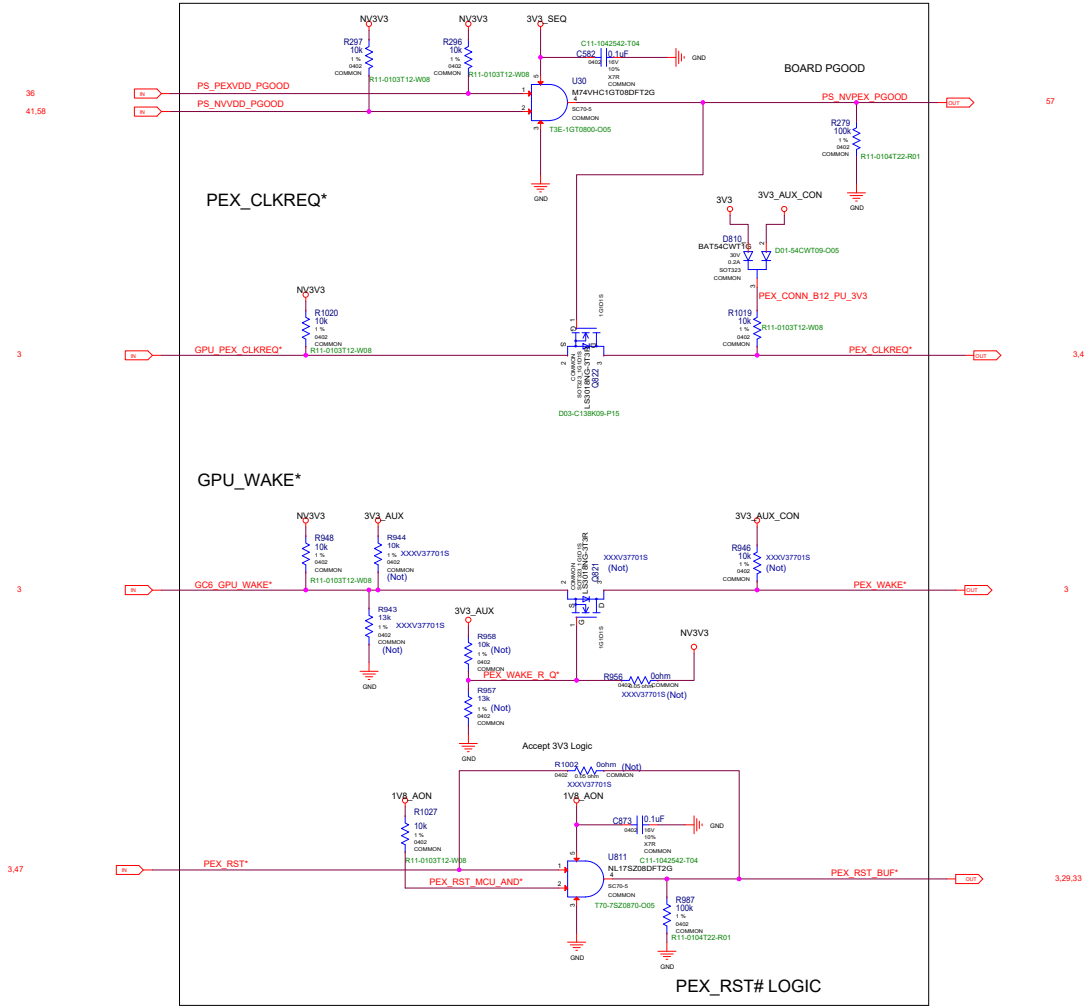
INA3221:3V3_SEQ

Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs







LED BOOST

Remove LED BOOST

05

29.30.47

29.30.47

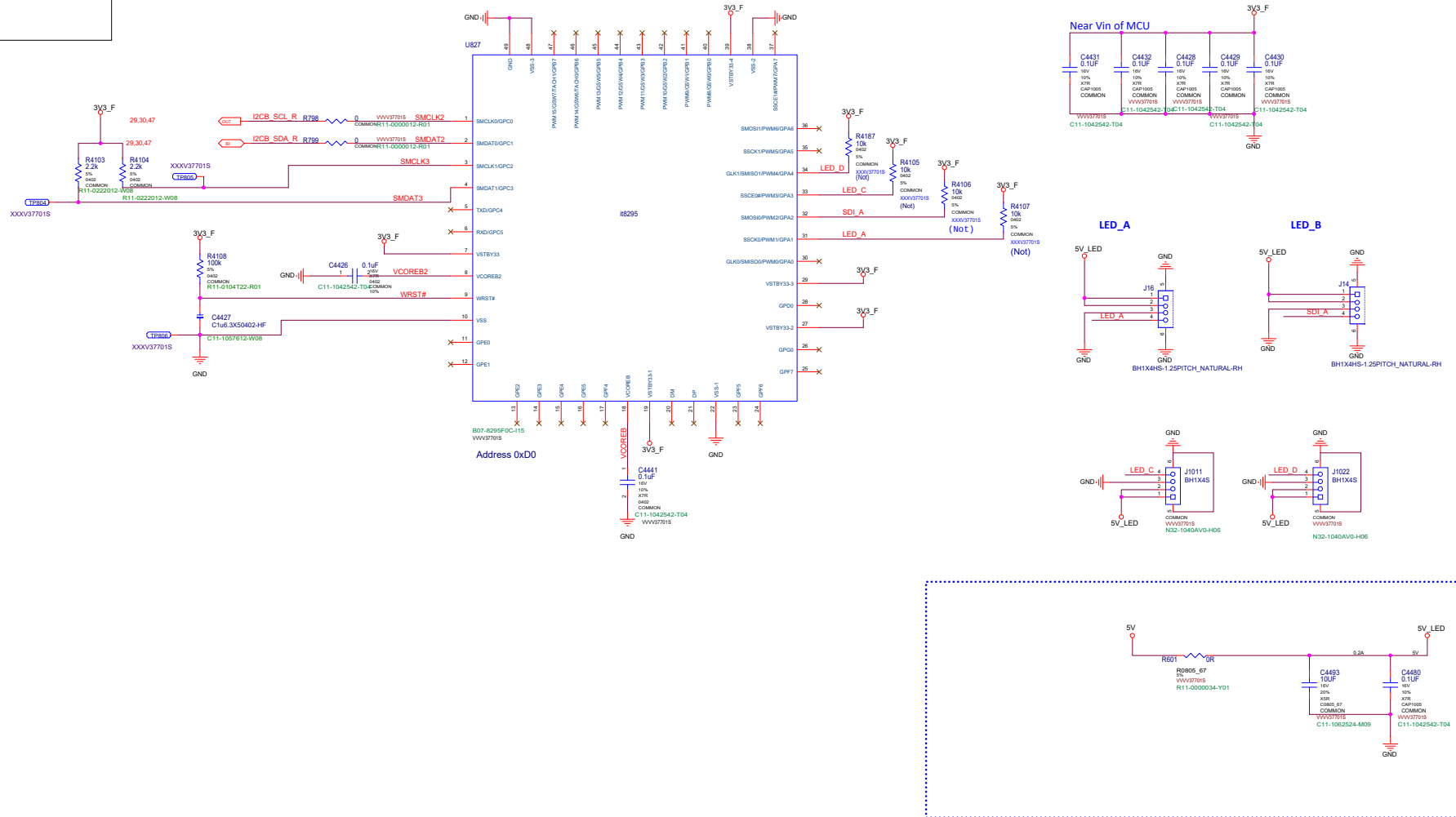


29,30,47

29,30,47

9/27 Remove J803
9/27 ADD TP804 / TP805

Firmware Programming Debug



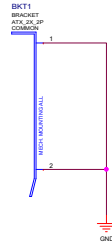
ZERO IDLE POWER MCU



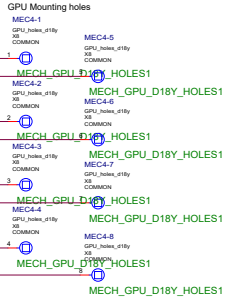
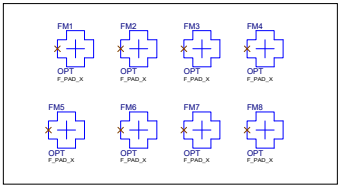
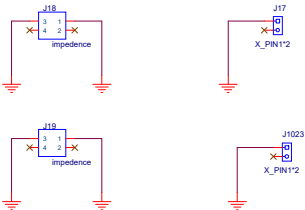
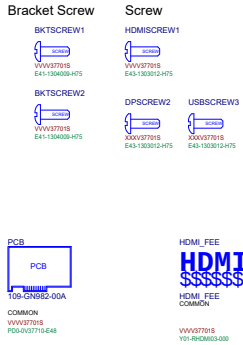
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Mechanical: Bracket/Thermal Solution

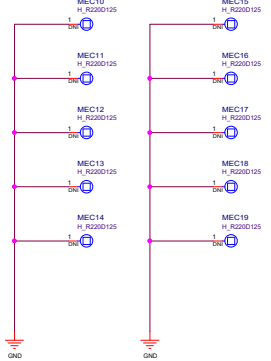
Brackets:



Bracket Screw



Mechanical Holes Symbol



VR THERMAL PROTECTION

41,42,43,44,45

IN

PS_NVVDD_TMON

R313

0ohm

Req. 6.3.2.3.1

R11-000012-R01

37,39,40

IN

PS_FBVDD_TMON

R341

0ohm

Req. 6.3.2.3.1

R11-000012-R01