PG150-C03

384b GDDR6 x16
TALL DP + DP + DP + HDMI/DP + USB

TABLE OF CONTENTS

Page	Description
1	Table of Contents
2	BLOCK DIAGRAM
3	PCI EXPRESS
4	PCIE TERM
5	MEMORY: GPU PARTITION A/B
6	MEMORY: FBA PARTITION[31:0]
7	MEMORY: FBA PARTITION[63:32]
8	MEMORY: FBB PARTITION[31:0]
9	MEMORY: FBB PARTITION[63:32]
10	MEMORY: GPU PARTITION C/D
11	MEMORY: FBC PARTITION[31:0]
12	MEMORY: FBC PARTITION[63:32]
13	MEMORY: FBD PARTITION[31:0]
14	MEMORY: FBD PARTITION[63:32]
15	MEMORY: GPU PARTITION E/F
16	MEMORY: FBE PARTITION[31:0]
17	MEMORY: FBE PARTITION[63:32]
18	MEMORY: FBF PARTITION[31:0]
19	MEMORY: FBF PARTITION[63:32]
20	GPU PWR AND GND
21	GPU PWR, GND and NCs
22	GPU DECOUPLING
23	GPU DECOUPLING 2
24	IFPA/B DP
25	IFPE DP
26	IFPF USB
27	IFPC HDMI/DP
28	IFPD DP
29	NVHS X16
30	MISC: THERMAL, JTAG, GPIO, STEREO
31	MISC: ROM, STRAPS
32	MISC: XTAL, PLL
33	MISC: USB PPC
34	PS: USB_C VR
35	PS: 5V
36	PS: PEXVDD 1V8 Rail
37	PS: FBVDD Controller
38	PS: FBVDD Controller OVR3
39	PS: FBVDD Phase 1, 2
40	PS: FBVDD Phase 3
41	PS: NVVDD Controller_OVR8
42	PS: NVVDD Phase 1
43	PS: NVVDD Phase 2
44	PS: NVVDD Phase 3, 4
45	PS: NVVDD Phase 5
46	PS: NVVDD Phase 7, 8
47	PS: NVVDD Phase 9, 10
48	PS: NVVDD Phase 11, 12
49	PS: NVVDD Phase 13, 14
50	PS: INPUT SWITCH_RTD3
51	PS: INPUT SWITCH_RTD3 USB
52	PS: INPUT SWITCH RAIL BALANCE
53	PS: DISCRETE STEERING
54	PS: Input, filtering, and Monitoring
55	PS: Current Sterring, Hot Unplug
56	PS: Prefilter
57	Sequence: 5V, 1V8, NV3V3 EN
58	Sequence: NV, PEX, FB EN
59	Sequence: PCIE Voltage Monitor
60	Sequence: Discharge
61	Sequence: MISC
62	MISC: FAN & LED1
63	MISCL: LED 2
64	MCU ZERO POWER IDLE
65	MECH
66	VR Thermal Protection

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Table of Contents

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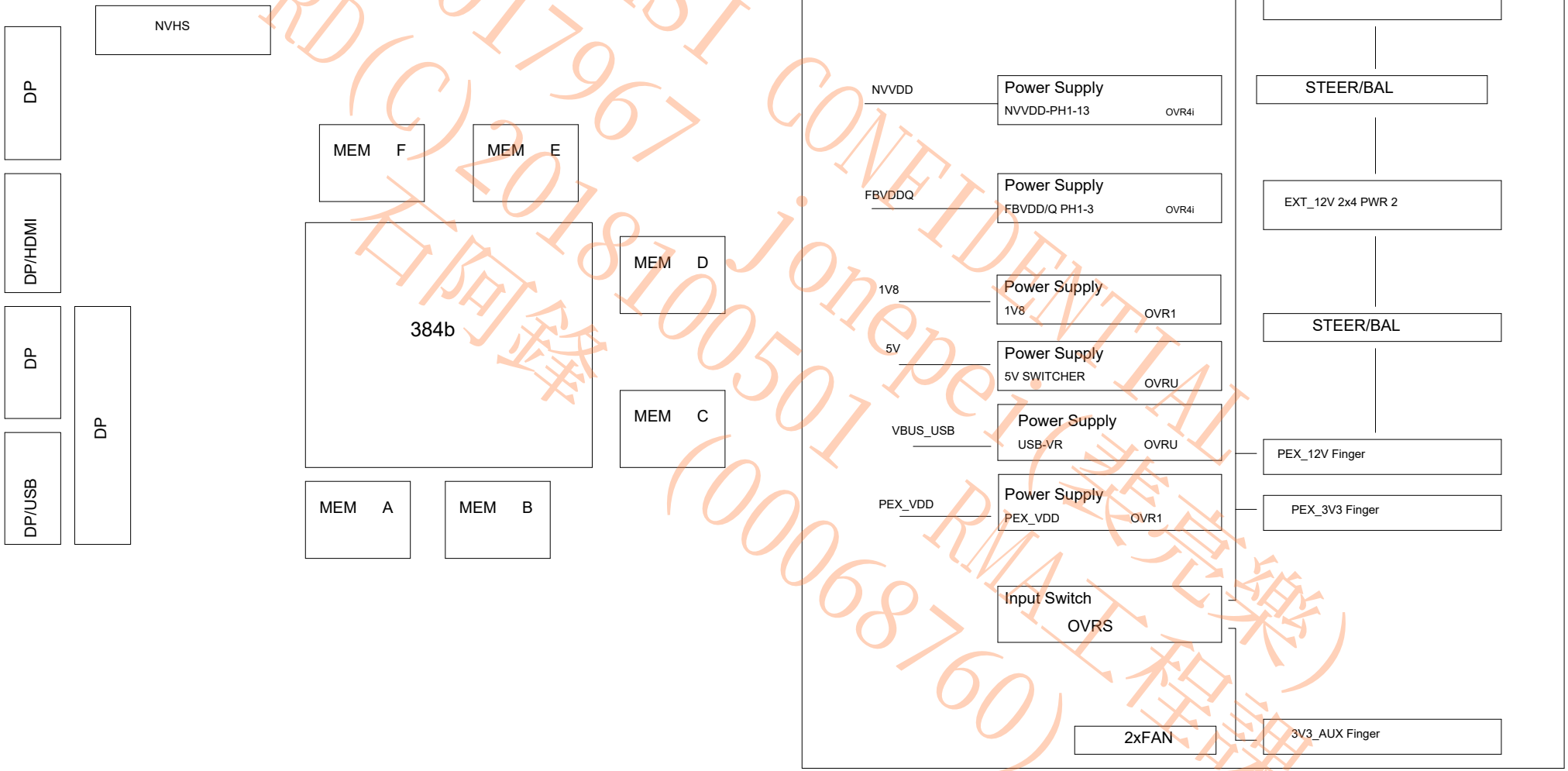
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	1 OF 66
BOM REV	A	DATE	09-JUL-2018

Block Diagram



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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	2 OF 66
BOM REV	A	DATE	09-JUL-2018

PCI Express

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
3V3	3.0A	0.400	
GND	8.5A	0.400	

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCI EXPRESS

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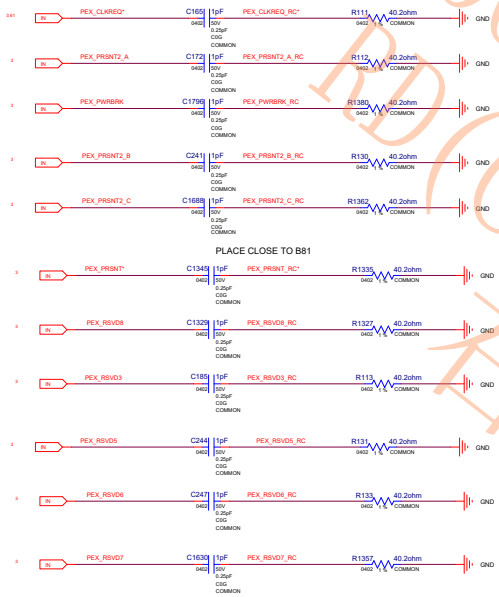
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	3 OF 66
BOM REV	A	DATE	09-JUL-2018

PCI TERM



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PAGE DETAIL	PCIE TERM

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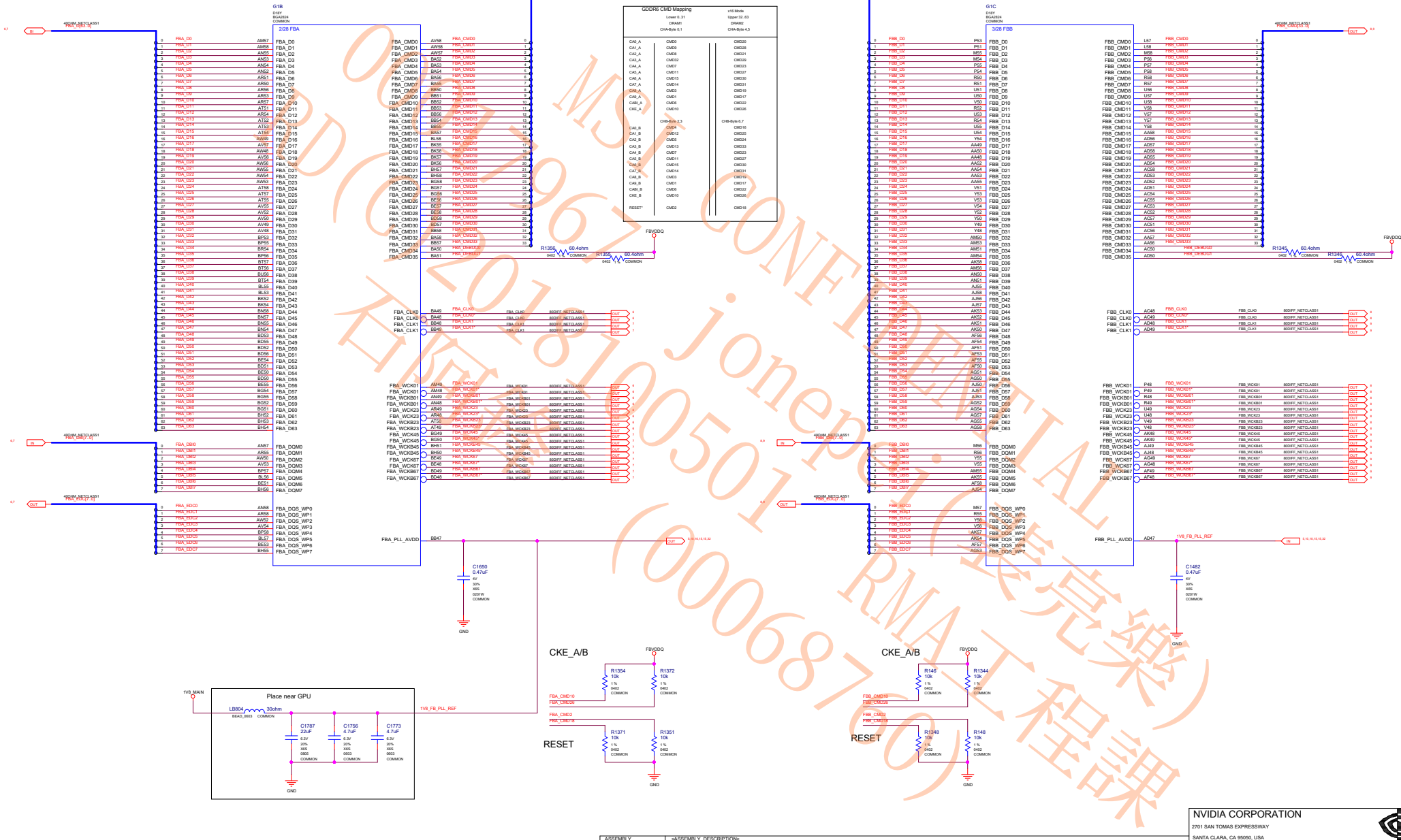
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	4 OF 66
BOM REV	A	DATE	09-JUL-2018

MEMORY: GPU Partition A/B



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NVIDIA CORPORATION
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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	5 OF 66
BOM REV	A	DATE	09-JUL-2018

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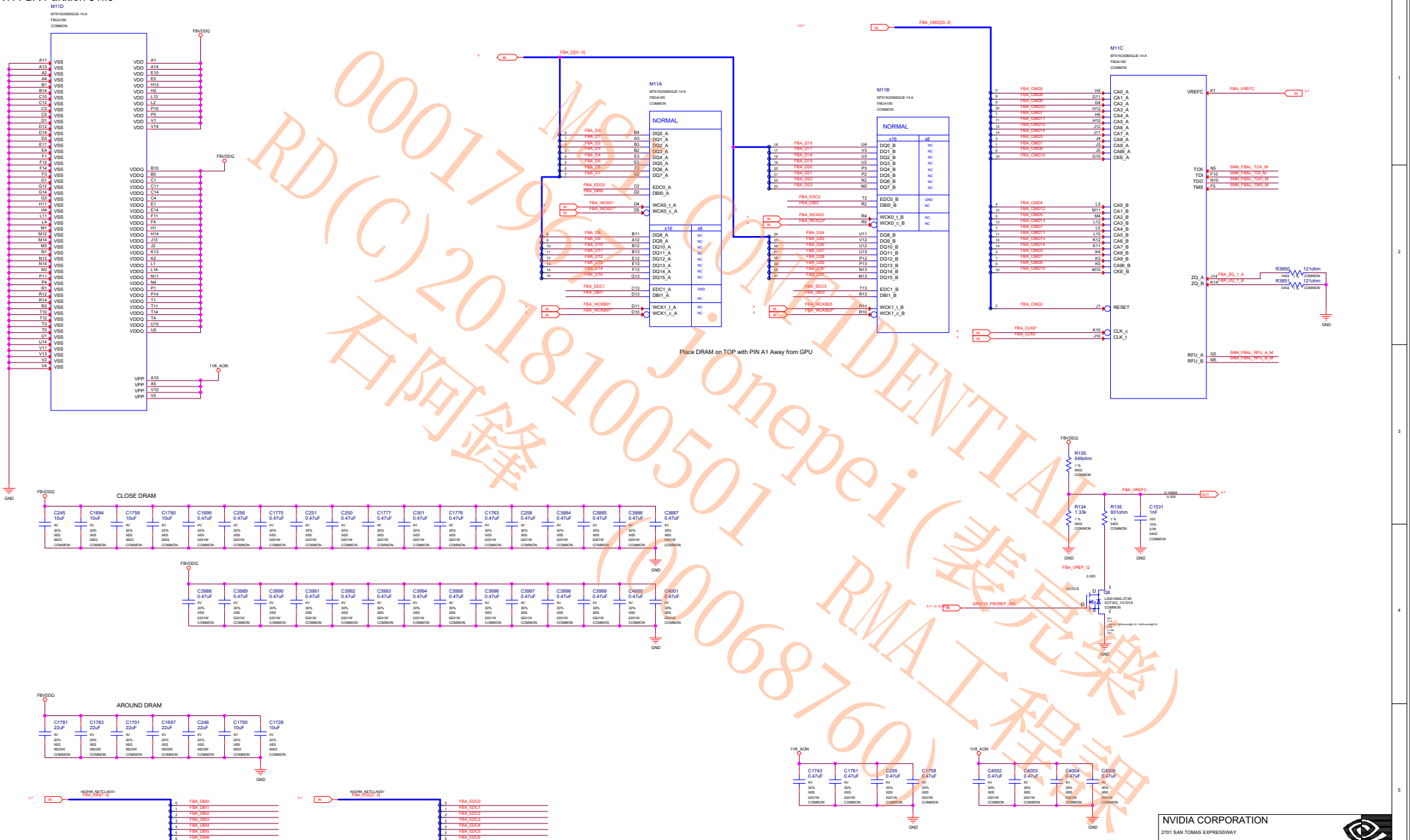
MEMORY: FBA Partition 31..0



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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	6 OF 66
BOM REV	A	DATE	09-JUL-2018

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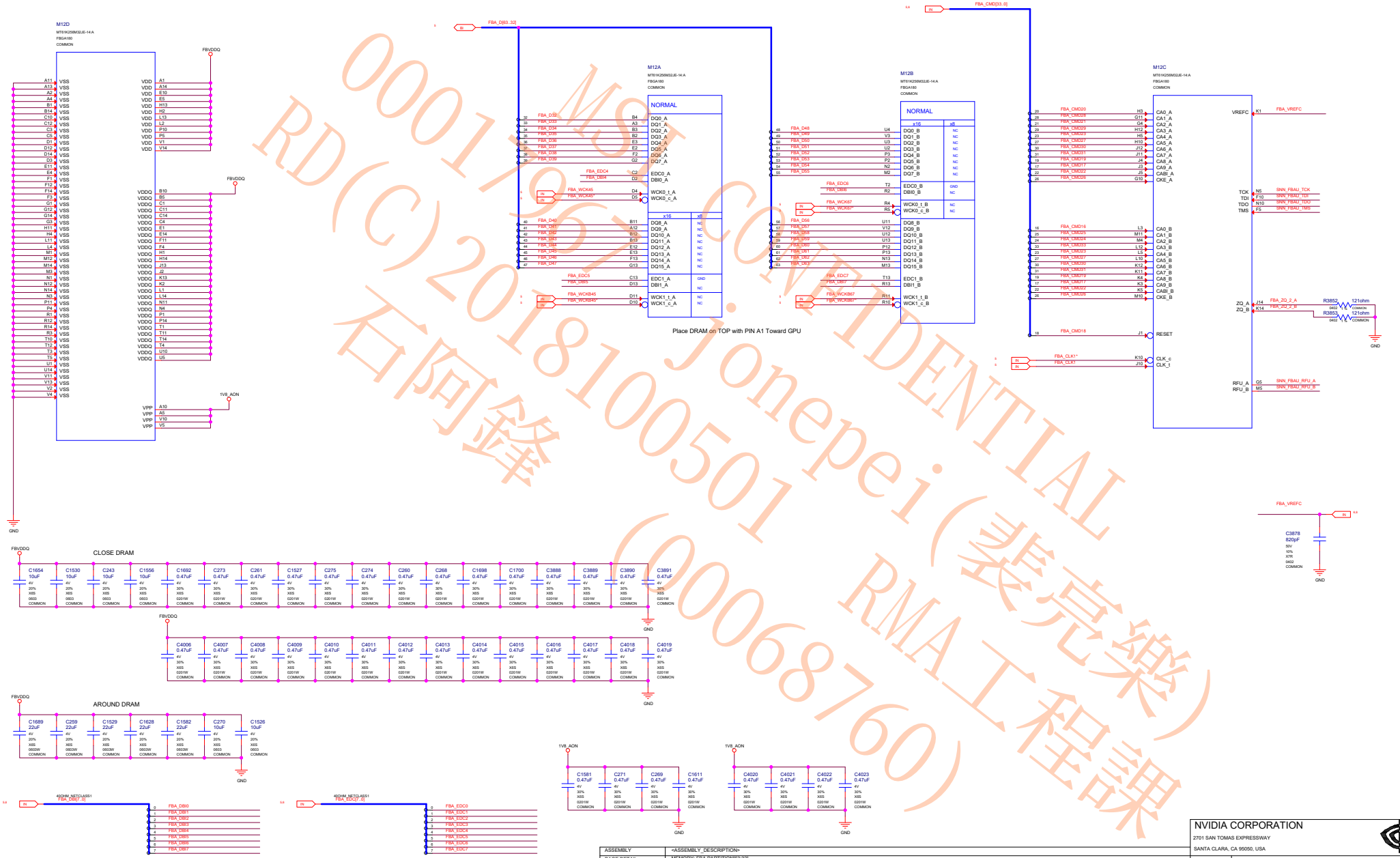
MEMORY: FBA Partition 63..32



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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	7 OF 66
BOM REV	A	DATE	09-JUL-2018

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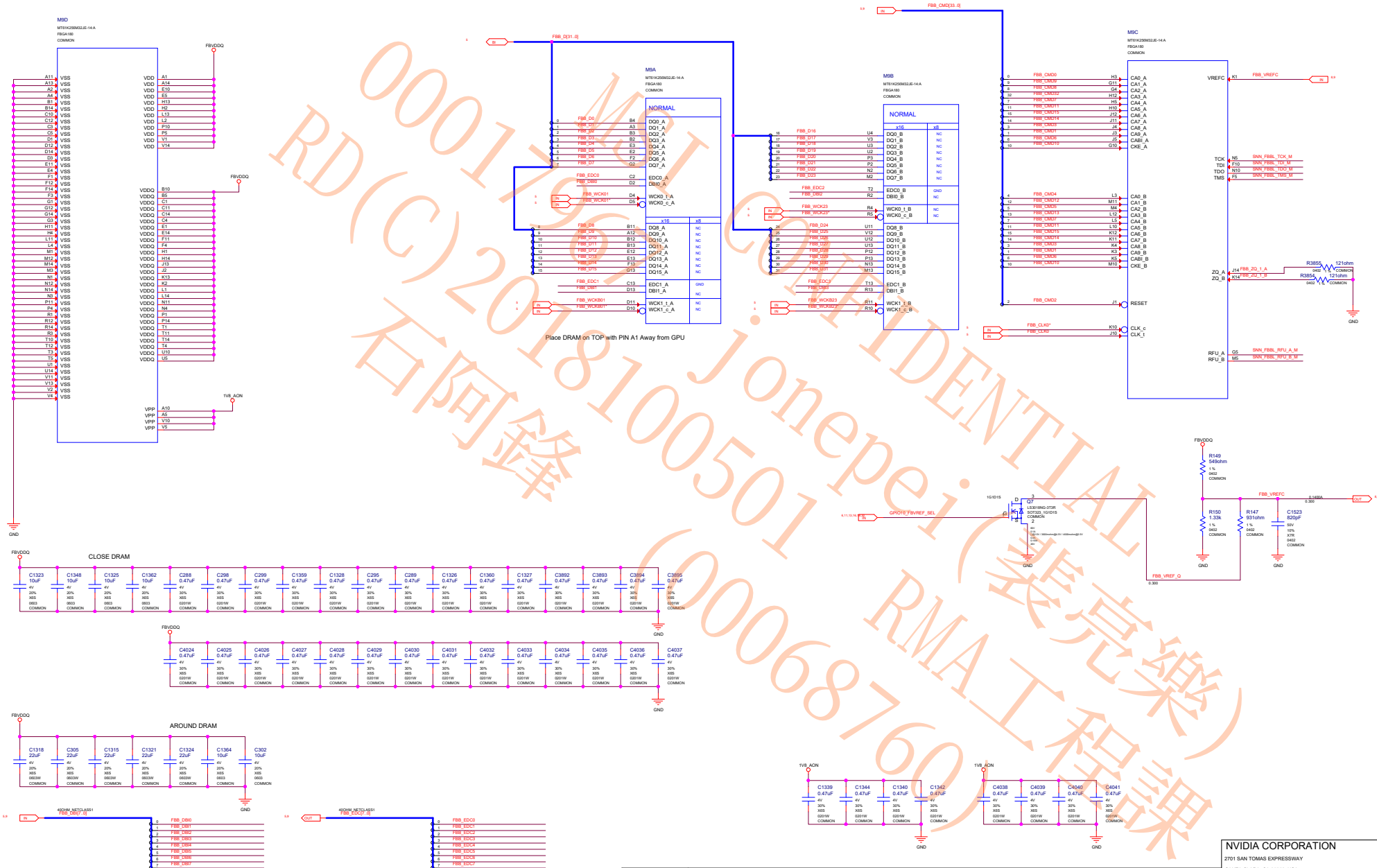

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PAGE DETAIL	MEMORY: FBB PARTITION[31:0]

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	8 OF 66
BOM REV	A	DATE	09-JUL-2018

MEMORY: FBB Partition 63..32

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	9 OF 66
BOM REV	A	DATE	09-JUL-2018

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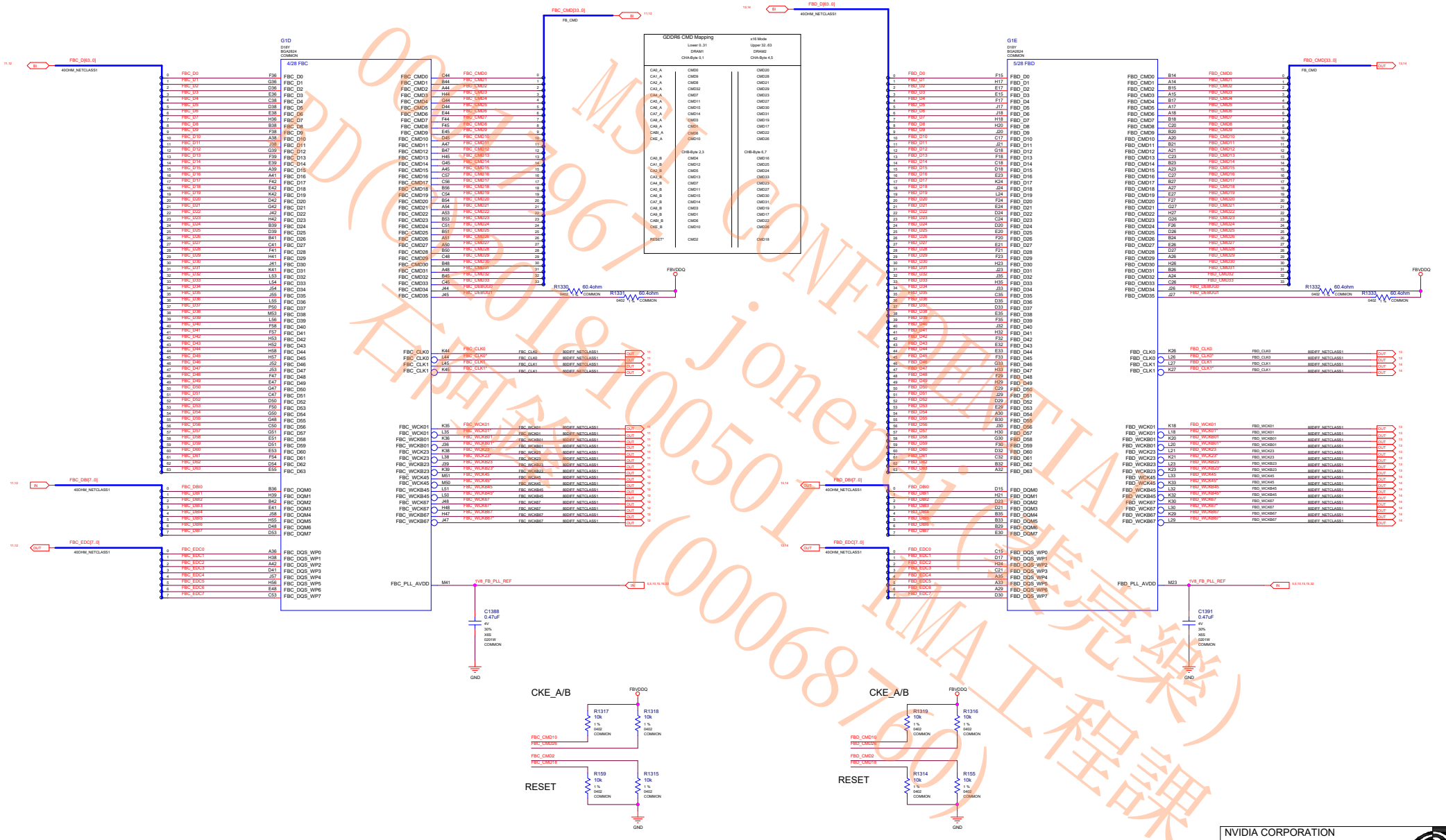

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	10 OF 66
BOM REV	A	DATE	09-JUL-2018

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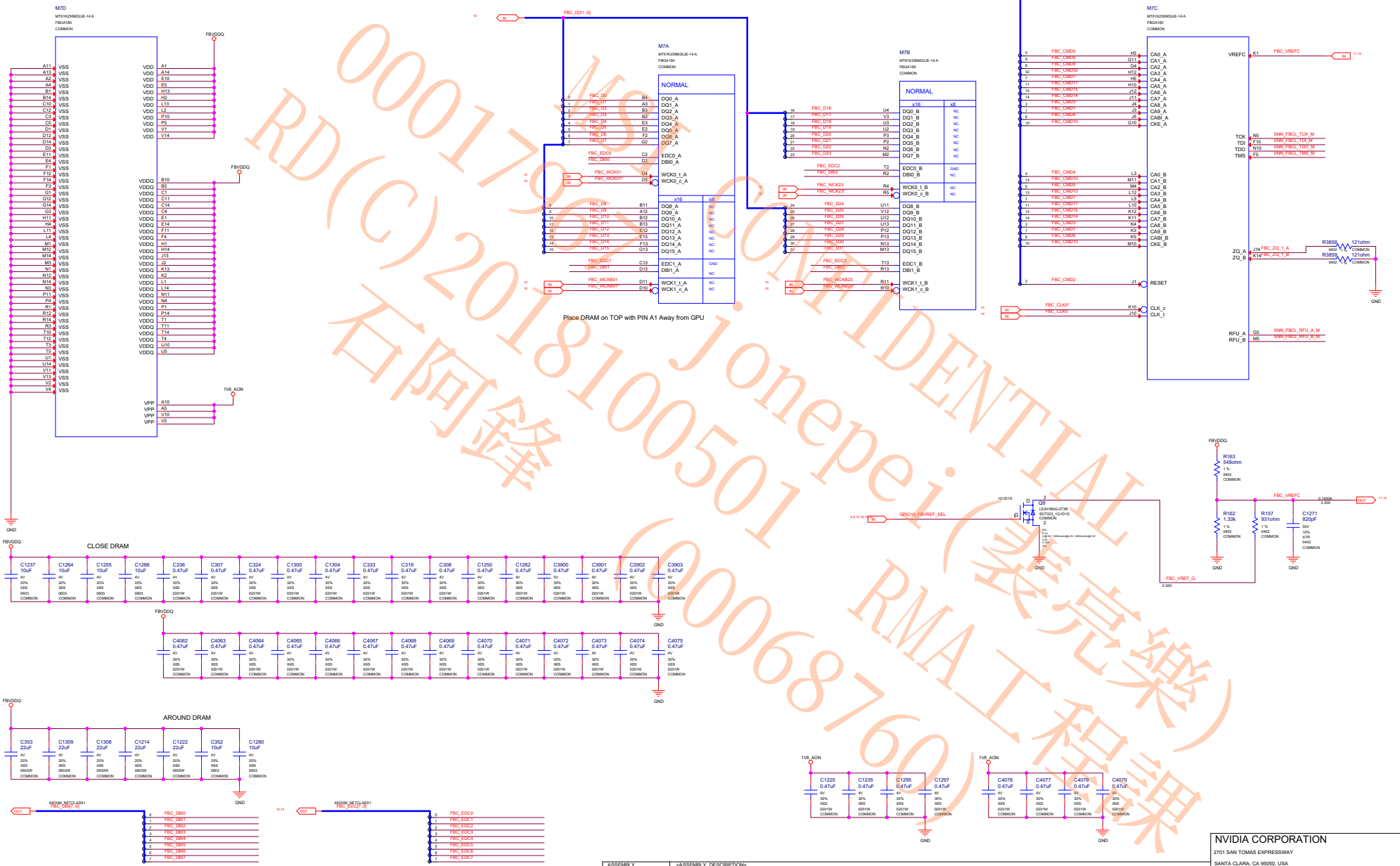

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	11 OF 66
BOM REV	A	DATE	09-JUL-2018

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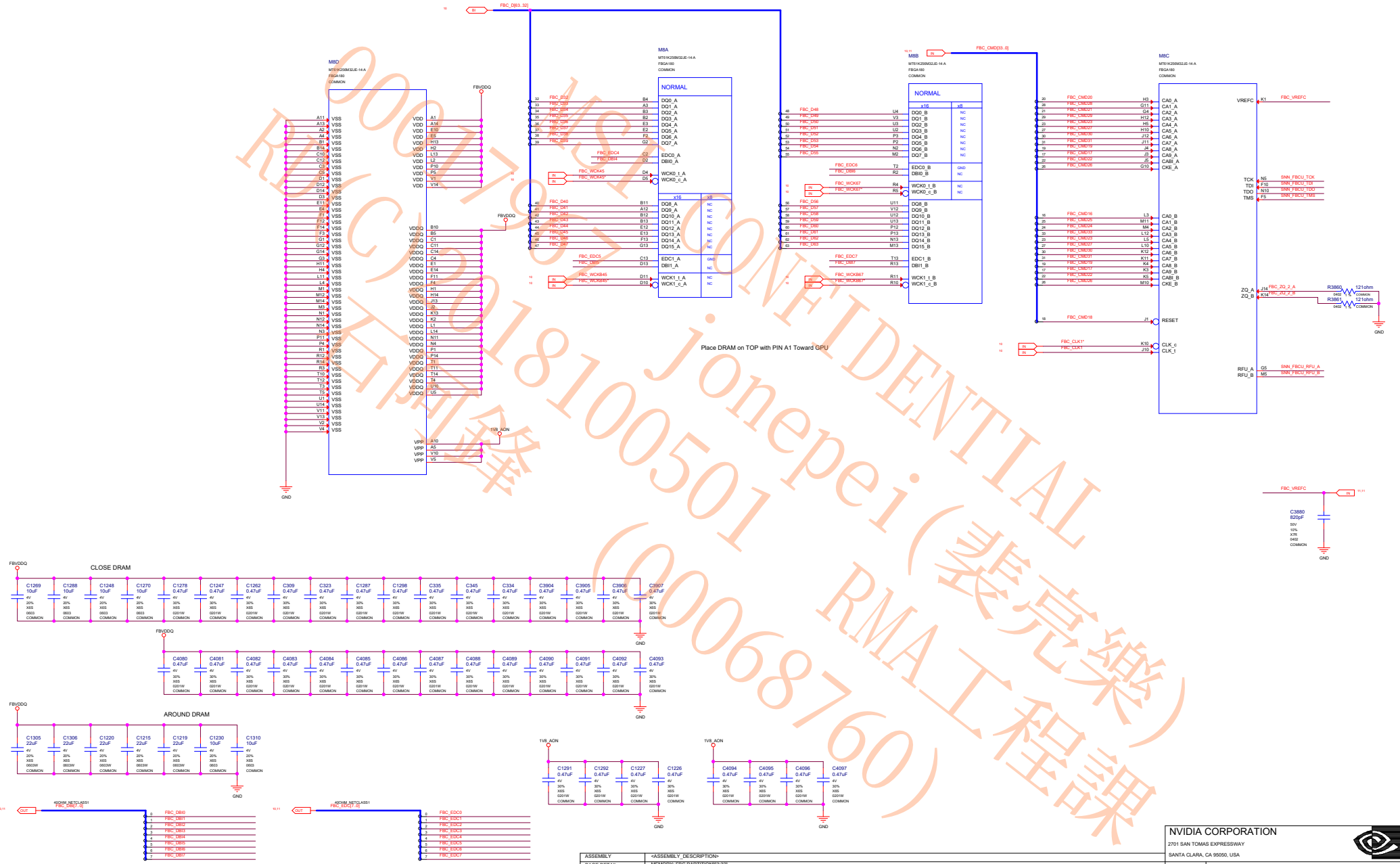

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PAGE DETAIL	MEMORY: FBC PARTITION[63:32]

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	12 OF 66
BOM REV	A	DATE	09-JUL-2018

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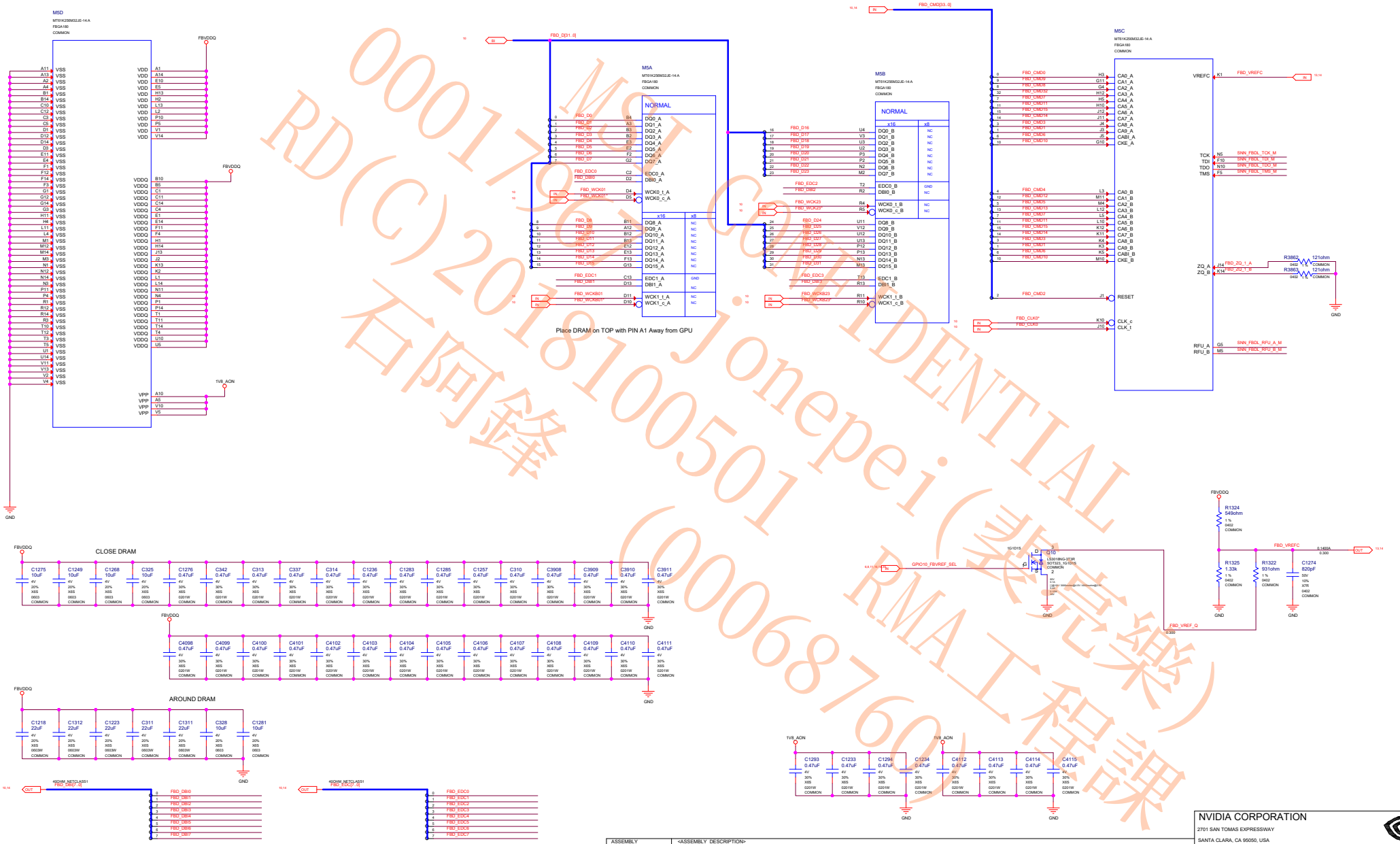

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	13 OF 66
BOM REV	A	DATE	09-JUL-2018

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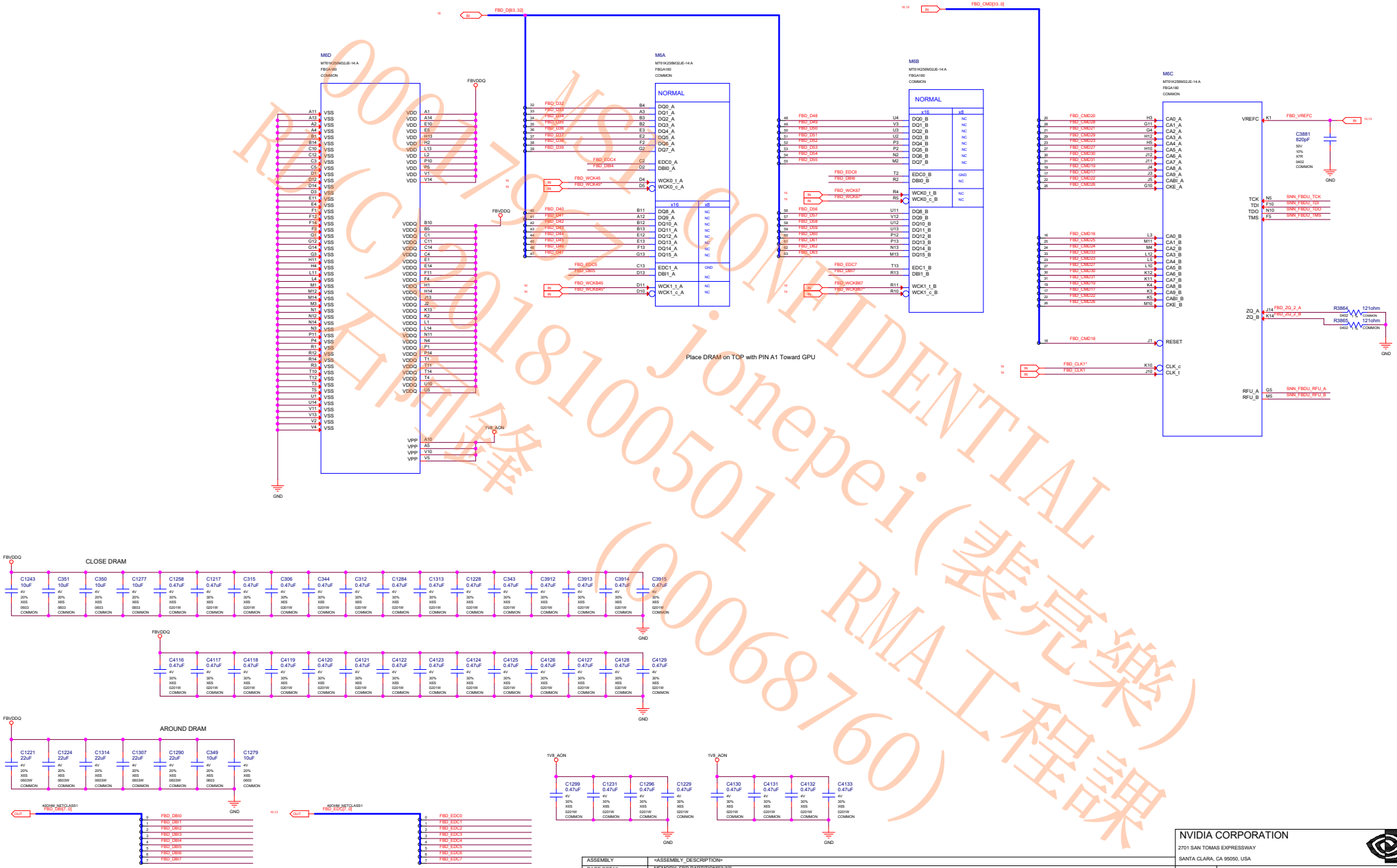

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBD PARTITION[63:32]

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	14 OF 66
BOM REV	A	DATE	09-JUL-2018

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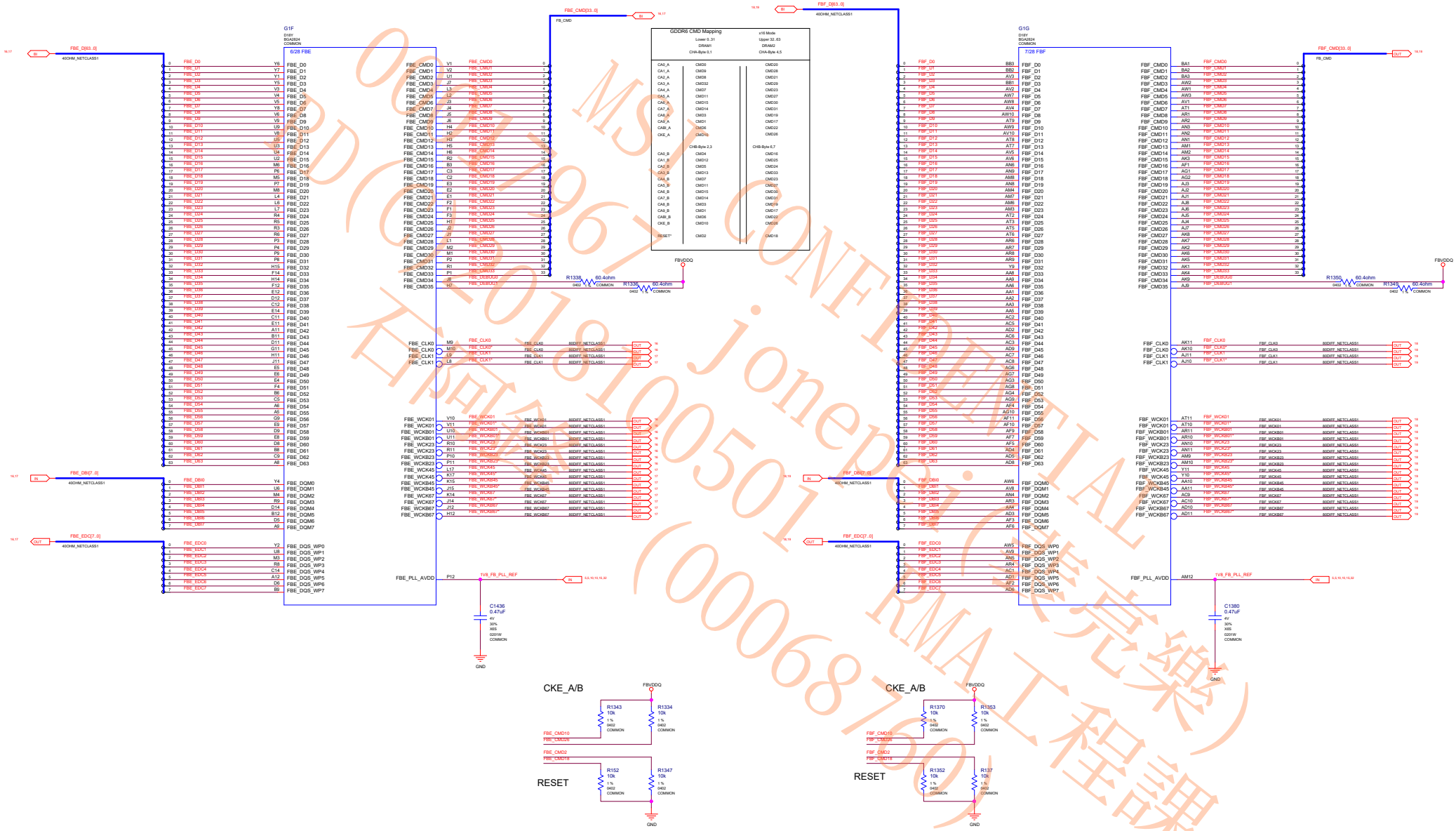

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PCB REV	PG150-C03	PAGE	15 OF 66
BOM REV	A	DATE	09-JUL-2018

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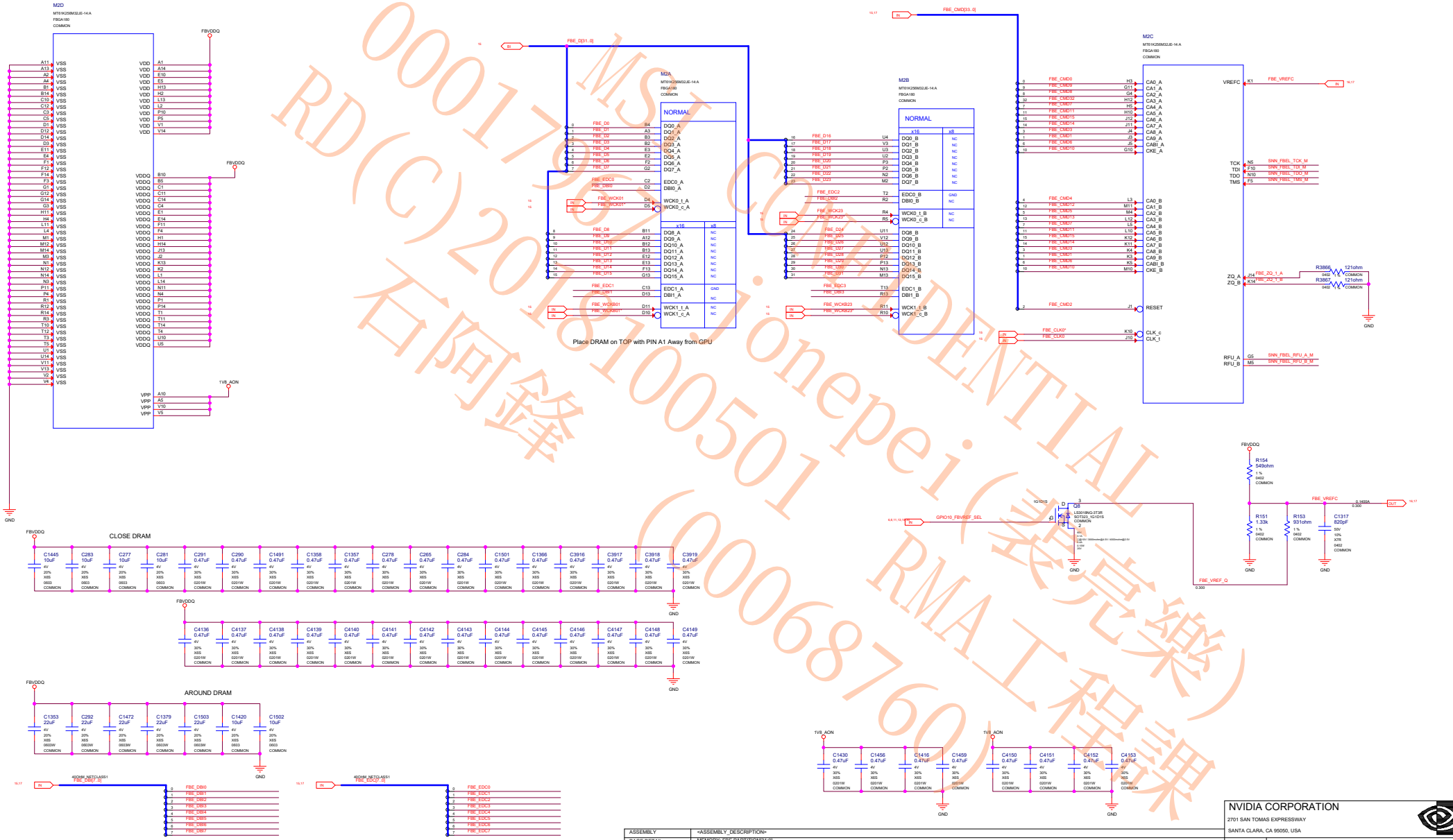
MEMORY: FBE Partition 31..0



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBE PARTITION[31:0]

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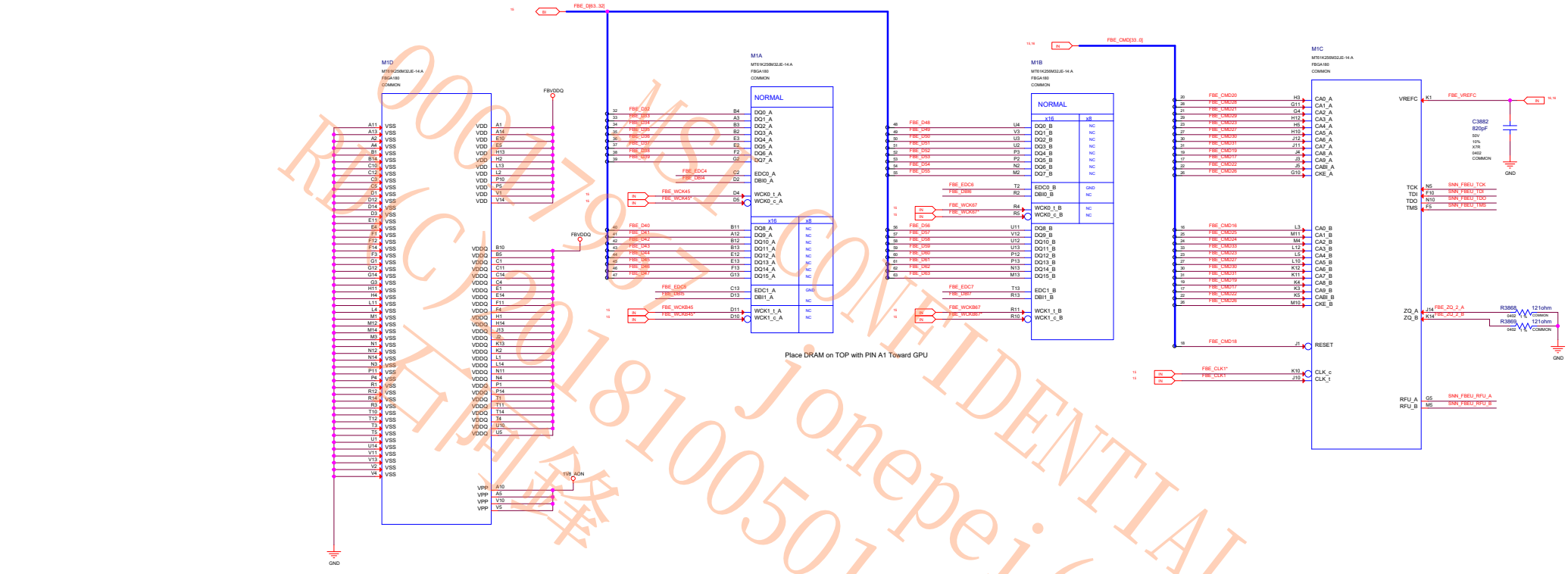
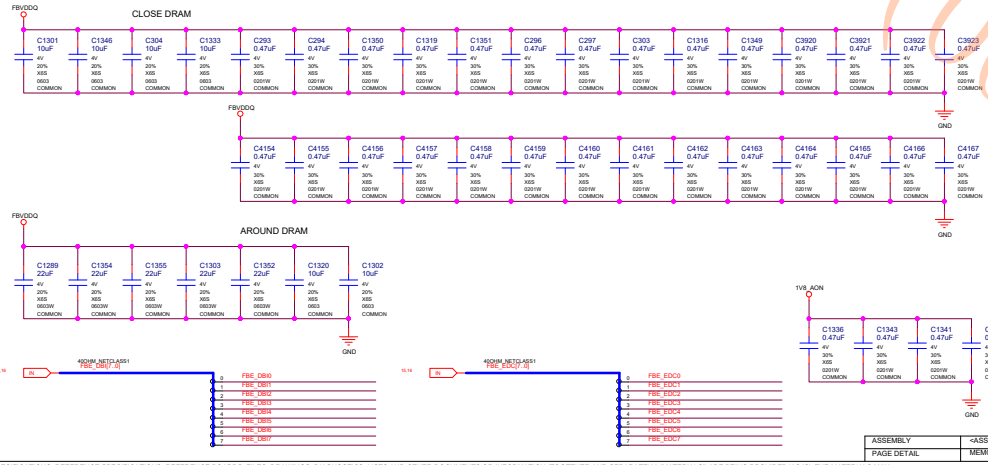
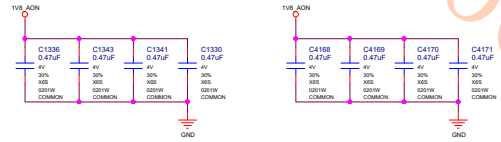
RD(C)2018100501(000687602(RMA工程課
石阿鋒

MEMORY: FBE Partition 63..32







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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	17 OF 66
BOM REV	A	DATE	09-JUL-2018

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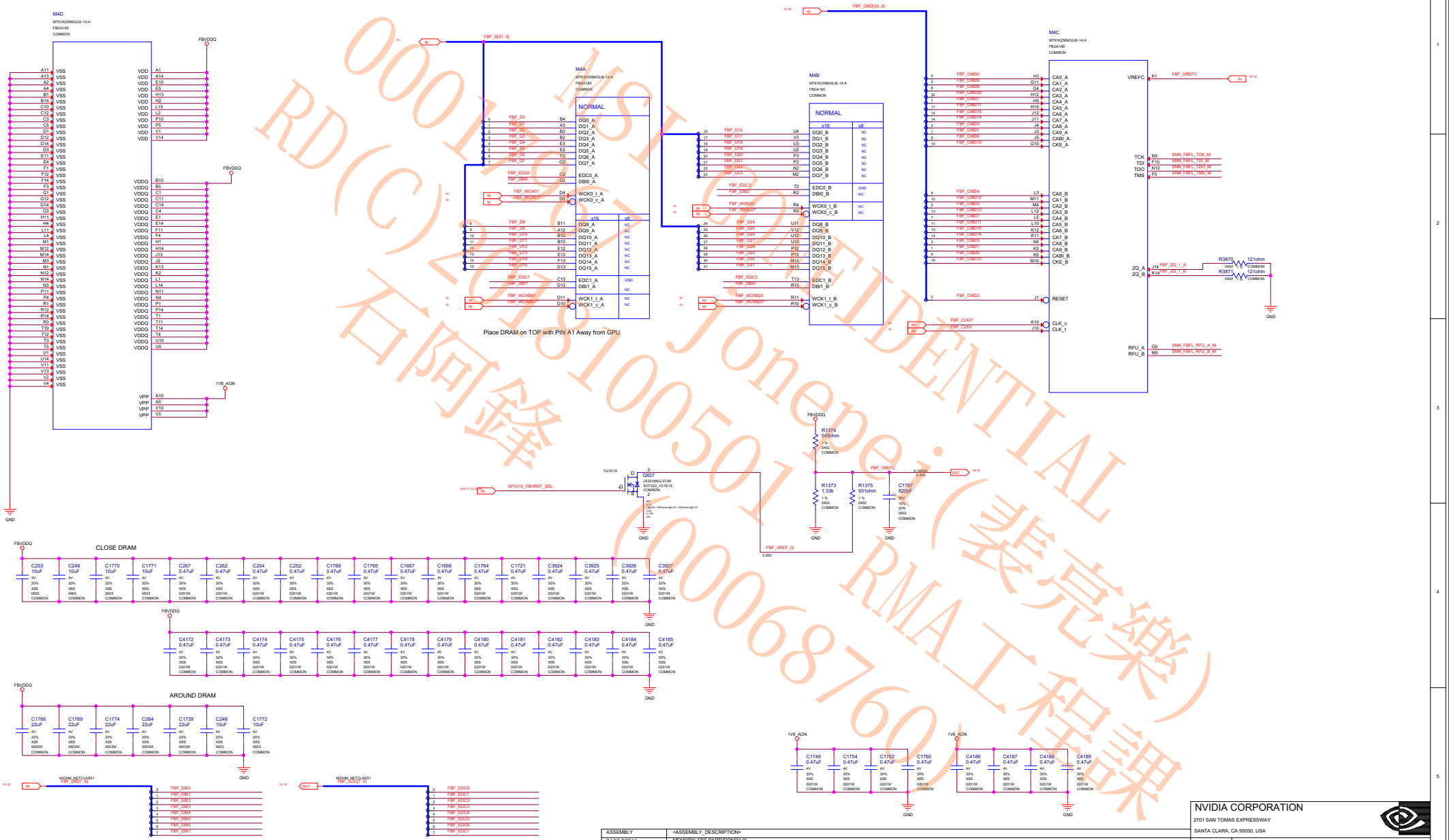
RMA工程課
(000068760)
RMA(C)2018100501
000179

MEMORY: FBF Partition 31..0



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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	18 OF 66
BOM REV	A	DATE	09-JUL-2018

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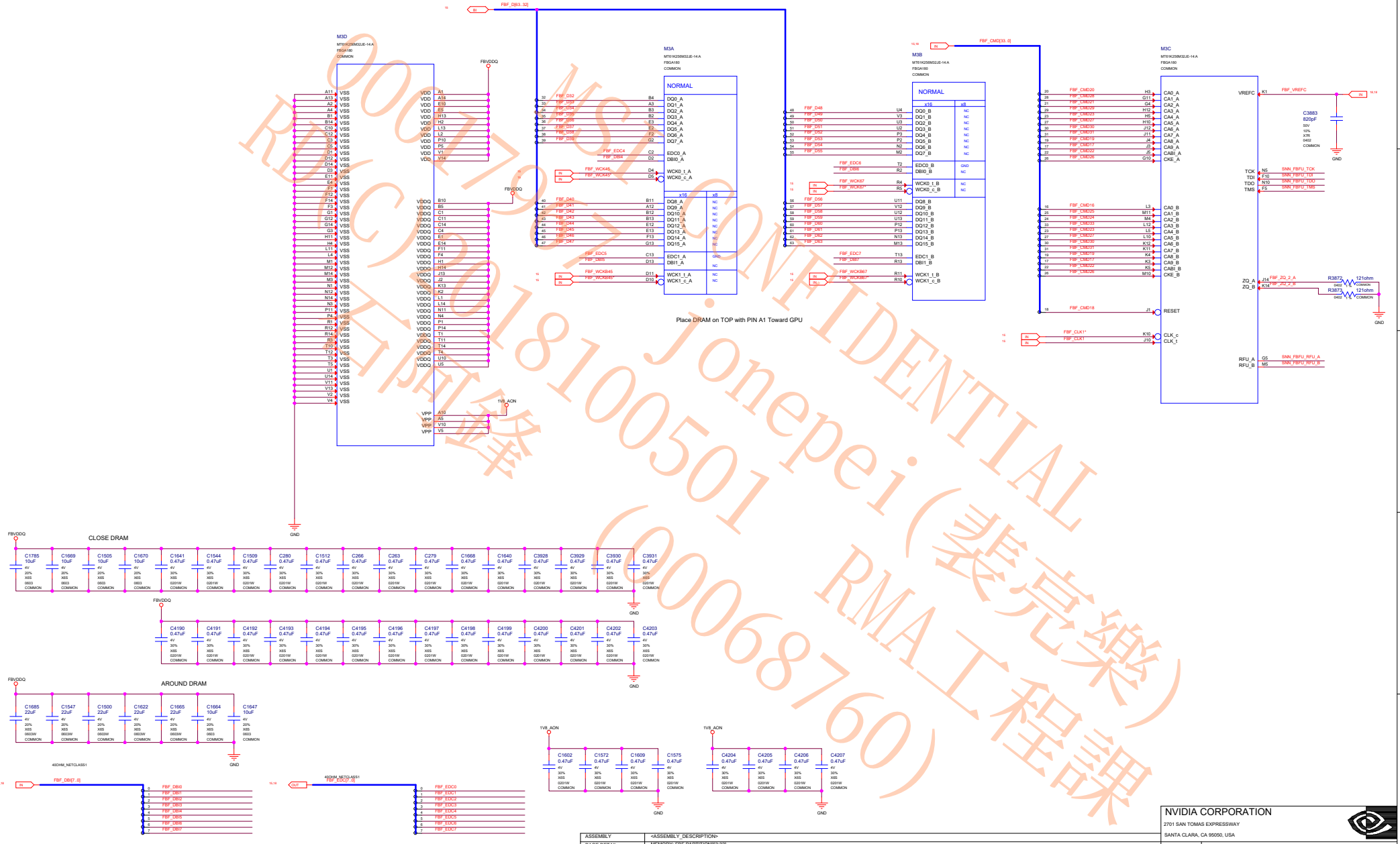
MEMORY: FBF Partition 63..32



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PAGE DETAIL	MEMORY: FBF PARTITION[63:32]

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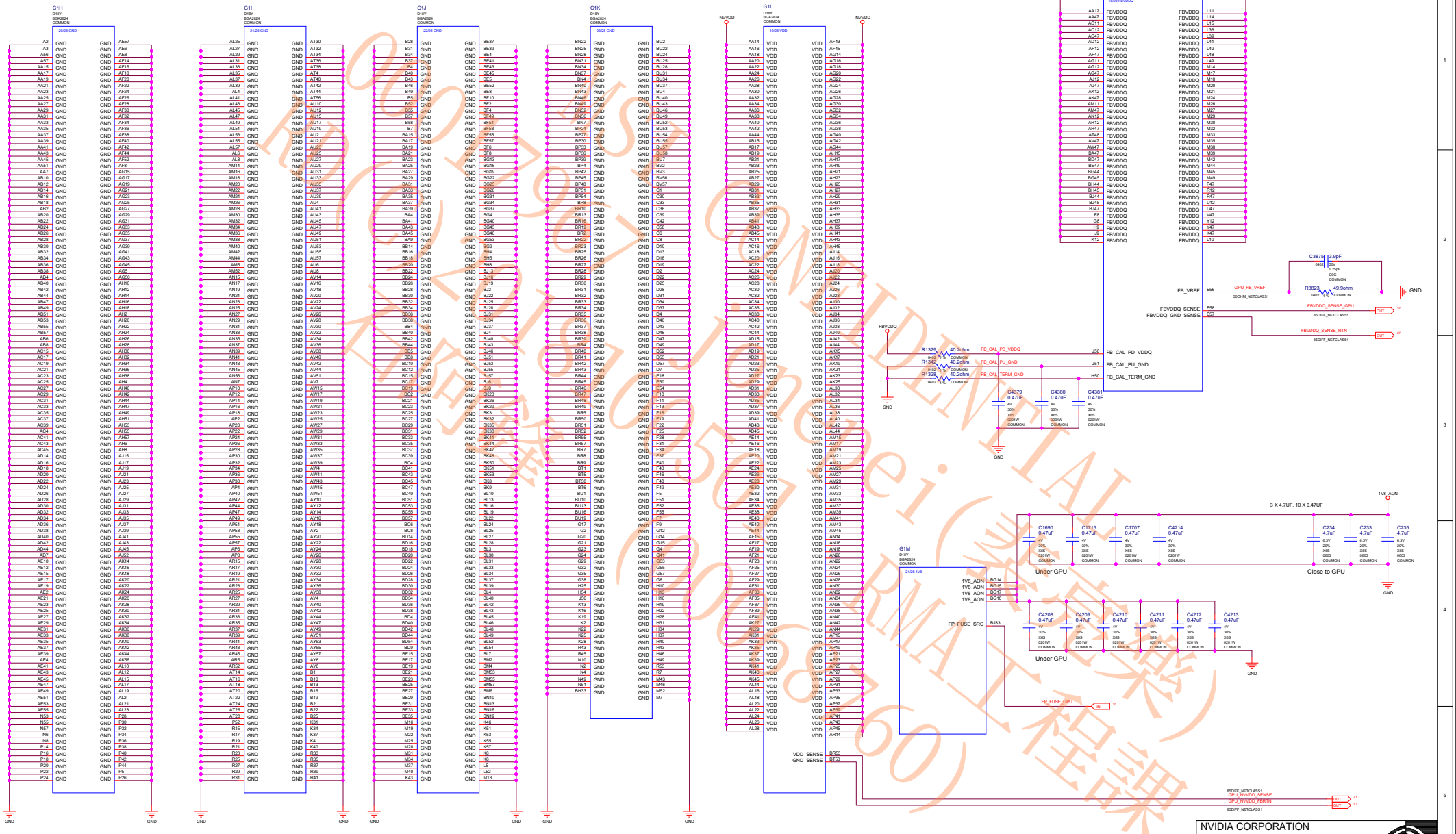
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	19 OF 66
BOM REV	A	DATE	09-JUL-2018

GPU PWR and GND



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR AND GND

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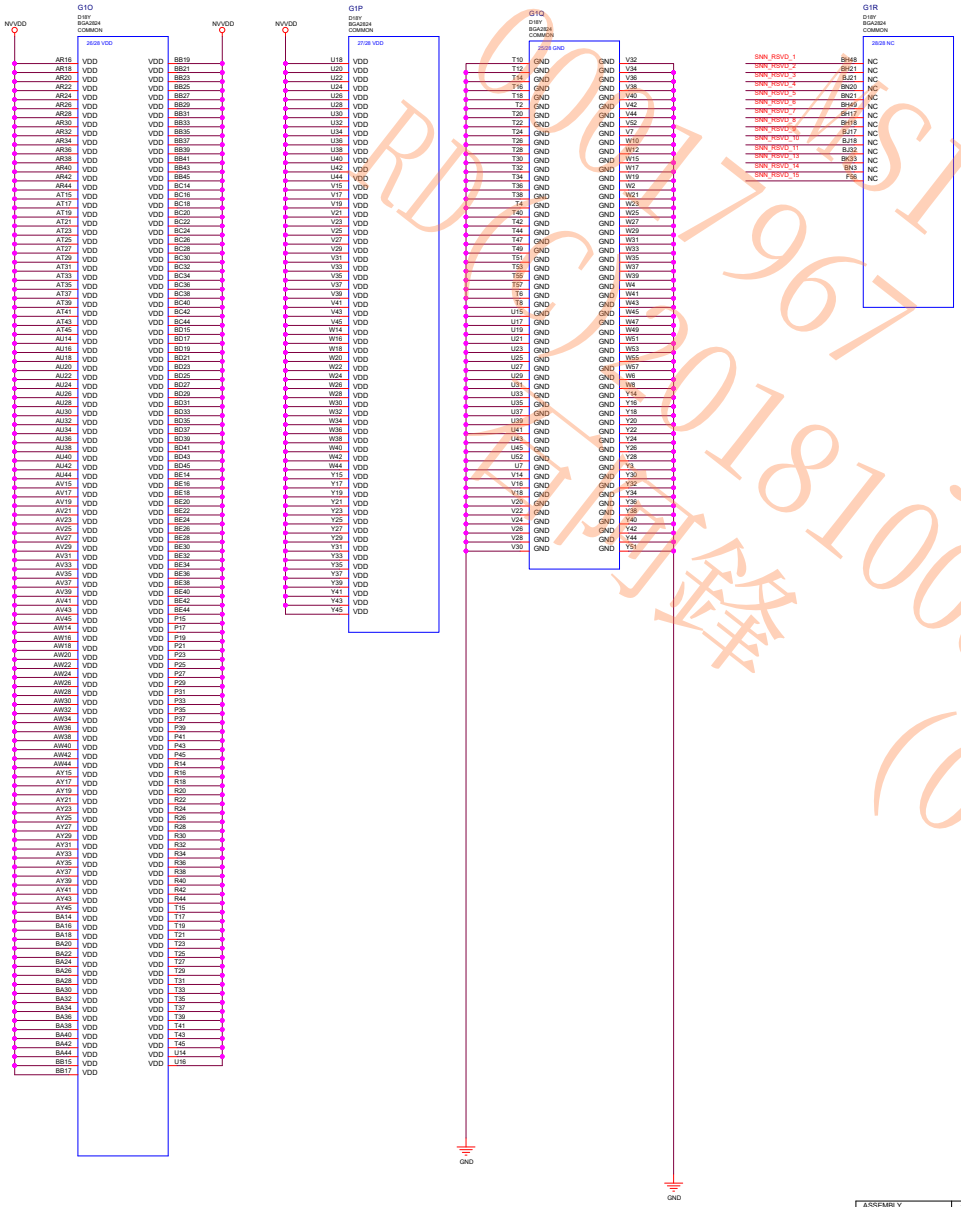
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	20 OF 66
BOM REV	A	DATE	09-JUL-2018

GPU PWR GND NCs



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RD(2018100501)

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR, GND and NCs

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	21 OF 66
BOM REV	A	DATE	09-JUL-2018

GPU Decoupling

FBVDDQ

FBVDDQ

Partition A
2 X 10UF, 6 X 0.47UF

C1616 0.47uF, C1704 0.47uF, C1583 0.47uF, C1599 0.47uF, C1557 0.47uF, C1555 0.47uF, C1639 10uF, C1734 10uF

Partition B
2 X 10UF, 6 X 0.47UF

C1508 0.47uF, C1438 0.47uF, C1386 0.47uF, C1457 0.47uF, C1497 0.47uF, C1468 0.47uF, C1534 10uF, C1428 10uF

Partition C
2 X 10UF, 6 X 0.47UF

C1387 0.47uF, C1374 0.47uF, C1383 0.47uF, C1401 0.47uF, C1375 0.47uF, C1411 0.47uF, C1361 10uF, C1376 10uF

Partition D
2 X 10UF, 6 X 0.47UF

C1392 0.47uF, C1368 0.47uF, C1373 0.47uF, C1367 0.47uF, C1382 0.47uF, C1385 0.47uF, C1378 10uF, C1384 10uF

Partition E
2 X 10UF, 6 X 0.47UF

C1427 0.47uF, C1443 0.47uF, C1418 0.47uF, C1458 0.47uF, C1393 0.47uF, C1370 0.47uF, C1398 10uF, C1464 10uF

Partition F
2 X 10UF, 6 X 0.47UF

C1568 0.47uF, C1473 0.47uF, C1587 0.47uF, C1507 0.47uF, C1545 0.47uF, C1489 0.47uF, C1629 10uF, C1579 10uF

Place close to GPU
6 X 10UF

C1377 10uF, C1331 10uF, C1372 10uF, C1576 10uF, C1744 10uF, C1347 10uF

Place close to GPU
14 x 22UF

C1684 22uF, C1334 22uF, C1337 22uF, C1511 22uF, C1553 22uF, C1332 22uF, C1421 22uF

C1470 22uF, C1338 22uF, C1399 22uF, C1439 22uF, C1335 22uF, C1610 22uF, C1607 22uF

NVVDD

NVVDD

1 X 470UF + 10 x 47UF overlap

C1577 470uF

PCB CO-LAYOUT

C1561 47uF, C1562 47uF, C1592 47uF, C1564 47uF, C1593 47uF, C1567 47uF, C1595 47uF, C1566 47uF, C1596 47uF, C1597 47uF

1 X 470UF + 10 x 47UF overlap

C1467 470uF

PCB CO-LAYOUT

C1479 47uF, C1480 47uF, C1447 47uF, C1485 47uF, C1448 47uF, C1486 47uF, C1452 47uF, C1449 47uF, C1481 47uF, C1450 47uF

12 X 47UF

C1590 47uF, C1591 47uF, C1446 47uF, C1559 47uF, C1563 47uF, C1565 47uF, C1589 47uF, C1487 47uF, C1453 47uF, C1484 47uF, C1451 47uF, C1483 47uF

6 X 22UF

C1455 22uF, C1624 22uF, C1422 22uF, C1434 22uF, C1594 22uF, C1623 22uF

30 X 10UF

C1653 10uF, C1652 10uF, C1651 10uF, C1642 10uF, C1403 10uF, C1514 10uF, C1521 10uF, C1400 10uF, C1515 10uF, C1517 10uF, C1686 10uF, C1615 10uF, C1614 10uF, C1638 10uF, C1636 10uF, C1516 10uF, C1520 10uF, C1519 10uF, C1518 10uF, C1513 10uF

C1645 10uF, C1644 10uF, C1643 10uF, C1677 10uF, C1543 10uF, C1432 10uF, C1620 10uF, C1433 10uF, C1407 10uF, C1536 10uF

16 X 4.7UF

C1541 4.7uF, C1424 4.7uF, C1619 4.7uF, C1429 4.7uF, C1634 4.7uF, C1539 4.7uF, C1617 4.7uF, C1425 4.7uF, C1535 4.7uF, C1537 4.7uF, C1626 4.7uF, C1431 4.7uF, C1542 4.7uF, C1404 4.7uF, C1540 4.7uF, C1538 4.7uF

80 X 0.47UF

C1442 0.47uF, C1462 0.47uF, C1419 0.47uF, C1660 0.47uF, C1510 0.47uF, C1631 0.47uF, C1569 0.47uF, C1532 0.47uF, C1406 0.47uF, C1414 0.47uF, C1627 0.47uF, C1548 0.47uF, C1490 0.47uF, C1408 0.47uF, C1656 0.47uF, C1549 0.47uF, C1454 0.47uF, C1469 0.47uF, C1552 0.47uF, C1533 0.47uF

C1426 0.47uF, C1588 0.47uF, C1410 0.47uF, C1499 0.47uF, C1649 0.47uF, C1655 0.47uF, C1436 0.47uF, C1554 0.47uF, C1475 0.47uF, C1474 0.47uF, C1394 0.47uF, C1676 0.47uF, C1466 0.47uF, C1460 0.47uF, C1635 0.47uF, C1498 0.47uF, C1494 0.47uF, C1570 0.47uF, C1440 0.47uF, C1413 0.47uF

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C1405 0.47uF, C1658 0.47uF, C1493 0.47uF, C1578 0.47uF, C1435 0.47uF, C1522 0.47uF, C1551 0.47uF, C1444 0.47uF, C1550 0.47uF, C1471 0.47uF, C1604 0.47uF, C1492 0.47uF, C1415 0.47uF, C1546 0.47uF, C1395 0.47uF, C1673 0.47uF, C1601 0.47uF, C1637 0.47uF, C1657 0.47uF, C1584 0.47uF

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PAGE DETAIL	GPU DECOUPLING

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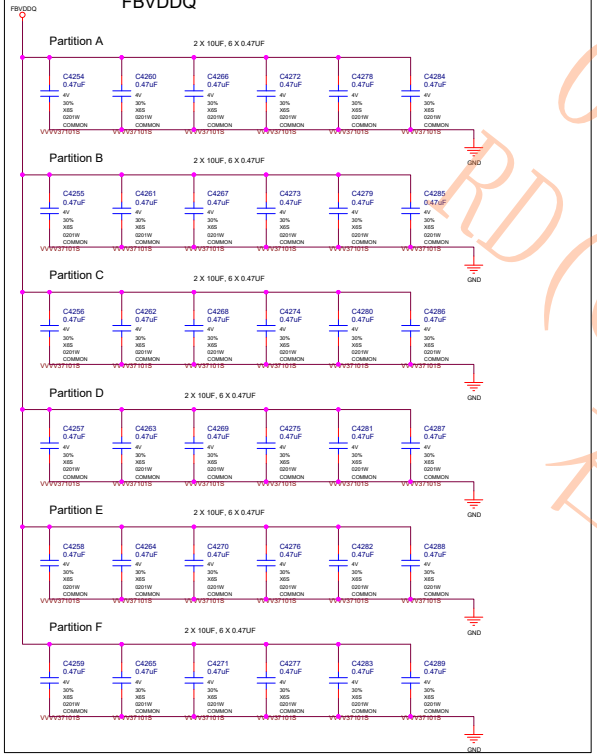
PCB REV	PG150-C03	PAGE	22 OF 66
BOM REV	A	DATE	09-JUL-2018

GPU Decoupling

FBVDDQ



NVVDD

0001706-1 NVIDIA CONFIDENTIAL
RD(C)2018100501 Jonepei(裴完樂)
石阿鋒 (00068760) RMA工程課

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING 2

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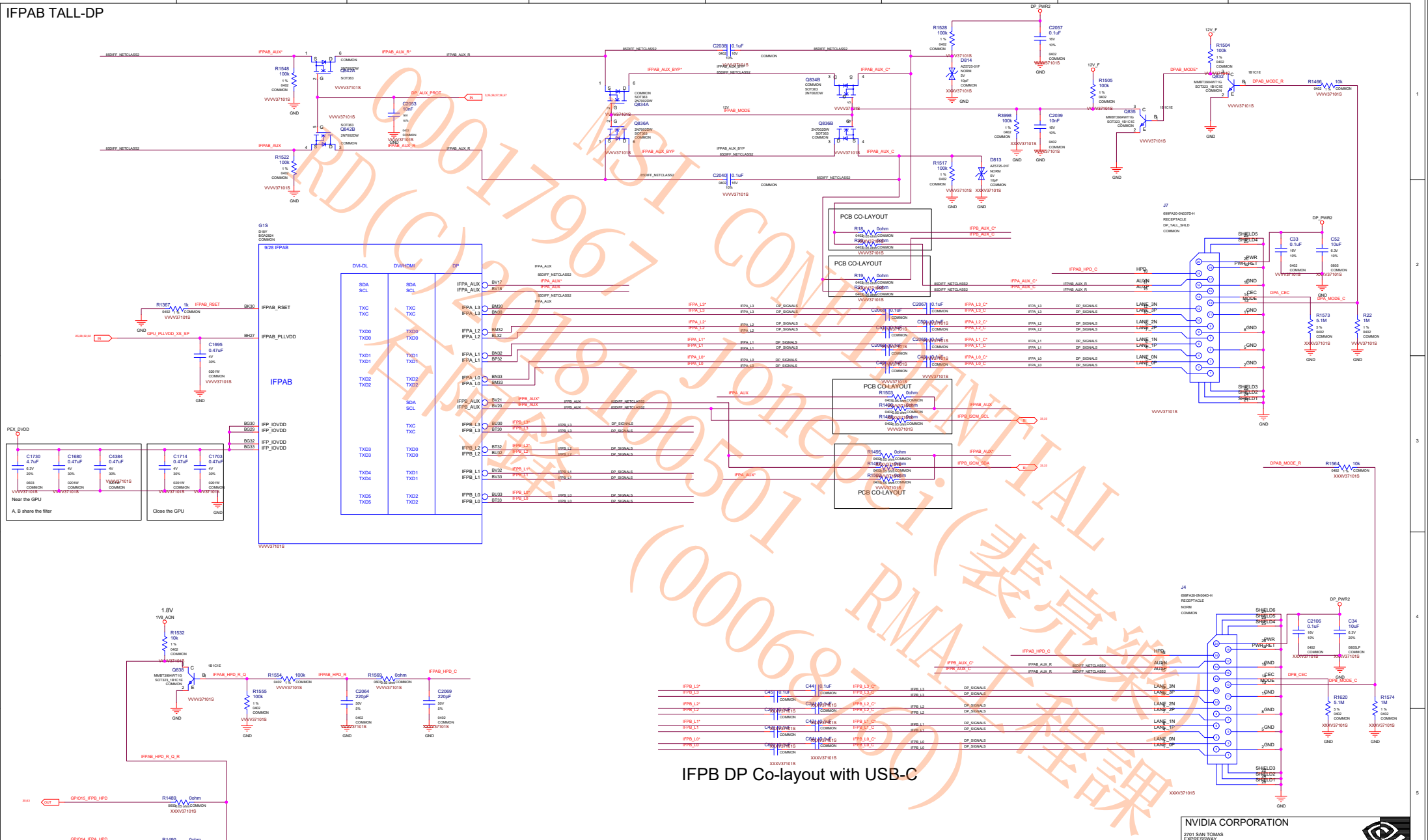
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	23 OF 66
BOM REV	A	DATE	09-JUL-2018

IFPAB TALL-DP



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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	24 OF 66
BOM REV	A	DATE	09-JUL-2018

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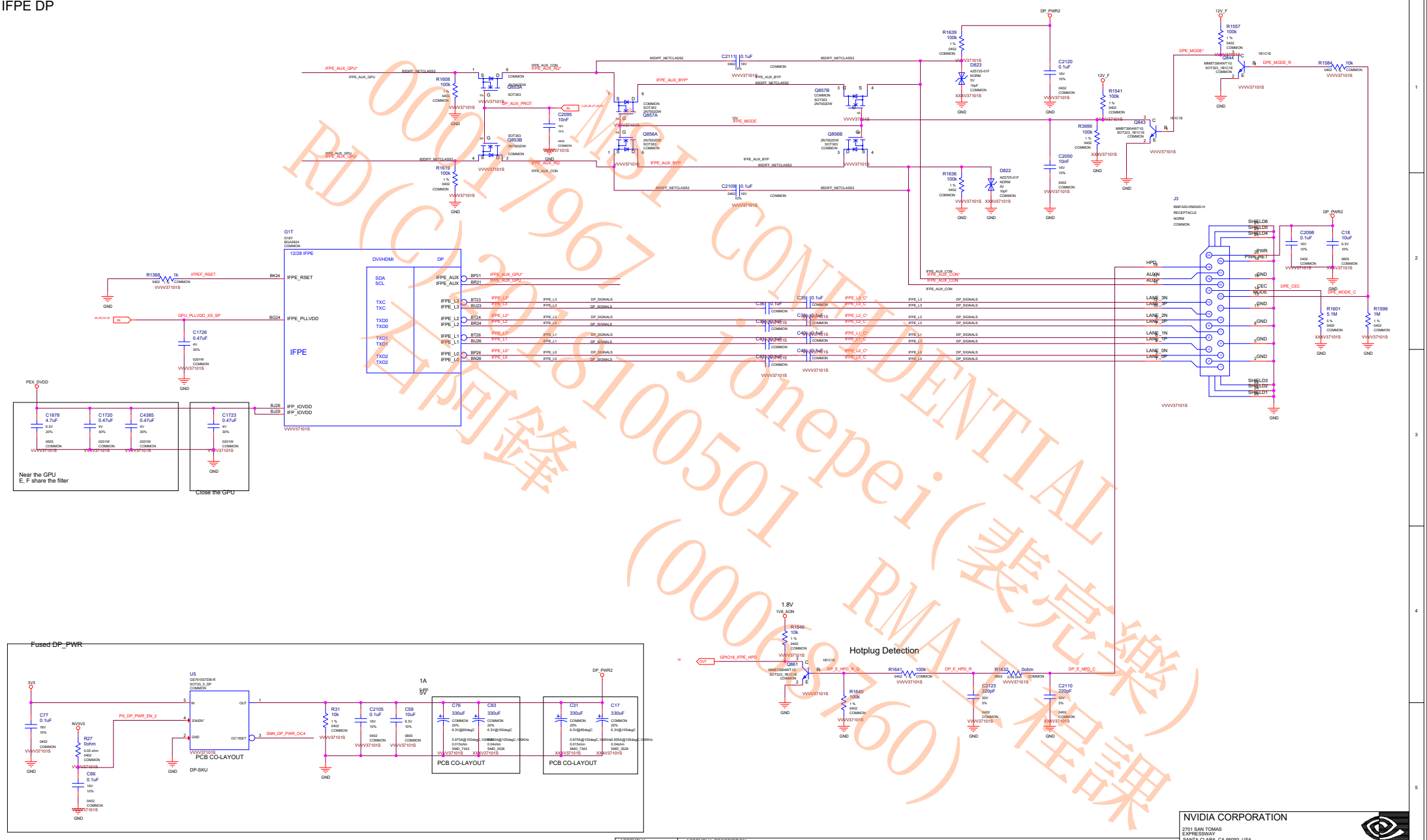

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PAGE DETAIL	IFPE DP

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	25 OF 66
BOM REV	A	DATE	09-JUL-2018

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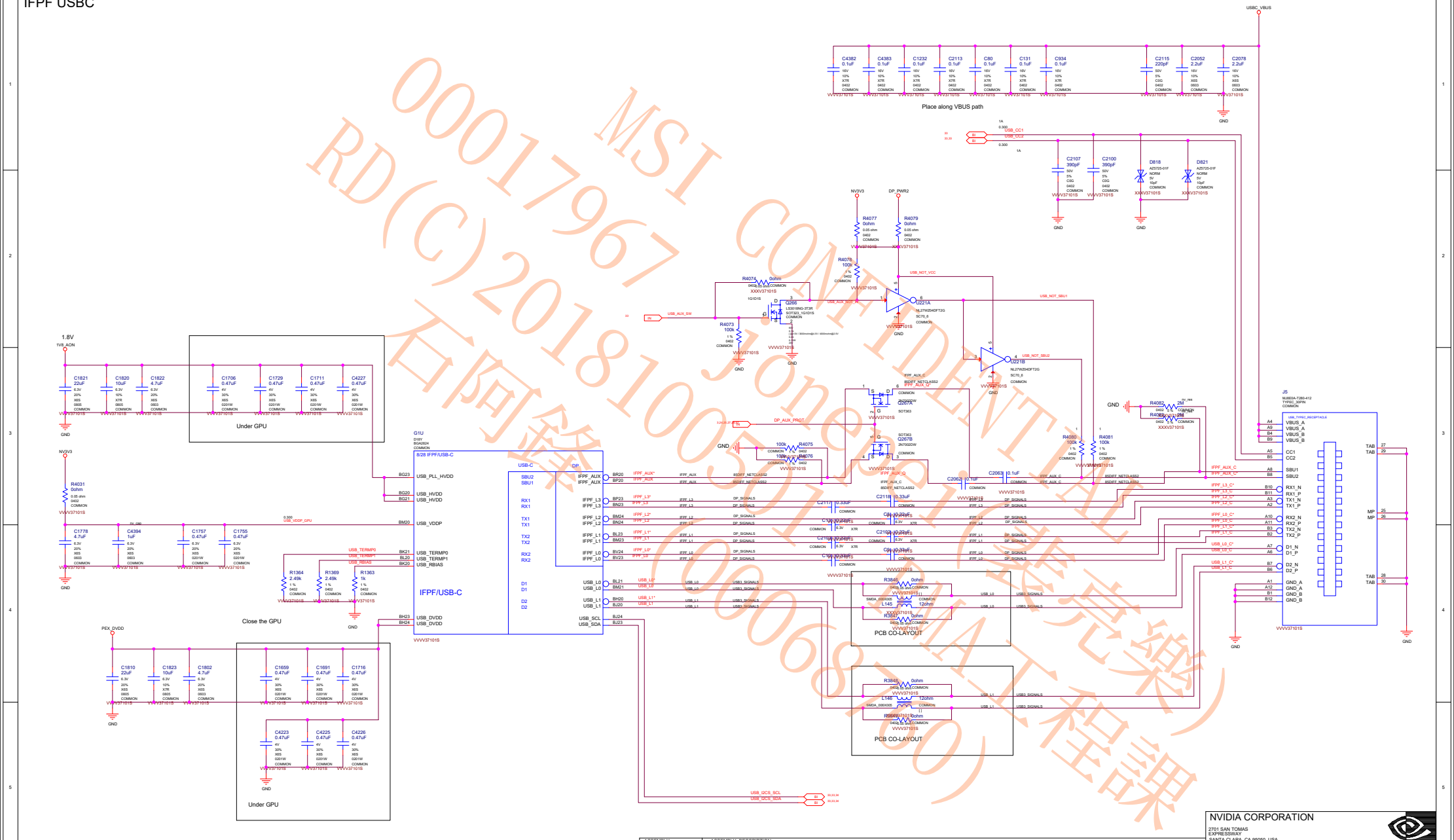

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石阿銘(0906820)
Jones Shih(完整版)

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PAGE DETAIL	IFPF USB

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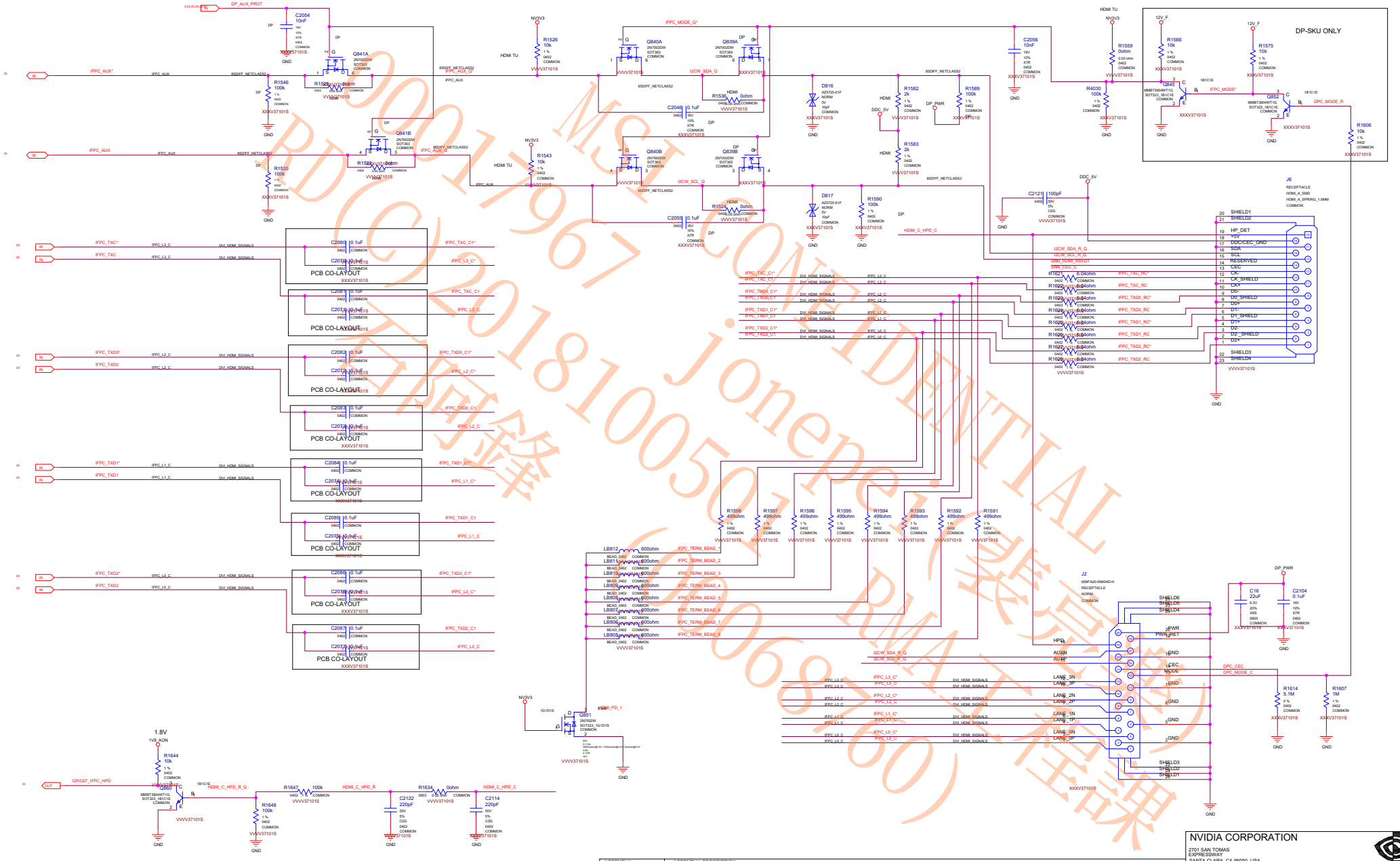
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	26 OF 66
BOM REV	A	DATE	09-JUL-2018

IFPC HDMI 2.0/DP



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPC HDMI/DP

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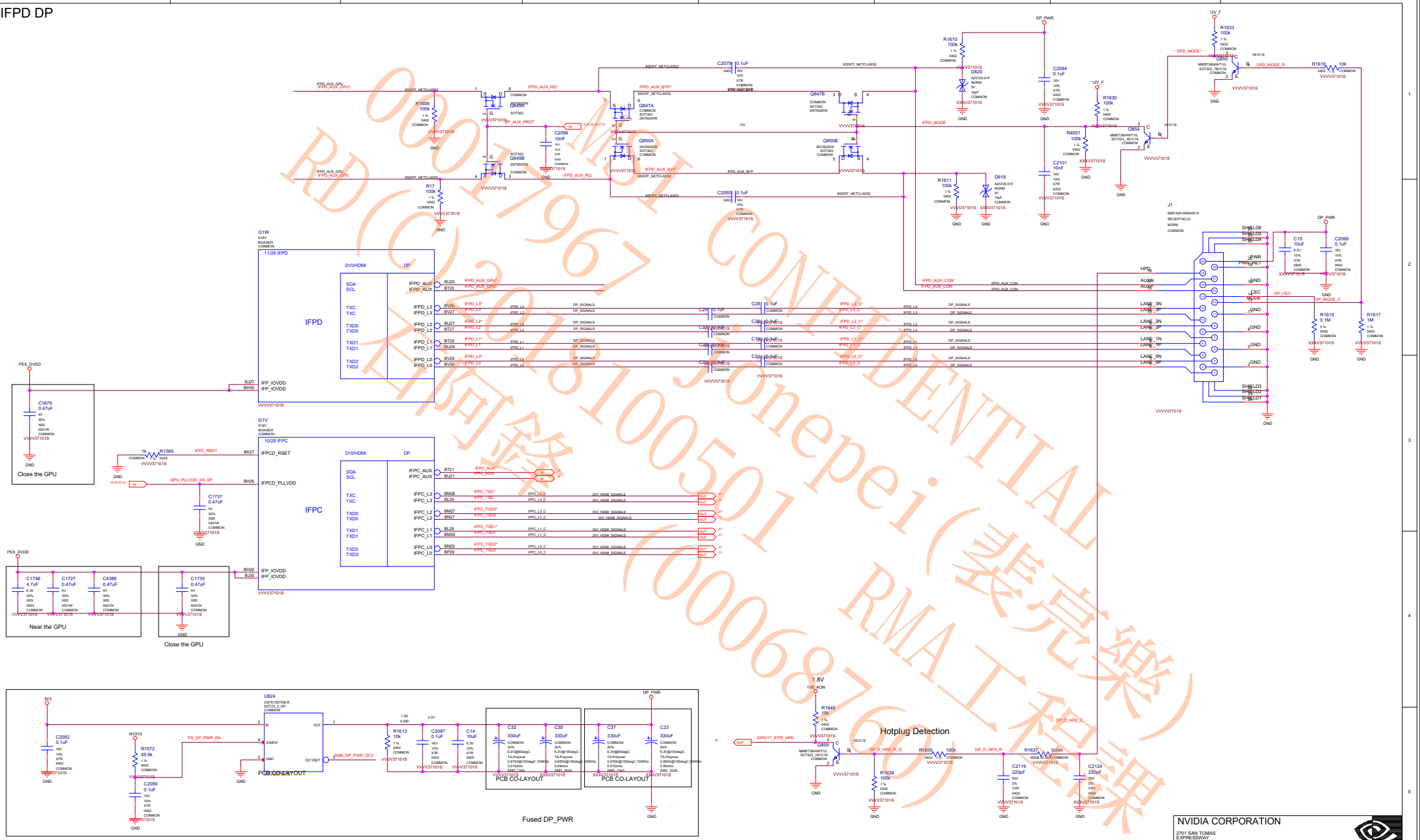
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	27 OF 66
BOM REV	A	DATE	09-JUL-2018

001967 Jonepei 20181005 (2068760) RMA 保密 RDC

IFPD DP



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPD DP

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	28 OF 66
BOM REV	A	DATE	09-JUL-2018

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NVHS Interface and FRAME LOCK

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	NVHS X16

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	29 OF 66
BOM REV	A	DATE	09-JUL-2018

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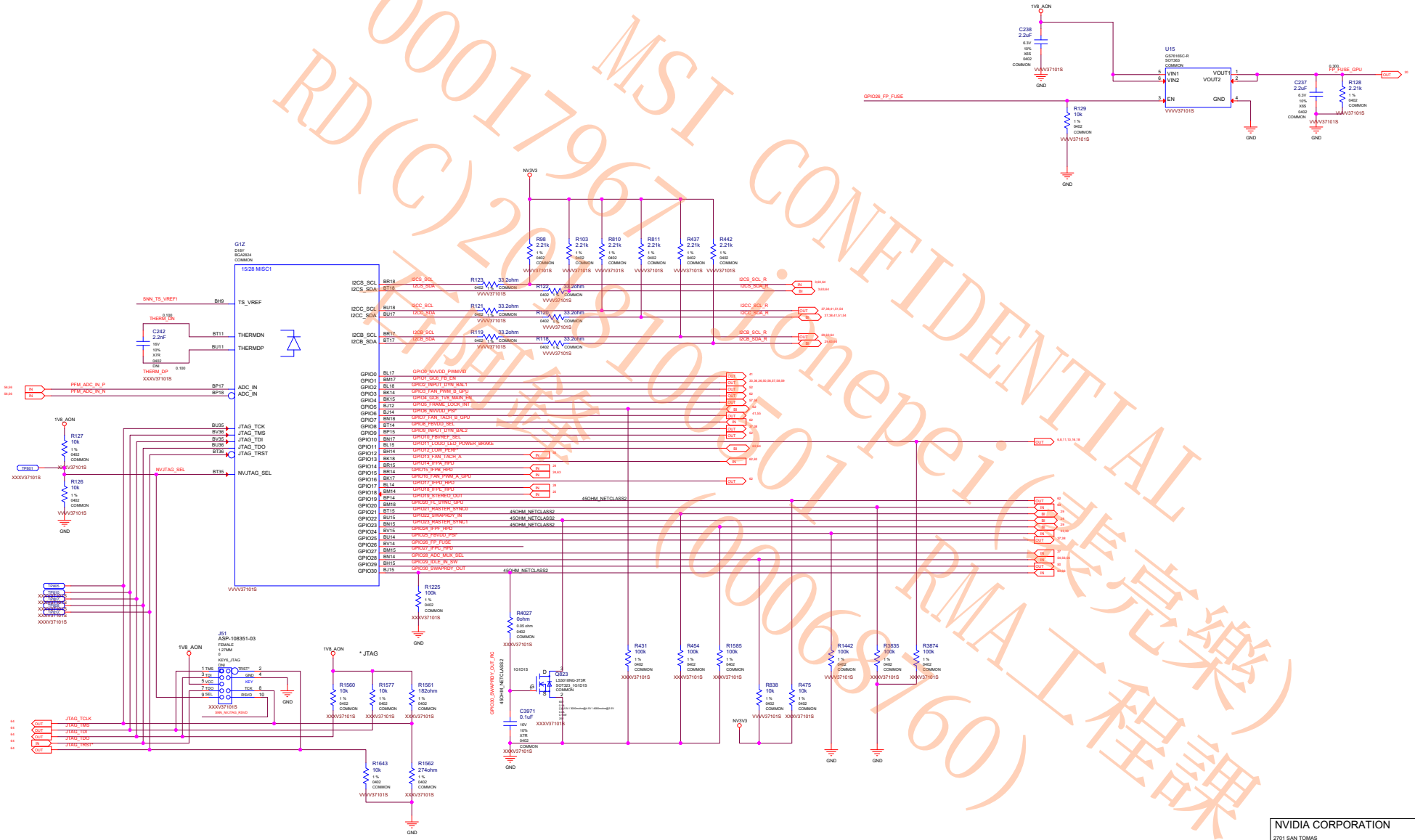
RD(GX)2018(0001)
Jonen.Li@163.com
阿鲜 (000680) 保密协议

MISC1: Fan, Thermal, JTAG, GPIO, STEREO



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0001796 Lionepei(張完樂)
RD(C)2018/10/01
內部機密 (000688760)
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: THERMAL, JTAG, GPIO, STEREO

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	30 OF 66
BOM REV	A	DATE	09-JUL-2018

MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	
L	L	H	00001	DEFAULT
L	H	L	00010	
L	H	H	00011	
H	L	L	00100	
H	L	H	00101	
H	H	L	00110	
H	H	H	00111	
L	L	M	01000	
L	M	L	01001	

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	H	XXX0	FS_OVERT DISABLE	

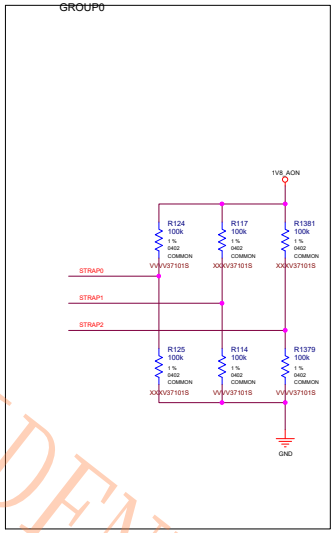
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	SKU 200

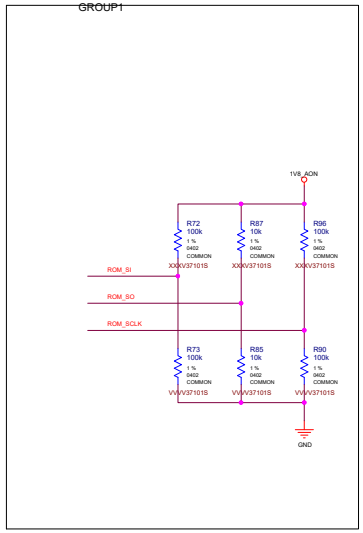
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

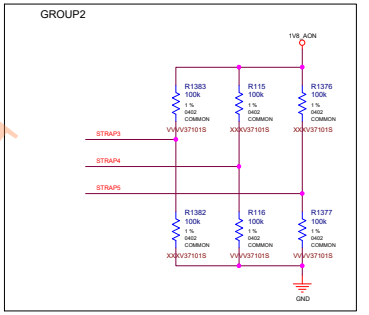
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

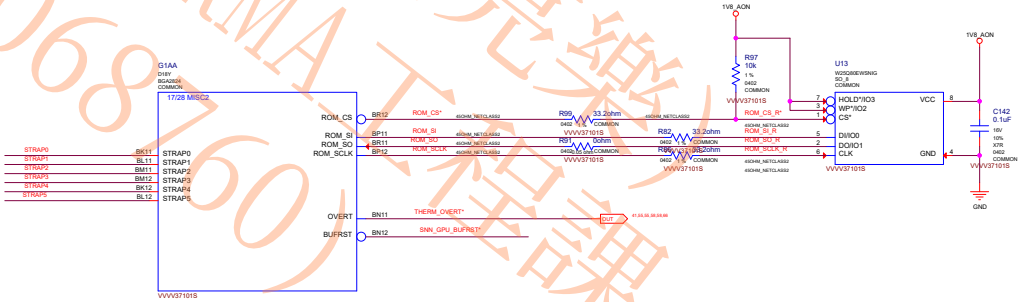
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE









ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: ROM, STRAPS

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	31 OF 66
BOM REV	A	DATE	09-JUL-2018

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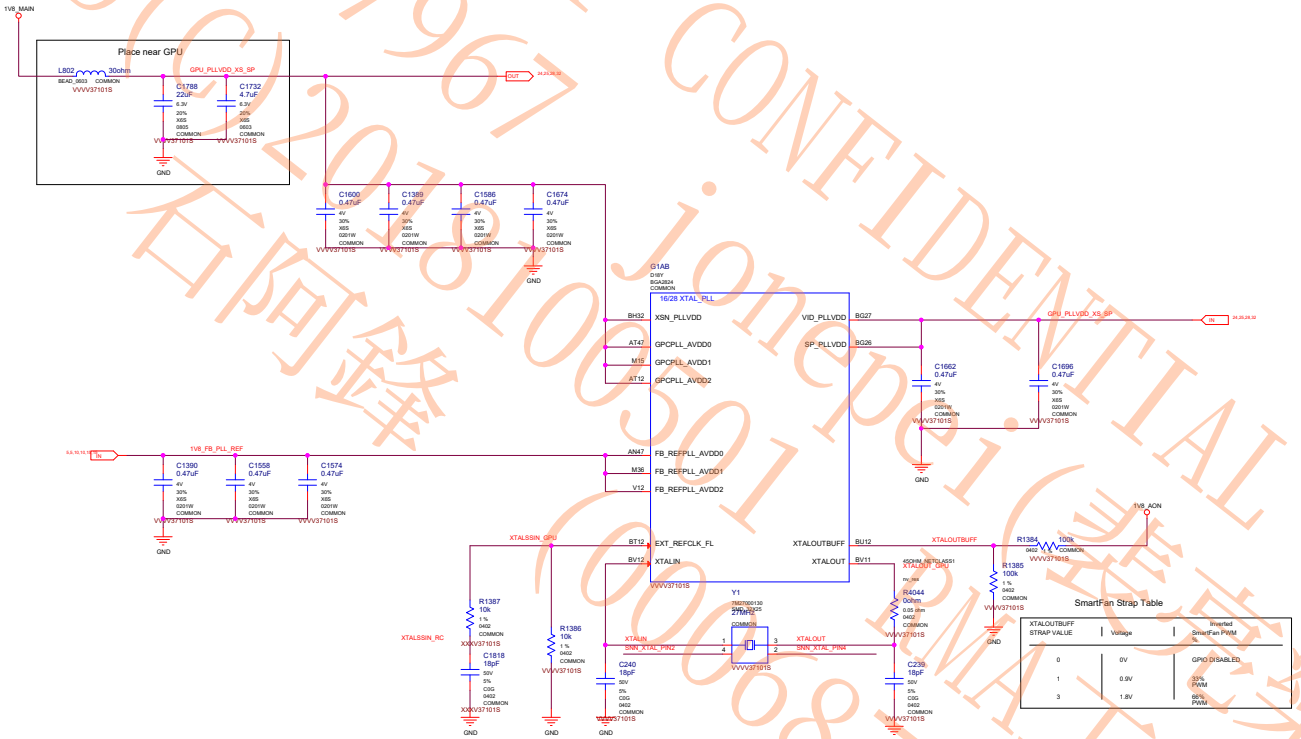
RD(C)2018100501 Jonepei(装完整个)
(0006876O) RMA下箱保

MISC2: XTAL. PLL



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jonepei(裴榮)
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: XTAL. PLL

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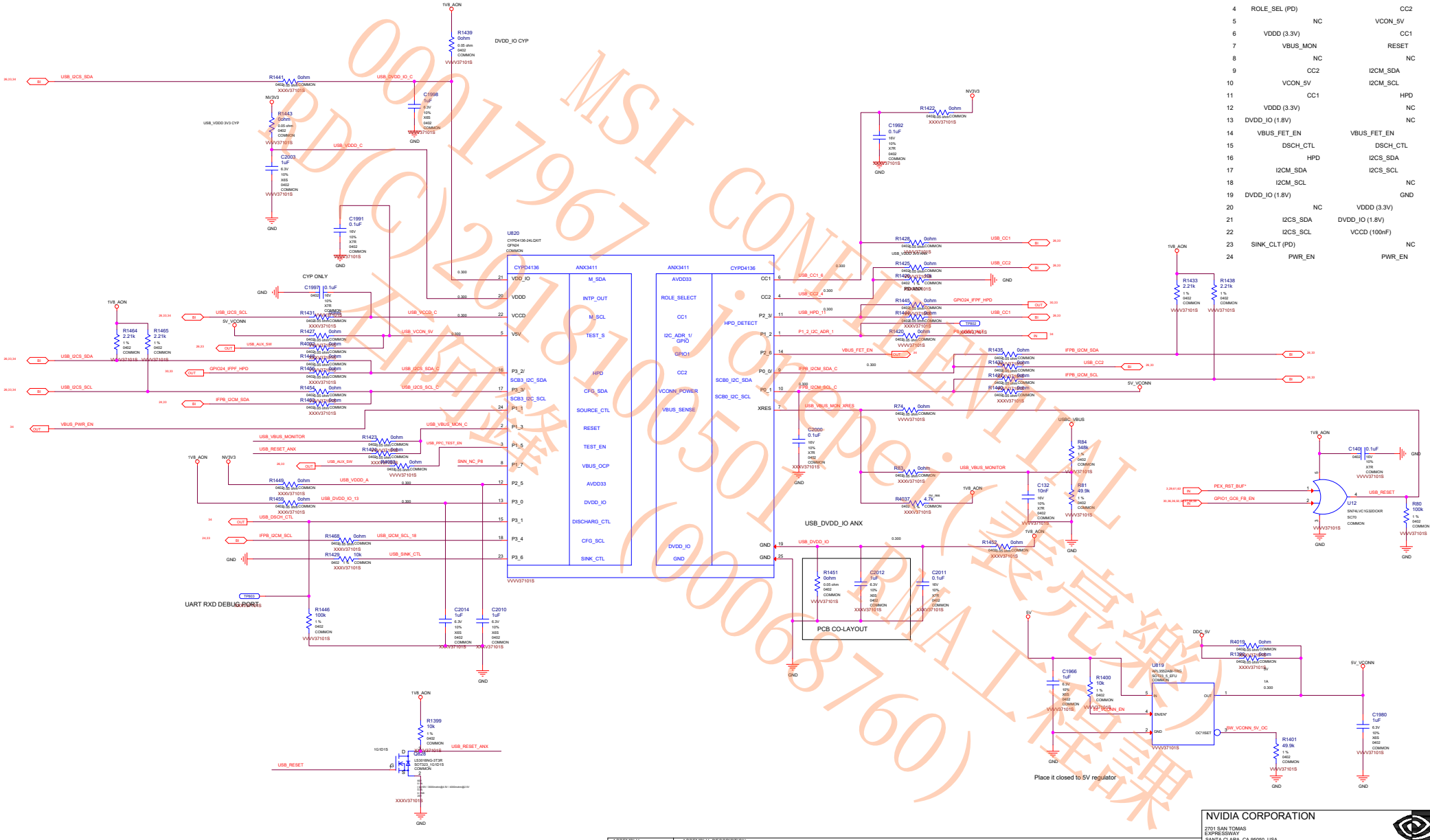
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	32 OF 66
BOM REV	A	DATE	09-JUL-2018

MISC: USB PPC



PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: USB PPC

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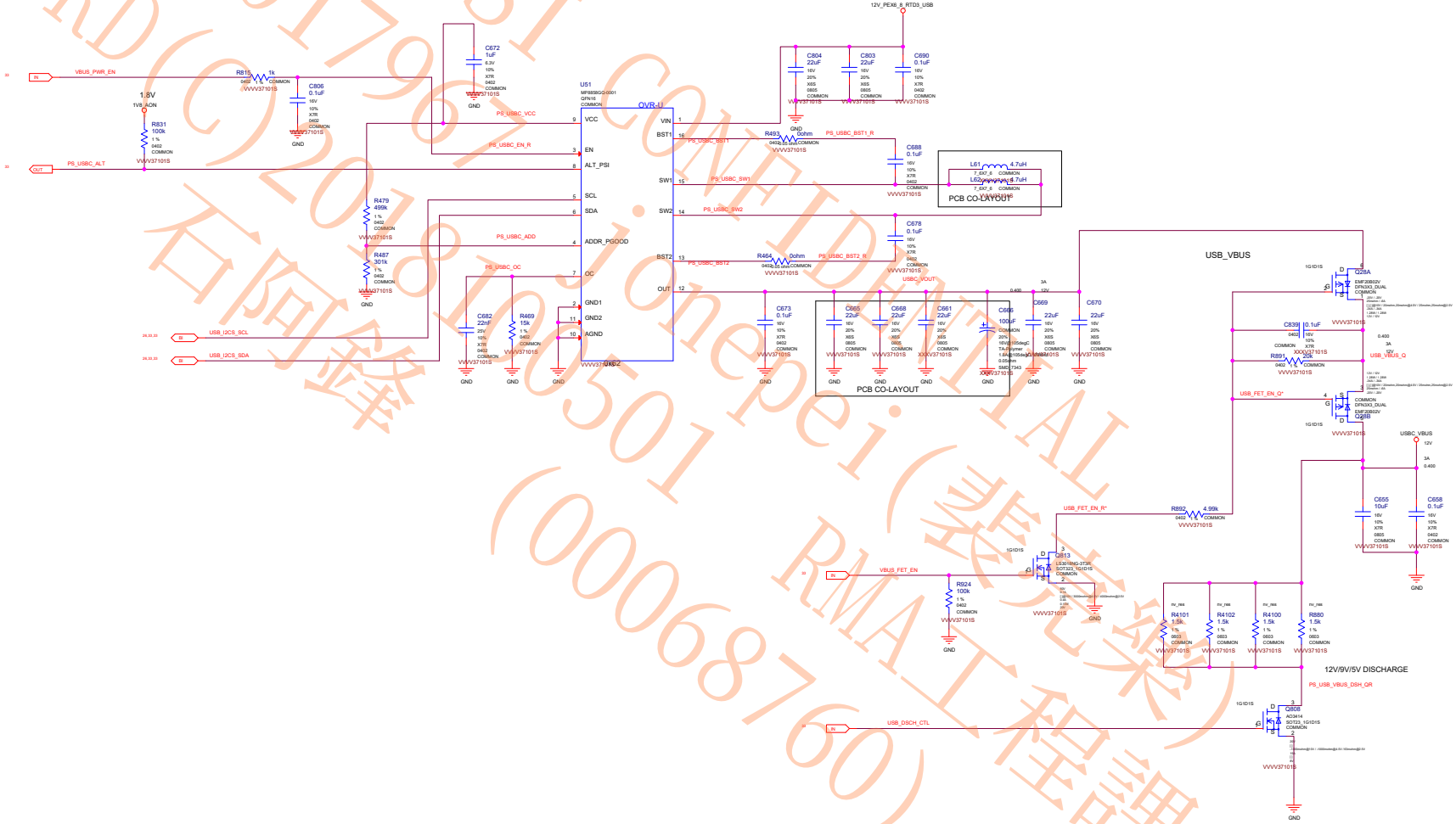
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	33 OF 66
BOM REV	A	DATE	09-JUL-2018

PS: USB VR



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: USB_C VR

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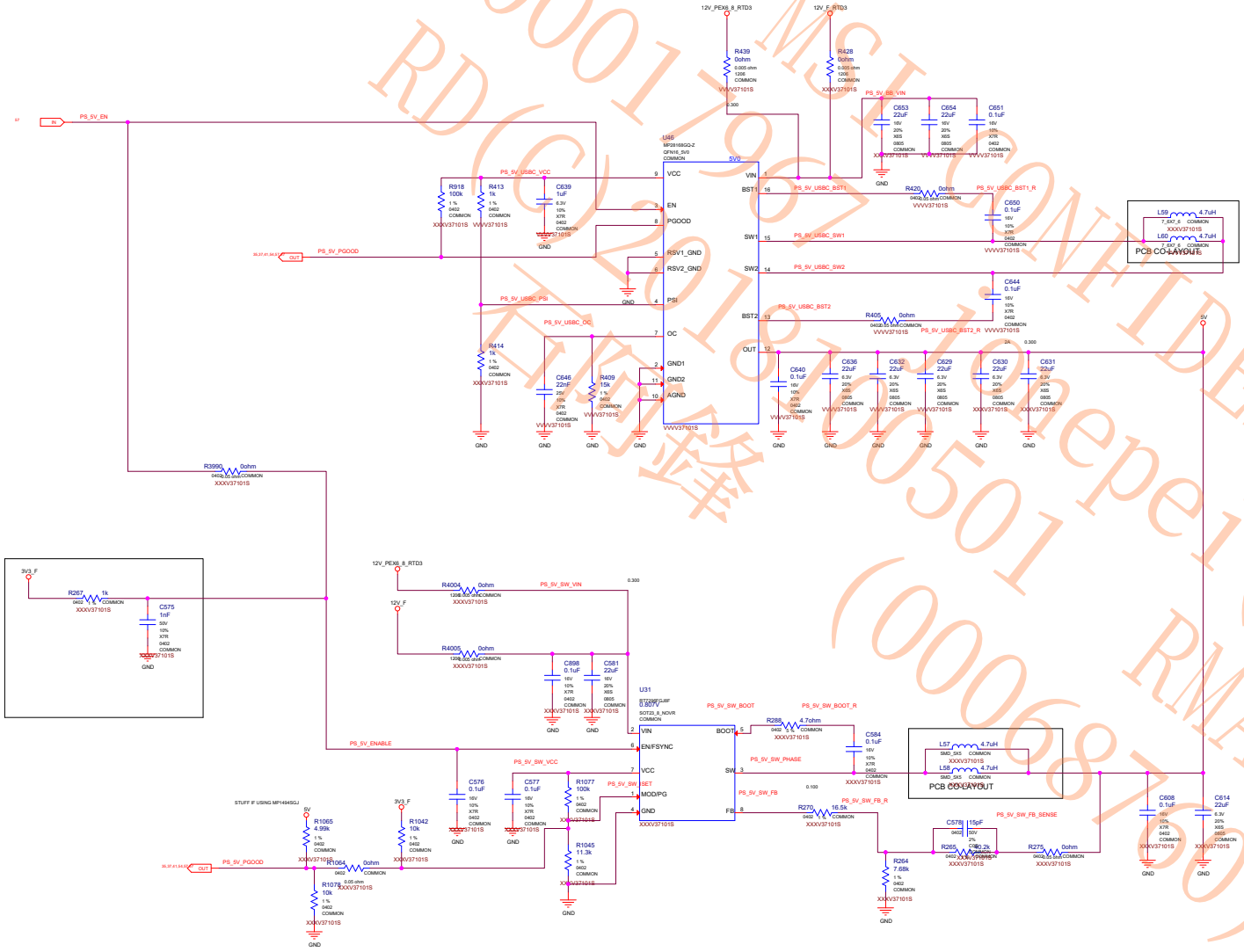
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	34 OF 66
BOM REV	A	DATE	09-JUL-2018

PS: 5V, 5V_BACKUP



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PAGE DETAIL	PS: 5V

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	35 OF 66
BOM REV	A	DATE	09-JUL-2018

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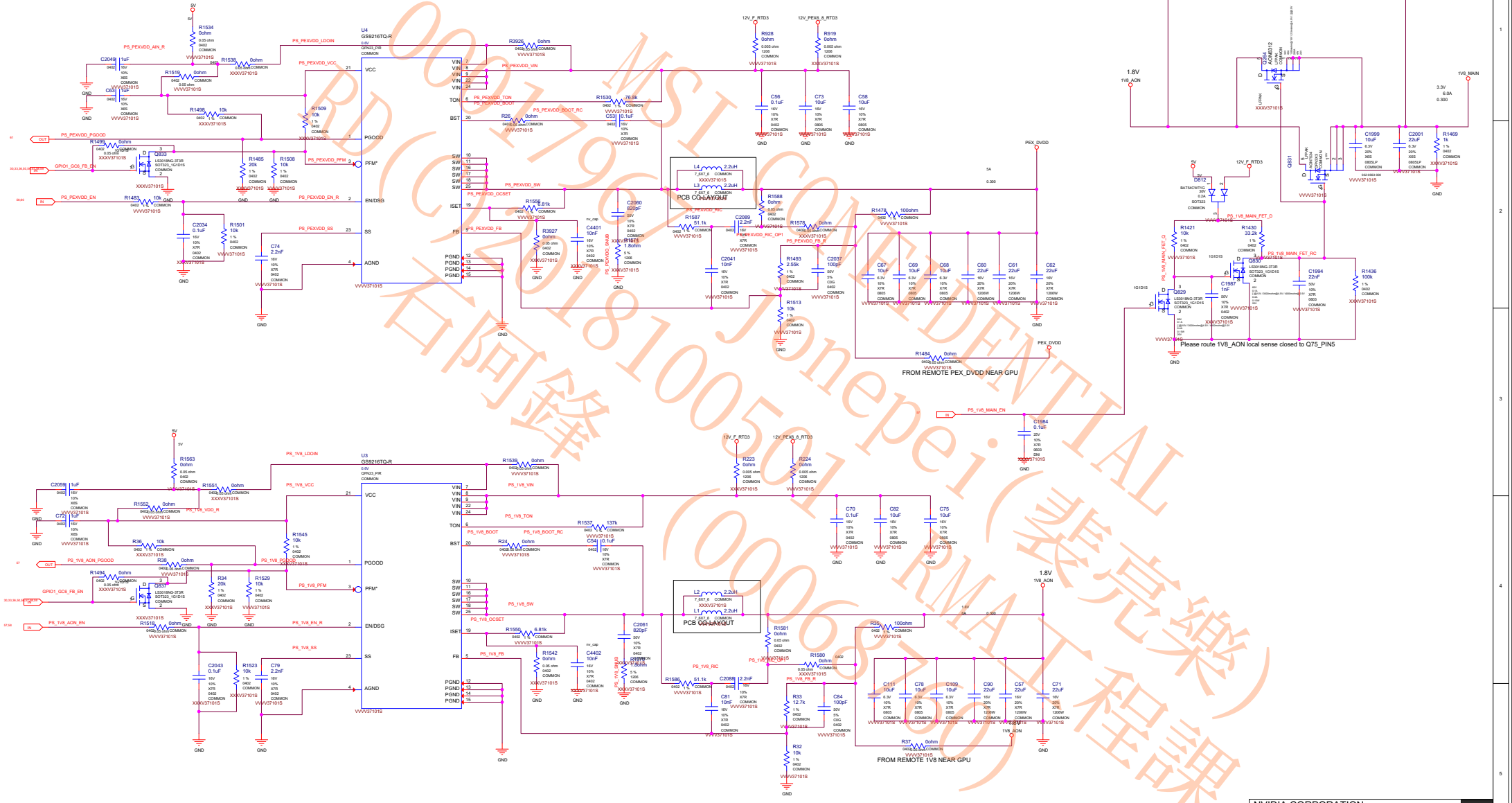
RD(C)2018/06/01 Honepei(裝完樂)
RMA工程課 (0006875)

PS: PEXVDD 1V8 Rail



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石阿锋

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PEXVDD 1V8 Rail

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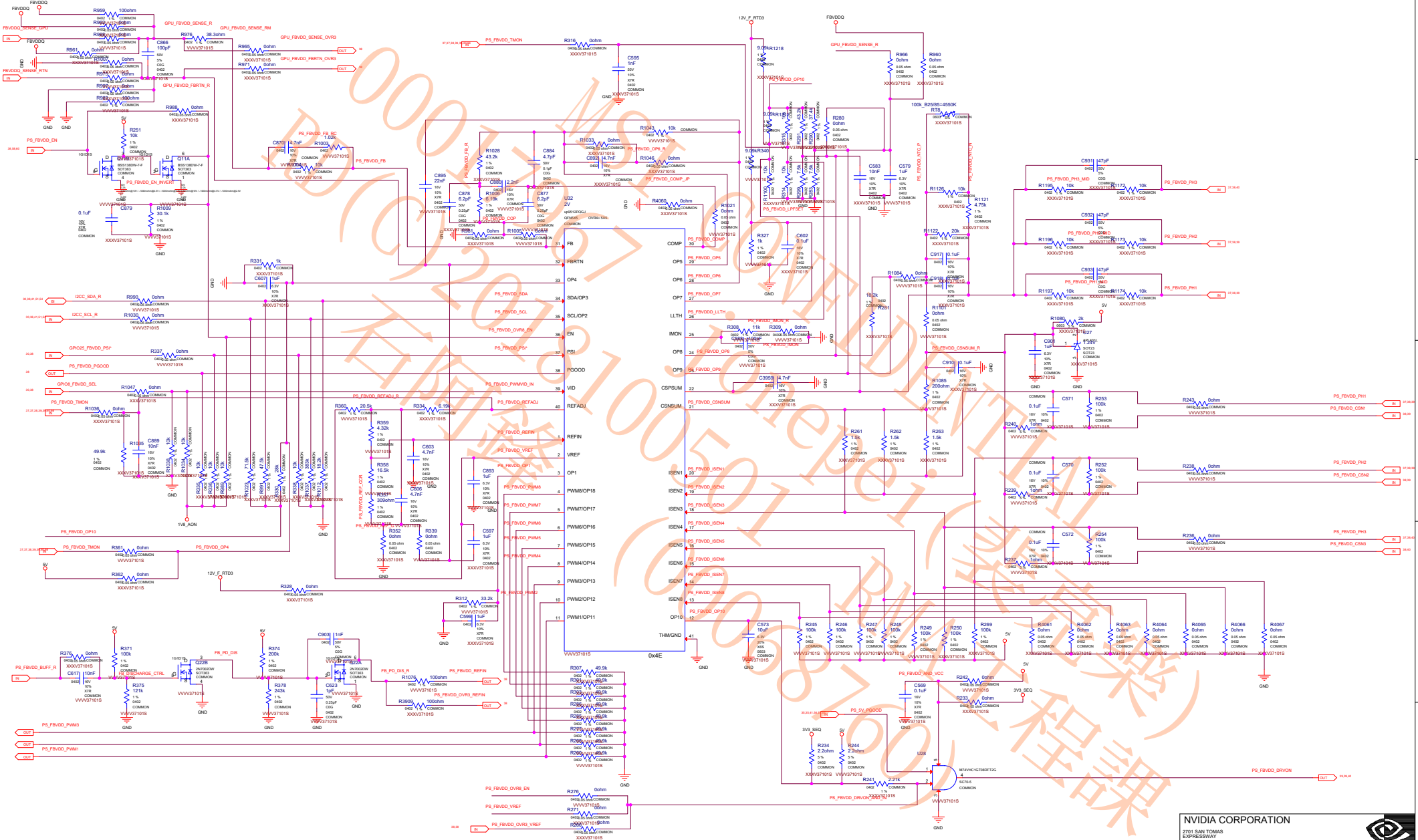
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	36 OF 66
BOM REV	A	DATE	09-JUL-2018

PS: FBVDD Controller



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDD Controller

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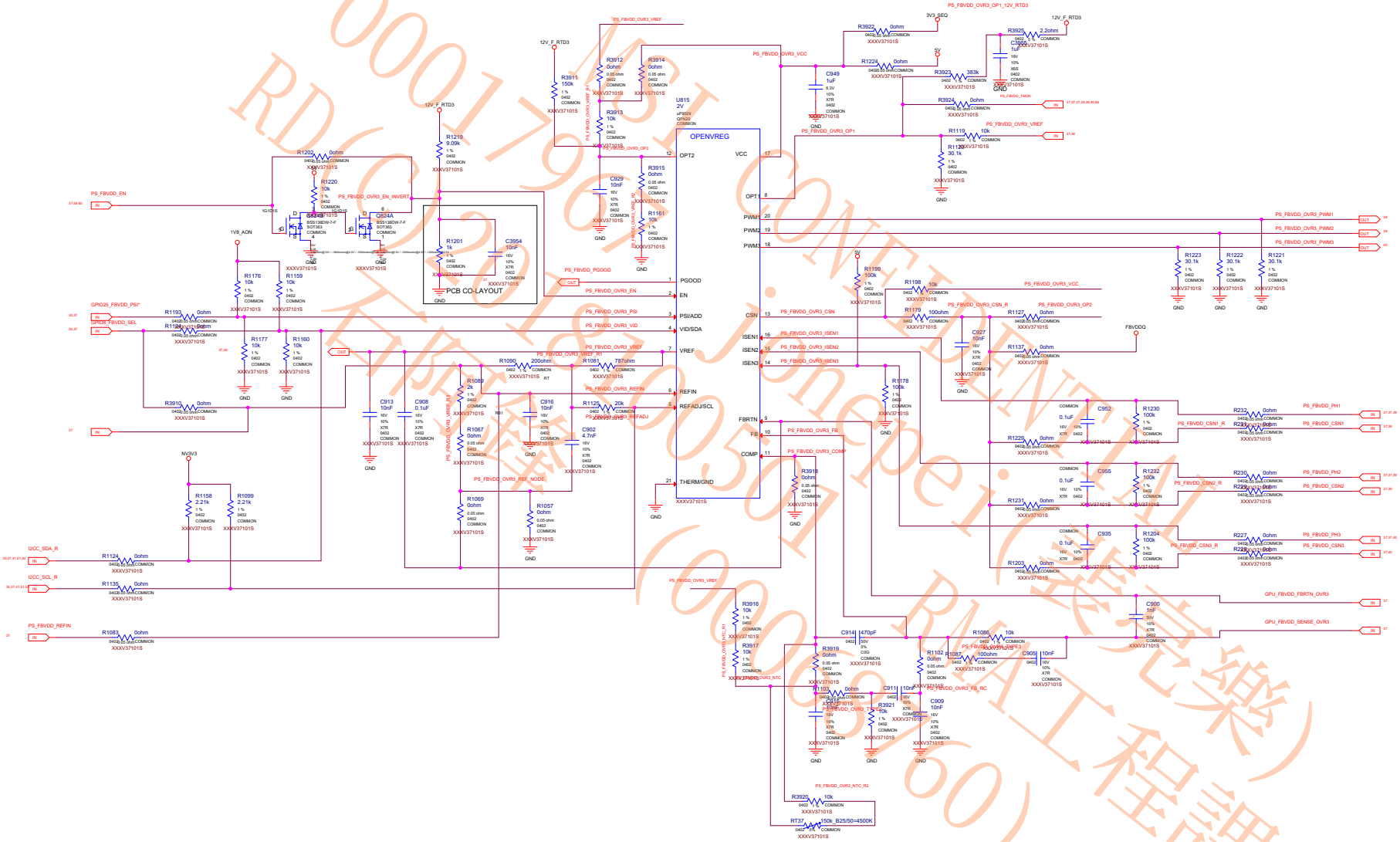
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	37 OF 66
BOM REV	A	DATE	09-JUL-2018

PS: FBVDD Controller OVR3



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDD Controller OVR3

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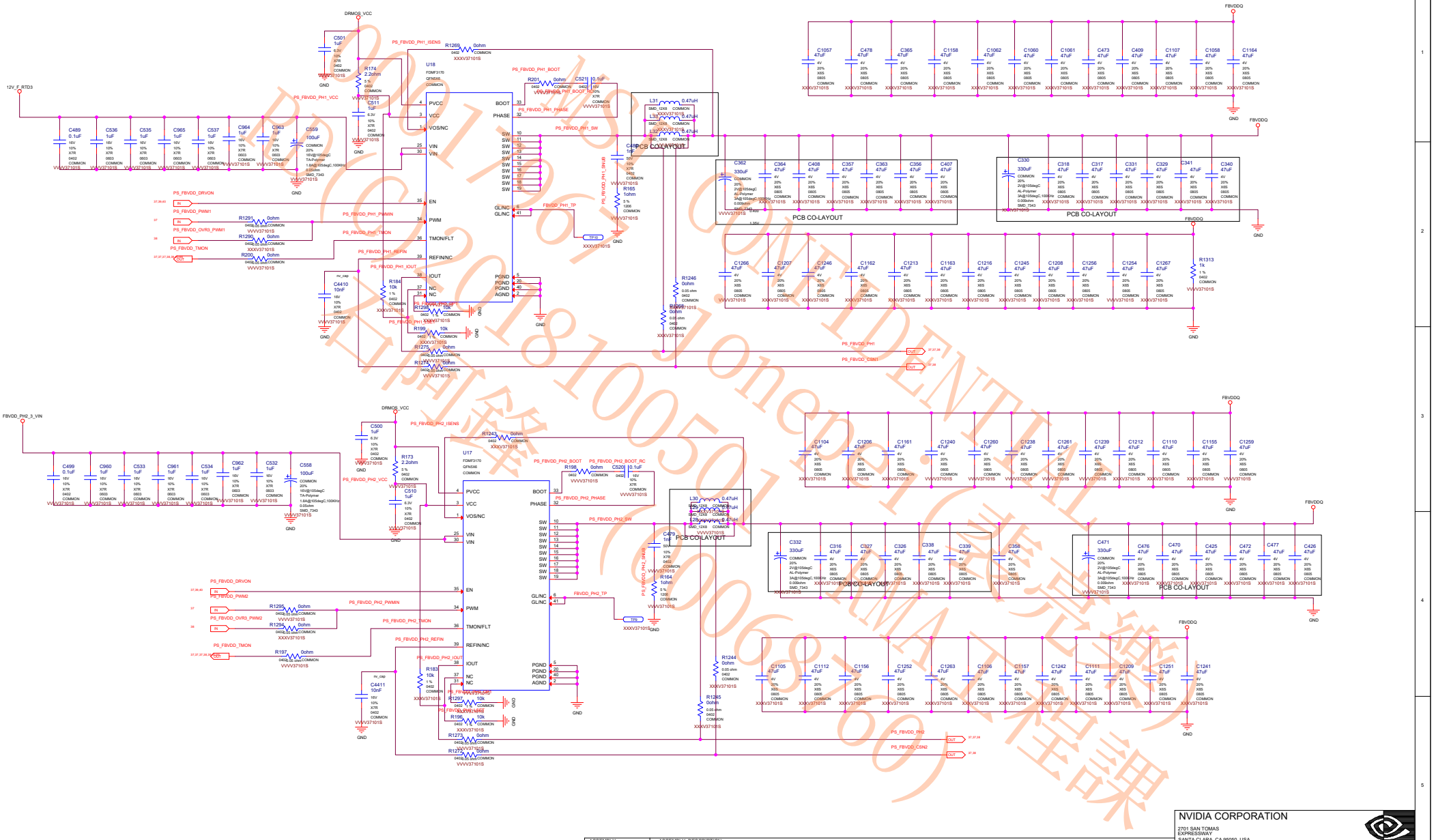
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	38 OF 66
BOM REV	A	DATE	09-JUL-2018

0001796 MSI CONFIDENTIAL Jenper(機密) RD(02)0501 RMA工程課 (000060)

PS: FBVDD PH1, 2



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDD Phase 1, 2

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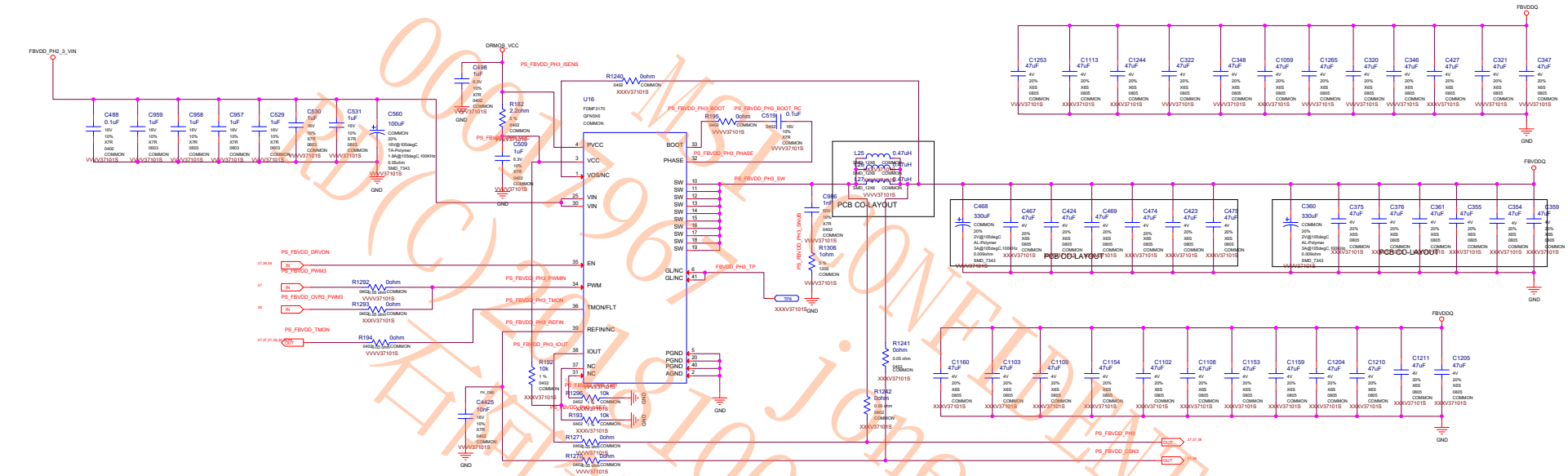
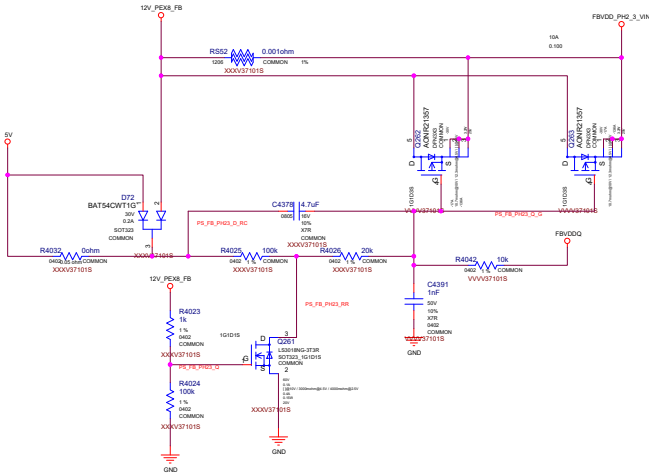
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	39 OF 66
BOM REV	A	DATE	09-JUL-2018

PS: FBVDD PH3





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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: FBVDD Phase 3

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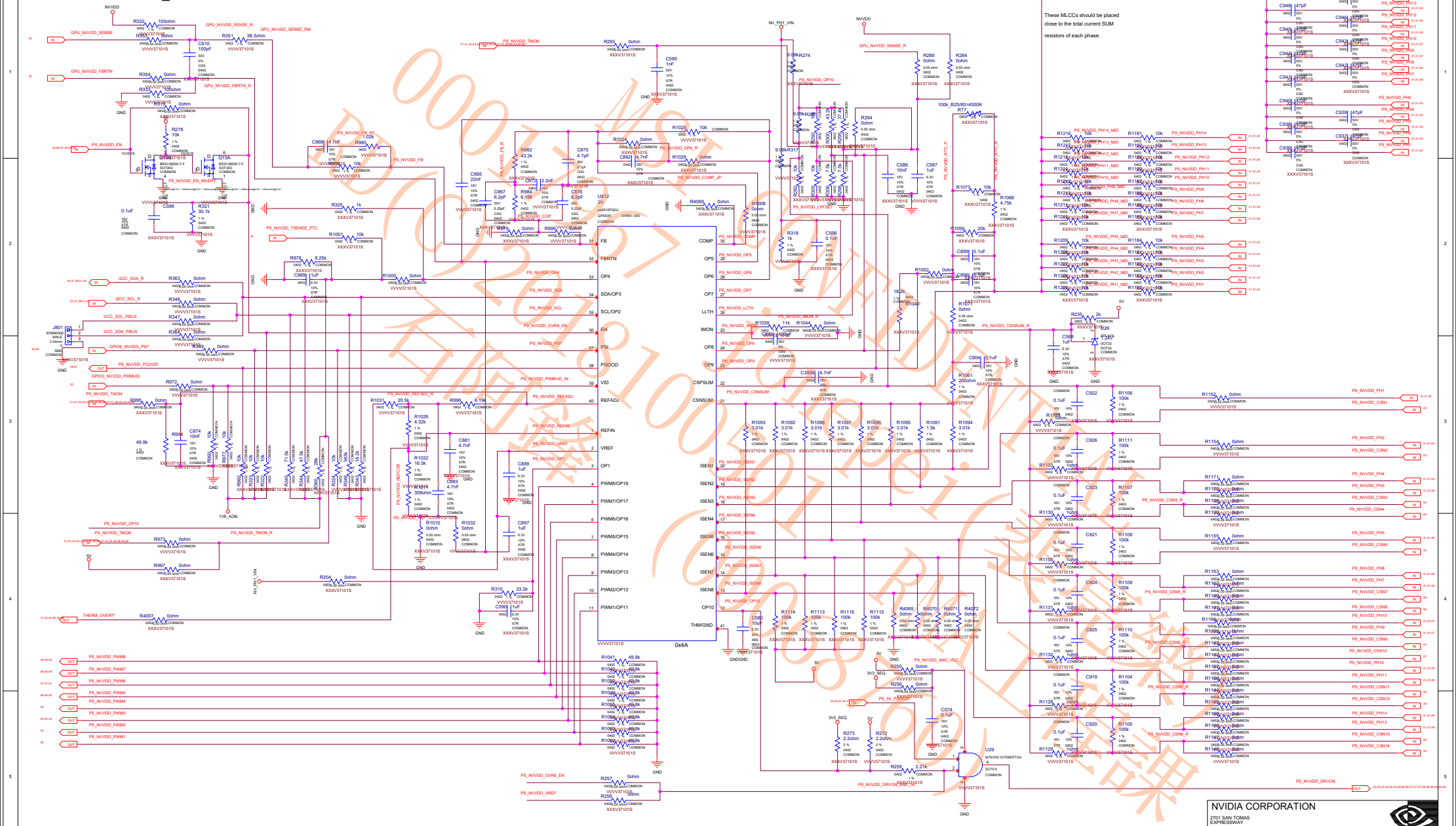
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	40 OF 66
BOM REV	A	DATE	09-JUL-2018

06121961 Manufacturer Jonepei(裝完樂) 100501 (00068760) RMA工程課 CONFIDENTIAL

PS: NVVDD Controller_OVR8



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PAGE DETAIL	PS: NVVDD Controller_OVR8

NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	41 OF 66
BOM REV	A	DATE	09-JUL-2018

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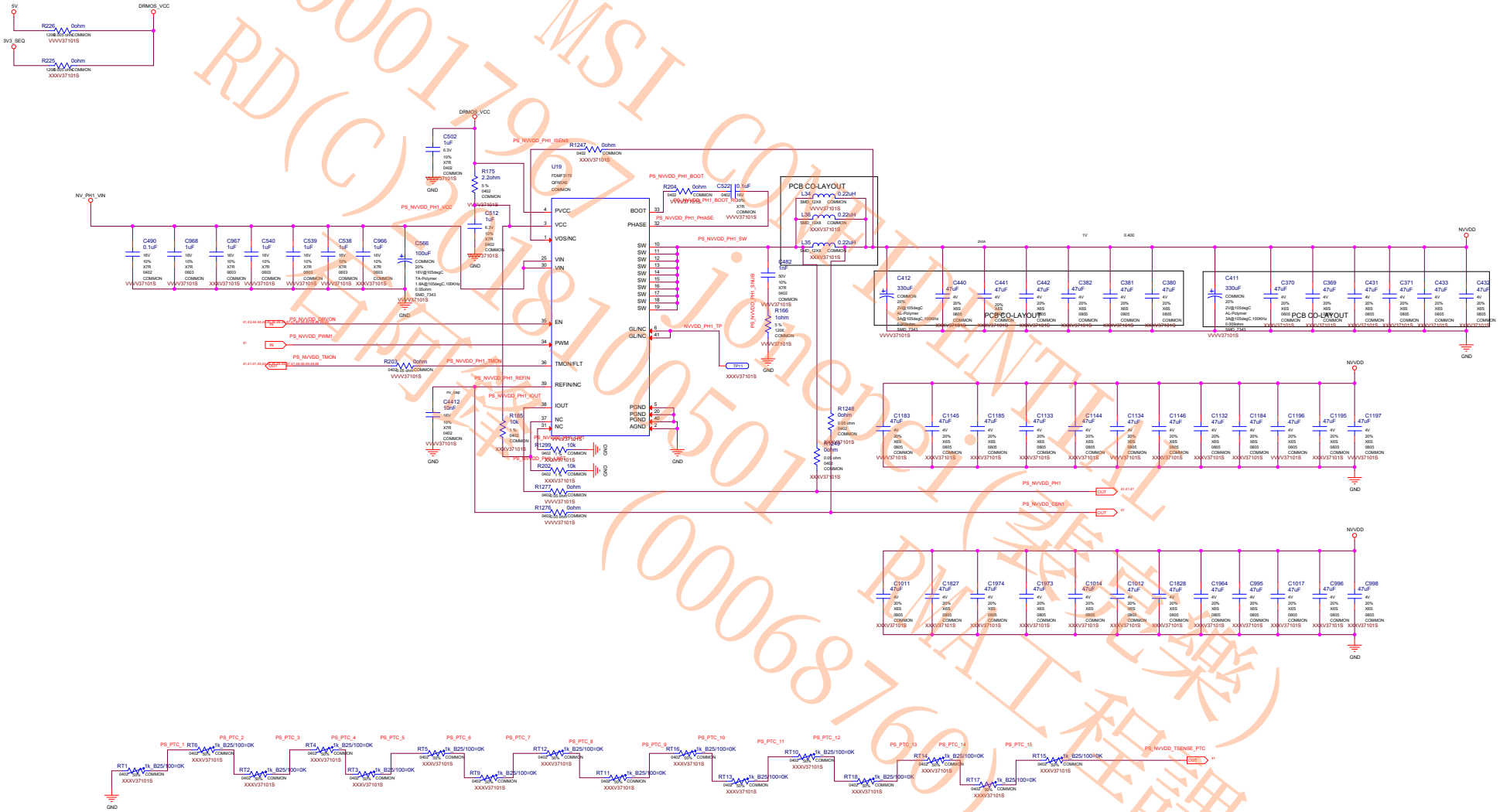
PS: NVVDD Phase 1



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0001796701 Jishenpei(紀慎培)
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Phase 1

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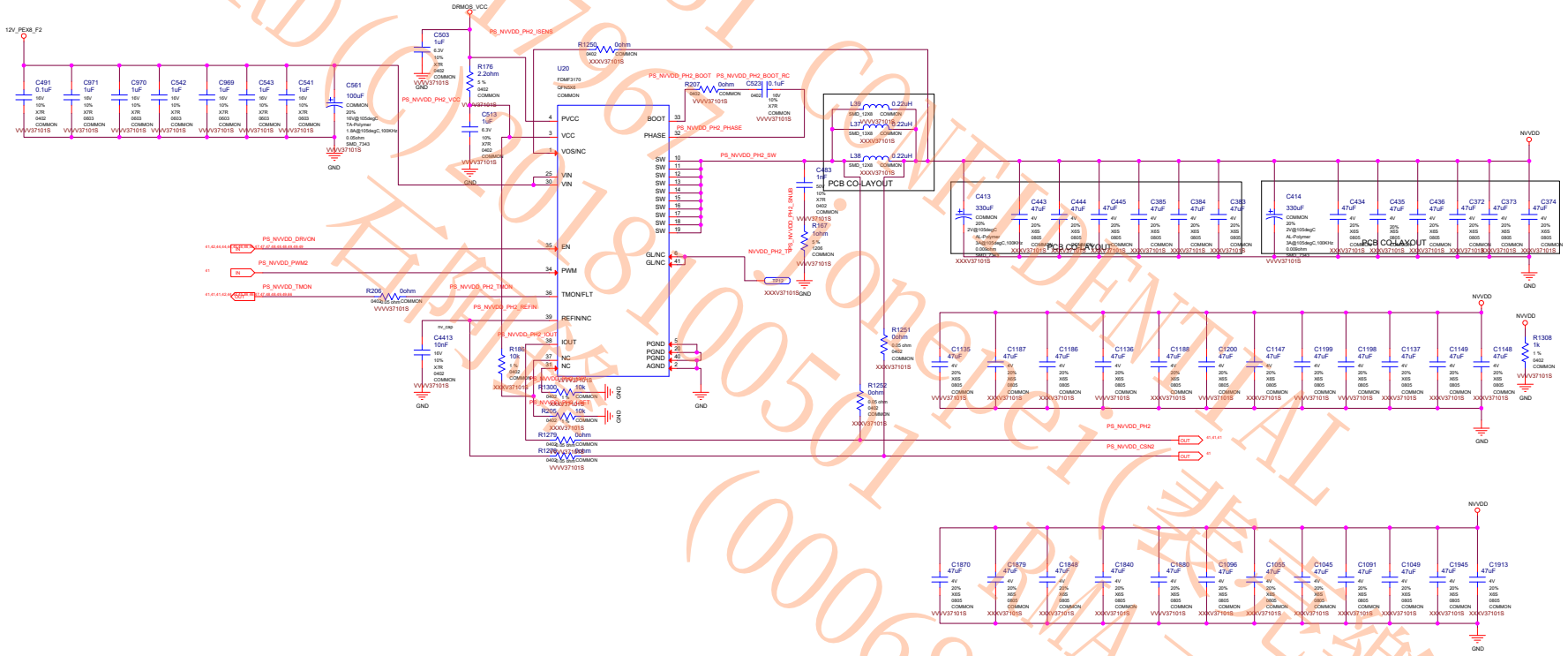
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	42 OF 66
BOM REV	A	DATE	09-JUL-2018

PS: NVVDD Phase 2



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: NVVDD Phase 2

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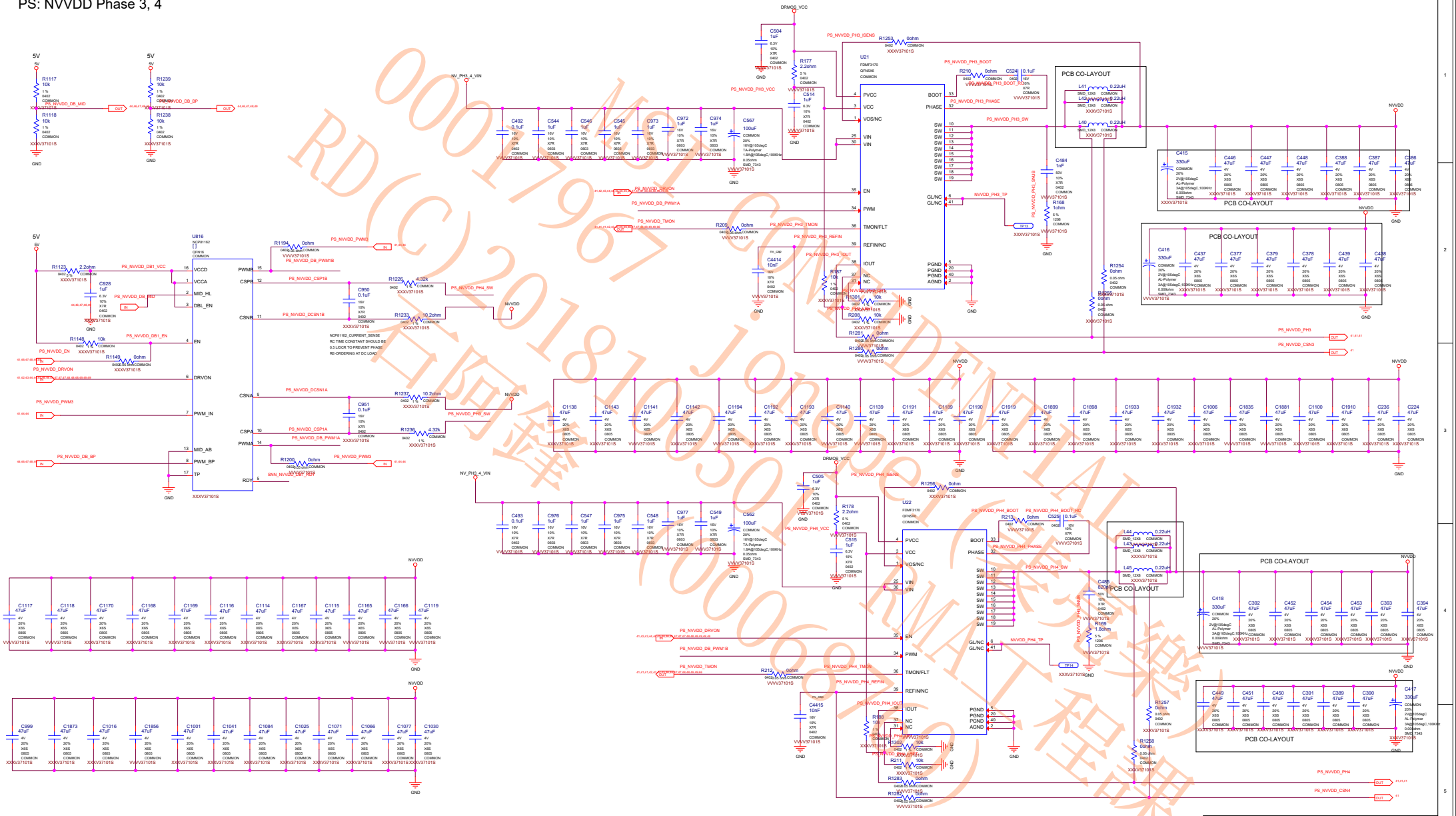
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	43 OF 66
BOM REV	A	DATE	09-JUL-2018

PS: NVVDD Phase 3, 4



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PAGE DETAIL	PS: NVVDD Phase 3, 4

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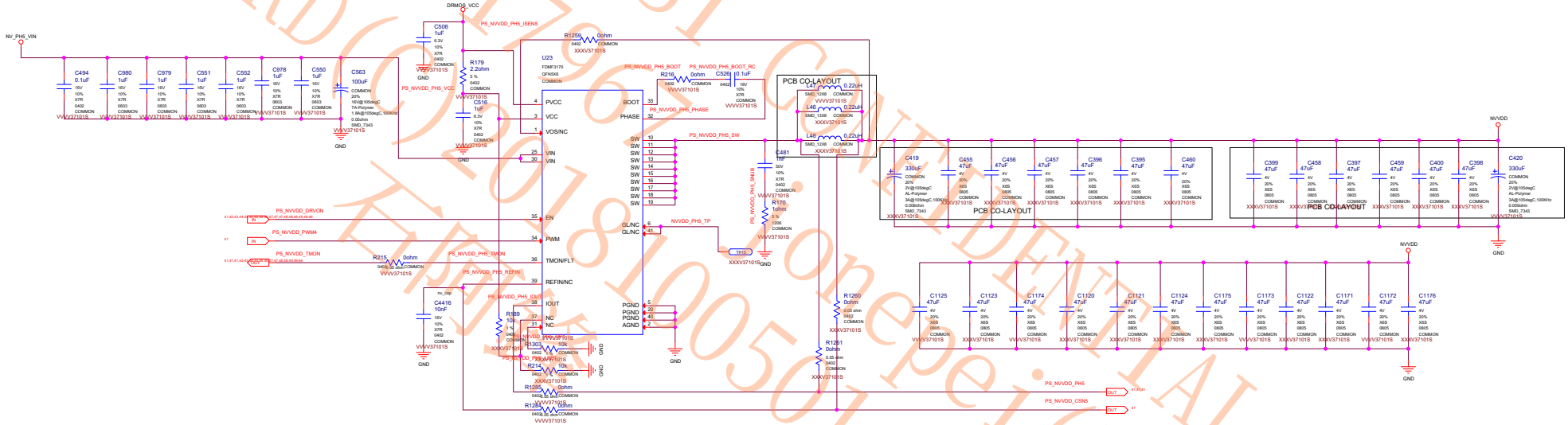
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	44 OF 66
BOM REV	A	DATE	09-JUL-2018

0001967 NVIDIA CONFIDENTIAL Jonsen RD(C)2018 1030 0068 RMA 工程樣

PS: NVVDD Phase 5



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PAGE DETAIL	PS: NVVDD Phase 5

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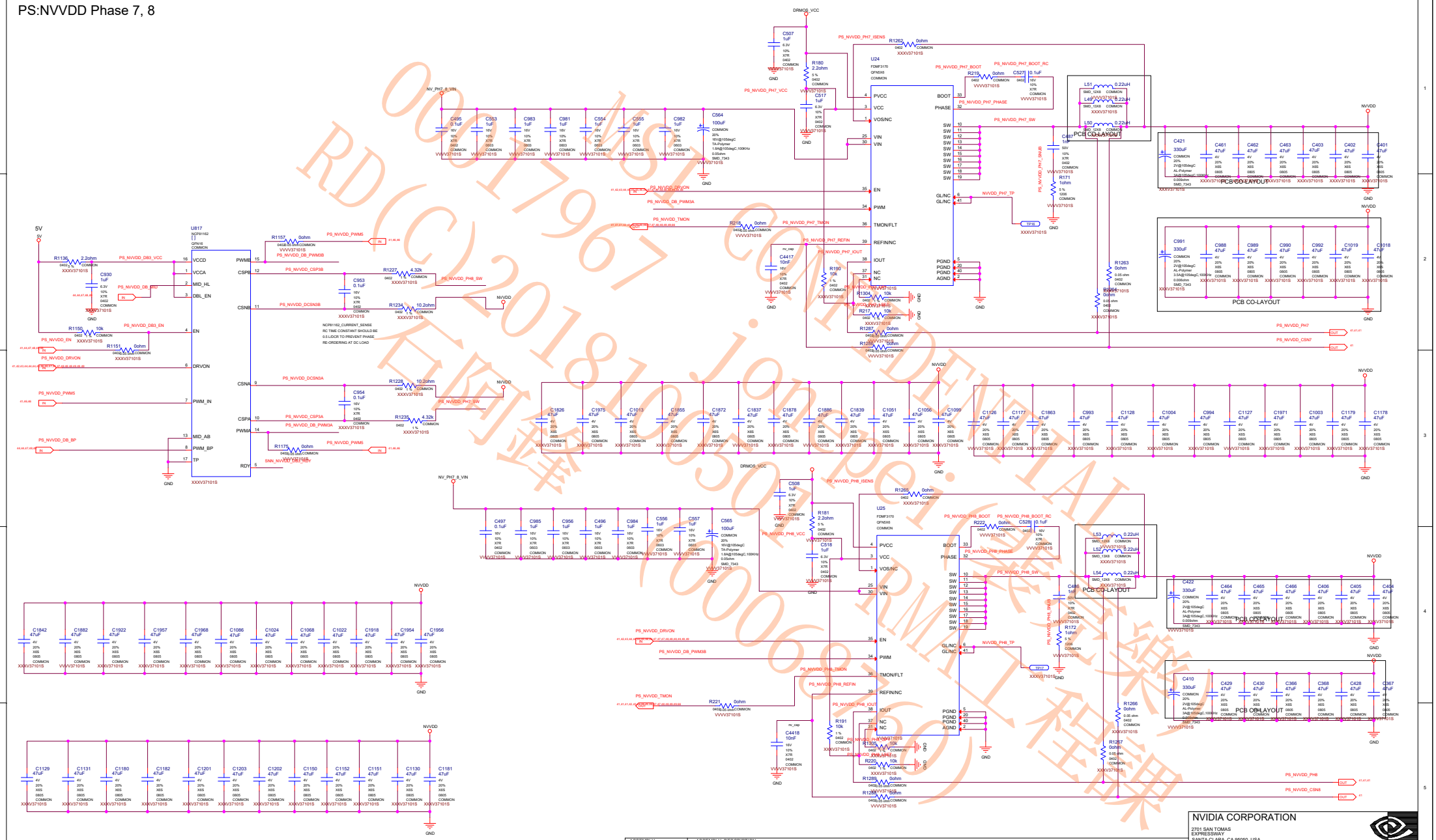
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	45 OF 66
BOM REV	A	DATE	09-JUL-2018

PS:NVVDD Phase 7, 8



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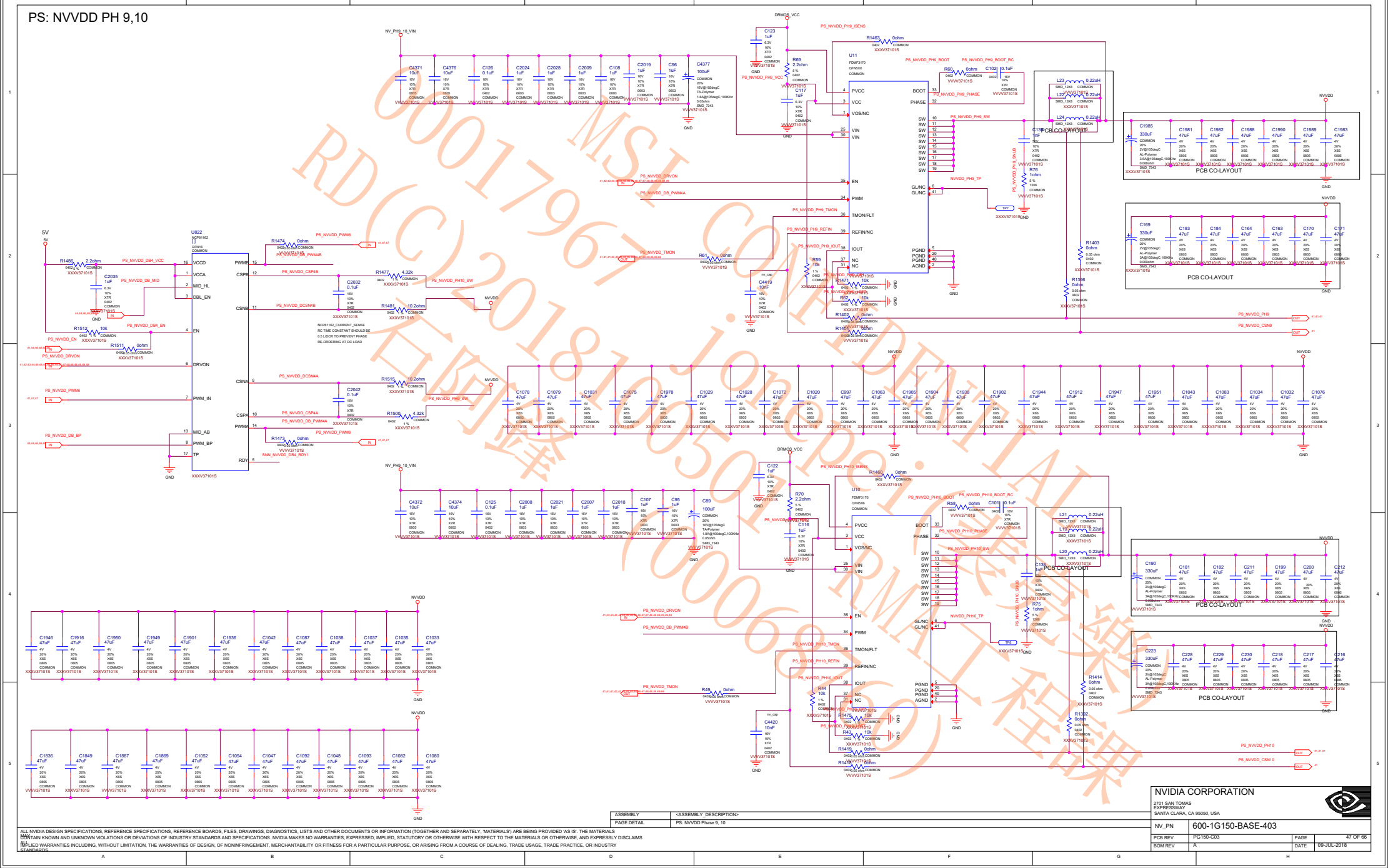
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	46 OF 66
BOM REV	A	DATE	09-JUL-2018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NV_PH9_10_VIN
DRMOS_VCC
U11
FDMF3170
DFN56
COMMON
PS_NVVDD_PH9_IBENS
PS_NVVDD_PH9_BOOT
PS_NVVDD_PH9_BOOT_RC
PS_NVVDD_PH9_VCC
PS_NVVDD_PH9_PHASE
PS_NVVDD_PH9_SW
PS_NVVDD_PH9_SNUB
NVVDD_PH9_TP
PS_NVVDD_DRVON
PS_NVVDD_DB_PWM4A
PS_NVVDD_PH9_TMON
PS_NVVDD_PH9_REFIN
PS_NVVDD_PH9_IOUT
PS_NVVDD_TMON
PS_NVVDD_PWM1
PS_NVVDD_REFS
PS_NVVDD_PH9
PS_NVVDD_CSN9
PCB CO-LAYOUT
5V
U822
NCP81162
QFN16
PS_NVVDD_DB4_VCC
PS_NVVDD_DB_MID
PS_NVVDD_DB4_EN
PS_NVVDD_EN
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PS_NVVDD_PH10_SW
PS_NVVDD_DCSN4A
PS_NVVDD_CSP4A
PS_NVVDD_DB_PWM4A
PS_NVVDD_DB_BP
SNN_NVVDD_DB4_RDY1
NCP81162_CURRENT_SENSE
RC TIME CONSTANT SHOULD BE
0.5 LOCR TO PREVENT PHASE
RE-ORDERING AT DC LOAD
NV_PH9_10_VIN
DRMOS_VCC
U10
FDMF3170
DFN56
COMMON
PS_NVVDD_PH10_IBENS
PS_NVVDD_PH10_BOOT
PS_NVVDD_PH10_BOOT_RC
PS_NVVDD_PH10_PHASE
PS_NVVDD_PH10_SW
PS_NVVDD_PH10_SNUB
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PS_NVVDD_DRVON
PS_NVVDD_DB_PWM4B
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PS_NVVDD_PH10_REFIN
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PS_NVVDD_PWM2
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PS_NVVDD_PH10
PS_NVVDD_CSN10
PCB CO-LAYOUT
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NV_PN 600-1G150-BASE-403
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BOM REV A
PAGE 47 OF 66
DATE 09-JUL-2018
ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL PS: NVVDD Phase 9, 10
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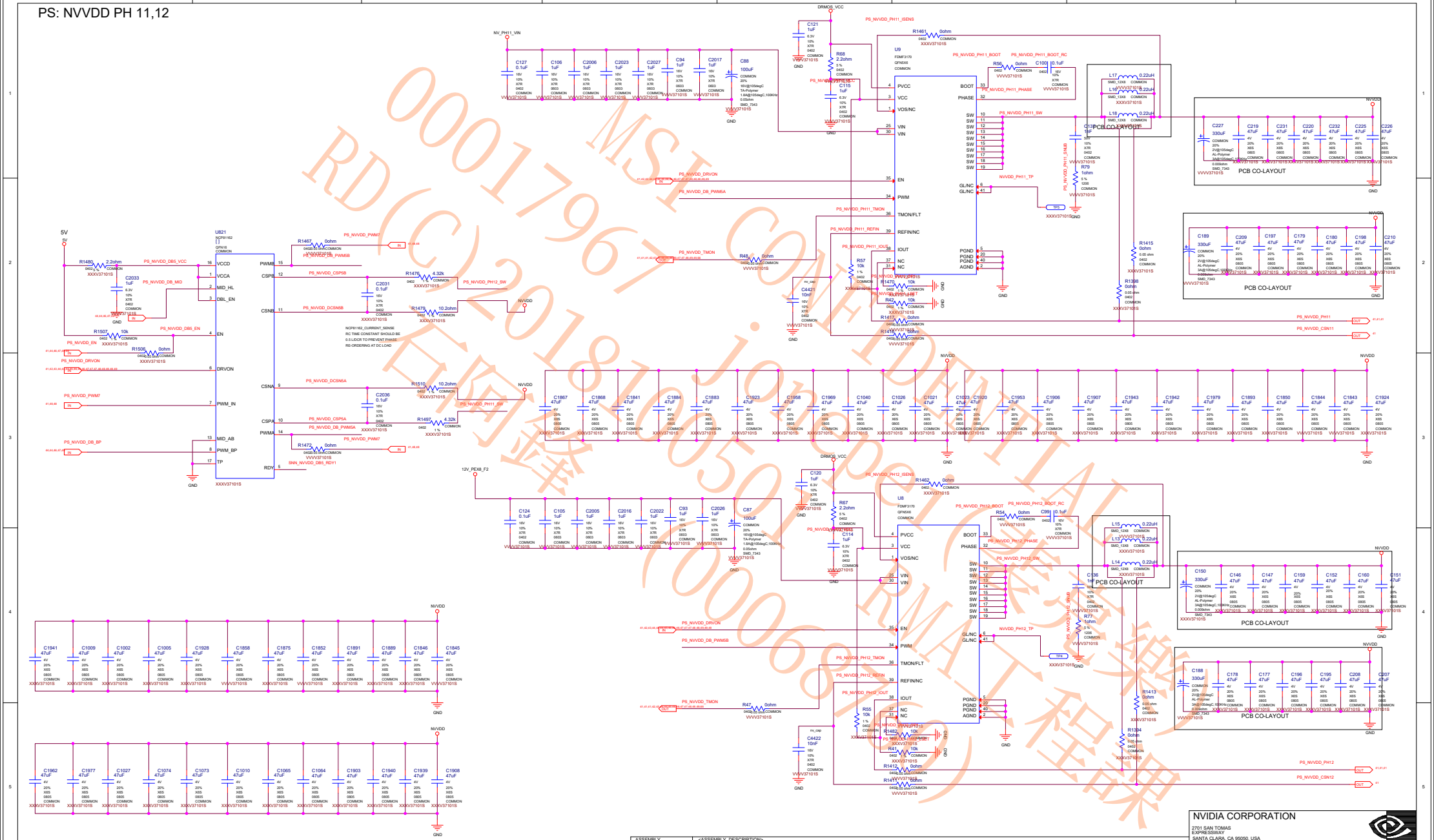
PS: NVVDD PH 11,12



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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	48 OF 66
BOM REV	A	DATE	09-JUL-2018

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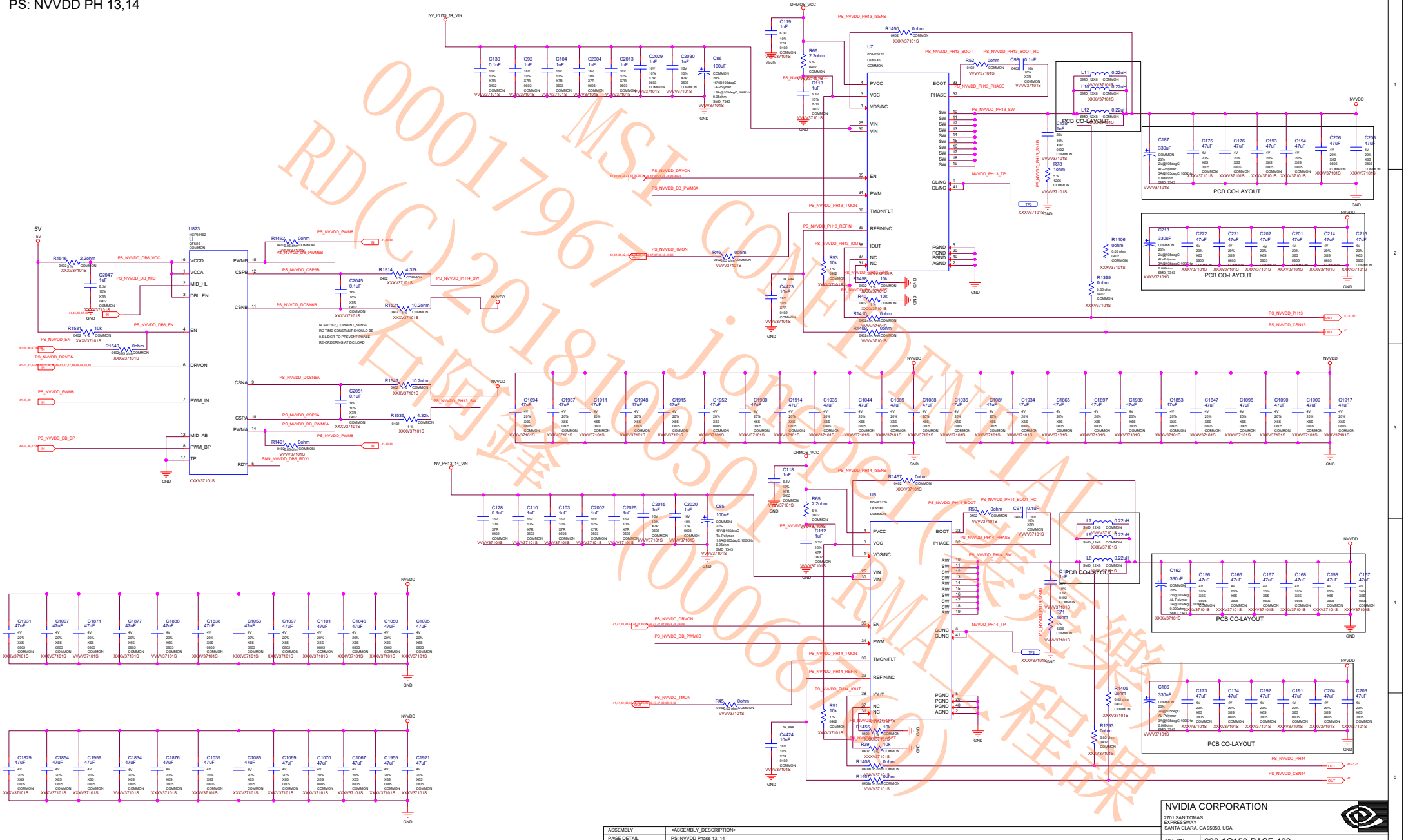
PS: NVVDD PH 13,14



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PCB REV	PG150-C03	PAGE	49 OF 66
BOM REV	A	DATE	09-JUL-2018

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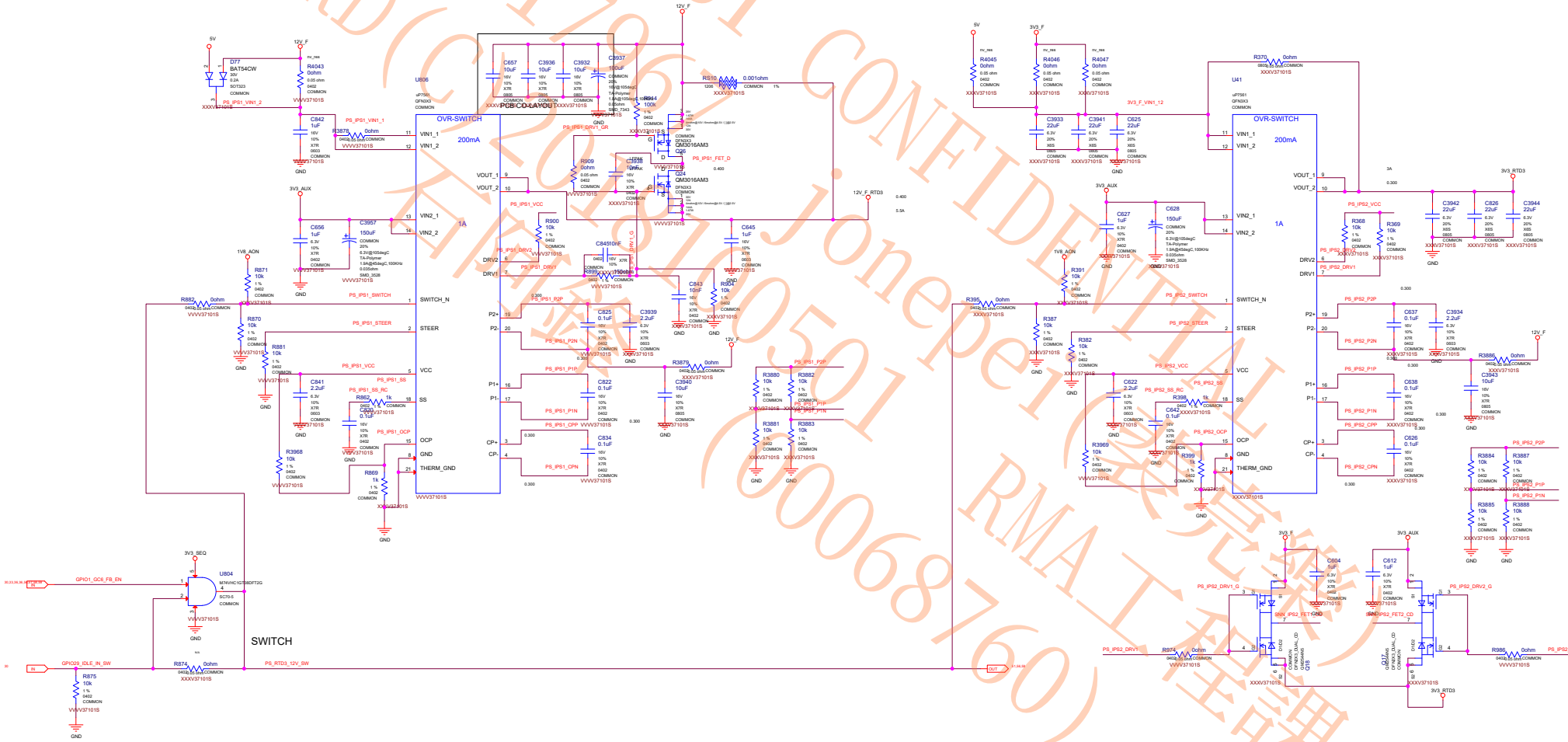
PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: INPUT SWITCH_RTD3

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	50 OF 66
BOM REV	A	DATE	09-JUL-2018

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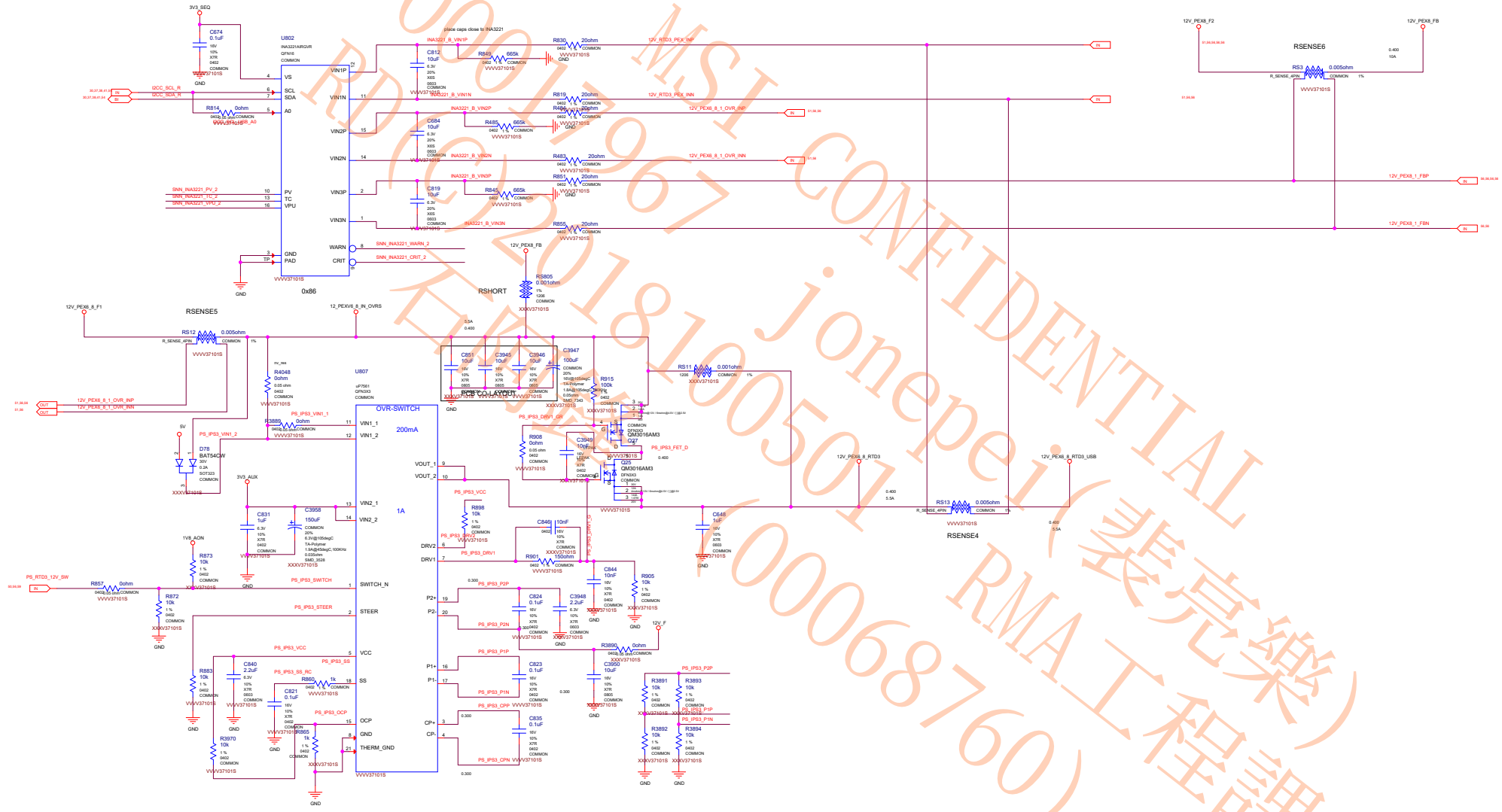

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: INPUT SWITCH_RTD3 USB

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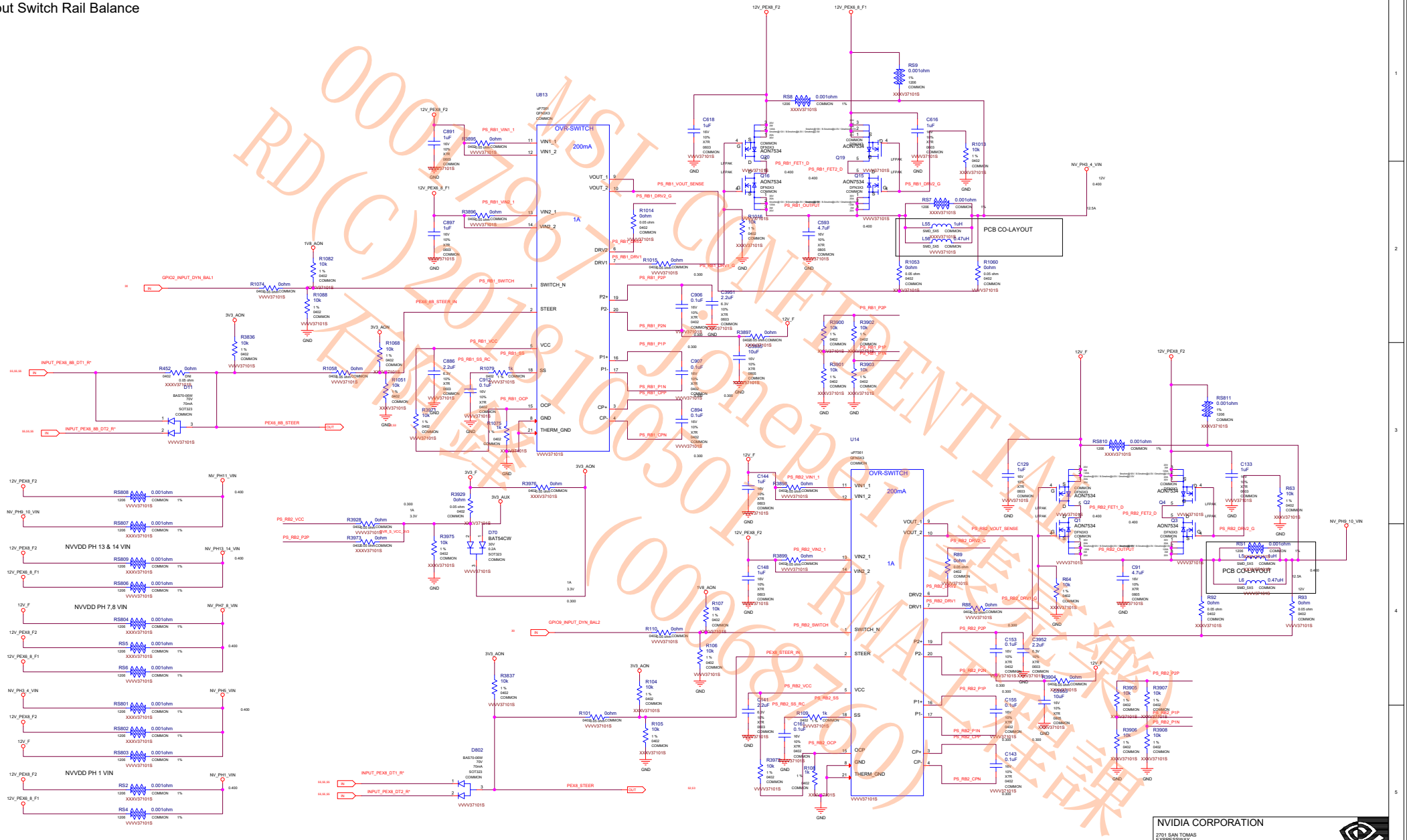
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	51 OF 66
BOM REV	A	DATE	09-JUL-2018

PS: Input Switch Rail Balance



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: INPUT SWITCH RAIL BALANCE

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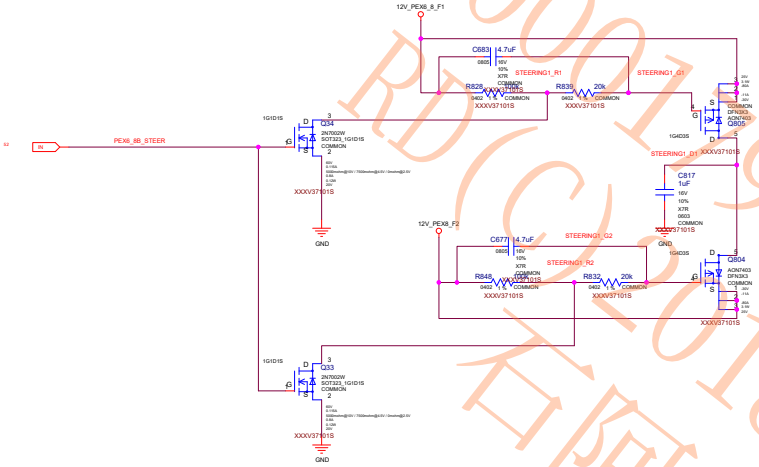
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	52 OF 66
BOM REV	A	DATE	09-JUL-2018

12V CURRENT STEERING (UNDER POWER BOOT):

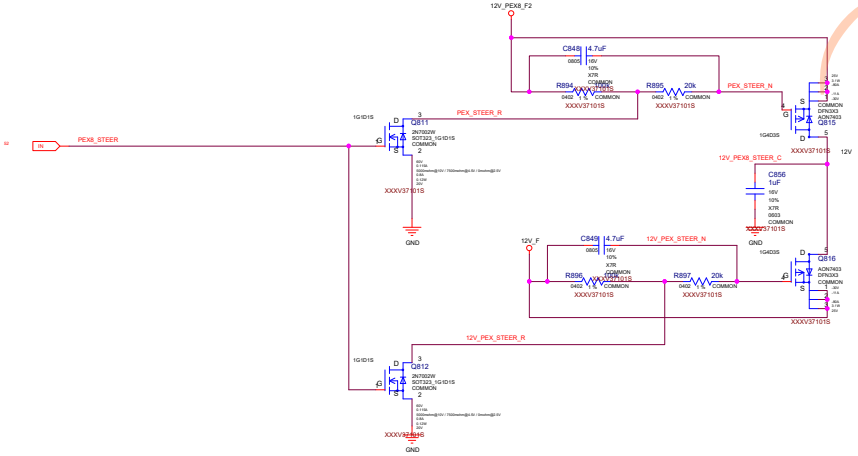
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: DISCRETE STEERING

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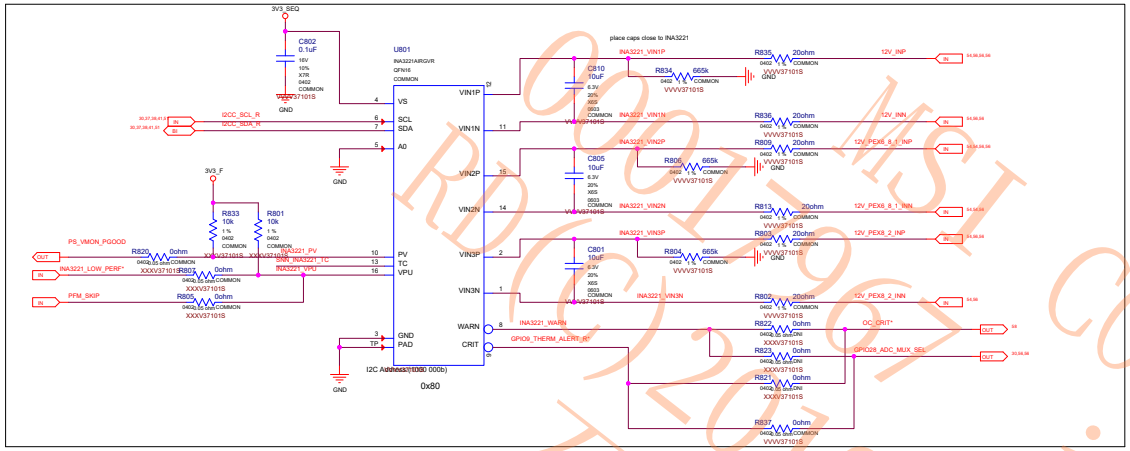
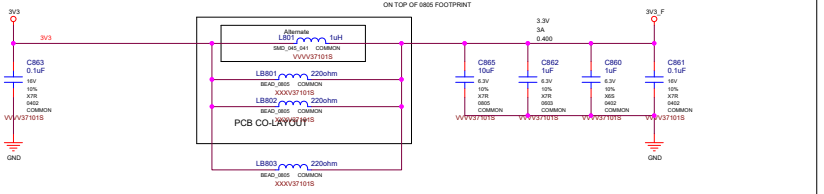
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	53 OF 66
BOM REV	A	DATE	09-JUL-2018

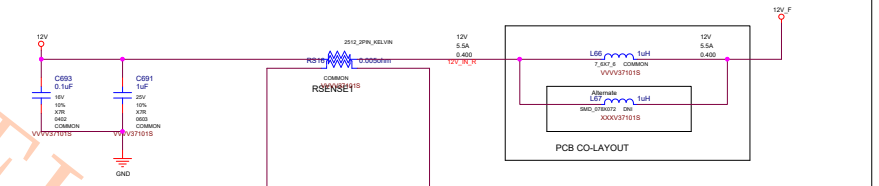
PS: Inputs, Filtering, and Monitoring



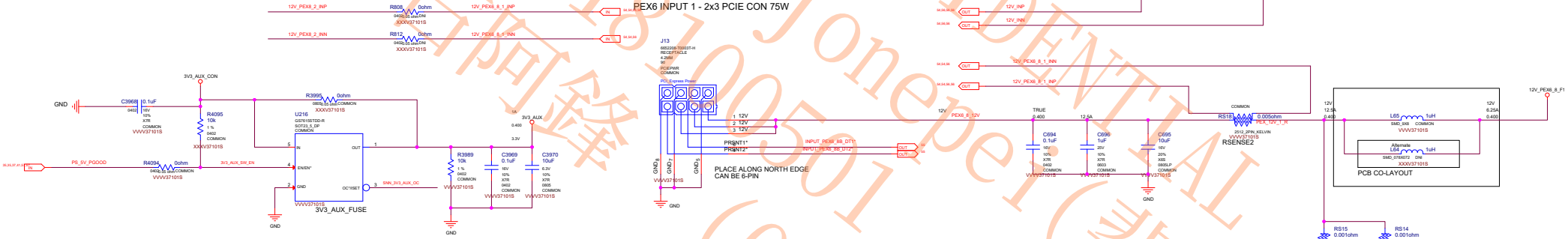
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



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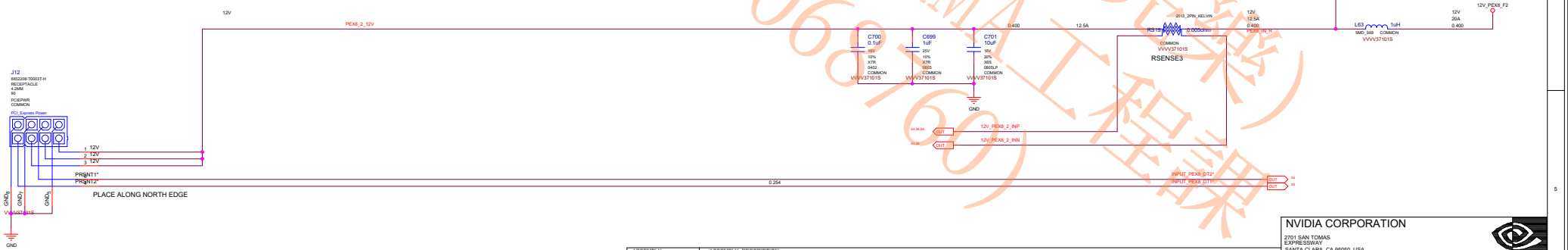

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Input, filtering, and Monitoring

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	54 OF 66
BOM REV	A	DATE	09-JUL-2018

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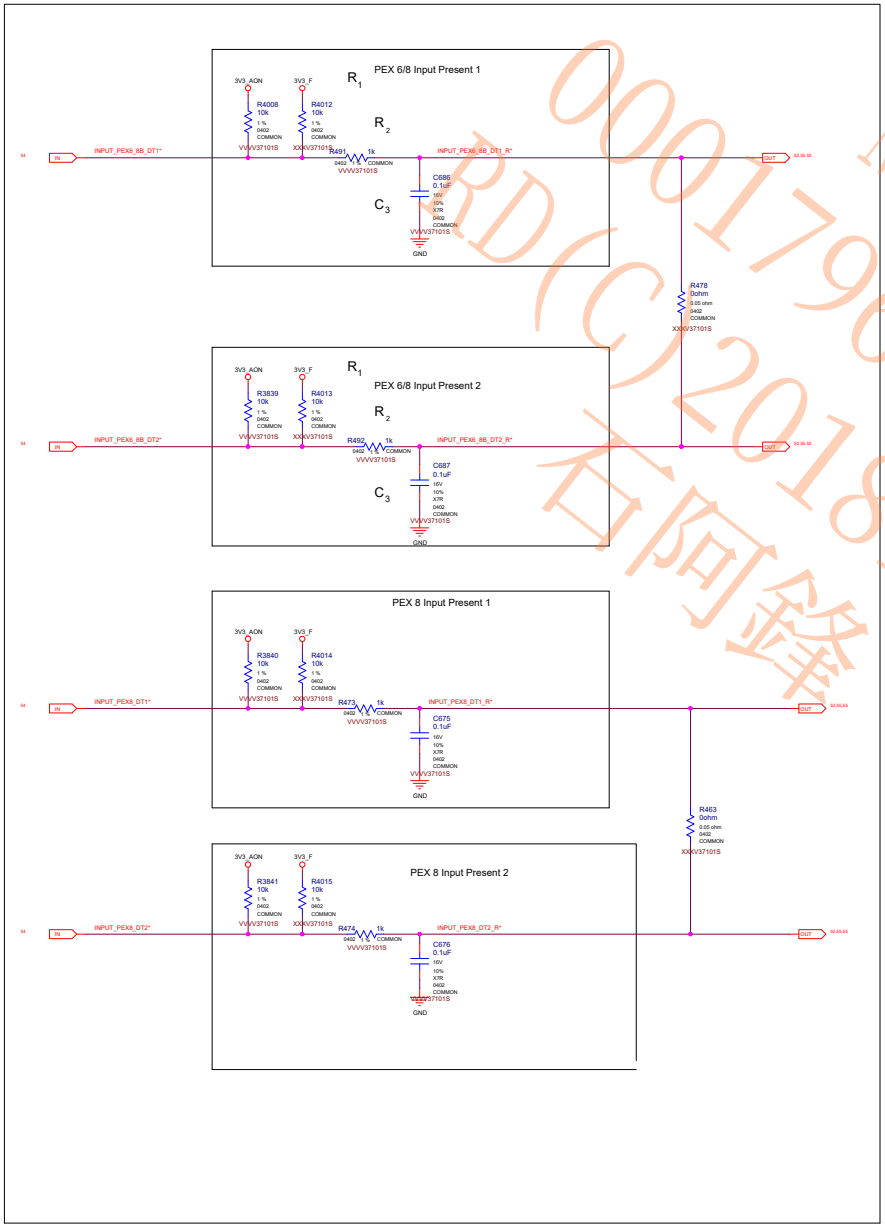
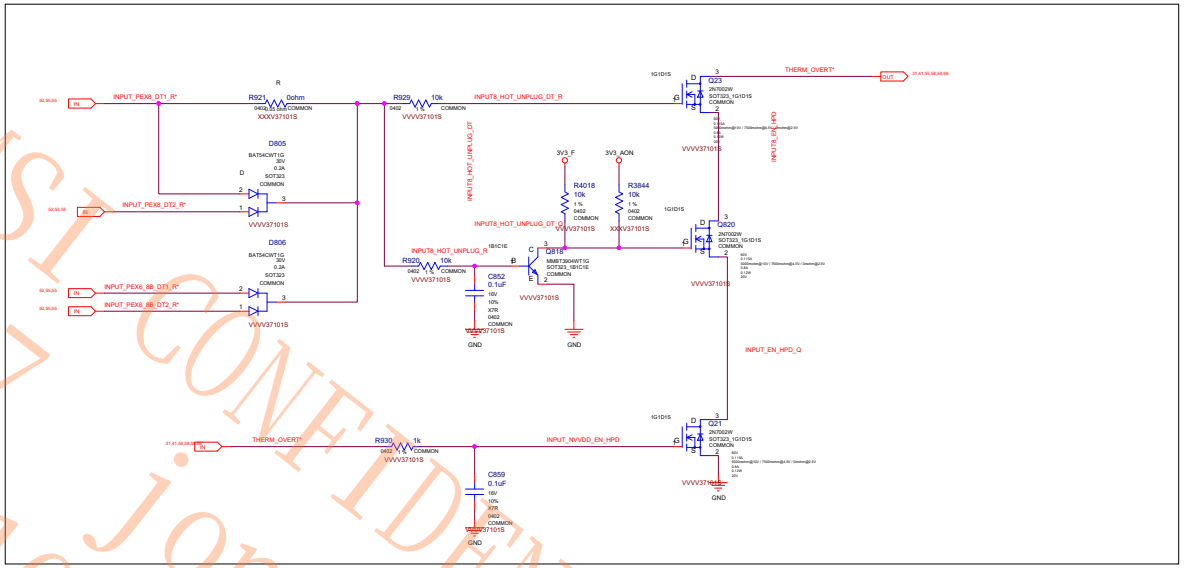
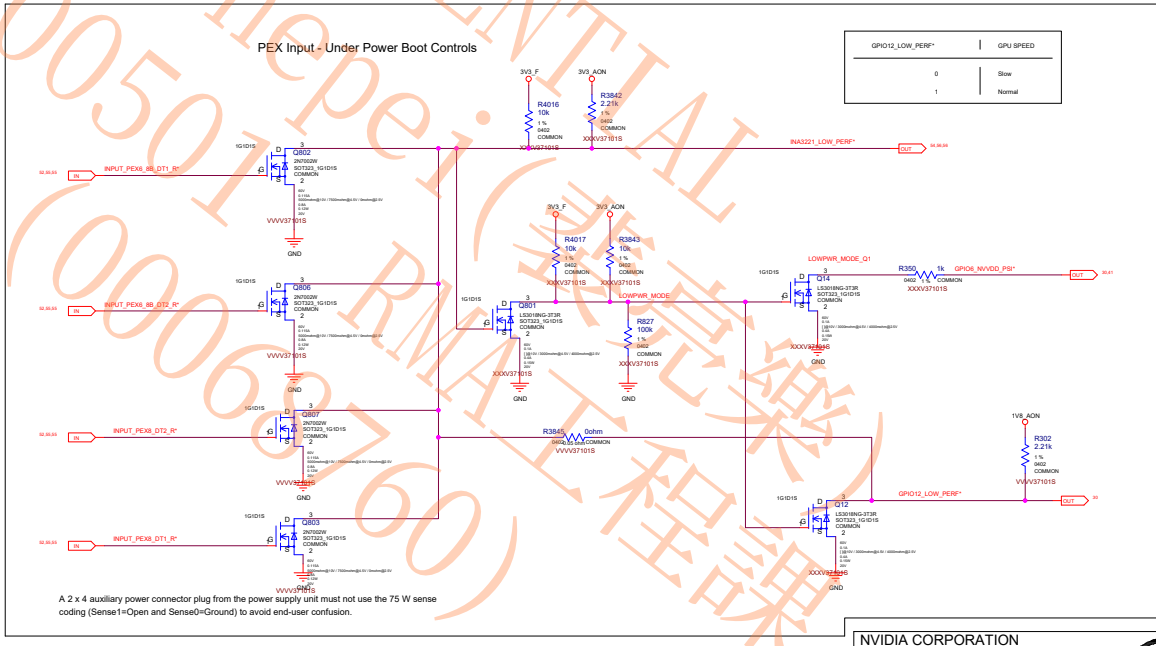
RD(C)2018.00501 Jonepei(姜完锋)
(0006876) RMA工程课

PS: 12V Current Steering & Hot Unplug Detect







A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Current Sterring, Hot Unplug

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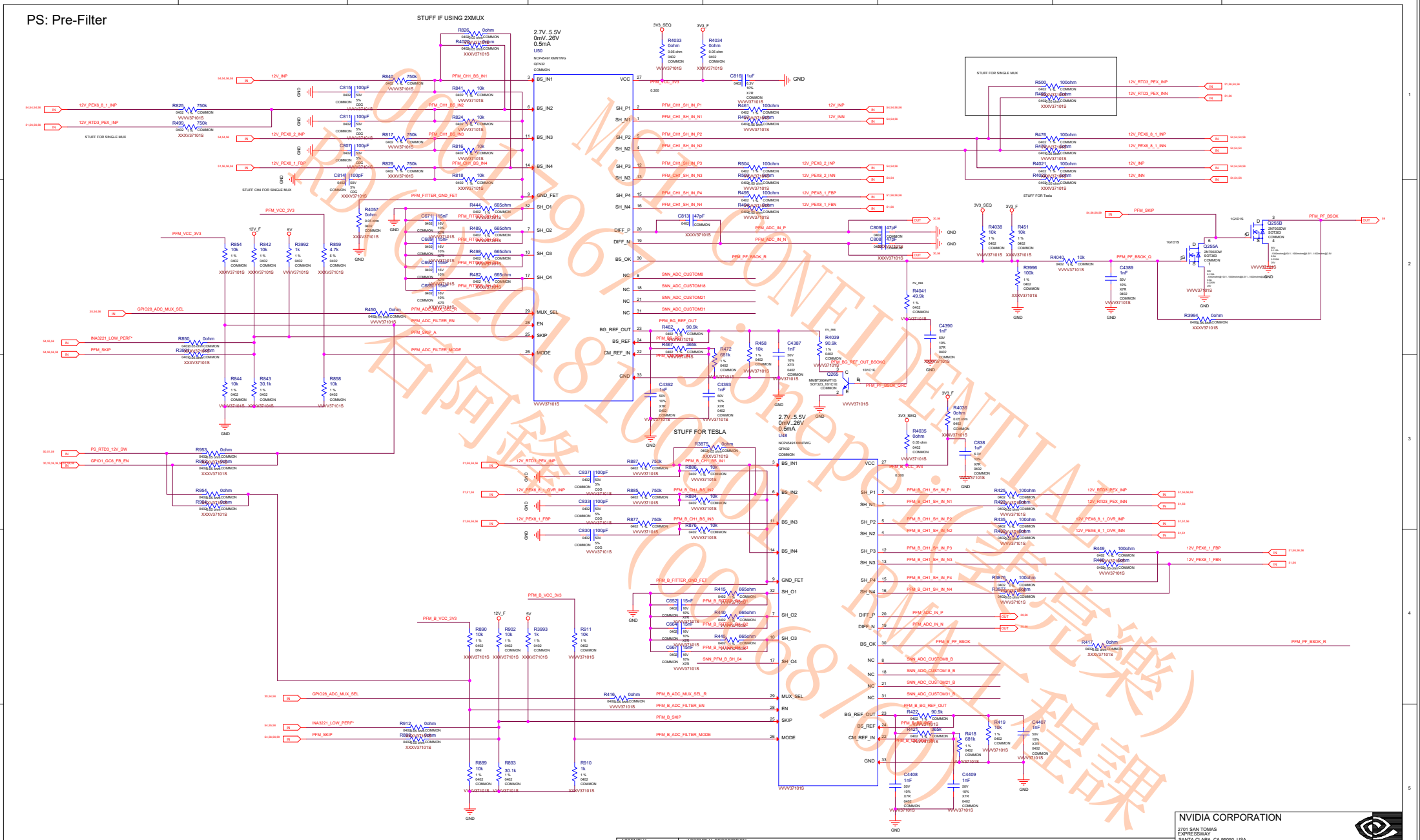
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	55 OF 66
BOM REV	A	DATE	09-JUL-2018

0001796 7 Jonepei(00066760) MSI CONFIDENTIAL RD(C)20181005 石阿锋 RMA工程课

PS: Pre-Filter



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: Prefilter

NVIDIA CORPORATION
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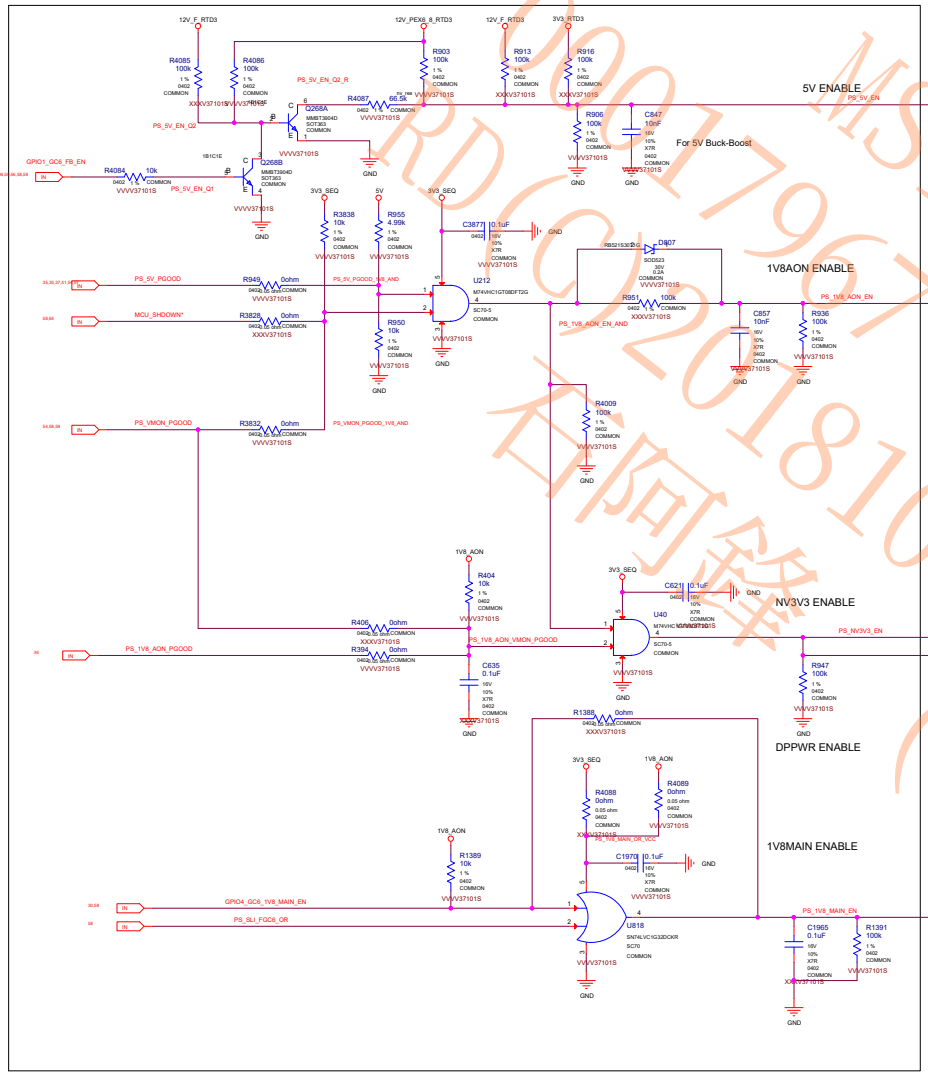
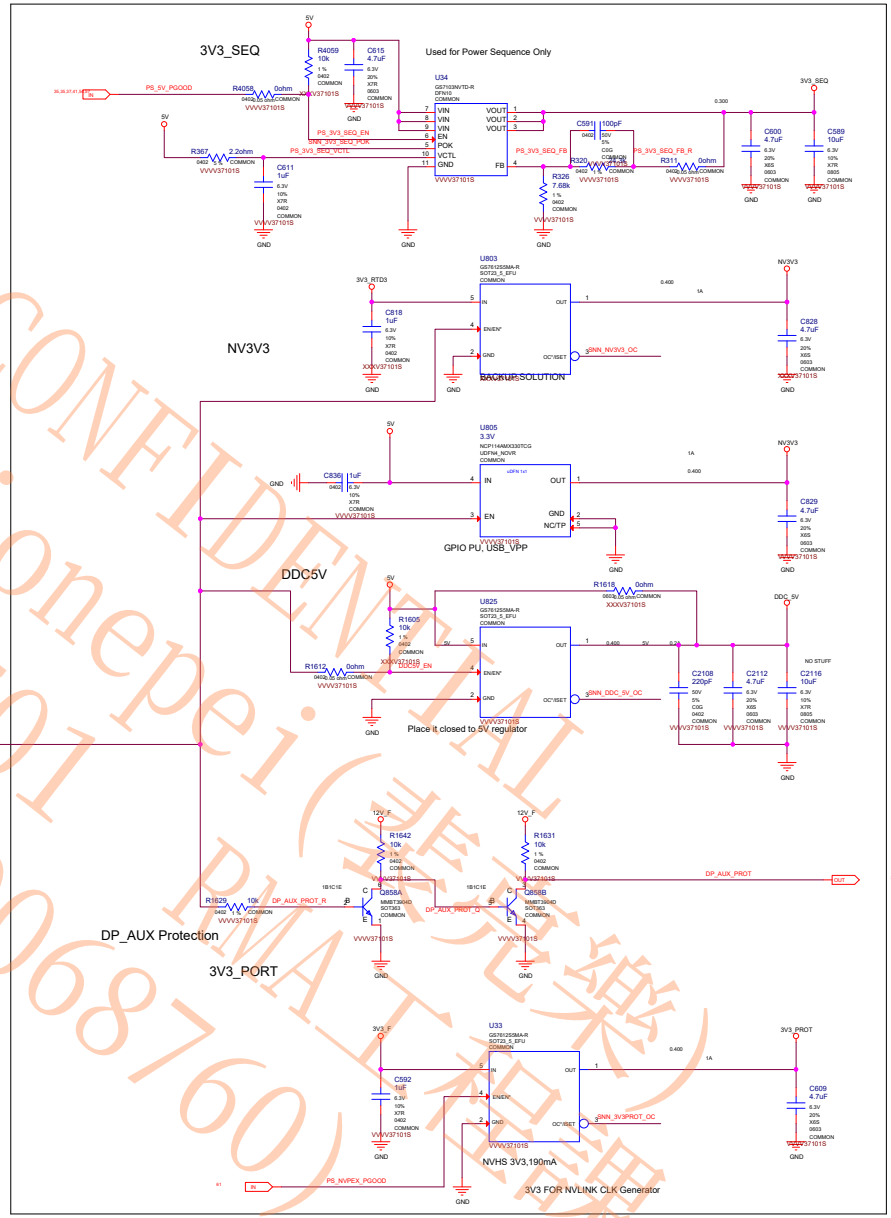
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	56 OF 66
BOM REV	A	DATE	09-JUL-2018

SEQUENCE:5V,1V8,NV3V3 ENABLE





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0017967 jonepei(裴完燃)
RD(C)2018100501 (00068760)
石阿饺 PMA工程师

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Sequence: 5V, 1V8, NV3V3 EN

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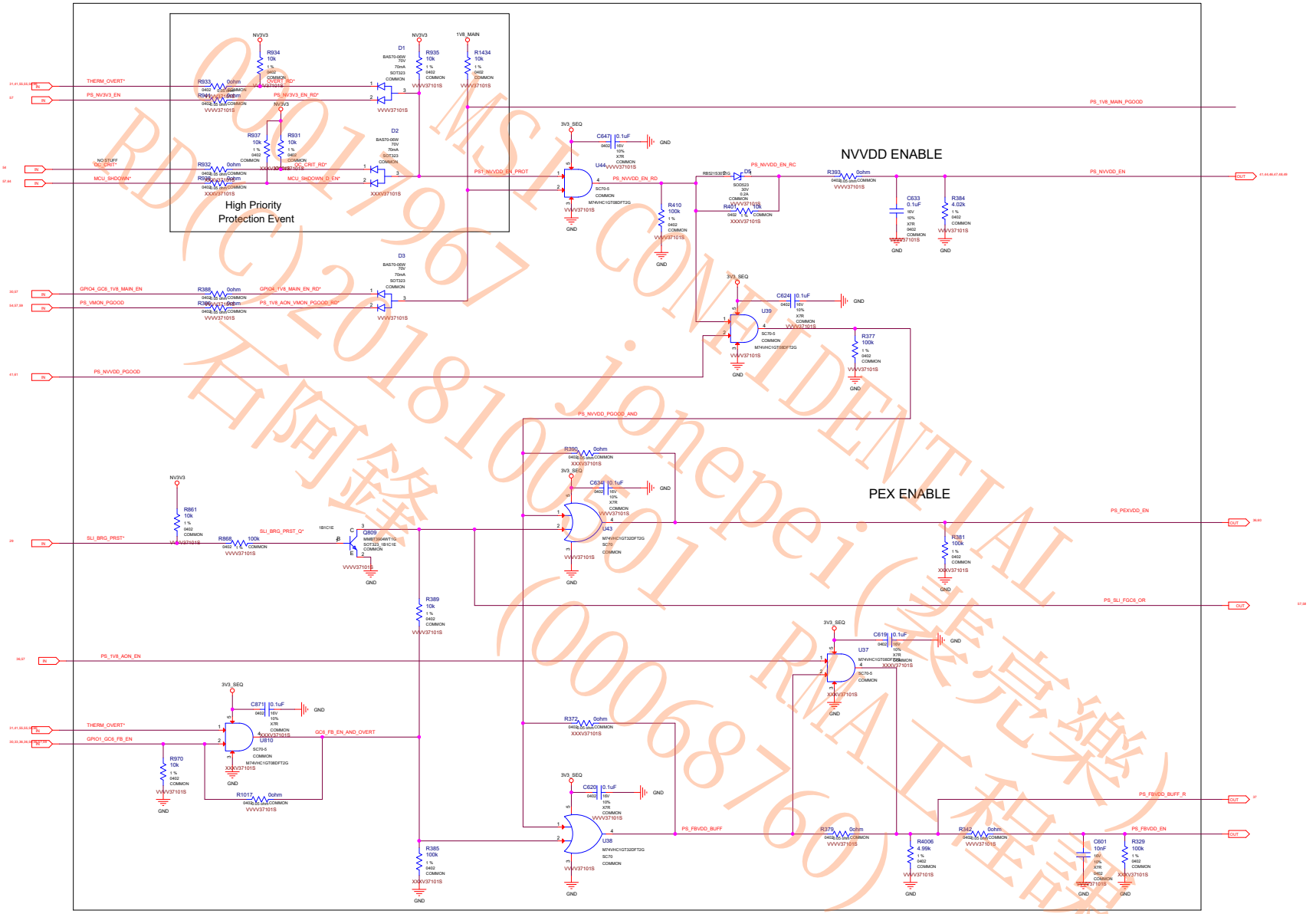
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	57 OF 66
BOM REV	A	DATE	09-JUL-2018

SEQUENCE:NV,PEX,FB ENABLE



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Sequence: NV, PEX, FB EN

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	58 OF 66
BOM REV	A	DATE	09-JUL-2018

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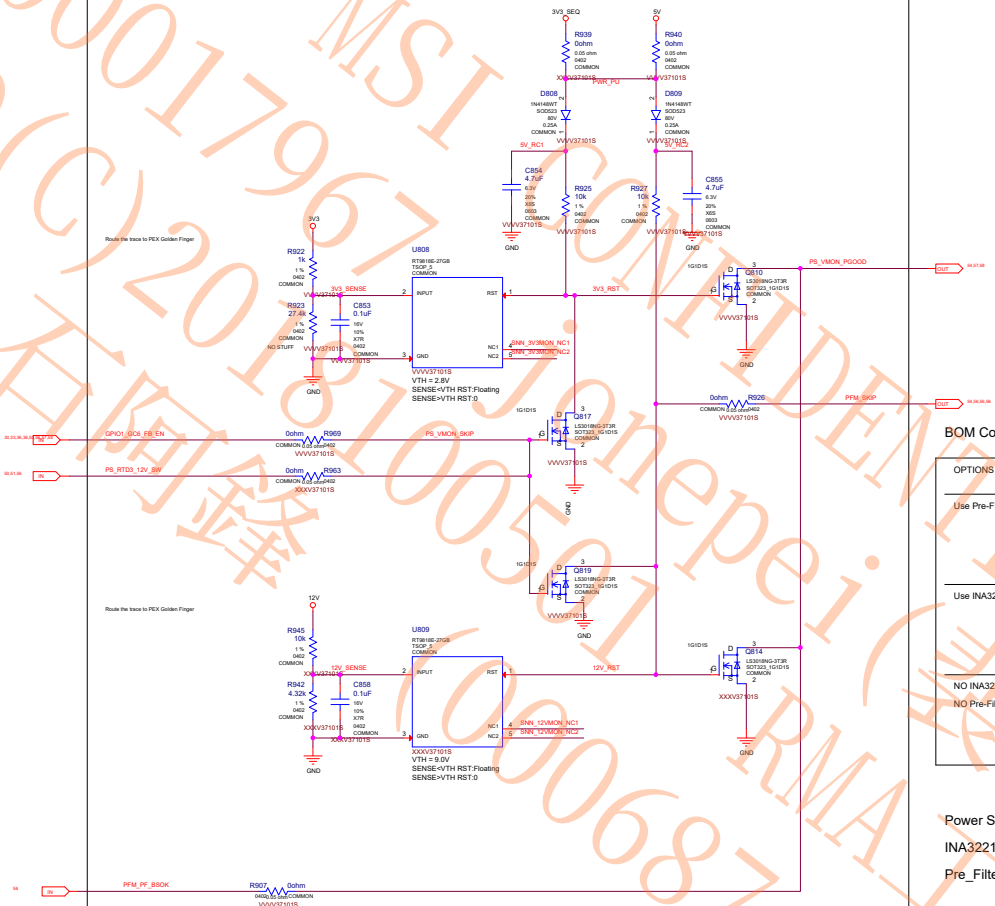
(00068760) RMA工程課

SEQUENCE:PCIE Voltage Monitor

PCIE Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX

and All Input 12Vs

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Sequence: PCIE Voltage Monitor

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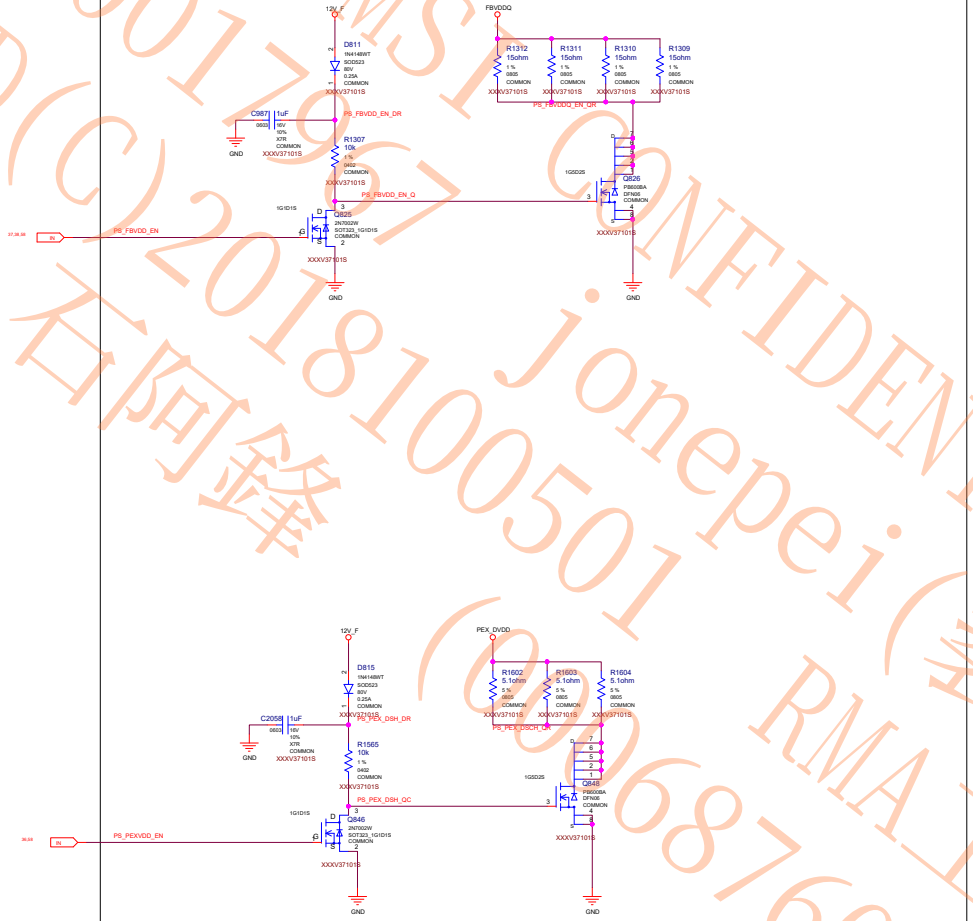
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	59 OF 66
BOM REV	A	DATE	09-JUL-2018

SEQUENCE:Discharge



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jonepei(裴完樂)
0001786760
RD(C)20181005O1
RMA工程課

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Sequence: Discharge

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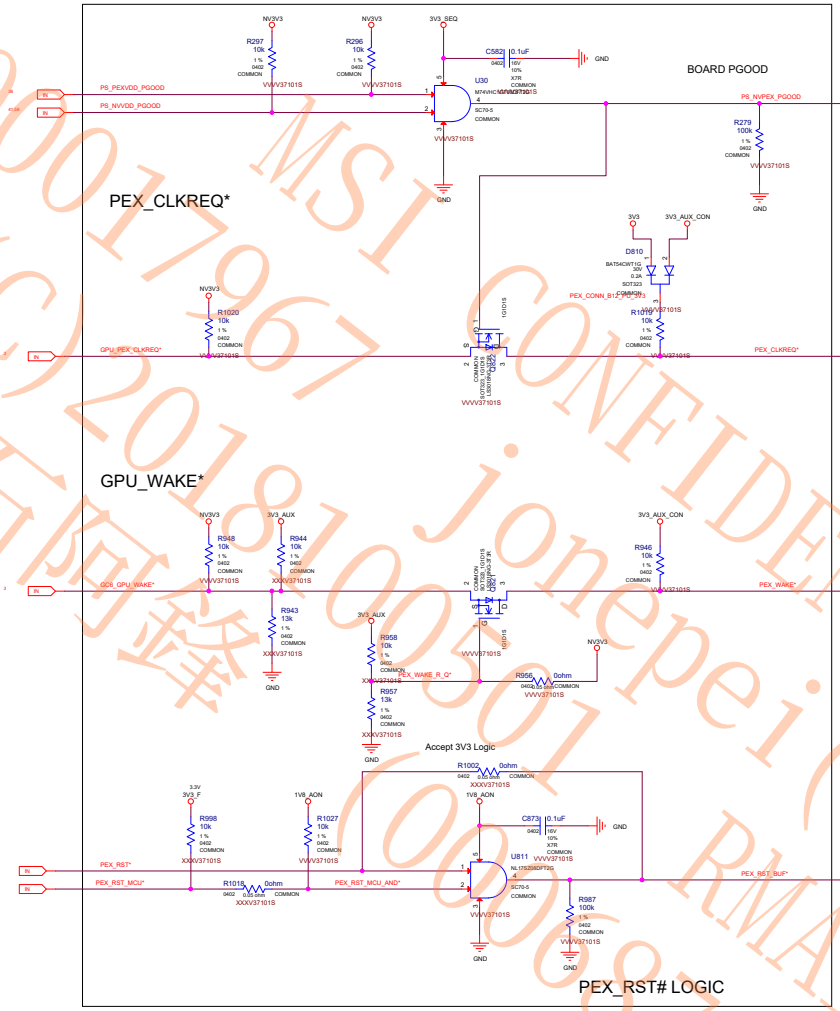
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	60 OF 66
BOM REV	A	DATE	09-JUL-2018

SEQUENCE:MISC



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0001967 jonepei(裴完樂)
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PAGE DETAIL	Sequence: MISC

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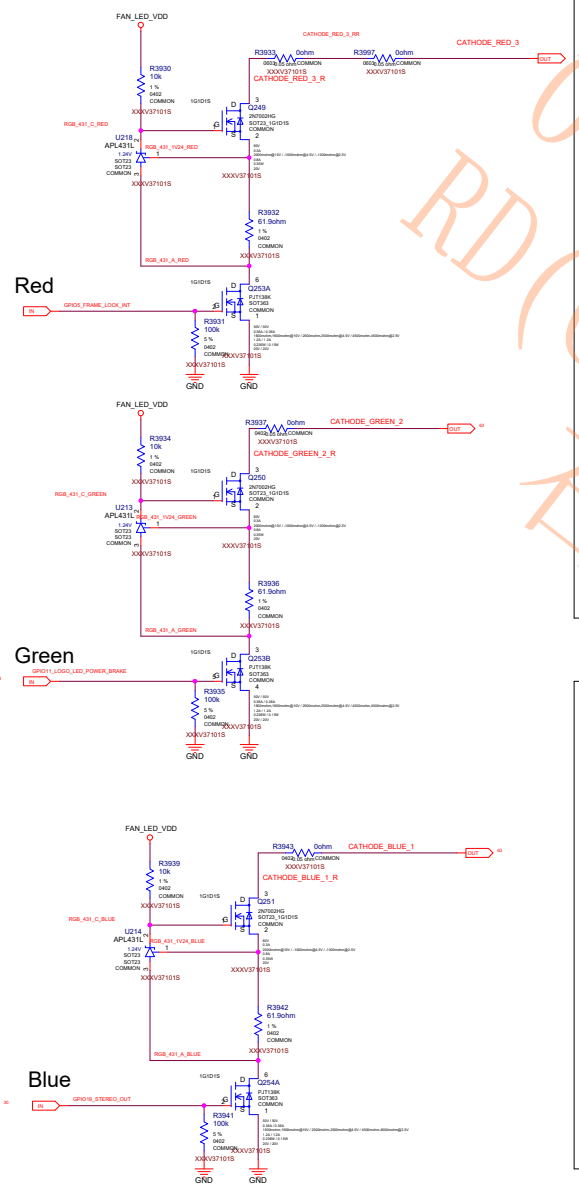
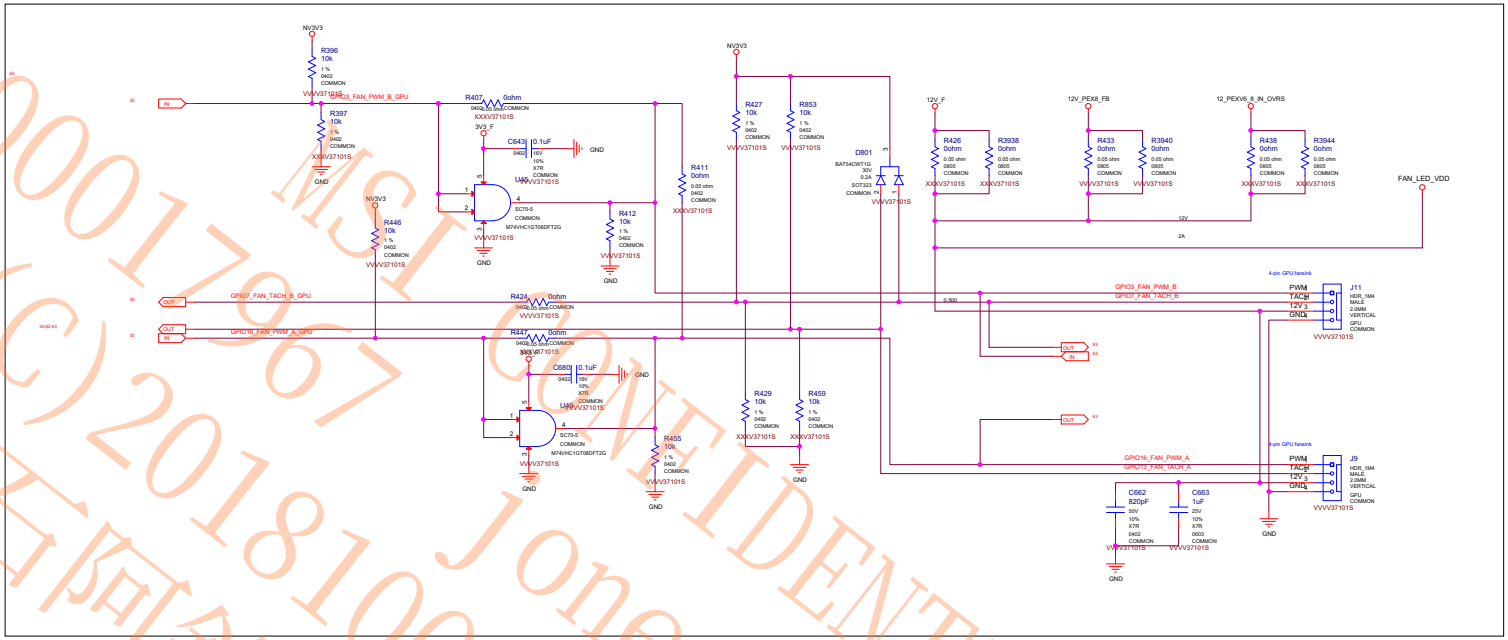
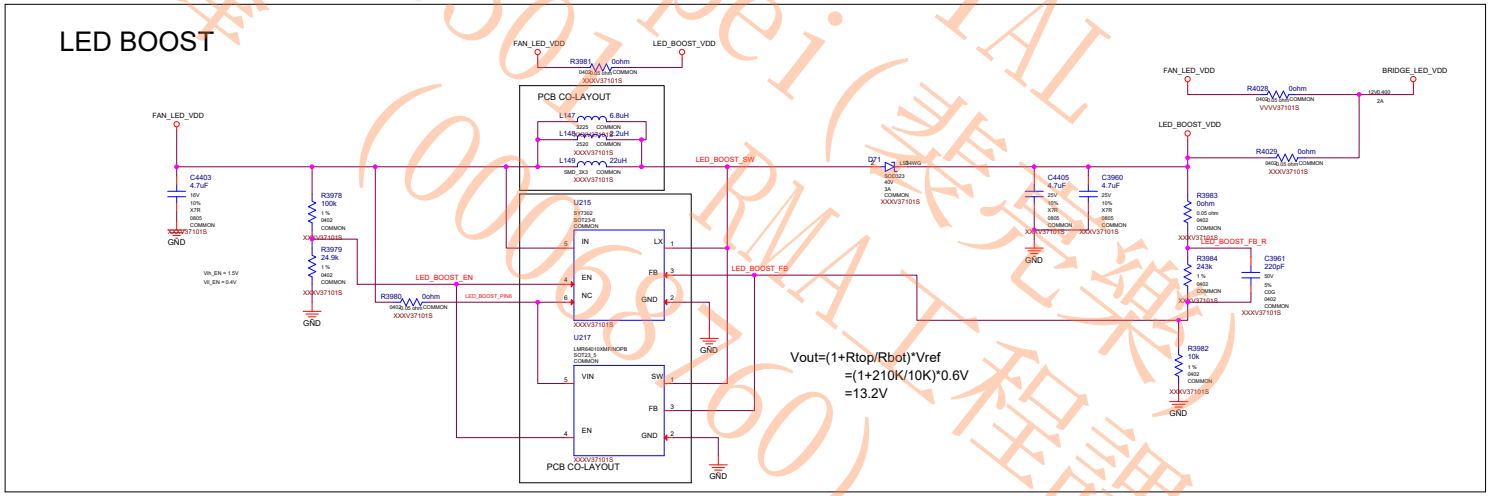
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	61 OF 66
BOM REV	A	DATE	09-JUL-2018

MISC: FAN & LED1







0001796 7 NVIDIA CONFIDENTIAL Jonepei(精完集)
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RMA(00668760)
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: FAN & LED1

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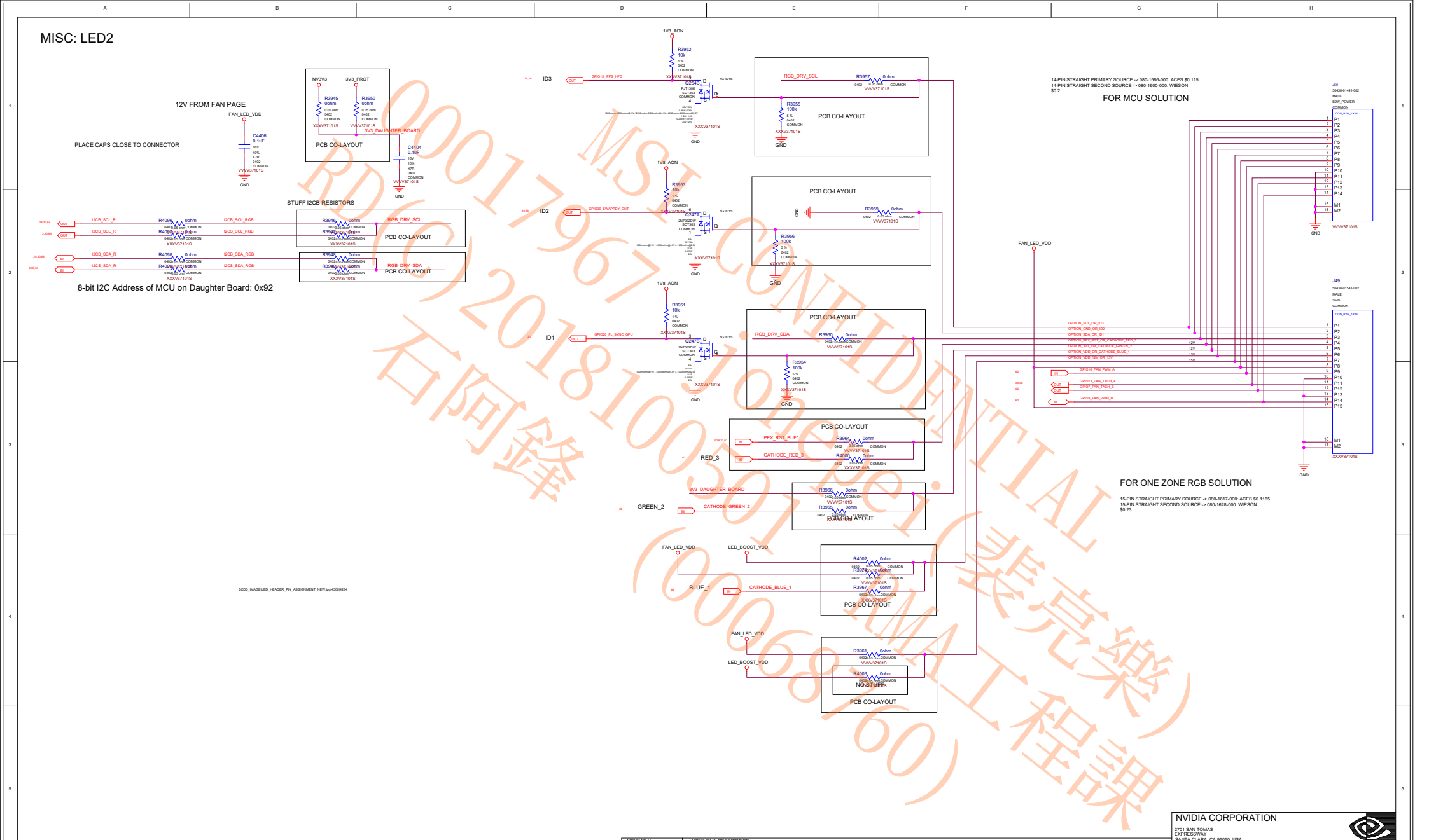
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	62 OF 66
BOM REV	A	DATE	09-JUL-2018

MISC: LED2



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC: LED 2

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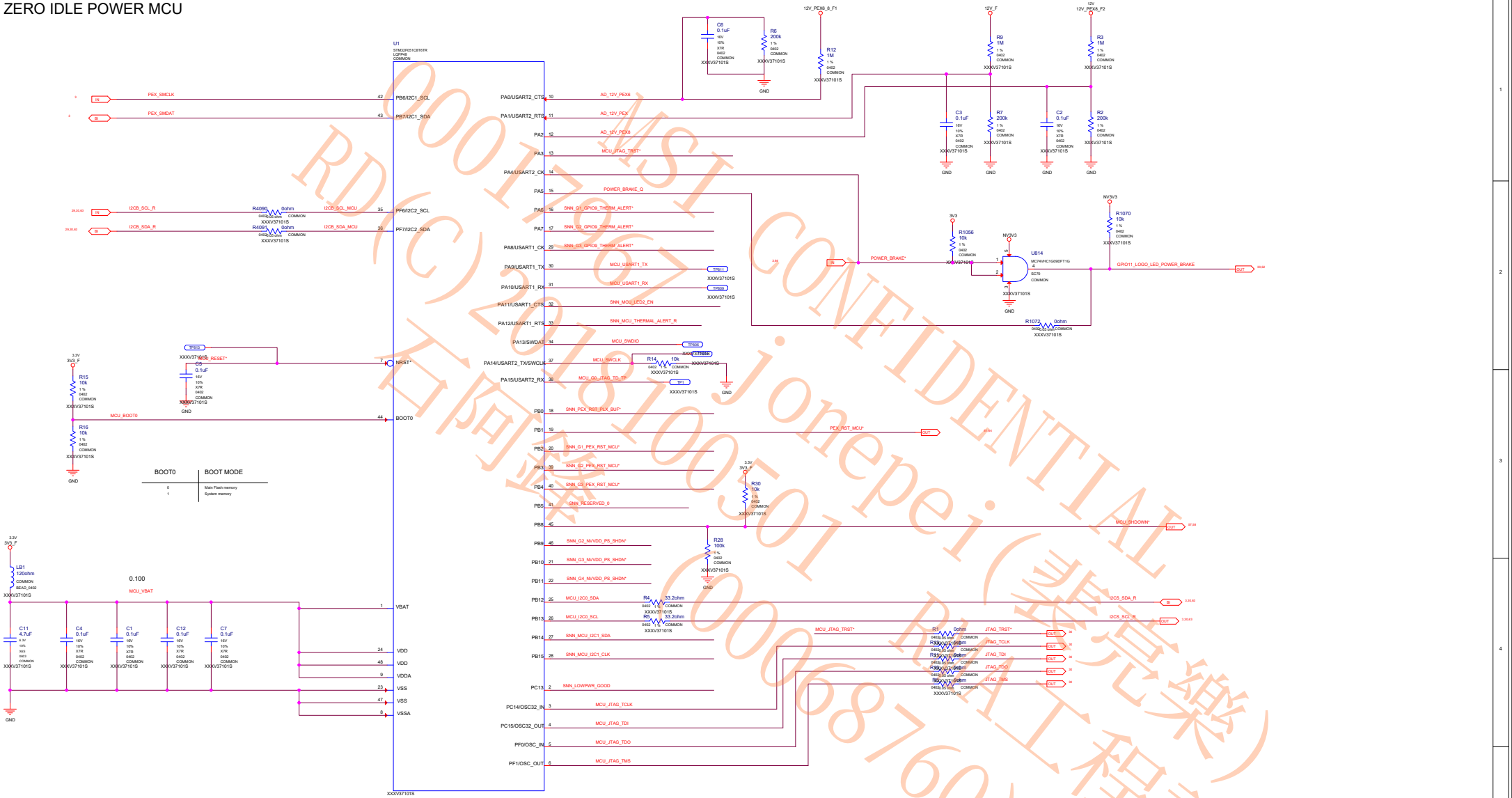
NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	63 OF 66
BOM REV	A	DATE	09-JUL-2018

0017967 MSI CONFIDENTIAL 1018Rev1.0(樣完樂) RD6 2018100301 (000688760) 石阿鋒 RMA工程課

ZERO IDLE POWER MCU



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PAGE DETAIL	MCU ZERO POWER IDLE

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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	64 OF 66
BOM REV	A	DATE	09-JUL-2018

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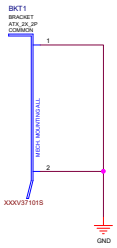
RD(C)2018100501 Jonepei(裴完樂)
000068760 PVT工程課

Mechanical: Bracket/Thermal Solution

Brackets:

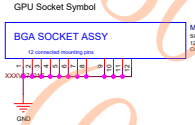


Bracket Screw

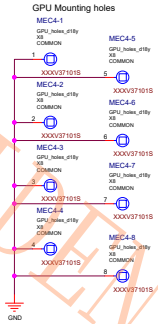
Back Cover

GPU Stiffner back side

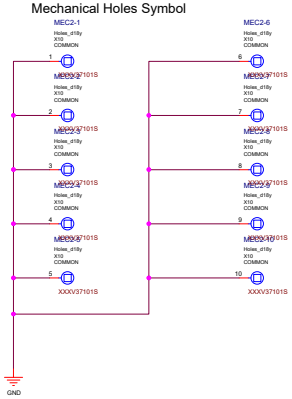
GPU Socket Symbol



GPU Mounting holes



Mechanical Holes Symbol



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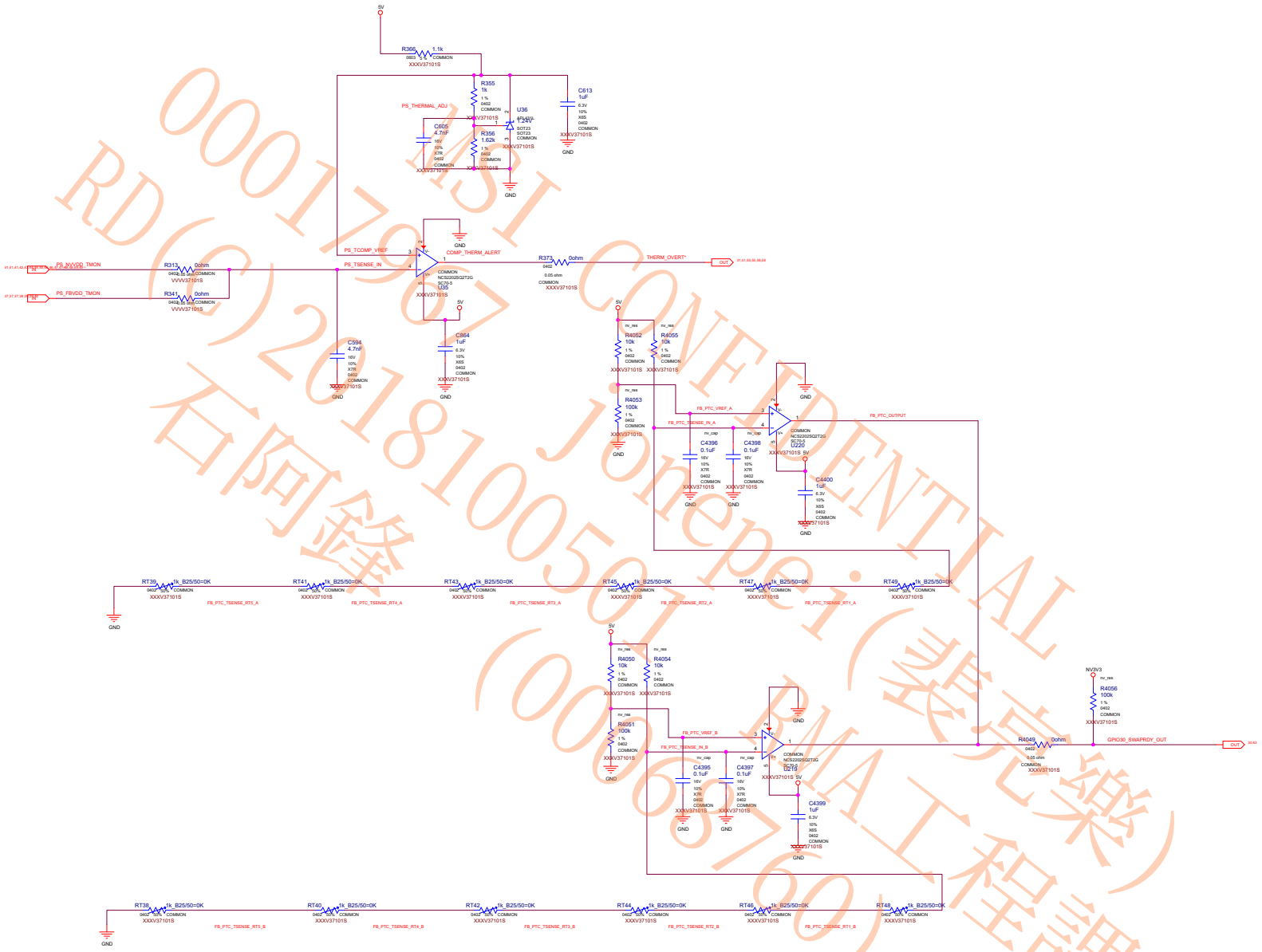
PCB REV	PG150-C03	PAGE	65 OF 66
BOM REV	A	DATE	09-JUL-2018

VR THERMAL PROTECTION



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NV_PN	600-1G150-BASE-403		
PCB REV	PG150-C03	PAGE	66 OF 66
BOM REV	A	DATE	09-JUL-2018