PG150-C03

384b GDDR6 x16
TALL DP + DP + DP + HDMI/DP + USB

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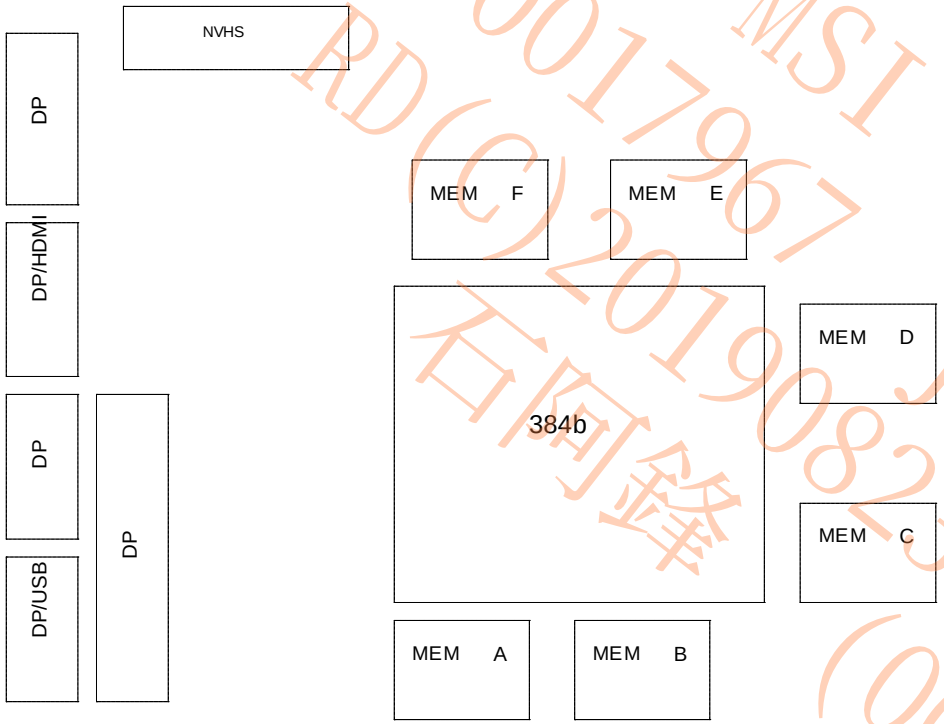
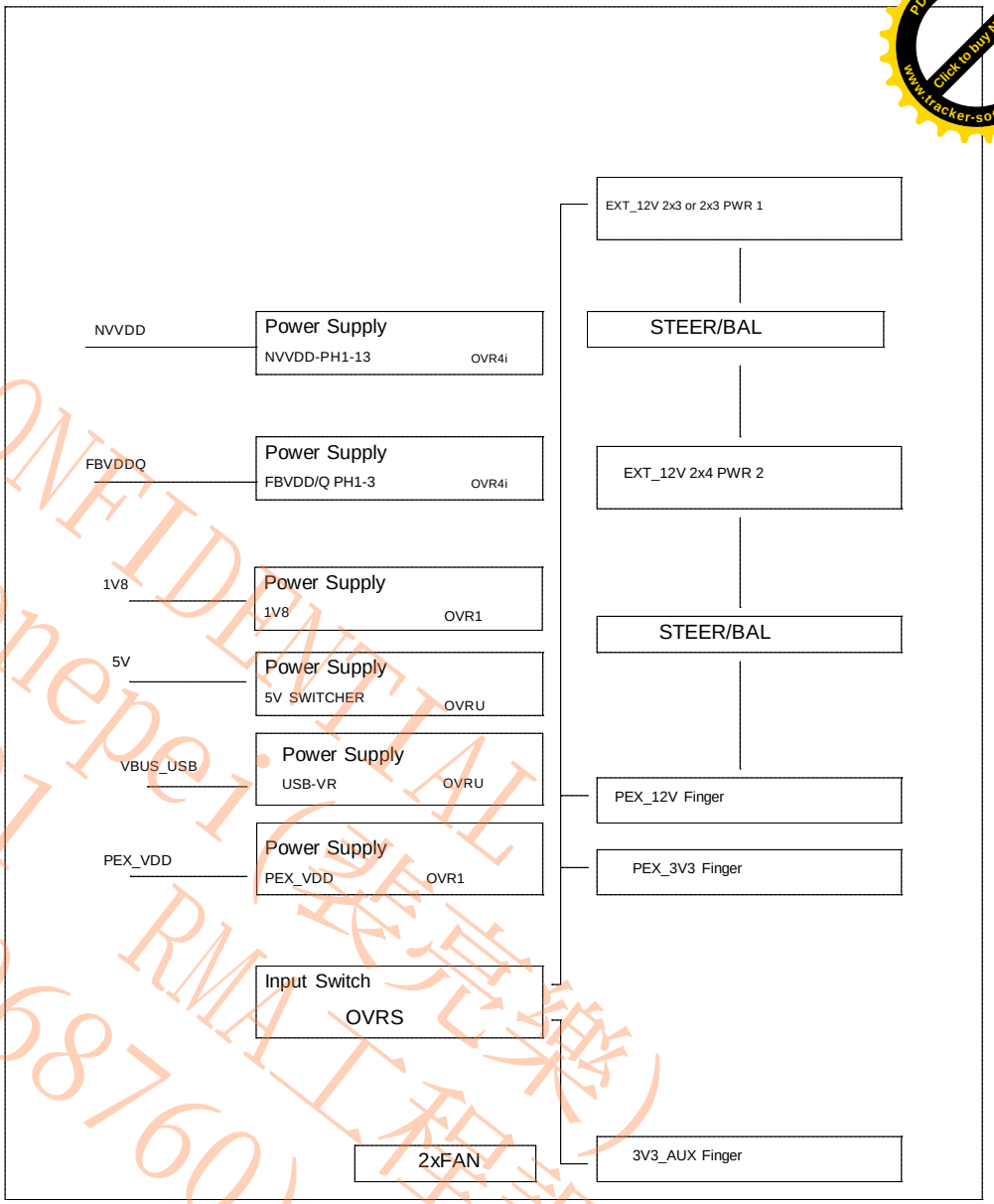
Block Diagram





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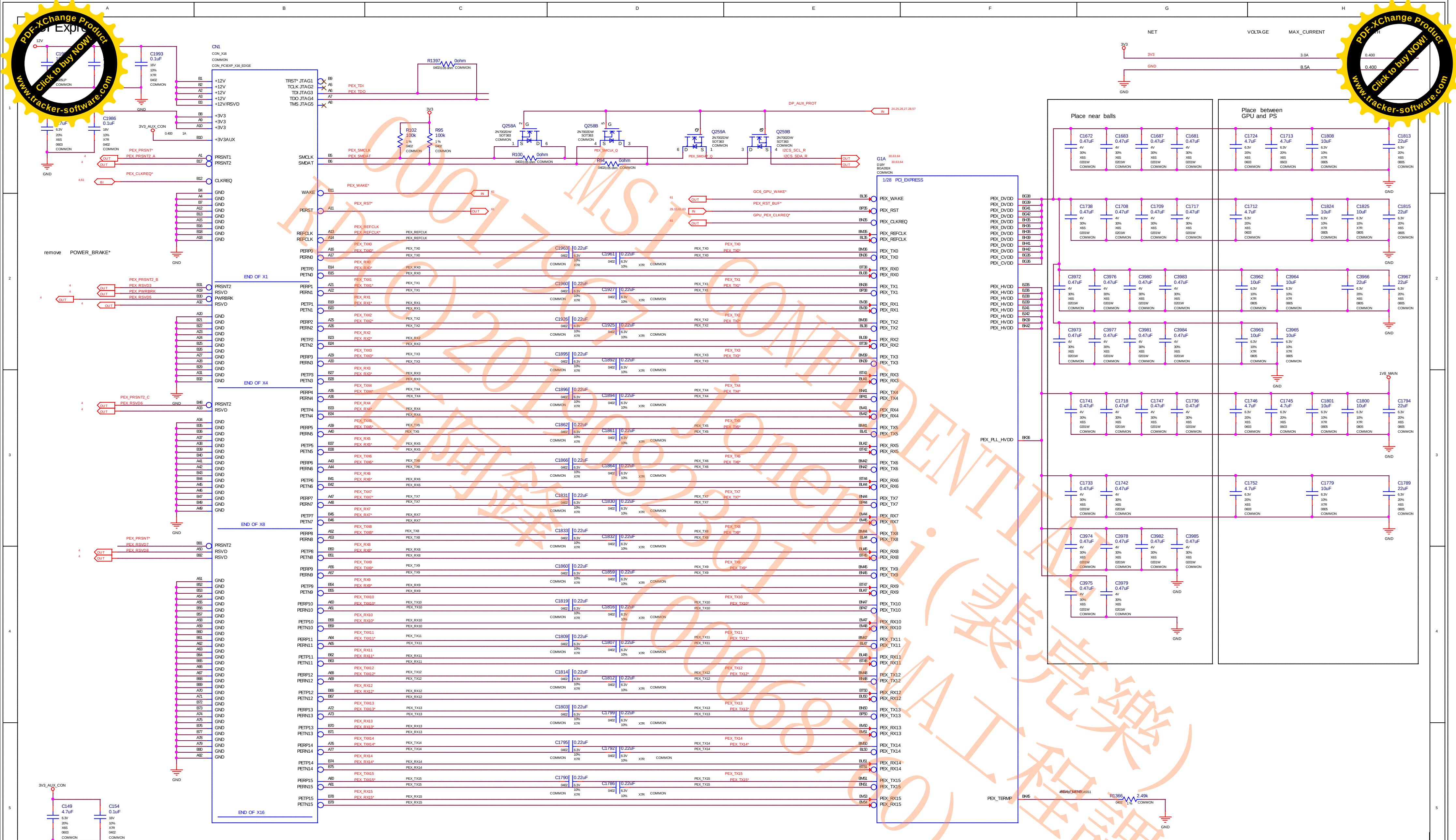

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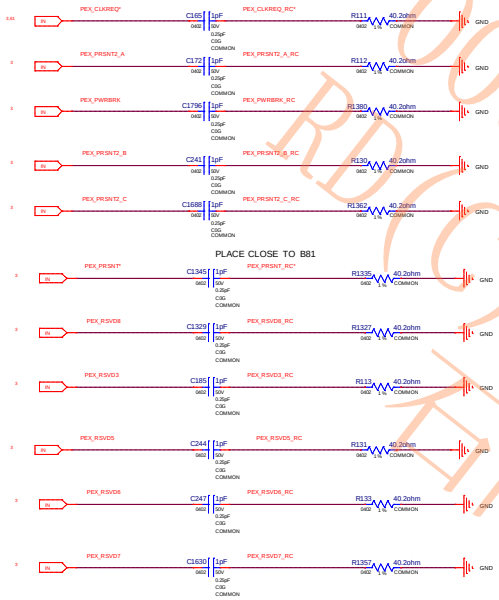
PCI TERM



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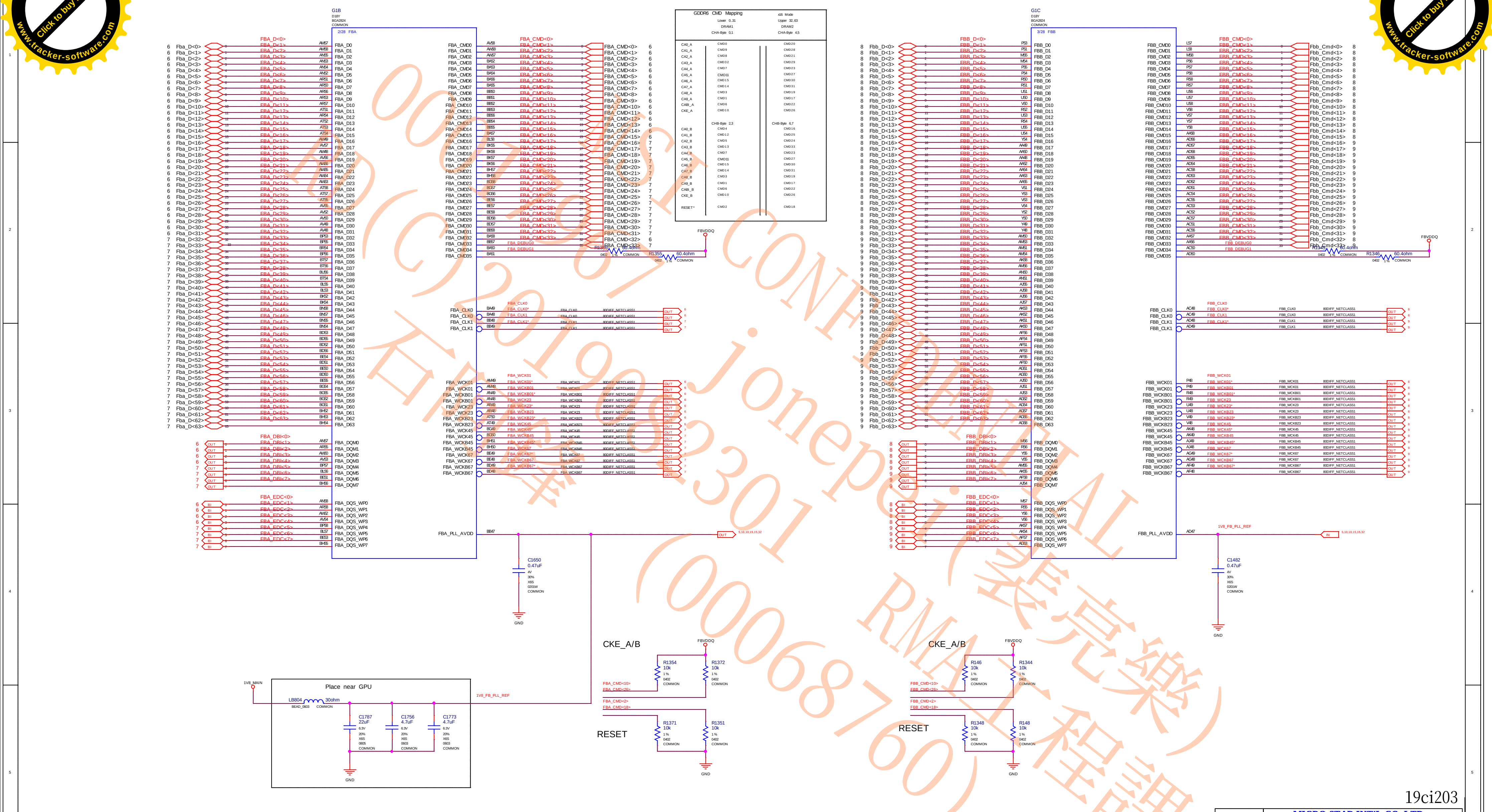

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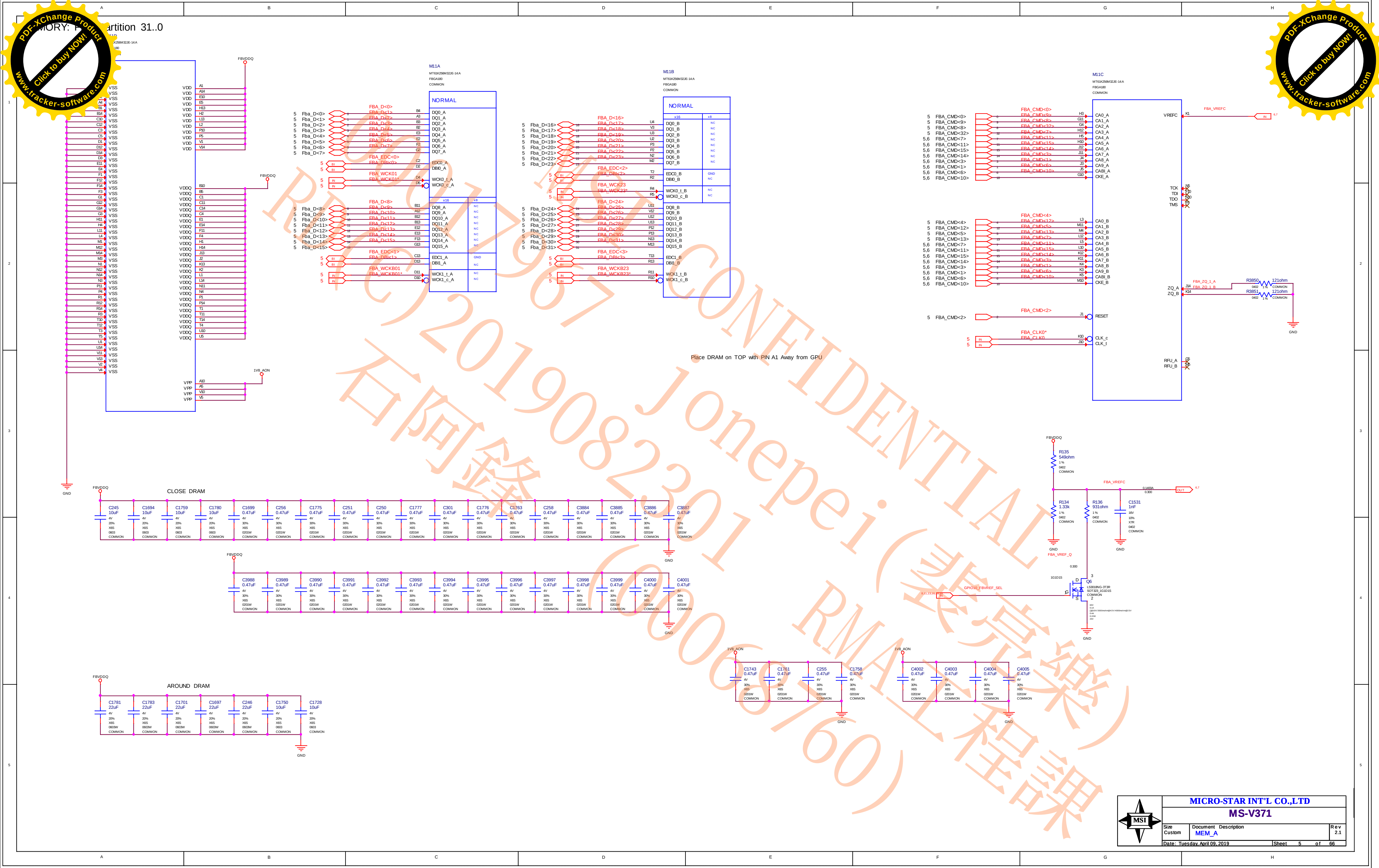

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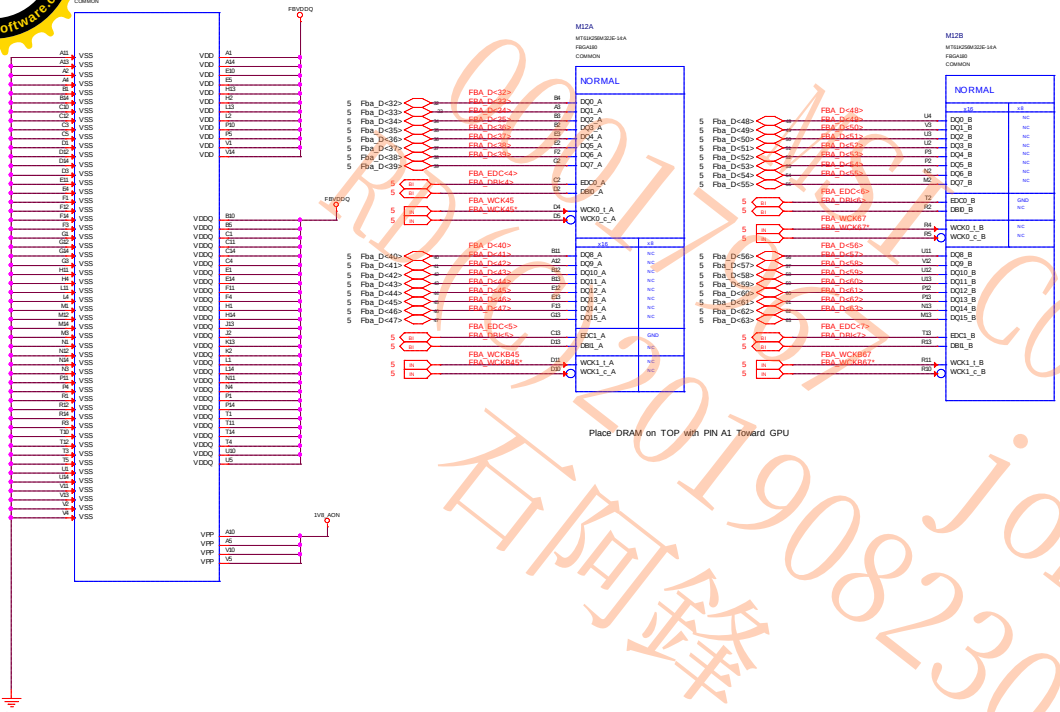
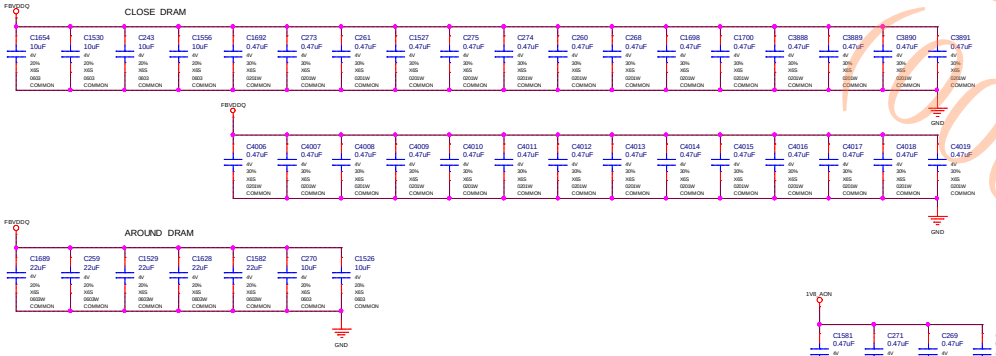
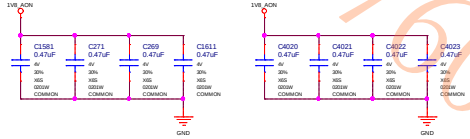
MEMORY: GPU Partition 63..32







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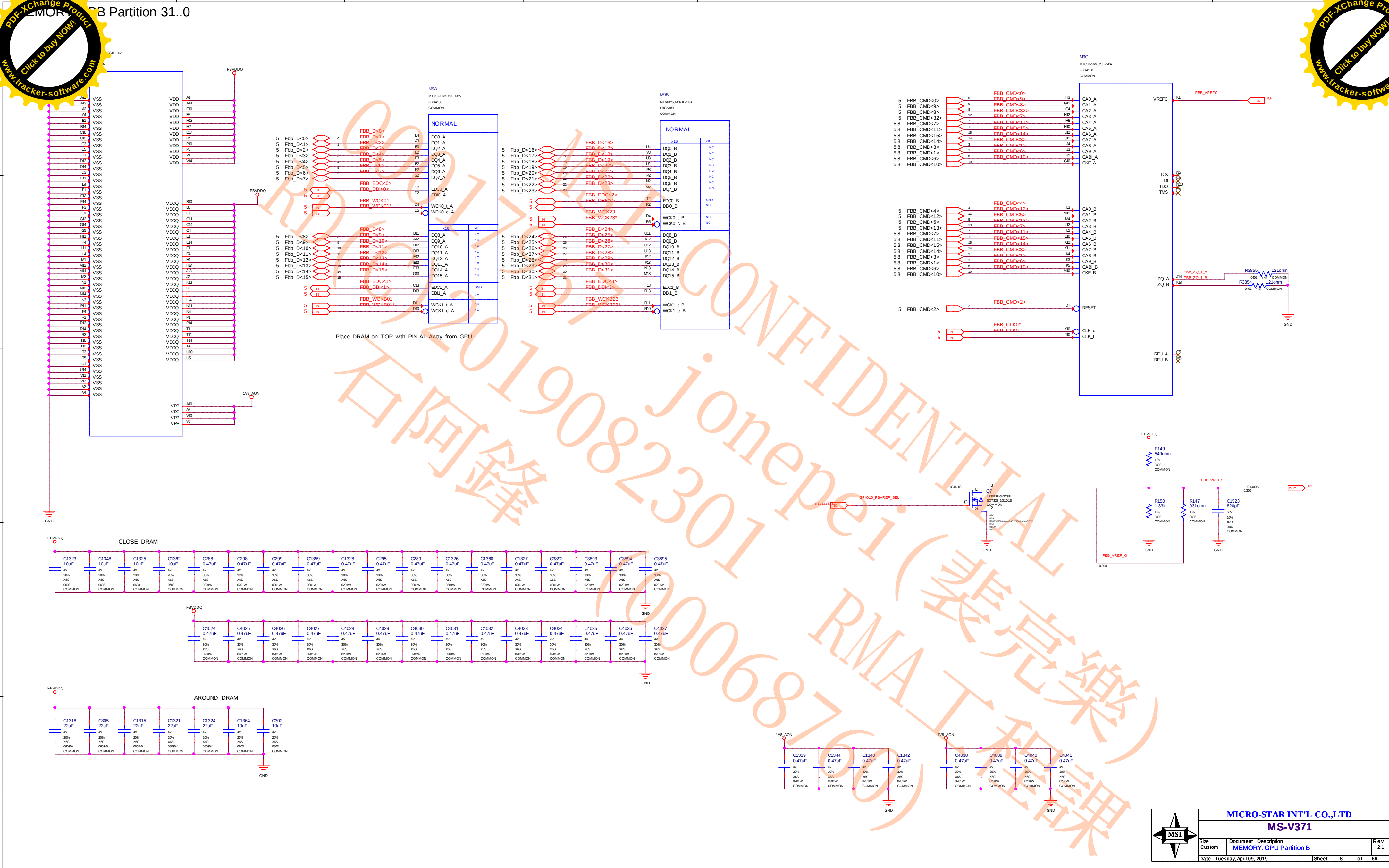
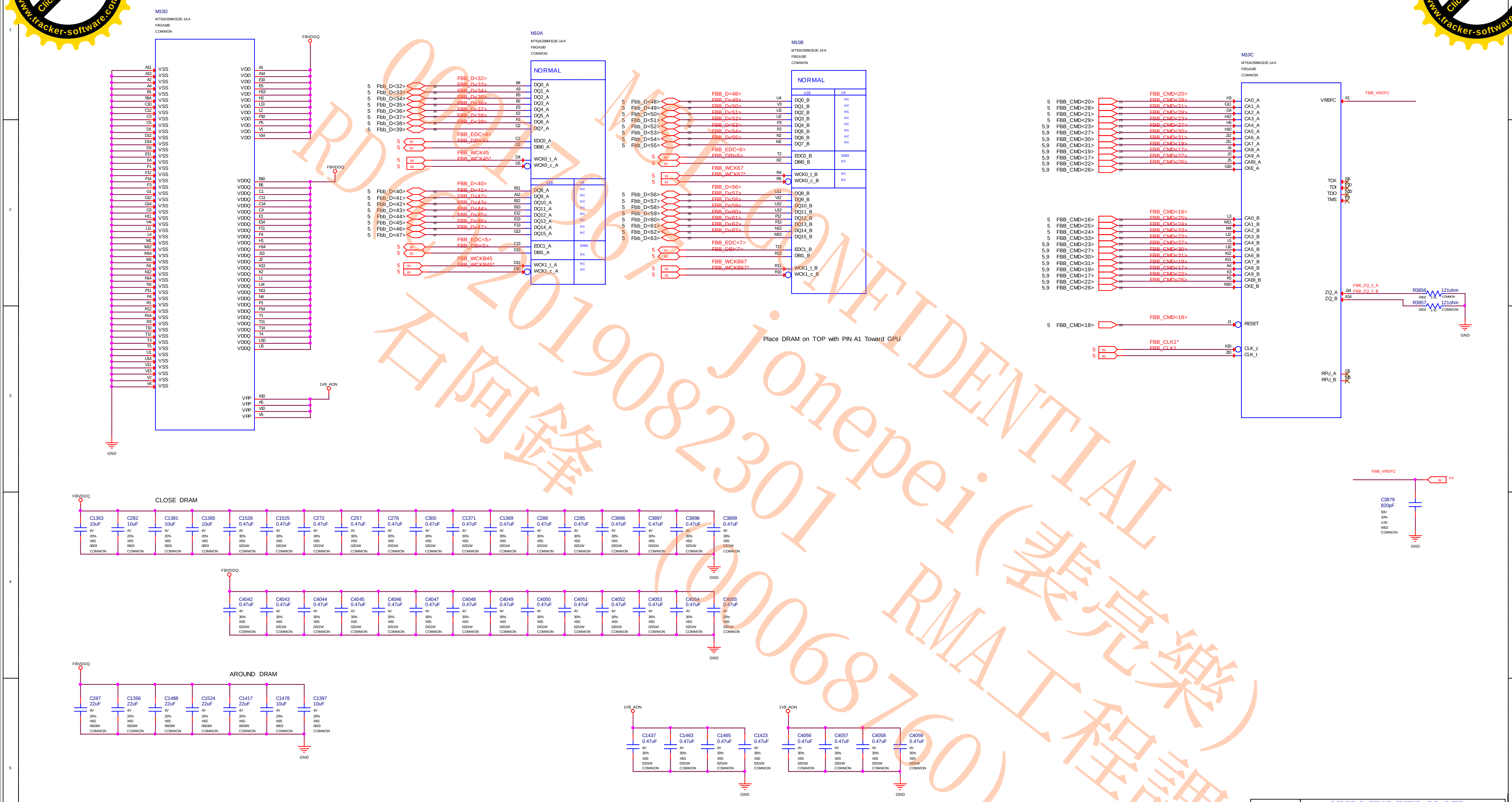


MEMOR... B Partition 63..32



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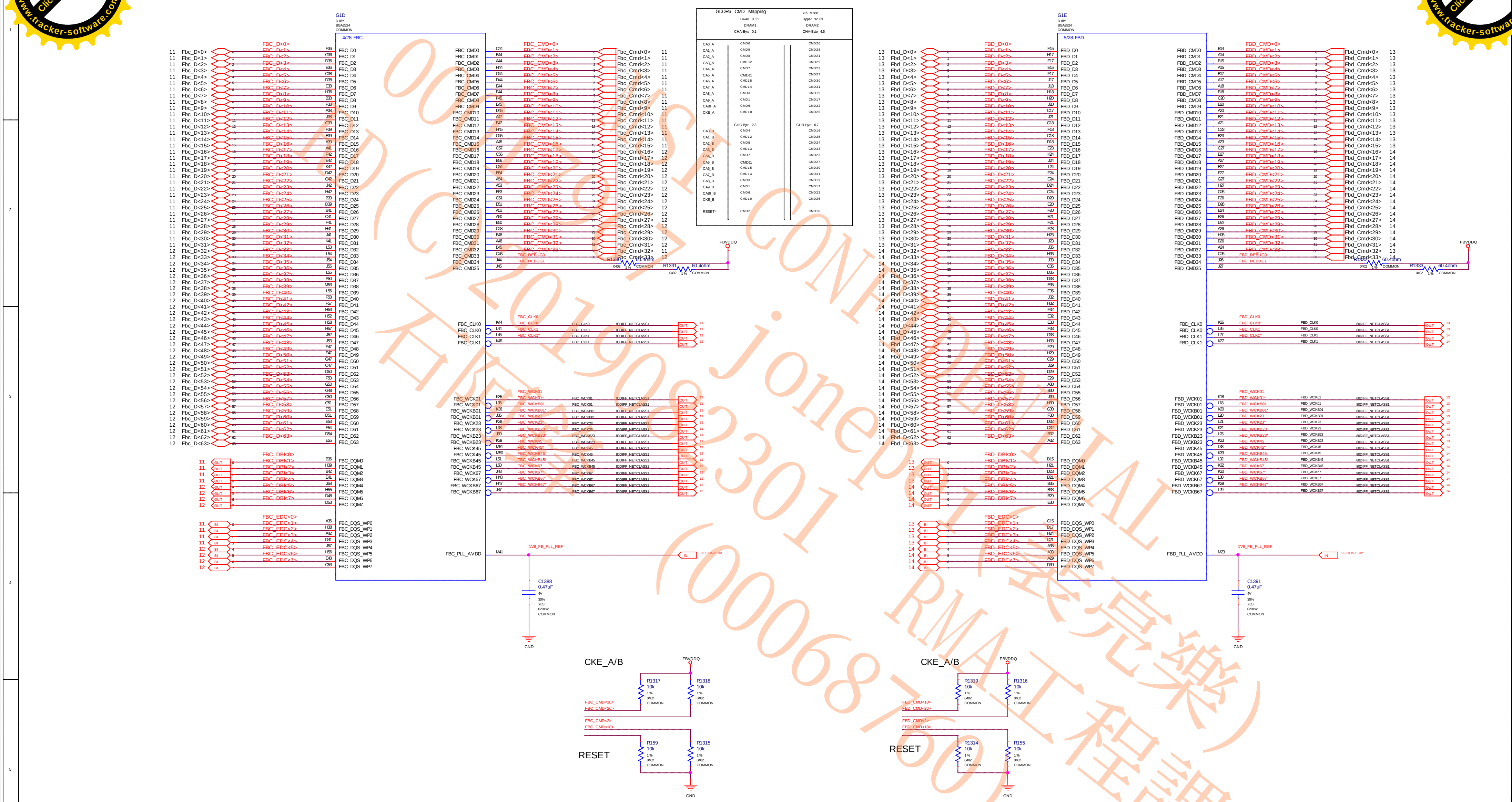
MEMORY: GPU Partition C/D



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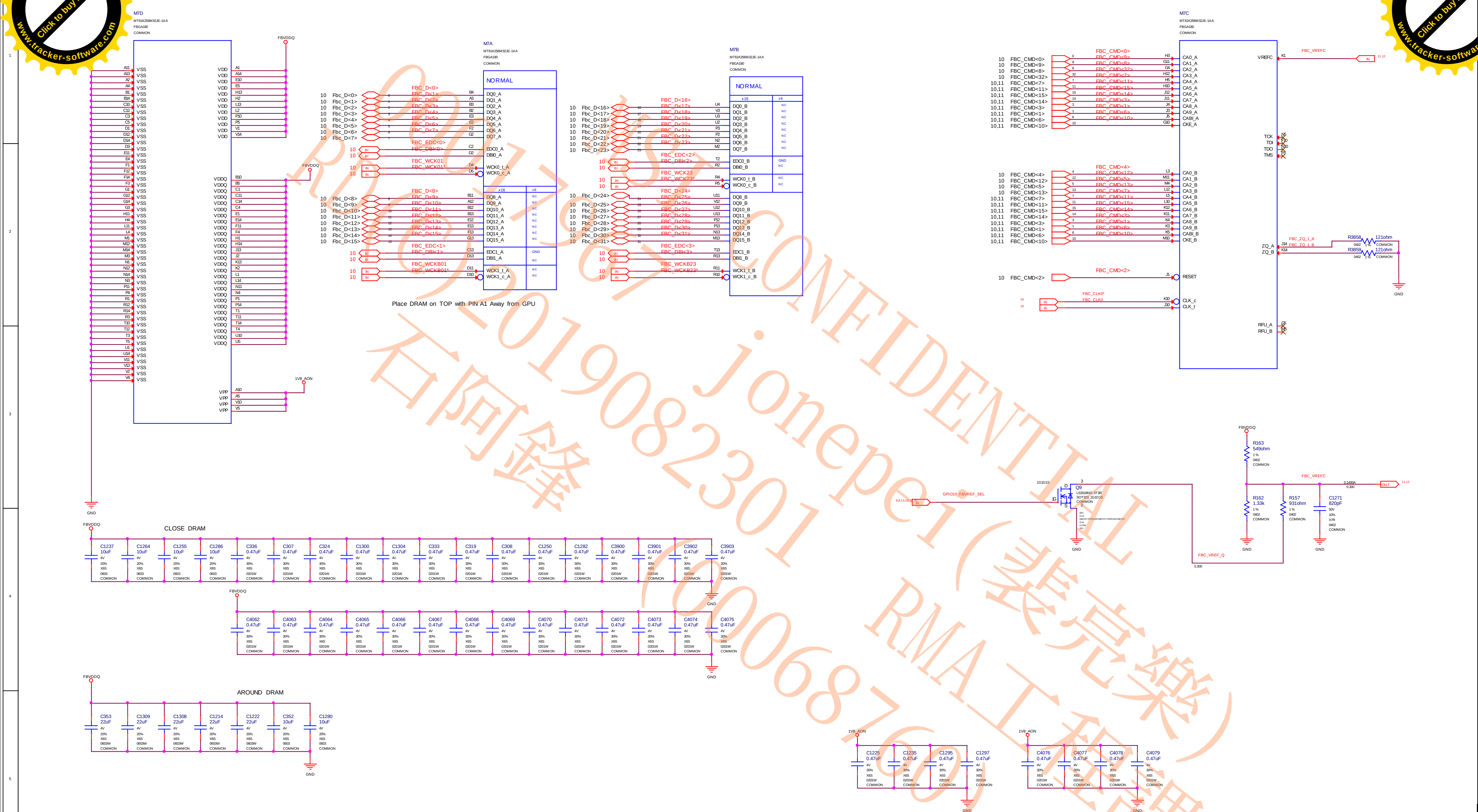
MEMORY: FBC Partition 31..0



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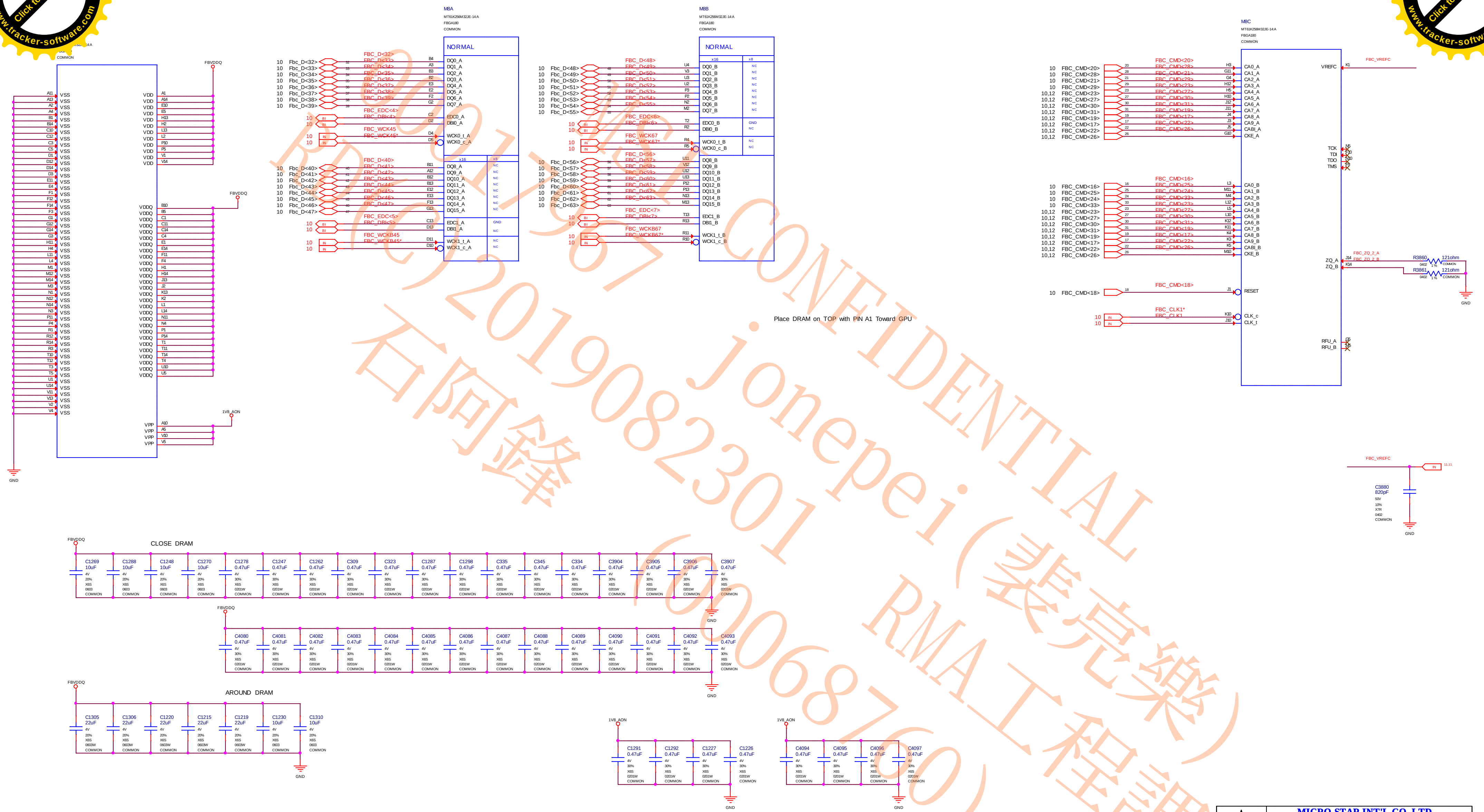
EMOR C Partition 63..32



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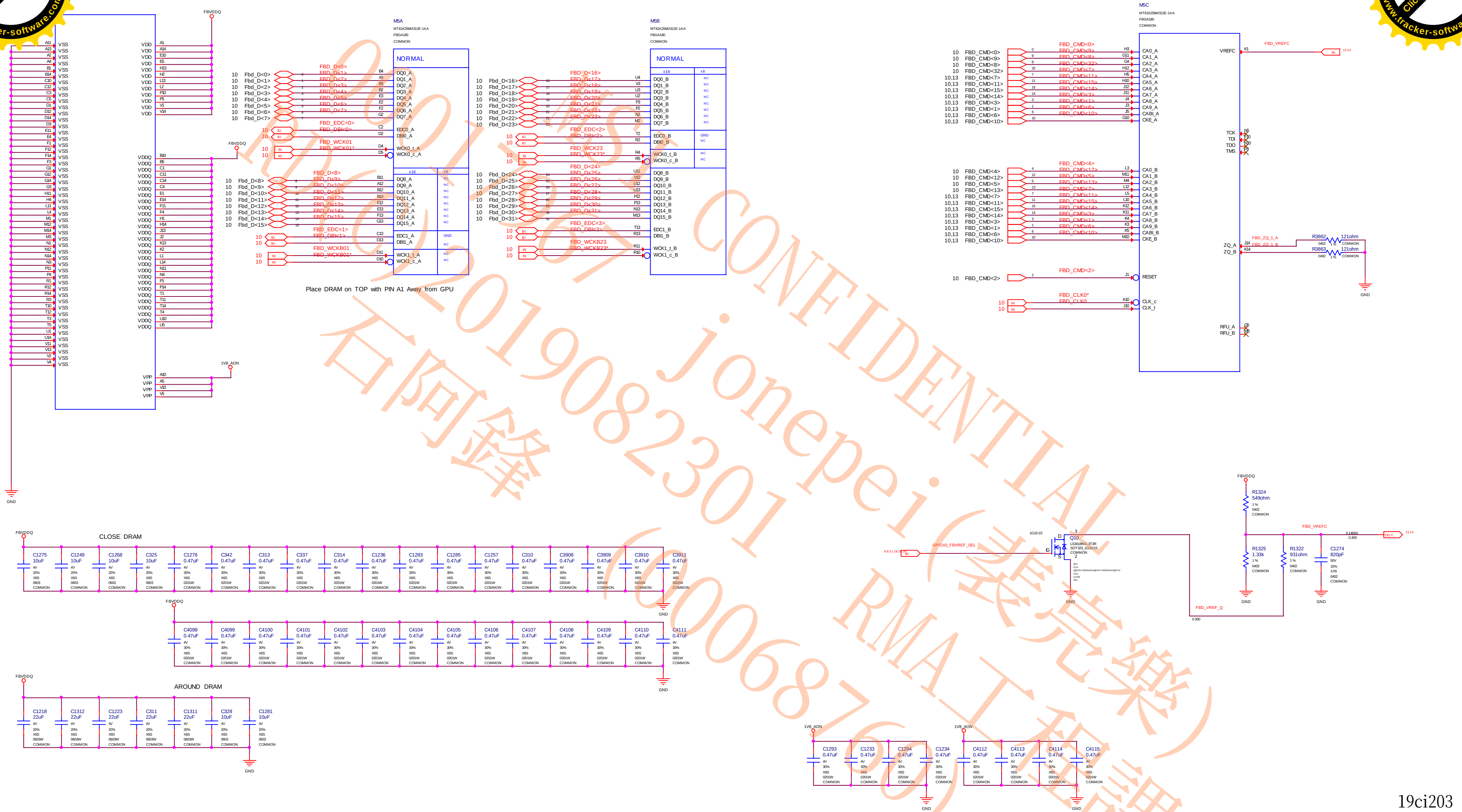
MEMORY: GPD Partition 31..0



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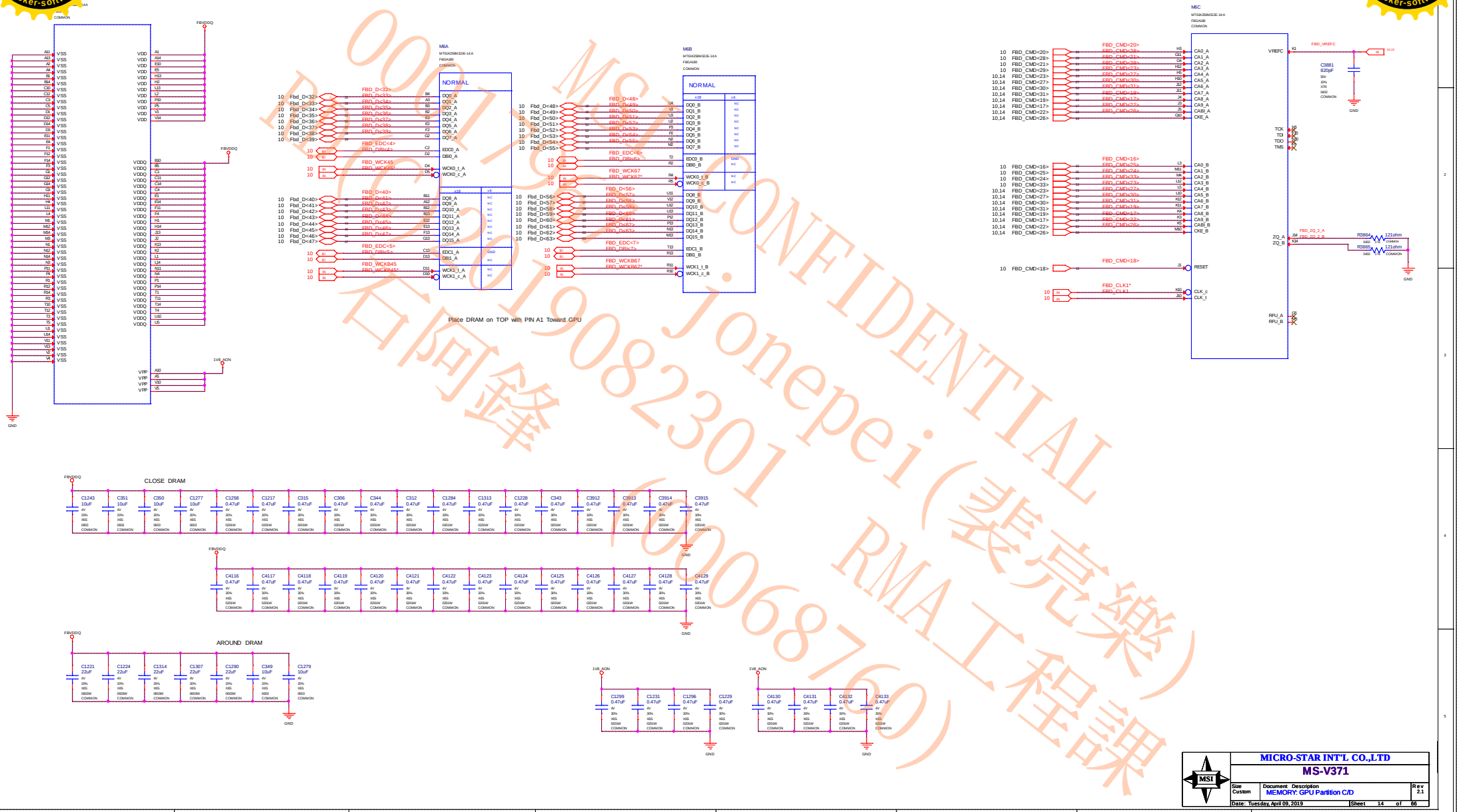
MEMORY GPU Partition 63..32



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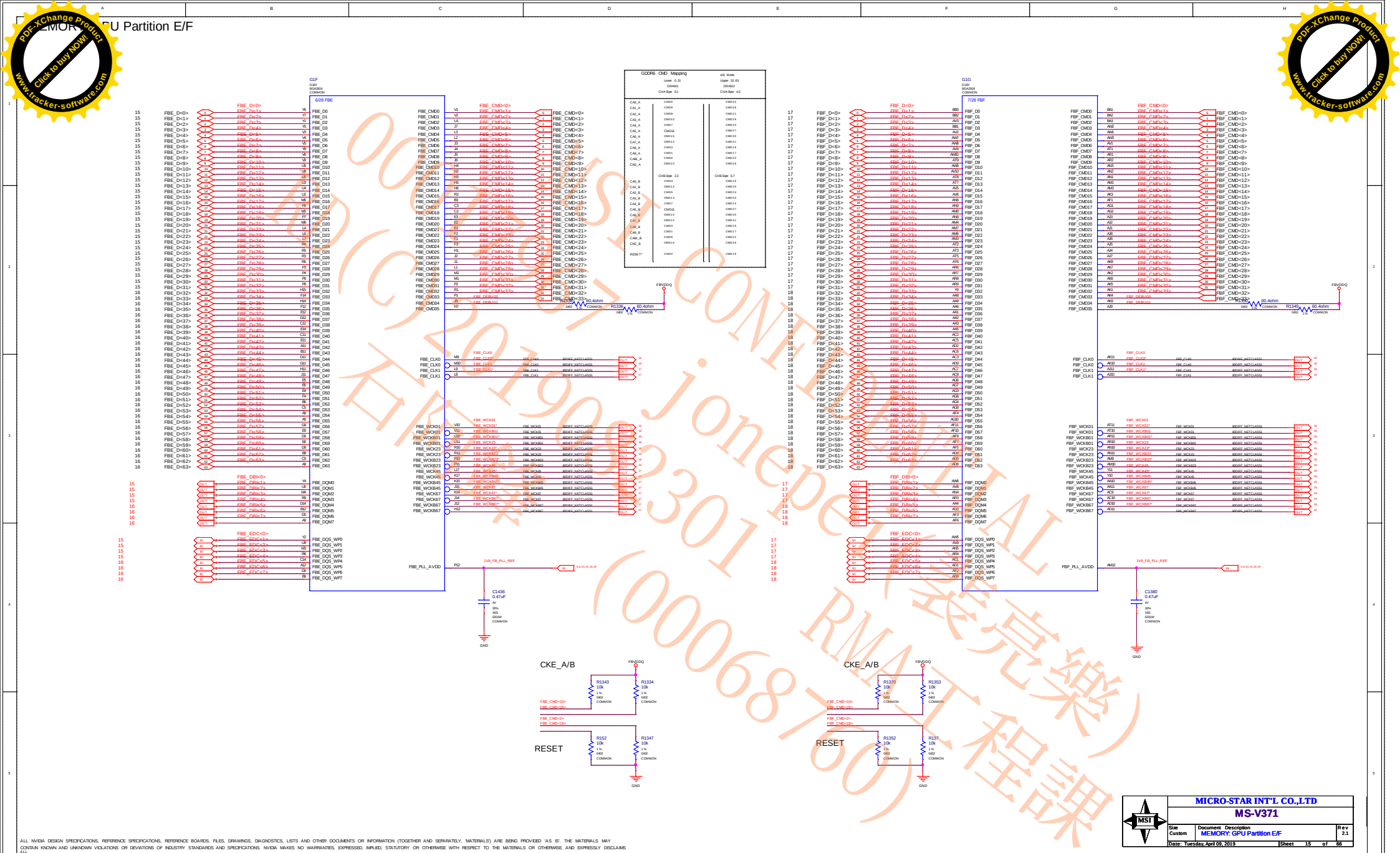
MEMORY: GPU Partition E/F



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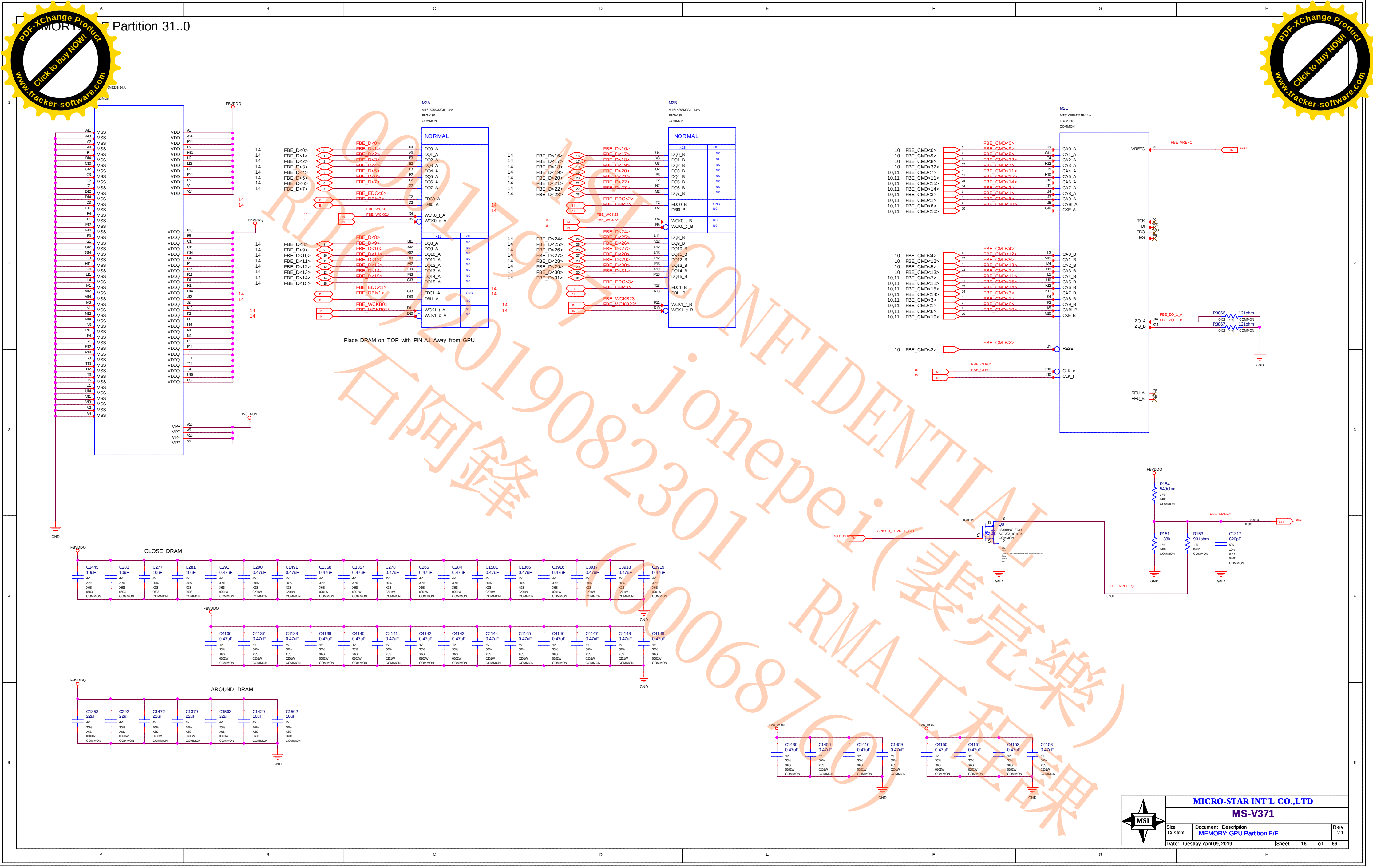

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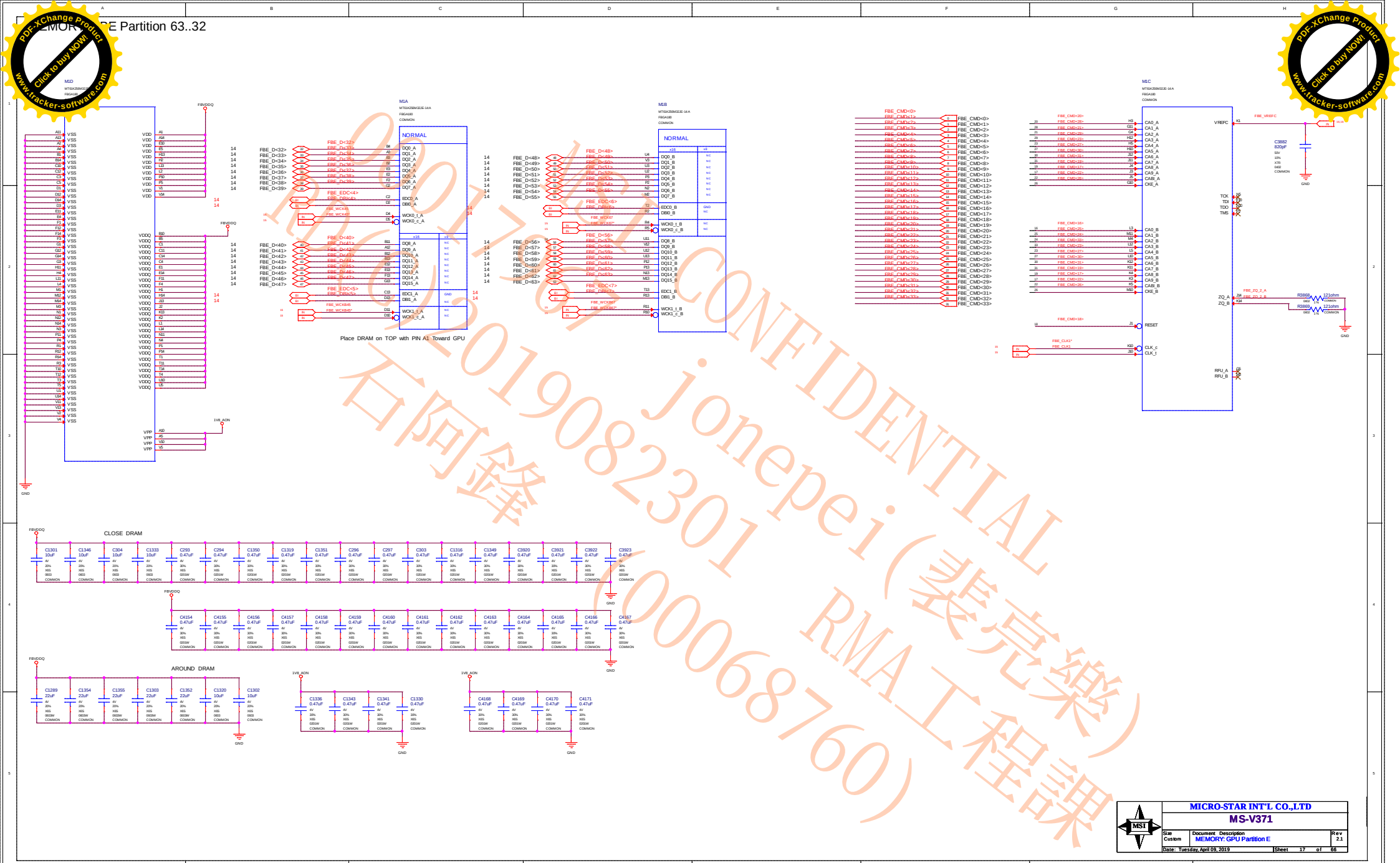

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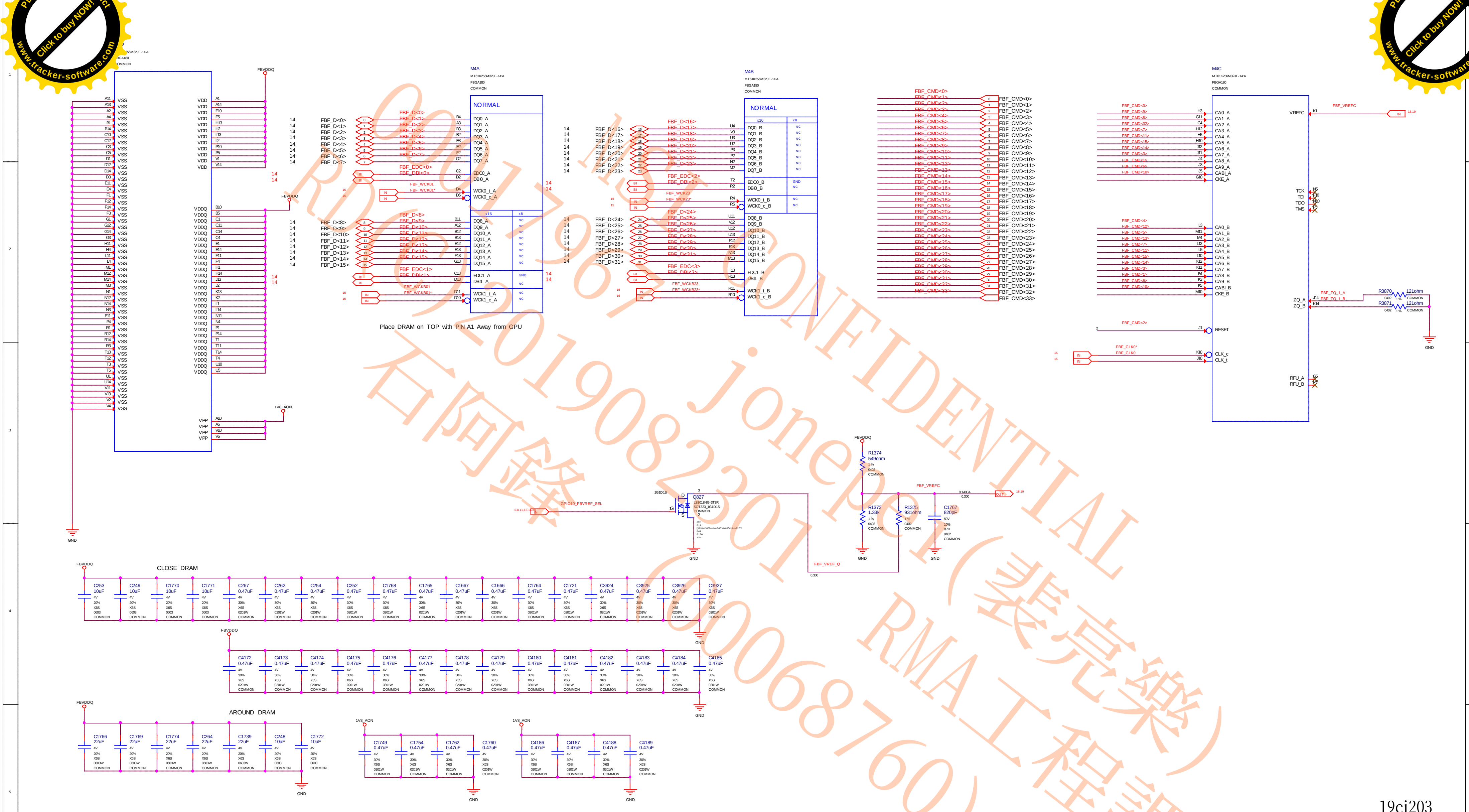
MEMORY: F Partition 31..0



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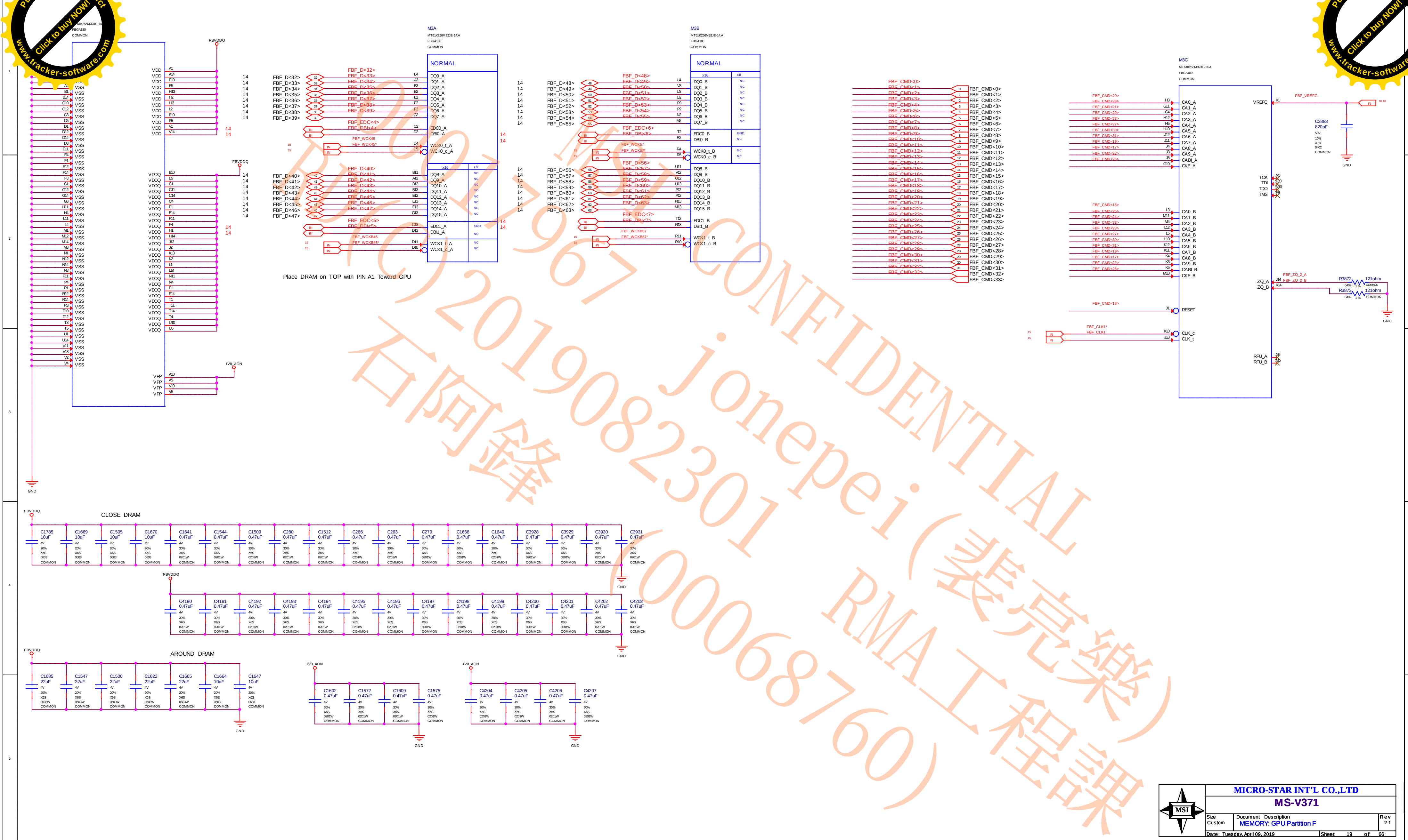
MEMORY: ...F Partition 63..32



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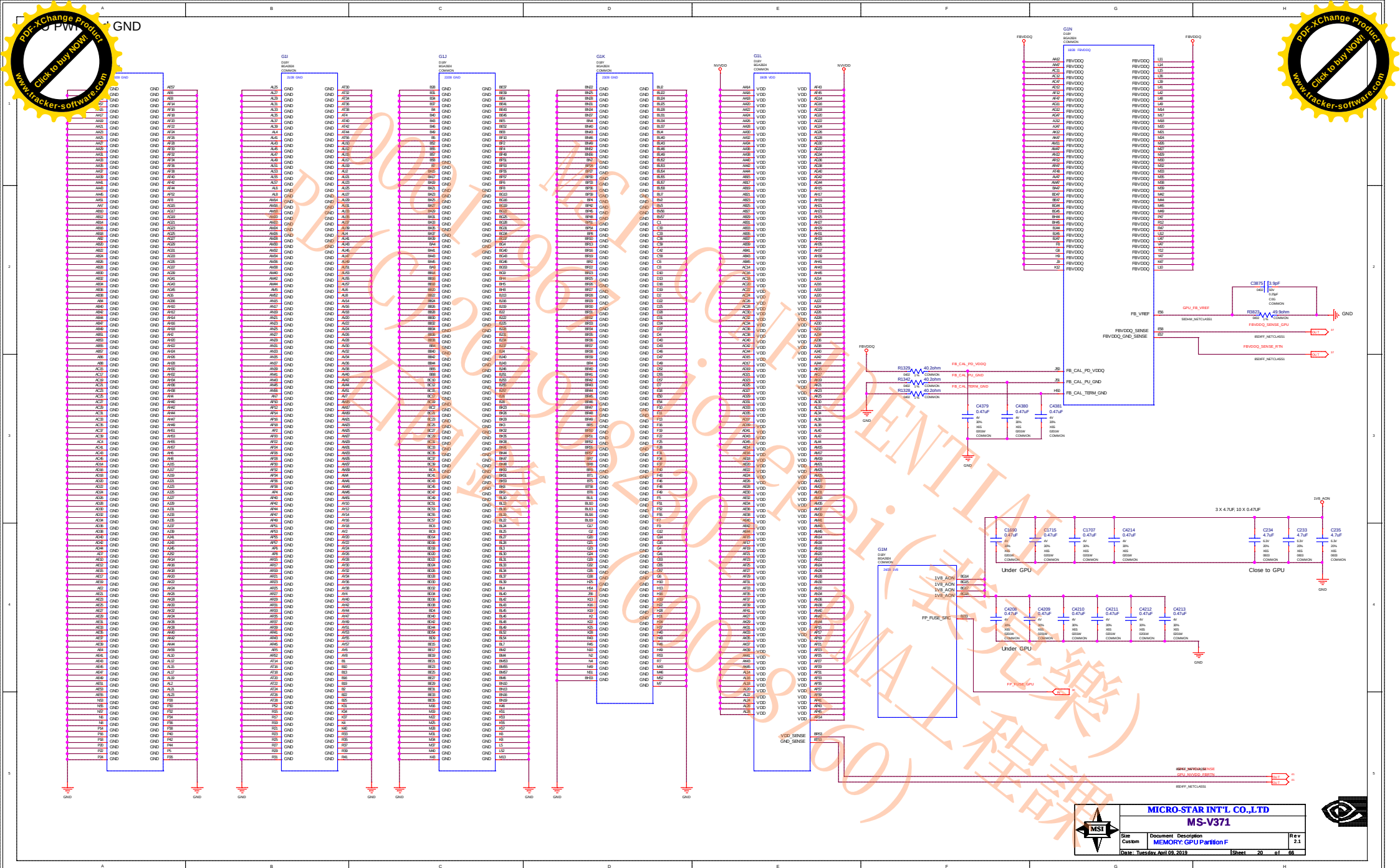
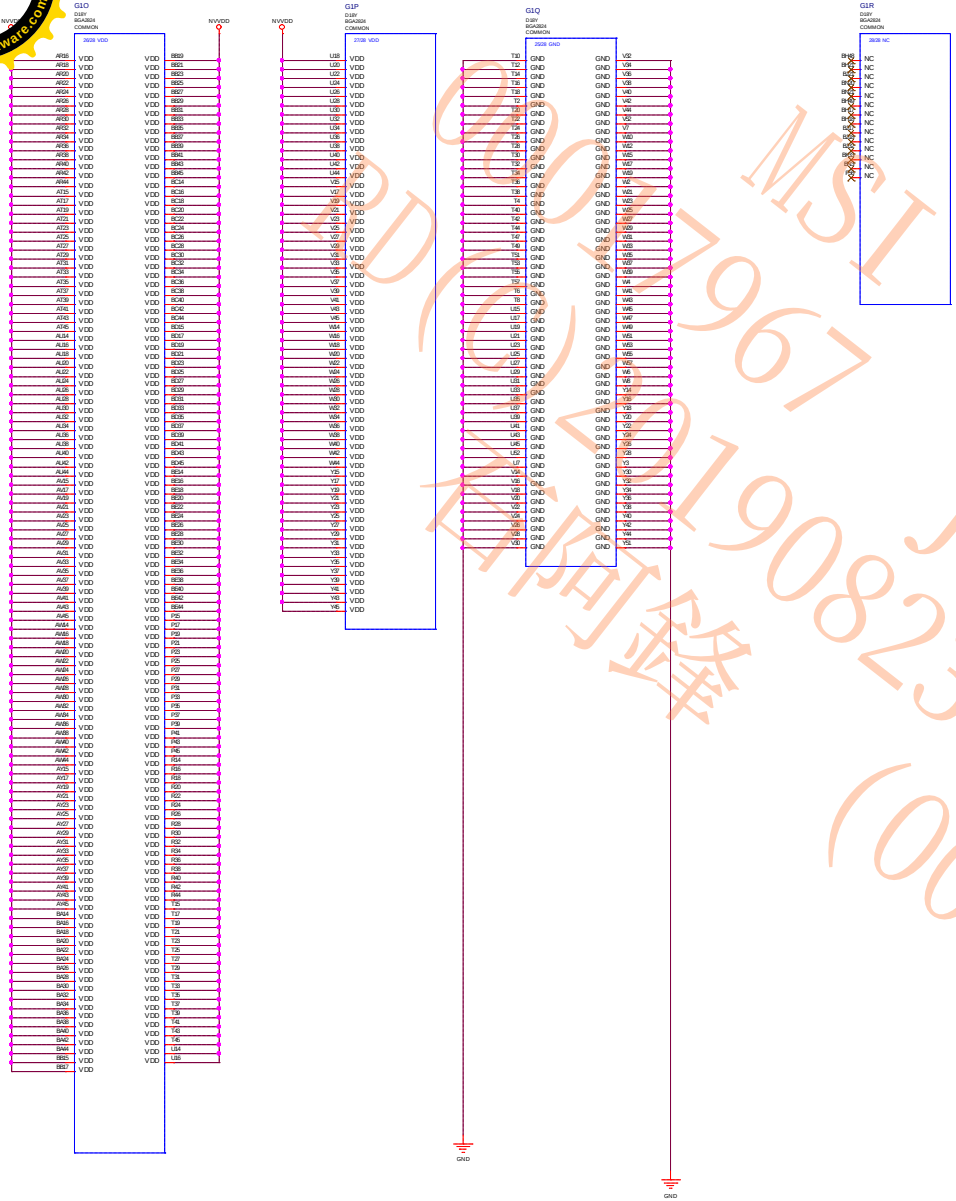


GPU PWR GND NCs



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5 Decoupling

FBVDDQ

Partition A — 2 X 10UF, 6 X 0.47UF

C1704 0.47uF, C1583 0.47uF, C1599 0.47uF, C1557 0.47uF, C1555 0.47uF, C1639 10uF, C1734 10uF

Partition B — 2 X 10UF, 6 X 0.47UF

C1508 0.47uF, C1438 0.47uF, C1386 0.47uF, C1457 0.47uF, C1497 0.47uF, C1468 0.47uF, C1534 10uF, C1428 10uF

Partition C — 2 X 10UF, 6 X 0.47UF

C1387 0.47uF, C1374 0.47uF, C1383 0.47uF, C1401 0.47uF, C1375 0.47uF, C1411 0.47uF, C1391 10uF, C1376 10uF

Partition D — 2 X 10UF, 6 X 0.47UF

C1392 0.47uF, C1368 0.47uF, C1373 0.47uF, C1367 0.47uF, C1382 0.47uF, C1385 0.47uF, C1378 10uF, C1384 10uF

Partition E — 2 X 10UF, 6 X 0.47UF

C1427 0.47uF, C1443 0.47uF, C1418 0.47uF, C1458 0.47uF, C1393 0.47uF, C1370 0.47uF, C1398 10uF, C1464 10uF

Partition F — 2 X 10UF, 6 X 0.47UF

C1568 0.47uF, C1473 0.47uF, C1587 0.47uF, C1507 0.47uF, C1545 0.47uF, C1489 0.47uF, C1629 10uF, C1579 10uF

Place close to GPU — 6 X 10UF

C1377 10uF, C1331 10uF, C1372 10uF, C1576 10uF, C1744 10uF, C1347 10uF

Place close to GPU — 14 X 22UF

C1684 22uF, C1334 22uF, C1337 22uF, C1511 22uF, C1553 22uF, C1332 22uF, C1421 22uF

C1470 22uF, C1338 22uF, C1399 22uF, C1439 22uF, C1335 22uF, C1610 22uF, C1607 22uF

NVVDD

PCB CO-LAYOUT

1 X 470UF + 10 X 47UF overlap

C1577 470uF, C1561 47uF, C1562 47uF, C1592 47uF, C1564 47uF, C1593 47uF, C1567 47uF, C1595 47uF, C1566 47uF, C1596 47uF, C1597 47uF

1 X 470UF + 10 X 47UF overlap

C1467 470uF, C1479 47uF, C1490 47uF, C1447 47uF, C1485 47uF, C1448 47uF, C1486 47uF, C1452 47uF, C1449 47uF, C1 47uF

PCB CO-LAYOUT

12 X 47UF

C1590 47uF, C1591 47uF, C1446 47uF, C1559 47uF, C1563 47uF, C1565 47uF, C1589 47uF, C1487 47uF, C1453 47uF, C1484 47uF, C1451 47uF, C1483 47uF

6 X 22UF

C1455 22uF, C1624 22uF, C1422 22uF, C1434 22uF, C1594 22uF, C1623 22uF

30 X 10UF

C1653 10uF, C1652 10uF, C1651 10uF, C1642 10uF, C1403 10uF, C1514 10uF, C1521 10uF, C1400 10uF, C1515 10uF, C1517 10uF, C1686 10uF, C1615 10uF, C1614 10uF, C1638 10uF, C1636 10uF, C1516 10uF, C1520 10uF, C1519 10uF, C1518 10uF, C1513 10uF

C1645 10uF, C1644 10uF, C1643 10uF, C1677 10uF, C1543 10uF, C1432 10uF, C1620 10uF, C1433 10uF, C1407 10uF, C1536 10uF

16 X 4.7UF

C1541 4.7uF, C1424 4.7uF, C1619 4.7uF, C1429 4.7uF, C1634 4.7uF, C1539 4.7uF, C1617 4.7uF, C1425 4.7uF, C1535 4.7uF, C1537 4.7uF, C1626 4.7uF, C1431 4.7uF, C1542 4.7uF, C1404 4.7uF, C1540 4.7uF, C1538 4.7uF

80 X 0.47UF

C1442 0.47uF, C1462 0.47uF, C1419 0.47uF, C1660 0.47uF, C1510 0.47uF, C1631 0.47uF, C1569 0.47uF, C1532 0.47uF, C1406 0.47uF, C1414 0.47uF, C1627 0.47uF, C1548 0.47uF, C1490 0.47uF, C1408 0.47uF, C1656 0.47uF, C1549 0.47uF, C1454 0.47uF, C1469 0.47uF, C1552 0.47uF, C1533 0.47uF

C1426 0.47uF, C1588 0.47uF, C1410 0.47uF, C1499 0.47uF, C1649 0.47uF, C1655 0.47uF, C1496 0.47uF, C1554 0.47uF, C1475 0.47uF, C1474 0.47uF, C1394 0.47uF, C1676 0.47uF, C1466 0.47uF, C1460 0.47uF, C1635 0.47uF, C1498 0.47uF, C1494 0.47uF, C1570 0.47uF, C1440 0.47uF, C1413 0.47uF

C1412 0.47uF, C1476 0.47uF, C1598 0.47uF, C1603 0.47uF, C1477 0.47uF, C1585 0.47uF, C1571 0.47uF, C1671 0.47uF, C1495 0.47uF, C1573 0.47uF, C1625 0.47uF, C1409 0.47uF, C1461 0.47uF, C1396 0.47uF, C1402 0.47uF, C1441 0.47uF, C1560 0.47uF, C1580 0.47uF, C1613 0.47uF, C1605 0.47uF

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GPU De[illegible]pling

FBVDDQ

FBVDDQ

Partition A — 2 X 10UF, 6 X 0.47UF — 80 X 0.47UF

C4260 C4266 C4272 C4278 C4284

Partition B — 2 X 10UF, 6 X 0.47UF

C4255 C4261 C4267 C4273 C4279 C4285

Partition C — 2 X 10UF, 6 X 0.47UF

C4256 C4262 C4268 C4274 C4280 C4286

Partition D — 2 X 10UF, 6 X 0.47UF

C4257 C4263 C4269 C4275 C4281 C4287

Partition E — 2 X 10UF, 6 X 0.47UF

C4258 C4264 C4270 C4276 C4282 C4288

Partition F — 2 X 10UF, 6 X 0.47UF

C4259 C4265 C4271 C4277 C4283 C4289

Each: 0.47uF, 4V, 30%, X6S, 0201W, COMMON; GND

NVVDD

NVVDD

C4290 C4294 C4298 C4302 C4306 C4310 C4314 C4318 C4322 C4326 C4330 C4334 C4338 C4342 C4346 C4350 C4354 C4358 C4362 C4366

C4291 C4295 C4299 C4303 C4307 C4311 C4315 C4319 C4323 C4327 C4331 C4335 C4339 C4343 C4347 C4351 C4355 C4359 C4363 C4367

C4292 C4296 C4300 C4304 C4308 C4312 C4316 C4320 C4324 C4328 C4332 C4336 C4340 C4344 C4348 C4352 C4356 C4360 C4364 C4368

C4293 C4297 C4301 C4305 C4309 C4313 C4317 C4321 C4325 C4329 C4333 C4337 C4341 C4345 C4349 C4353 C4357 C4361 C4365 C4369

Each: 0.47uF, 4V, 30%, X6S, 0201W, COMMON; GND

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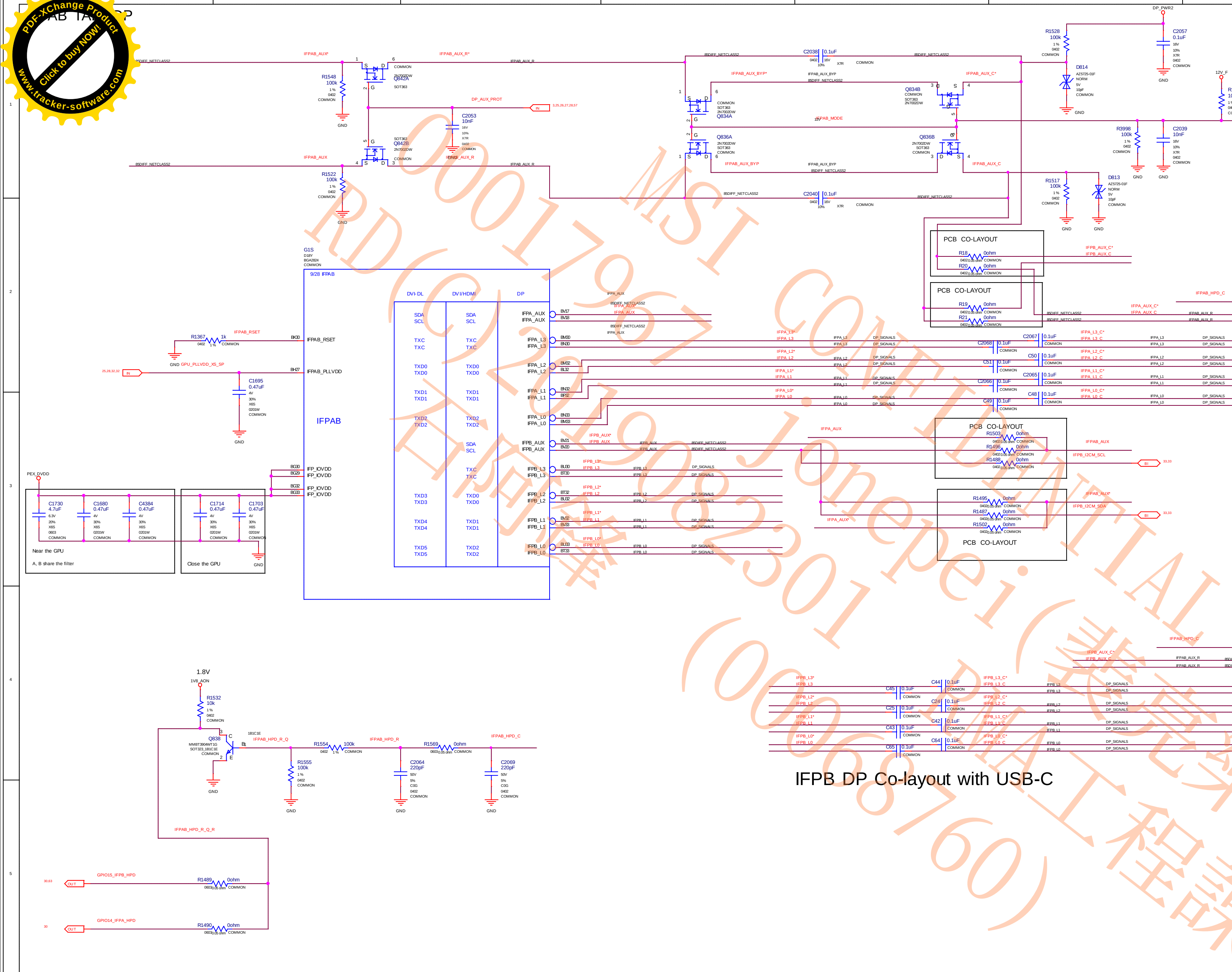

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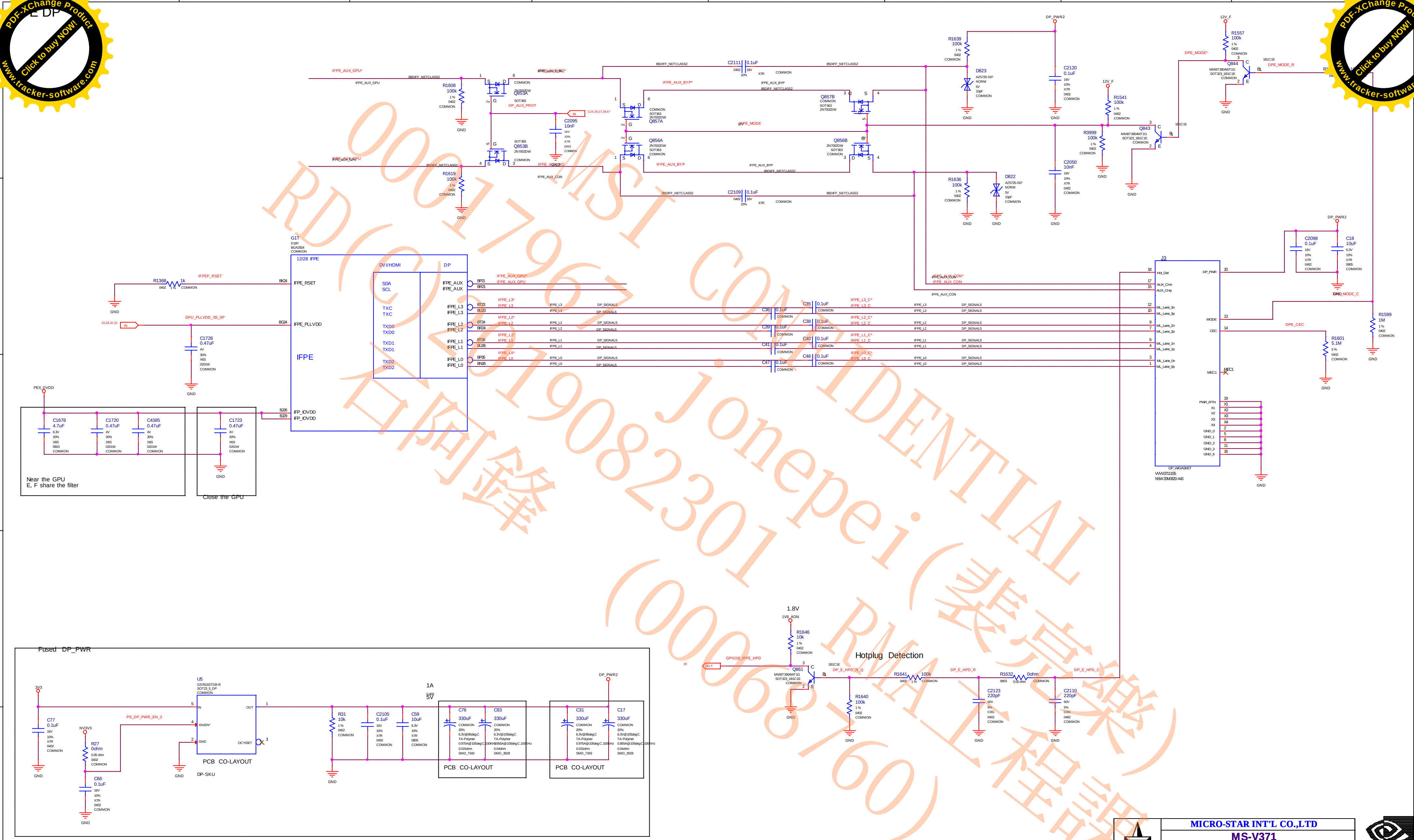
IFPE DP



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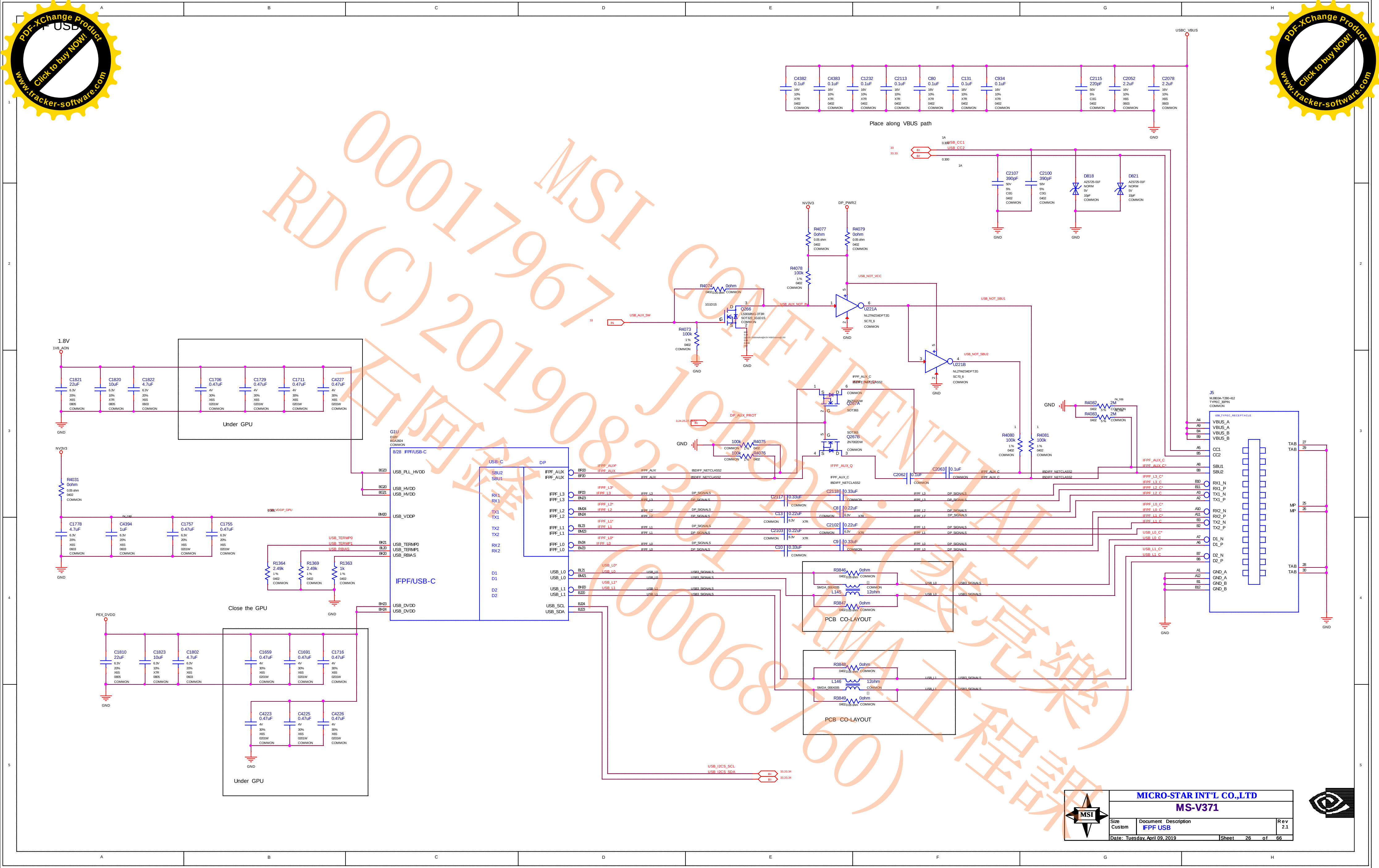

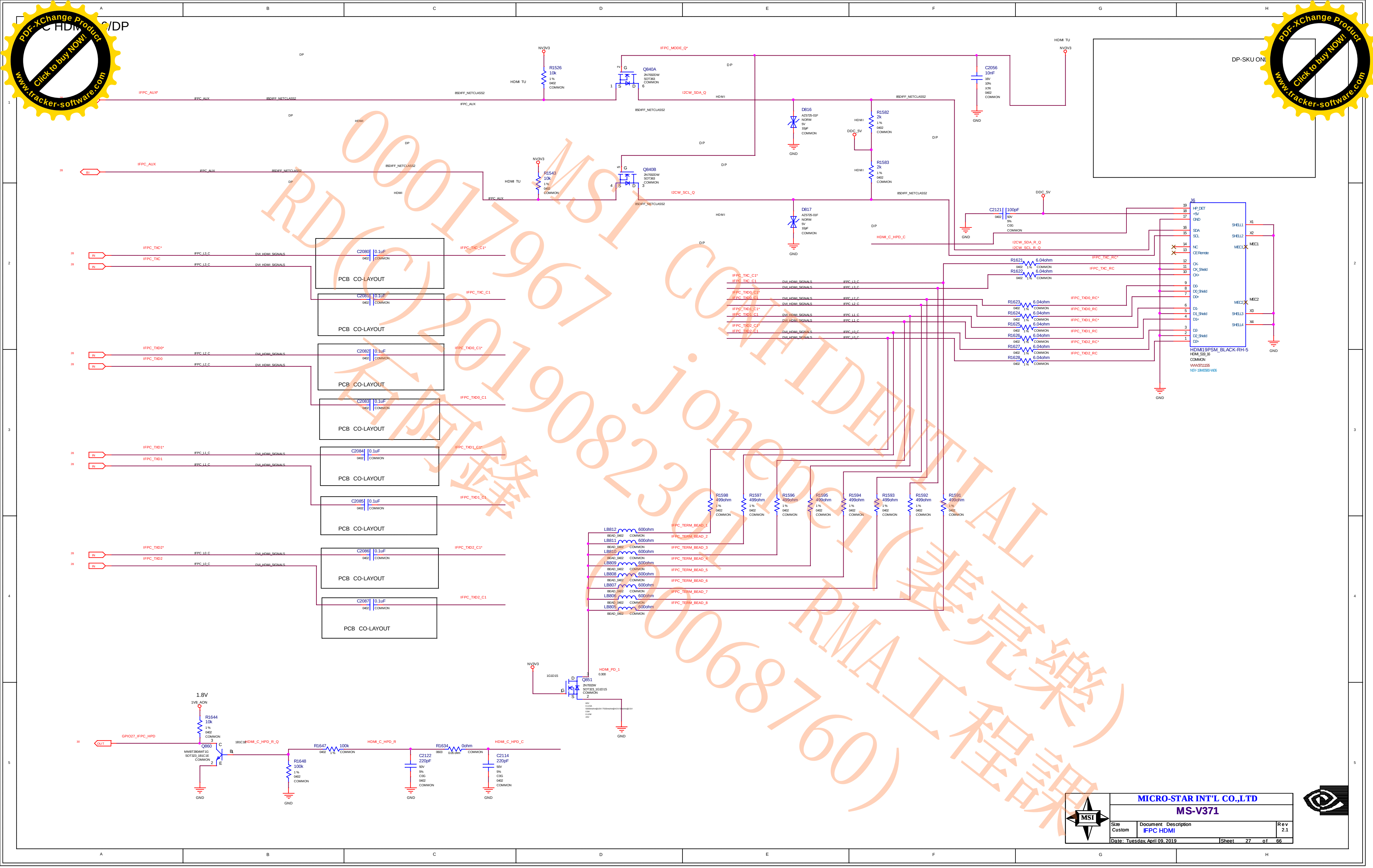

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NV3V3
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IFPC_AUX*
IFPC_AUX
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I2CW_SCL_Q
Q840A
Q840B
2N7002DW
R1526 10k
R1543 10k
D816
D817
AZ5725-01F
R1582 2k
R1583 2k
DDC_5V
C2056 10nF
C2121 100pF
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IFPC_TXC
IFPC_TXD0*
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R1648 100k
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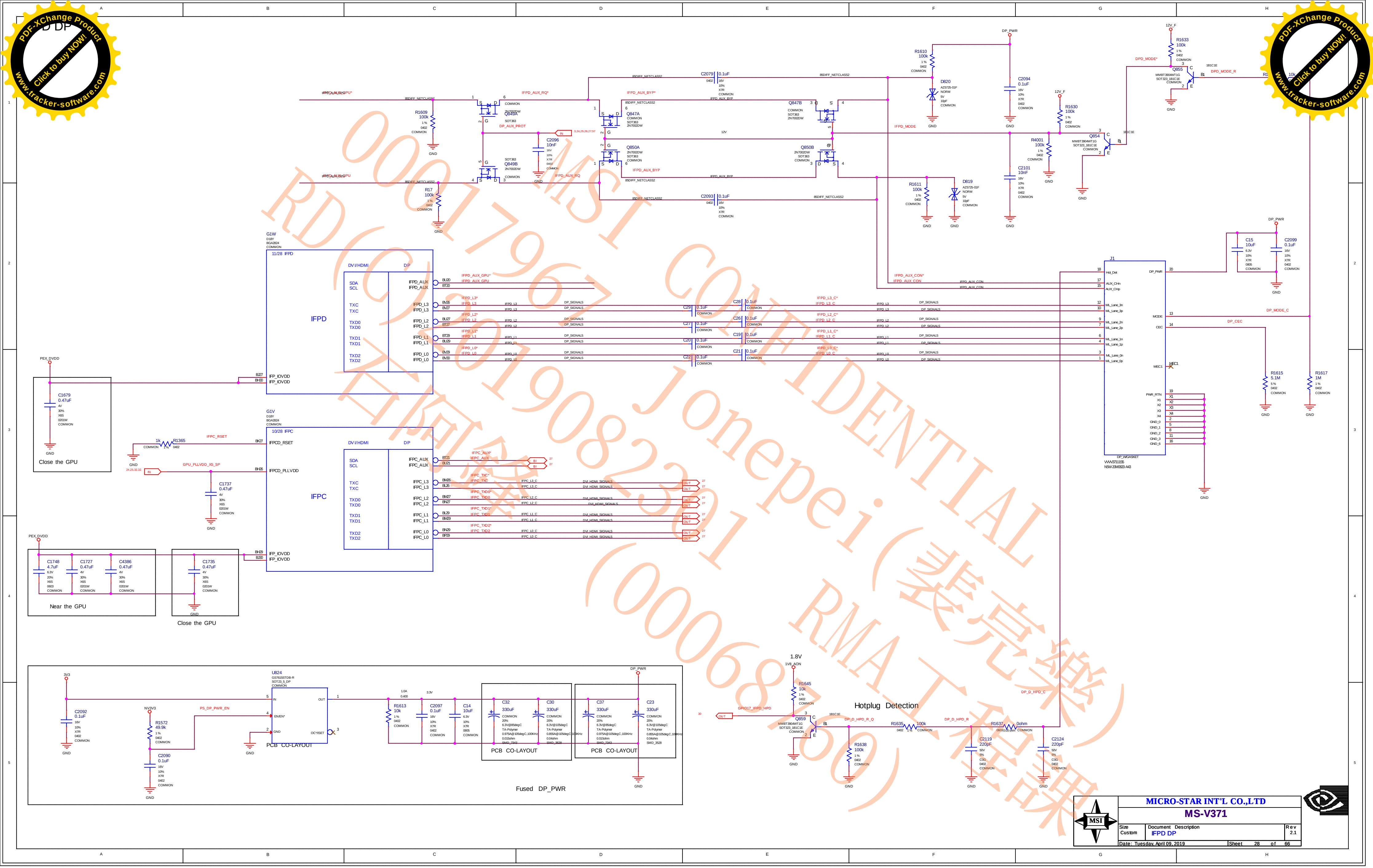

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NVHS Interface and FRAME LOCK

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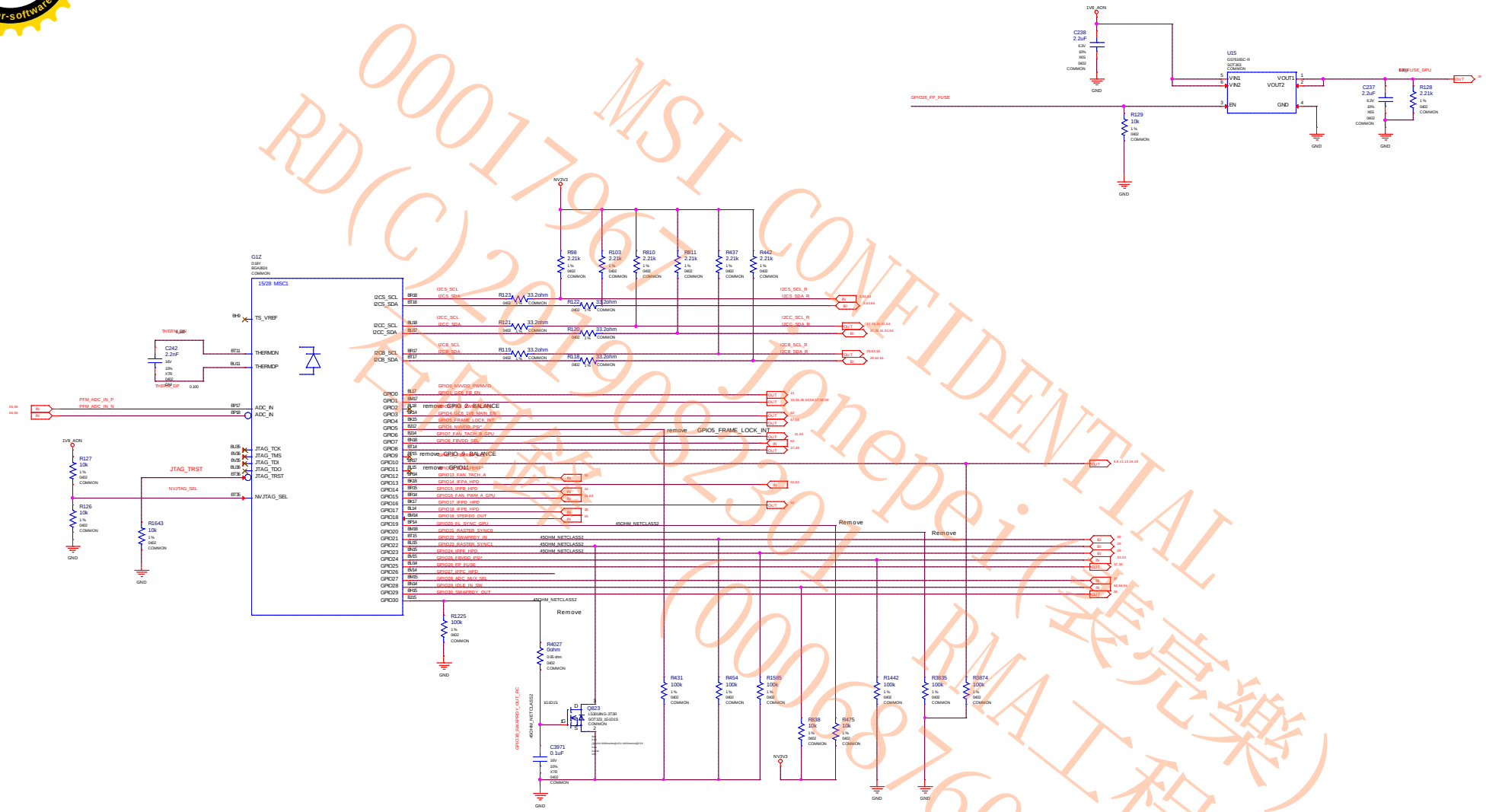
SC1: Fan, Thermal, JTAG, GPIO, STEREO



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[illegible]SC2: R[illegible] Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
[illegible]	L	L	00000	
L	L	H	00001	DEFAULT
[illegible]	H	L	00010	
[illegible]	H	H	00011	
H	L	L	00100	
H	L	H	00101	
H	H	L	00110	
H	H	H	00111	
L	L	M	01000	
L	M	L	01001	

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	H	XXX0	FS_OVERT DISABLE	

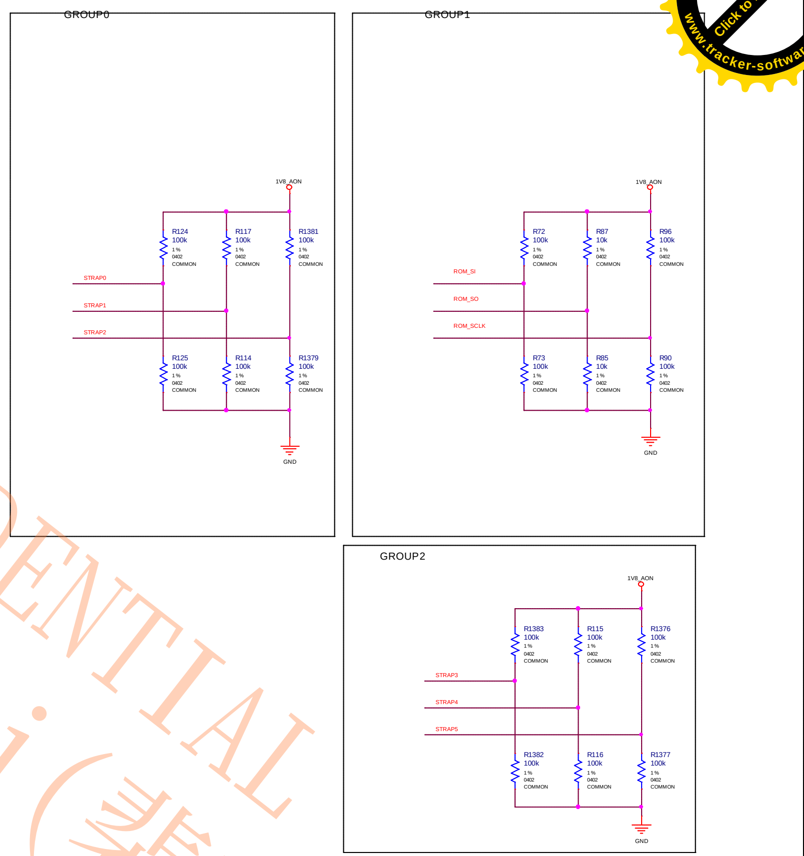
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

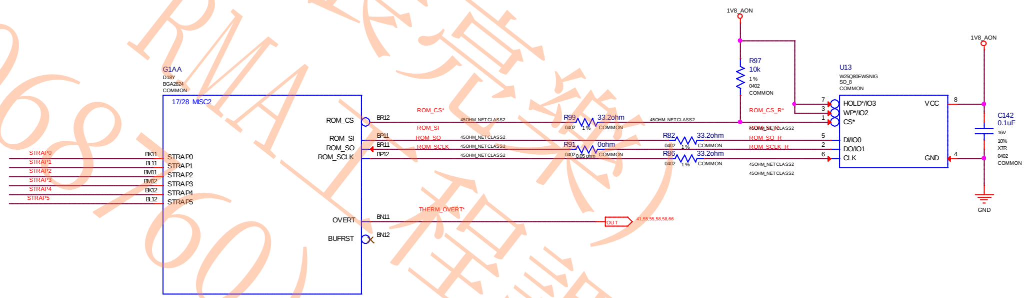
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	SKU 200





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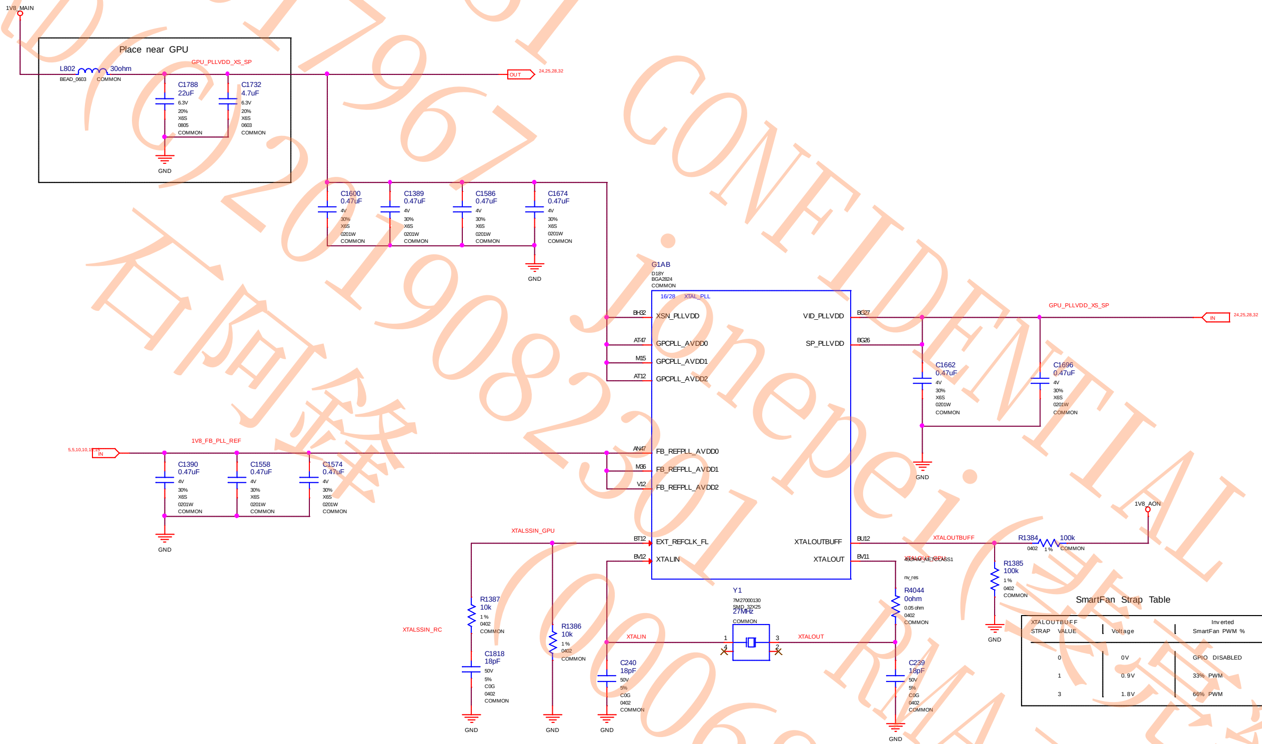
GC2: X[illegible] PLL



SmartFan Strap Table

XTALOUTBUFF STRAP VALUE	Voltage	Inverted SmartFan PWM %
0	0V	GPIO DISABLED
1	0.9V	33% PWM
3	1.8V	66% PWM

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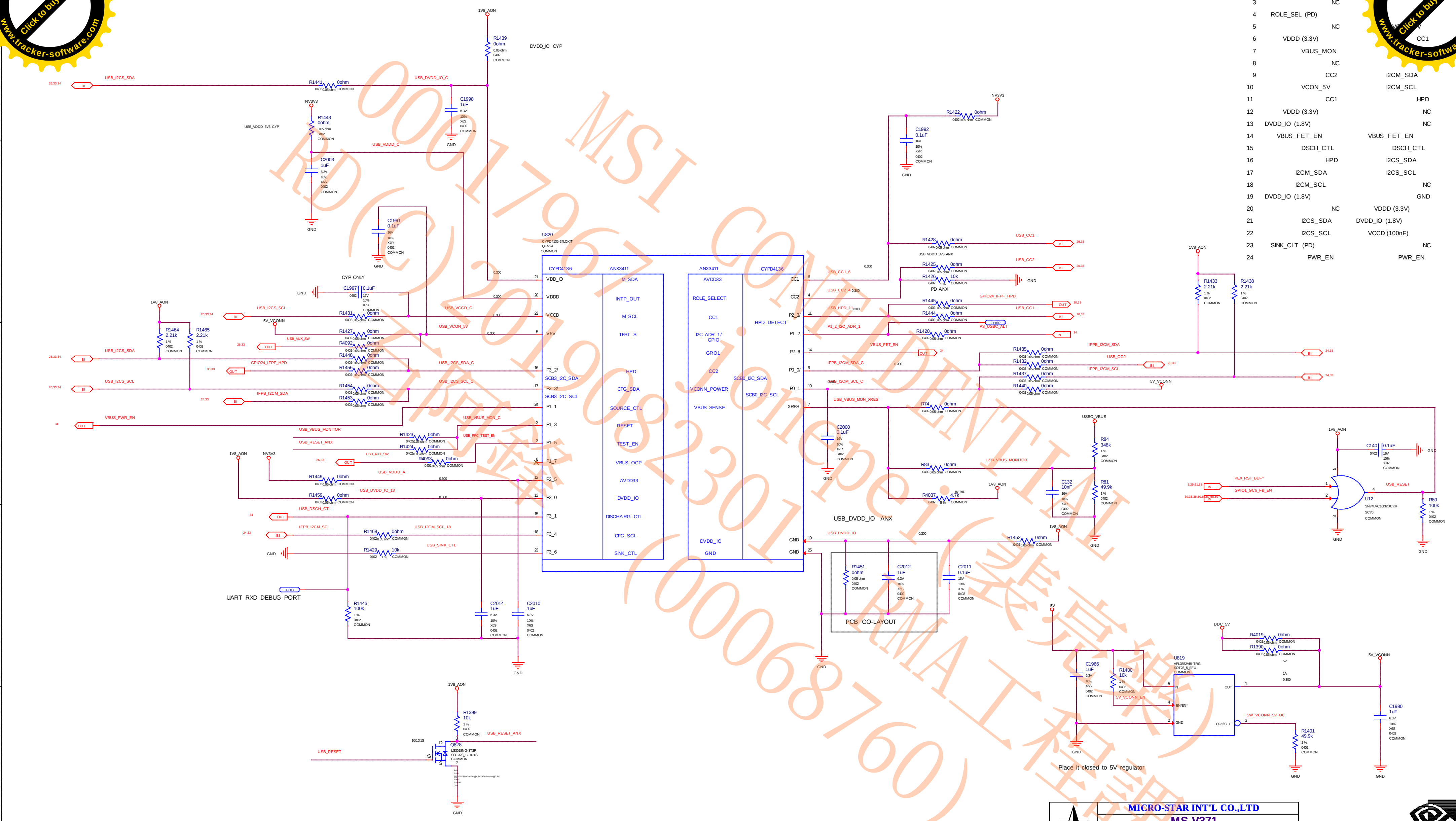
MISC: U[illegible]PPC

PIN	ANX	CYP
1	TP	TP
2	RESET	[illegible]BUS_MON
3	NC	[illegible]
4	ROLE_SEL (PD)	[illegible]
5	NC	[illegible]
6	VDDD (3.3V)	CC1
7	VBUS_MON	[illegible]
8	NC	[illegible]
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN



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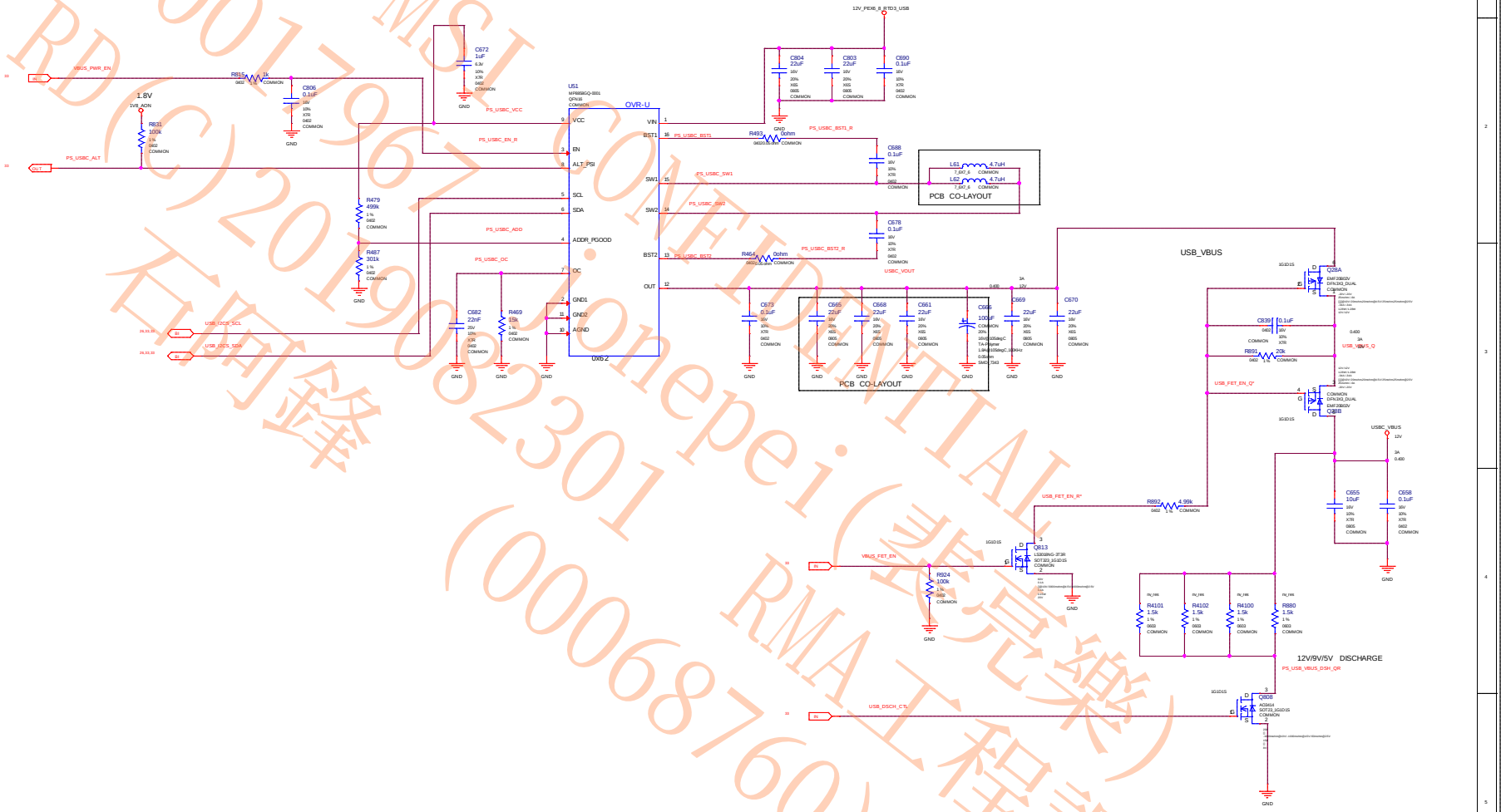

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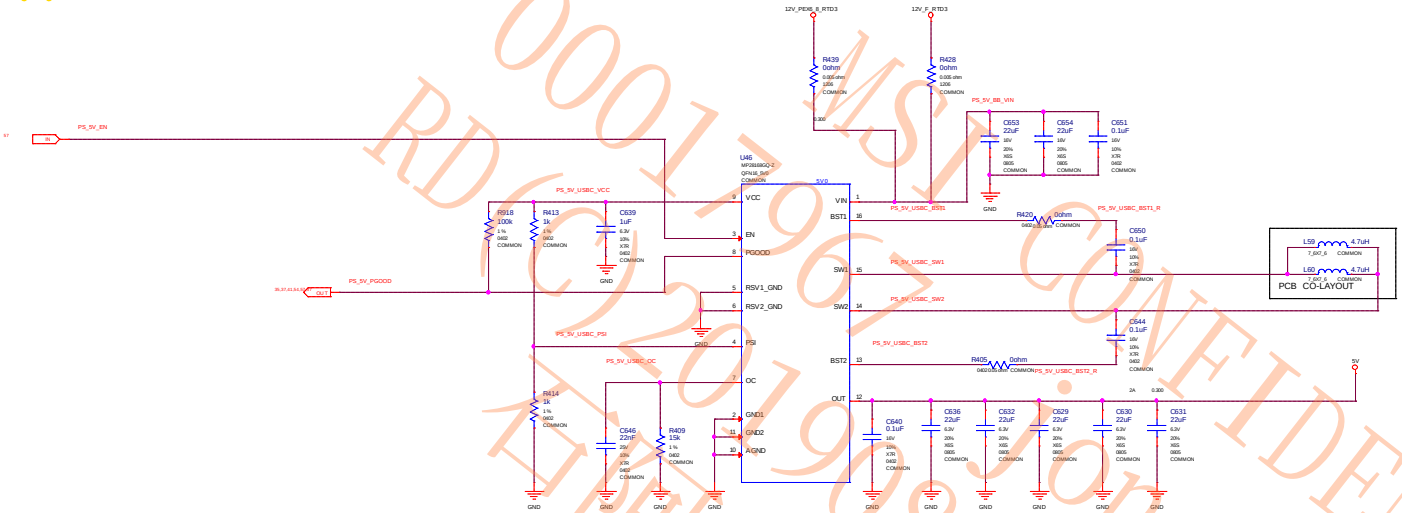
PS: 5V BACKUP



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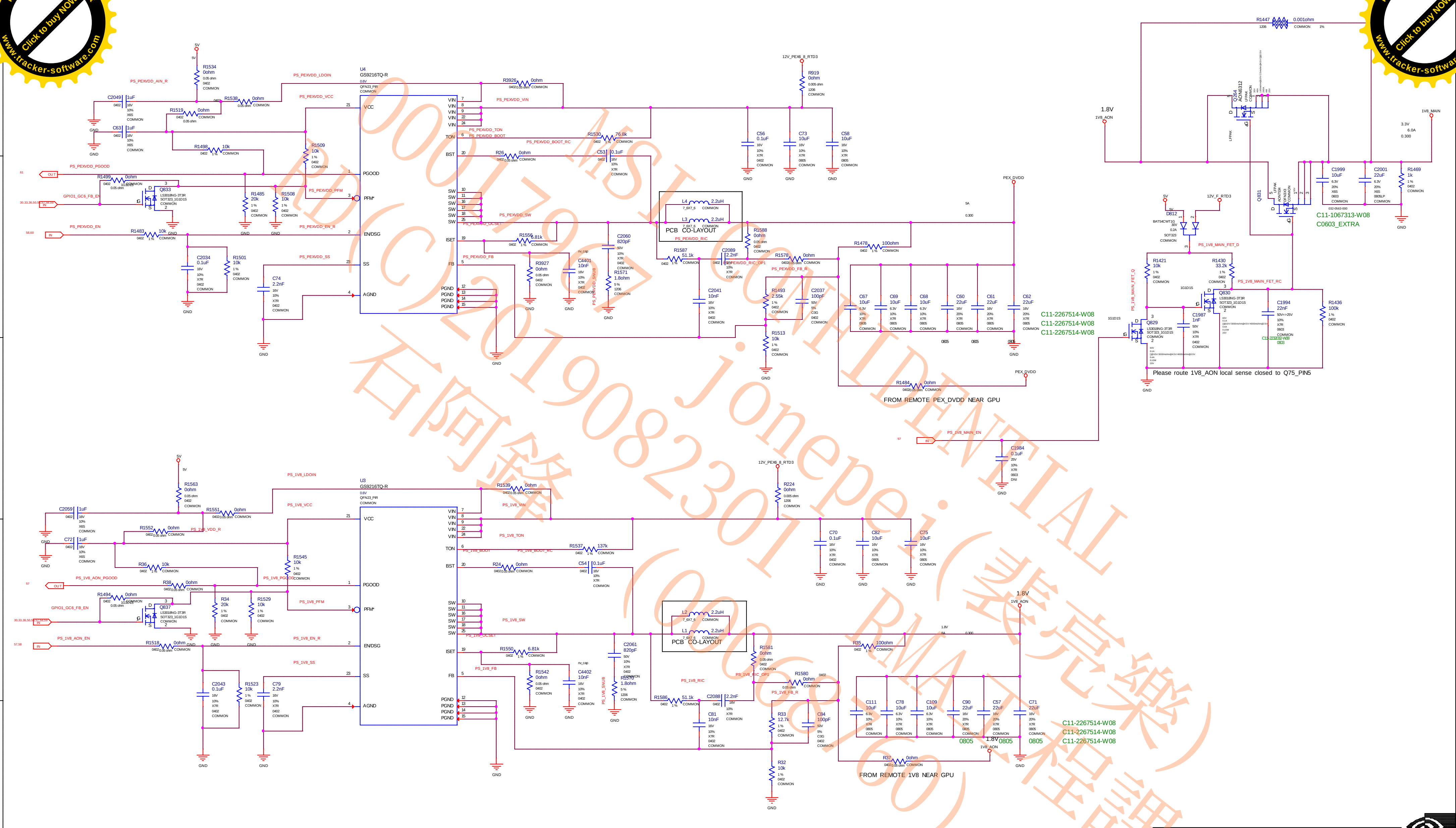
PS: PEXVDD 1V8 Rail



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Custom	1V8	2.1

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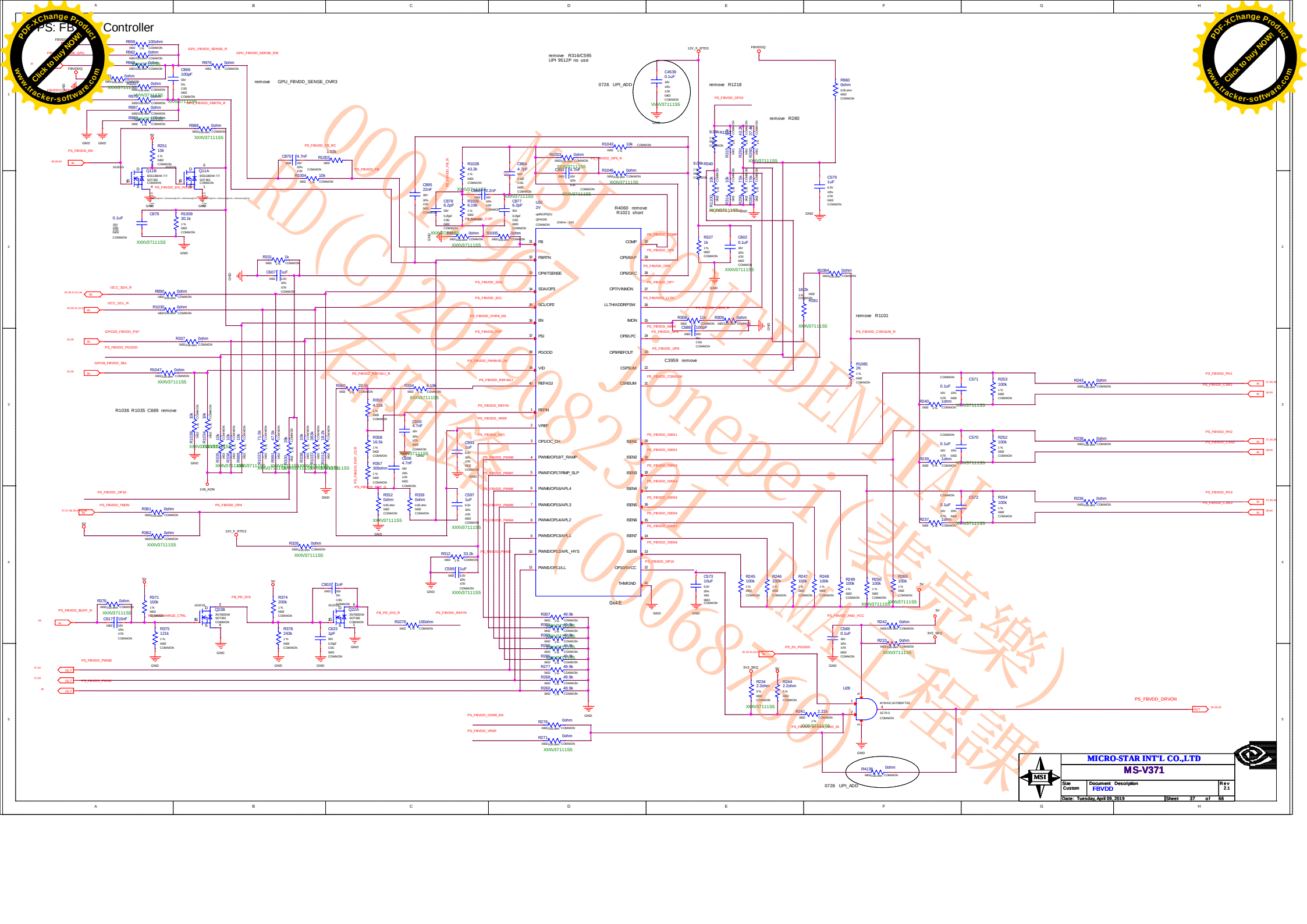
PS: FB Controller



PS: PWM Controller OVR3

remove FBVDDQ

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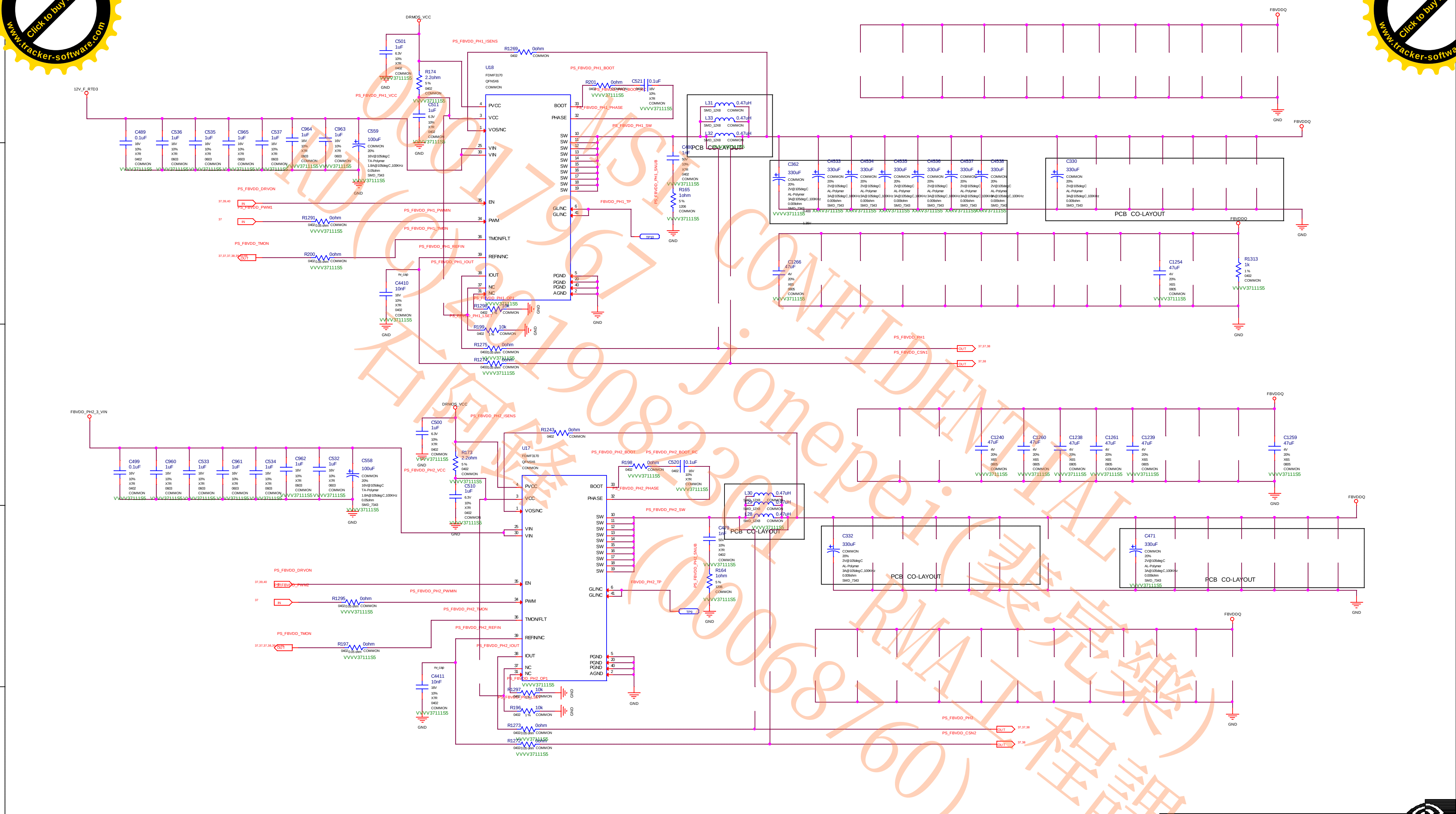
PS: FBVDD PH1, 2



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Custom	FBVDD 1/2	2.1

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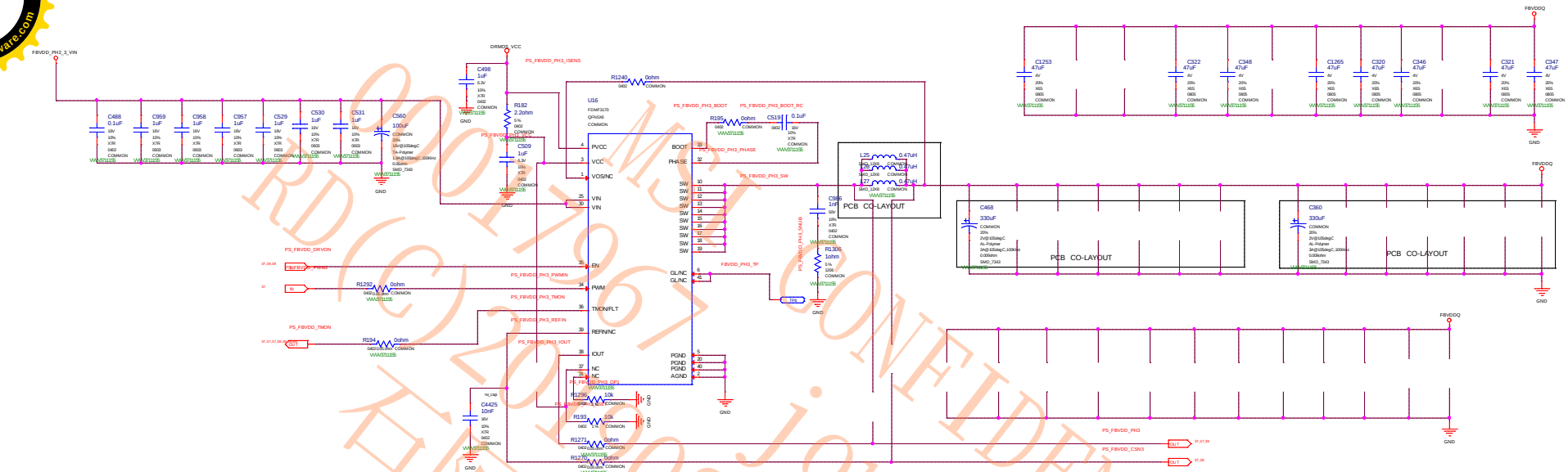
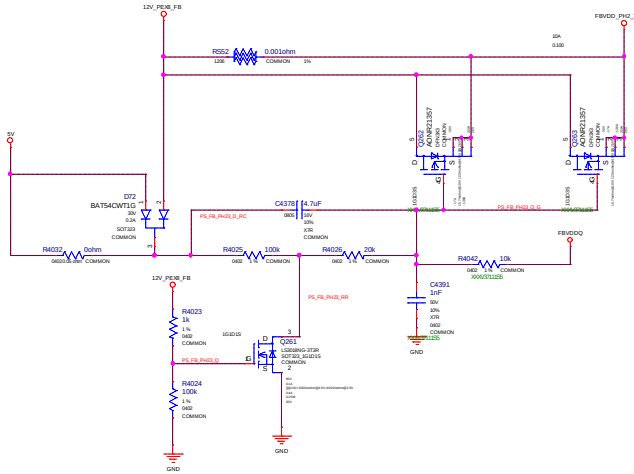
PS: FB[illegible]_PH3





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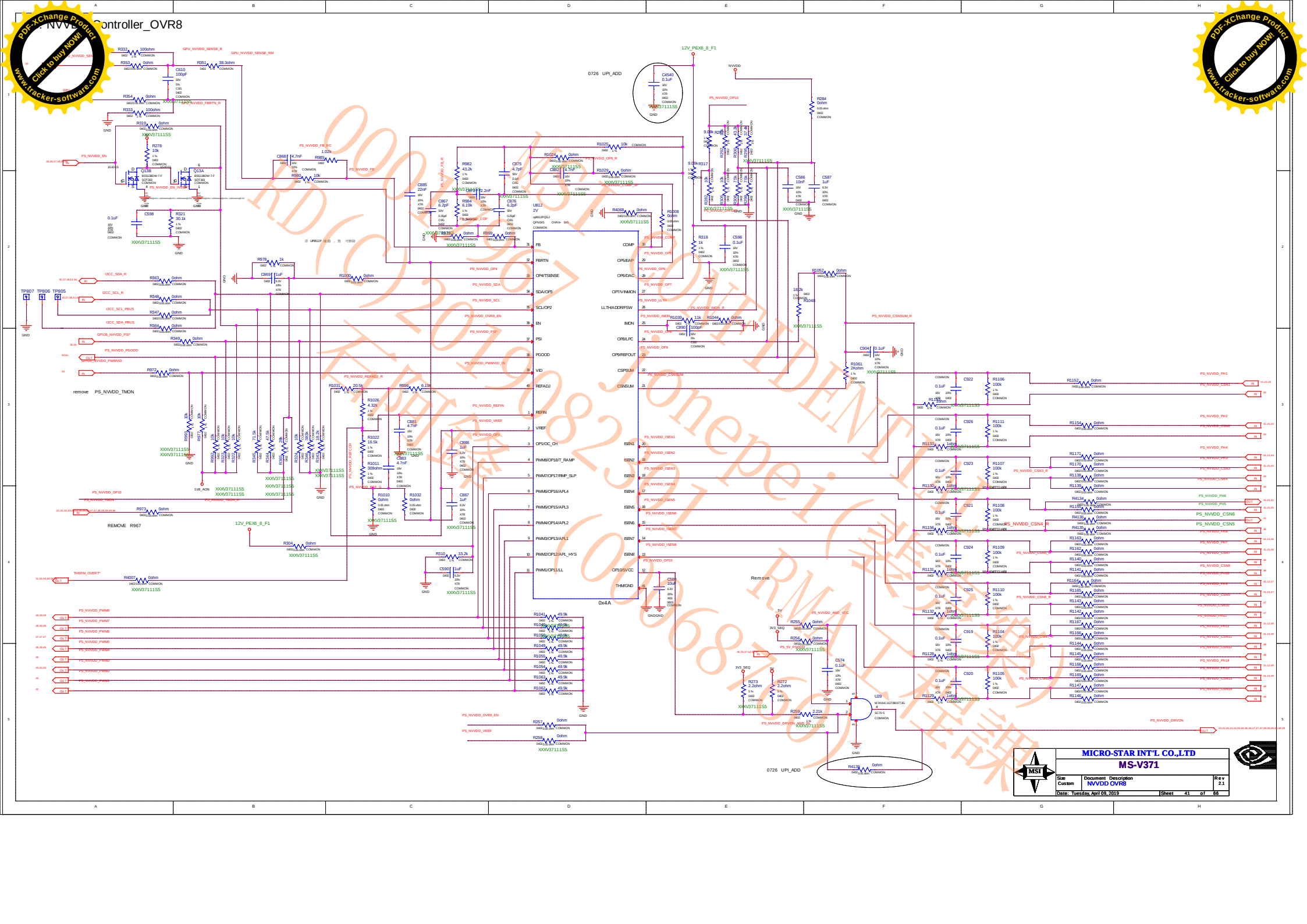
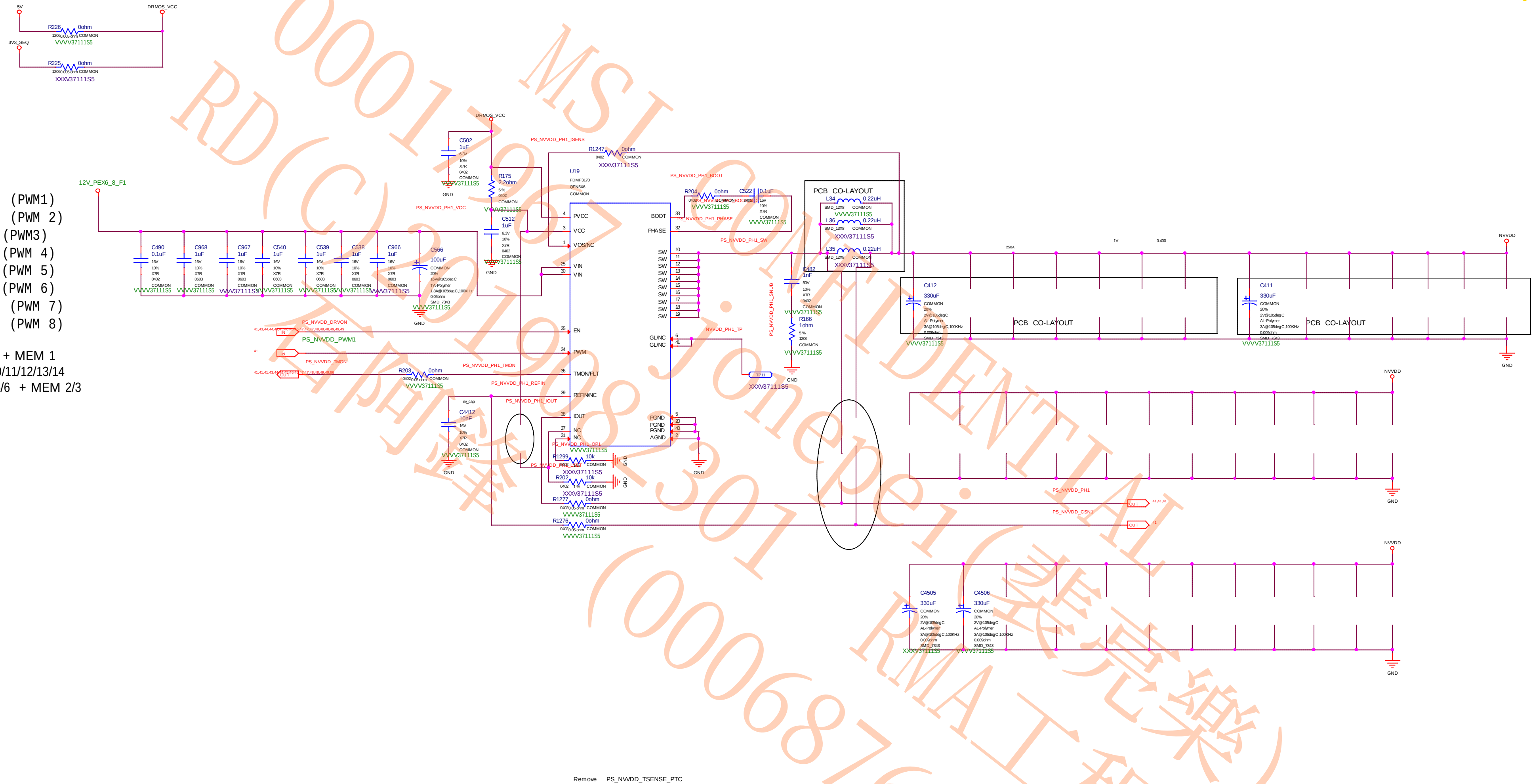
NVVDD_Controller_OVR8



S: NVVDD Phase 1



1 F1 (PWM1)
2 F2 (PWM 2)
3/4 F2 (PWM3)
5/6 F2 (PWM 4)
7/8 12V_F (PWM 5)
9/10 F1 (PWM 6)
11/12 F1 (PWM 7)
13/14 F1 (PWM 8)

12V_F NVVDD 7/8 + MEM 1
F1 NVVDD-1/9/10/11/12/13/14
F2 NVVDD-2/3/4/5/6 + MEM 2/3

Remove PS_NVVDD_TSENSE_PTC

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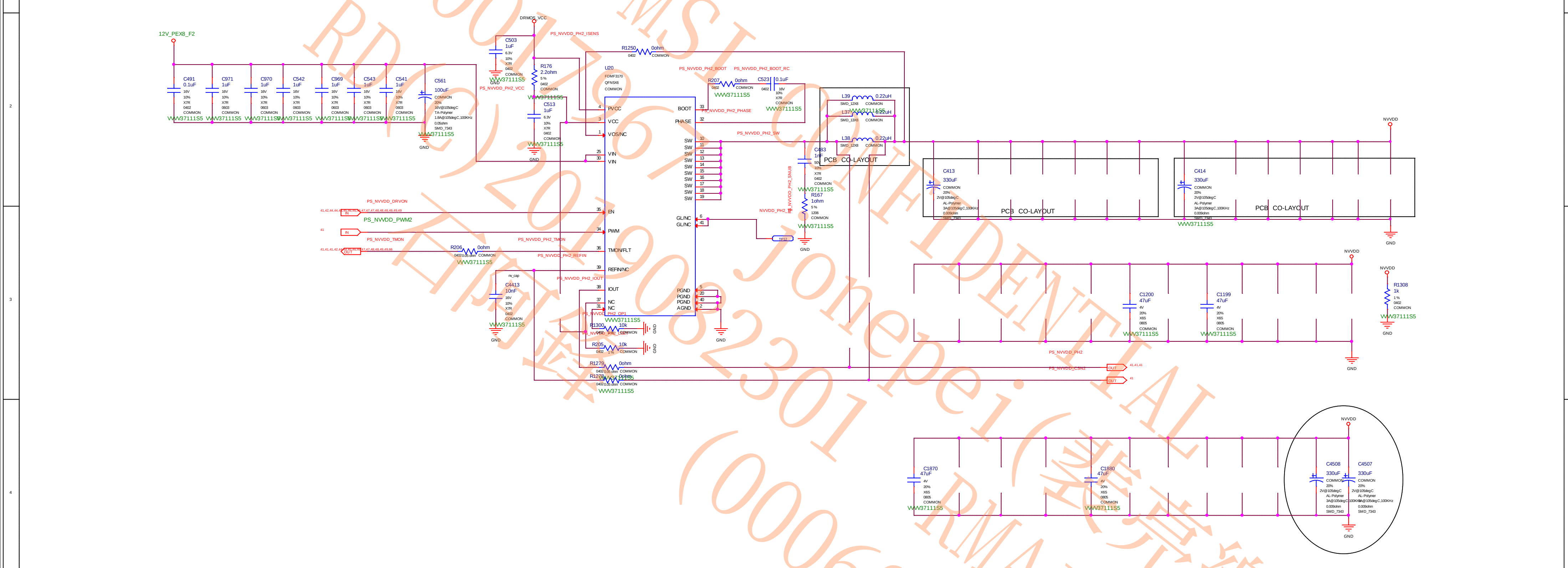
PS: NV Phase 2



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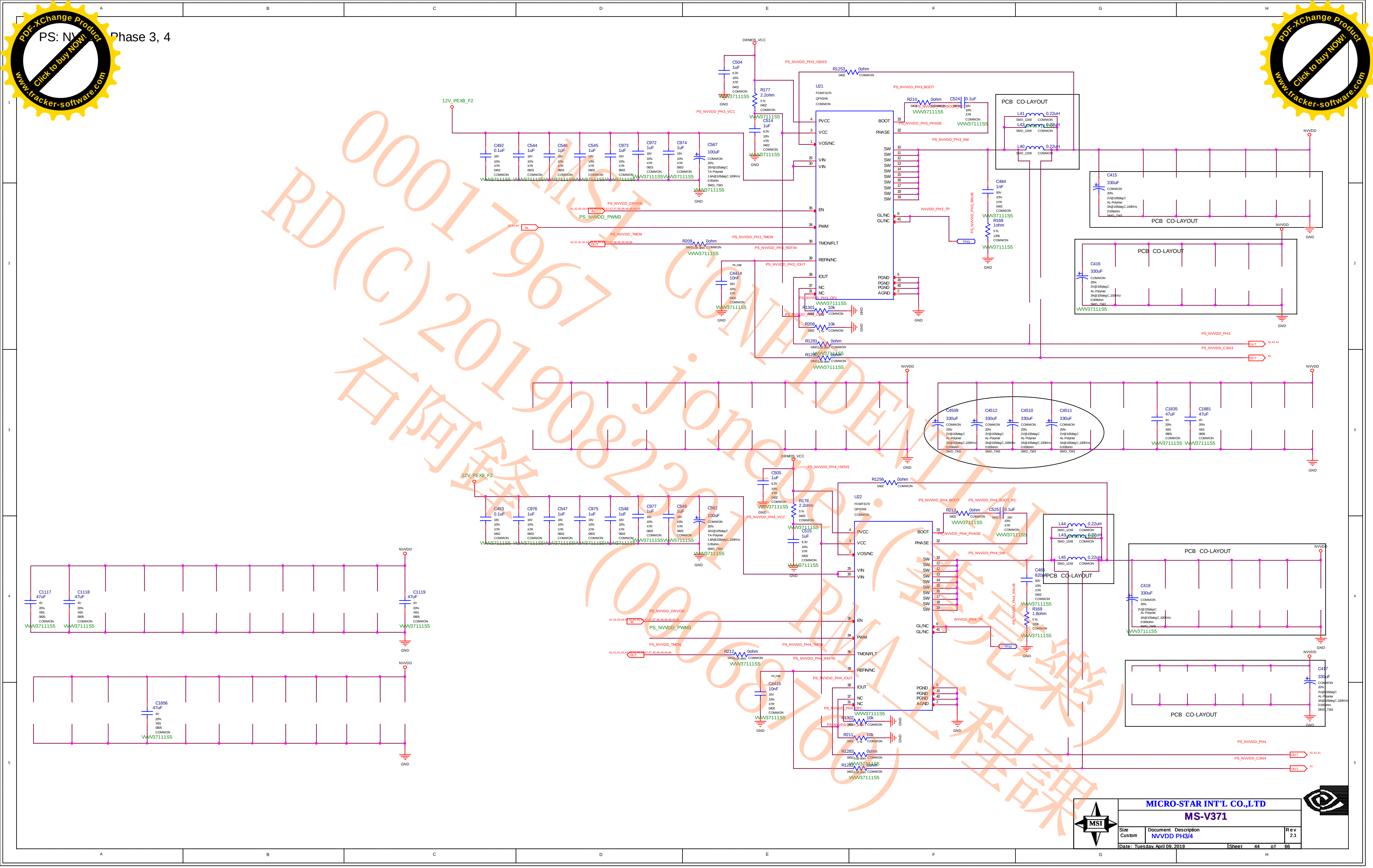
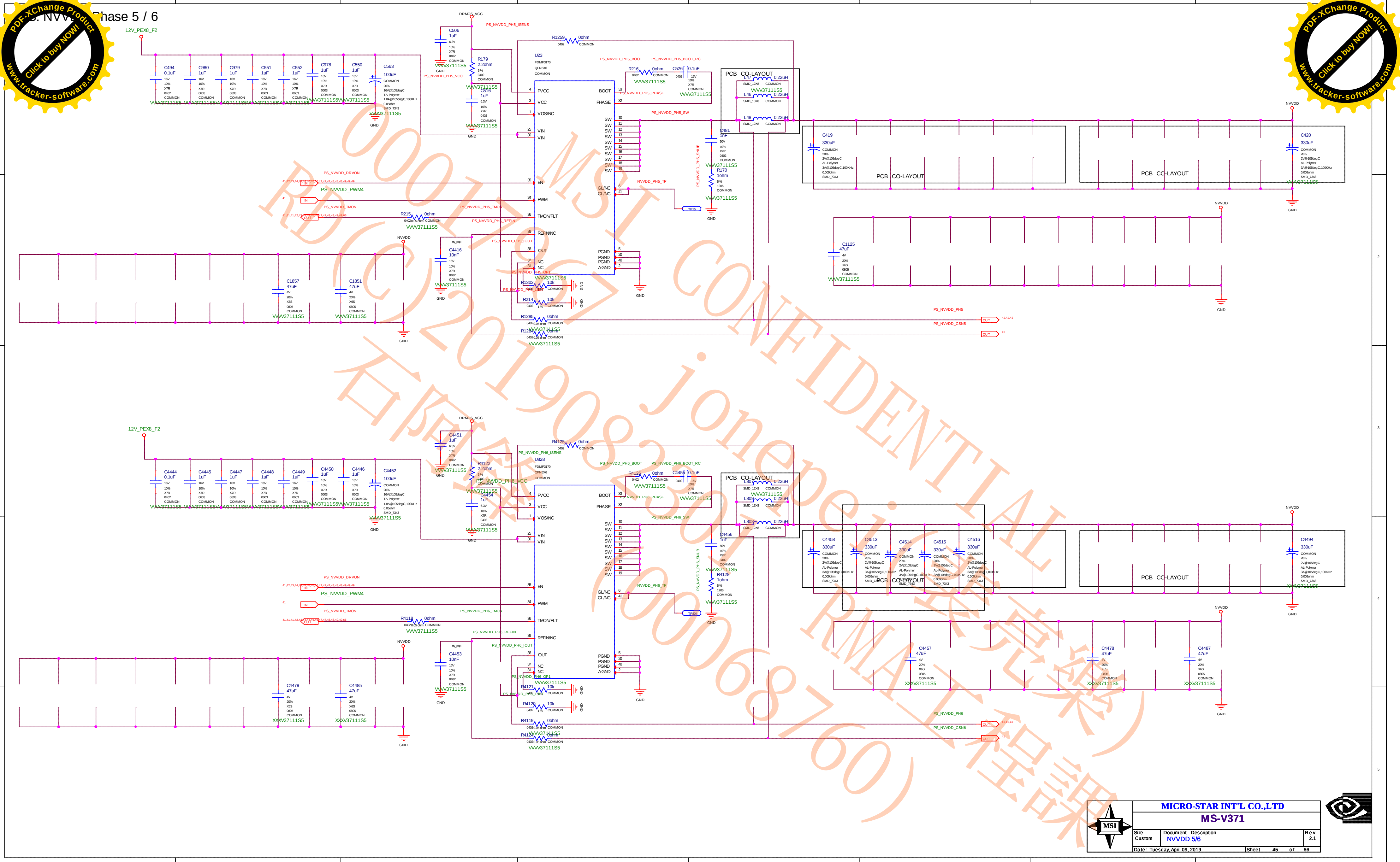


5. NVVDD Phase 5 / 6



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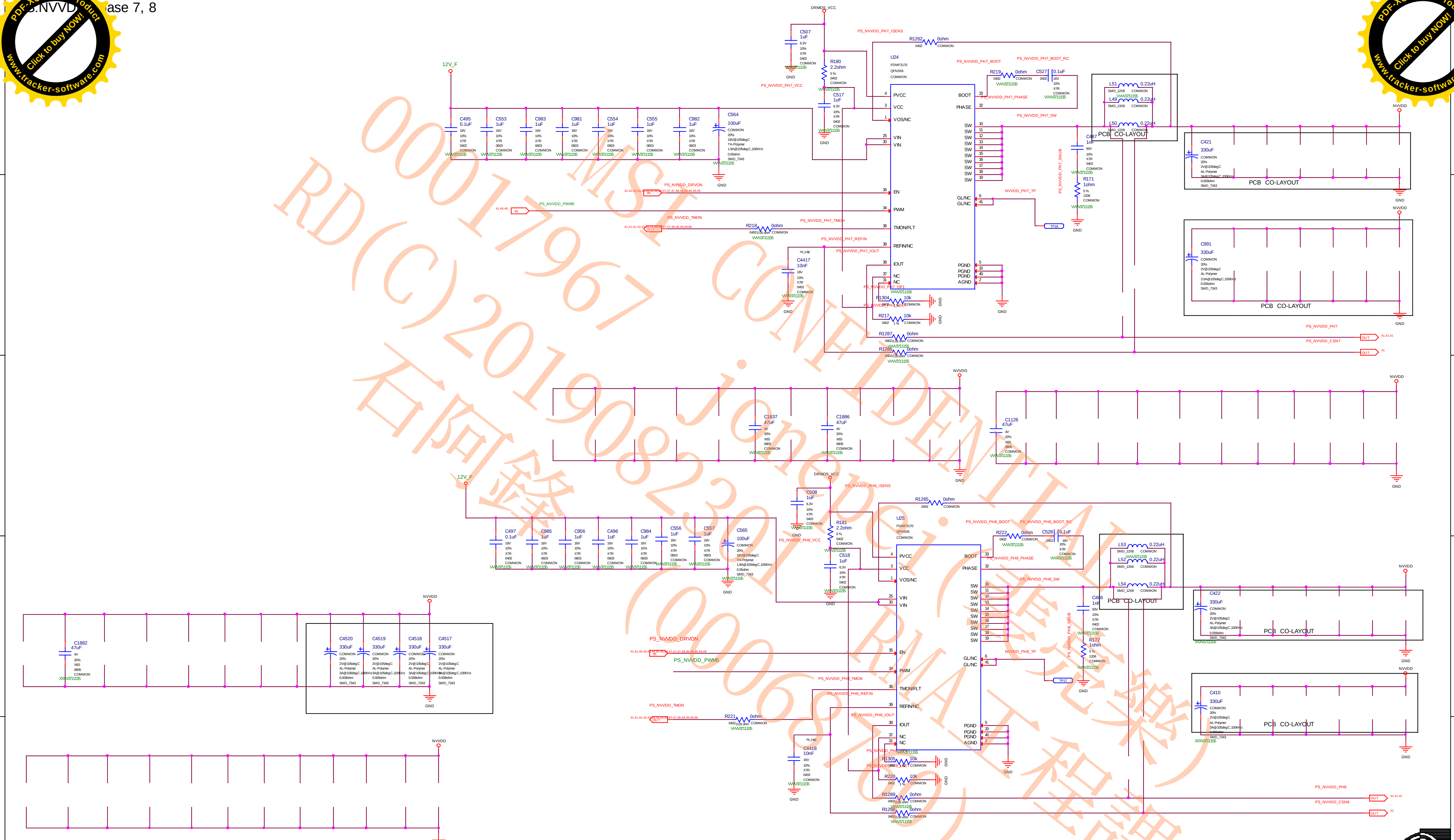
MS.NVVDD Phase 7, 8



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Custom	NVVDD 7/8	2.1

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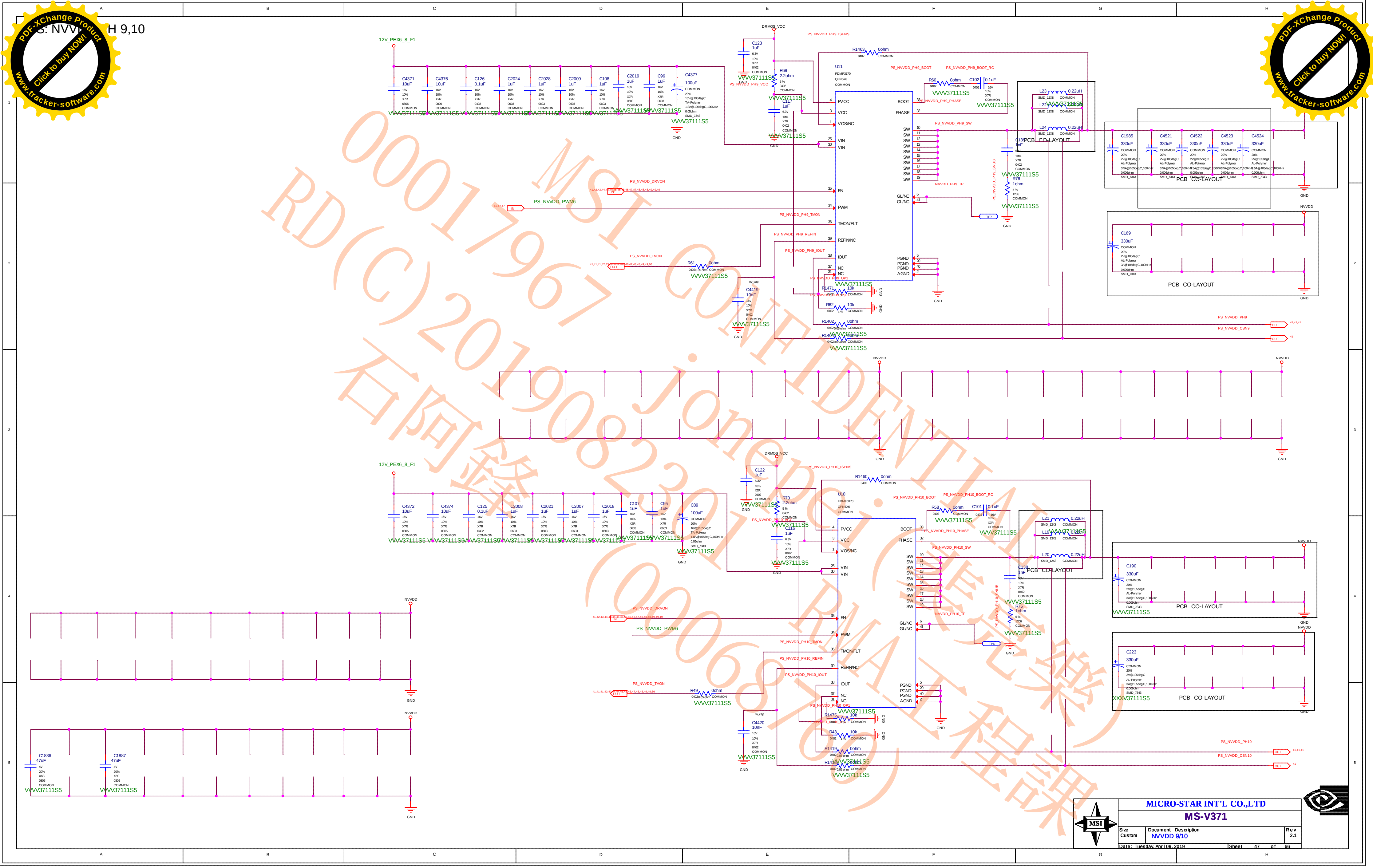
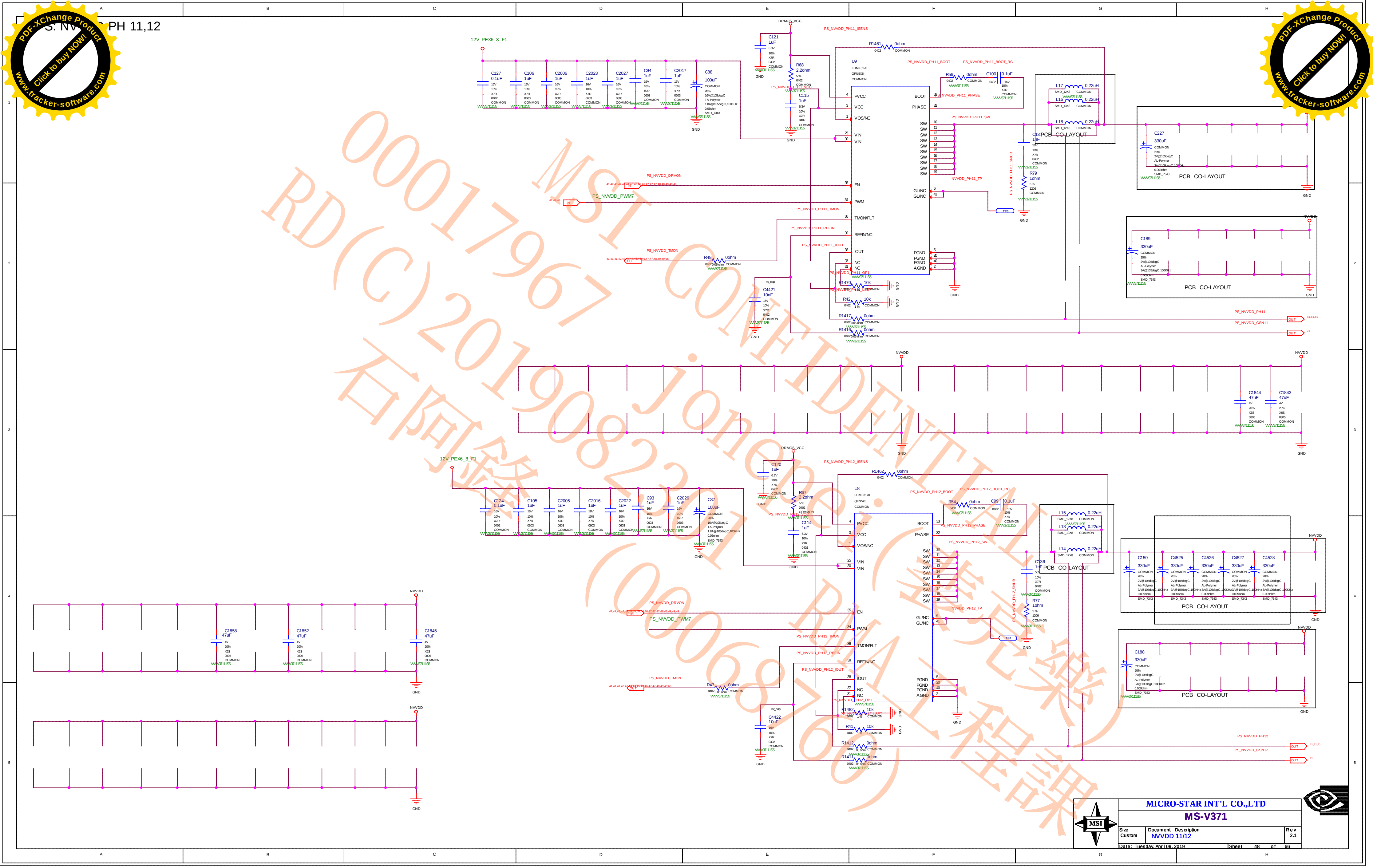
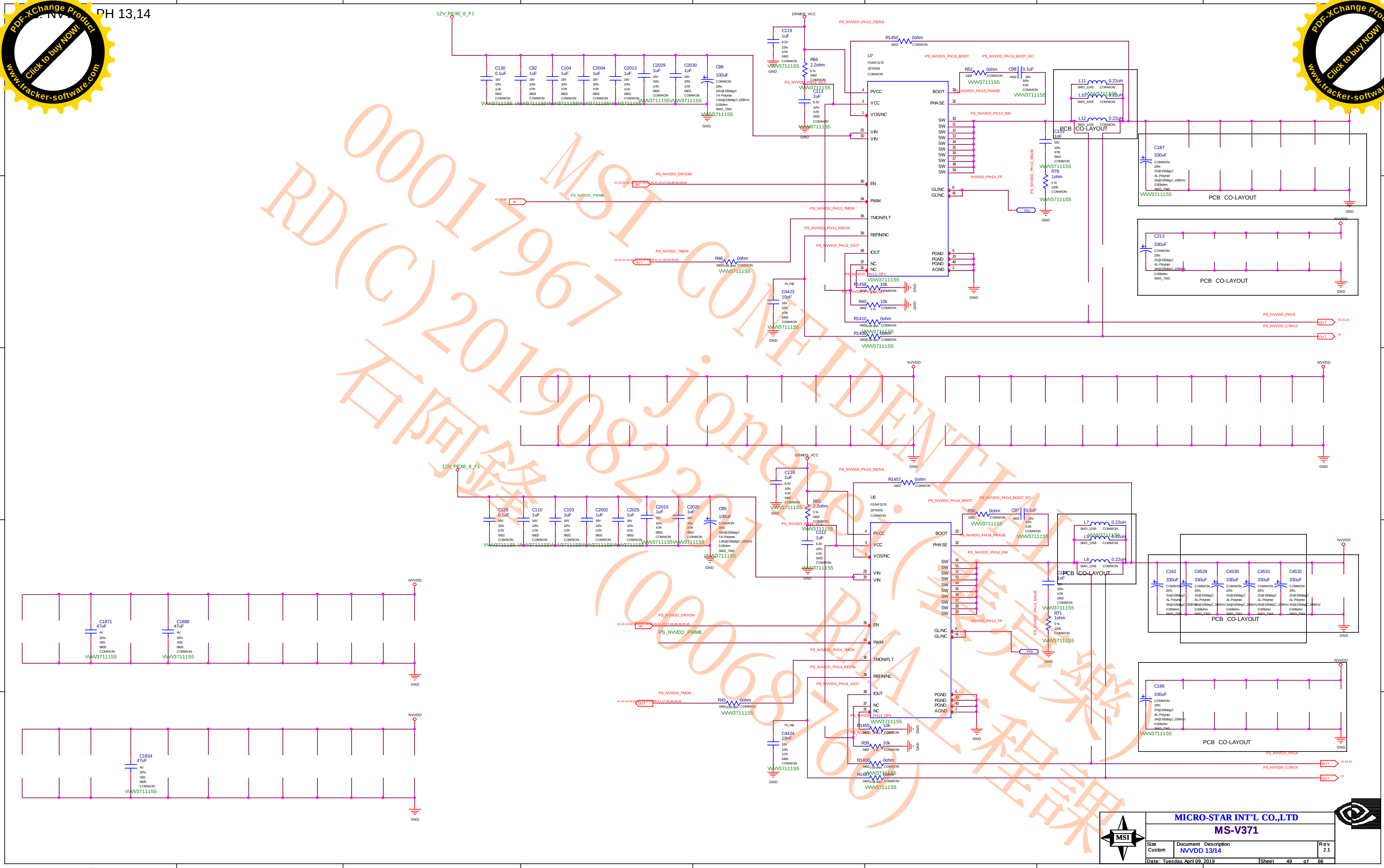




PH 13,14



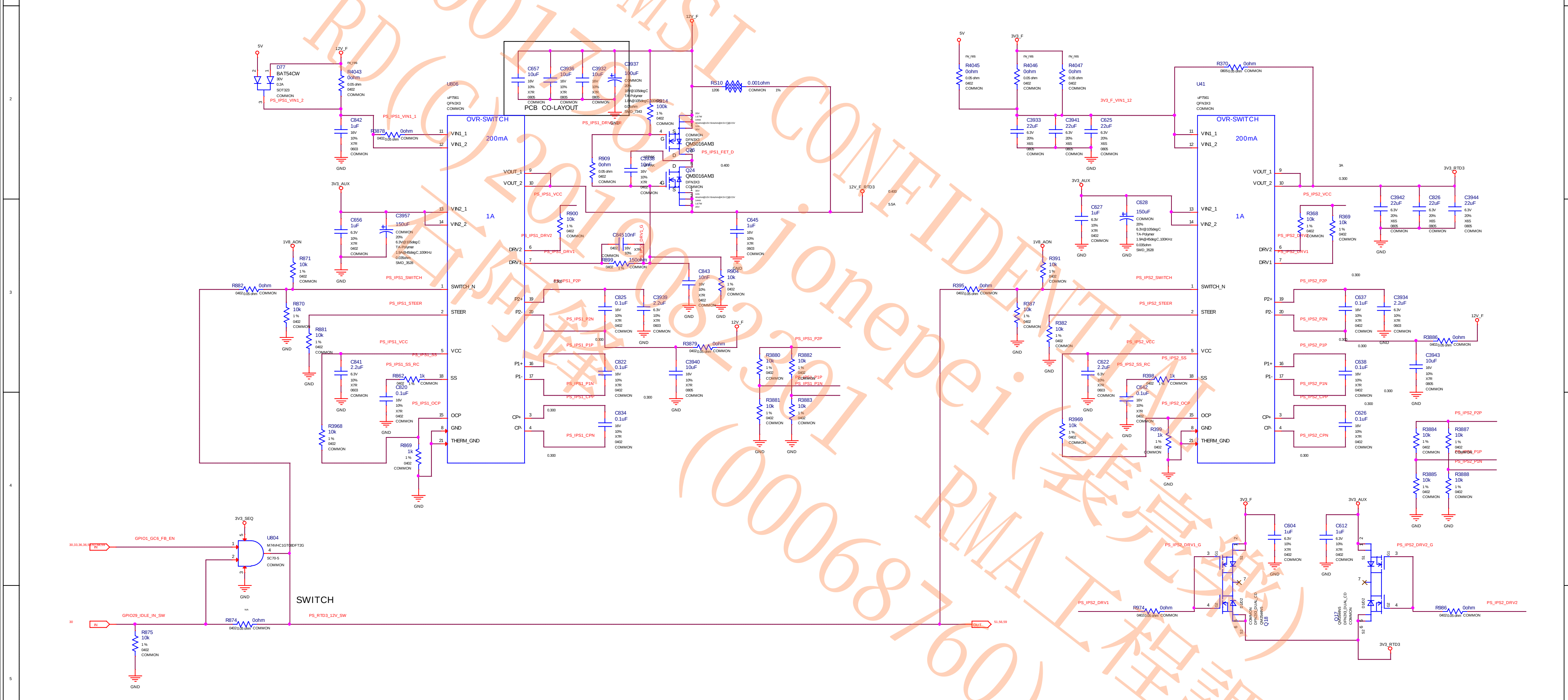
PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



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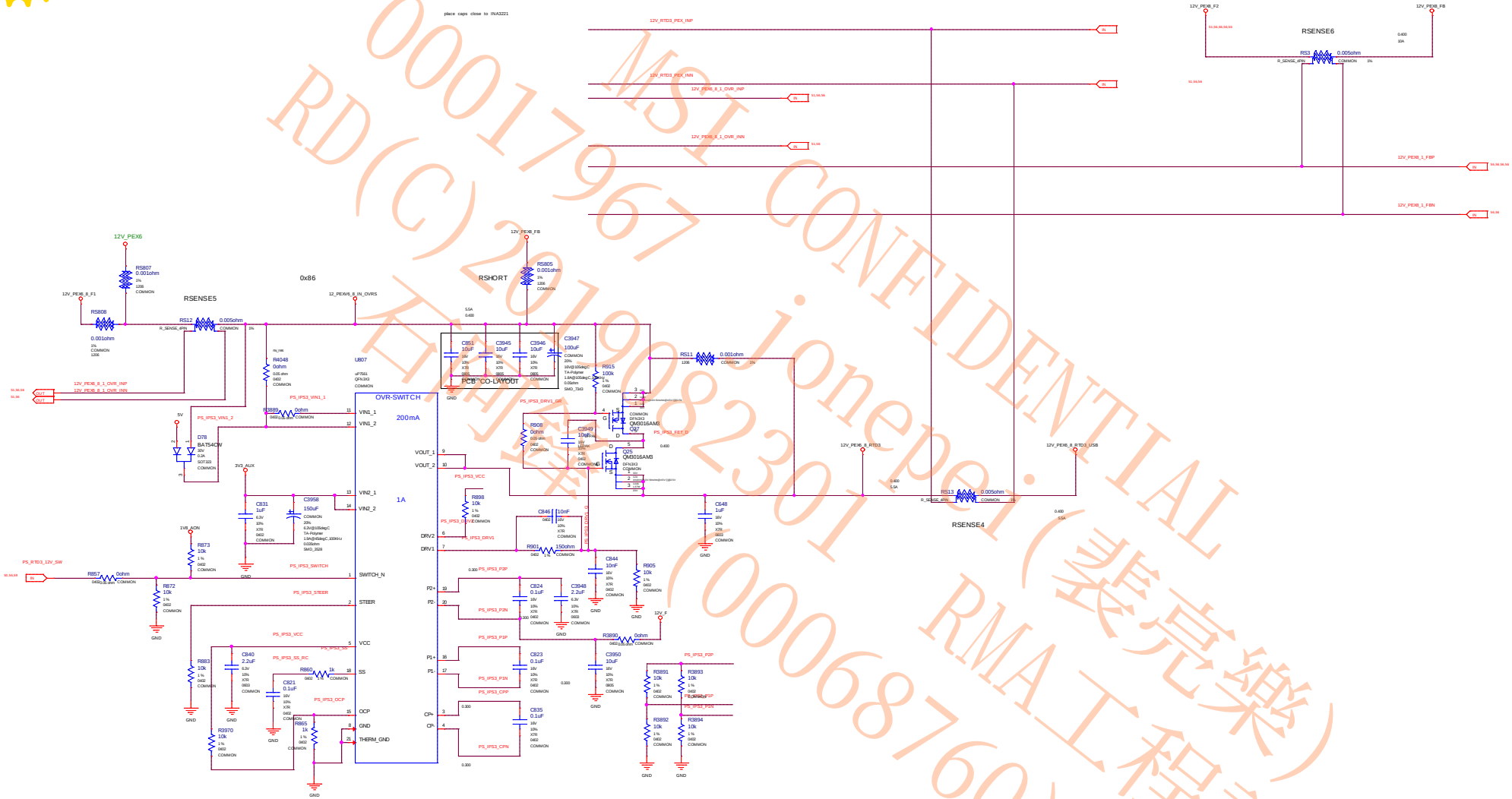

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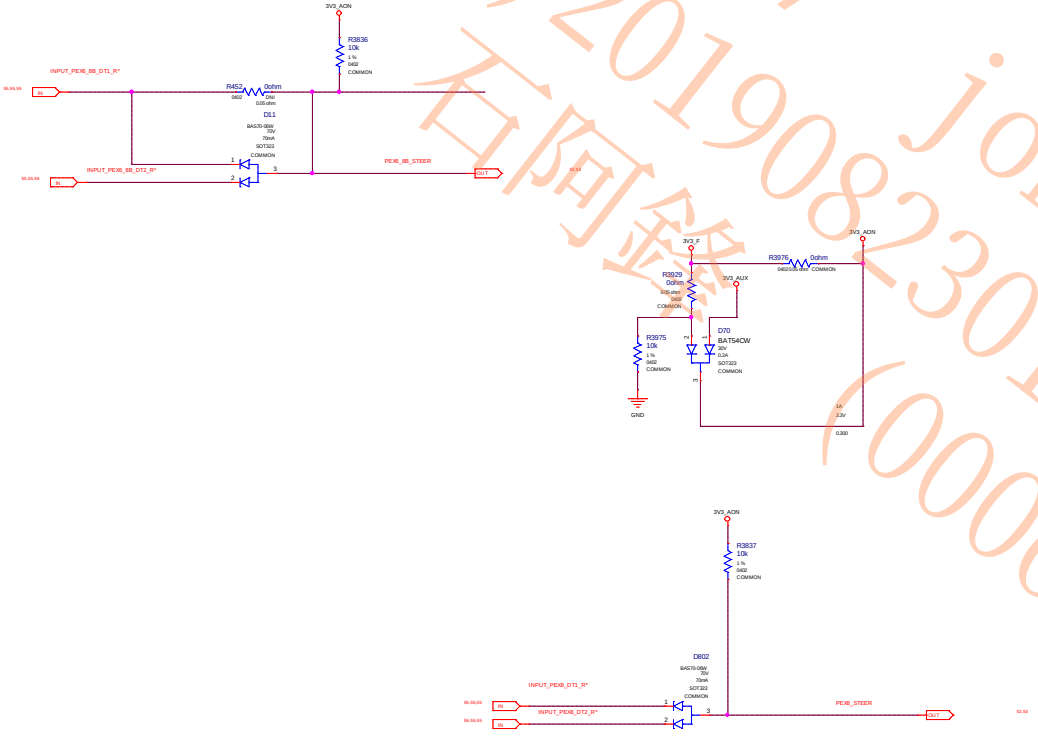
5. Input Switch Rail Balance



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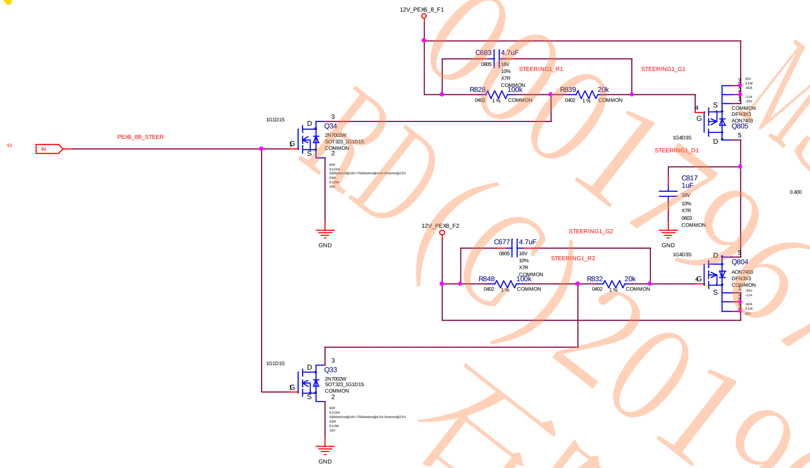
12V CURRENT STEERING (UNDER POWER BOOT):

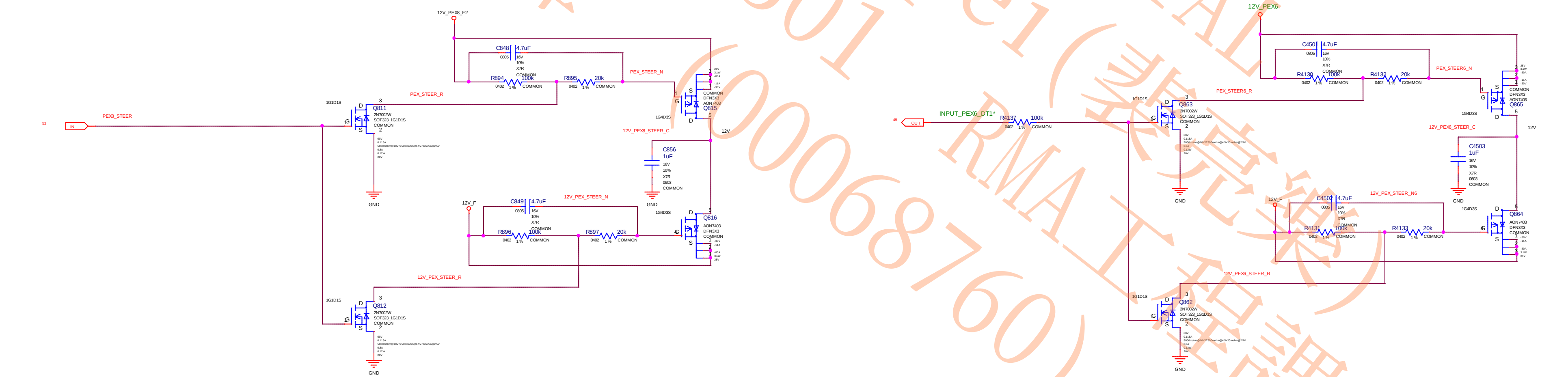
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



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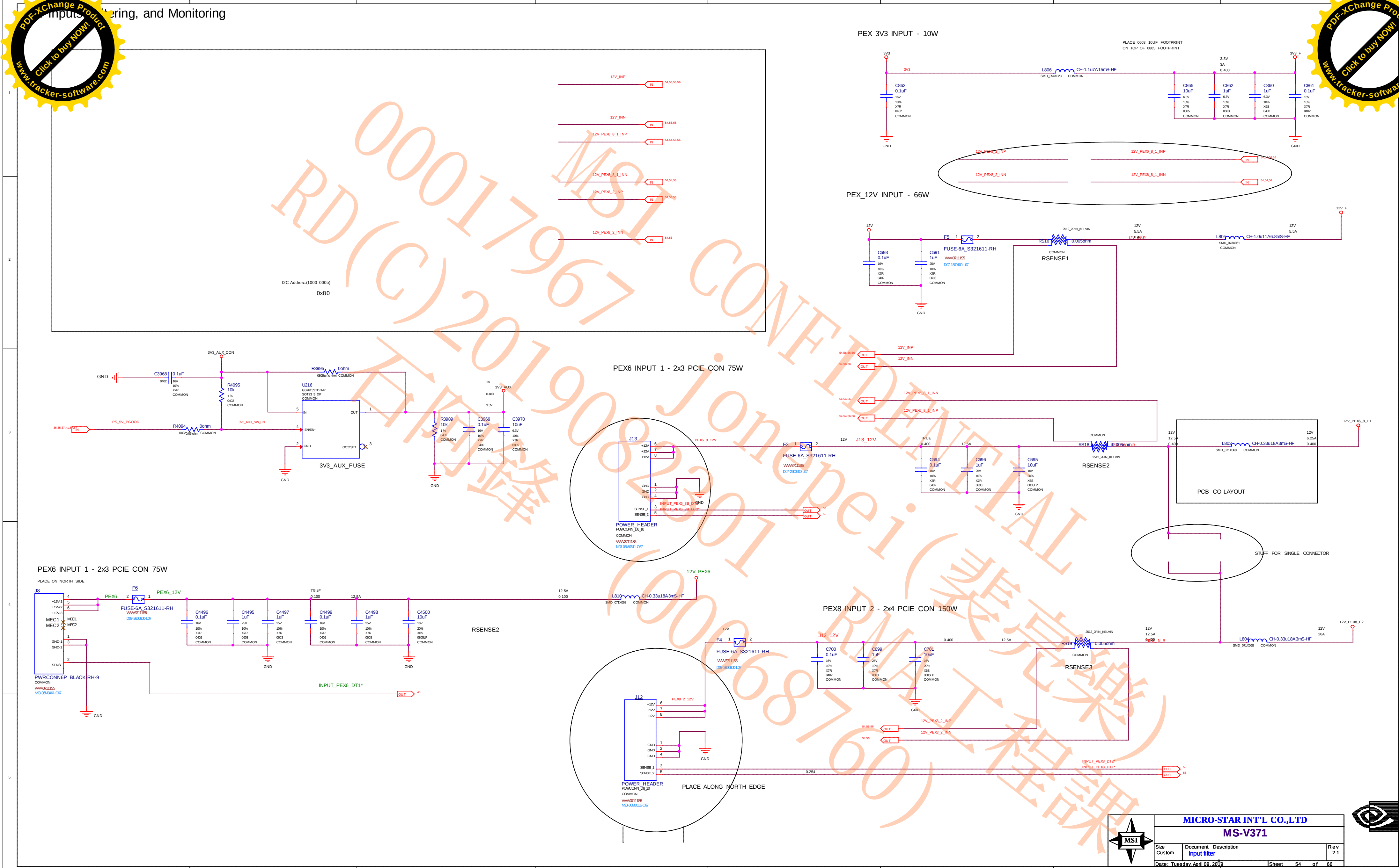
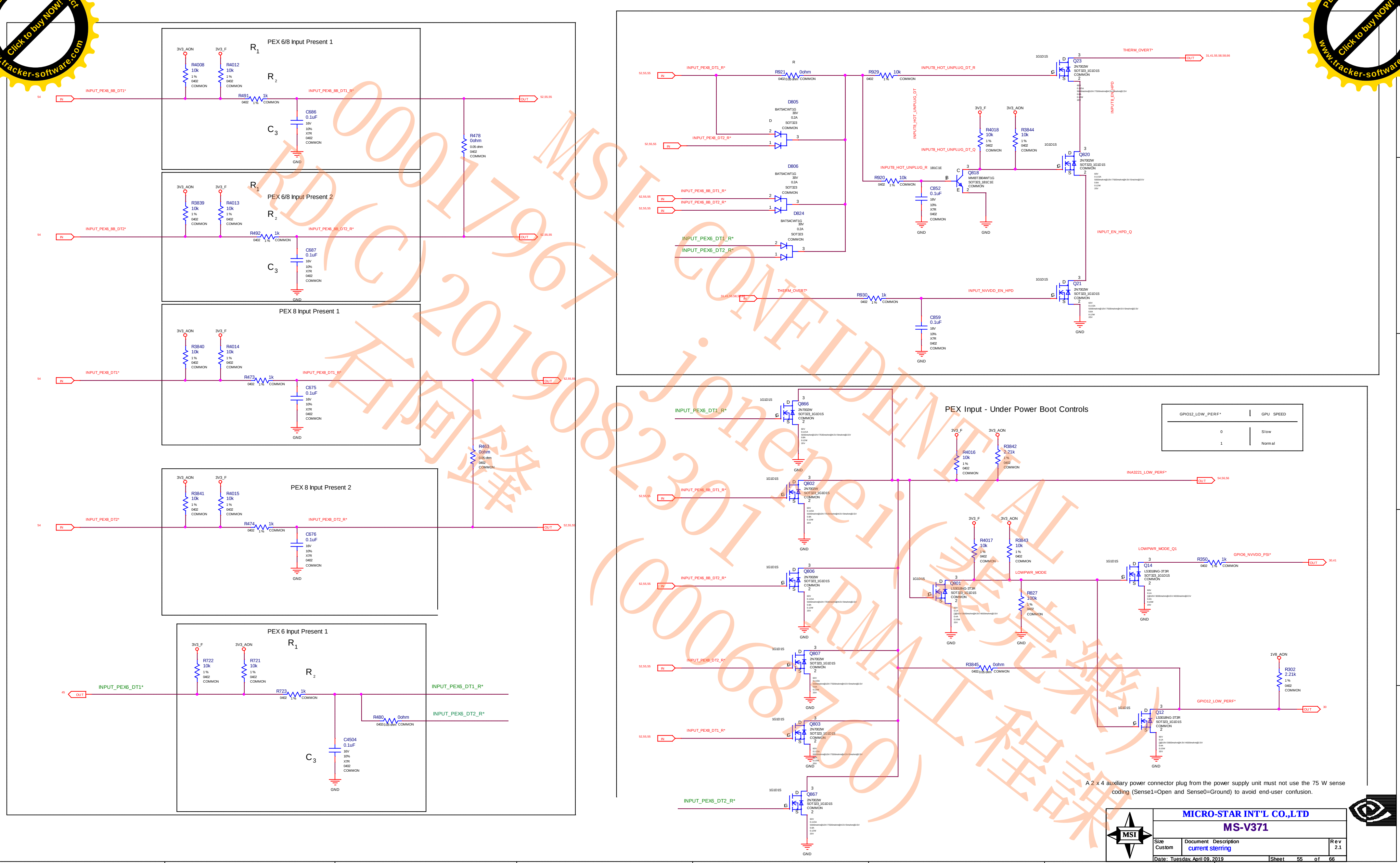
Inputs, ...ering, and Monitoring



12V C... t Steering & Hot Unplug Detect



A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

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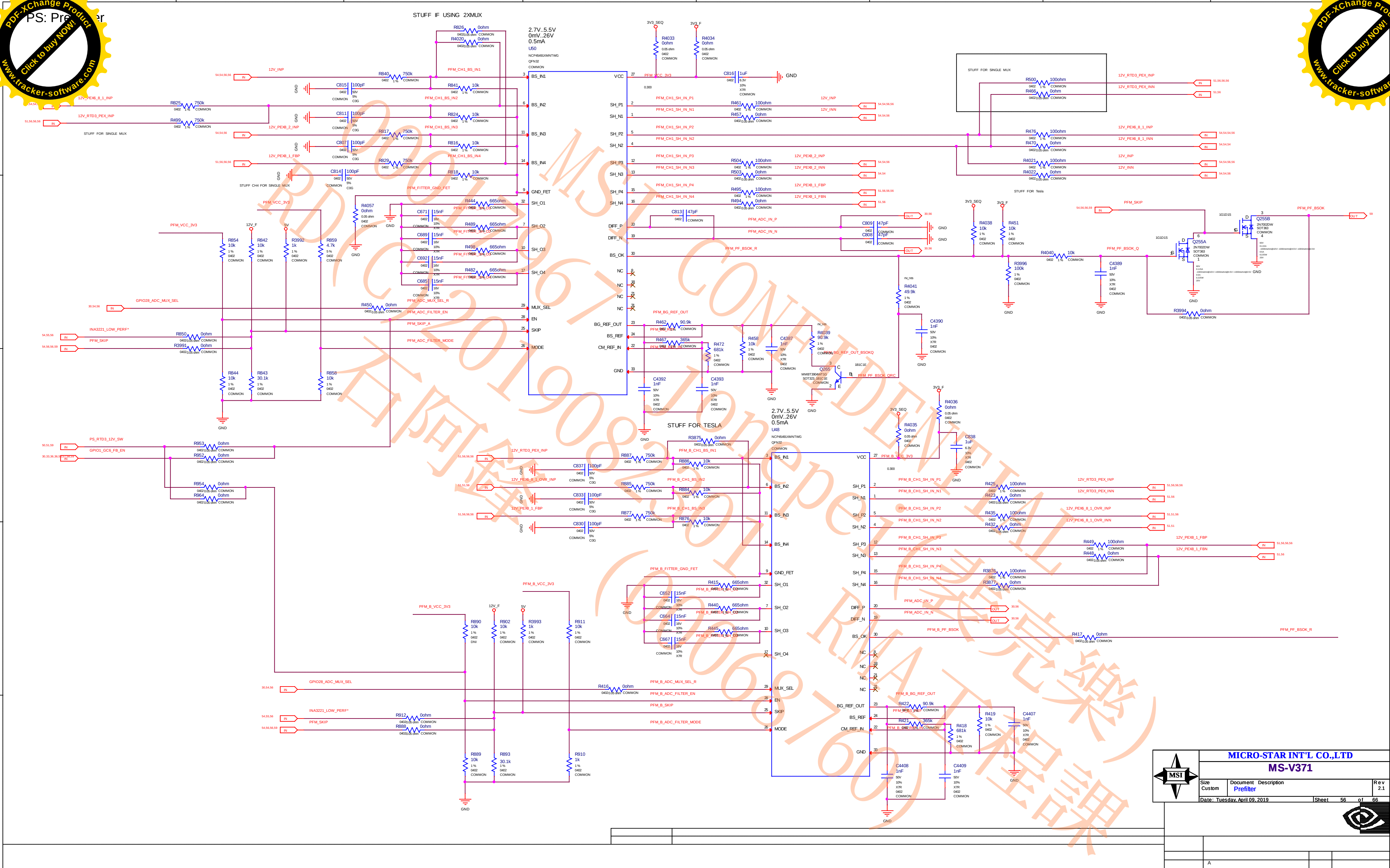
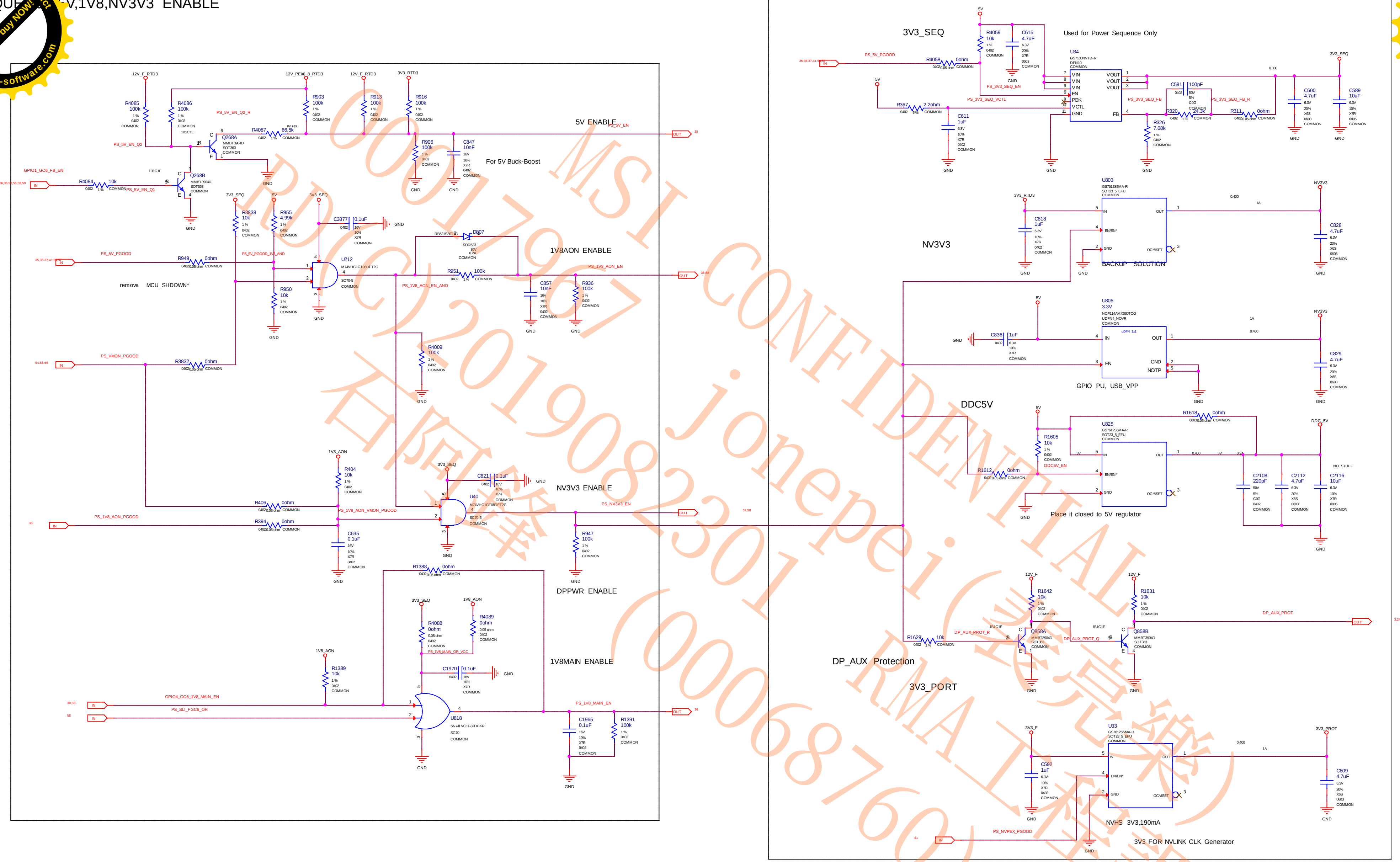


SEQUENCE: 5V,1V8,NV3V3 ENABLE



ASSEMBLY <ASSEMBLY_DESCRIPTION>
PAGE DETAIL Sequence: 5V, 1V8, NV3V3 EN

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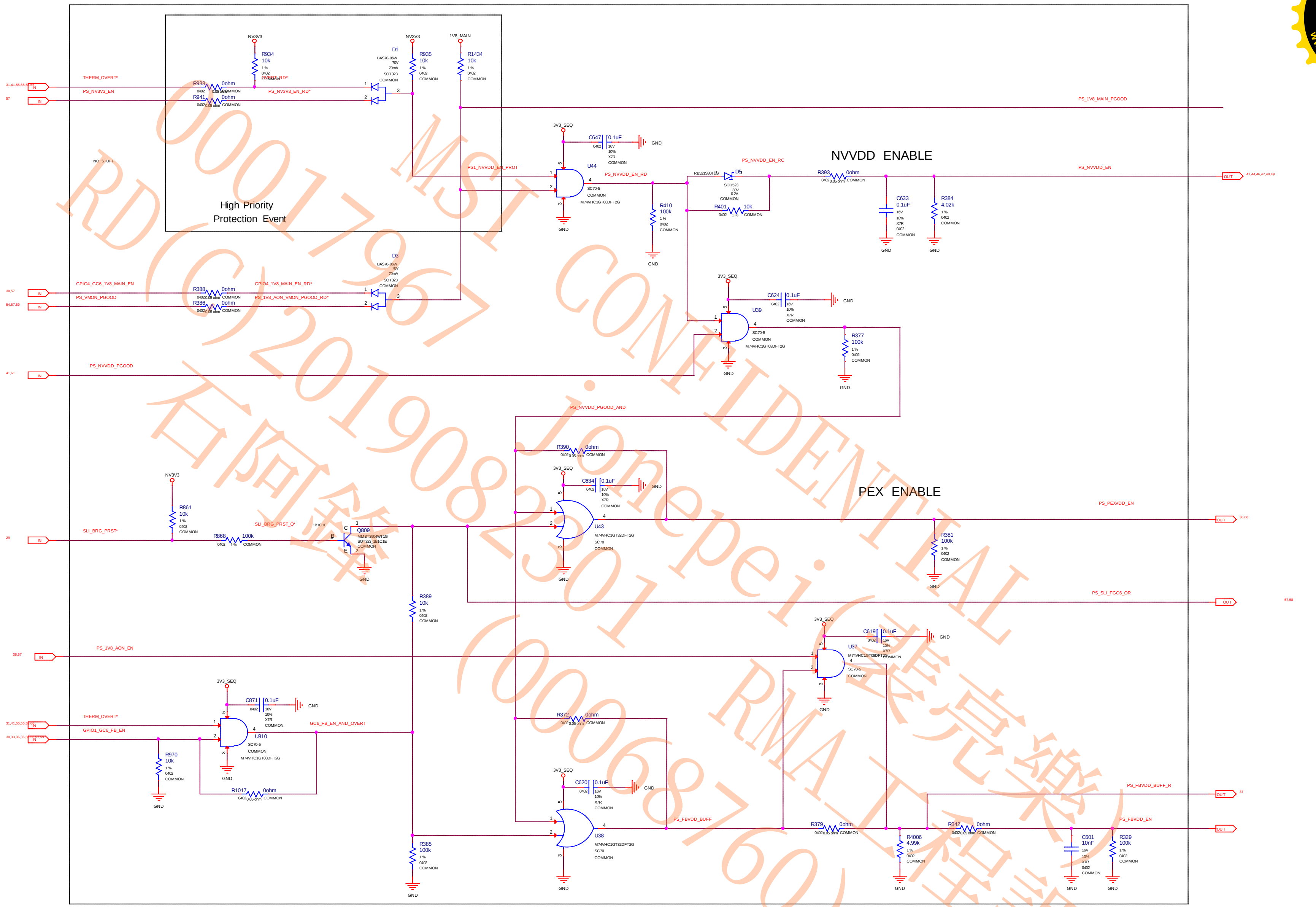
SEQUENCE:NV,PEX,FB ENABLE

remove OC_CRIT
remove MCU_SHDOWN*



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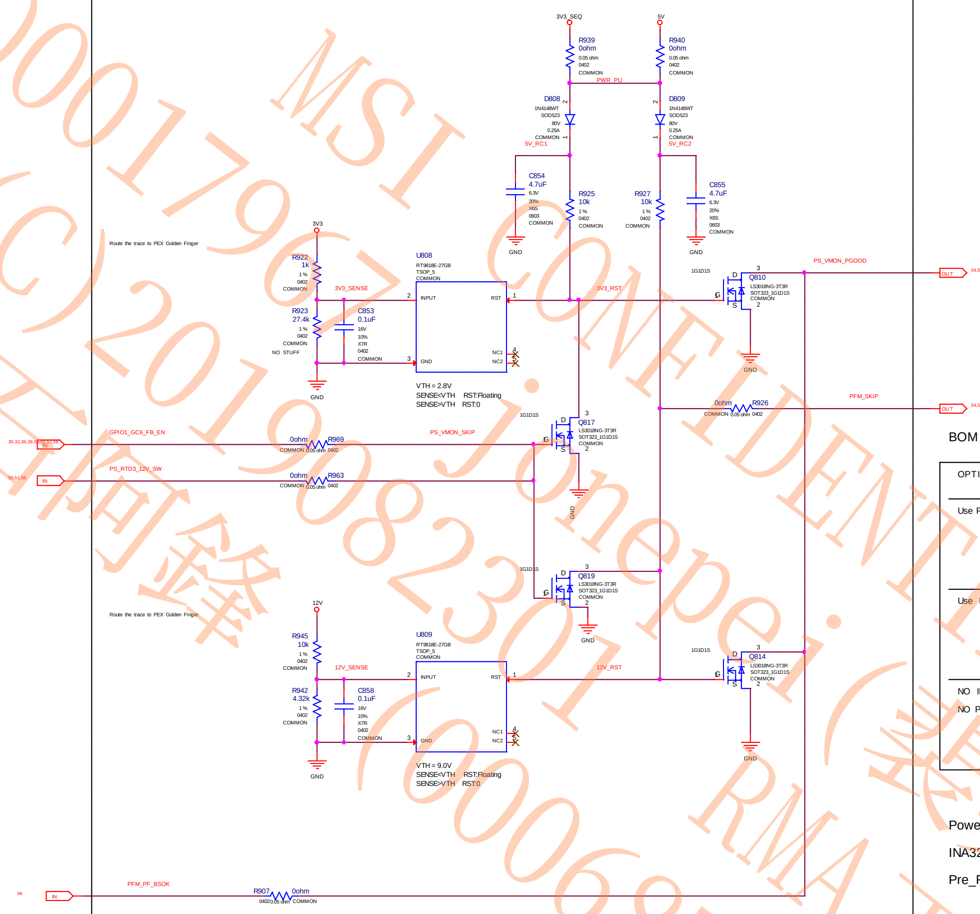
SEQU… PCIE Voltage Monitor

PCIE Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

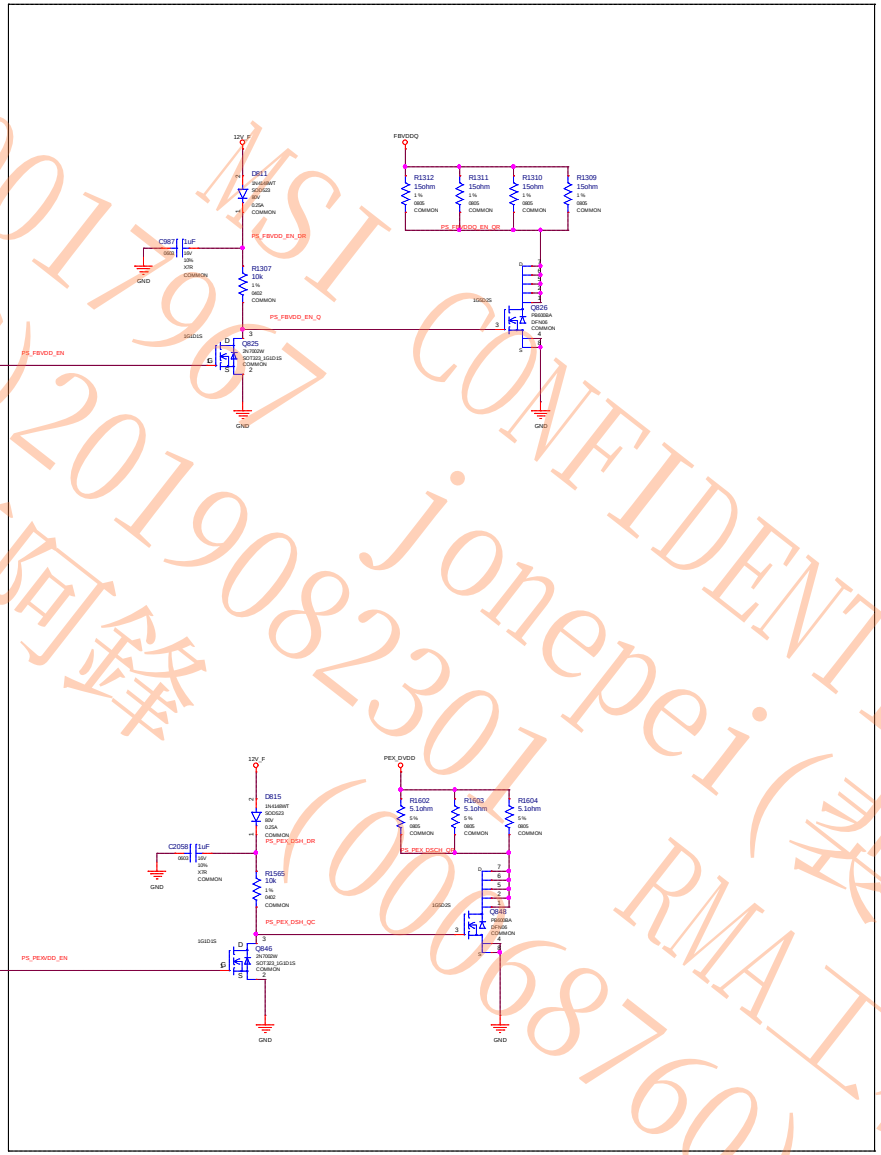
Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX

and All Input 12Vs

SEQUENCE:Discharge



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Size: Custom	Document Description: SEQUENCE:Discharge	Rev: 2.1
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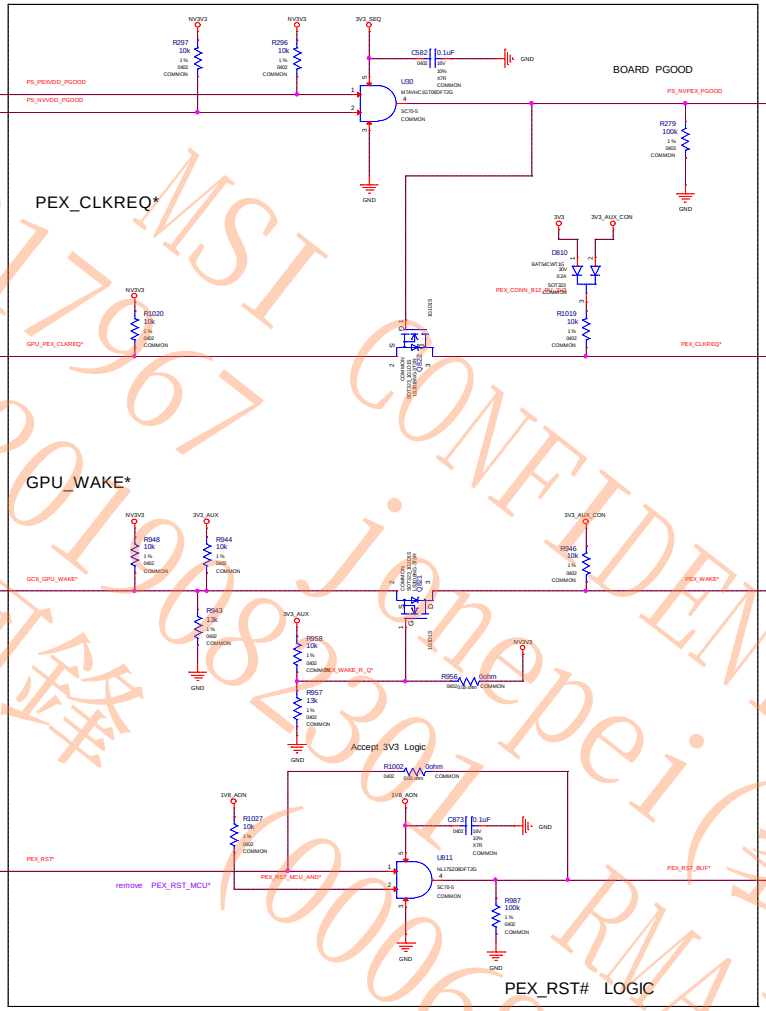
SEQUENCE-MISC



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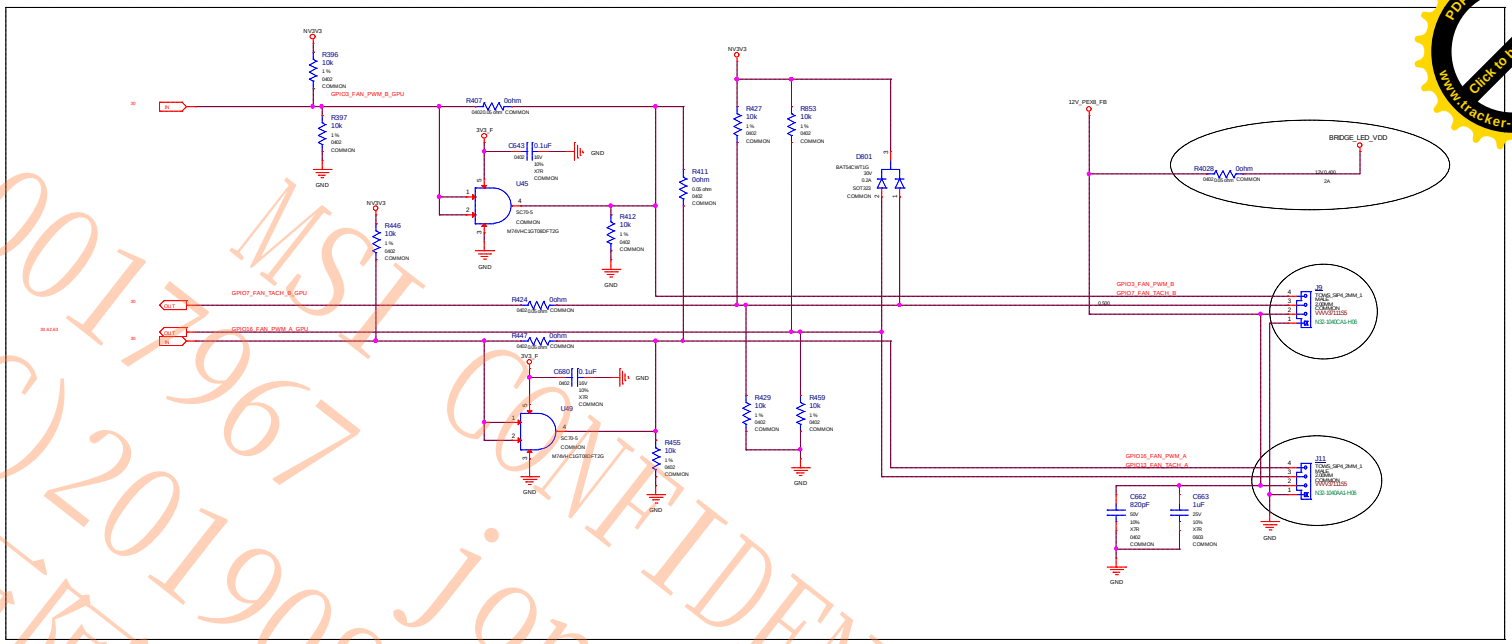

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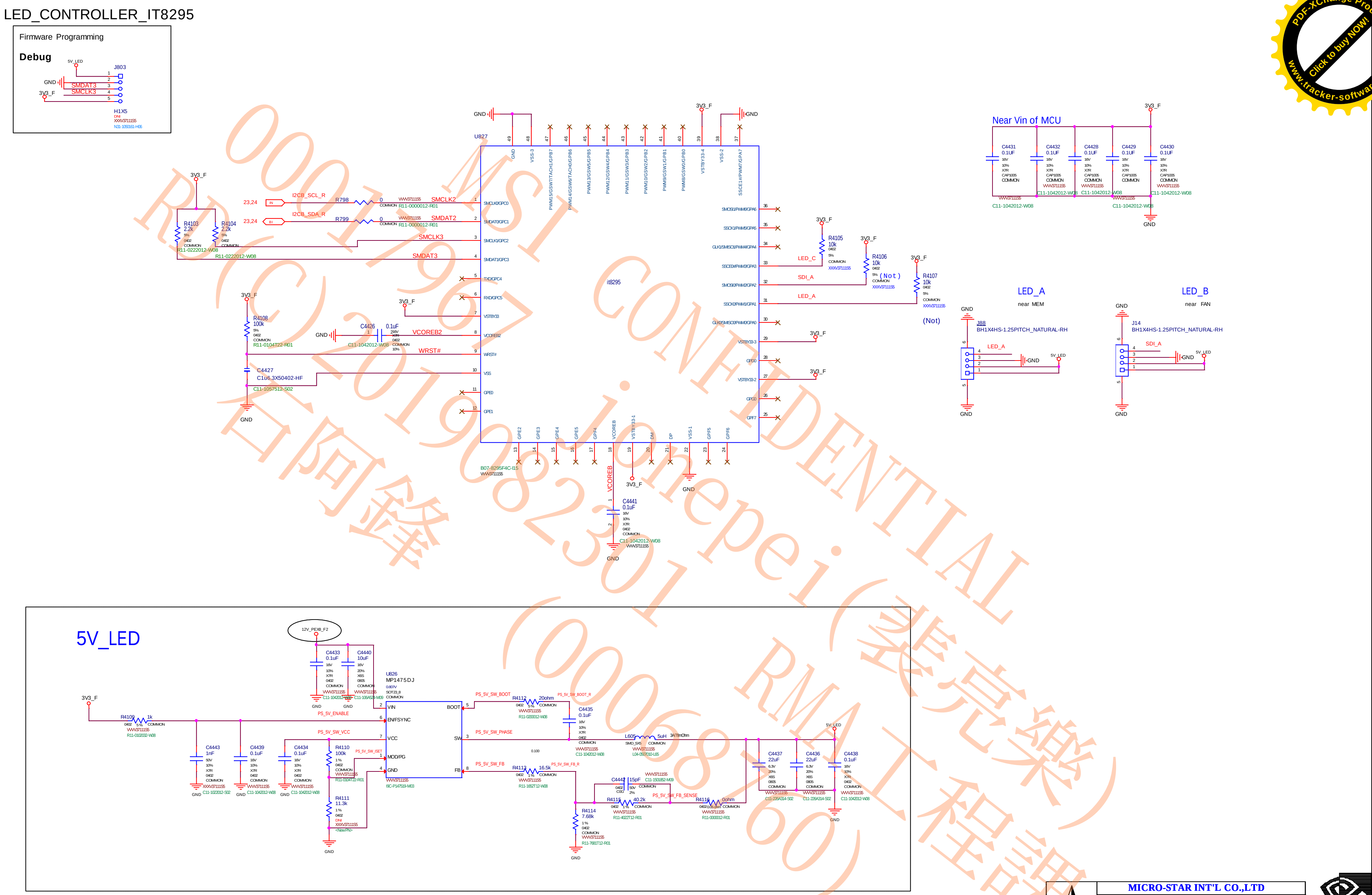

A	B	C	D	E	F	G	H

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ZERO IDLE POWER MCU

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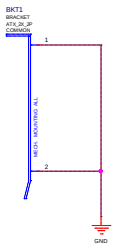
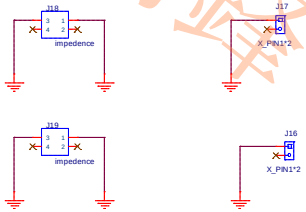
Mechanical Bracket/Thermal Solution

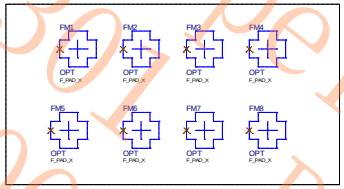
Brackets:



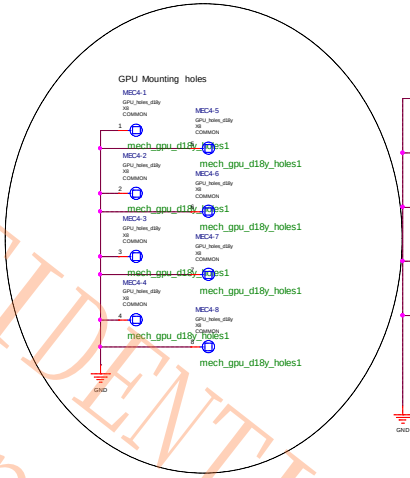
Bracket Screw

Screw

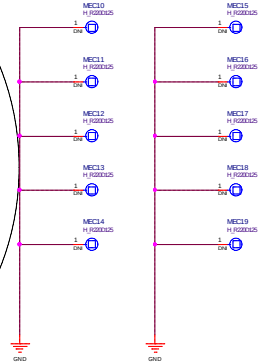




0 7 2 6 避開除孔點 螺絲 孔 位



Mechanical Holes Symbol



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