PG180-A02

256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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OrgName	Engineer: James_Huang	
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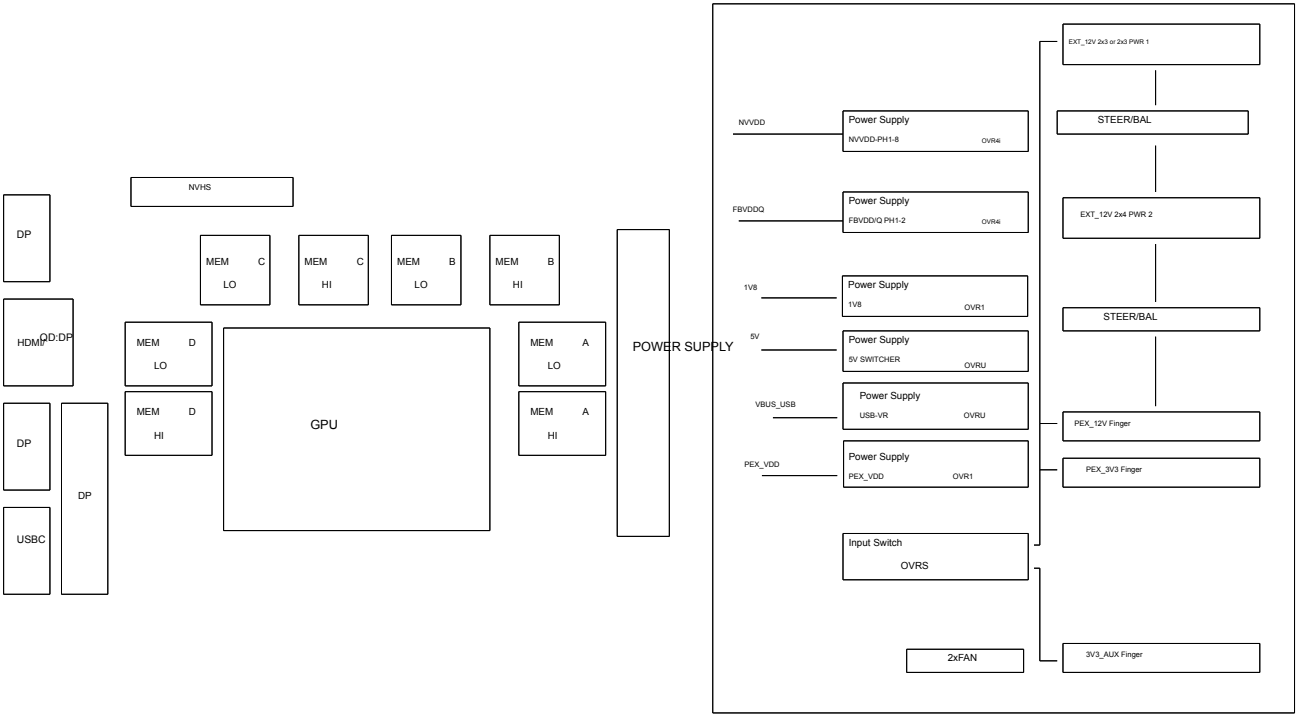
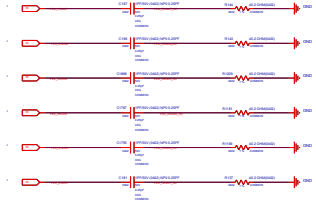
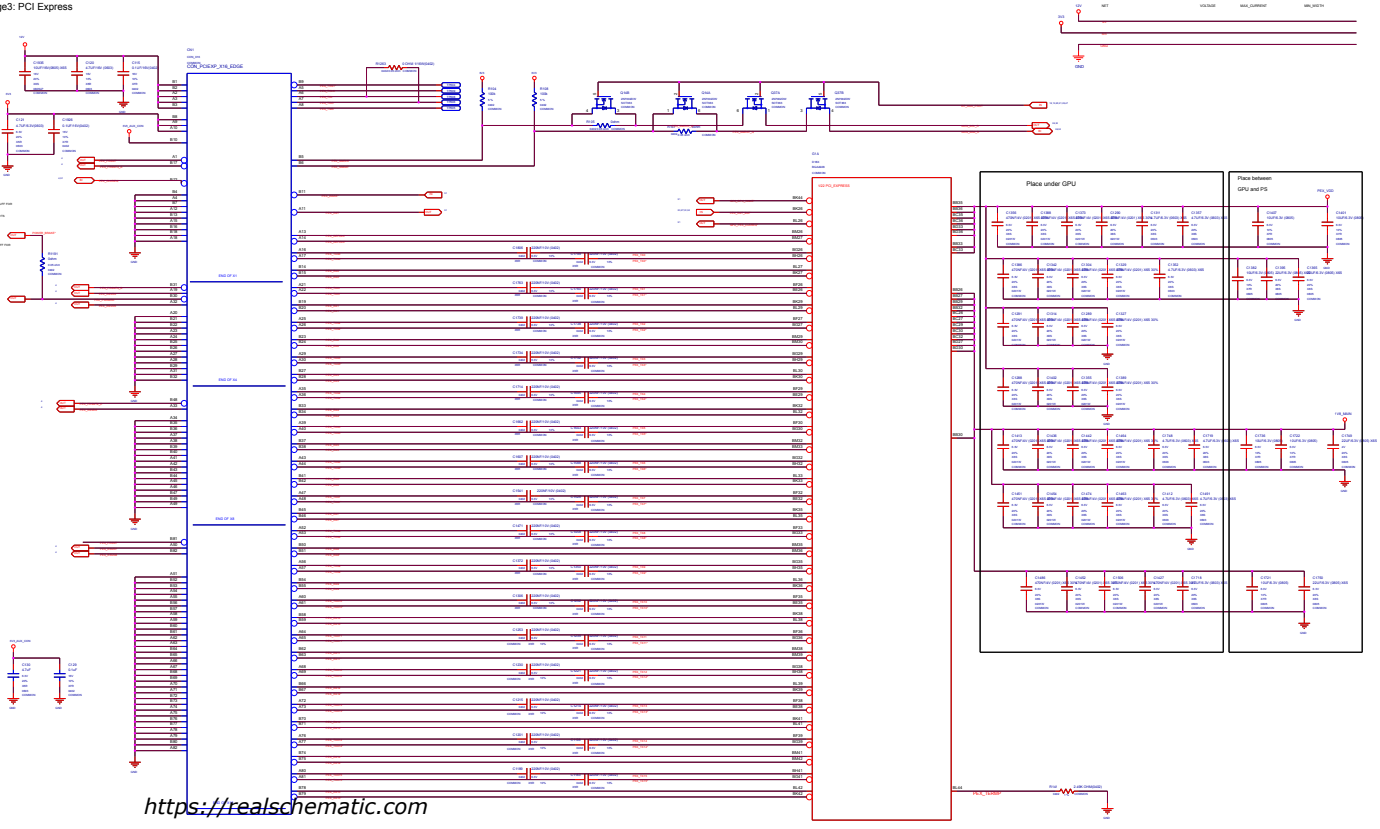
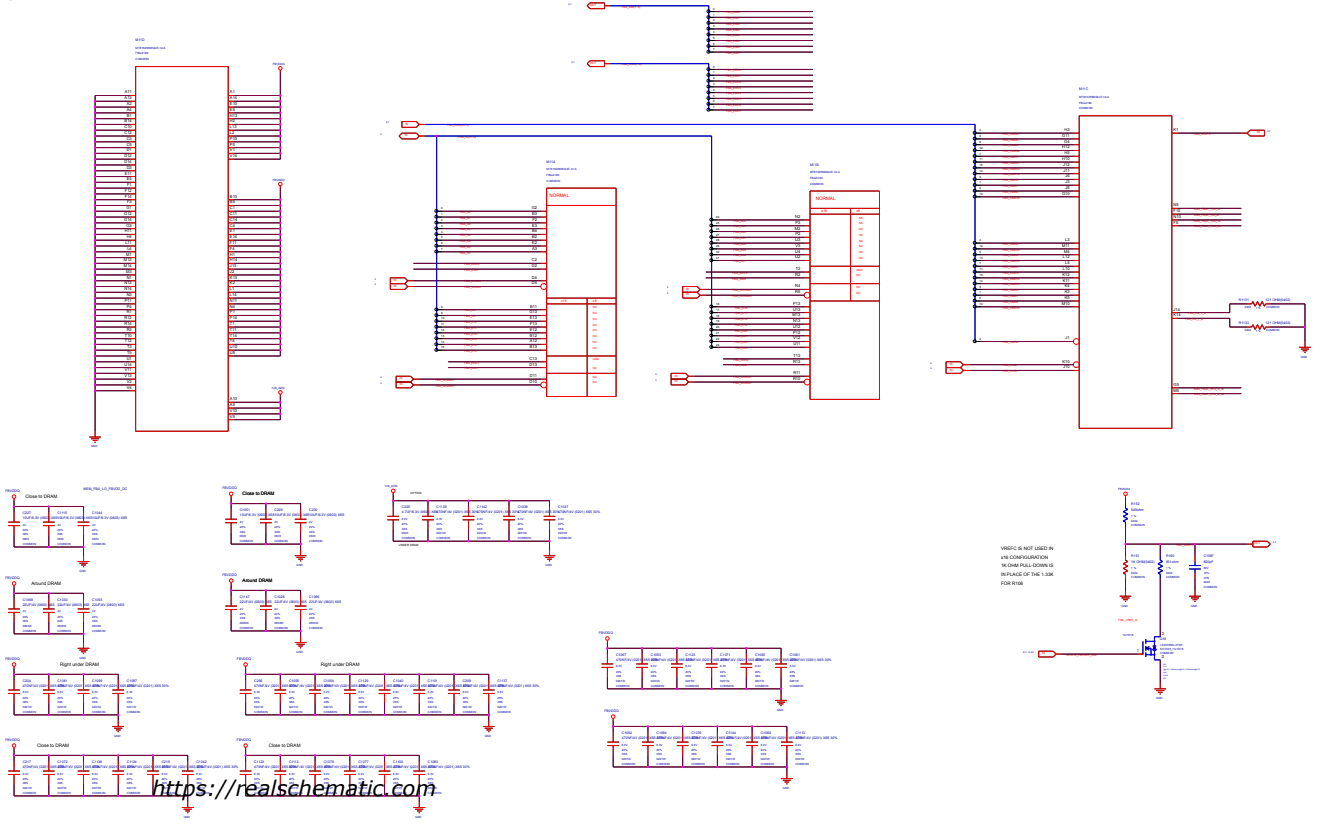


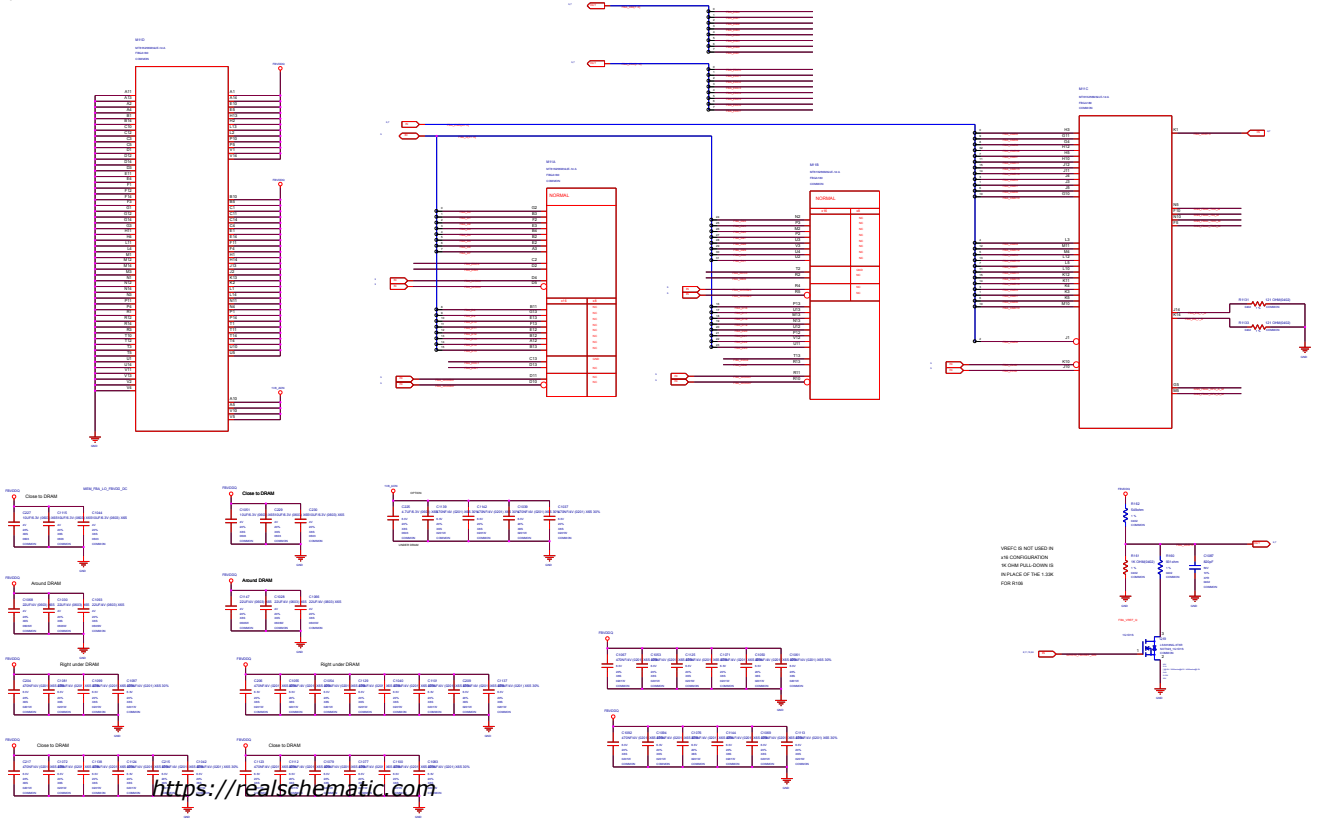
OrgName	Title : Block Diagram		
	Engineer: James_Huang		
Size: Custom	Project Name: CG180P2		Rev: 1.00
Date: 27-JUN-2018	Sheet 2 of 47		

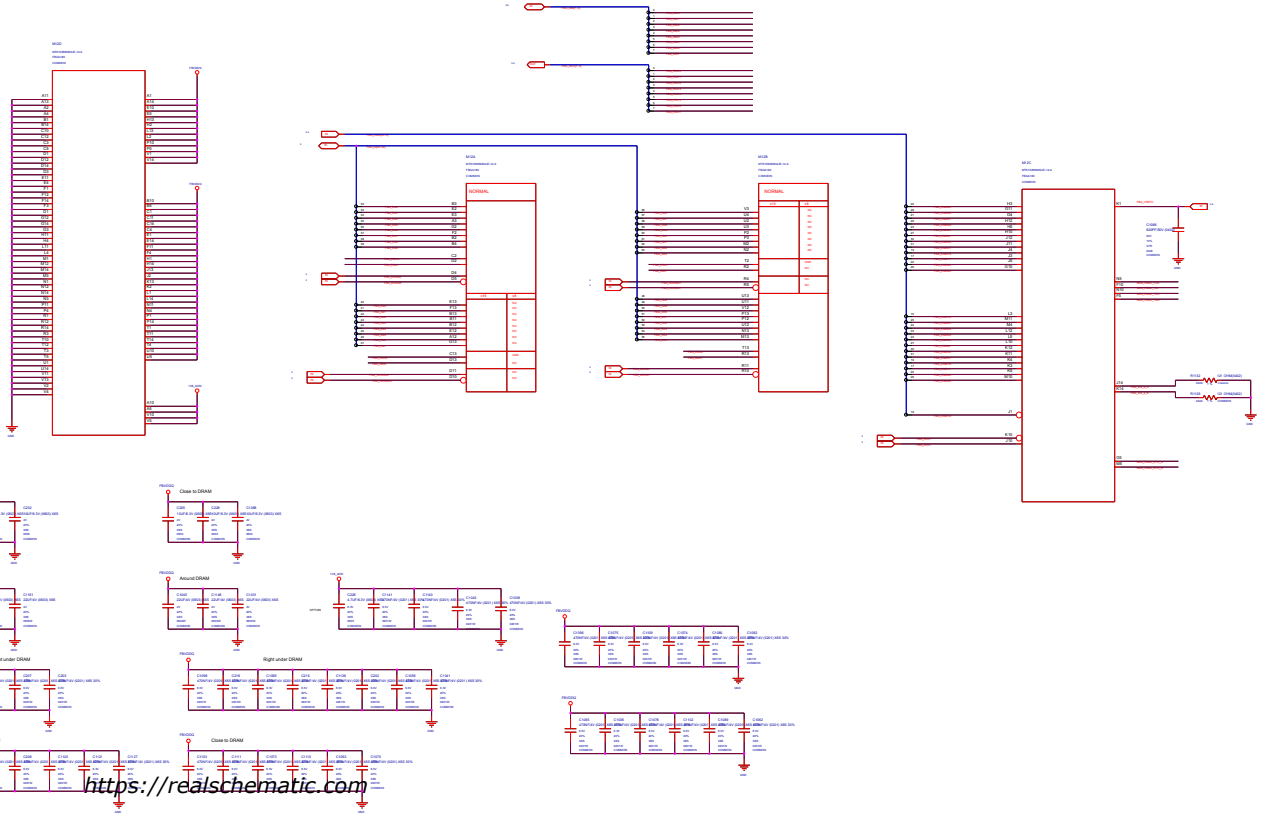
PLACE CLOSE TO 68/1

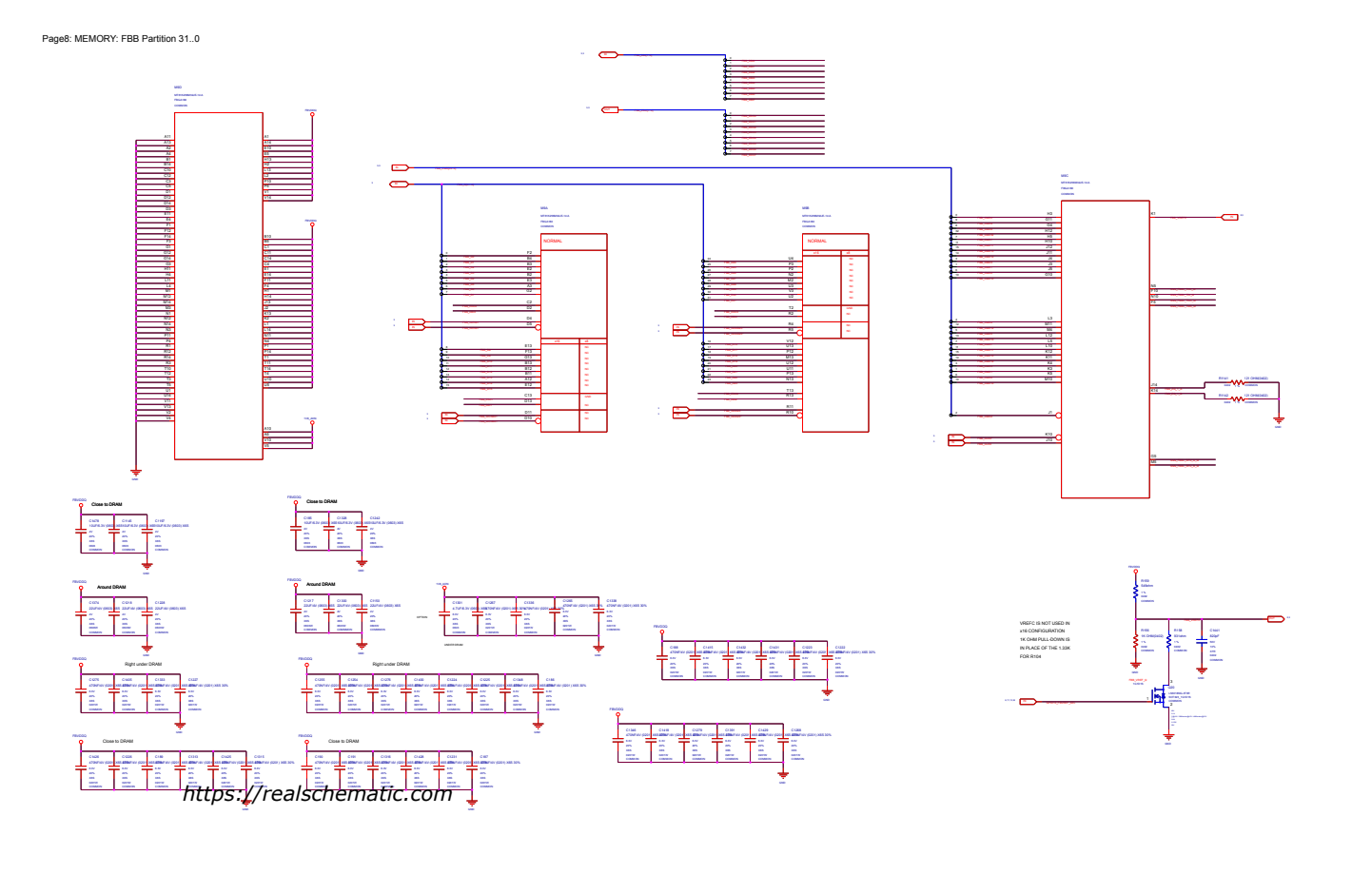


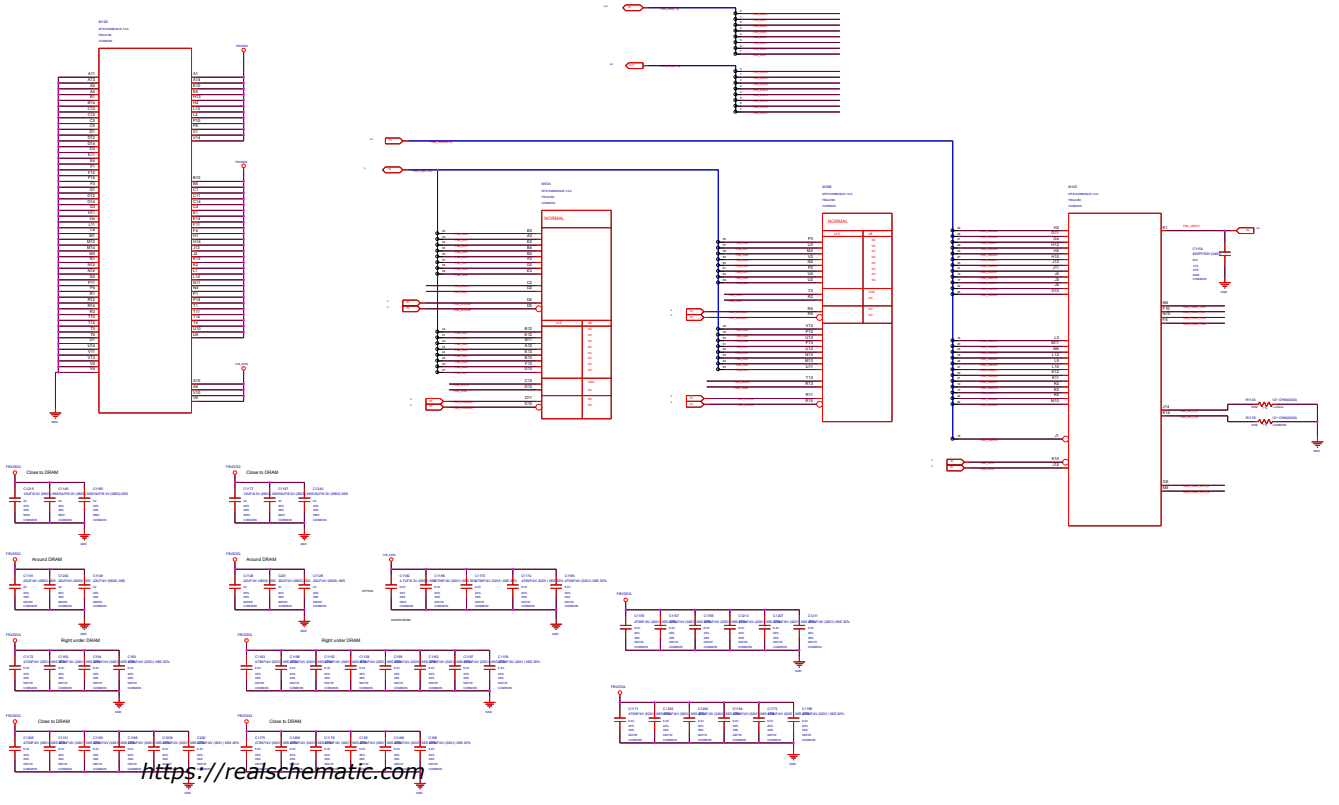


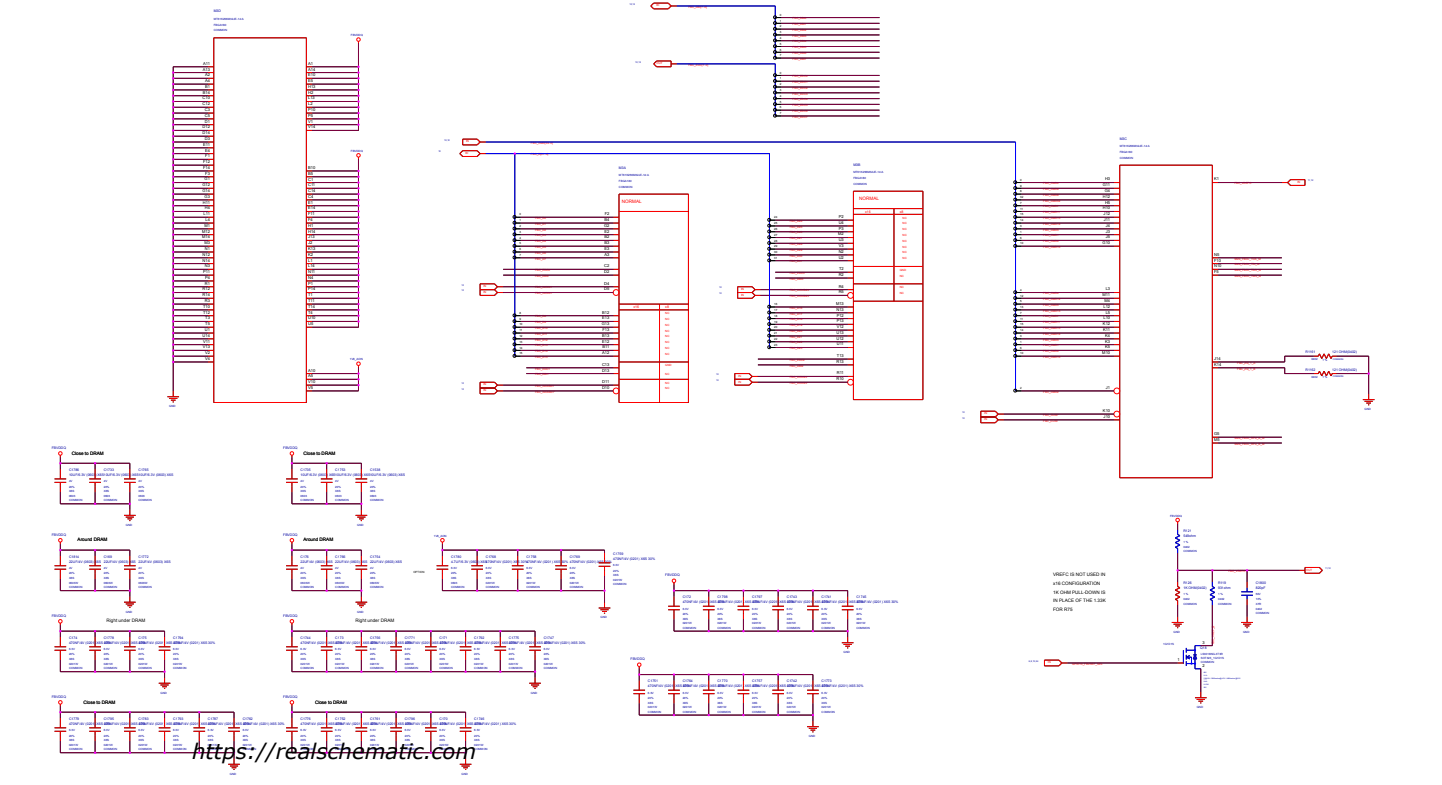


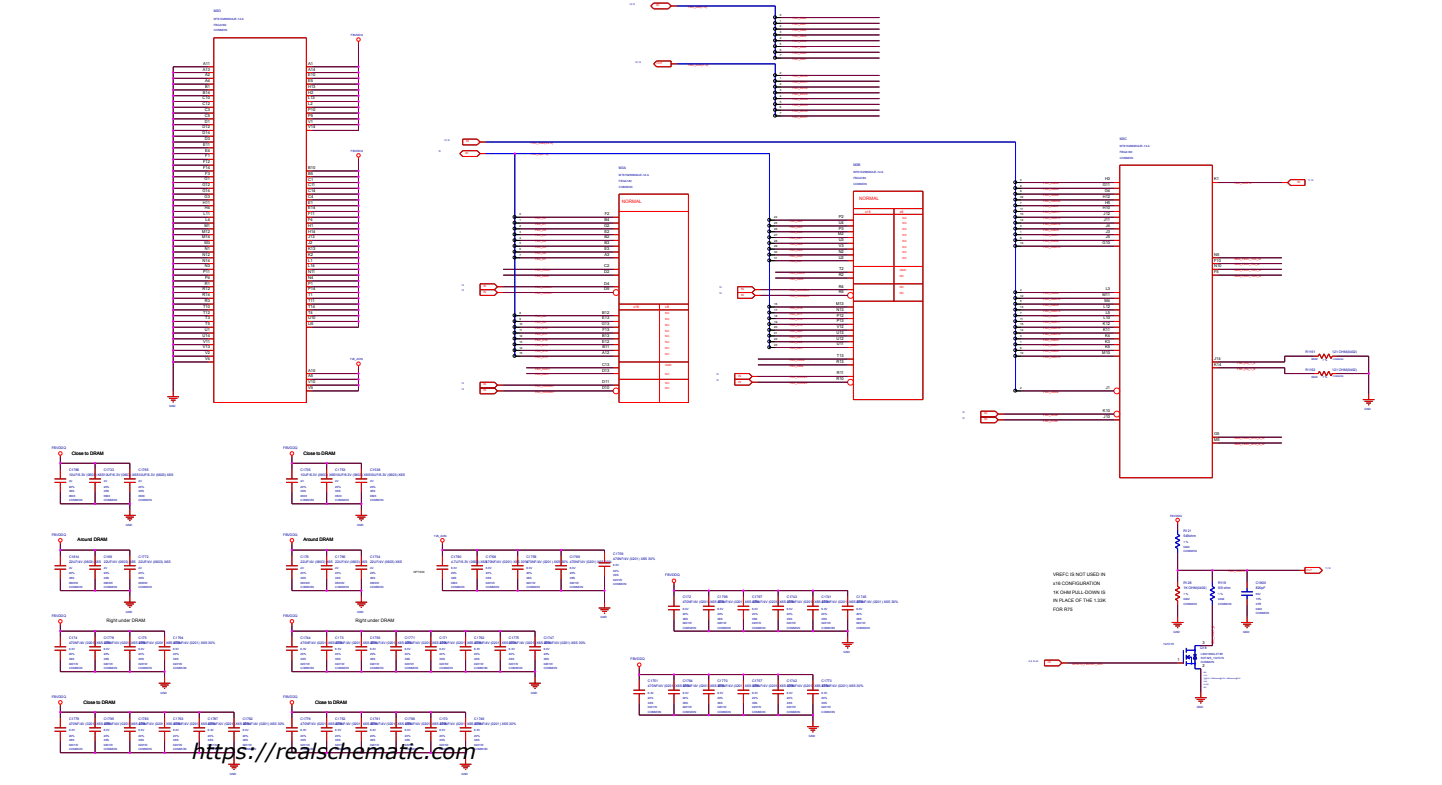


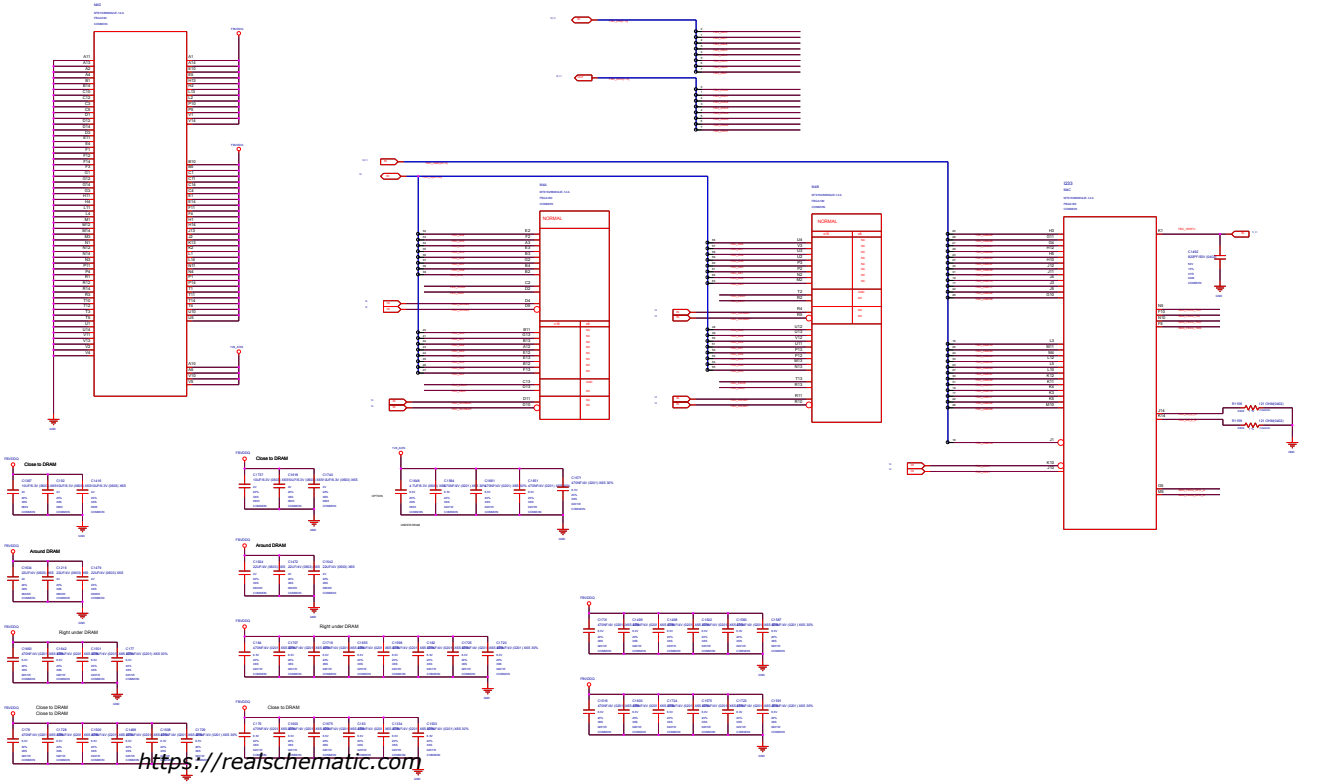


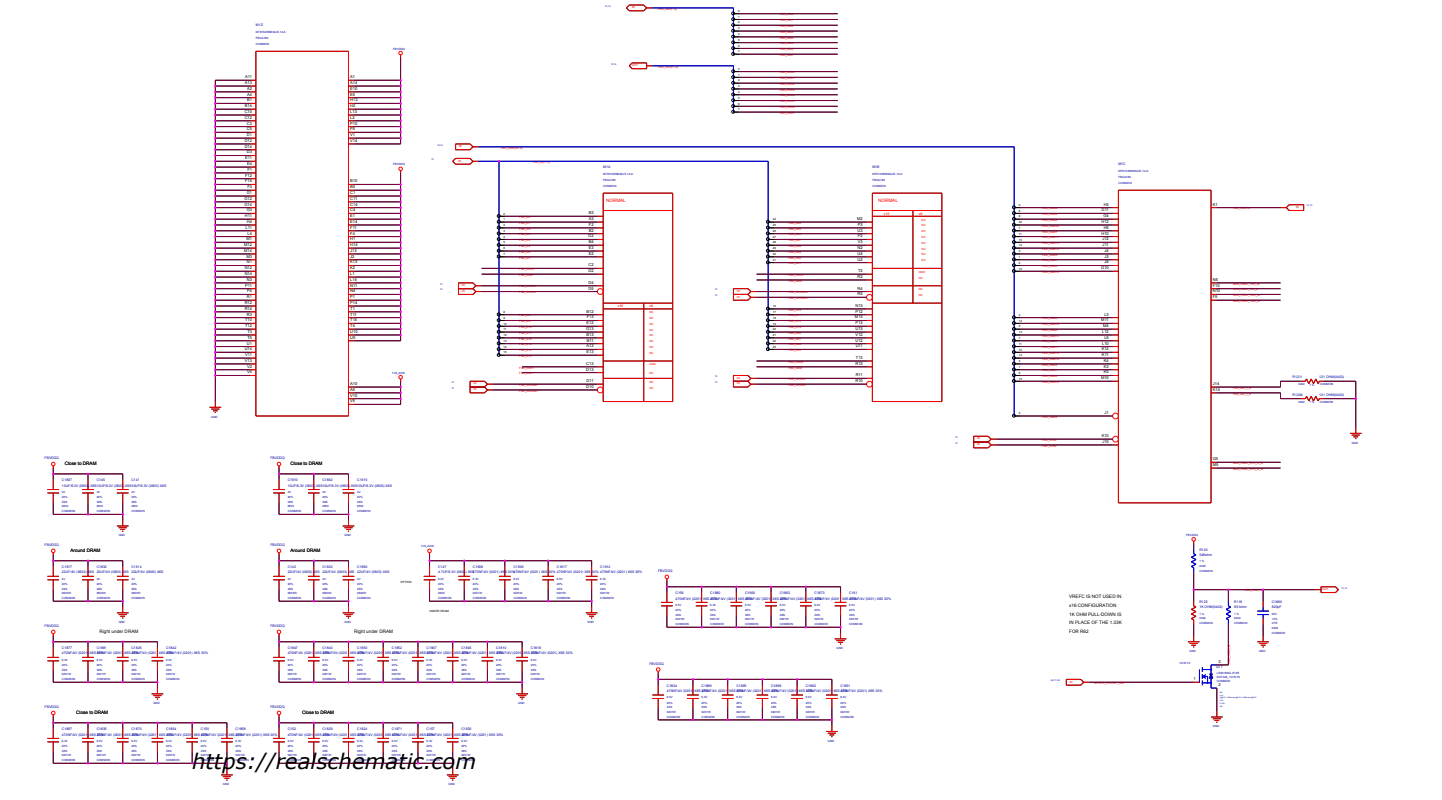


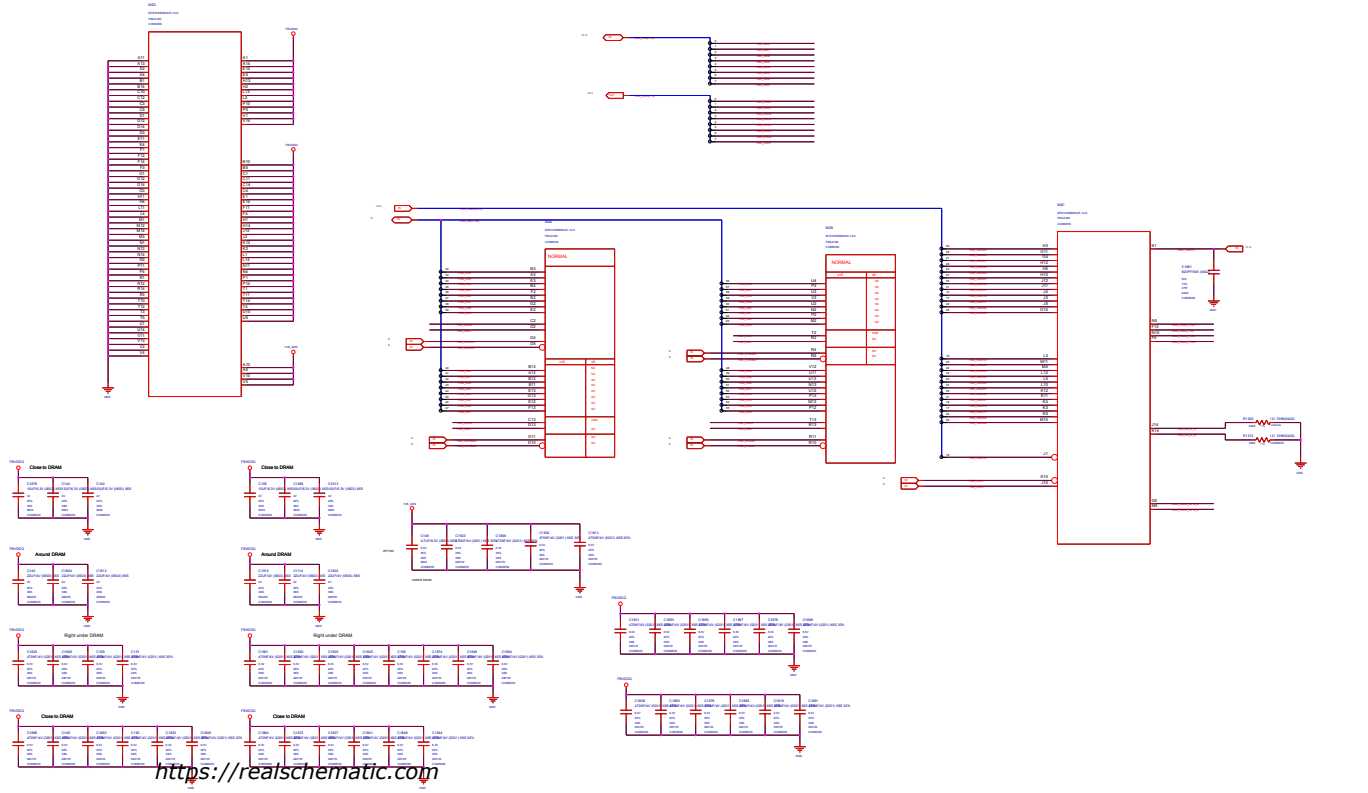


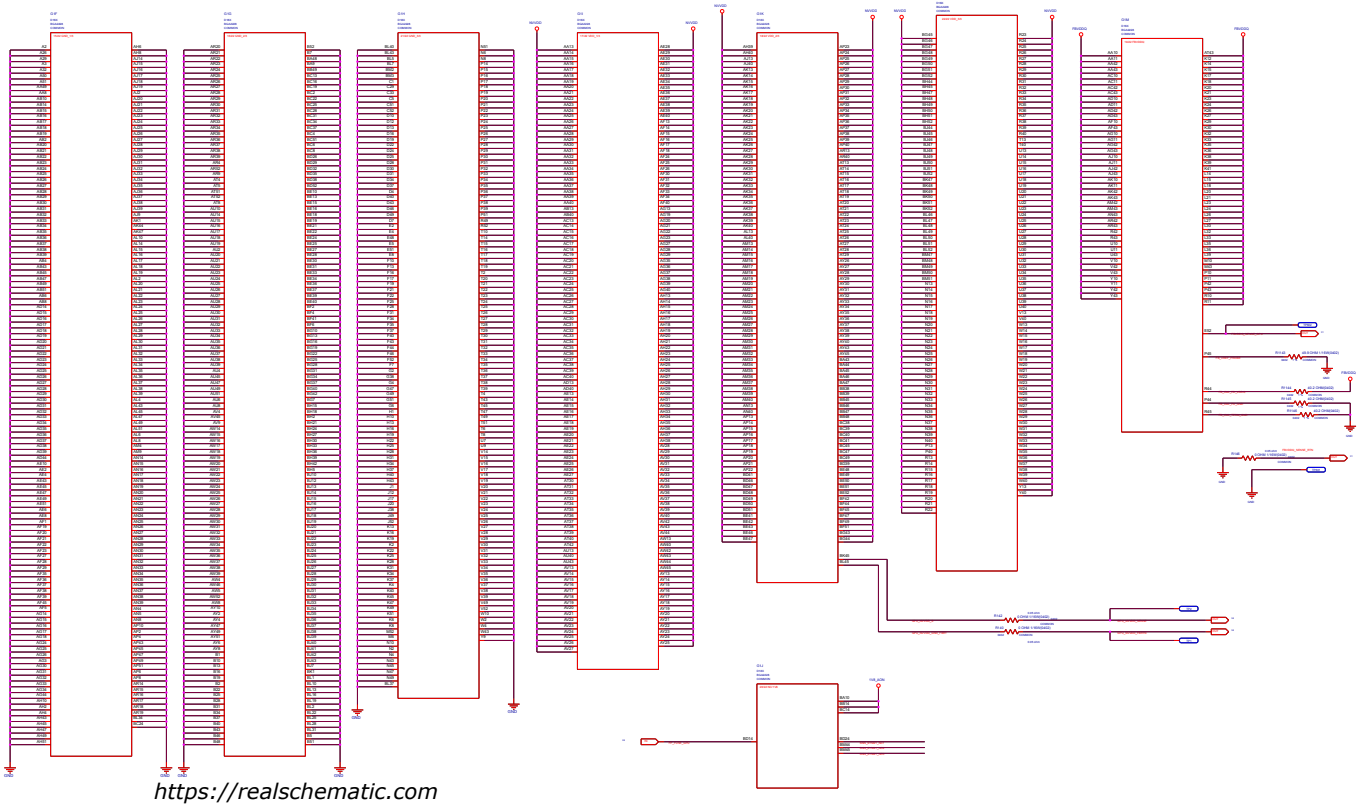












FBVDDQ

Partition A

Partition B

Partition C

Partition D

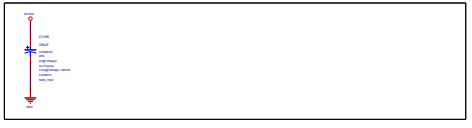
Place Close to GPU

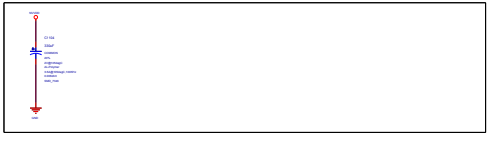
Place Close to GPU

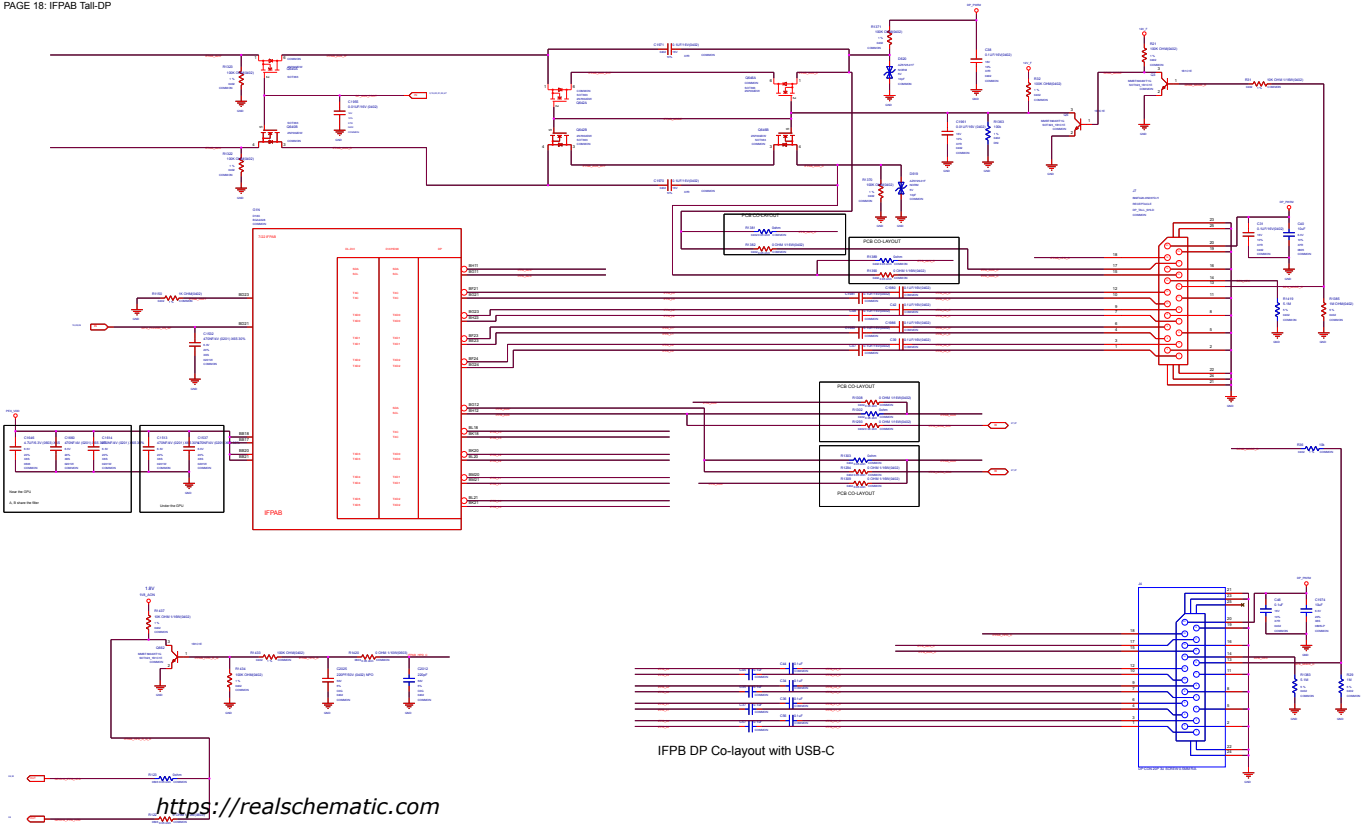
NVVDD

1V8_AON

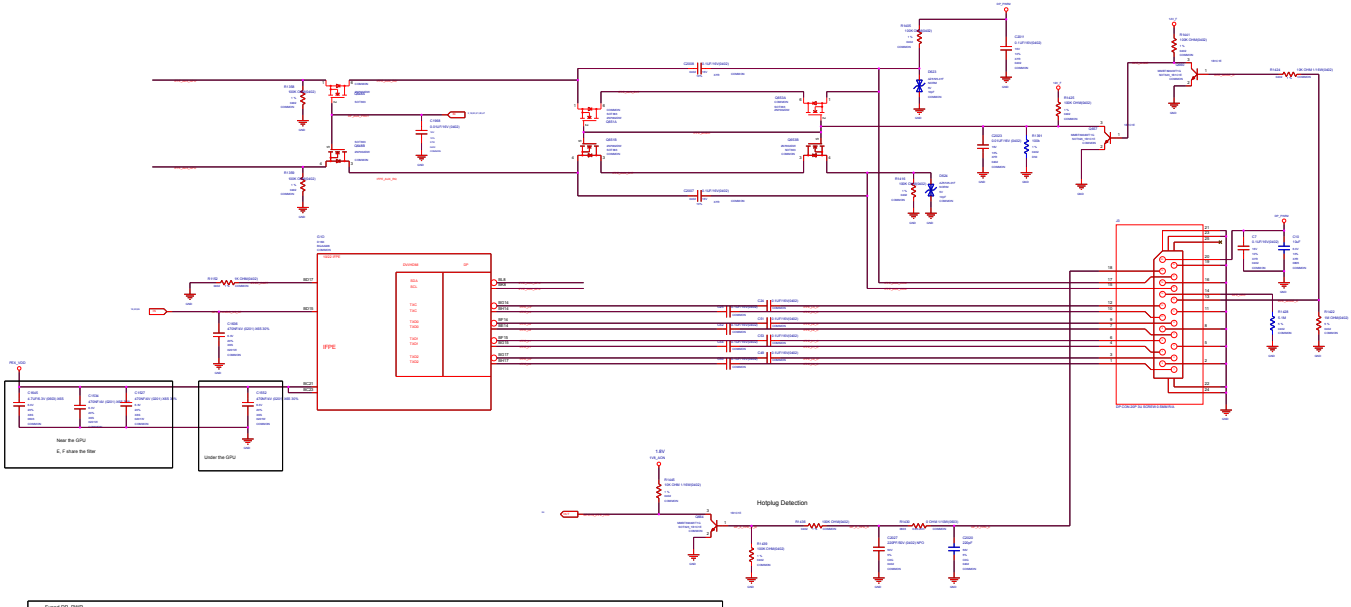
NVVDD

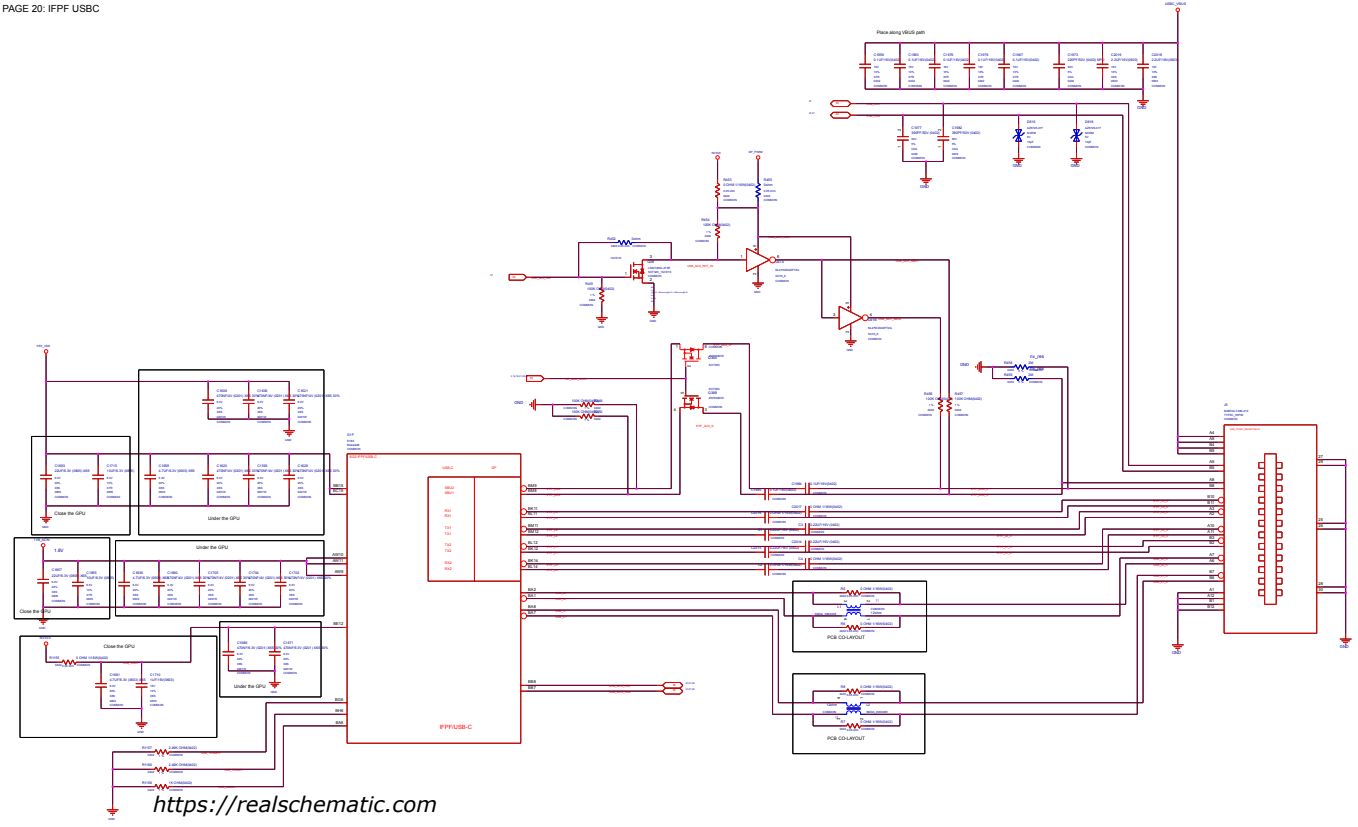


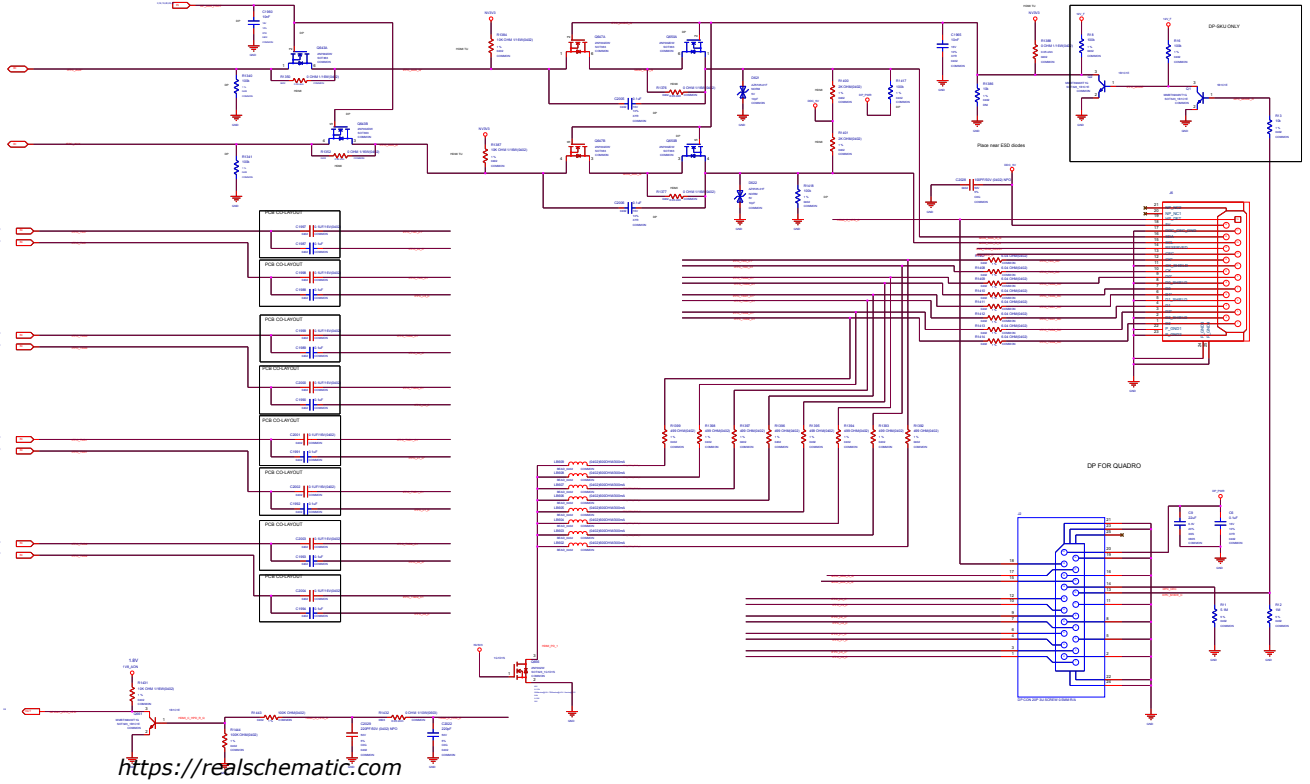


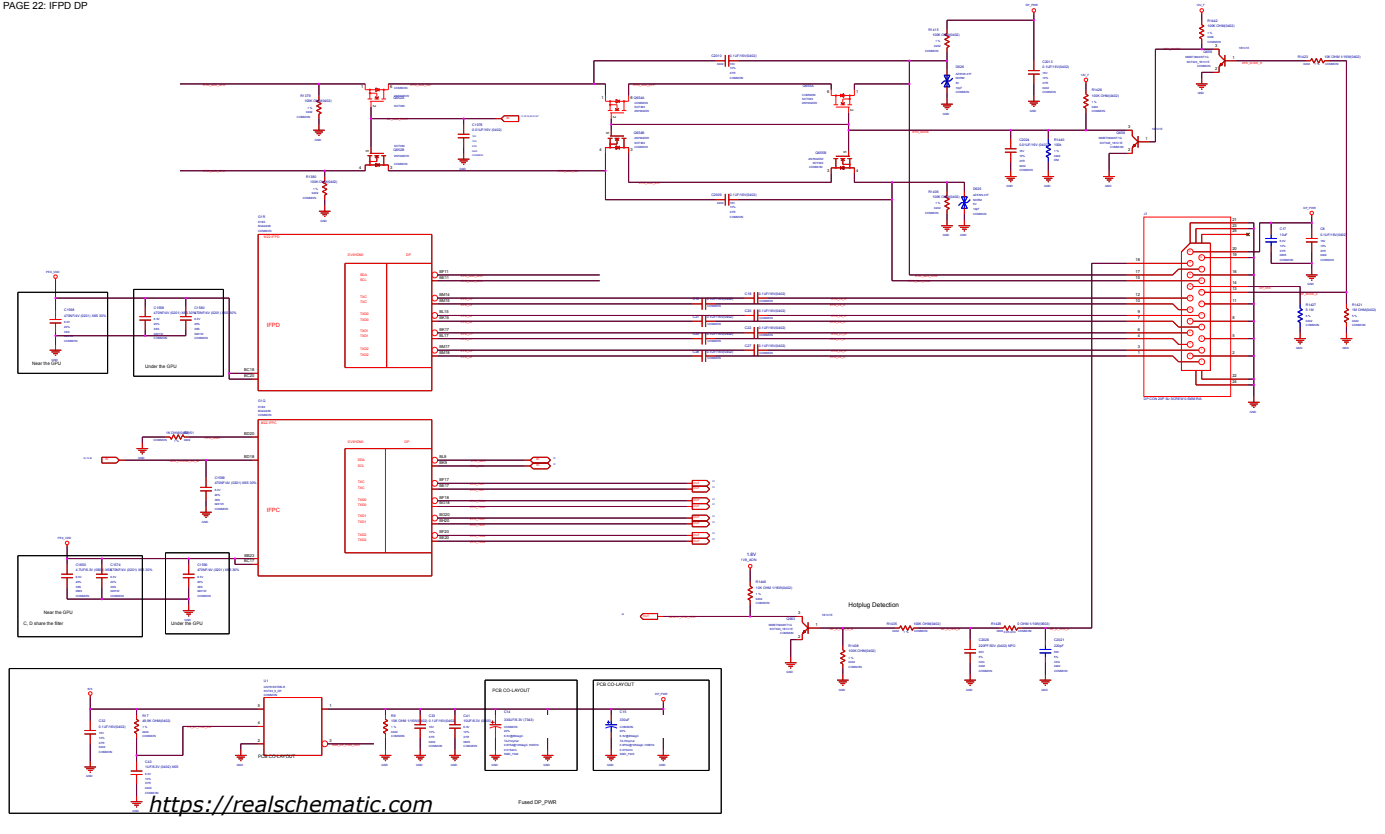


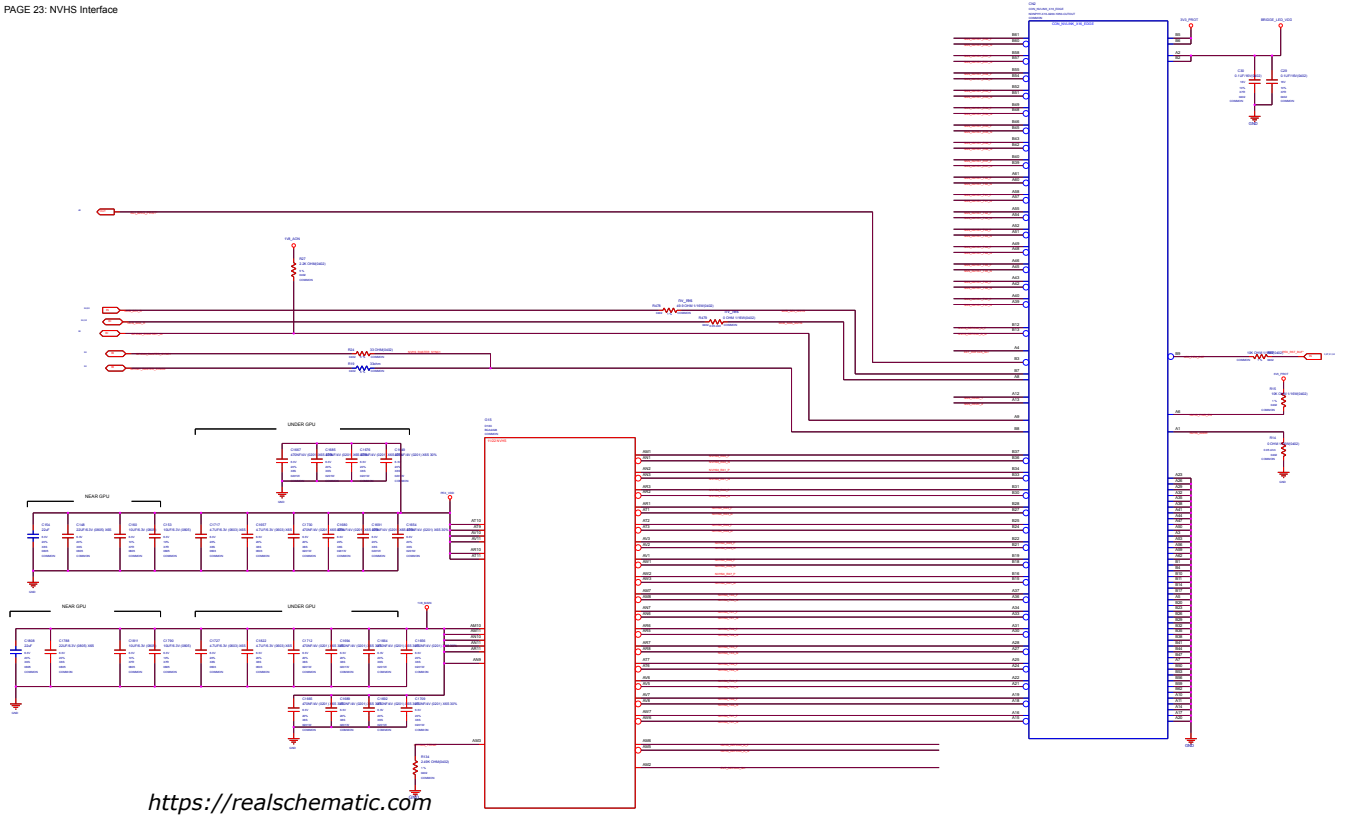
IFPB DP Co-layout with USB-C

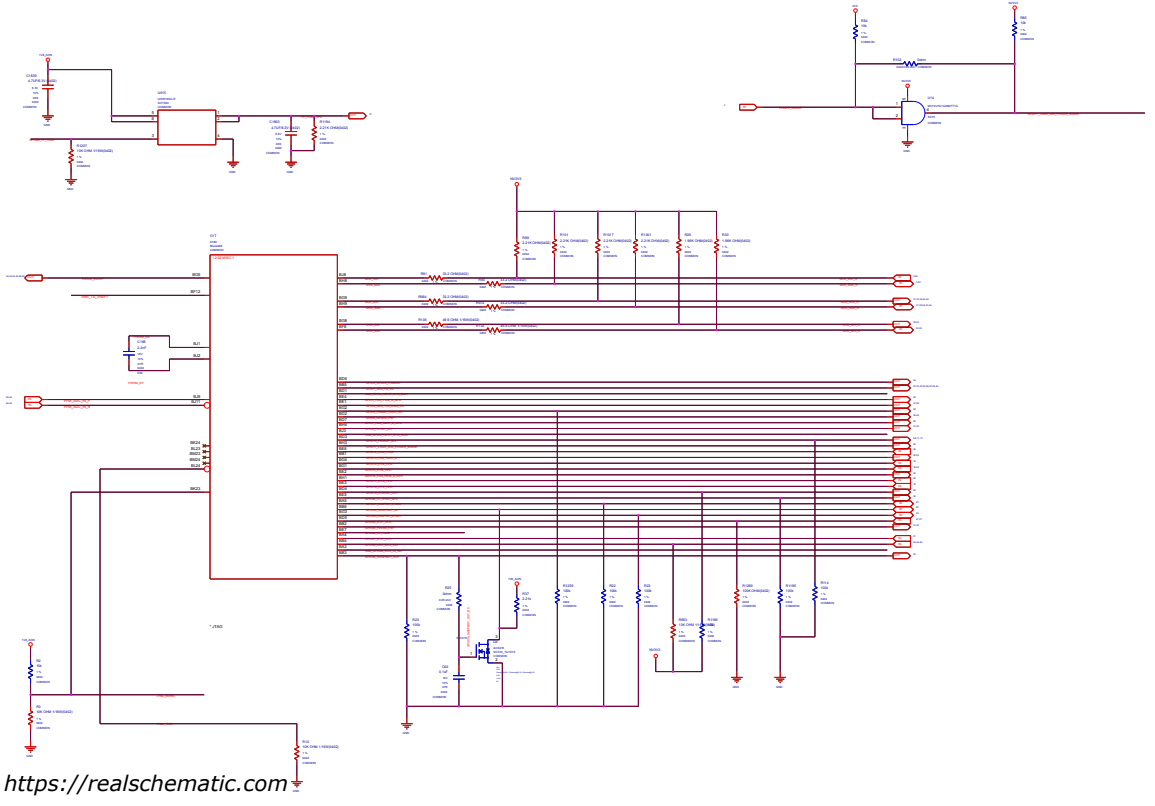



Place along VBUS path
Close the GPU
Under the GPU
1.8V
IFPF/USB-C
PCB CO-LAYOUT
https://realschematic.com




IFPD
IFPC
Near the GPU
Under the GPU
Near the GPU
C, D share the filter
Under the GPU
Hotplug Detection
PCB CO-LAYOUT
PCB CO-LAYOUT
Fused DP_PWR
https://realschematic.com





H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]		
L	L	L	00000	RAMCFG TBD	
L	L	H	00001	RAMCFG TBD	DEFAULT
L	H	L	00010	RAMCFG TBD	
L	H	H	00011	RAMCFG TBD	
H	H	L	00110	RAMCFG TBD	
H	H	H	00111	RAMCFG TBD	

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0]:FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

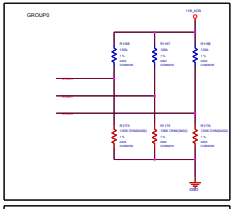
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

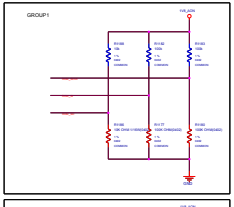
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

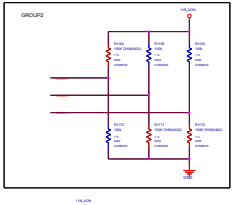
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

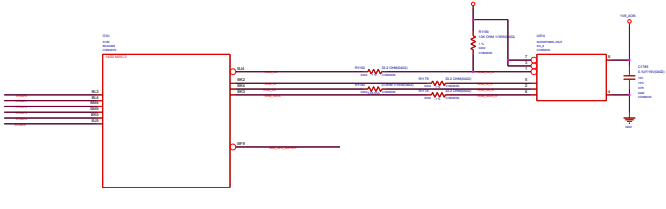
Default

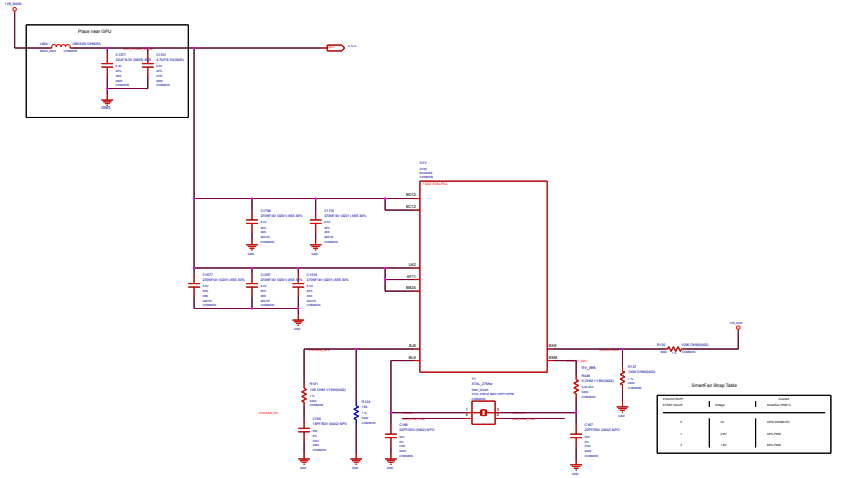
RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung

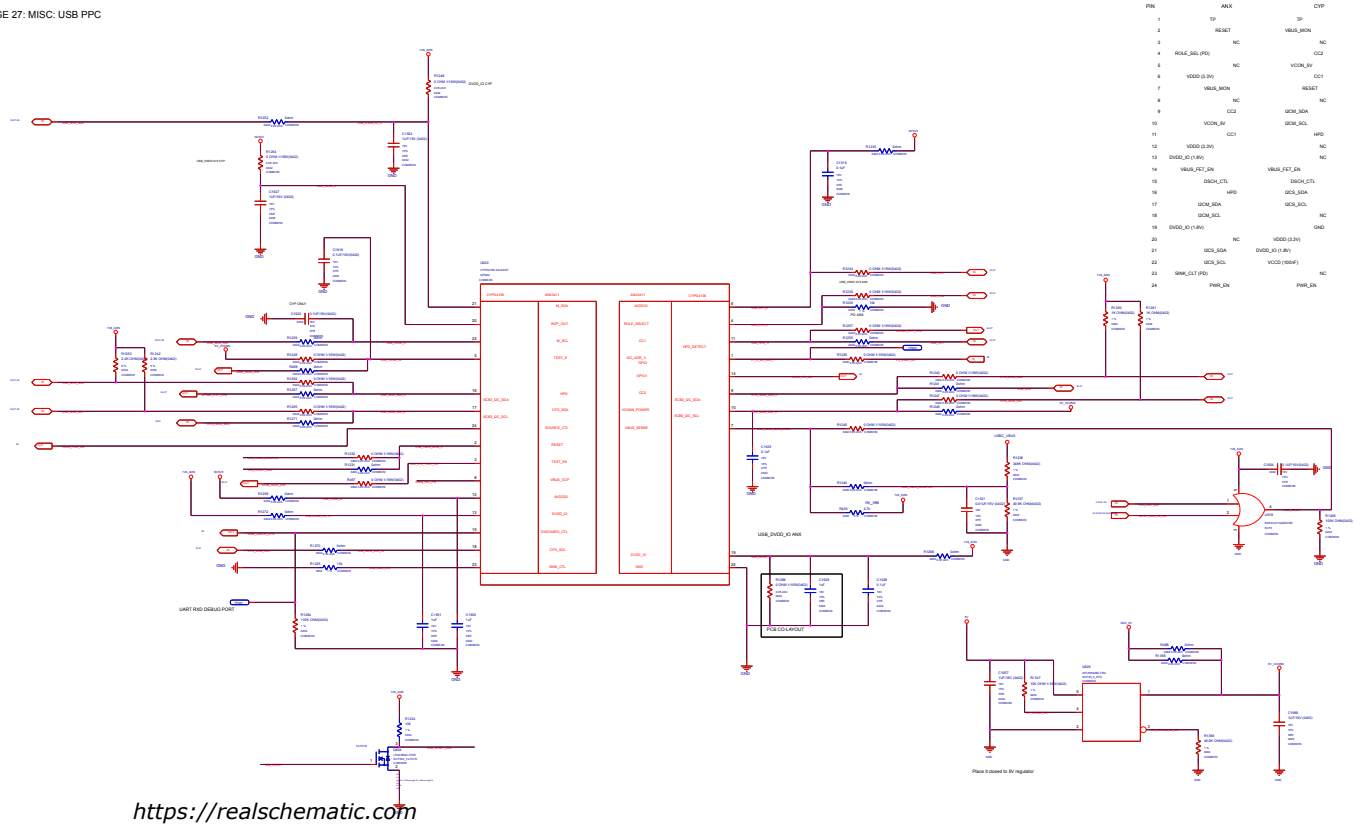


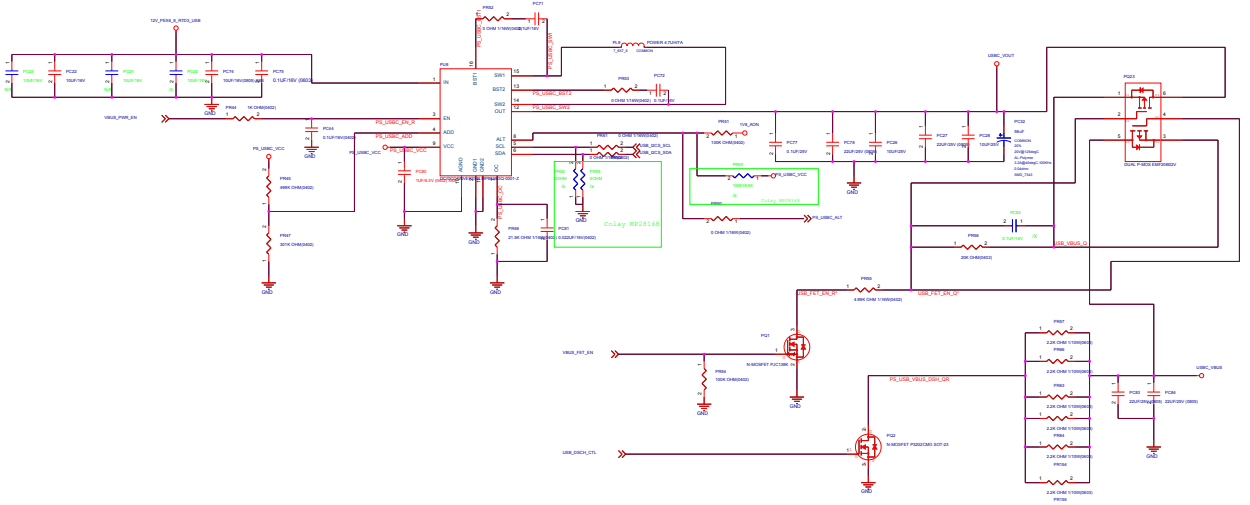




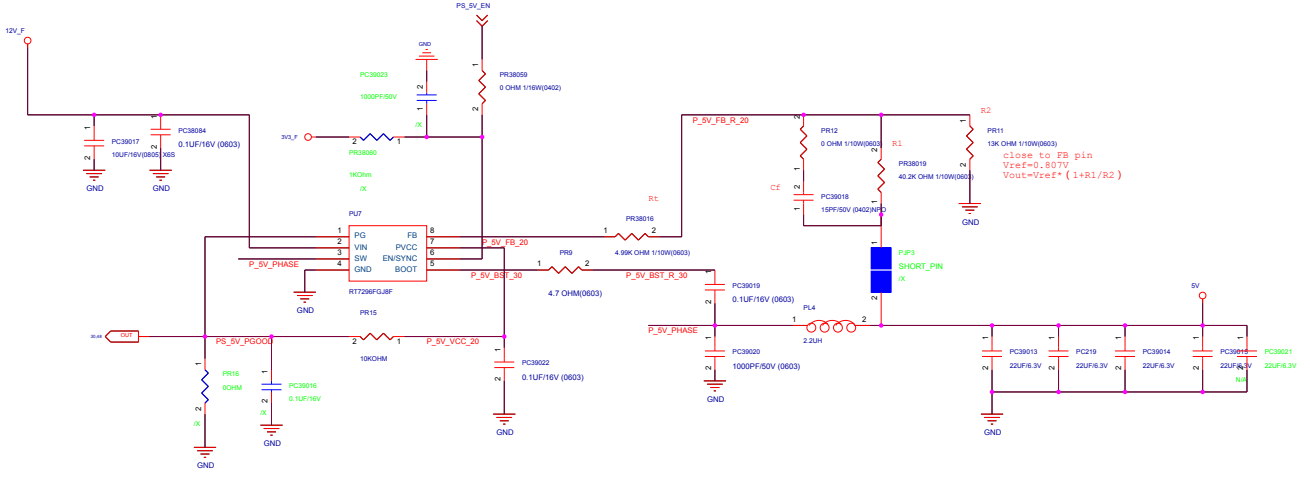


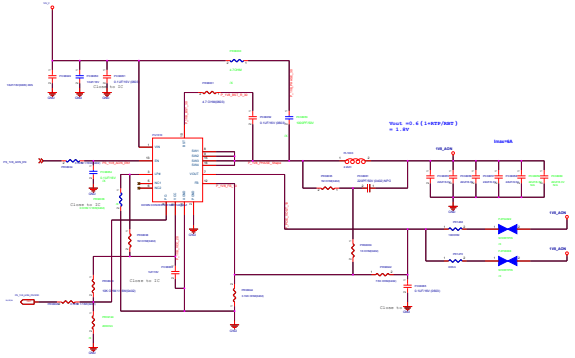


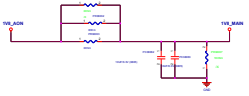


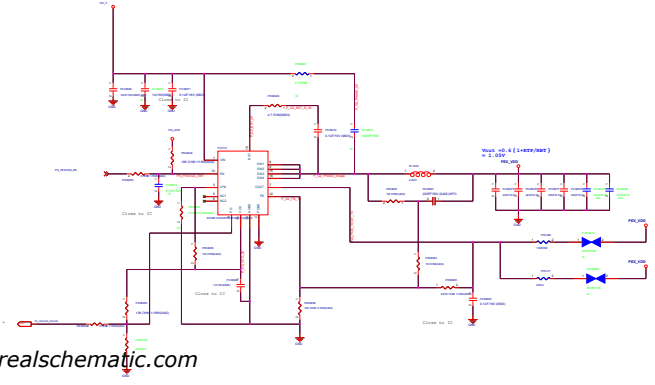


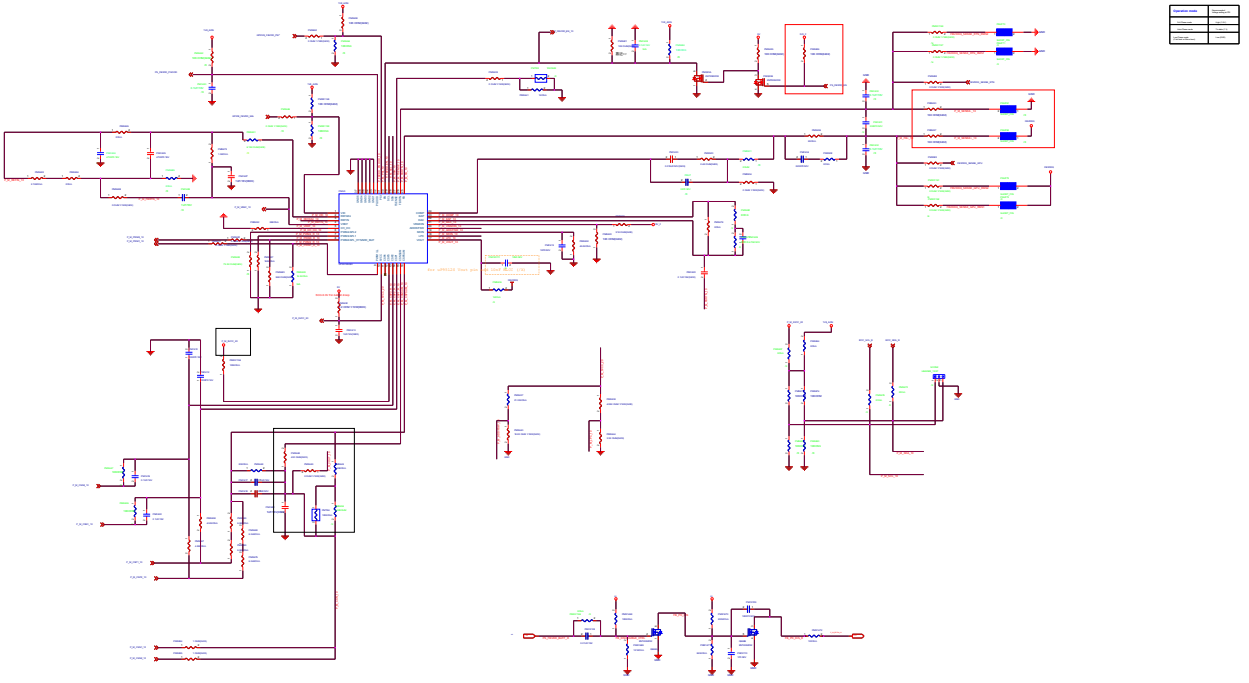
https://realschematic.com

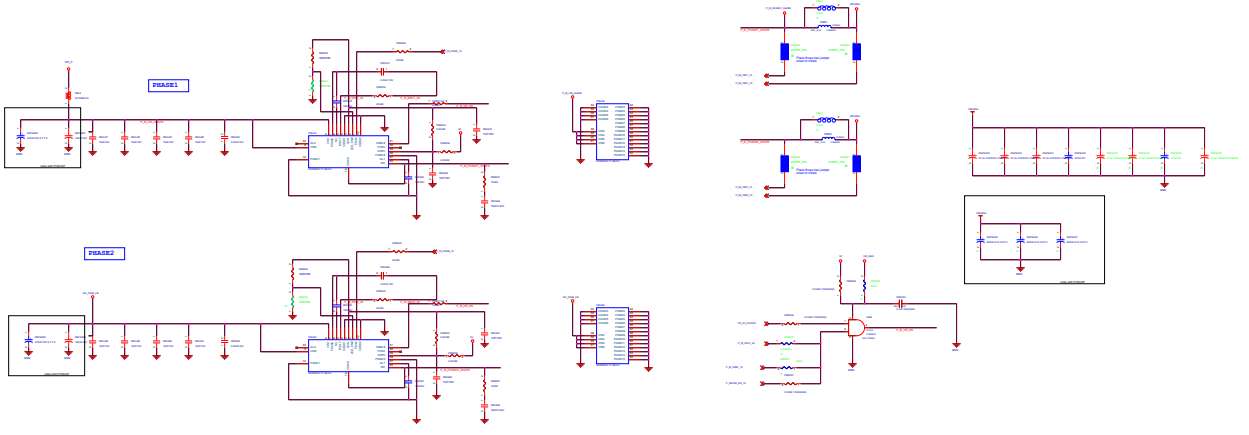


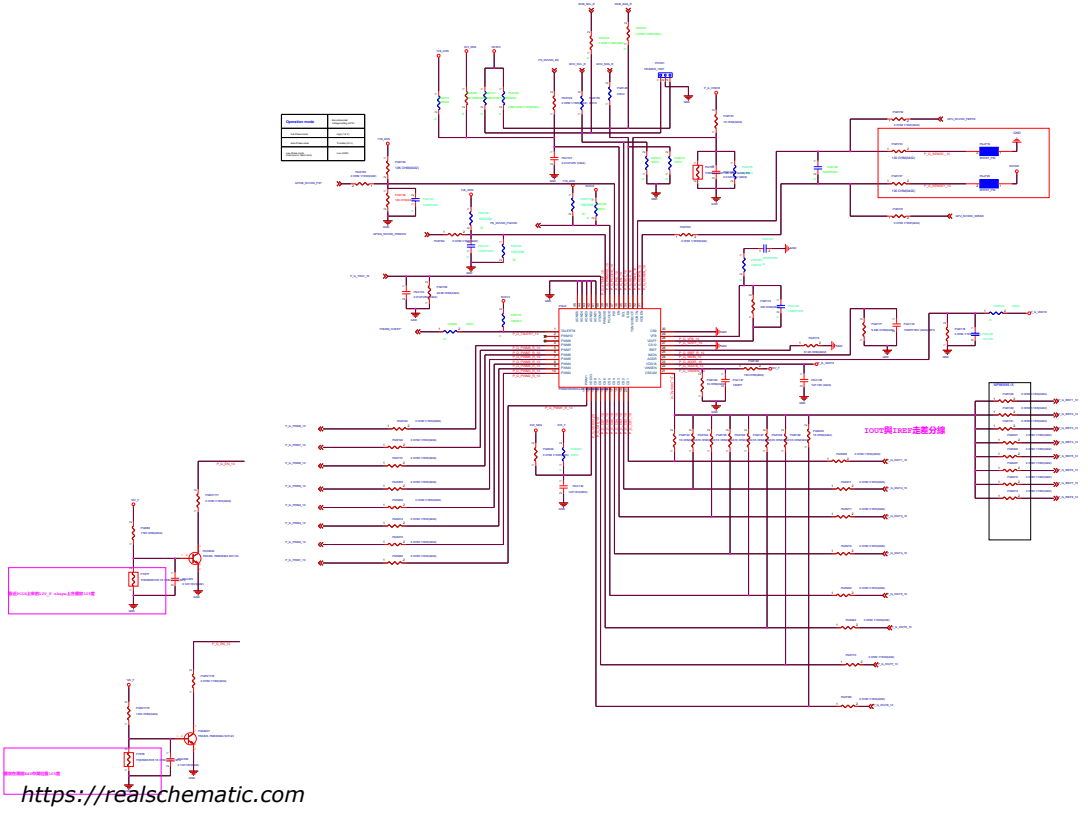


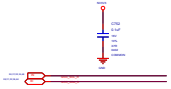


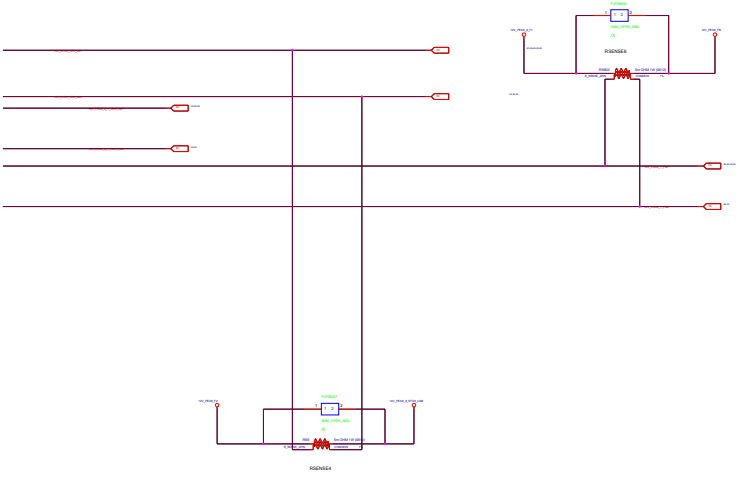


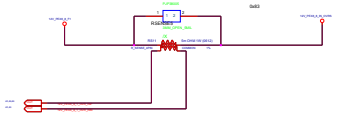


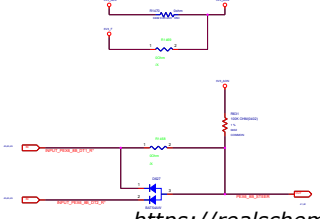


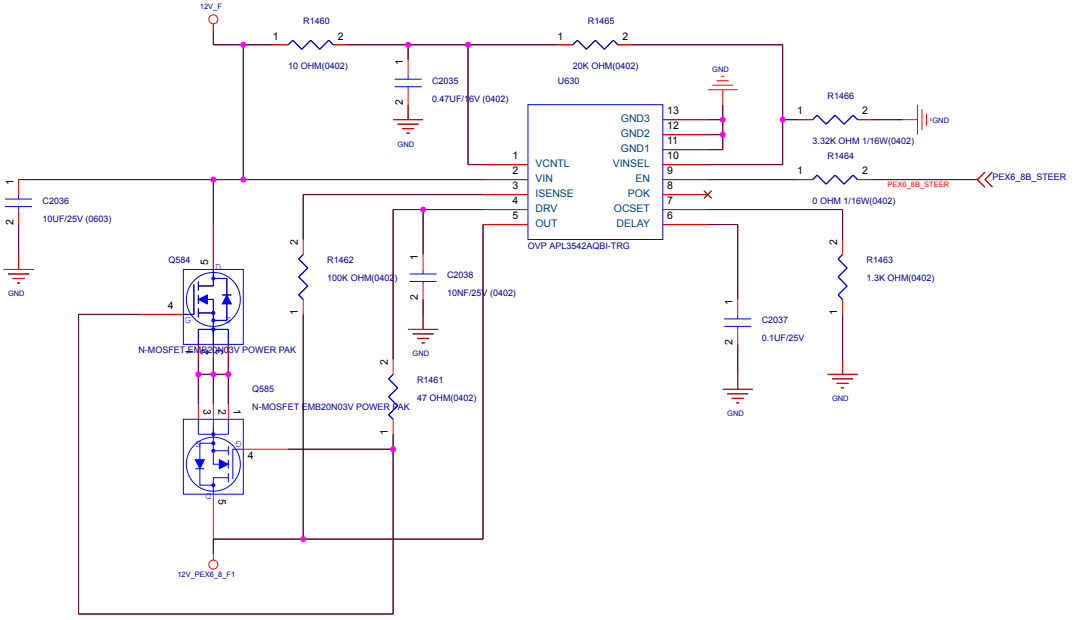


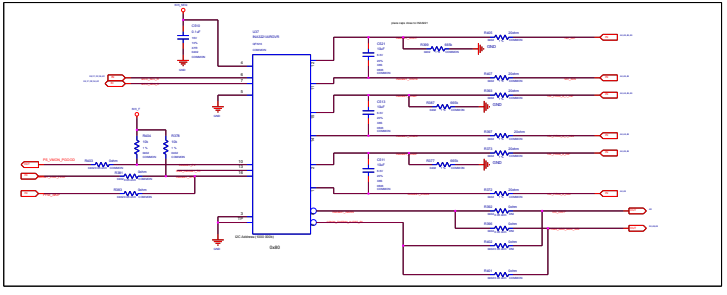


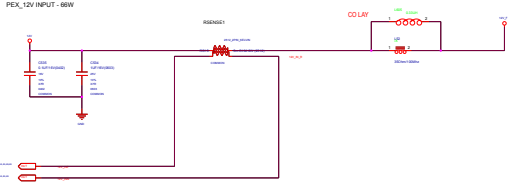


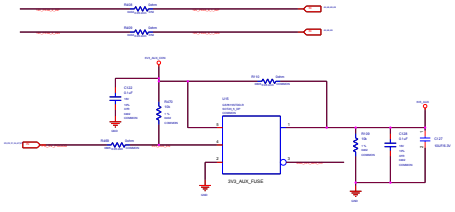




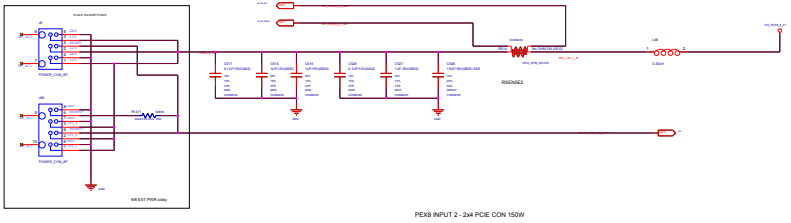




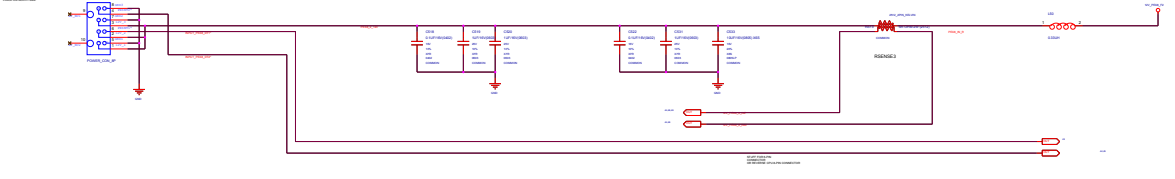


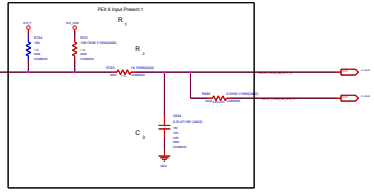


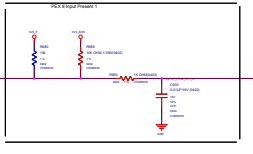
PEX6 INPUT 1 - 2x3 PCIE CON 75W

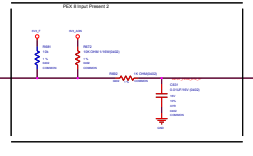


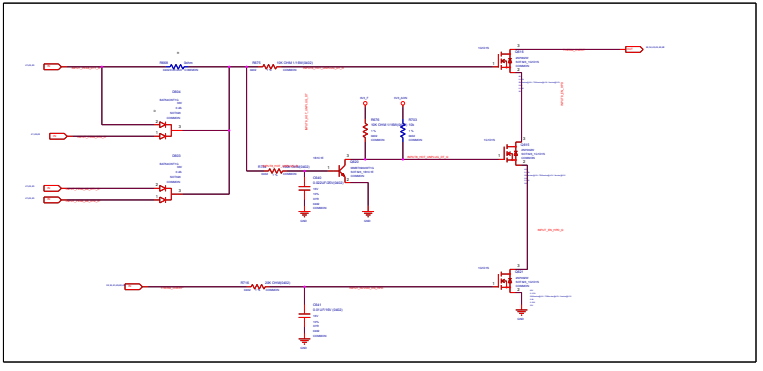
PEX8 INPUT 2 - 2x4 PCIE CON 150W

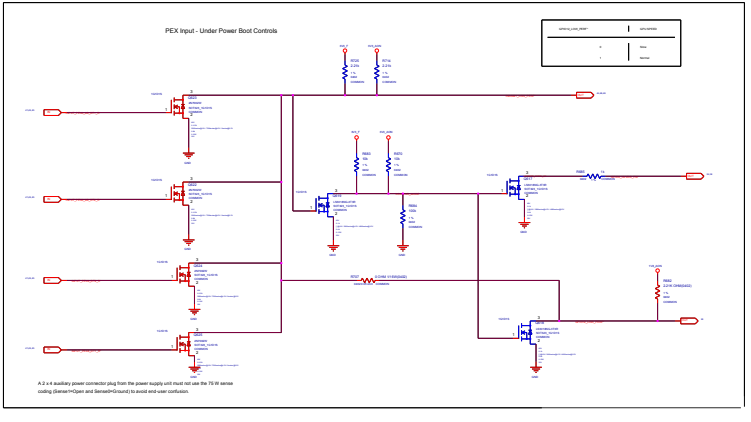


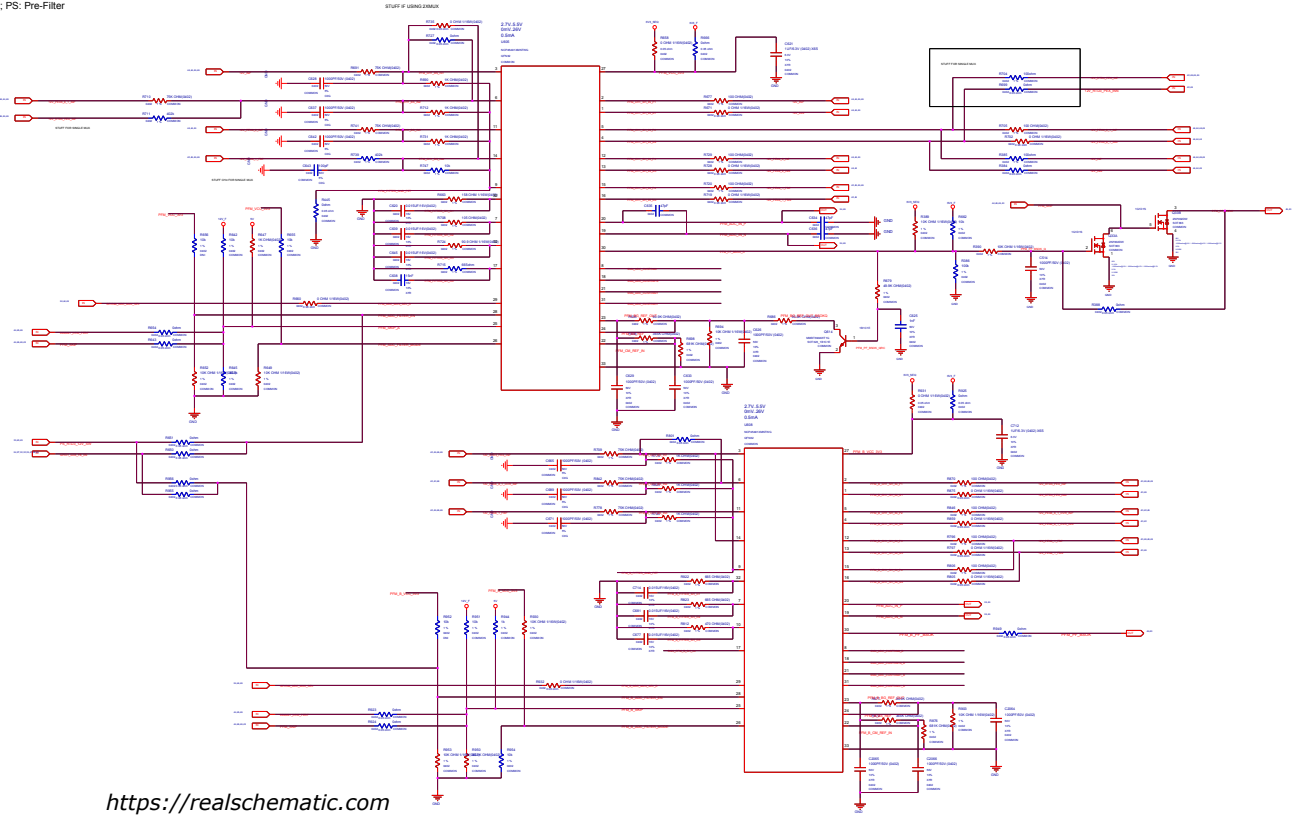


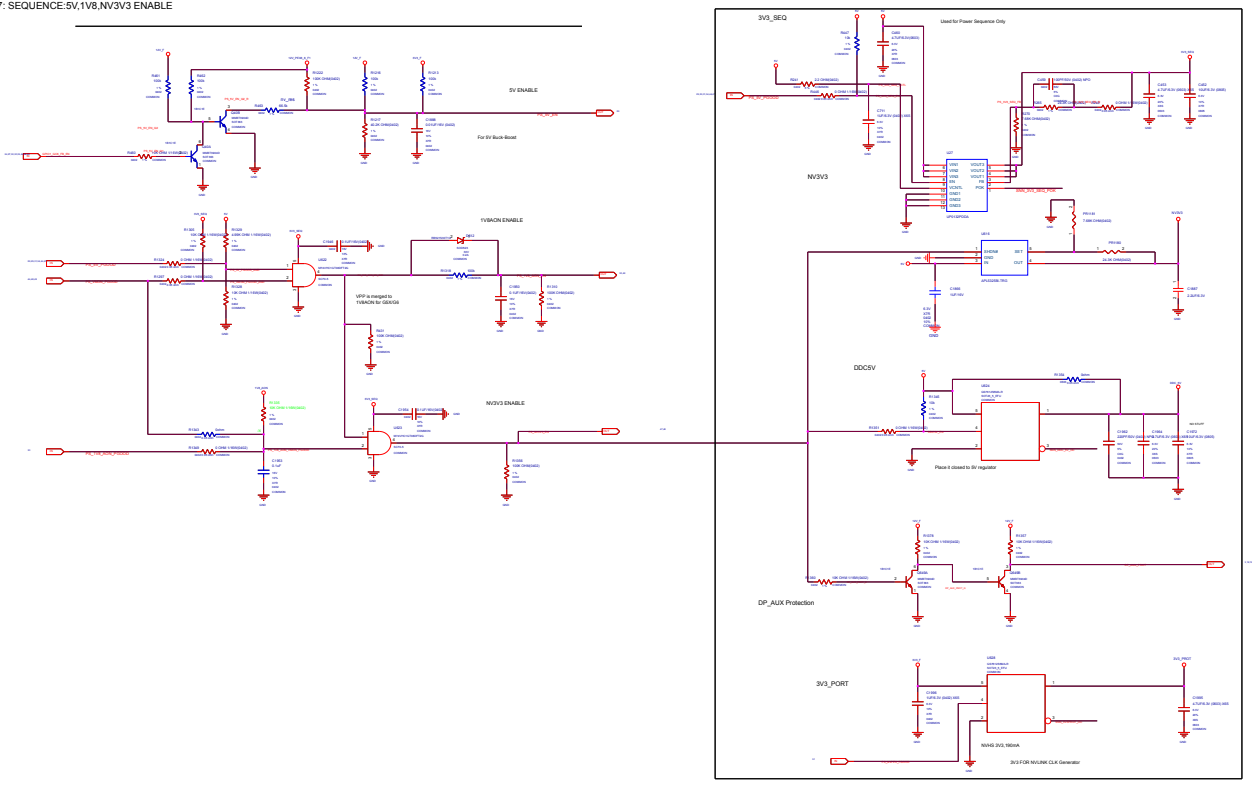


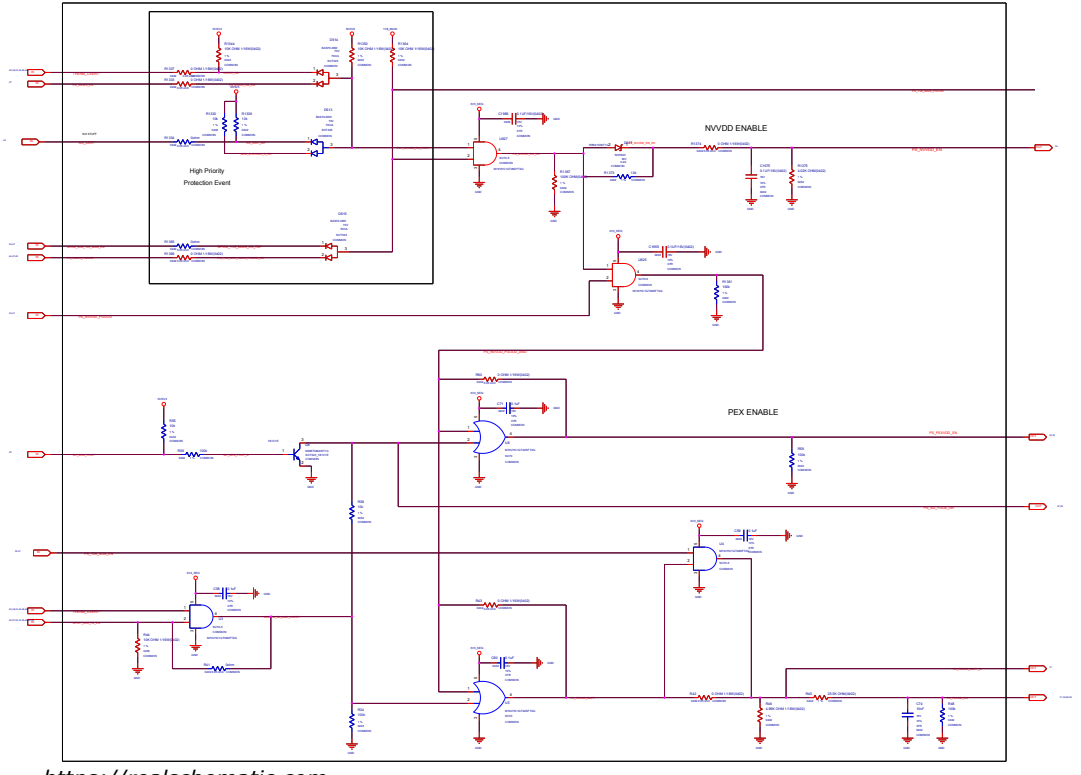


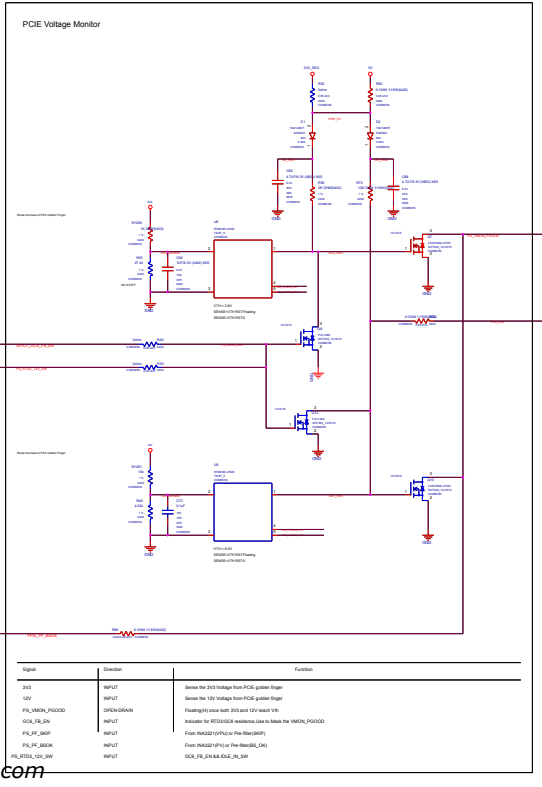












Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(Hi) once both 3V3 and 12V reach Vth
GCIL_FB_EN	INPUT	Indicator for RTD3/GCIL residence.Use to Mask the VMON_PGOOD
PS_PF_2A3P	INPUT	From INA3221(VPU) or Pre-filter(3A3P)
PS_PF_B3OK	INPUT	From INA3221(PV) or Pre-filter(B3_OK)
PS_RTD3_12V_SW	INPUT	GCIL_FB_EN && !DLE_IN_SW

BOM Configuration

OPTIONS	PEXIN3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

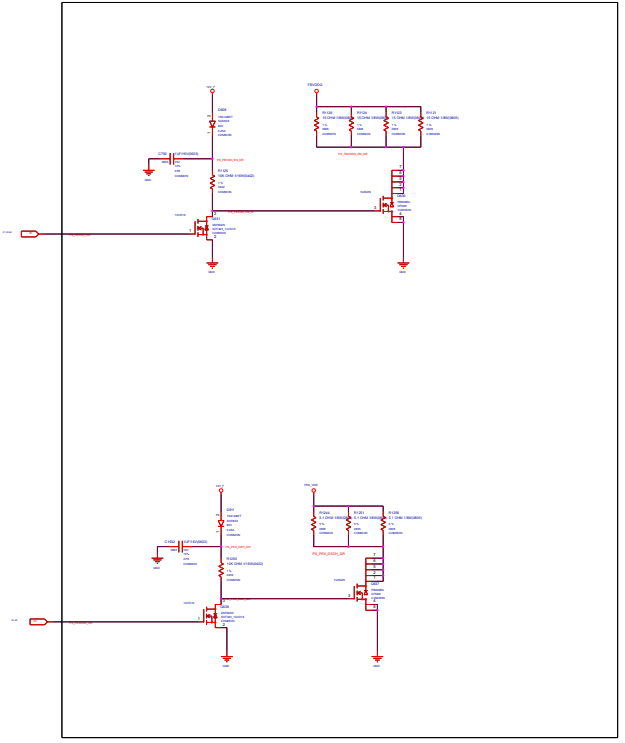
INA3221:3V3_SEQ

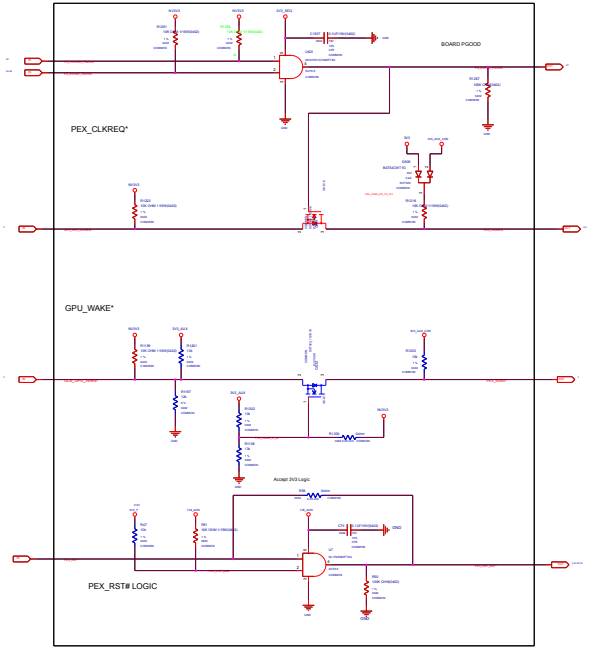
Pre_Filter(ADC_MUX):3V3(PEX)

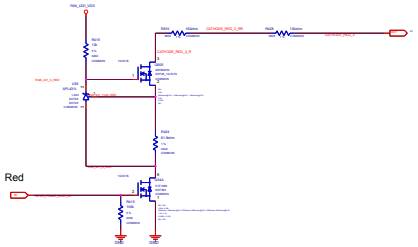
Dual Pre-Filter case:

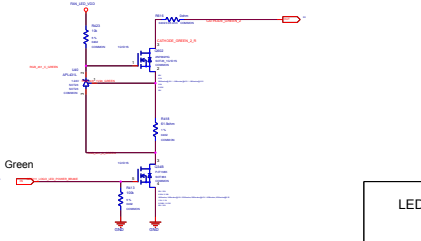
Only use the Primary Pre-Filter to sense 3V3PEX

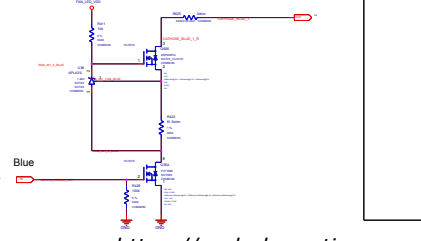
and All Input 12Vs

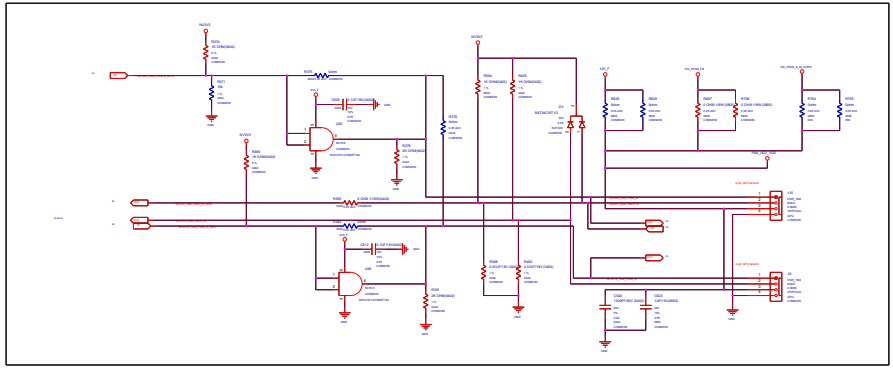


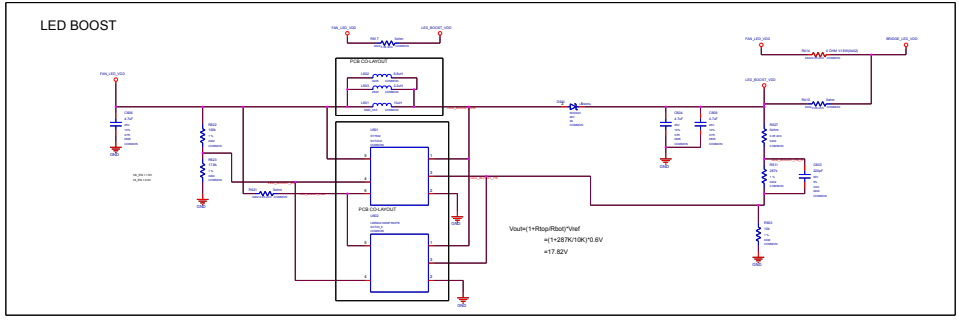


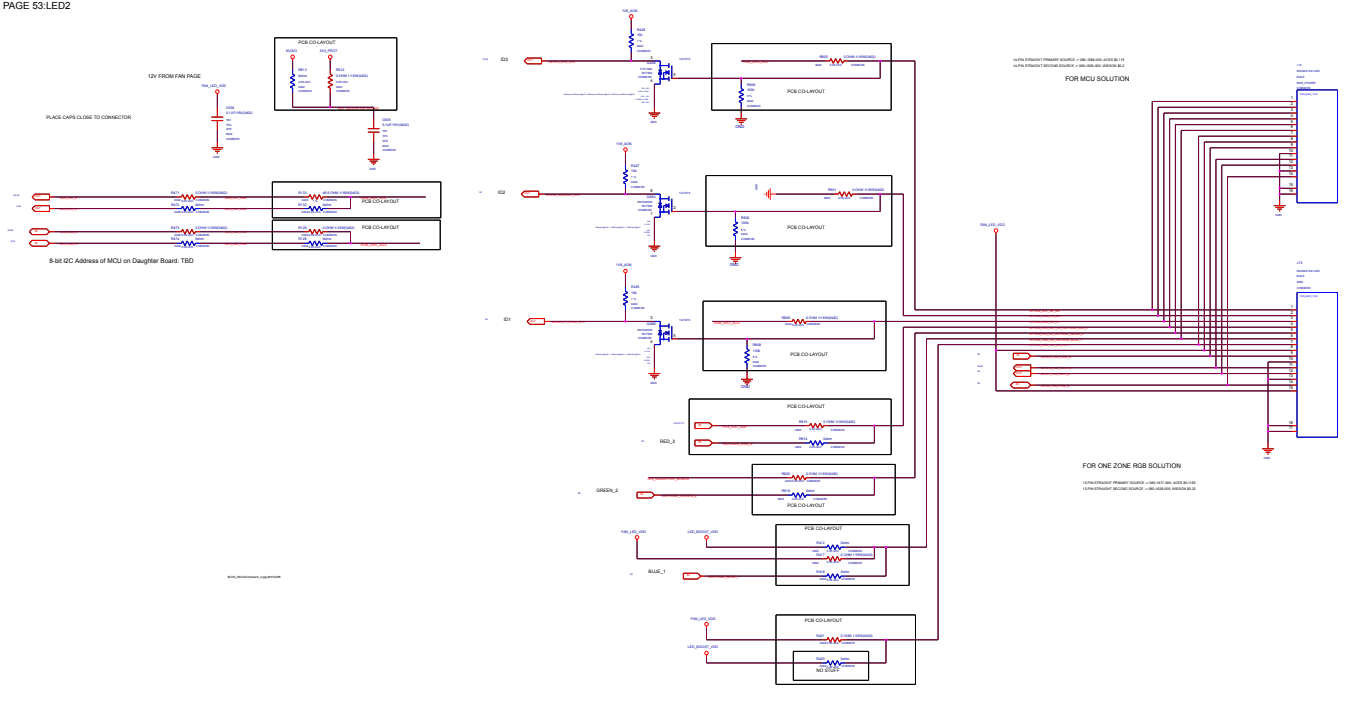










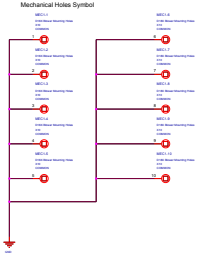


Brackets:

Bracket Screw

STIFFENER

Mechanical Holes Symbol



GPU Socket Symbol