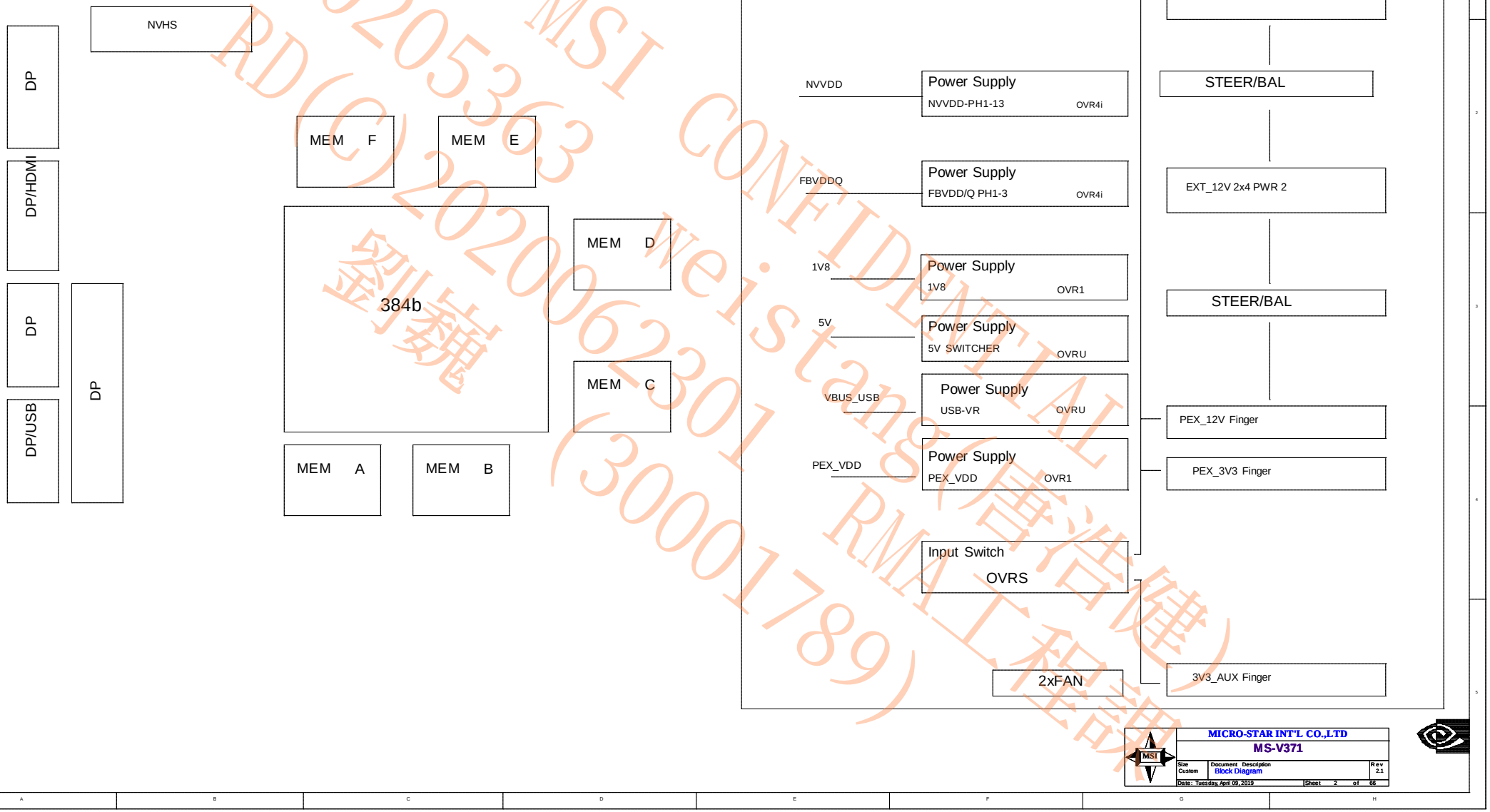
PG150-C03

384b GDDR6 x16
TALL DP + DP + DP + HDMI/DP + USB

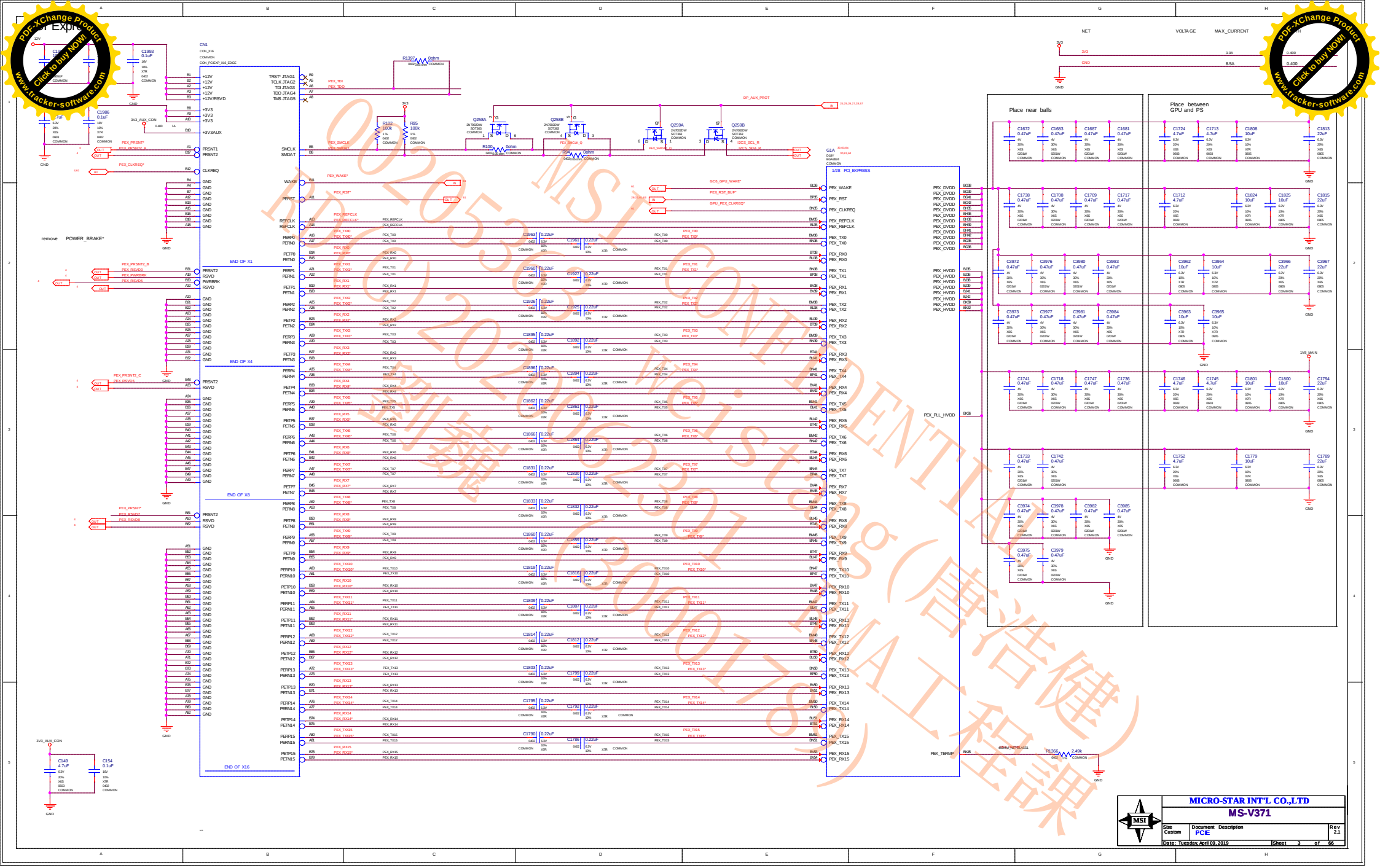
TABLE OF CONTENTS

MICRO-STAR INT'L CO.,LTD
MS-V371
Size: Custom | Document Description: TABLE | Rev: 2.1
Date: Tuesday, April 09, 2019 | Sheet 1 of 66

Block Diagram



MICRO-STAR INT'L CO.,LTD		
MS-V371		
Size: Custom	Document Description: Block Diagram	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 2 of 66	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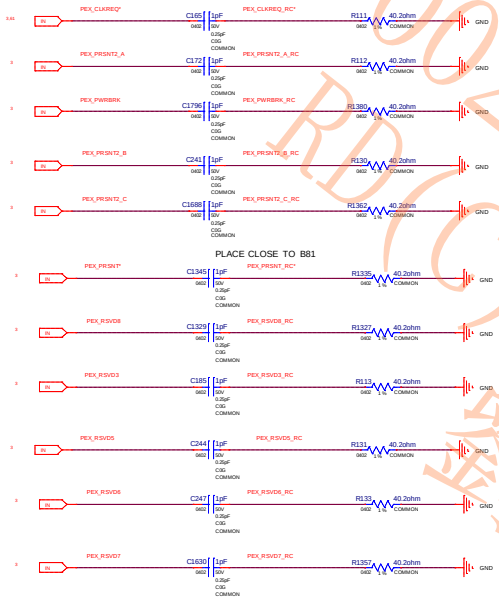
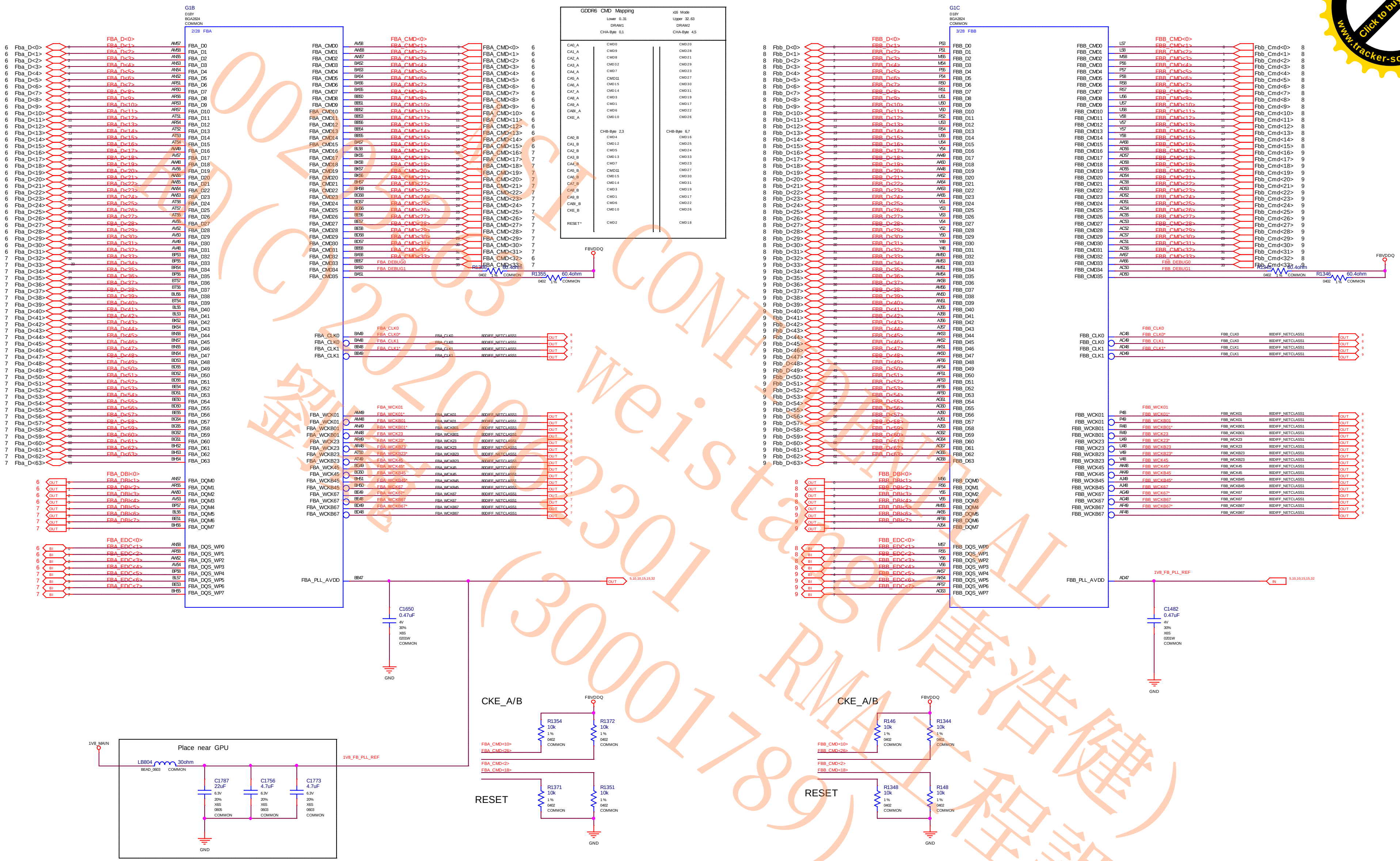
CN1
CON_X16
COMMON
CON_PCIEXP_X16_EDGE
END OF X1
END OF X4
END OF X8
END OF X16
remove POWER_BRAKE*
G1A
1128 PCI_EXPRESS
NET
VOLTAGE
MAX_CURRENT
Place near balls
Place between GPU and PS
MICRO-STAR INT'L CO.,LTD
MS-V371
Size Custom
Document Description PCE
Rev 2.1
Date: Tuesday, April 09, 2019
Sheet 3 of 66

PCI TERM



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V371	
Size: Custom	Document Description: PCIE TERM	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 4 of 66	

MEMORY: GPU Partition A/B



MICRO-STAR INT'L CO.,LTD	
MS-V371	
Size: Custom	Document Description: MEMORY: GPU Partition A/B
Rev: 2.1	
Date: Tuesday, April 09, 2019	Sheet 5 of 66

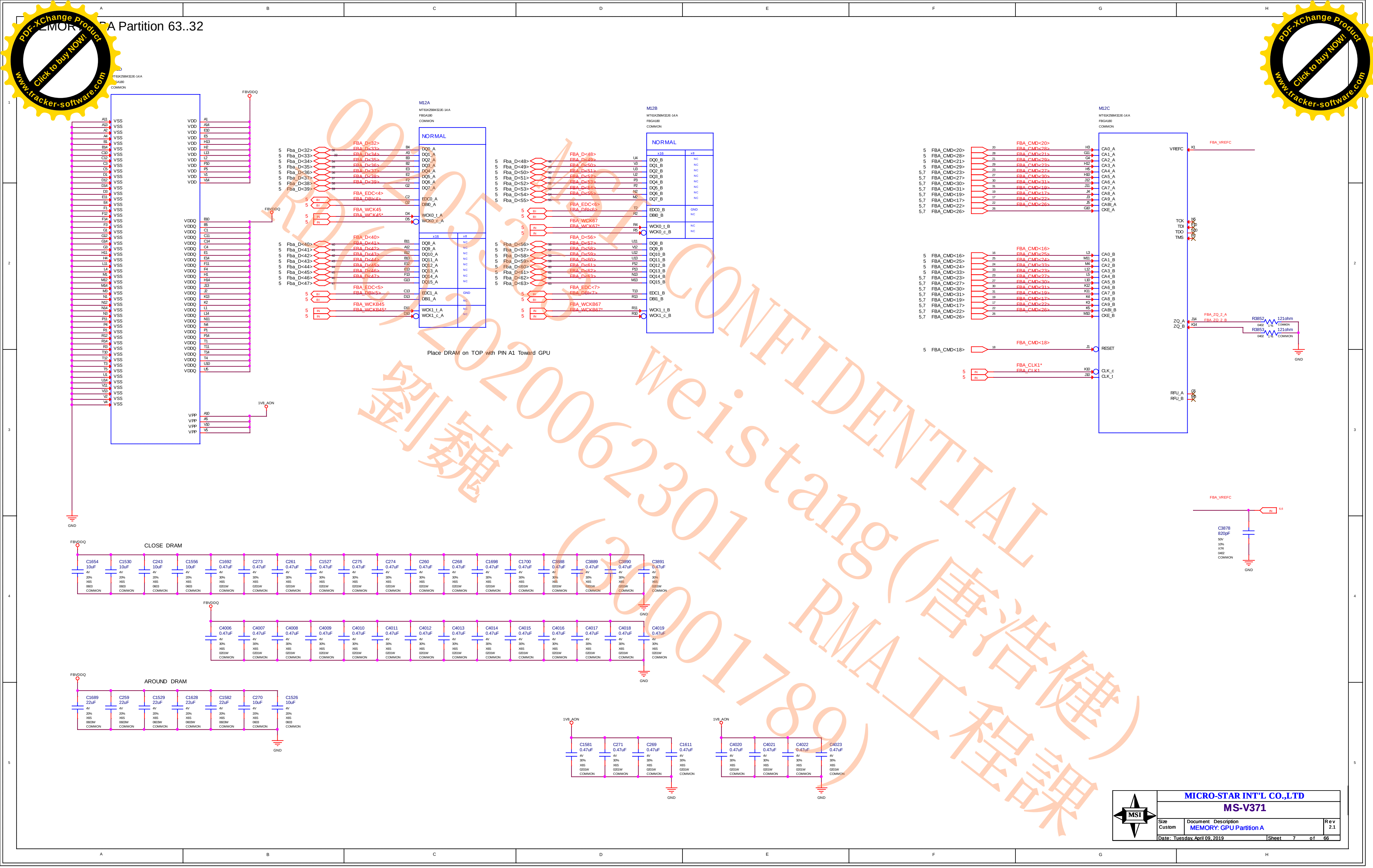
MICRO-STAR INT'L CO.,LTD

MS-V371

Size	Document Description	Rev
Custom	MEM_A	2.1

Date: Tuesday, April 09, 2019 Sheet 5 of 66

MEMORY: GPU Partition 63..32



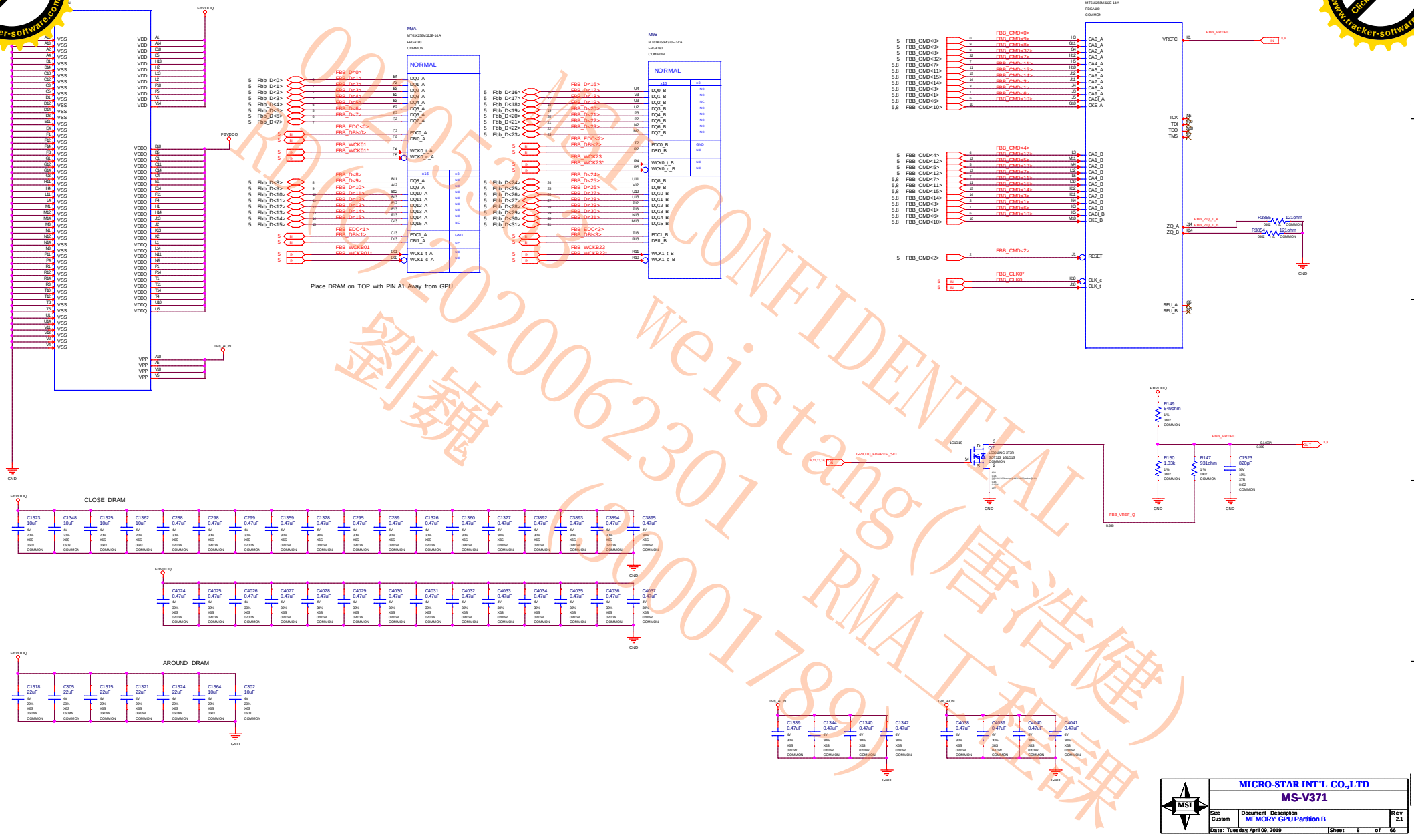
MICRO-STAR INT'L CO.,LTD

MS-V371

Size	Document Description	Rev
Custom	MEMORY: GPU Partition A	2.1

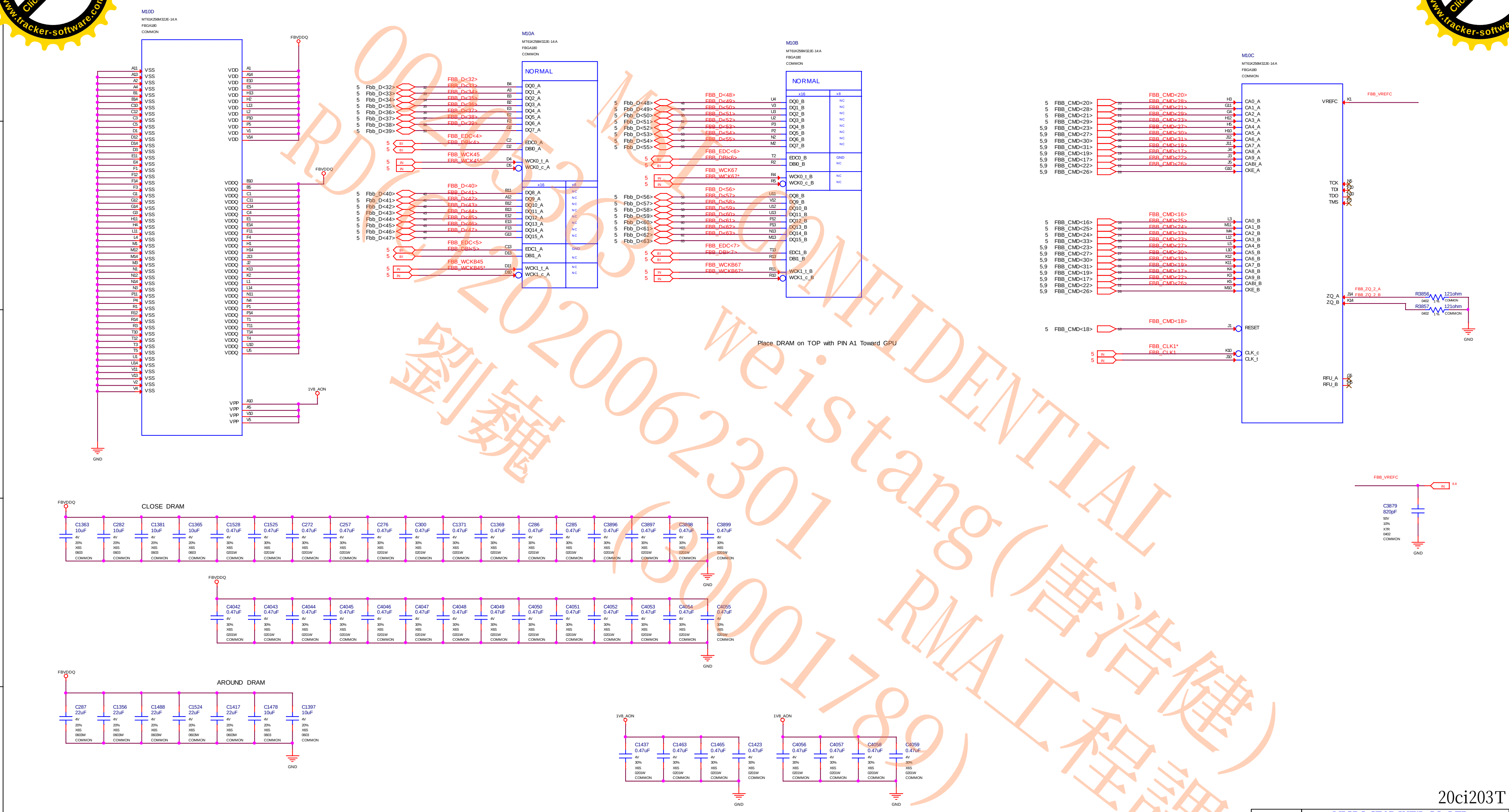
Date: Tuesday, April 09, 2019 Sheet 7 of 66

MEMORY: FBB Partition 31..0



MICRO-STAR INT'L CO.,LTD		
MS-V371		
Size: Custom	Document Description: MEMORY: GPU Partition B	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 8 of 66	

MEMORY: 3B Partition 63..32



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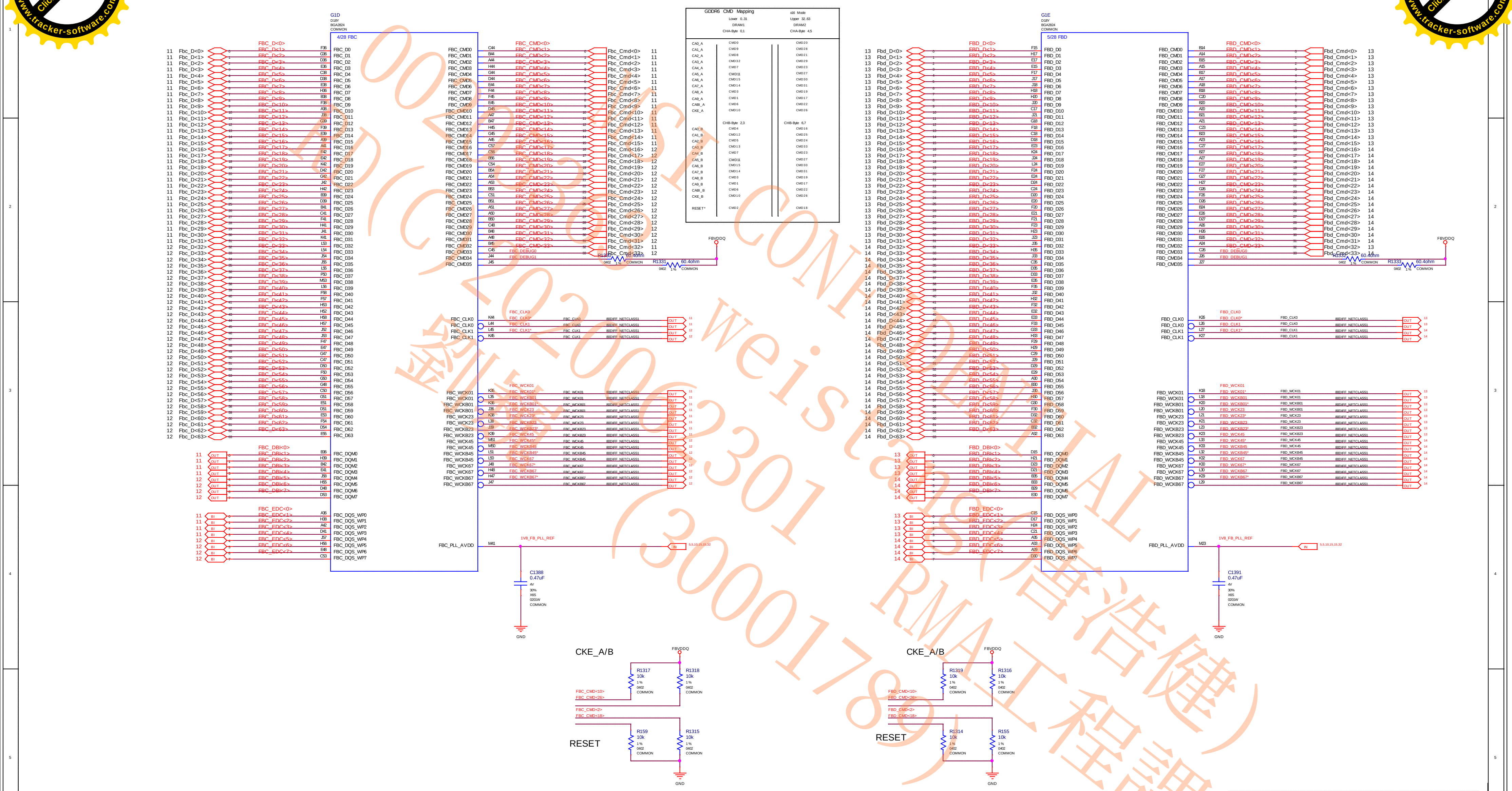
MICRO-STAR INT'L CO.,LTD

MS-V371

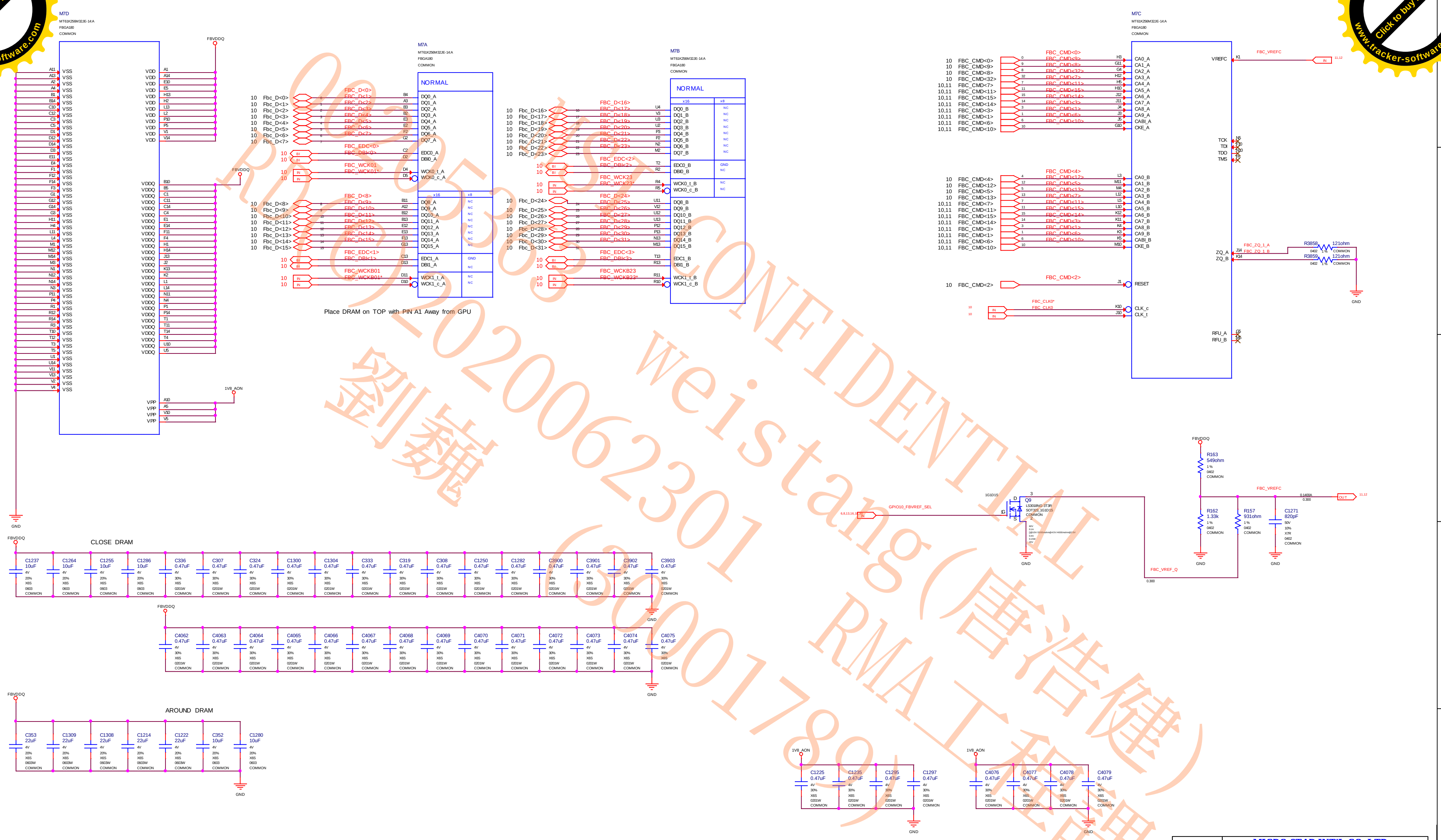
Size	Document Description	Rev
Custom	MEMORY: GPU Partition B	2.1

Date: Tuesday, April 09, 2019 | Sheet 9 of 66



MICRO-STAR INT'L CO.,LTD		
MS-V371		
Size: Custom	Document Description: MEMORY: GPU Partition C/D	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 10 of 66	

MEMORY: ...C Partition 31..0



M7D
MT61K256M32JE-14:A
FBGA180
COMMON
FBVDDQ
VSS
VDD
VDDQ
VPP
1V8_AON
GND
M7A
NORMAL
Fbc_D<0>
Fbc_D<7>
FBC_EDC<0>
FBC_DBI<0>
FBC_WCK01
FBC_WCK01*
DQ0_A
EDC0_A
DBI0_A
WCK0_t_A
WCK0_c_A
FBC_D<8>
FBC_D<15>
FBC_EDC<1>
FBC_DBI<1>
FBC_WCKB01
FBC_WCKB01*
M7B
Fbc_D<16>
Fbc_D<31>
FBC_EDC<2>
FBC_DBI<2>
FBC_WCK23
FBC_WCK23*
FBC_EDC<3>
FBC_DBI<3>
FBC_WCKB23
FBC_WCKB23*
Place DRAM on TOP with PIN A1 Away from GPU
M7C
FBC_CMD<0>
FBC_CMD<10>
CA0_A
CKE_A
VREFC
FBC_VREFC
TCK
TDI
TDO
TMS
CA0_B
CKE_B
ZQ_A
ZQ_B
FBC_ZQ_1_A
FBC_ZQ_1_B
R3858
121ohm
R3859
121ohm
FBC_CMD<2>
RESET
FBC_CLK0*
FBC_CLK0
CLK_c
CLK_t
RFU_A
RFU_B
R163
549ohm
Q9
GPIO10_FBVREF_SEL
R162
1.33k
R157
931ohm
C1271
820pF
FBC_VREF_Q
CLOSE DRAM
C1237
10uF
C1264
10uF
C1255
10uF
C1286
10uF
C336
0.47uF
C307
0.47uF
C324
0.47uF
C1300
0.47uF
C1304
0.47uF
C333
0.47uF
C319
0.47uF
C308
0.47uF
C1250
0.47uF
C1282
0.47uF
C3900
0.47uF
C3901
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C3902
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C3903
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C4070
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C4071
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C4072
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C4073
0.47uF
C4074
0.47uF
C4075
0.47uF
AROUND DRAM
C353
22uF
C1309
22uF
C1308
22uF
C1214
22uF
C1222
22uF
C352
10uF
C1280
10uF
C1225
0.47uF
C1235
0.47uF
C1295
0.47uF
C1297
0.47uF
C4076
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C4077
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C4078
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C4079
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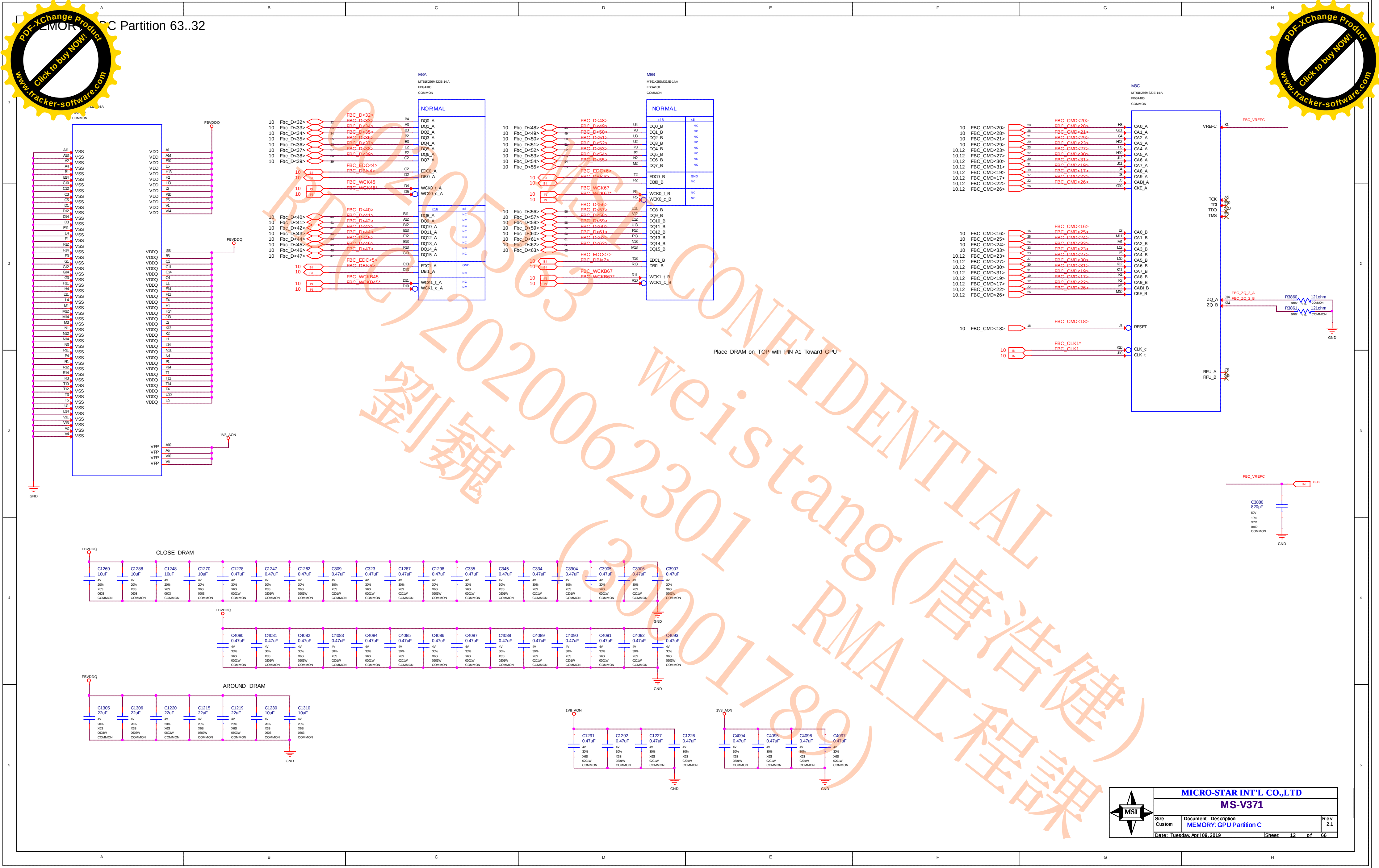
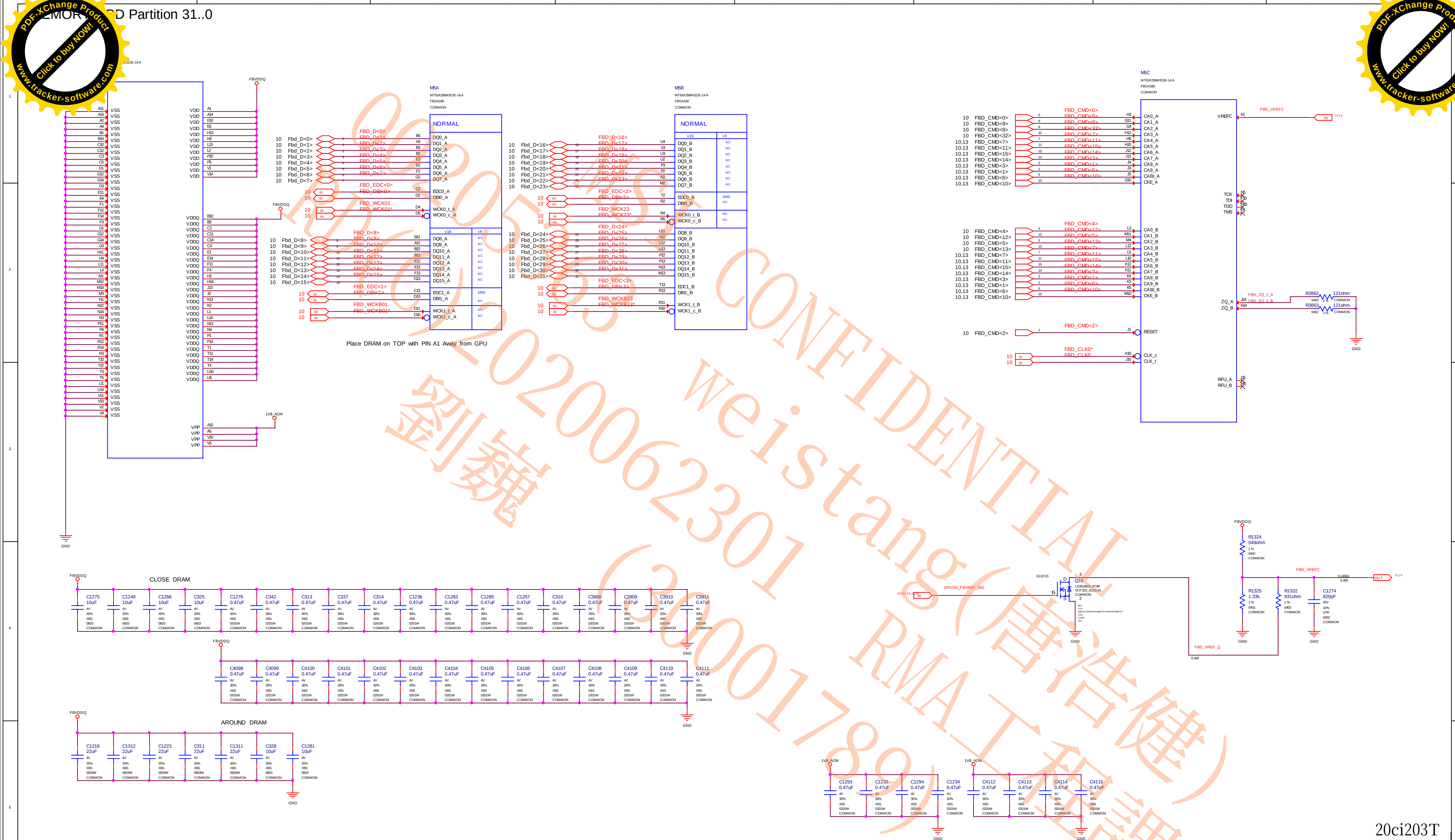
MICRO-STAR INT'L CO.,LTD

MS-V371

Size	Document Description	Rev
Custom	MEMORY: GPU Partition C	2.1

Date: Tuesday, April 09, 2019 Sheet 11 of 66





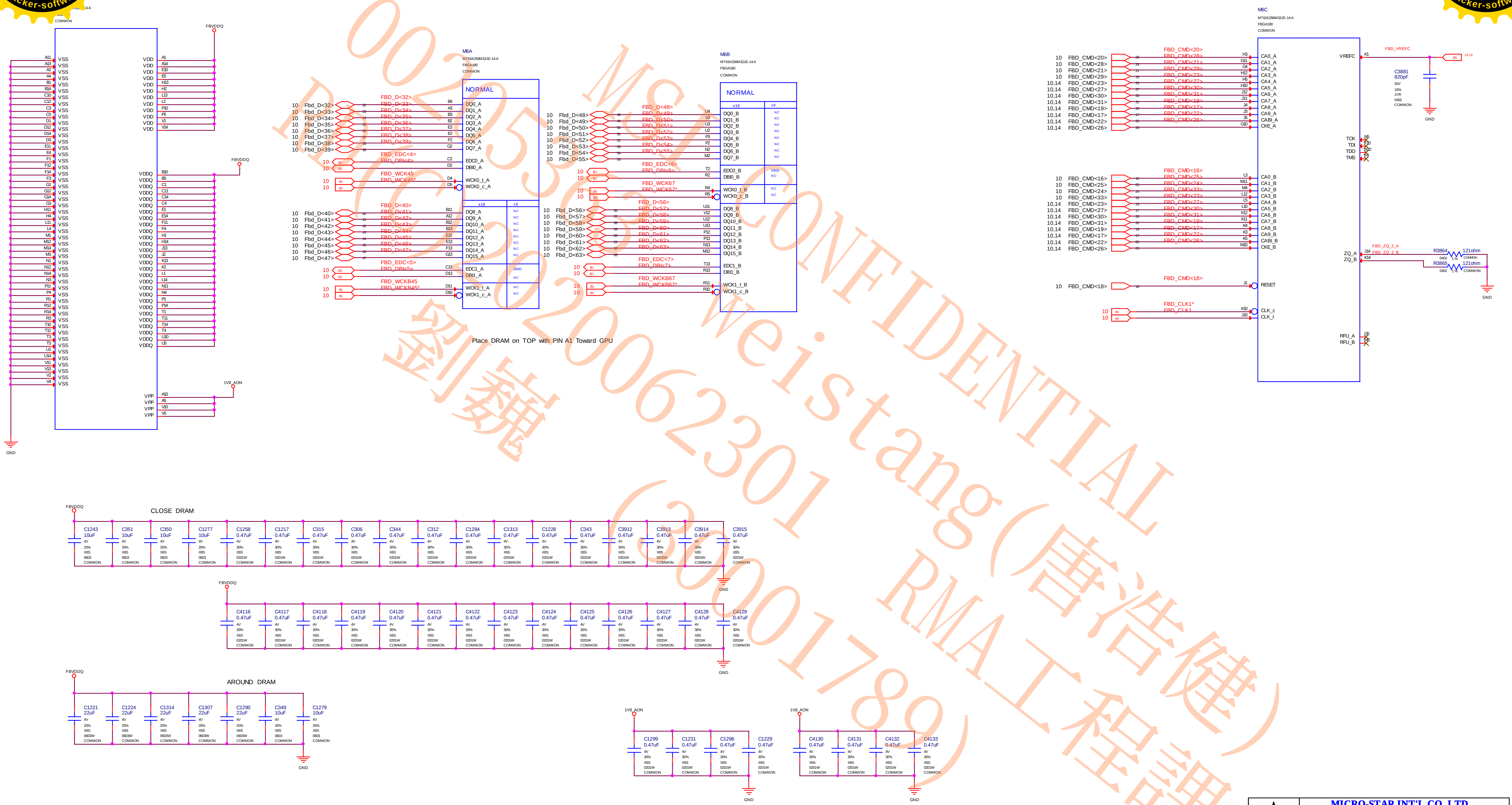
MICRO-STAR INT'L CO.,LTD

MS-V371

Size	Document Description	Rev
Custom	MEMORY: GPU Partition D	2.1

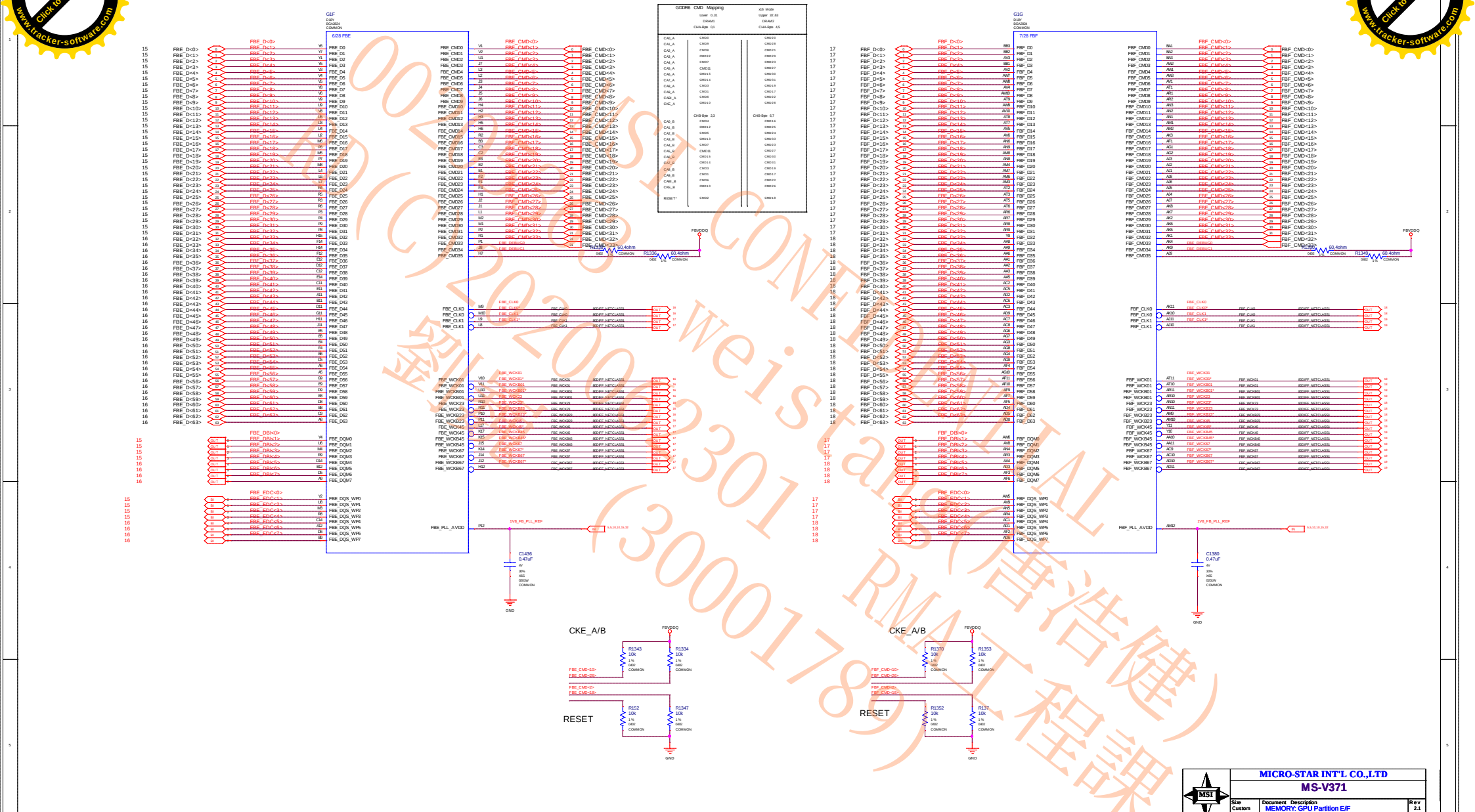
Date: Tuesday, April 09, 2019 Sheet 13 of 66

MEMORY: GPU Partition 63..32



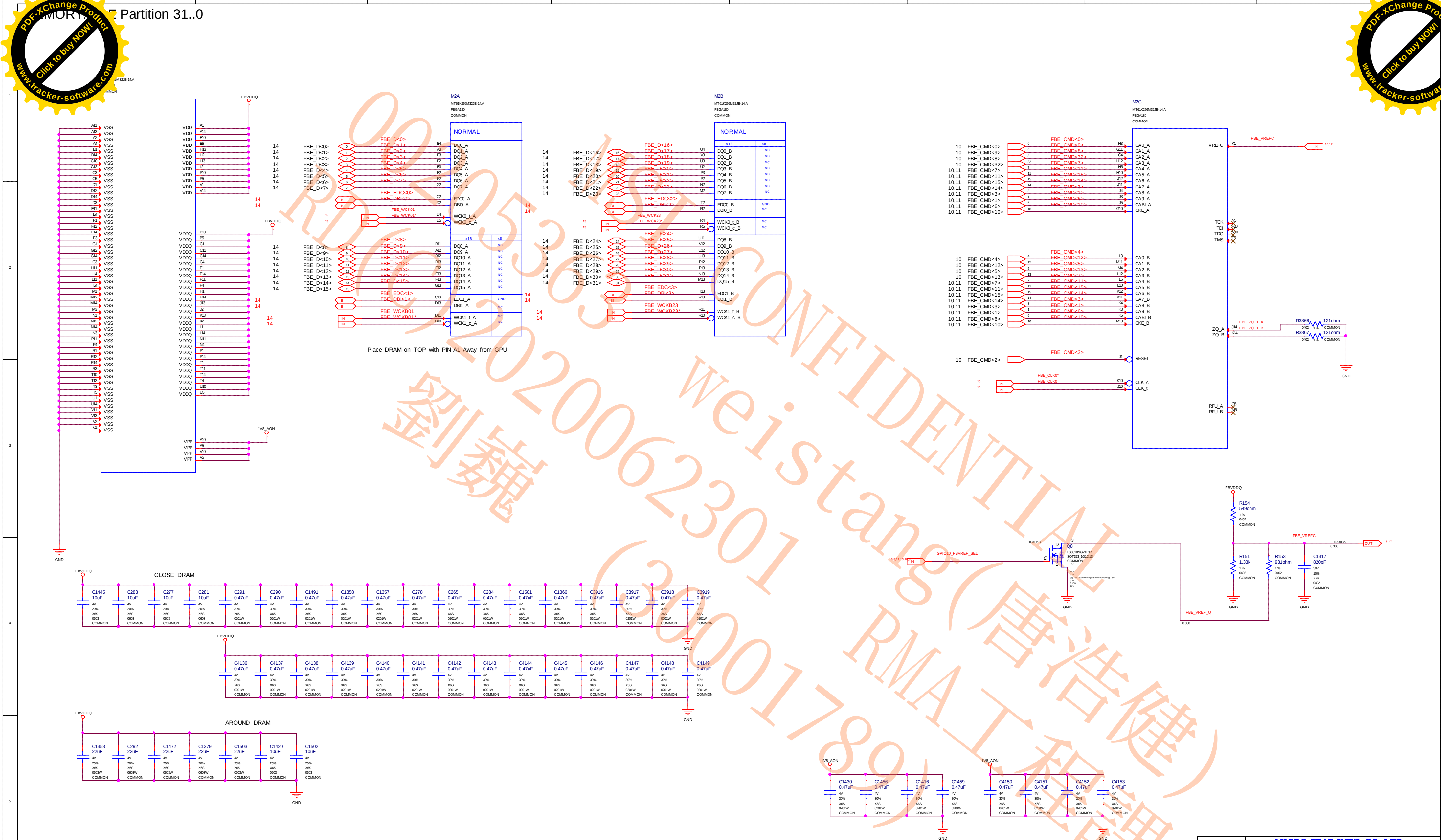
MICRO-STAR INT'L CO.,LTD		
MS-V371		
Size: Custom	Document Description: MEMORY: GPU Partition C/D	Rev 2.1
Date: Tuesday, April 09, 2019	Sheet 14 of 66	

MEMORY: GPU Partition E/F



MICRO-STAR INT'L CO.,LTD	
MS-V371	
Size: Custom	Document Description: MEMORY: GPU Partition E/F
Rev: 2.1	
Date: Tuesday, April 09, 2019	Sheet 15 of 66

MEMORY: E Partition 31..0



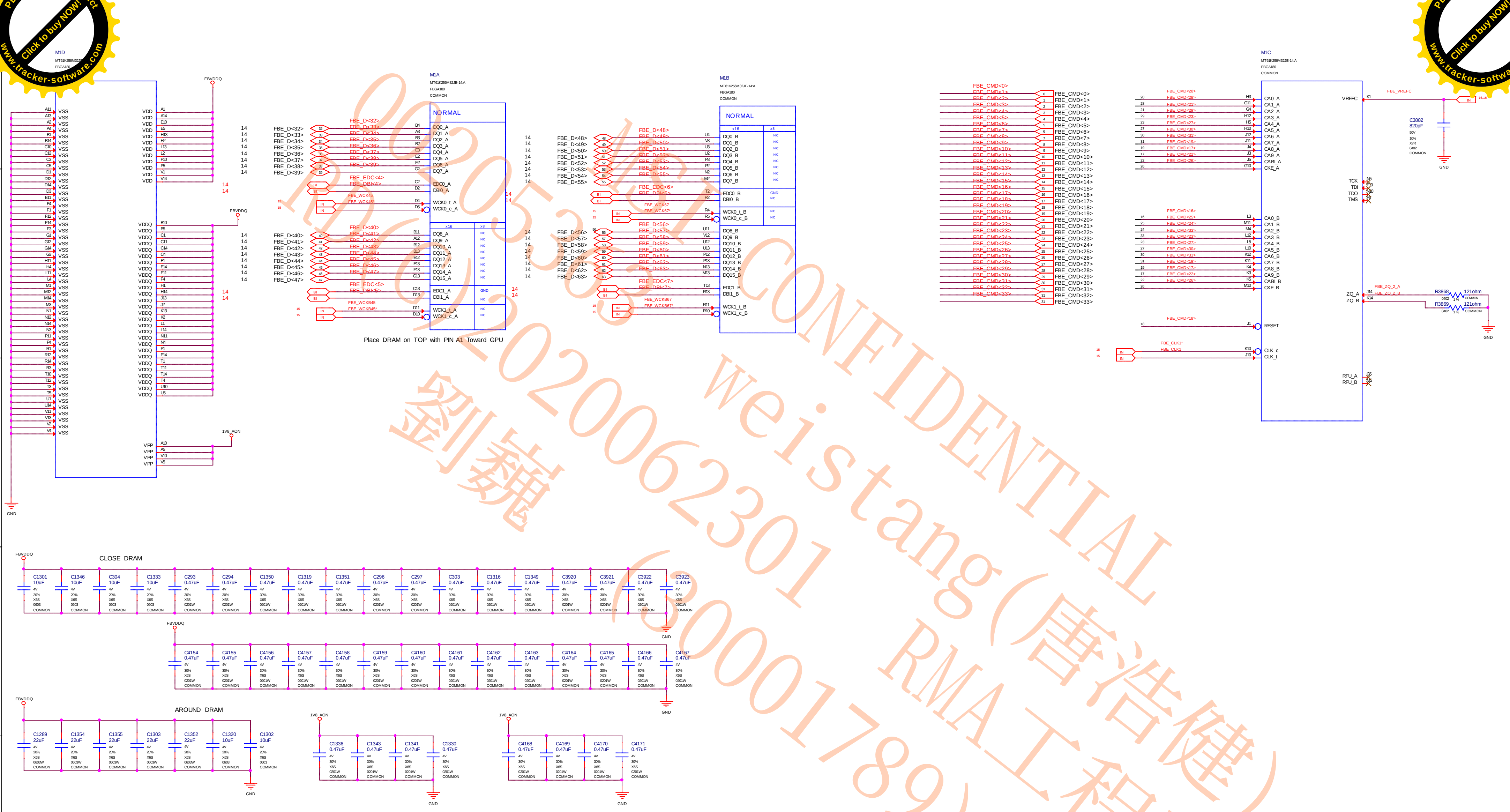
MICRO-STAR INT'L CO.,LTD

MS-V371

Size	Document Description	Rev
Custom	MEMORY: GPU Partition E/F	2.1

Date: Tuesday, April 09, 2019 Sheet 16 of 66

MEMORY: GPU Partition E Partition 63..32


M1D
M1A
M1B
M1C
NORMAL
FBVDDQ
1V8_AON
GND
VSS
VDD
VDDQ
VPP
FBE_D<32> … FBE_D<63>
FBE_EDC<4> FBE_EDC<5> FBE_EDC<6> FBE_EDC<7>
FBE_DBI<4> FBE_DBI<5> FBE_DBI<6> FBE_DBI<7>
FBE_WCK45 FBE_WCK45*
FBE_WCK67 FBE_WCK67*
FBE_CMD<0> … FBE_CMD<33>
FBE_VREF
FBE_CLK1 FBE_CLK1*
FBE_ZQ_2_A FBE_ZQ_2_B
VREFC
RESET
CLK_c
CLK_t
ZQ_A
ZQ_B
TCK TDI TDO TMS
RFU_A RFU_B
C3882 820pF
R3868 121ohm
R3869 121ohm
Place DRAM on TOP with PIN A1 Toward GPU
CLOSE DRAM
AROUND DRAM
C1301 10uF
C1346 10uF
C304 10uF
C1333 10uF
C293 0.47uF
C294 0.47uF
C1350 0.47uF
C1319 0.47uF
C1351 0.47uF
C296 0.47uF
C297 0.47uF
C303 0.47uF
C1316 0.47uF
C1349 0.47uF
C3920 0.47uF
C3921 0.47uF
C3922 0.47uF
C3923 0.47uF
C4154 0.47uF
C4155 0.47uF
C4156 0.47uF
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C4160 0.47uF
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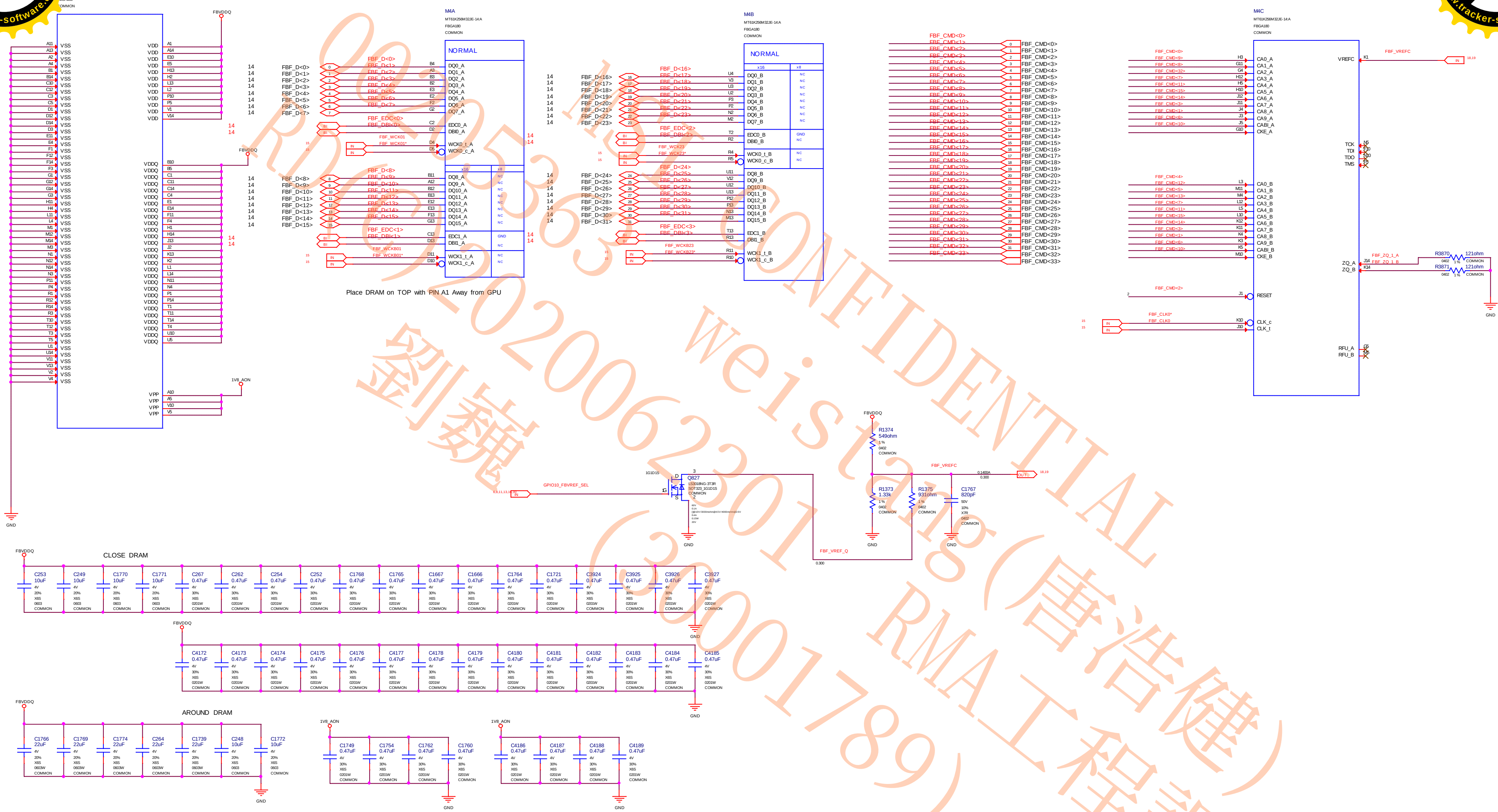
C4162 0.47uF
C4163 0.47uF
C4164 0.47uF
C4165 0.47uF
C4166 0.47uF
C4167 0.47uF
C1289 22uF
C1354 22uF
C1355 22uF
C1303 22uF
C1352 22uF
C1320 10uF
C1302 10uF
C1336 0.47uF
C1343 0.47uF
C1341 0.47uF
C1330 0.47uF
C4168 0.47uF
C4169 0.47uF
C4170 0.47uF
C4171 0.47uF

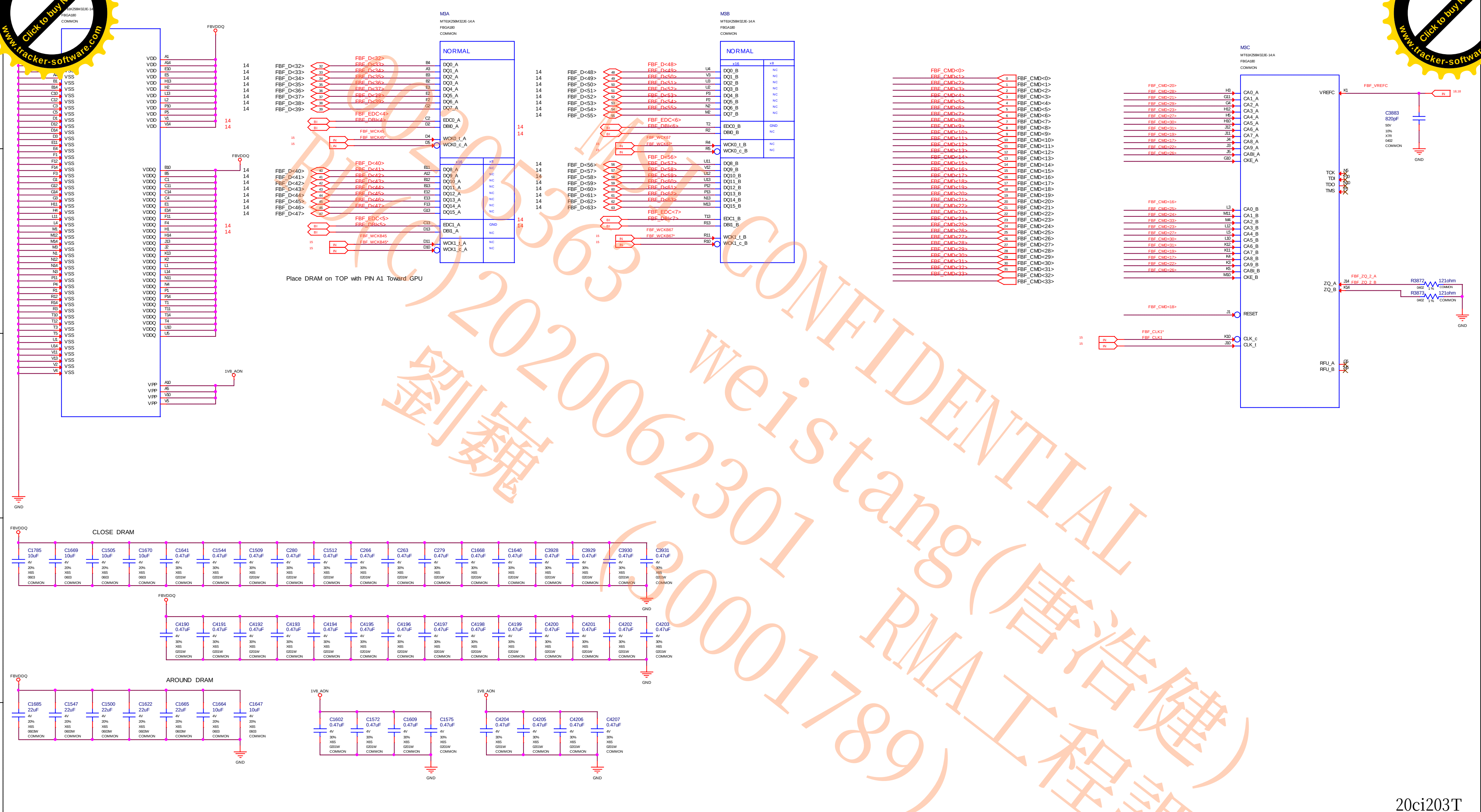
MICRO-STAR INT'L CO.,LTD		
MS-V371		
Size: Custom	Document Description: MEMORY: GPU Partition E	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 17 of 66	

MEMORY: GPU Partition 31..0



MICRO-STAR INT'L CO.,LTD	
MS-V371	
Size: Custom	Document Description: MEMORY: GPU Partition F
Rev: 2.1	
Date: Tuesday, April 09, 2019	Sheet 18 of 66

MEMORY: F Partition 63..32

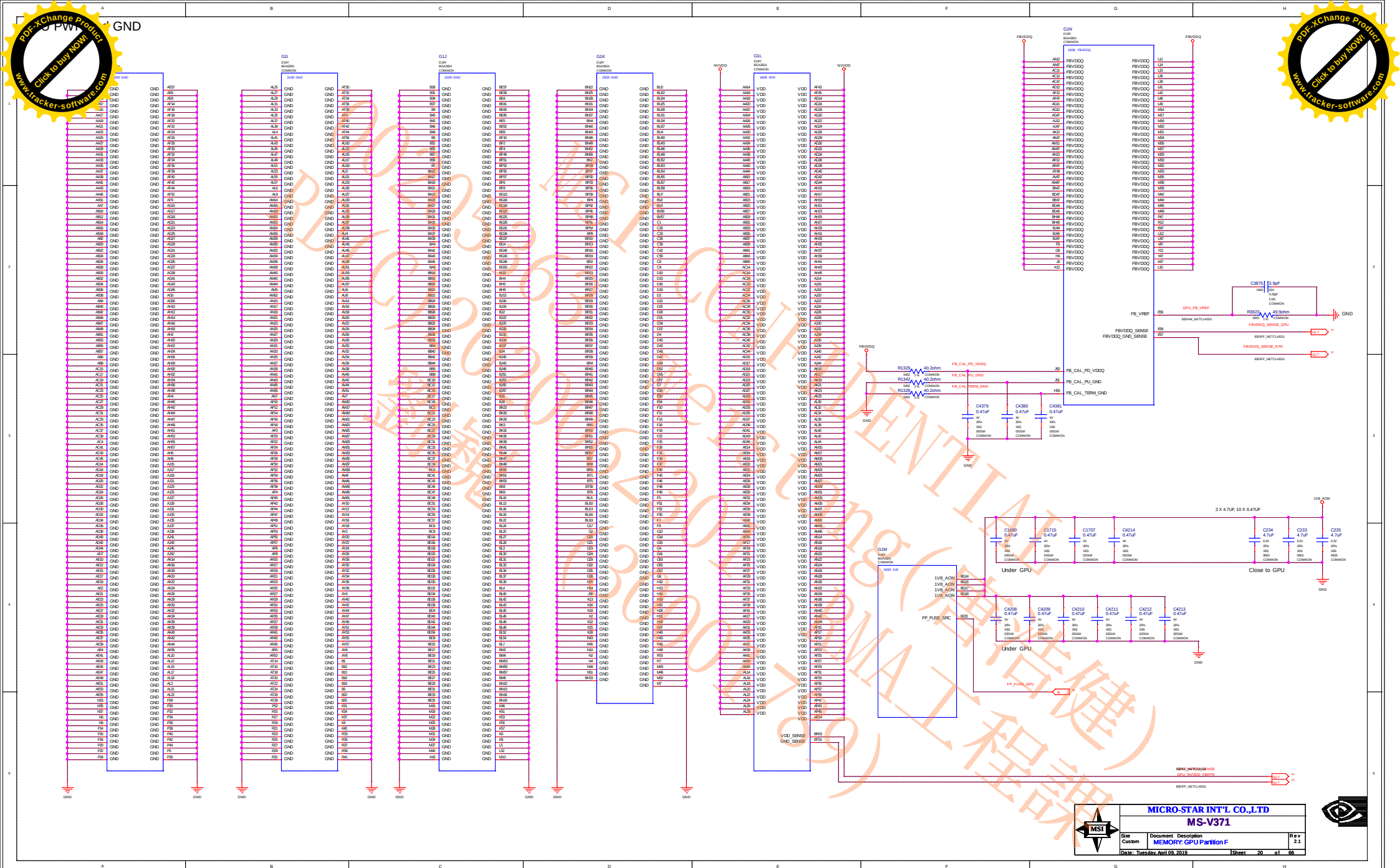


20ci203T

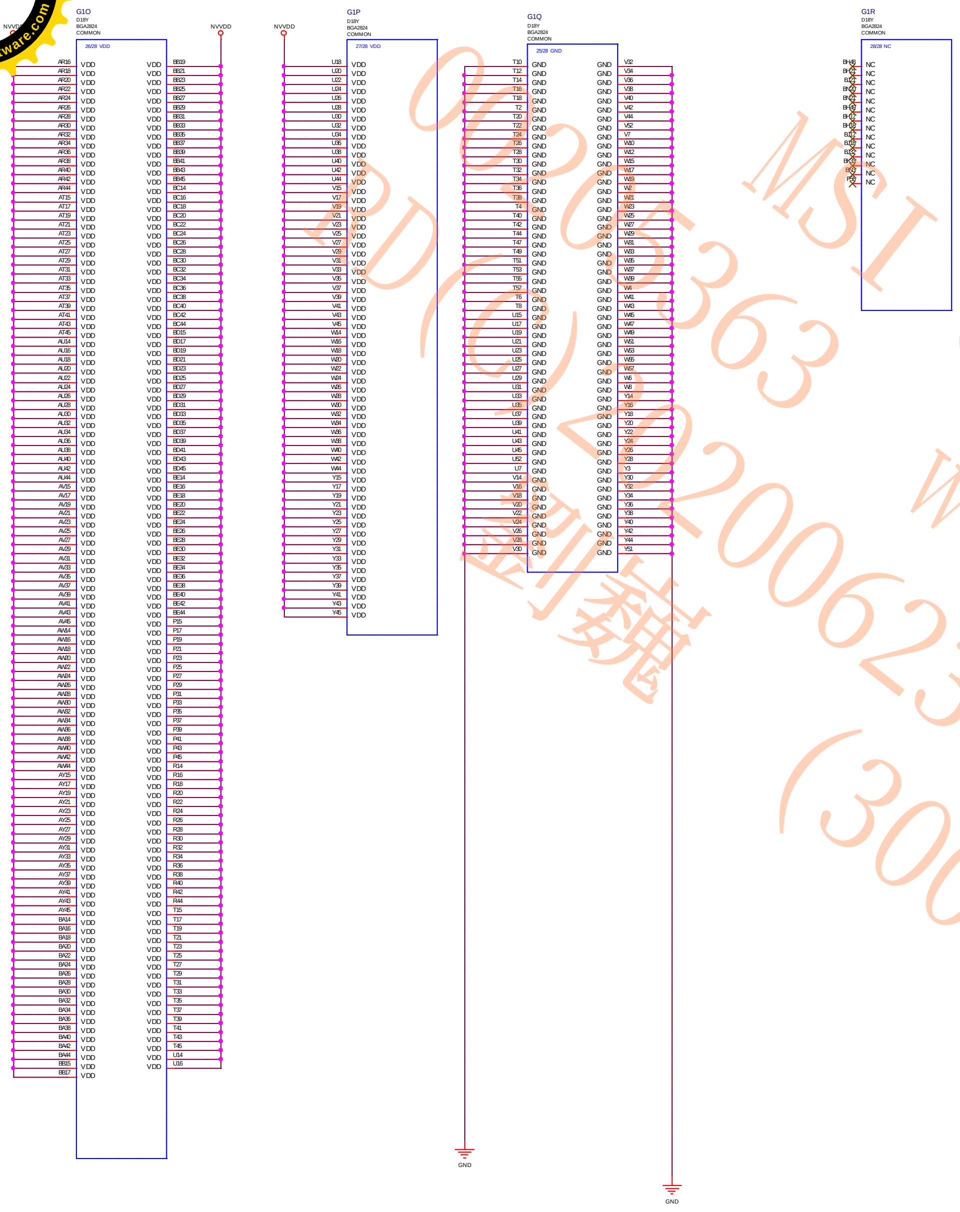
MICRO-STAR INT'L CO.,LTD
MS-V371

Size	Document Description	Rev
Custom	MEMORY: GPU Partition F	2.1

Date: Tuesday, April 09, 2019 Sheet 19 of 66



GPU PWR AND NCs



MICRO-STAR INT'L CO.,LTD	
MS-V371	
Size: Custom	Document Description: GPU PWR GND
Rev: 2.1	
Date: Tuesday, April 09, 2019	Sheet 21 of 66

5 Decoupling

FBVDDQ

Partition A — 2 X 10UF, 6 X 0.47UF

C1704 0.47uF, C1583 0.47uF, C1599 0.47uF, C1557 0.47uF, C1555 0.47uF, C1639 10uF, C1734 10uF

Partition B — 2 X 10UF, 6 X 0.47UF

C1508 0.47uF, C1438 0.47uF, C1386 0.47uF, C1457 0.47uF, C1497 0.47uF, C1468 0.47uF, C1534 10uF, C1428 10uF

Partition C — 2 X 10UF, 6 X 0.47UF

C1387 0.47uF, C1374 0.47uF, C1383 0.47uF, C1401 0.47uF, C1375 0.47uF, C1411 0.47uF, C1361 10uF, C1376 10uF

Partition D — 2 X 10UF, 6 X 0.47UF

C1392 0.47uF, C1368 0.47uF, C1373 0.47uF, C1367 0.47uF, C1382 0.47uF, C1385 0.47uF, C1378 10uF, C1384 10uF

Partition E — 2 X 10UF, 6 X 0.47UF

C1427 0.47uF, C1443 0.47uF, C1418 0.47uF, C1458 0.47uF, C1393 0.47uF, C1370 0.47uF, C1398 10uF, C1464 10uF

Partition F — 2 X 10UF, 6 X 0.47UF

C1568 0.47uF, C1473 0.47uF, C1587 0.47uF, C1507 0.47uF, C1545 0.47uF, C1489 0.47uF, C1629 10uF, C1579 10uF

Place close to GPU — 6 X 10UF

C1377 10uF, C1331 10uF, C1372 10uF, C1576 10uF, C1744 10uF, C1347 10uF

Place close to GPU — 14 X 22UF

C1684 22uF, C1334 22uF, C1337 22uF, C1511 22uF, C1553 22uF, C1332 22uF, C1421 22uF

C1470 22uF, C1338 22uF, C1399 22uF, C1439 22uF, C1335 22uF, C1610 22uF, C1607 22uF

NVVDD

NVVDD — 1 X 470UF + 10 X 47UF overlap — PCB CO-LAYOUT

C1577 470uF, C1561 47uF, C1562 47uF, C1592 47uF, C1564 47uF, C1593 47uF, C1567 47uF, C1595 47uF, C1566 47uF, C1596 47uF, C1597 47uF

1 X 470UF + 10 X 47UF overlap — PCB CO-LAYOUT

C1467 470uF, C1479 47uF, C1490 47uF, C1447 47uF, C1485 47uF, C1448 47uF, C1486 47uF, C1452 47uF, C1449 47uF, C1 47uF

12 X 47UF

C1590 47uF, C1591 47uF, C1446 47uF, C1559 47uF, C1563 47uF, C1565 47uF, C1589 47uF, C1487 47uF, C1453 47uF, C1484 47uF, C1451 47uF, C1483 47uF

6 X 22UF

C1455 22uF, C1624 22uF, C1422 22uF, C1434 22uF, C1594 22uF, C1623 22uF

30 X 10UF

C1653 10uF, C1652 10uF, C1651 10uF, C1642 10uF, C1403 10uF, C1514 10uF, C1521 10uF, C1400 10uF, C1515 10uF, C1517 10uF, C1686 10uF, C1615 10uF, C1614 10uF, C1638 10uF, C1636 10uF, C1516 10uF, C1520 10uF, C1519 10uF, C1518 10uF, C1513 10uF

C1645 10uF, C1644 10uF, C1643 10uF, C1677 10uF, C1543 10uF, C1432 10uF, C1620 10uF, C1433 10uF, C1407 10uF, C1536 10uF

16 X 4.7UF

C1541 4.7uF, C1424 4.7uF, C1619 4.7uF, C1429 4.7uF, C1634 4.7uF, C1539 4.7uF, C1617 4.7uF, C1425 4.7uF, C1535 4.7uF, C1537 4.7uF, C1626 4.7uF, C1431 4.7uF, C1542 4.7uF, C1404 4.7uF, C1540 4.7uF, C1538 4.7uF

80 X 0.47UF

C1442 0.47uF, C1462 0.47uF, C1419 0.47uF, C1660 0.47uF, C1510 0.47uF, C1631 0.47uF, C1569 0.47uF, C1532 0.47uF, C1406 0.47uF, C1414 0.47uF, C1627 0.47uF, C1548 0.47uF, C1490 0.47uF, C1408 0.47uF, C1656 0.47uF, C1549 0.47uF, C1454 0.47uF, C1469 0.47uF, C1552 0.47uF, C1533 0.47uF

C1426 0.47uF, C1588 0.47uF, C1410 0.47uF, C1499 0.47uF, C1649 0.47uF, C1655 0.47uF, C1496 0.47uF, C1554 0.47uF, C1475 0.47uF, C1474 0.47uF, C1394 0.47uF, C1676 0.47uF, C1466 0.47uF, C1460 0.47uF, C1635 0.47uF, C1498 0.47uF, C1494 0.47uF, C1570 0.47uF, C1440 0.47uF, C1413 0.47uF

C1412 0.47uF, C1476 0.47uF, C1598 0.47uF, C1603 0.47uF, C1477 0.47uF, C1585 0.47uF, C1571 0.47uF, C1671 0.47uF, C1495 0.47uF, C1573 0.47uF, C1625 0.47uF, C1409 0.47uF, C1461 0.47uF, C1396 0.47uF, C1402 0.47uF, C1441 0.47uF, C1560 0.47uF, C1580 0.47uF, C1613 0.47uF, C1605 0.47uF

C1405 0.47uF, C1658 0.47uF, C1493 0.47uF, C1578 0.47uF, C1435 0.47uF, C1522 0.47uF, C1551 0.47uF, C1444 0.47uF, C1550 0.47uF, C1471 0.47uF, C1604 0.47uF, C1492 0.47uF, C1415 0.47uF, C1546 0.47uF, C1395 0.47uF, C1673 0.47uF, C1601 0.47uF, C1637 0.47uF, C1657 0.47uF, C1584 0.47uF

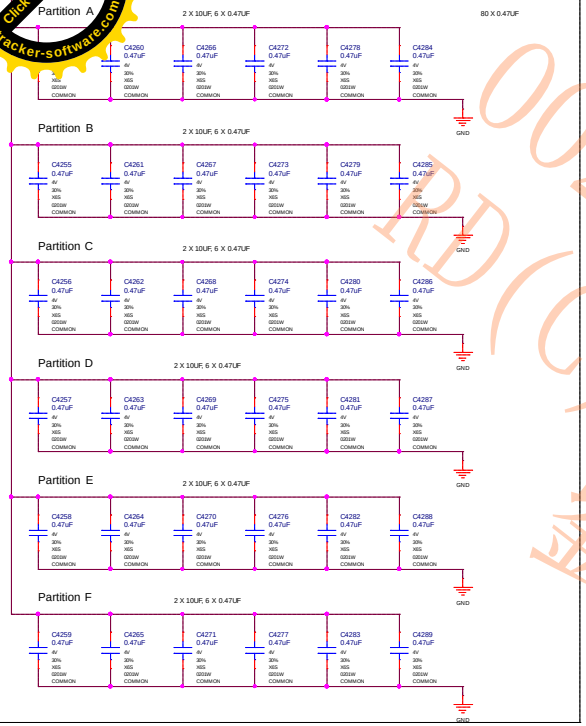
MICRO-STAR INT'L CO.,LTD
MS-V371

Size	Document Description	Rev
Custom	Decoupling	2.1

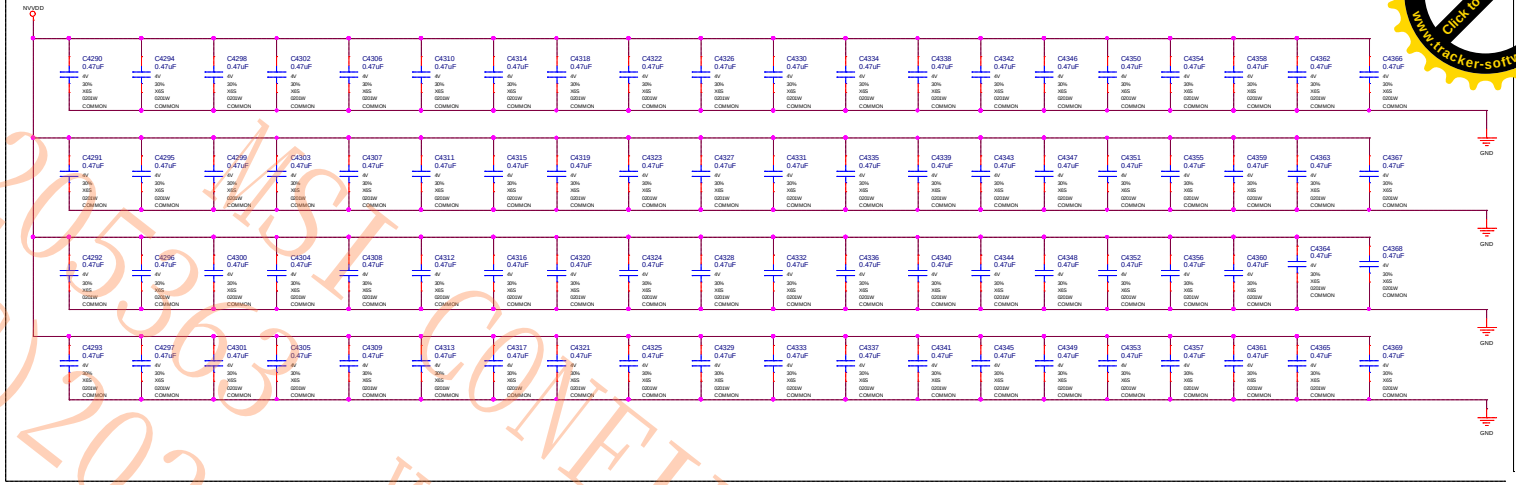
Date: Tuesday, April 09, 2019 Sheet 22 of 66

GPU De[illegible]pling

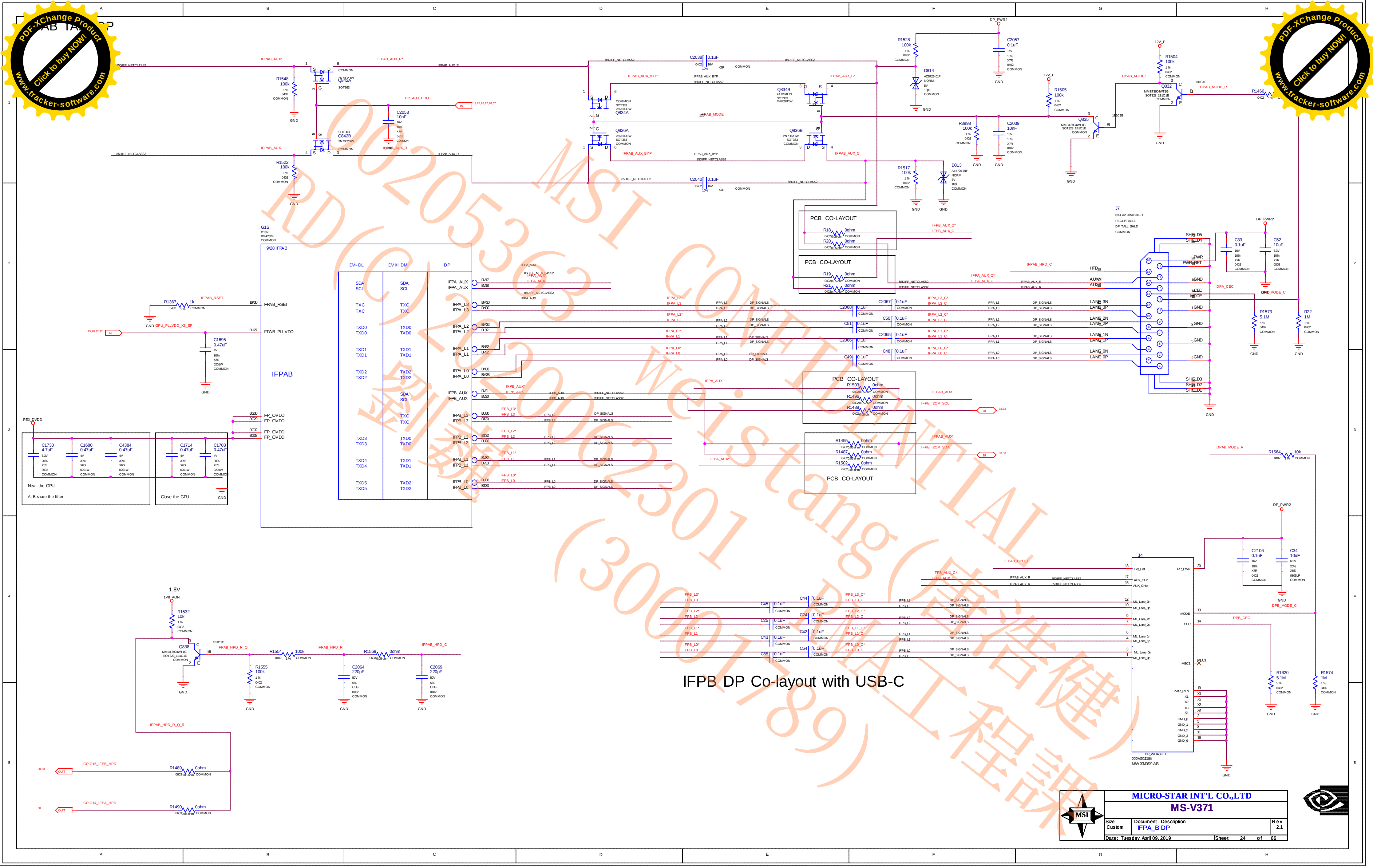
FBVDDQ

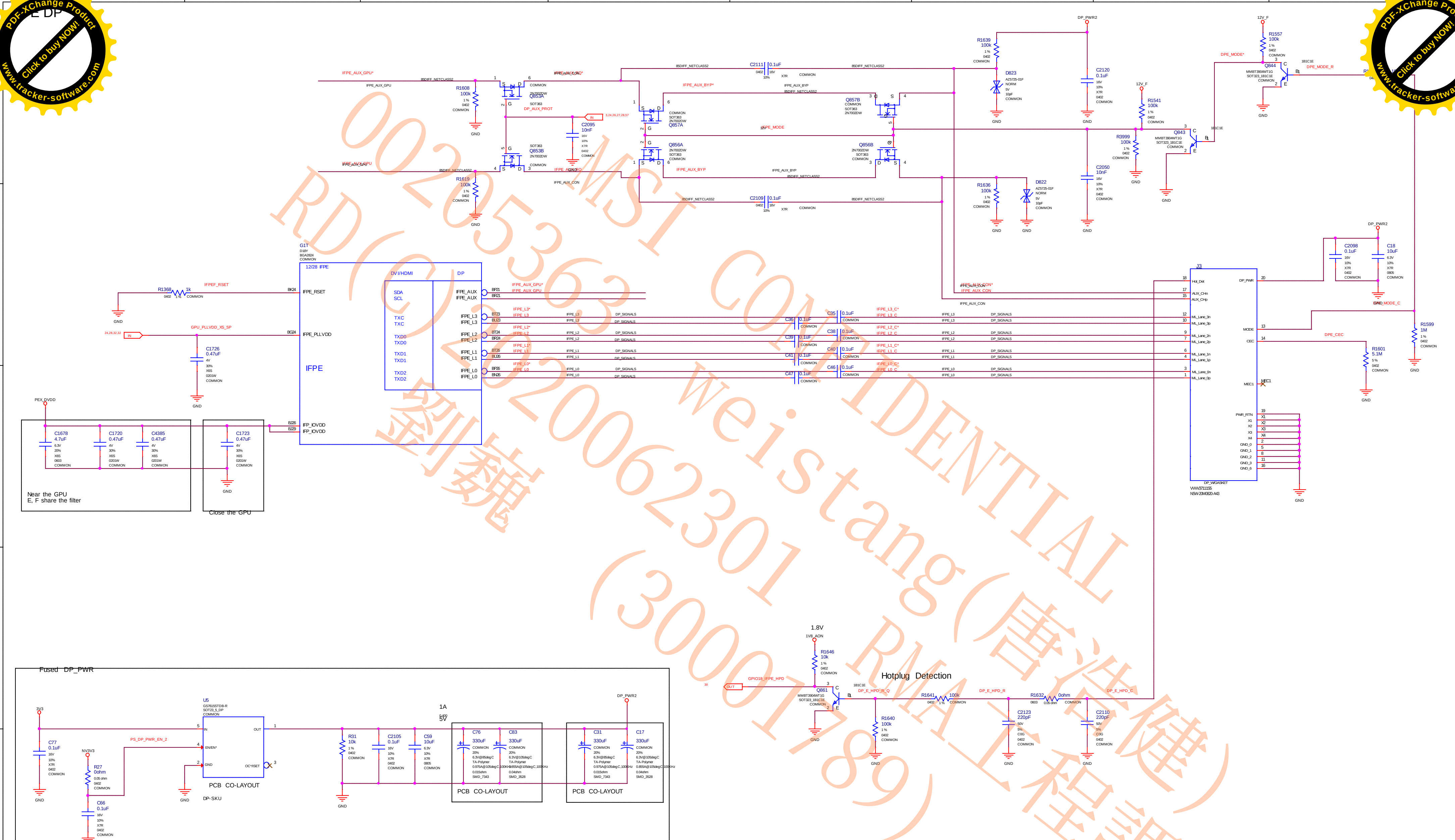


NVVDD



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V371	
Size: Custom	Document Description: DECOUPLING 2	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 23 of 66	





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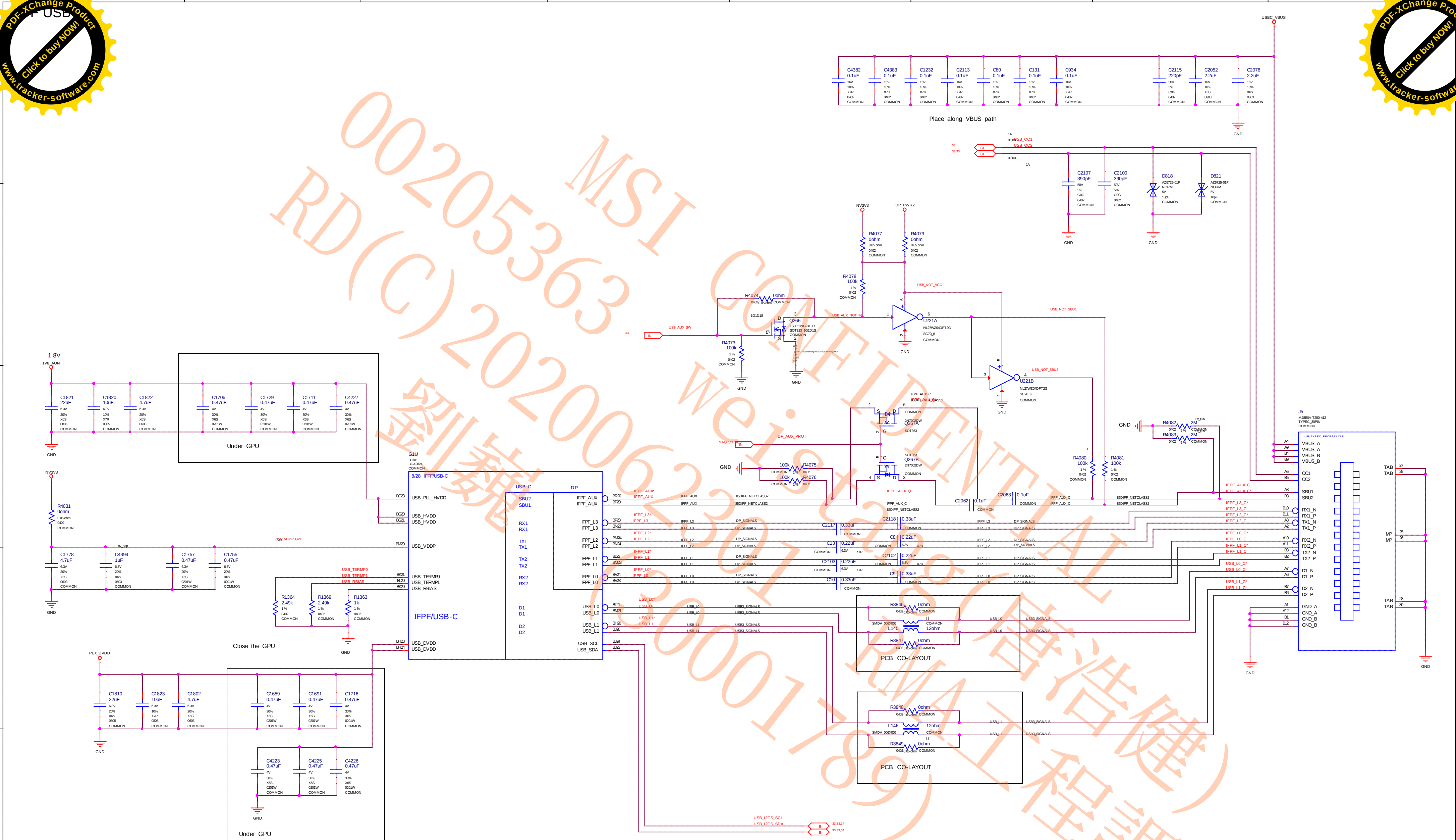
MS-V371

Size	Document Description	Rev
Custom	IFPE DP	2.1

Date: Tuesday, April 09, 2019 Sheet 25 of 66


IFPF USB
USBC_VBUS
Place along VBUS path
C4382 0.1uF
C4383 0.1uF
C1232 0.1uF
C2113 0.1uF
C80 0.1uF
C131 0.1uF
C934 0.1uF
C2115 220pF
C2052 2.2uF
C2078 2.2uF
GND
USB_CC1
USB_CC2
C2107 390pF
C2100 390pF
D818
D821
NV3V3
DP_PWR2
R4077 0ohm
R4079 0ohm
R4078 100k
USB_NOT_VCC
R4074 0ohm
USB_AUX_SW
USB_AUX_NOT_IN
Q266
U221A
USB_NOT_SBU1
U221B
USB_NOT_SBU2
R4073 100k
1.8V
1V8_AON
C1821 22uF
C1820 10uF
C1822 4.7uF
C1706 0.47uF
C1729 0.47uF
C1711 0.47uF
C4227 0.47uF
Under GPU
NV3V3
R4031 0ohm
C1778 4.7uF
C4394 1uF
C1757 0.47uF
C1755 0.47uF
USB_TERMP0
USB_TERMP1
USB_RBIAS
R1364 2.49k
R1369 2.49k
R1363 1k
Close the GPU
PEX_DVDD
C1810 22uF
C1823 10uF
C1802 4.7uF
C1659 0.47uF
C1691 0.47uF
C1716 0.47uF
C4223 0.47uF
C4225 0.47uF
C4226 0.47uF
Under GPU
G1U
8/28 IFPF/USB-C
USB_PLL_HVDD
USB_HVDD
USB_VDDP
USB_TERMP0
USB_TERMP1
USB_RBIAS
IFPF/USB-C
USB_DVDD
USB-C
DP
SBU2
SBU1
RX1
TX1
TX2
RX2
D1
D2
IFPF_AUX
IFPF_L3
IFPF_L2
IFPF_L1
IFPF_L0
USB_L0
USB_L1
USB_SCL
USB_SDA
DP_AUX_PROT
Q267A
Q267B
R4075 100k
R4076 100k
R4080 100k
R4081 100k
R4082 2M
R4083 2M
C2062 0.1uF
C2063 0.1uF
C2117 0.33uF
C2118 0.33uF
C13 0.22uF
C8 0.22uF
C2103 0.22uF
C2102 0.22uF
C10 0.33uF
C9 0.33uF
R3846 0ohm
L145 12ohm
R3847 0ohm
PCB CO-LAYOUT
R3848 0ohm
L146 12ohm
R3849 0ohm
PCB CO-LAYOUT
USB_I2CS_SCL
USB_I2CS_SDA
J5
USB_TYPEC_RECEPTACLE
VBUS_A
VBUS_B
CC1
CC2
SBU1
SBU2
RX1_N
RX1_P
TX1_N
TX1_P
RX2_N
RX2_P
TX2_N
TX2_P
D1_N
D1_P
D2_N
D2_P
GND_A
GND_B
TAB
MP

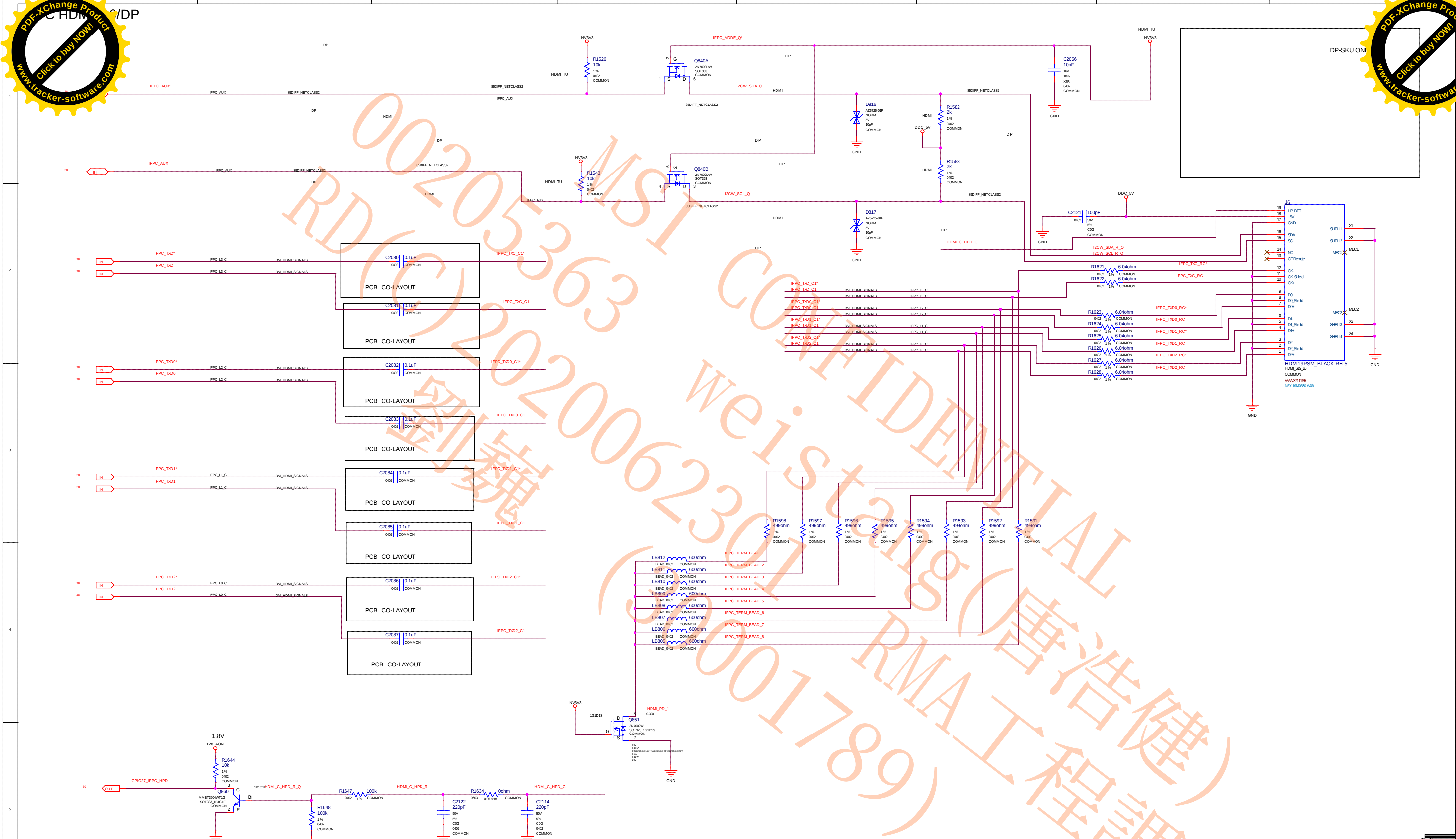
MICRO-STAR INT'L CO.,LTD

MS-V371

Size	Document Description	Rev
Custom	IFPF USB	2.1

Date: Tuesday, April 09, 2019 Sheet 26 of 66

IFPC HDMI/DP



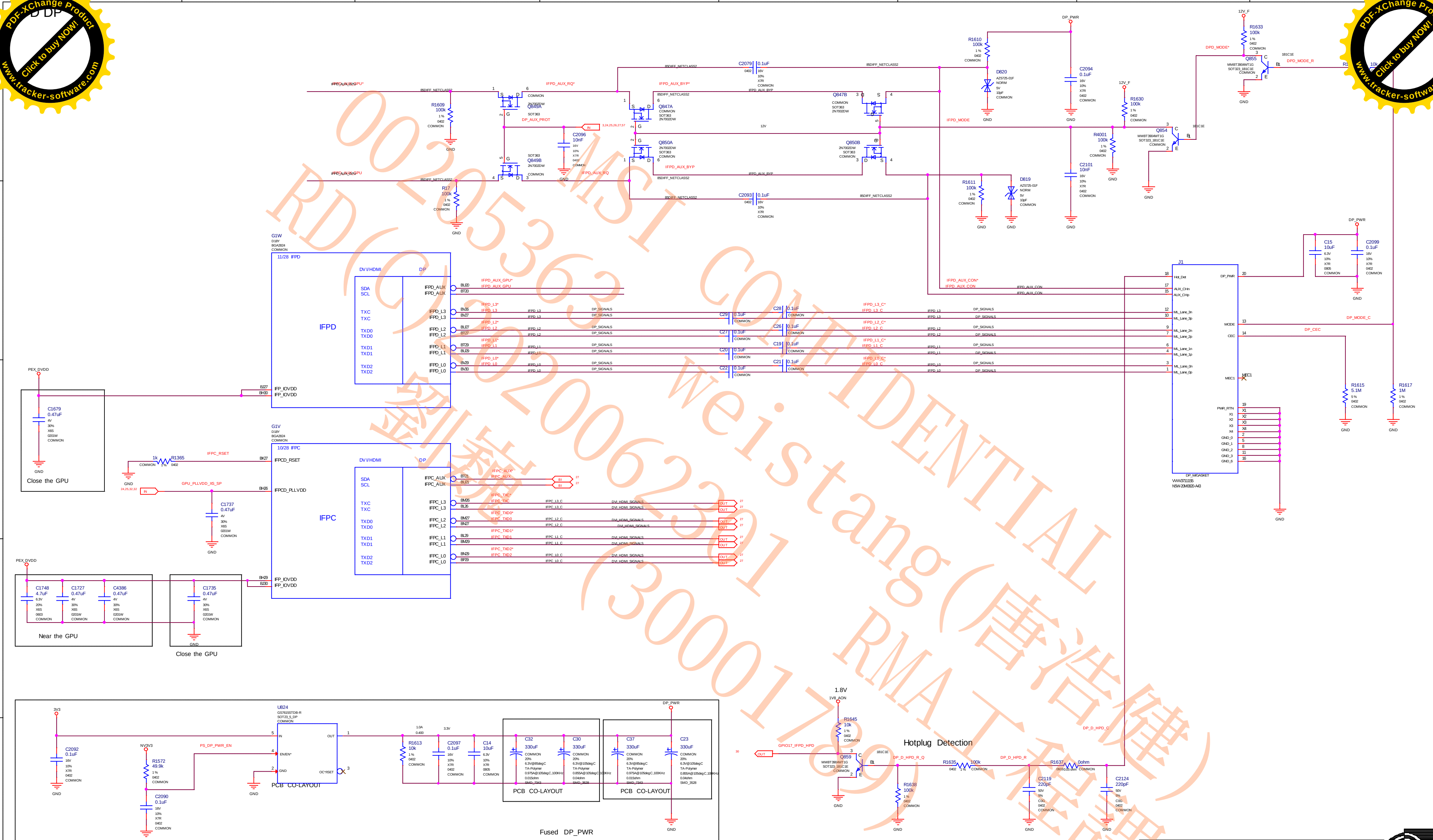
DP-SKU ONLY
NV3V3
R1526 10k
R1543 10k
Q840A 2N7002DW
Q840B 2N7002DW
C2056 10nF
D816 AZ5725-01F
D817 AZ5725-01F
R1582 2k
R1583 2k
C2121 100pF
DDC_5V
I2CW_SDA_Q
I2CW_SCL_Q
IFPC_AUX*
IFPC_AUX
IFPC_MODE_Q*
HDMI_C_HPD_C
J6
HDMI19PSM_BLACK-RH-5
R1621 6.04ohm
R1622 6.04ohm
R1623 6.04ohm
R1624 6.04ohm
R1625 6.04ohm
R1626 6.04ohm
R1627 6.04ohm
R1628 6.04ohm
C2080 0.1uF
C2081 0.1uF
C2082 0.1uF
C2083 0.1uF
C2084 0.1uF
C2085 0.1uF
C2086 0.1uF
C2087 0.1uF
PCB CO-LAYOUT
IFPC_TXC*
IFPC_TXC
IFPC_TXD0*
IFPC_TXD0
IFPC_TXD1*
IFPC_TXD1
IFPC_TXD2*
IFPC_TXD2
R1591 499ohm
R1592 499ohm
R1593 499ohm
R1594 499ohm
R1595 499ohm
R1596 499ohm
R1597 499ohm
R1598 499ohm
LB805 600ohm
LB806 600ohm
LB807 600ohm
LB808 600ohm
LB809 600ohm
LB810 600ohm
LB811 600ohm
LB812 600ohm
Q851 2N7002W
HDMI_PD_1
1.8V
1V8_AON
R1644 10k
Q860 MMBT3904WT1G
GPIO27_IFPC_HPD
R1648 100k
R1647 100k
R1634 0ohm
C2122 220pF
C2114 220pF
HDMI_C_HPD_R_Q
HDMI_C_HPD_R
HDMI_C_HPD_C
GND

MICRO-STAR INT'L CO.,LTD

MS-V371

Size	Document Description	Rev
Custom	IFPC HDMI	2.1

Date: Tuesday, April 09, 2019 Sheet 27 of 66

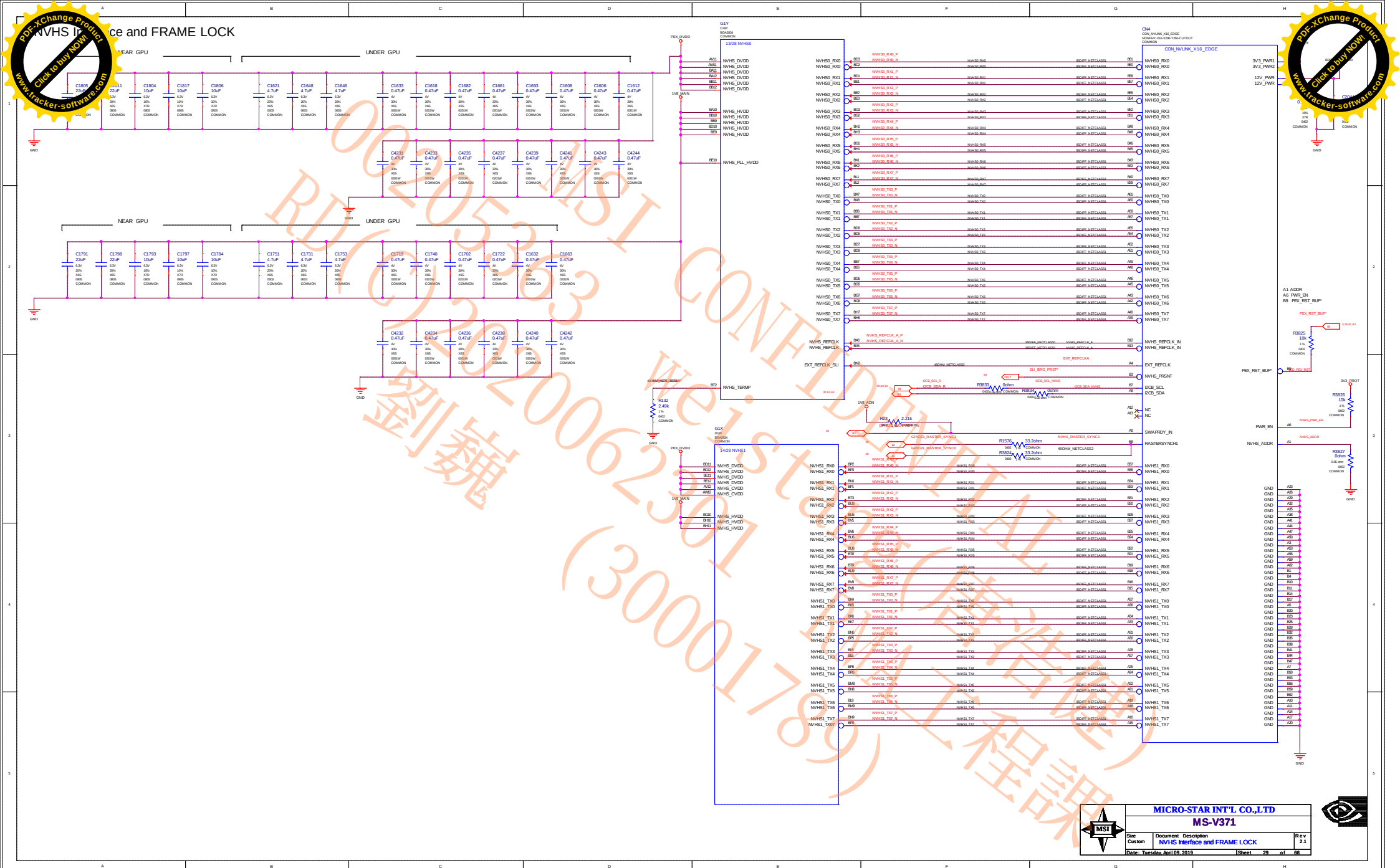

IFPD
IFPC
G1W
11/28 IFPD
G1V
10/28 IFPC
DVI/HDMI
DP
SDA
SCL
TXC
TXD0
TXD1
TXD2
IFPD_AUX
IFPD_L3
IFPD_L2
IFPD_L1
IFPD_L0
IFPC_AUX
IFPC_L3
IFPC_L2
IFPC_L1
IFPC_L0
IFP_IOVDD
IFPCD_RSET
IFPCD_PLLVDD
PEX_DVDD
C1679 0.47uF
Close the GPU
R1365 1k
IFPC_RSET
GPU_PLLVDD_XS_SP
C1737 0.47uF
C1748 4.7uF
C1727 0.47uF
C4386 0.47uF
C1735 0.47uF
Near the GPU
Close the GPU
R1609 100k
R17 100k
Q849A
Q849B
C2096 10nF
DP_AUX_PROT
Q847A
Q847B
Q850A
Q850B
IFPD_AUX_BYP
IFPD_AUX_RQ
C2079 0.1uF
C2093 0.1uF
R1610 100k
D820
DP_PWR
C2094 0.1uF
R1611 100k
D819
C2101 10nF
R4001 100k
R1630 100k
Q854
R1633 100k
Q855
DPD_MODE
IFPD_MODE
C28 0.1uF
C29 0.1uF
C26 0.1uF
C27 0.1uF
C19 0.1uF
C20 0.1uF
C21 0.1uF
C22 0.1uF
DP_SIGNALS
IFPD_AUX_CON
J1
Hot_Det
AUX_CHn
AUX_CHp
ML_Lane_3n
ML_Lane_3p
ML_Lane_2n
ML_Lane_2p
ML_Lane_1n
ML_Lane_1p
ML_Lane_0n
ML_Lane_0p
MODE
CEC
MEC1
PWR_RTN
C15 10uF
C2099 0.1uF
DP_MODE_C
DP_CEC
R1615 5.1M
R1617 1M
DVI_HDMI_SIGNALS
3V3
C2092 0.1uF
NV3V3
R1572 49.9k
C2090 0.1uF
U824
PS_DP_PWR_EN
IN
OUT
EN/EN*
GND
OC*/SET
PCB CO-LAYOUT
R1613 10k
C2097 0.1uF
C14 10uF
C32 330uF
C30 330uF
C37 330uF
C23 330uF
PCB CO-LAYOUT
PCB CO-LAYOUT
Fused DP_PWR
1.8V
1V8_AON
R1645 10k
Q859
GPIO17_IFPD_HPD
Hotplug Detection
R1638 100k
R1635 100k
R1637 0ohm
DP_D_HPD_R
DP_D_HPD_C
C2119 220pF
C2124 220pF
GND

MICRO-STAR INT'L CO.,LTD

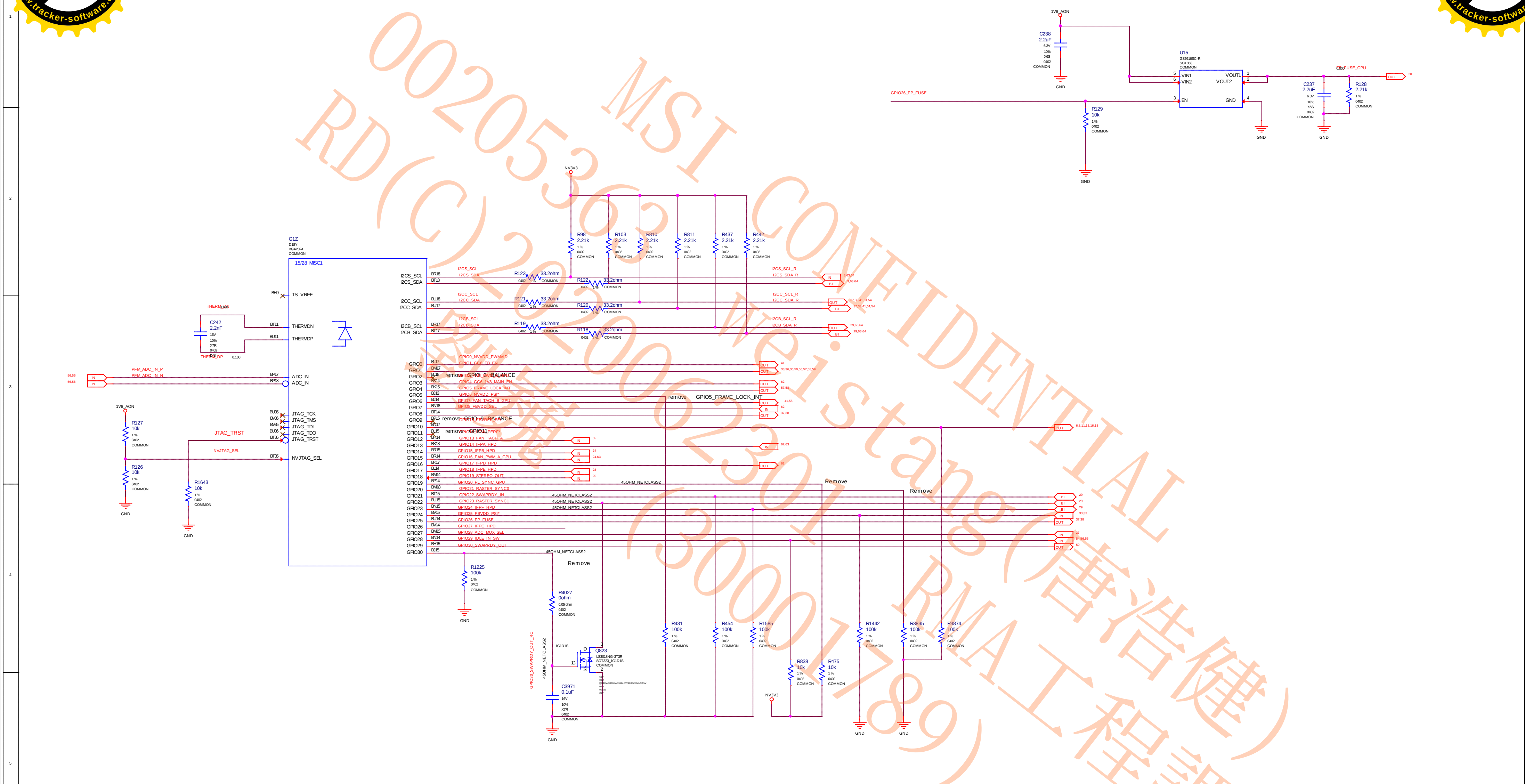
MS-V371

Size	Document Description	Rev
Custom	IFPD DP	2.1

Date: Tuesday, April 09, 2019 Sheet 28 of 66


NVHS Interface and FRAME LOCK
NEAR GPU
UNDER GPU
NEAR GPU
UNDER GPU
G1Y
13/28 NVHS0
G1X
14/28 NVHS1
CN4
CON_NVLINK_X16_EDGE
NVHS_REFCLK_A_P
NVHS_REFCLK_A_N
EXT_REFCLK_SLI
NVHS_TERMP
R132 2.49k
EXT_REFCLK
NVHS_PRSNT
I2CB_SCL
I2CB_SDA
SLI_BRG_PRST*
I2CB_SCL_R
I2CB_SDA_R
I2CB_SCL_NVHS
I2CB_SDA_NVHS
R3832 0ohm
R3834 0ohm
R33 2.21k
GPIO23_RASTER_SYNC1
GPIO21_RASTER_SYNC0
R1576 33.2ohm
R3824 33.2ohm
NVHS_RASTER_SYNC1
SWAPRDY_IN
RASTERSYNCH1
NC
NC
PEX_RST_BUF*
R3825 10k
R3826 10k
R3827 0ohm
NVHS_PWR_EN
NVHS_ADDR
PWR_EN
A1 ADDR
A6 PWR_EN
B9 PEX_RST_BUF*
3V3_PWR3
3V3_PWR2
12V_PWR
12V_PWR
PEX_DVDD
1V8_MAIN
1V8_ACN
GND
MICRO-STAR INT'L CO.,LTD
MS-V371
Size Custom
Document Description NVHS Interface and FRAME LOCK
Rev 2.1
Date: Tuesday, April 09, 2019
Sheet 29 of 66

...Thermal, JTAG, GPIO, STEREO



G1Z
15/28 MISC1
I2CS_SCL
I2CS_SDA
I2CC_SCL
I2CC_SDA
I2CB_SCL
I2CB_SDA
TS_VREF
THERMDN
THERMDP
ADC_IN
JTAG_TCK
JTAG_TMS
JTAG_TDI
JTAG_TDO
JTAG_TRST
NVJTAG_SEL
GPIO0
GPIO1
GPIO2
GPIO3
GPIO4
GPIO5
GPIO6
GPIO7
GPIO8
GPIO9
GPIO10
GPIO11
GPIO12
GPIO13
GPIO14
GPIO15
GPIO16
GPIO17
GPIO18
GPIO19
GPIO20
GPIO21
GPIO22
GPIO23
GPIO24
GPIO25
GPIO26
GPIO27
GPIO28
GPIO29
GPIO30
remove GPIO 2 BALANCE
remove GPIO 9 BALANCE
remove GPIO11
remove GPIO5_FRAME_LOCK_INT
Remove
U15
VIN1
VIN2
EN
VOUT1
VOUT2
GND
GPIO26_FP_FUSE
1V8_AON
NV3V3
FUSE_GPU
PFM_ADC_IN_P
PFM_ADC_IN_N
JTAG_TRST
NVJTAG_SEL
Q823

MICRO-STAR INT'L CO.,LTD

MS-V371

Size	Document Description	Rev
Custom	MISC	2.1

Date: Tuesday, April 09, 2019 Sheet 30 of 66

[illegible]SC2: RO[illegible] Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
[illegible]	L	L	00000	
L	L	H	00001	DEFAULT
[illegible]	H	L	00010	
[illegible]	H	H	00011	
H	L	L	00100	
H	L	H	00101	
H	H	L	00110	
H	H	H	00111	
L	L	M	01000	
L	M	L	01001	

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	H	XXX0	FS_OVERT DISABLE	

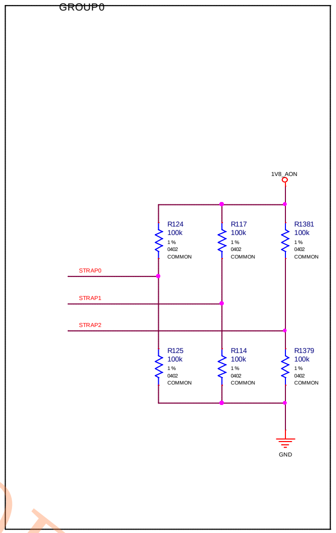
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	SKU 200

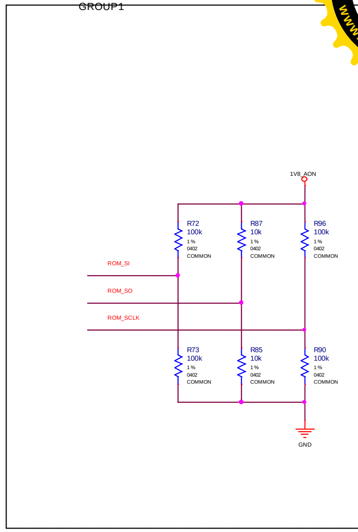
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

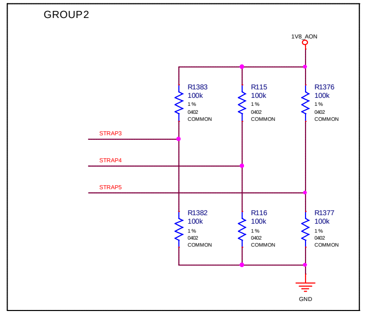
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

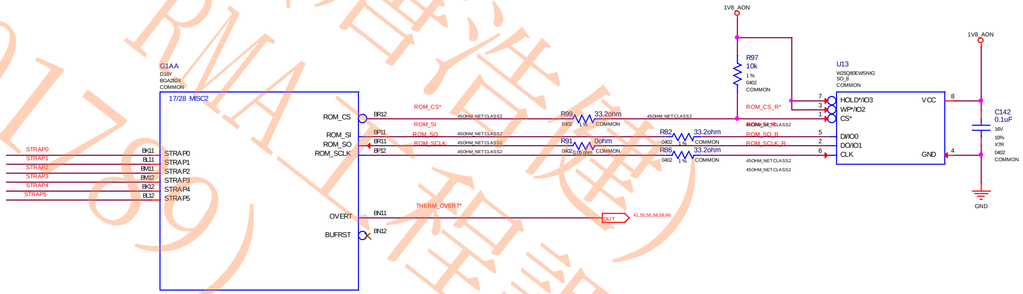
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE







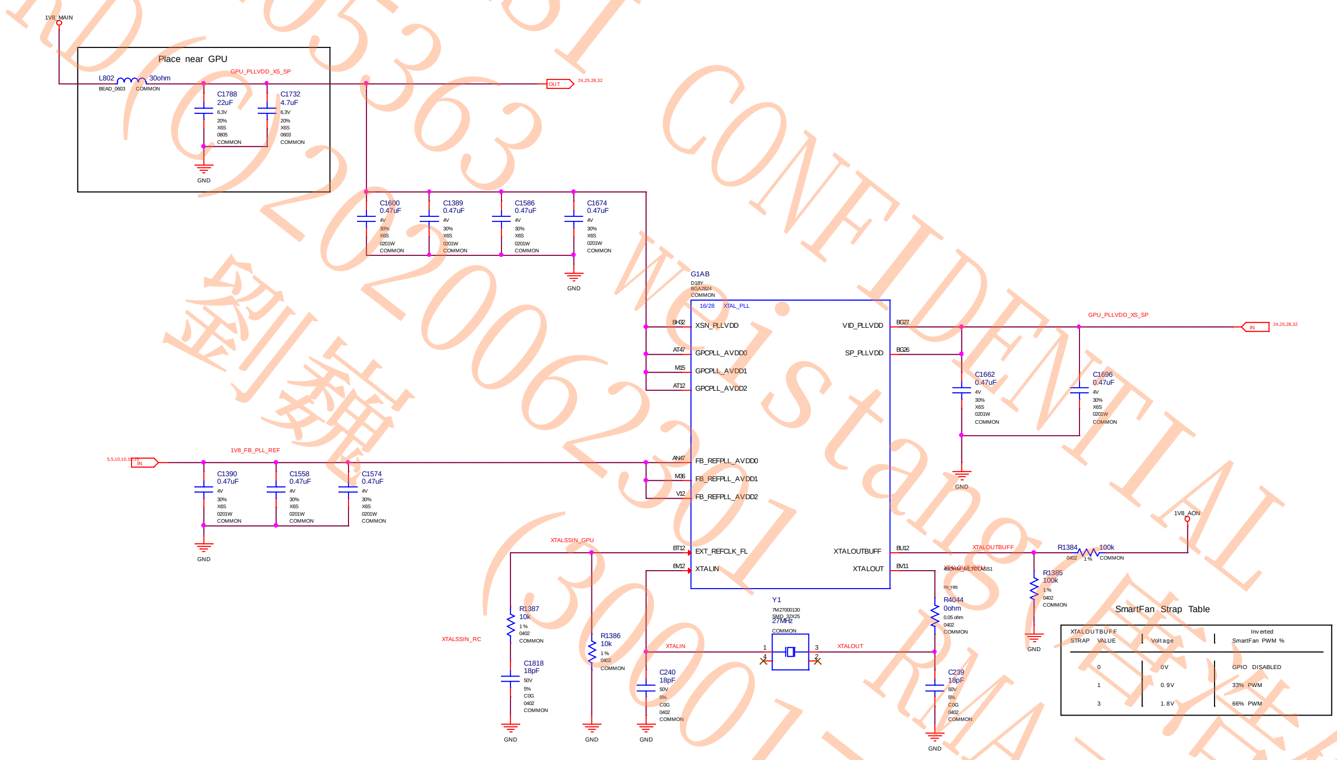


MICRO-STAR INT'L CO.,LTD
MS-V371

Size	Document Description	Rev
Custom	ROM/STRAPS	2.1

Date: Tuesday, April 09, 2019 Sheet 31 of 66

C2: X[illegible] PLL



1V8_MAIN
Place near GPU
L802
30ohm
BEAD_0603
COMMON
GPU_PLLVDD_XS_SP
OUT
C1788
22uF
C1732
4.7uF
GND
C1600
0.47uF
C1389
0.47uF
C1586
0.47uF
C1674
0.47uF
G1AB
XTAL_PLL
XSN_PLLVDD
GPCPLL_AVDD0
GPCPLL_AVDD1
GPCPLL_AVDD2
FB_REFPLL_AVDD0
FB_REFPLL_AVDD1
FB_REFPLL_AVDD2
EXT_REFCLK_FL
XTALIN
VID_PLLVDD
SP_PLLVDD
XTALOUTBUFF
XTALOUT
IN
C1662
0.47uF
C1696
0.47uF
1V8_FB_PLL_REF
C1390
0.47uF
C1558
0.47uF
C1574
0.47uF
XTALSSIN_GPU
XTALSSIN_RC
R1387
10k
R1386
10k
C1818
18pF
C240
18pF
Y1
27MHz
XTALIN
XTALOUT
R4044
0ohm
C239
18pF
XTALOUTBUFF
R1384
100k
R1385
100k
1V8_AON

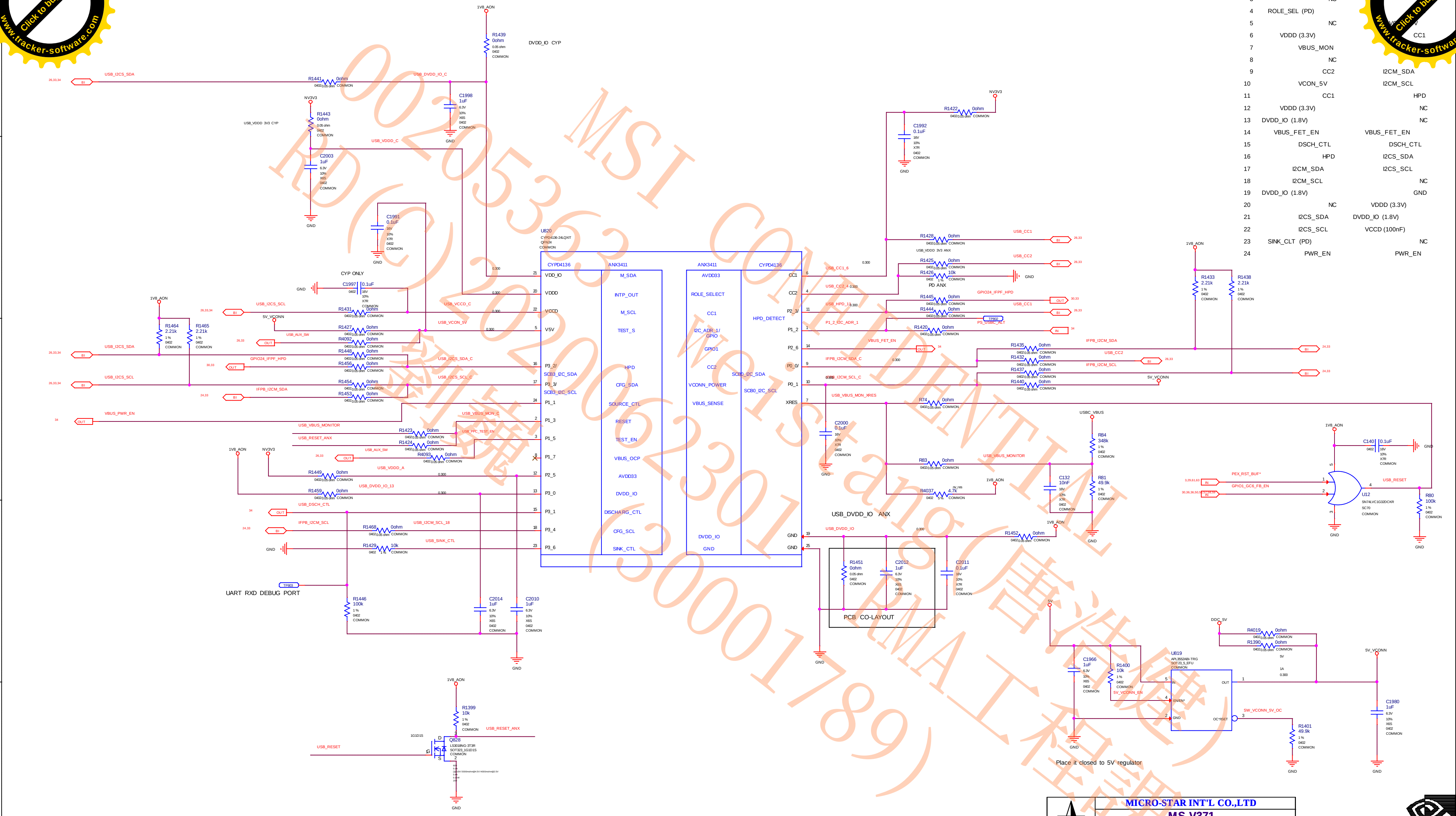
SmartFan Strap Table

XTALOUTBUFF STRAP VALUE	Voltage	Inverted SmartFan PWM %
0	0V	GPIO DISABLED
1	0.9V	33% PWM
3	1.8V	66% PWM

MICRO-STAR INT'L CO.,LTD		
MS-V371		
Size Custom	Document Description XTAL	Rev 2.1
Date: Tuesday, April 09, 2019	Sheet 32 of 66	

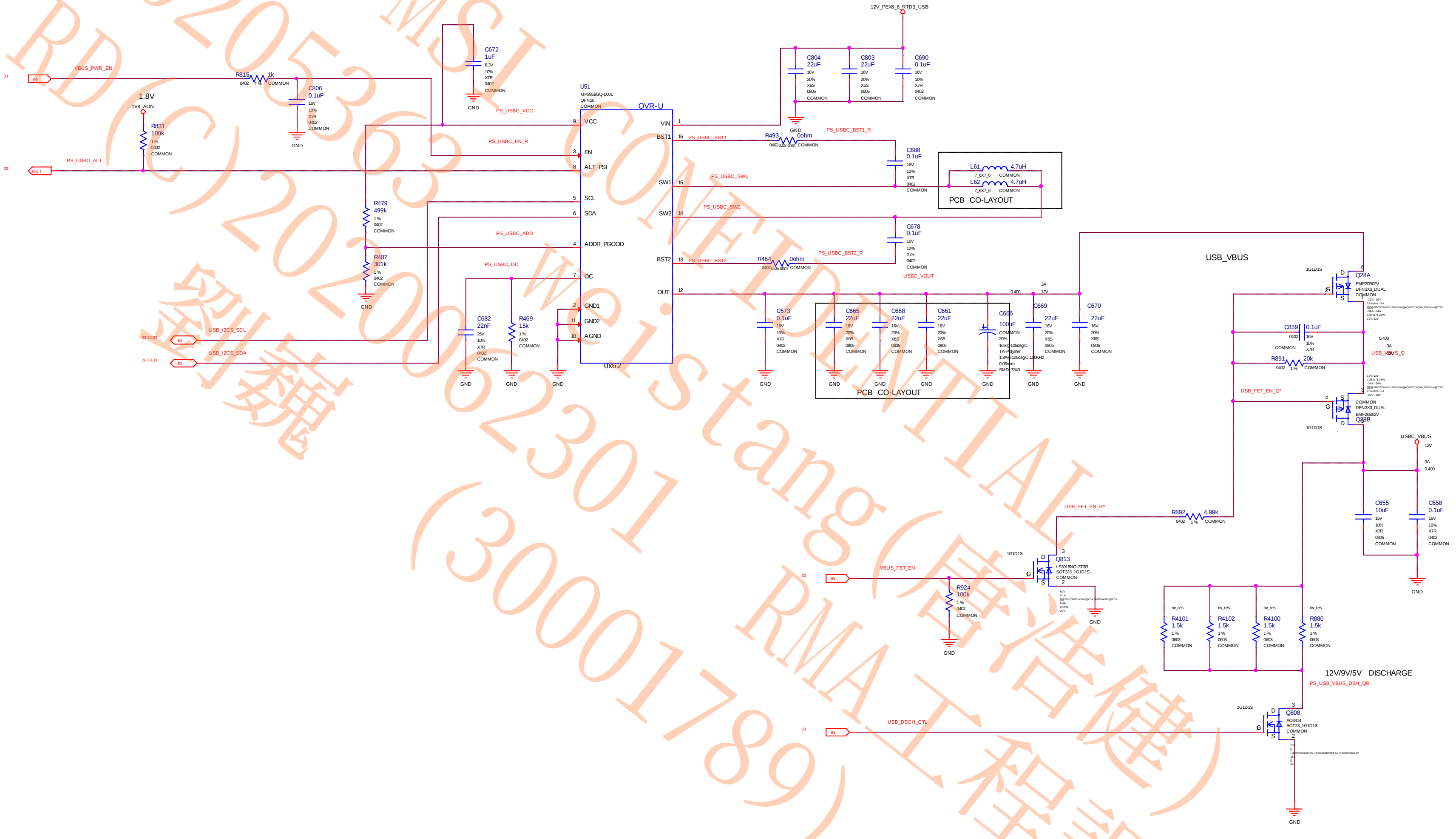
MISC: USB PCC

PIN	ANX	CYP
1	TP	TP
2	RESET	BUS_MON
3	NC	[illegible]
4	ROLE_SEL (PD)	[illegible]
5	NC	[illegible]
6	VDDD (3.3V)	CC1
7	VBUS_MON	[illegible]
8	NC	[illegible]
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN



MICRO-STAR INT'L CO.,LTD		
MS-V371		
Size: Custom	Document Description: USB PCC	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 33 of 66	

PS: US


12V_PEX6_8_RTD3_USB
VBUS_PWR_EN
R815 1k
C672 1uF
C806 0.1uF
1.8V
1V8_AON
R831 100k
PS_USBC_ALT
U51
OVR-U
VCC
EN
ALT_PSI
SCL
SDA
ADDR_PGOOD
OC
GND1
GND2
AGND
VIN
BST1
SW1
SW2
BST2
OUT
PS_USBC_VCC
PS_USBC_EN_R
R479 499k
R487 301k
PS_USBC_ADD
PS_USBC_OC
C682 22nF
R469 15k
USB_I2CS_SCL
USB_I2CS_SDA
C804 22uF
C803 22uF
C690 0.1uF
R493 0ohm
PS_USBC_BST1
PS_USBC_BST1_R
C688 0.1uF
L61 4.7uH
L62 4.7uH
PCB CO-LAYOUT
PS_USBC_SW1
PS_USBC_SW2
C678 0.1uF
R464 0ohm
PS_USBC_BST2
PS_USBC_BST2_R
USBC_VOUT
C673 0.1uF
C665 22uF
C668 22uF
C661 22uF
C686 100uF
C669 22uF
C670 22uF
PCB CO-LAYOUT
USB_VBUS
Q28A
C839 0.1uF
R891 20k
USB_VBUS_Q
USB_FET_EN_Q*
Q28B
USBC_VBUS
C655 10uF
C658 0.1uF
USB_FET_EN_R*
R892 4.99k
VBUS_FET_EN
Q813
R924 100k
R4101 1.5k
R4102 1.5k
R4100 1.5k
R880 1.5k
12V/9V/5V DISCHARGE
PS_USB_VBUS_DSH_QR
USB_DSCH_CTL
Q808
GND

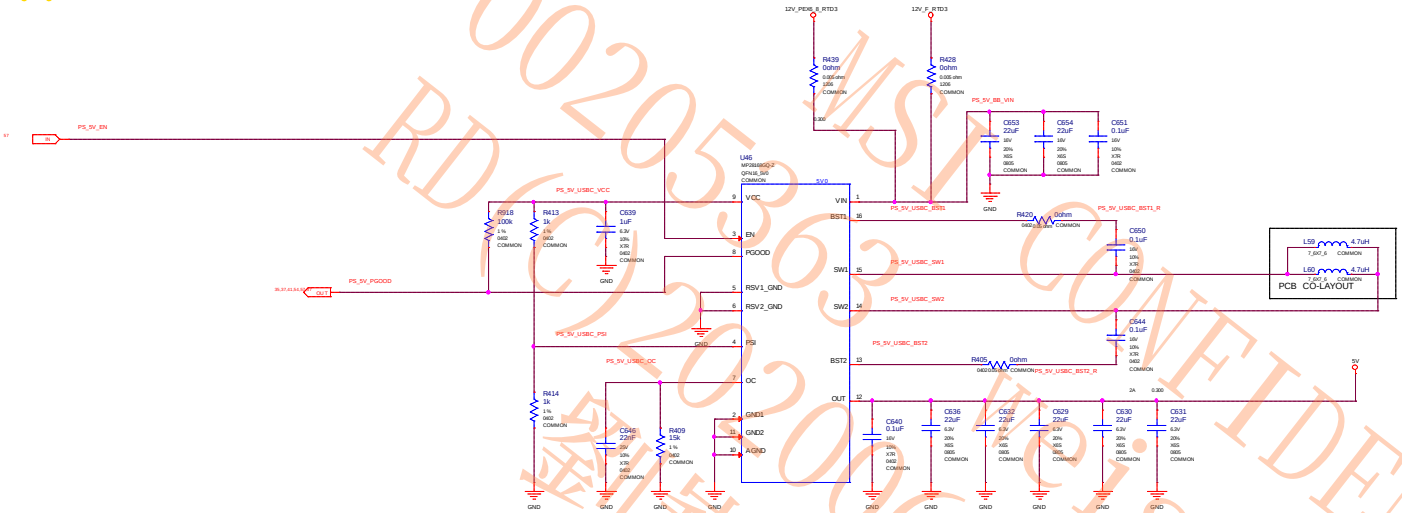
MICRO-STAR INT'L CO.,LTD

MS-V371

Size: Custom | Document Description: USB VR | Rev: 2.1

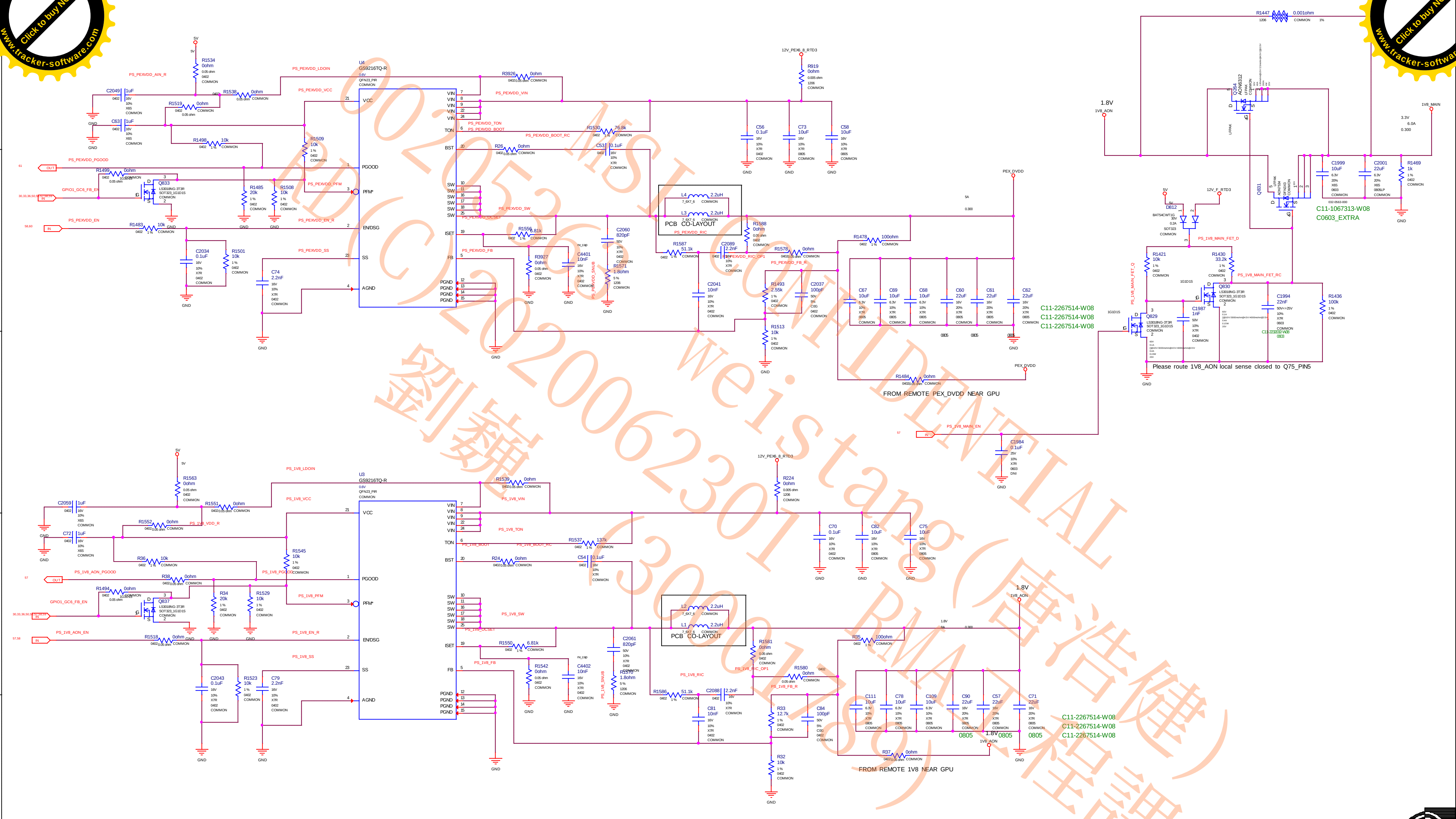
Date: Tuesday, April 09, 2019 | Sheet 34 of 66

PS: 5V BACKUP



MICRO-STAR INT'L CO.,LTD	
MS-V371	
Size: Custom	Document Description: 5V
Rev: 2.1	
Date: Tuesday, April 09, 2019	Sheet 35 of 66

PS: PEXVDD 1V8 Rail

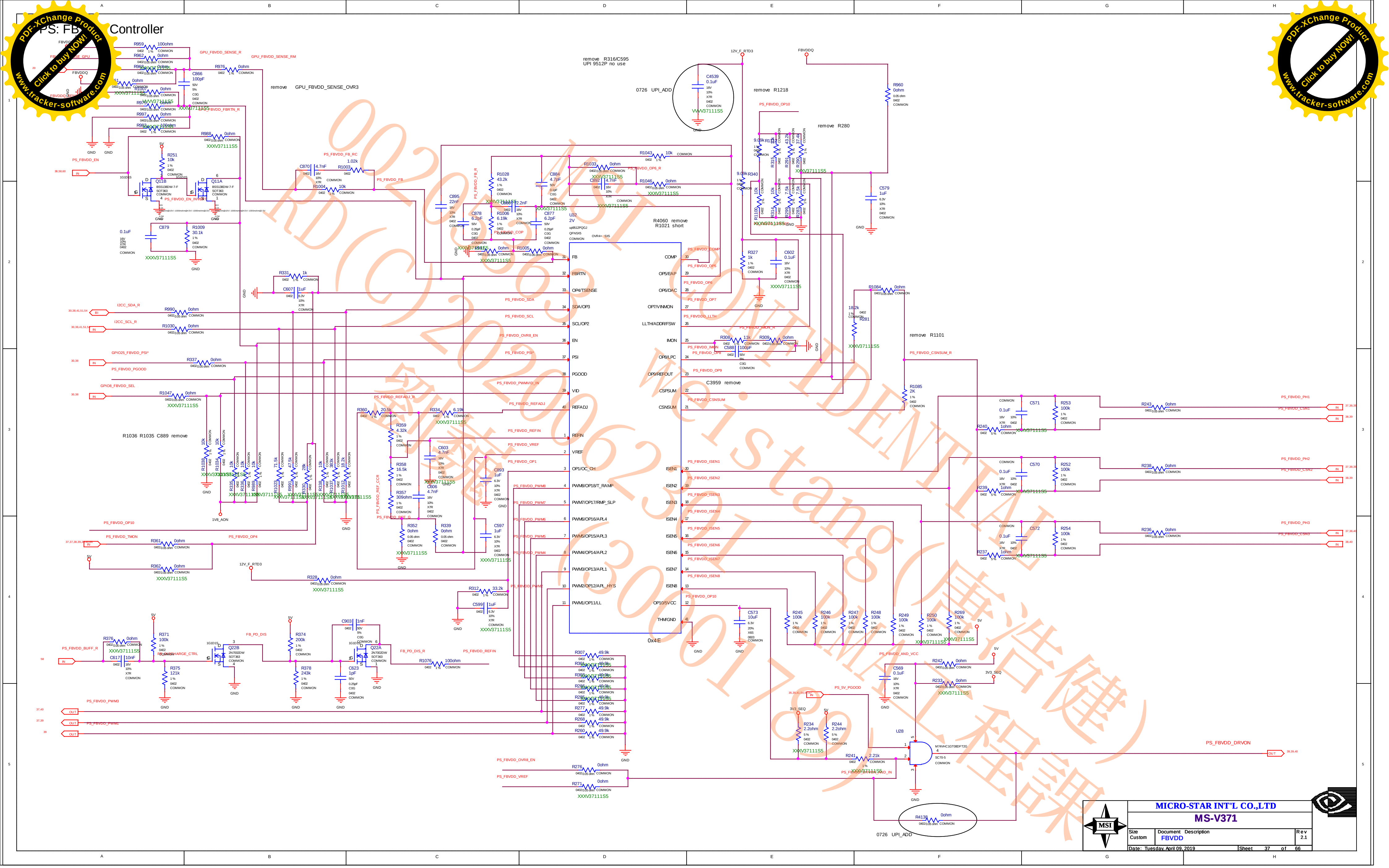


MICRO-STAR INT'L CO.,LTD

MS-V371

Size	Document Description	Rev
Custom	1V8	2.1

Date: Tuesday, April 09, 2019 Sheet 36 of 66

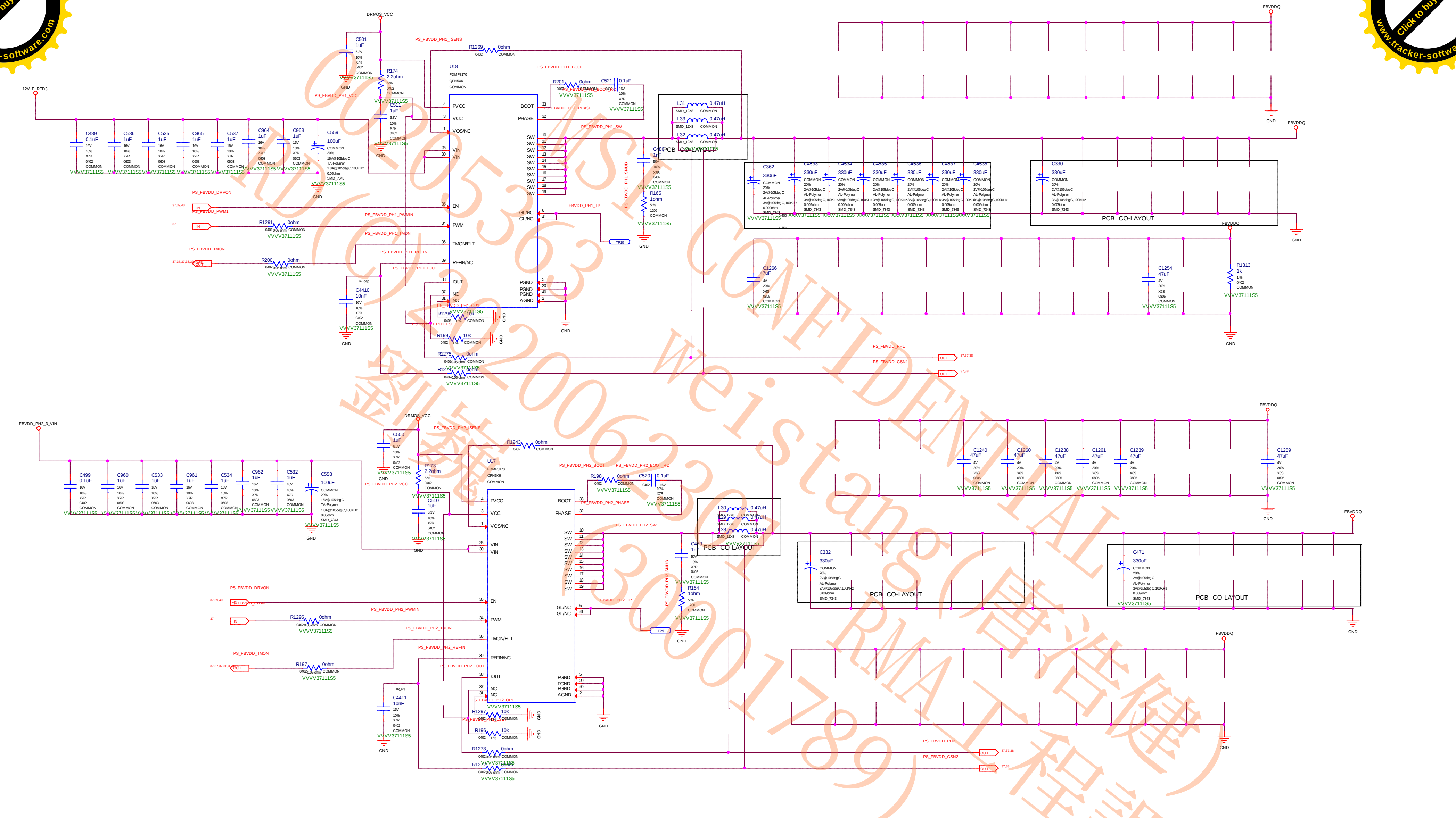


PS: [illegible] Controller OVR3

remove FBVDDQ

MICRO-STAR INT'L CO.,LTD	
MS-V371	
Size: Custom	Document Description: NA
Rev: 2.1	
Date: Tuesday, April 09, 2019	Sheet 38 of 66

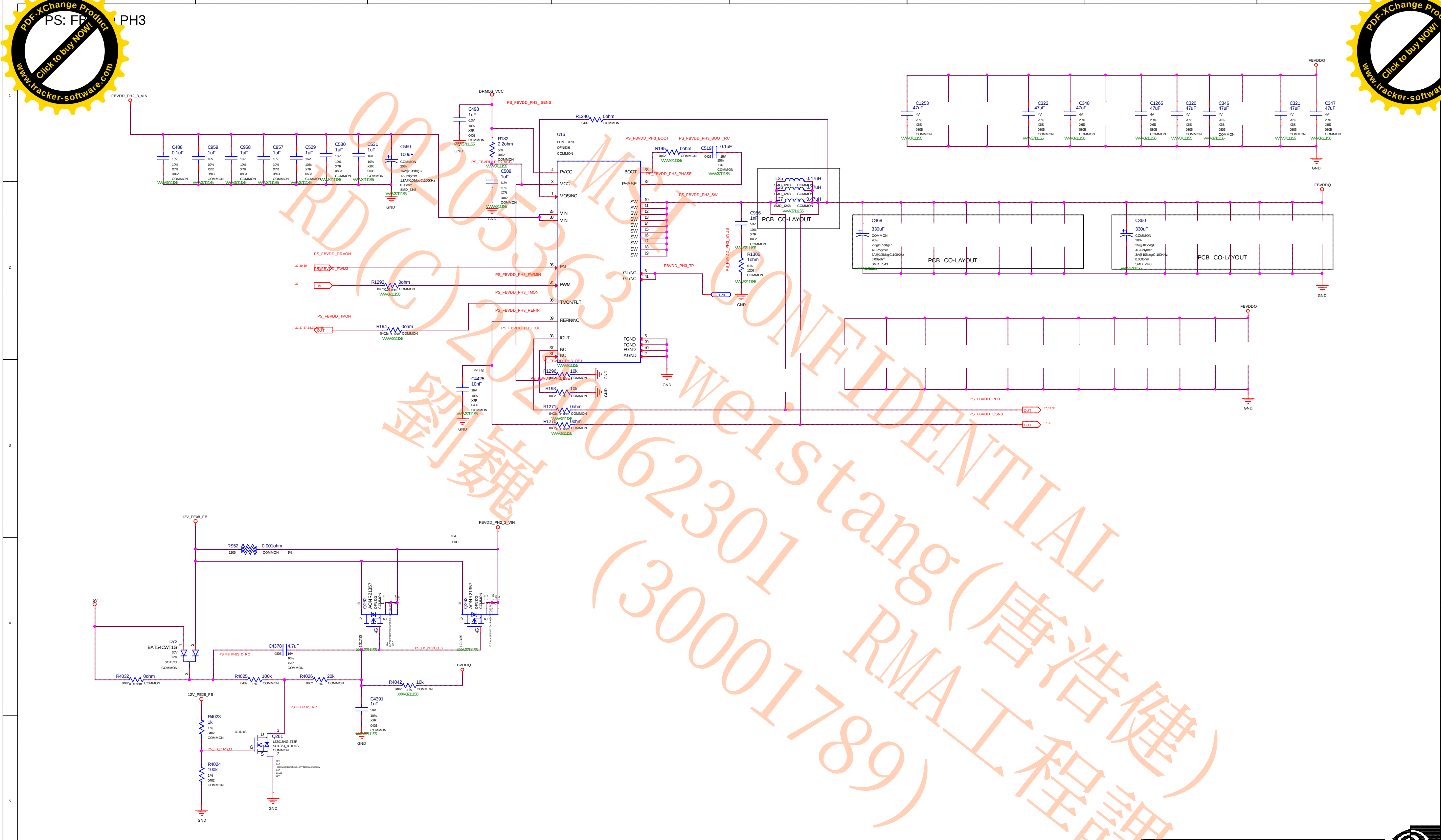
PS: FBVDD PH1, 2



DRMOS_VCC
12V_F_RTD3
U18
PVCC
VCC
VOS/NC
VIN
EN
PWM
TMON/FLT
REFIN/NC
IOUT
NC
BOOT
PHASE
SW
GL/NC
PGND
AGND
PS_FBVDD_PH1_ISENS
PS_FBVDD_PH1_BOOT
PS_FBVDD_PH1_PHASE
PS_FBVDD_PH1_SW
PS_FBVDD_PH1_VCC
PS_FBVDD_DRVON
PS_FBVDD_PH1_PWMN
PS_FBVDD_PH1_TMON
PS_FBVDD_PH1_REFIN
PS_FBVDD_PH1_IOUT
PS_FBVDD_TMON
FBVDD_PH1_TP
PS_FBVDD_PH1
PS_FBVDD_CSN1
PCB CO-LAYOUT
FBVDDQ
GND
FBVDD_PH2_3_VIN
U17
PS_FBVDD_PH2_ISENS
PS_FBVDD_PH2_BOOT
PS_FBVDD_PH2_PHASE
PS_FBVDD_PH2_SW
PS_FBVDD_PH2_VCC
PS_FBVDD_PH2_PWMN
PS_FBVDD_PH2_TMON
PS_FBVDD_PH2_REFIN
PS_FBVDD_PH2_IOUT
FBVDD_PH2_TP
PS_FBVDD_PH2
PS_FBVDD_CSN2

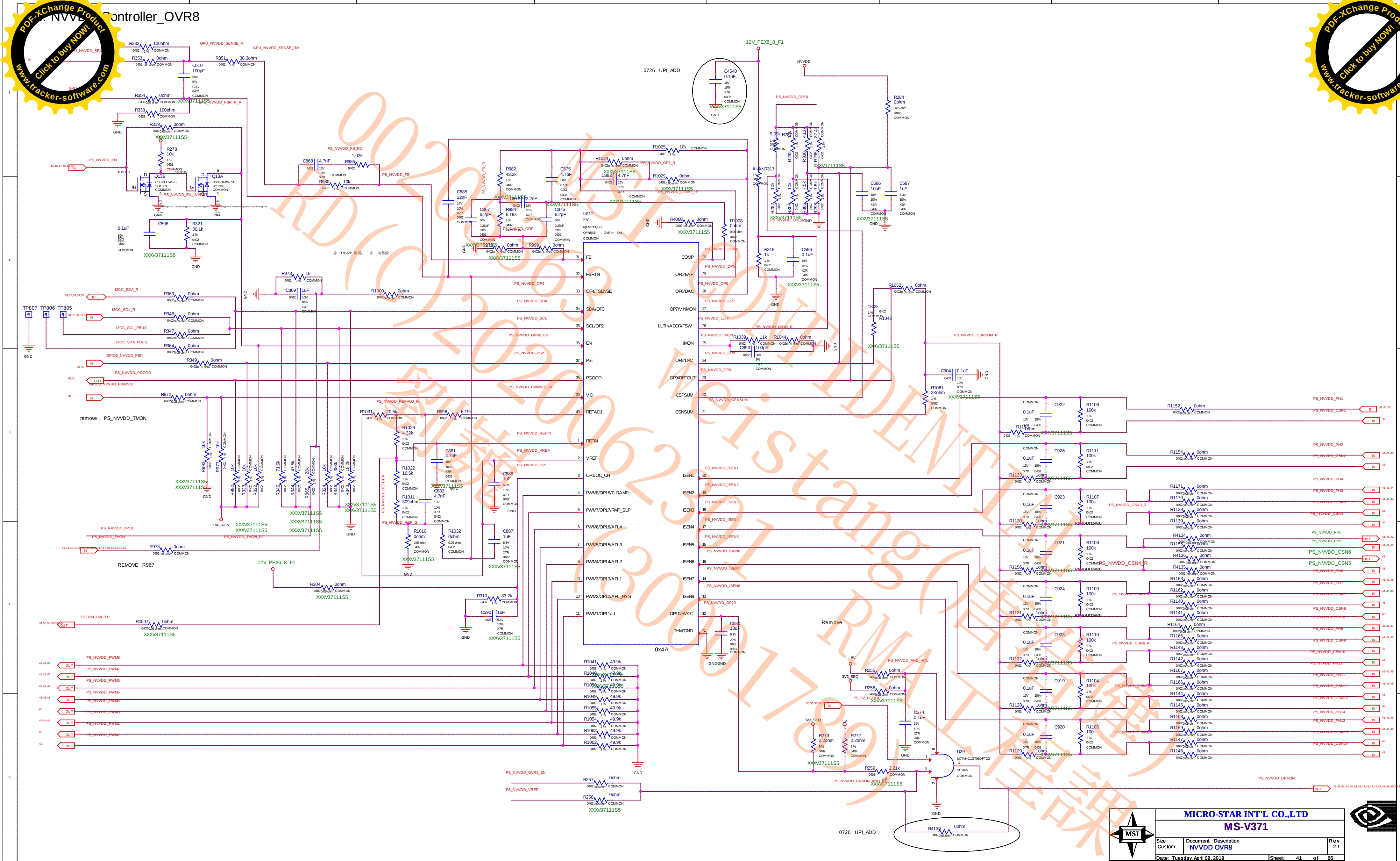
MICRO-STAR INT'L CO.,LTD		
MS-V371		
Size: Custom	Document Description: FBVDD 1/2	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 39 of 66	

PS: FBVDD PH3


FBVDD_PH2_3_VIN
DRMOS_VCC
PS_FBVDD_PH3_ISENS
C488 0.1uF
C959 1uF
C958 1uF
C957 1uF
C529 1uF
C530 1uF
C531 1uF
C560 100uF
C498 1uF
R182 2.2ohm
C509 1uF
R1240 0ohm
U16
PVCC
VCC
VOS/NC
VIN
EN
PWM
TMON/FLT
REFIN/NC
IOUT
NC
BOOT
PHASE
SW
GL/NC
PGND
AGND
PS_FBVDD_PH3_BOOT
PS_FBVDD_PH3_BOOT_RC
R195 0ohm
C519 0.1uF
PS_FBVDD_PH3_PHASE
PS_FBVDD_PH3_SW
L25 0.47uH
L26 0.47uH
L27 0.47uH
PCB CO-LAYOUT
C986 1nF
R1300 1ohm
FBVDD_PH3_TP
PS_FBVDD_DRVON
PS_FBVDD_PH3_PWMIN
PS_FBVDD_PH3_TMON
PS_FBVDD_PH3_REFIN
PS_FBVDD_PH3_IOUT
PS_FBVDD_TMON
R1292 0ohm
R194 0ohm
R1296 10k
R193 10k
C4425 10nF
R1271 0ohm
R1270 0ohm
PS_FBVDD_PH3
PS_FBVDD_CSN3
FBVDDQ
C1253 47uF
C322 47uF
C348 47uF
C1265 47uF
C320 47uF
C346 47uF
C321 47uF
C347 47uF
C468 330uF
C360 330uF
GND
12V_PEX8_FB
RS52 0.001ohm
FBVDD_PH2_3_VIN
Q262 AONR21357
Q263 AONR21357
5V
D72 BAT54CWT1G
C4378 4.7uF
PS_FB_PH23_D_RC
PS_FB_PH23_G_G
R4032 0ohm
R4025 100k
R4026 20k
R4042 10k
C4391 1nF
R4023 1k
R4024 100k
Q261
PS_FB_PH23_RR
PS_FB_PH23_G

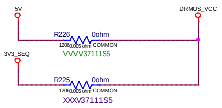
MICRO-STAR INT'L CO.,LTD			
MS-V371			
Size Custom	Document Description FBVDD 3		Rev 2.1
Date: Tuesday, April 09, 2019	Sheet 40	of 66	

NVVDD Controller_OVR8



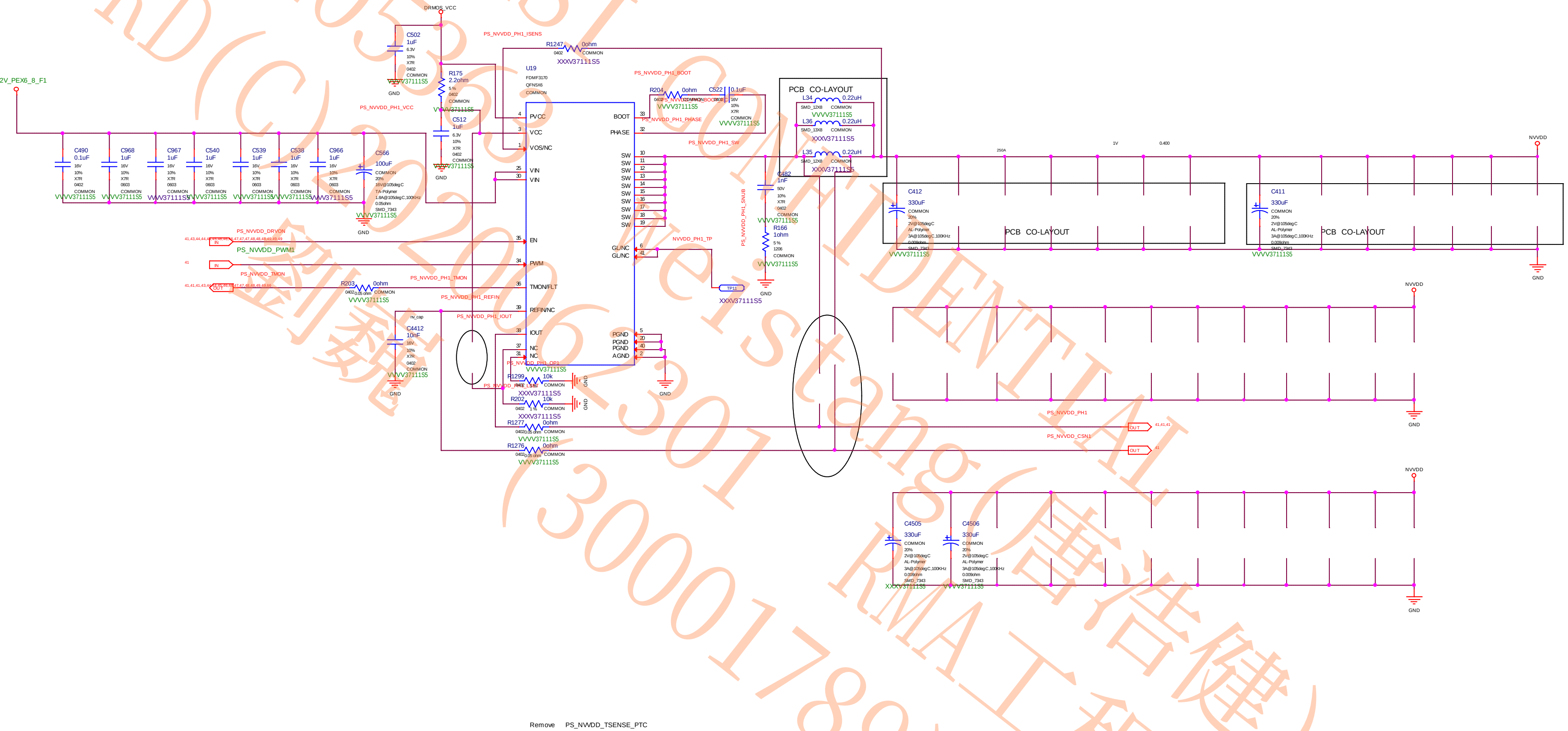
MICRO-STAR INT'L CO.,LTD		
MS-V371		
Size: Custom	Document Description: NVVDD OVR8	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 41 of 66	

S: NVV... hase 1



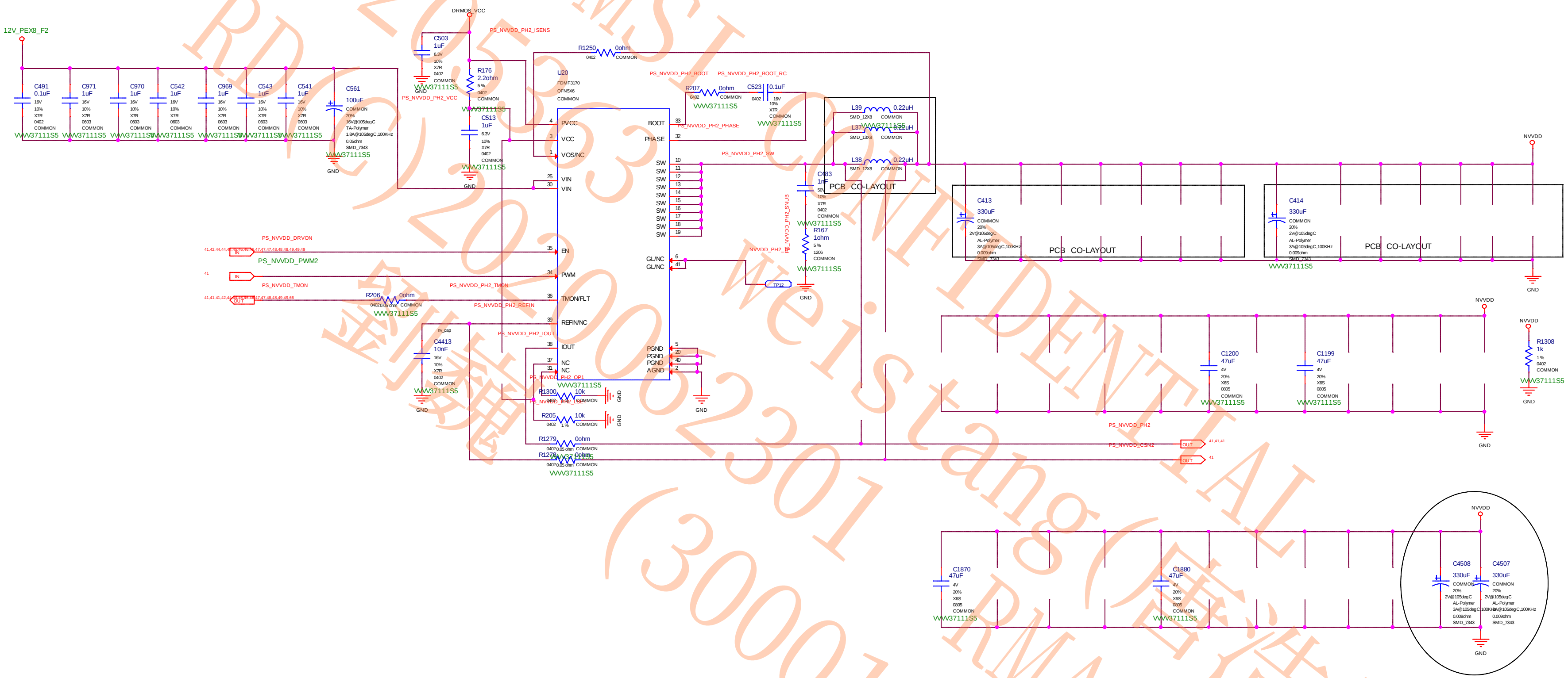
1	F1	(PWM1)
2	F2	(PWM 2)
3/4	F2	(PWM3)
5/6	F2	(PWM 4)
7/8	12V_F	(PWM 5)
9/10	F1	(PWM 6)
11/12	F1	(PWM 7)
13/14	F1	(PWM 8)

12V_F NVVDD 7/8 + MEM 1
F1 NVVDD-1/9/10/11/12/13/14
F2 NVVDD-2/3/4/5/6 + MEM 2/3



MICRO-STAR INT'L CO.,LTD		
MS-V371		
Size Custom	Document Description NVVDD PH1	Rev 2.1
Date: Tuesday, April 09, 2019	Sheet 42 of 66	

PS: NVVDD Phase 2



12V_PEX8_F2
DRMOS_VCC
PS_NVVDD_PH2_ISENS
C491 0.1uF
C971 1uF
C970 1uF
C542 1uF
C969 1uF
C543 1uF
C541 1uF
C561 100uF
C503 1uF
R176 2.2ohm
C513 1uF
R1250 0ohm
U20
PS_NVVDD_PH2_VCC
PS_NVVDD_PH2_BOOT
PS_NVVDD_PH2_BOOT_RC
R207 0ohm
C523 0.1uF
PS_NVVDD_PH2_PHASE
PS_NVVDD_PH2_SW
L39 0.22uH
L37 0.22uH
L38 0.22uH
PCB CO-LAYOUT
C483 1nF
R167 1ohm
PS_NVVDD_PH2_SNUB
PVCC
VCC
VOS/NC
VIN
BOOT
PHASE
SW
EN
PWM
TMON/FLT
REFIN/NC
IOUT
NC
GL/NC
PGND
AGND
PS_NVVDD_DRVON
PS_NVVDD_PWM2
PS_NVVDD_TMON
PS_NVVDD_PH2_TMON
R206 0ohm
PS_NVVDD_PH2_REFIN
PS_NVVDD_PH2_IOUT
C4413 10nF
R1300 10k
R205 10k
R1279 0ohm
R1278 0ohm
PS_NVVDD_PH2
PS_NVVDD_CS#2
NVVDD
C413 330uF
C414 330uF
R1308 1k
C1200 47uF
C1199 47uF
C1870 47uF
C1880 47uF
C4508 330uF
C4507 330uF
GND
WW37111S5

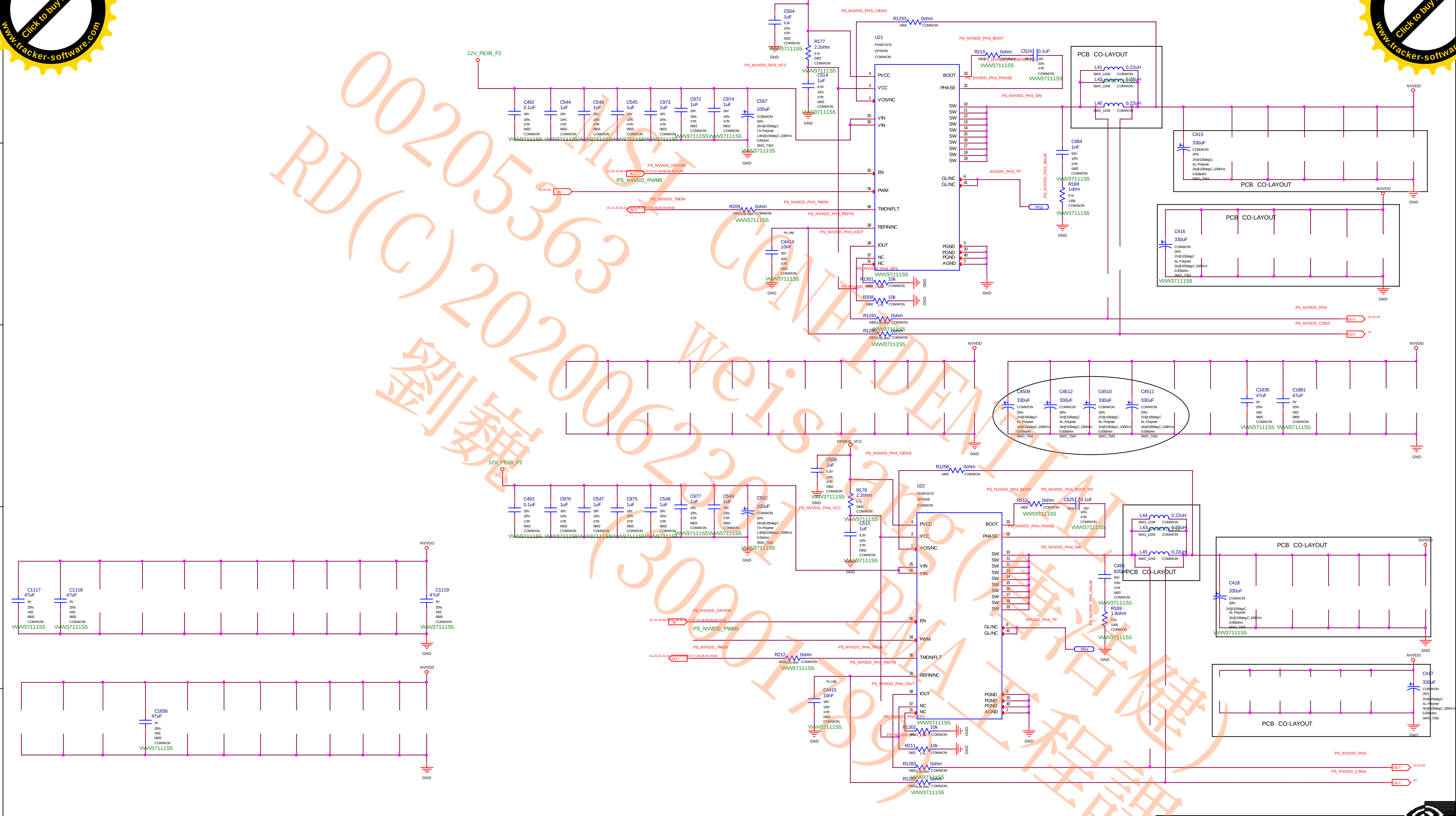
MICRO-STAR INT'L CO.,LTD

MS-V371

Size	Document Description	Rev
Custom	NVVDD PH2	2.1

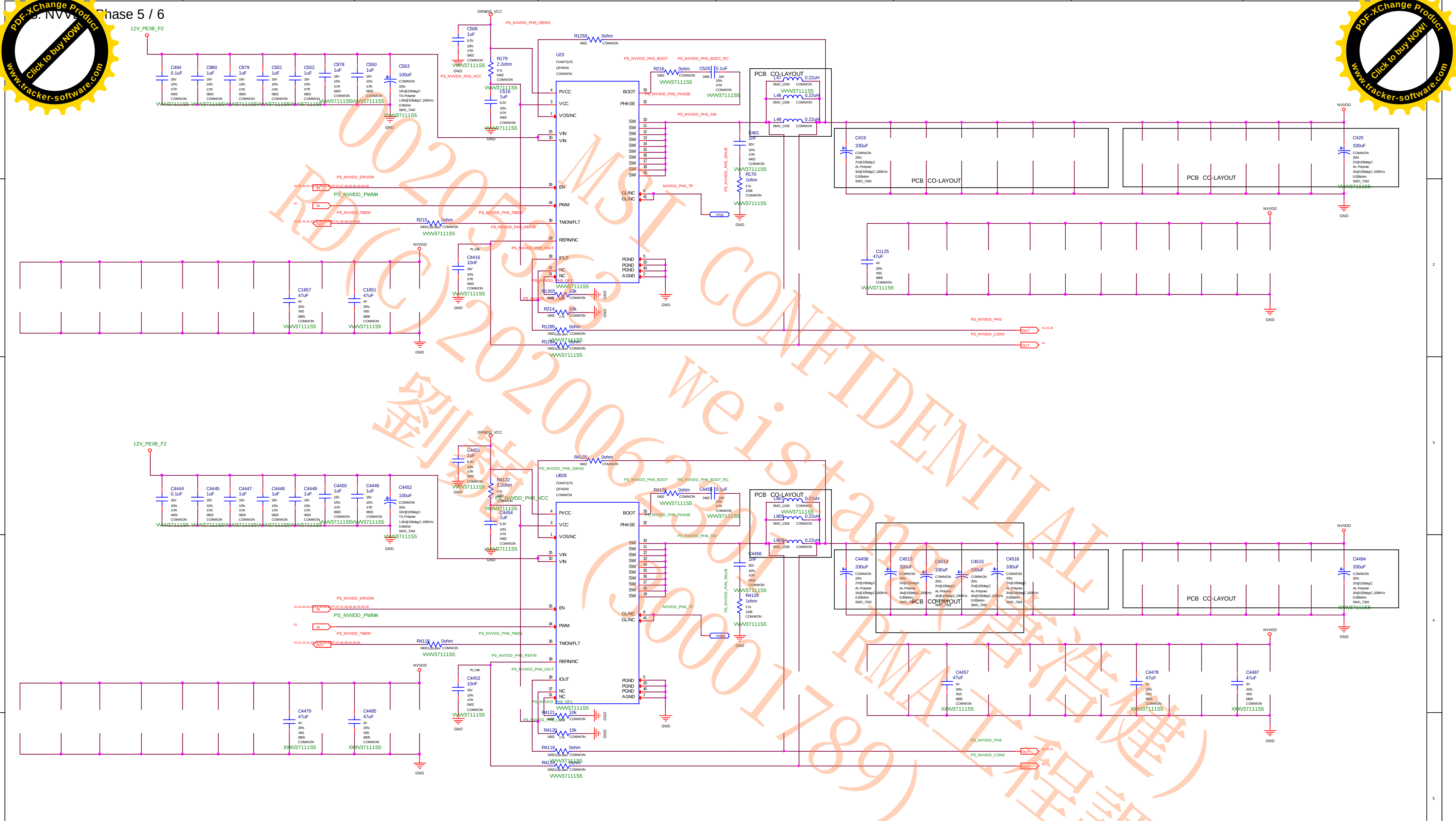
Date: Tuesday, April 09, 2019 Sheet 43 of 66

PS: NVVDD Phase 3, 4


DRMOS_VCC
12V_PEX8_F2
NVVDD
GND
U21
FDMF3170
QFN5X6
COMMON
PVCC
VCC
VOS/NC
VIN
EN
PWM
TMON/FLT
REFIN/NC
IOUT
NC
BOOT
PHASE
SW
GL/NC
PGND
AGND
U22
PS_NVVDD_PH3_ISENS
PS_NVVDD_PH3_BOOT
PS_NVVDD_PH3_PHASE
PS_NVVDD_PH3_SW
PS_NVVDD_PH3_VCC
PS_NVVDD_DRVON
PS_NVVDD_PWM3
PS_NVVDD_TMON
PS_NVVDD_PH3_TMON
PS_NVVDD_PH3_REFIN
PS_NVVDD_PH3_IOUT
NVVDD_PH3_TP
PS_NVVDD_PH3
PS_NVVDD_CSN3
PS_NVVDD_PH4_ISENS
PS_NVVDD_PH4_BOOT
PS_NVVDD_PH4_BOOT_RC
PS_NVVDD_PH4_PHASE
PS_NVVDD_PH4_SW
PS_NVVDD_PH4_VCC
PS_NVVDD_PWM3
PS_NVVDD_PH4_TMON
PS_NVVDD_PH4_REFIN
PS_NVVDD_PH4_IOUT
NVVDD_PH4_TP
PS_NVVDD_PH4
PS_NVVDD_CSN4
PCB CO-LAYOUT
L41 0.22uH
L42 0.22uH
L40 0.22uH
L44 0.22uH
L43 0.22uH
L45 0.22uH
C415 330uF
C416 330uF
C418 330uF
C437 330uF
C4509 330uF
C4512 330uF
C4510 330uF
C4511 330uF
C1835 47uF
C1881 47uF
C1117 47uF
C1118 47uF
C1119 47uF
C1856 47uF
WW37111S5

MICRO-STAR INT'L CO.,LTD	
MS-V371	
Size: Custom	Document Description: NVVDD PH3/4
Rev	2.1
Date: Tuesday, April 09, 2019	Sheet 44 of 66

5. NVVDD Phase 5 / 6



12V_PEX8_F2
DRMOS_VCC
PS_NVVDD_PH5_ISENS
R1259 0ohm
U23
FDMF3170
QFN56
PVCC
VCC
VOS/NC
VIN
EN
PWM
TMON/FLT
REFIN/NC
IOUT
NC
BOOT
PHASE
SW
GL/NC
PGND
AGND
PS_NVVDD_DRVON
PS_NVVDD_PWM4
PS_NVVDD_TMON
PS_NVVDD_PH5_BOOT
PS_NVVDD_PH5_BOOT_RC
PS_NVVDD_PH5_PHASE
PS_NVVDD_PH5_SW
PS_NVVDD_PH5_SNUB
NVVDD_PH5_TP
PCB CO-LAYOUT
L47 0.22uH
L46 0.22uH
L48 0.22uH
C419 330uF
C420 330uF
C1125 47uF
C1857 47uF
C1851 47uF
PS_NVVDD_PH5
PS_NVVDD_CSN5
NVVDD
GND
U828
PS_NVVDD_PH6_ISENS
PS_NVVDD_PH6_VCC
PS_NVVDD_PH6_BOOT
PS_NVVDD_PH6_BOOT_RC
PS_NVVDD_PH6_PHASE
PS_NVVDD_PH6_SW
PS_NVVDD_PH6_SNUB
NVVDD_PH6_TP
PS_NVVDD_PH6_TMON
PS_NVVDD_PH6_REFIN
PS_NVVDD_PH6_IOUT
L807 0.22uH
L808 0.22uH
L809 0.22uH
C4458 330uF
C4513 330uF
C4514 330uF
C4515 330uF
C4516 330uF
C4494 330uF
C4457 47uF
C4478 47uF
C4487 47uF
C4479 47uF
C4485 47uF
PS_NVVDD_PH6
PS_NVVDD_CSN6

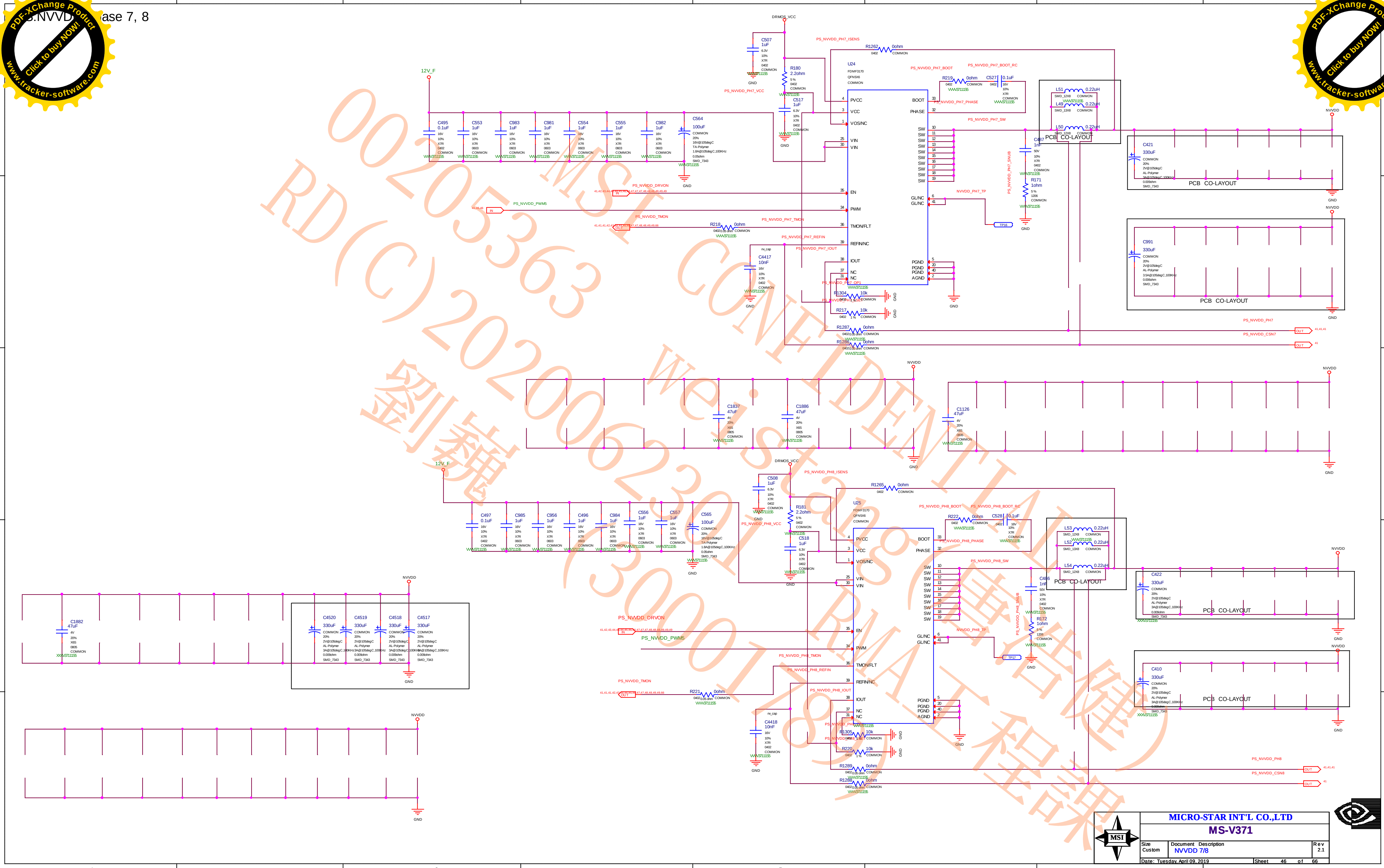
MICRO-STAR INT'L CO.,LTD

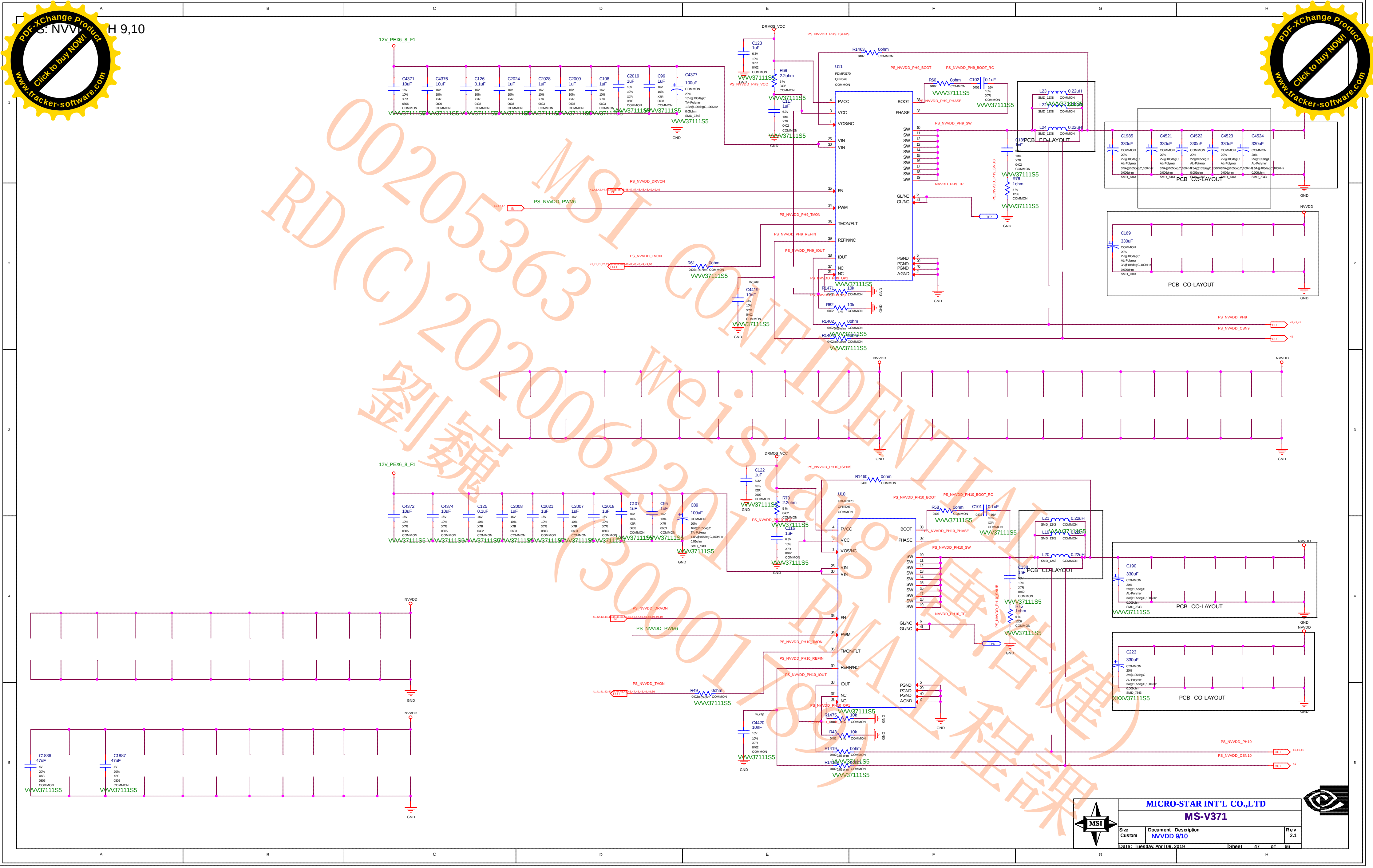
MS-V371

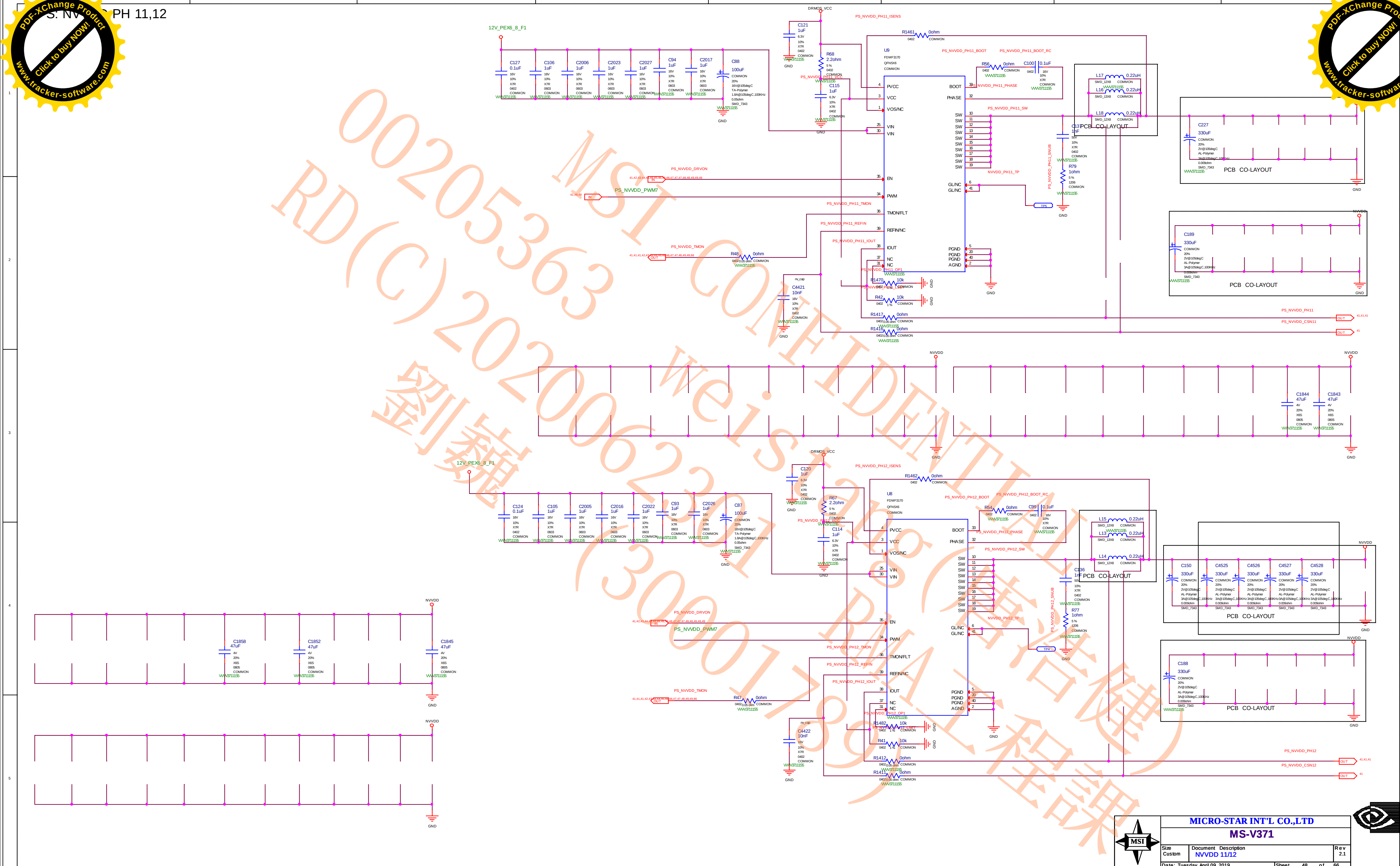
Size	Document Description	Rev
Custom	NVVDD 5/6	2.1

Date: Tuesday, April 09, 2019 Sheet 45 of 66

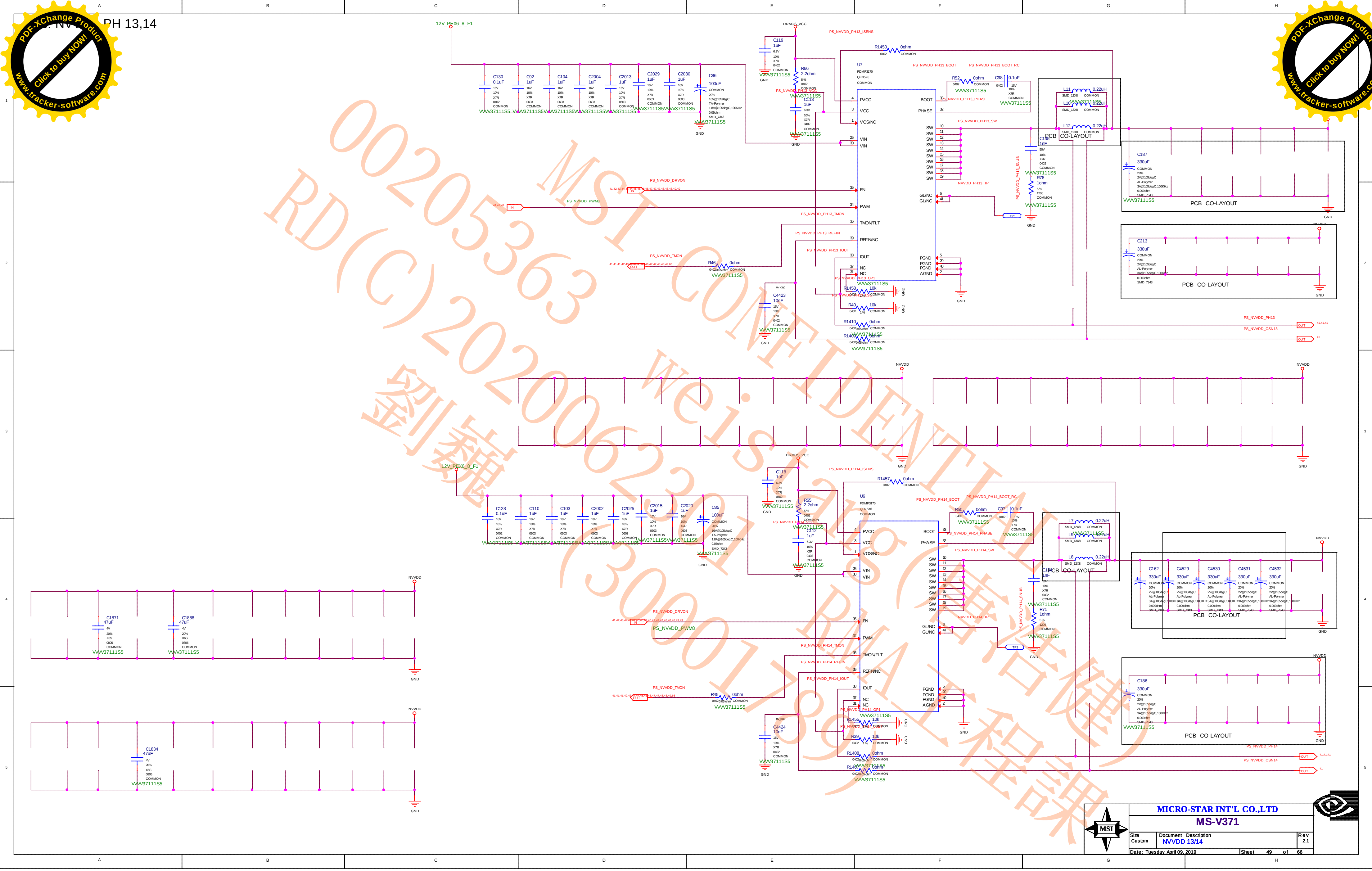
MS.NVVDD Phase 7, 8


DRMOS_VCC
12V_F
NVVDD
GND
U24
FDMF3170
QFN5X6
COMMON
PVCC
VCC
VOS/NC
VIN
EN
PWM
TMON/FLT
REFIN/NC
IOUT
NC
BOOT
PHASE
SW
GL/NC
PGND
AGND
PS_NVVDD_PH7_ISENS
PS_NVVDD_PH7_BOOT
PS_NVVDD_PH7_BOOT_RC
PS_NVVDD_PH7_PHASE
PS_NVVDD_PH7_SW
PS_NVVDD_PH7_VCC
PS_NVVDD_PH7_TMON
PS_NVVDD_PH7_REFIN
PS_NVVDD_PH7_IOUT
NVVDD_PH7_TP
PS_NVVDD_PH7
PS_NVVDD_CSN7
PS_NVVDD_DRVON
PS_NVVDD_PWM5
PS_NVVDD_TMON
U25
PS_NVVDD_PH8_ISENS
PS_NVVDD_PH8_BOOT
PS_NVVDD_PH8_BOOT_RC
PS_NVVDD_PH8_PHASE
PS_NVVDD_PH8_SW
PS_NVVDD_PH8_VCC
PS_NVVDD_PH8_TMON
PS_NVVDD_PH8_REFIN
PS_NVVDD_PH8_IOUT
NVVDD_PH8_TP
PS_NVVDD_PH8
PS_NVVDD_CSN8
PCB CO-LAYOUT
MICRO-STAR INT'L CO.,LTD
MS-V371
Size Custom
Document Description NVVDD 7/8
Rev 2.1
Date: Tuesday, April 09, 2019
Sheet 46 of 66


NVVDD PH 9,10
12V_PEX6_8_F1
DRMOS_VCC
PS_NVVDD_PH9_ISENS
PS_NVVDD_PH9_BOOT
PS_NVVDD_PH9_BOOT_RC
PS_NVVDD_PH9_PHASE
PS_NVVDD_PH9_SW
PS_NVVDD_DRVON
PS_NVVDD_PWM6
PS_NVVDD_PH9_TMON
PS_NVVDD_PH9_REFIN
PS_NVVDD_PH9_IOUT
PS_NVVDD_TMON
PS_NVVDD_PH9
PS_NVVDD_CSN9
U11
U10
PVCC
VCC
VOS/NC
VIN
EN
PWM
TMON/FLT
REFIN/NC
IOUT
NC
BOOT
PHASE
SW
GL/NC
PGND
AGND
PCB CO-LAYOUT
NVVDD
GND
PS_NVVDD_PH10_ISENS
PS_NVVDD_PH10_BOOT
PS_NVVDD_PH10_BOOT_RC
PS_NVVDD_PH10_PHASE
PS_NVVDD_PH10_SW
PS_NVVDD_PH10_TMON
PS_NVVDD_PH10_REFIN
PS_NVVDD_PH10_IOUT
PS_NVVDD_PH10
PS_NVVDD_CSN10
MICRO-STAR INT'L CO.,LTD
MS-V371
Size Custom
Document Description
NVVDD 9/10
Rev 2.1
Date: Tuesday, April 09, 2019
Sheet 47 of 66



MICRO-STAR INT'L CO.,LTD	
MS-V371	
Size: Custom	Document Description: NVVDD 11/12	Rev 2.1
Date: Tuesday, April 09, 2019	Sheet 48 of 66


PH 13,14
12V_PEX6_8_F1
DRMOS_VCC
NVVDD
GND
U7
U6
FDMF3170
QFN56
PVCC
VCC
VOS/NC
VIN
EN
PWM
TMON/FLT
REFIN/NC
IOUT
NC
BOOT
PHASE
SW
GL/NC
PGND
AGND
PS_NVVDD_PH13_ISENS
PS_NVVDD_PH13_BOOT
PS_NVVDD_PH13_BOOT_RC
PS_NVVDD_PH13_PHASE
PS_NVVDD_PH13_SW
PS_NVVDD_PH13_TP
PS_NVVDD_PH13_SNUB
PS_NVVDD_PH13_TMON
PS_NVVDD_PH13_REFIN
PS_NVVDD_PH13_IOUT
PS_NVVDD_PH13
PS_NVVDD_CSN13
PS_NVVDD_PH14_ISENS
PS_NVVDD_PH14_BOOT
PS_NVVDD_PH14_BOOT_RC
PS_NVVDD_PH14_PHASE
PS_NVVDD_PH14_SW
PS_NVVDD_PH14_TP
PS_NVVDD_PH14_TMON
PS_NVVDD_PH14_REFIN
PS_NVVDD_PH14_IOUT
PS_NVVDD_PH14
PS_NVVDD_CSN14
PS_NVVDD_DRVON
PS_NVVDD_PWM8
PS_NVVDD_TMON
PCB CO-LAYOUT
MICRO-STAR INT'L CO.,LTD
MS-V371
Size Custom
Document Description
NVVDD 13/14
Rev 2.1
Date: Tuesday, April 09, 2019
Sheet 49 of 66

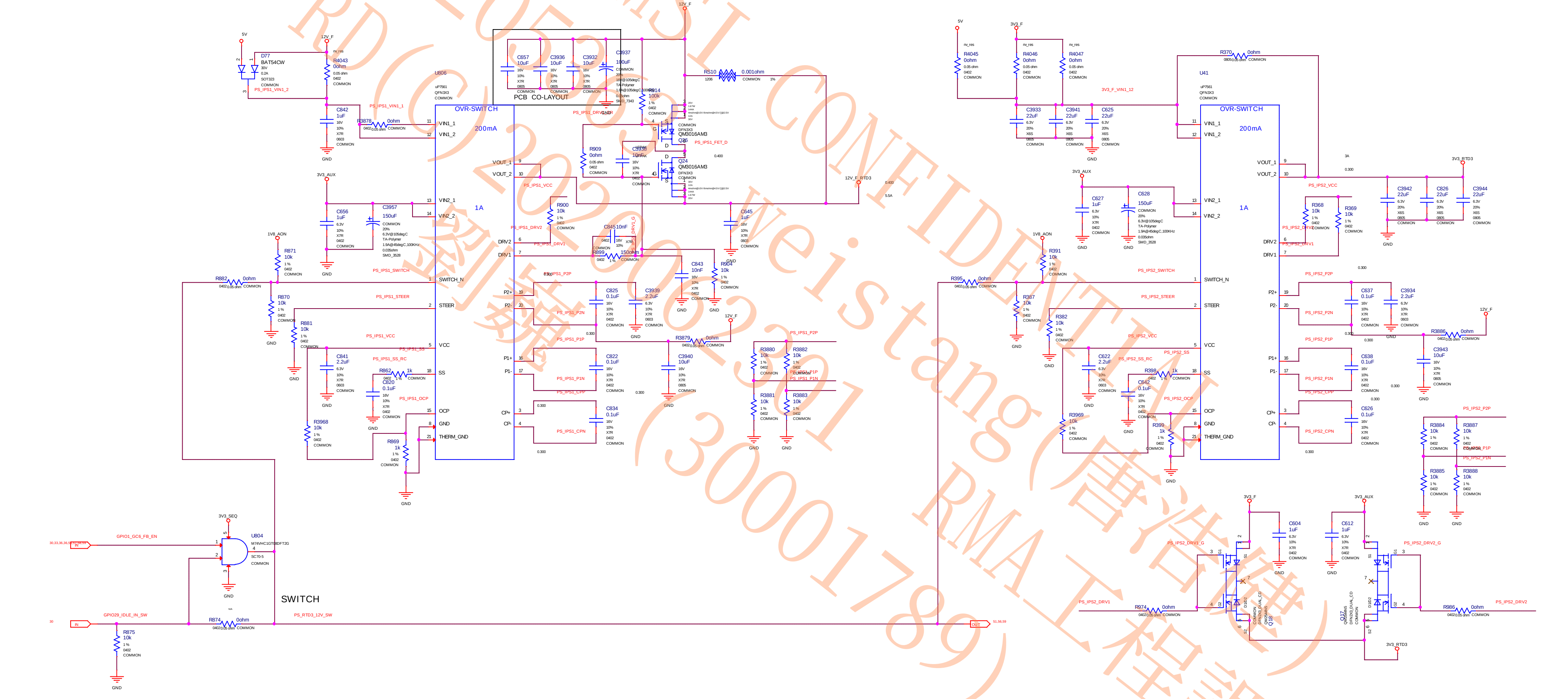
PS: INP[illegible]SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

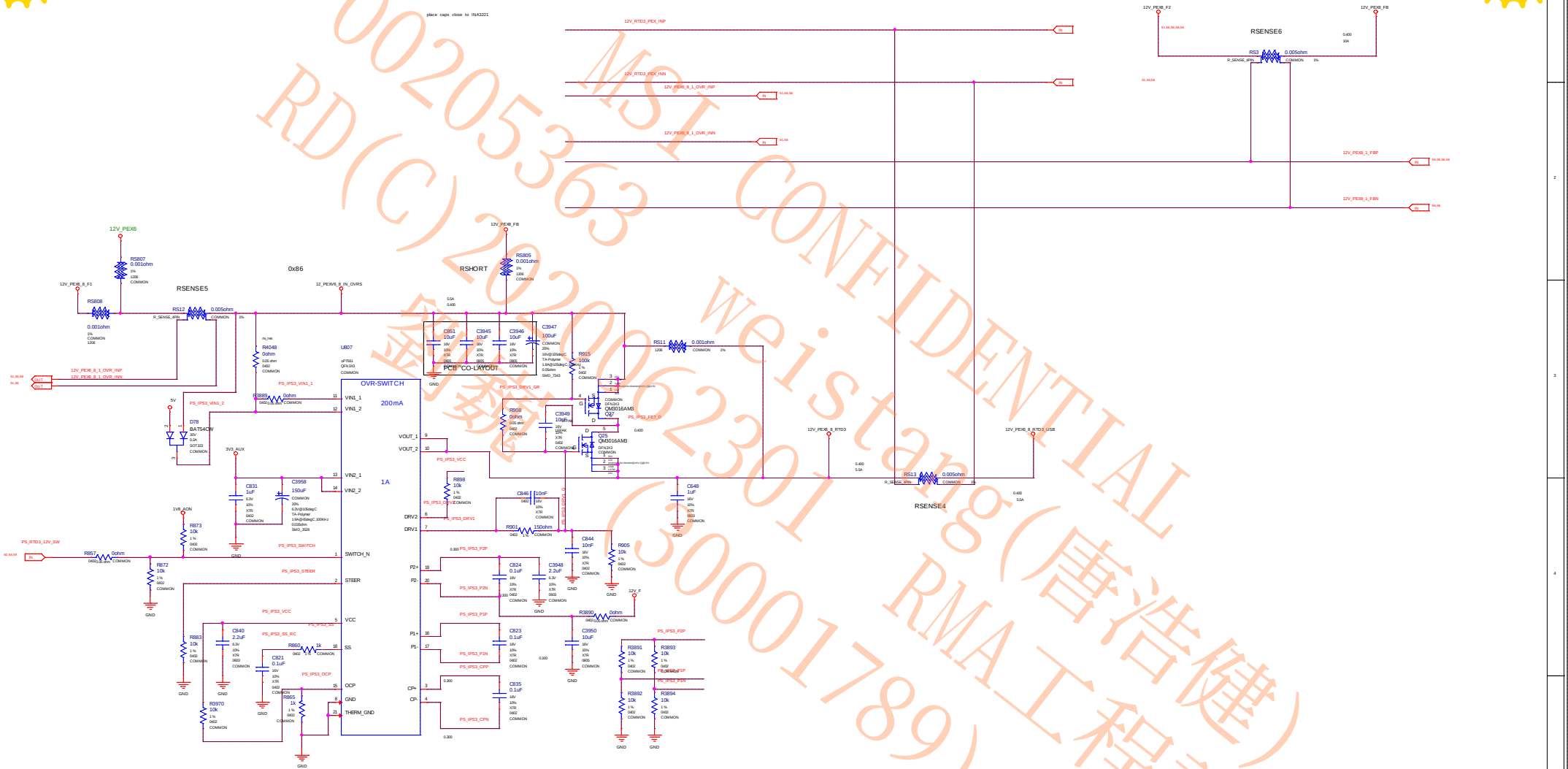


MICRO-STAR INT'L CO.,LTD

MS-V371

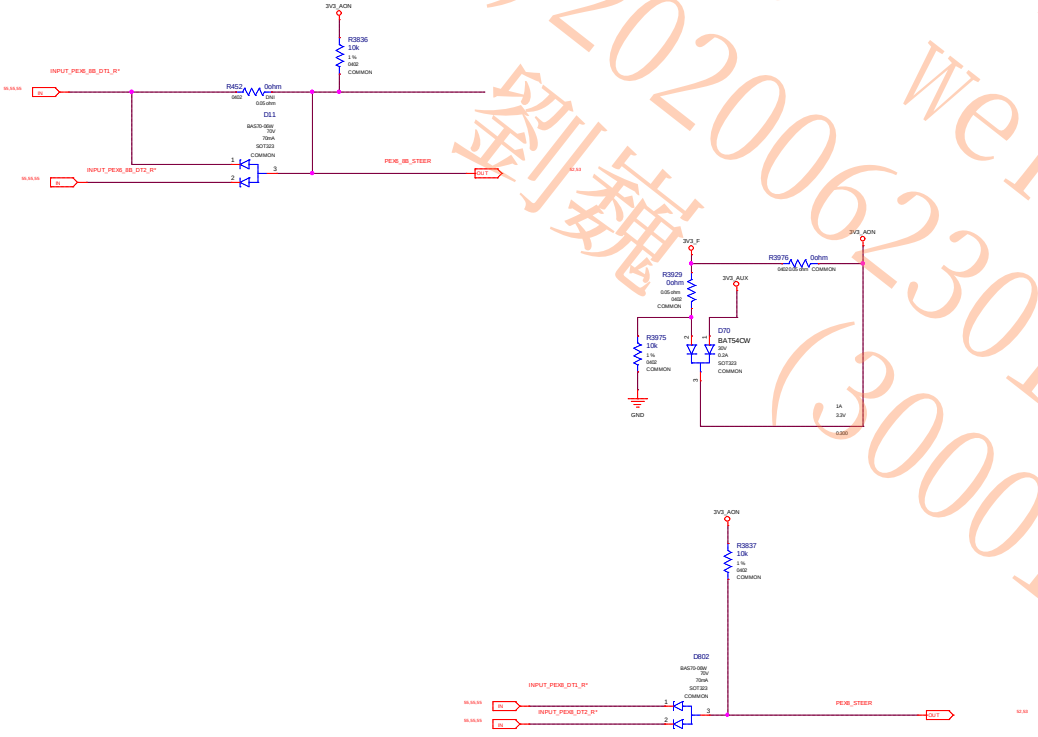
Size	Document Description	Rev
Custom	RTD3	2.1

Date: Tuesday, April 09, 2019 Sheet 50 of 66



MICRO-STAR INT'L CO.,LTD		
MS-V371		
Size: Custom	Document Description: RTD3 USB	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 51 of 66	

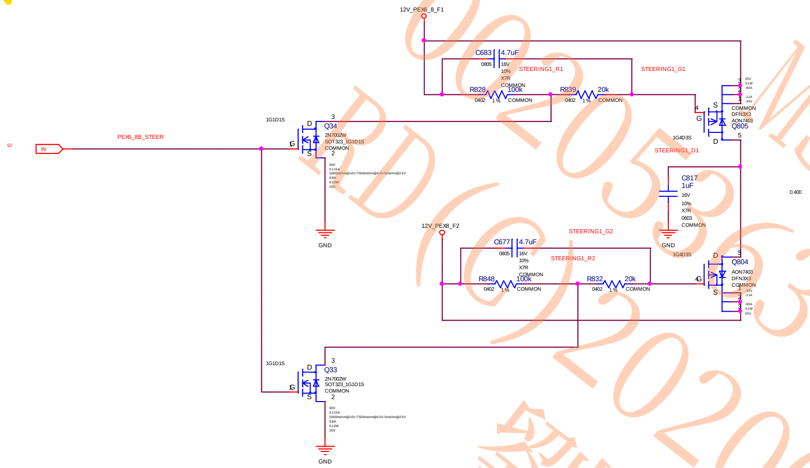
5. Input Switch Rail Balance



MICRO-STAR INT'L CO.,LTD		
MS-V371		
Size: Custom	Document Description: BALA	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 52 of 66	

12V CURRENT STEERING (UNDER POWER BOOT):

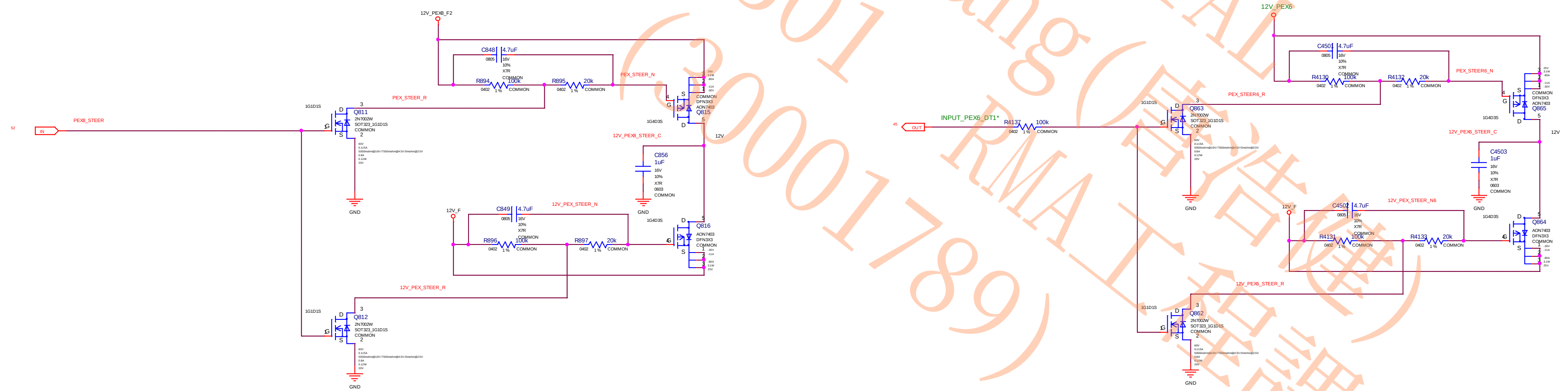
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



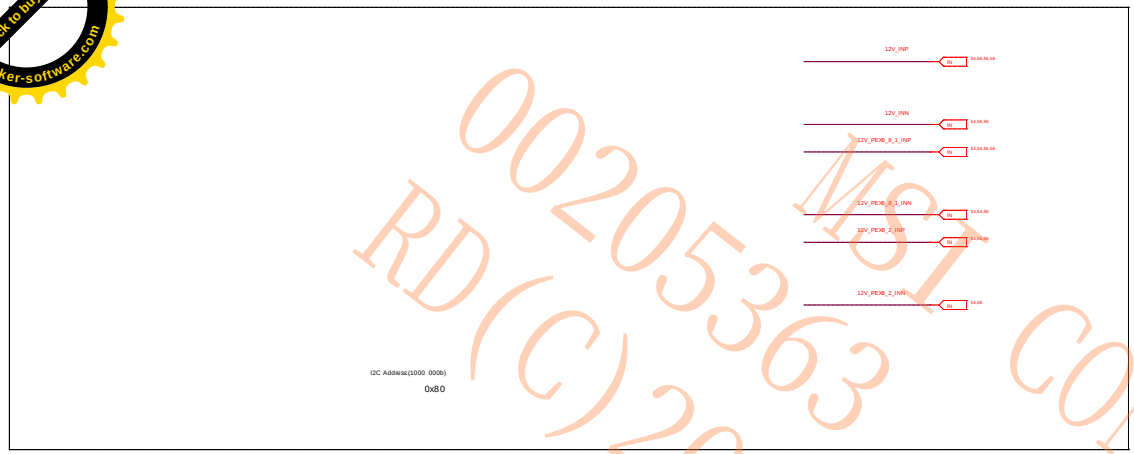
12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

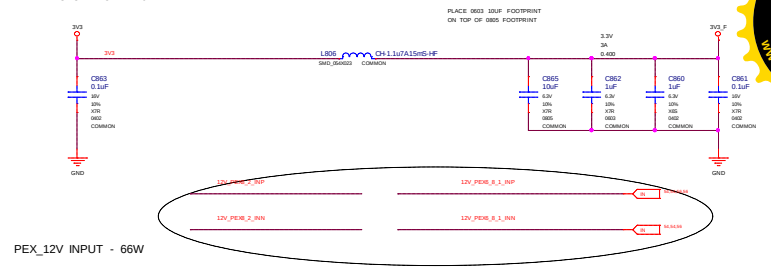
For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



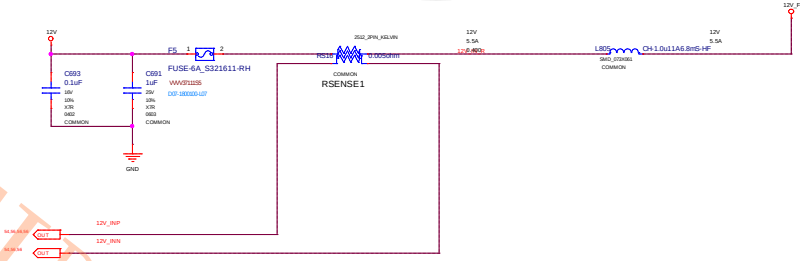
MICRO-STAR INT'L CO.,LTD		
MS-V371		
Size: Custom	Document Description: steering	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 53 of 66	

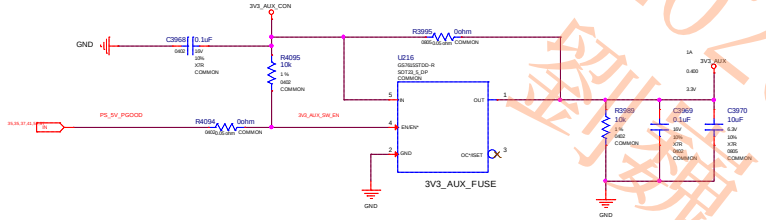


PEX 3V3 INPUT - 10W

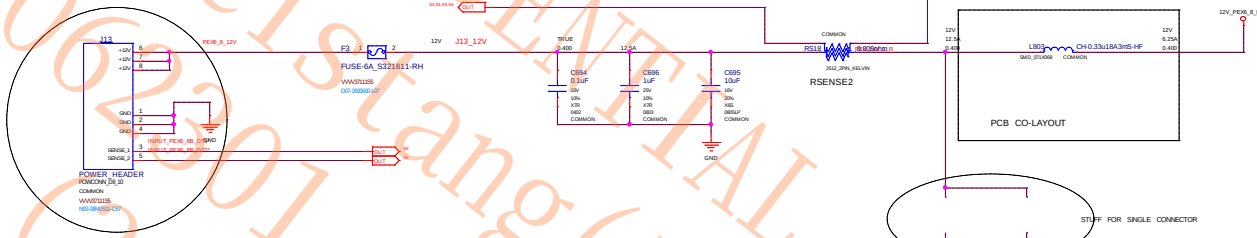


PEX_12V INPUT - 66W

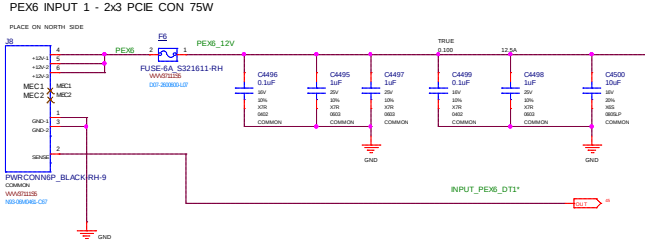




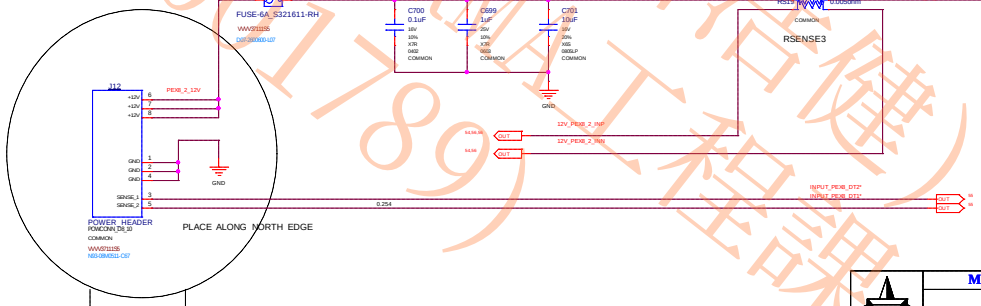
PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



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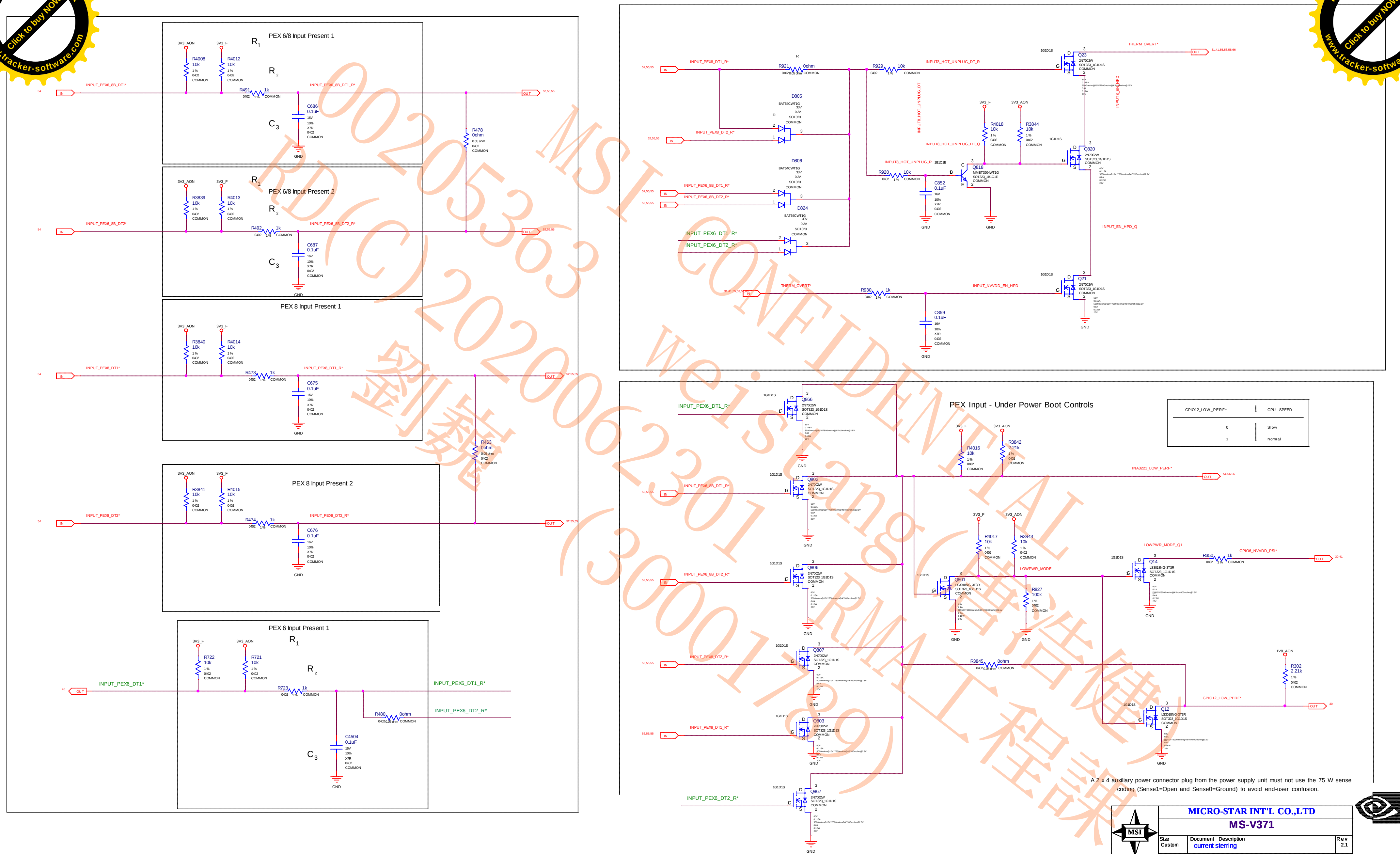
	MS-V371	
Size: Custom	Document Description: Input filter	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 54 of 66	

12V Current Steering & Hot Unplug Detect



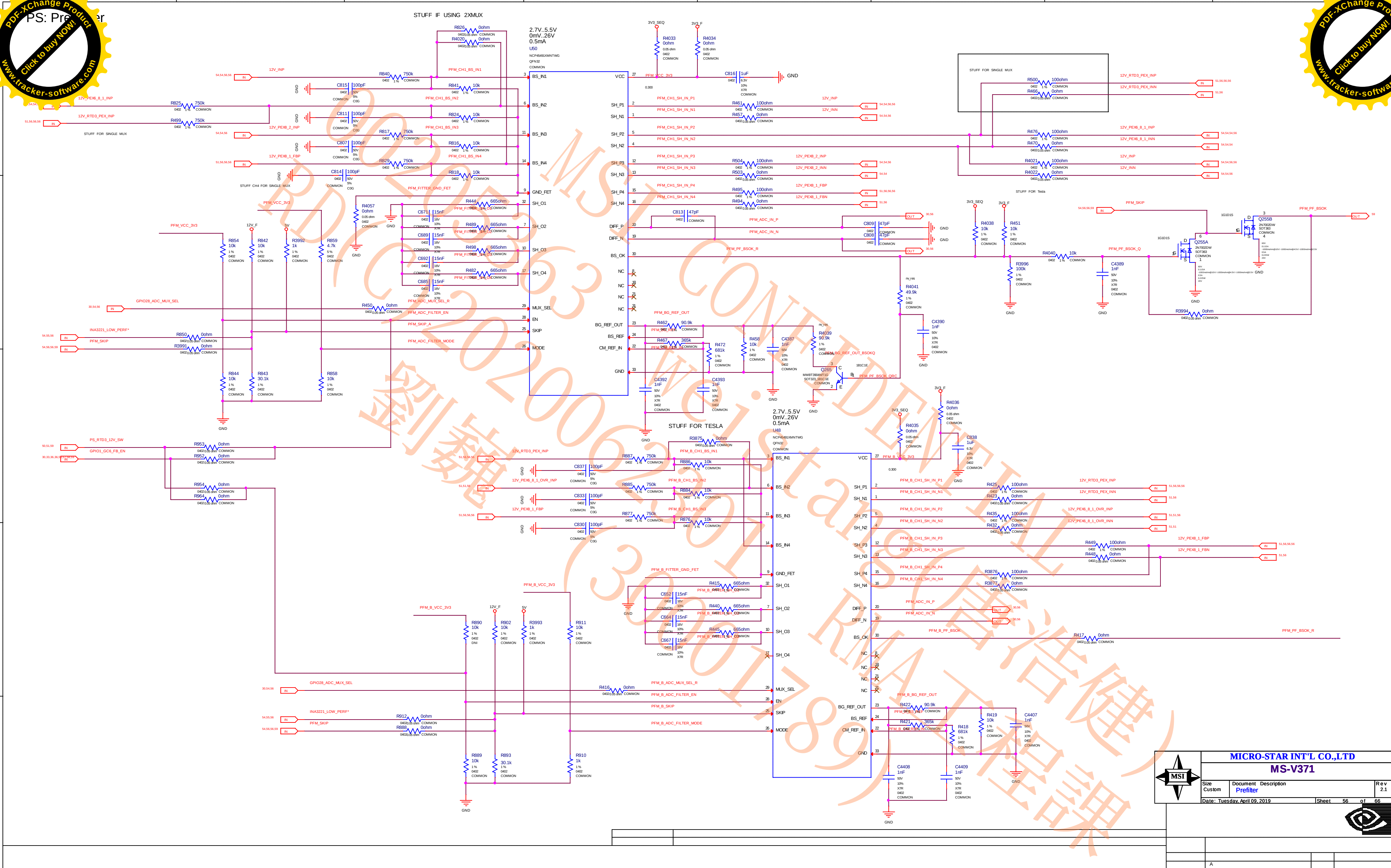
A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

MICRO-STAR INT'L CO.,LTD

MS-V371

Size	Document Description	Rev
Custom	current sterring	2.1

Date: Tuesday, April 09, 2019 Sheet 55 of 66


PS: Prefilter
STUFF IF USING 2XMUX
2.7V..5.5V
0mV..26V
0.5mA
U50
NCP45491XMNTWG
QFN32
STUFF FOR SINGLE MUX
STUFF CH4 FOR SINGLE MUX
STUFF FOR Tesla
STUFF FOR TESLA
2.7V..5.5V
0mV..26V
0.5mA
U48
NCP45491XMNTWG
QFN32
BS_IN1
BS_IN2
BS_IN3
BS_IN4
GND_FET
SH_O1
SH_O2
SH_O3
SH_O4
MUX_SEL
EN
SKIP
MODE
VCC
SH_P1
SH_N1
SH_P2
SH_N2
SH_P3
SH_N3
SH_P4
SH_N4
DIFF_P
DIFF_N
BS_OK
NC
BG_REF_OUT
BS_REF
CM_REF_IN
GND
12V_INP
12V_RTD3_PEX_INP
12V_RTD3_PEX_INN
12V_PEX8_1_INP
12V_PEX8_1_INN
12V_PEX8_2_INP
12V_PEX8_2_INN
12V_PEX8_1_FBP
12V_PEX8_1_FBN
PFM_VCC_3V3
PFM_SKIP
PFM_PF_BSOK
GPIO28_ADC_MUX_SEL
INA3221_LOW_PERF*
PS_RTD3_12V_SW
GPIO1_GC6_FB_EN
3V3_SEQ
3V3_F
12V_F
5V
Q255A
Q255B
Q265

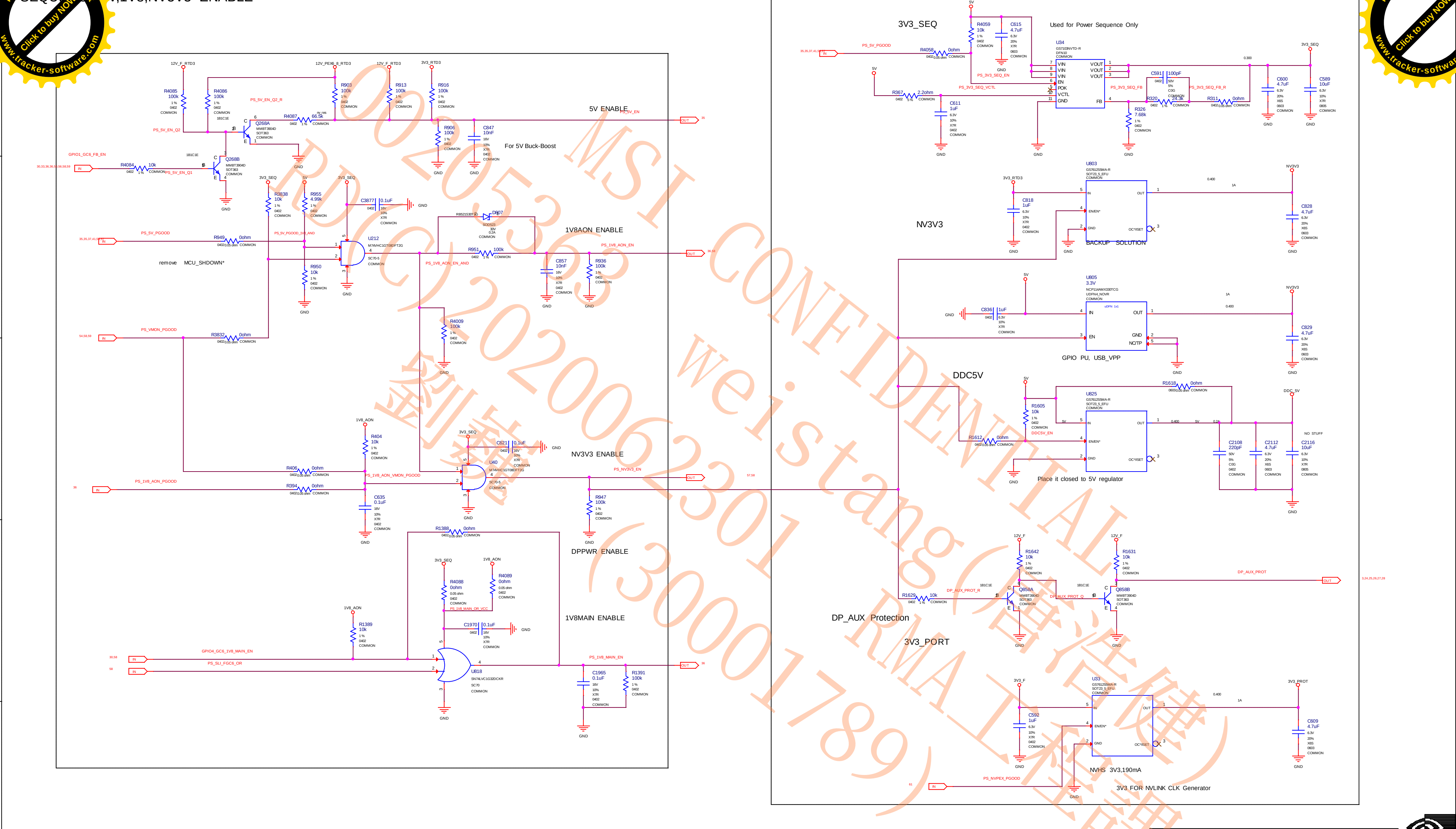
MICRO-STAR INT'L CO.,LTD

MS-V371

Size	Document Description	Rev
Custom	Prefilter	2.1

Date: Tuesday, April 09, 2019 Sheet 56 of 66

SEQUE... 5V,1V8,NV3V3 ENABLE



ASSEMBLY
PAGE DETAIL

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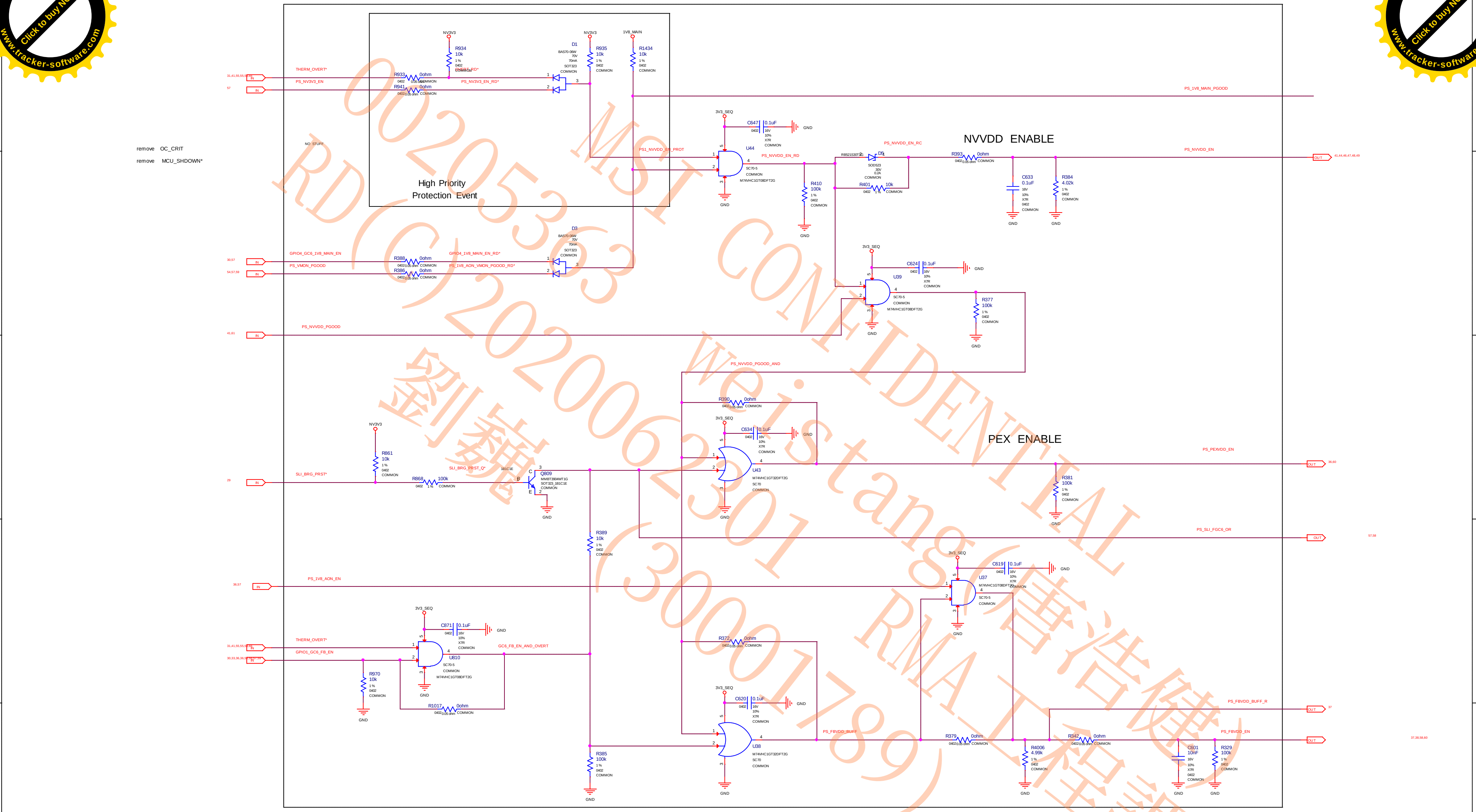
Sequence: 5V, 1V8, NV3V3 EN

MICRO-STAR INT'L CO.,LTD
MS-V371

Size	Document Description	Rev
Custom	5V/1V8/NV 3V3	2.1

Date: Tuesday, April 09, 2019 | Sheet 57 of 66

SEQUENCE:NV,PEX,FB ENABLE



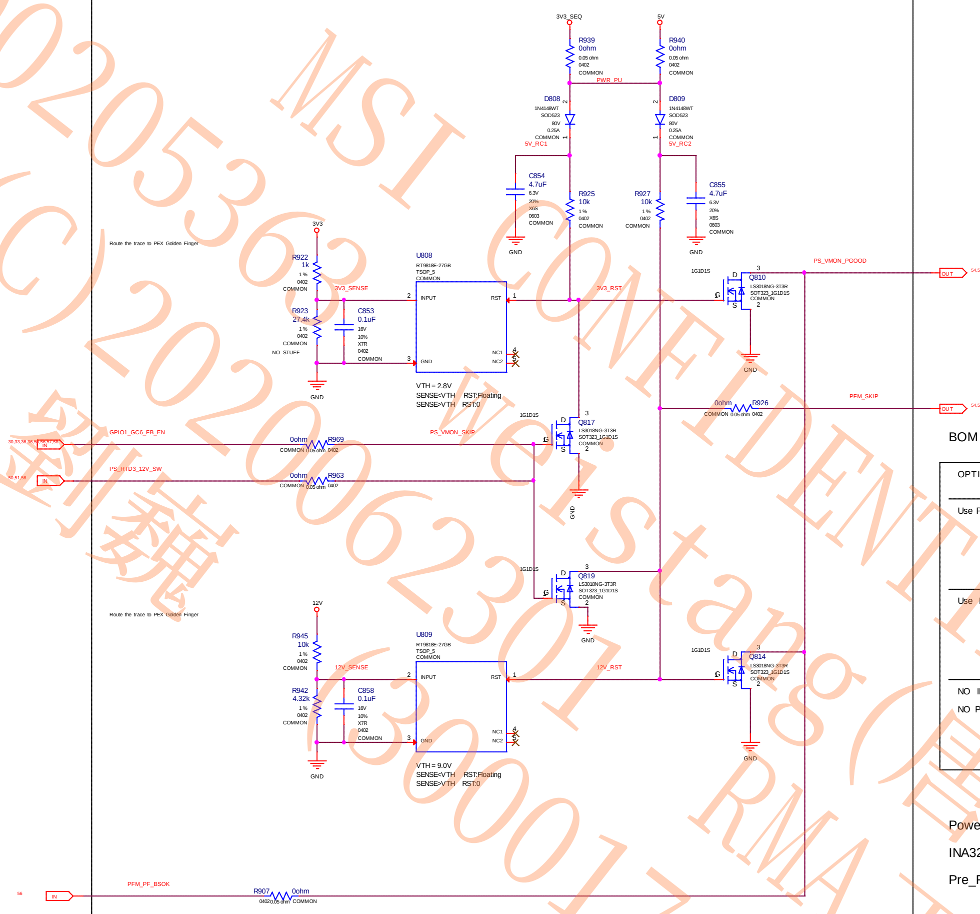
MICRO-STAR INT'L CO.,LTD

MS-V371

Size	Document Description	Rev
Custom	SEQUENCE:NV,PEX,FB ENABLE	2.1

Date: Tuesday, April 09, 2019 Sheet 58 of 66

PCIE Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

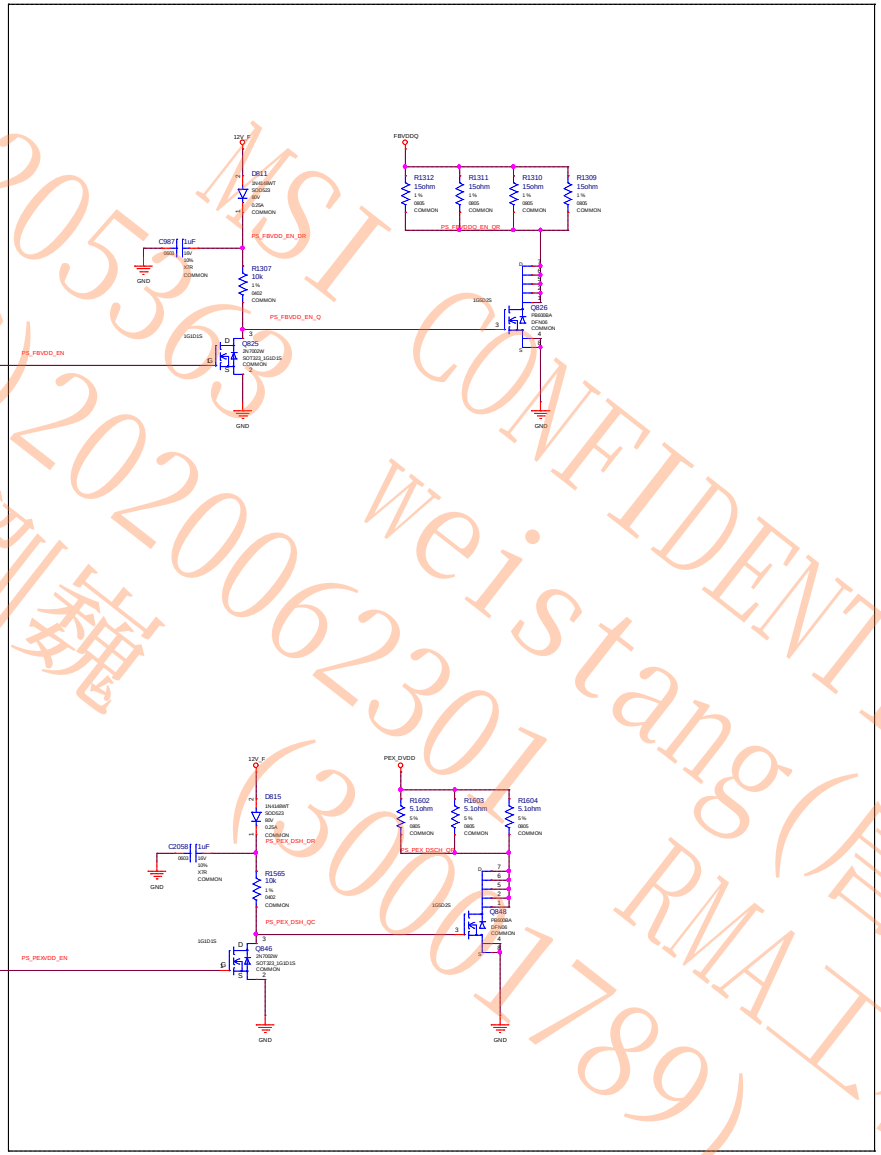
INA3221:3V3_SEQ

Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

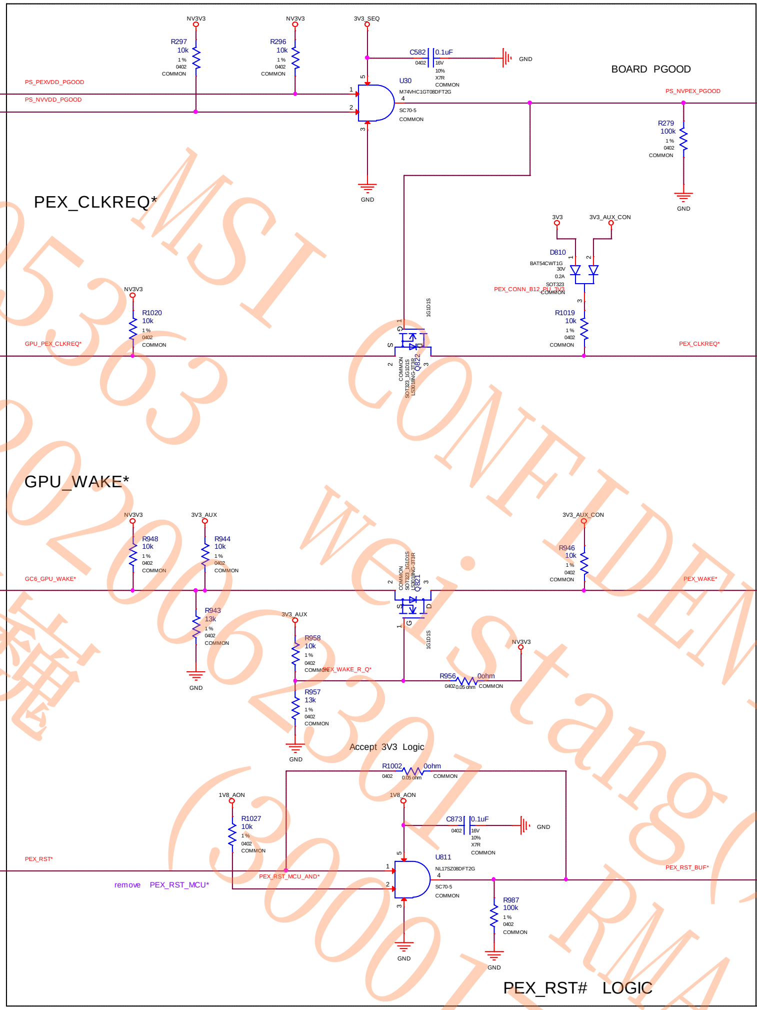
Only use the Primary Pre-Filter to sense 3V3PEX

and All Input 12Vs



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V371	
Size: Custom	Document Description: SEQUENCE:Discharge	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 60 of 66	

SEQU[illegible] MISC



BOARD PGOOD
PEX_CLKREQ*
GPU_WAKE*
Accept 3V3 Logic
PEX_RST# LOGIC
NV3V3
3V3_SEQ
R297 10k
R296 10k
C582 0.1uF
GND
U30
PS_PEXVDD_PGOOD
PS_NVVDD_PGOOD
PS_NVPEX_PGOOD
R279 100k
3V3
3V3_AUX_CON
D810
BAT54CWT1G
PEX_CONN_B12_PU_3V3
R1019 10k
R1020 10k
GPU_PEX_CLKREQ*
PEX_CLKREQ*
3V3_AUX
R948 10k
R944 10k
R946 10k
GC6_GPU_WAKE*
PEX_WAKE*
R943 13k
R958 10k
R957 13k
PEX_WAKE_R_Q*
R956 0ohm
R1002 0ohm
1V8_AON
R1027 10k
C873 0.1uF
U811
PEX_RST*
PEX_RST_MCU_AND*
remove PEX_RST_MCU*
PEX_RST_BUF*
R987 100k
IN
OUT
COMMON

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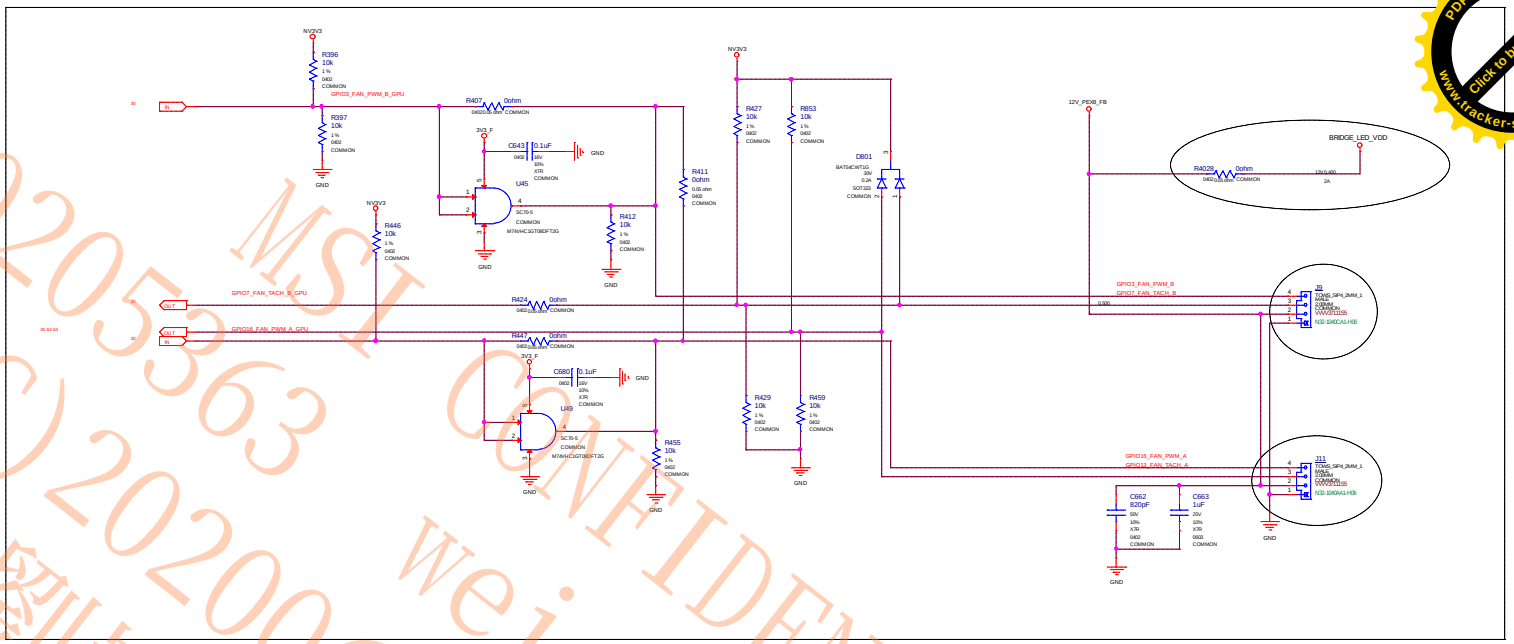
MS-V371

Size	Document Description	Rev
Custom	MISC	2.1

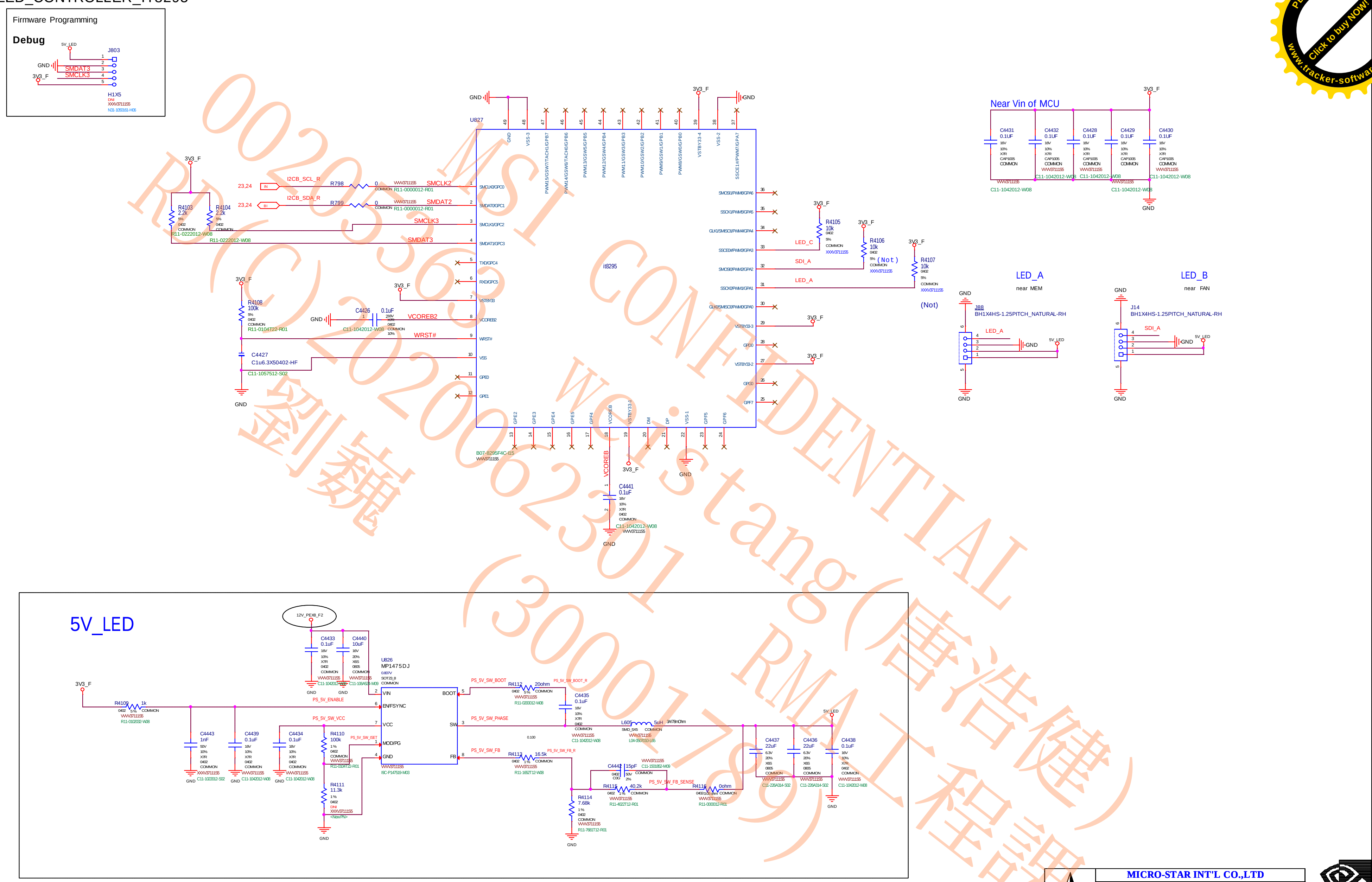
Date: Tuesday, April 09, 2019 Sheet 61 of 66

MISC: F[illegible] LED1



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V371	
Size: Custom	Document Description: MISC: FAN & LED1	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 63 of 66	

LED_CONTROLLER_IT8295



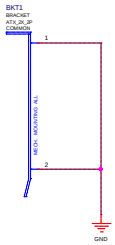
Firmware Programming
Debug
J803
H1X5
GND
3V3_F
5V_LED
SMDAT3
SMCLK3
U827
IT8295
B07-8295F4C-I15
I2CB_SCL_R
I2CB_SDA_R
R798
R799
SMCLK2
SMDAT2
SMCLK3
SMDAT3
R4103 2.2k
R4104 2.2k
R4108 100k
C4426 0.1uF
C4427 C1u6.3X50402-HF
VCOREB2
WRST#
VCOREB
C4441 0.1uF
LED_C
SDI_A
LED_A
R4105 10k
R4106 10k
R4107 10k
(Not)
Near Vin of MCU
C4431 0.1UF
C4432 0.1UF
C4428 0.1UF
C4429 0.1UF
C4430 0.1UF
LED_A
near MEM
J88
BH1X4HS-1.25PITCH_NATURAL-RH
LED_B
near FAN
J14
BH1X4HS-1.25PITCH_NATURAL-RH
5V_LED
12V_PEX8_F2
U826
MP1475DJ
C4433 0.1uF
C4440 10uF
VIN
EN/SYNC
VCC
MOD/PG
GND
BOOT
SW
FB
PS_5V_ENABLE
PS_5V_VCC
PS_5V_SW_BOOT
PS_5V_SW_PHASE
PS_5V_SW_FB
R4109 1k
C4443 1nF
C4439 0.1uF
C4434 0.1uF
R4110 100k
R4111 11.3k
R4112 20ohm
C4435 0.1uF
L605 5uH
R4113 16.5k
C4442 15pF
R4115 40.2k
R4114 7.68k
R4116 0ohm
PS_5V_SW_FB_SENSE
C4437 22uF
C4436 22uF
C4438 0.1uF

MICRO-STAR INT'L CO.,LTD		
MS-V371		
Size: Custom	Document Description: LED	Rev 2.1
Date: Tuesday, April 09, 2019	Sheet 63 of 66	

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V371	
Size: Custom	Document Description: ZERO IDLE POWER MCU	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 64 of 66	

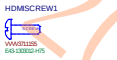
Mechanical Bracket/Thermal Solution

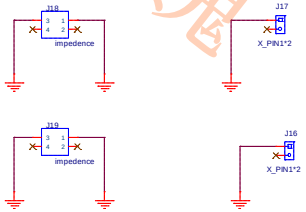
Brackets:

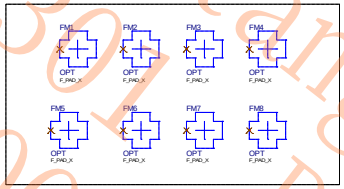


Bracket Screw

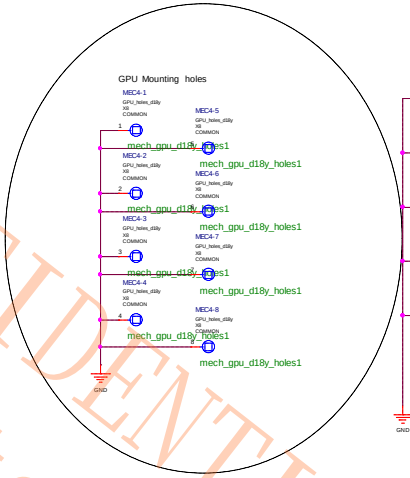
Screw



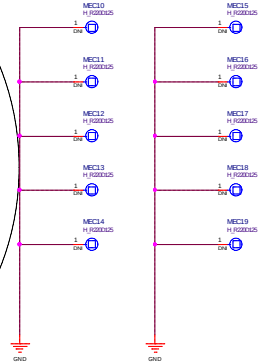




0 7 2 6 避開鈑金點 螺絲 孔 位



Mechanical Holes Symbol



MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V371	
Size: Custom	Document Description: MECH	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 65 of 66	

THERMAL PROTECTION

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V371	
Size: Custom	Document Description: VR THERMAL PROTECTION	Rev: 2.1
Date: Tuesday, April 09, 2019	Sheet 66 of 66	