

PG180-A03

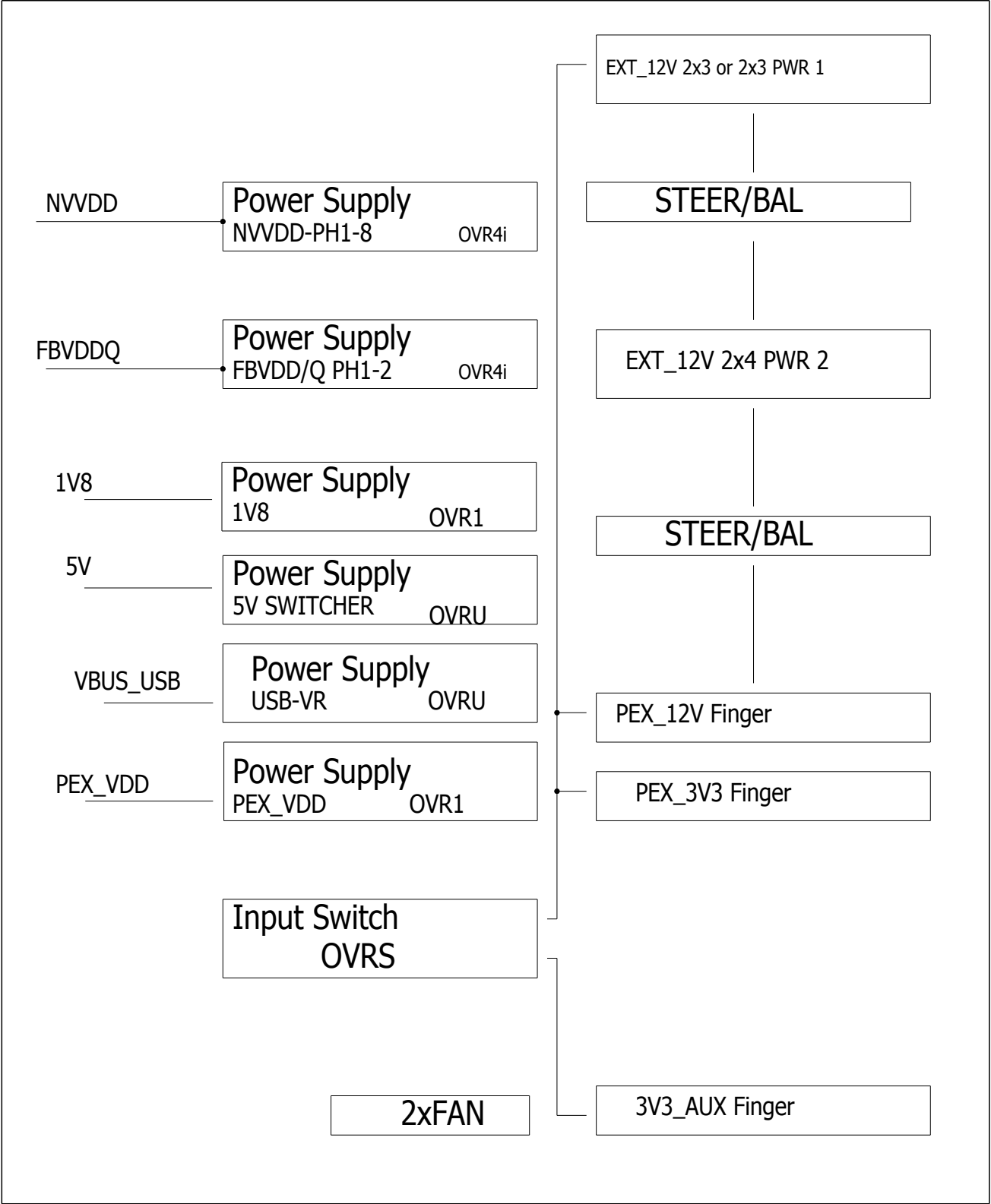
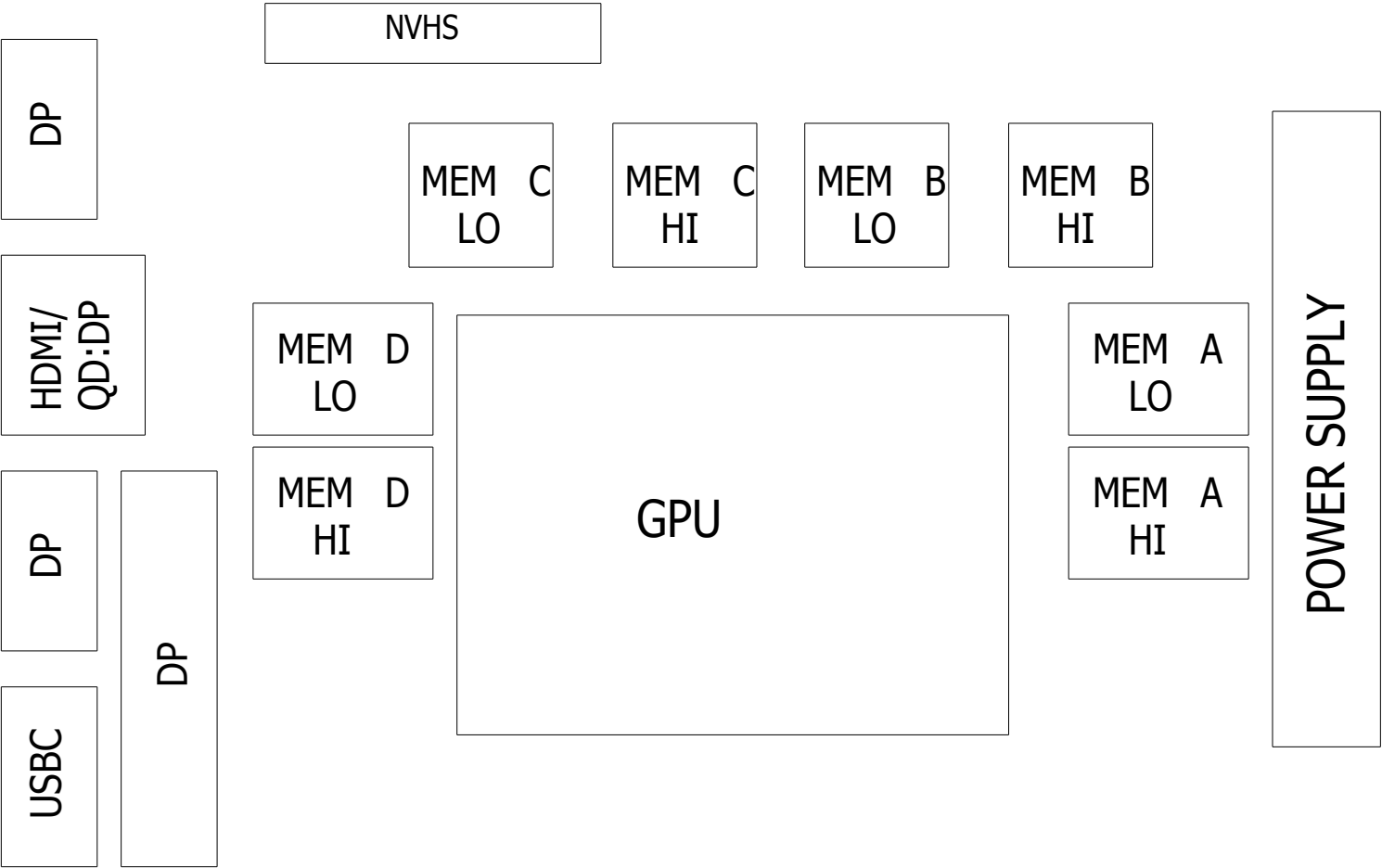
256b GDDR6 x16

TALL DP + DP + DP + HDMI/DP + USB

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Page2: Block Diagram

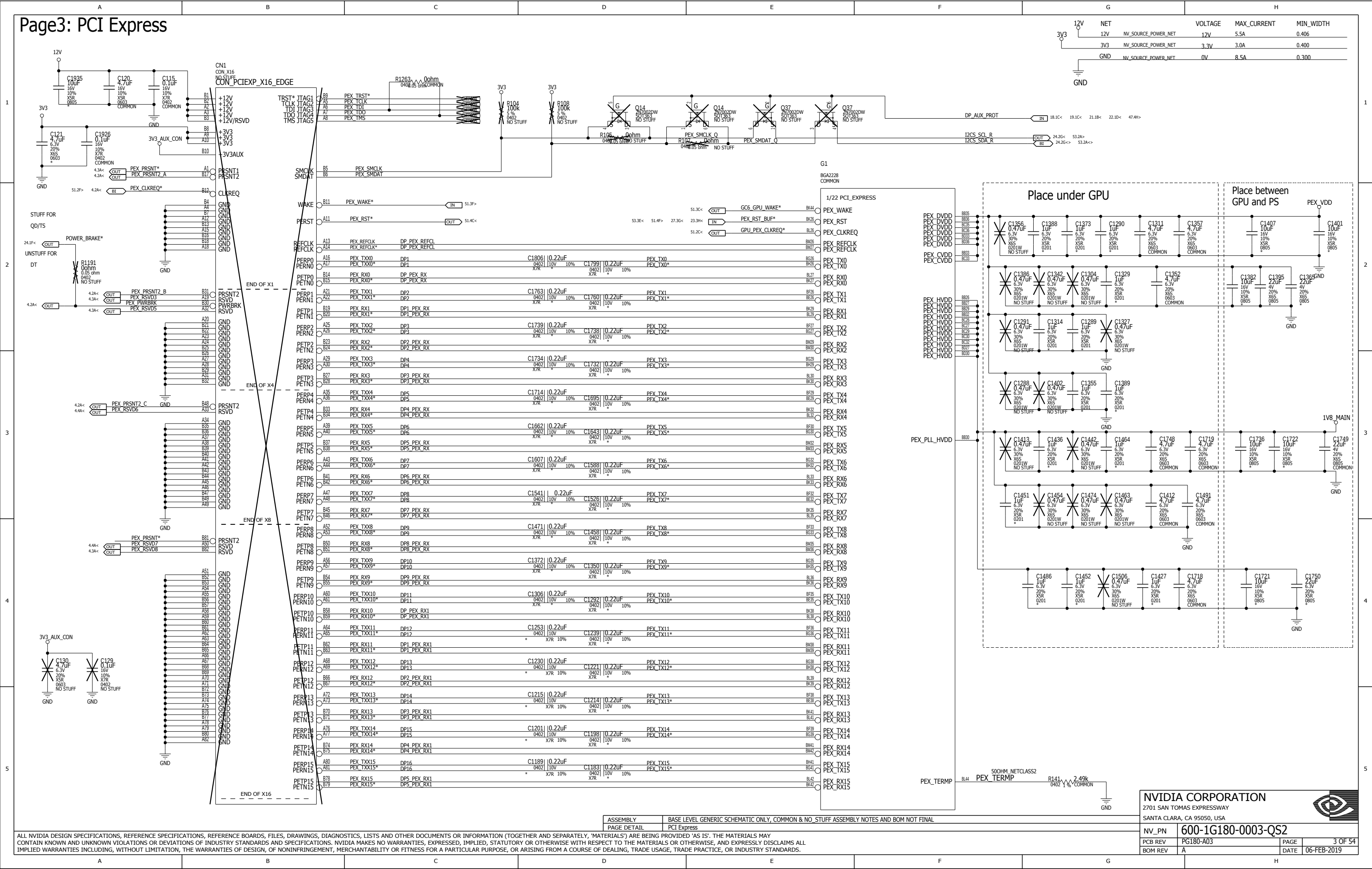


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	Block Diagram

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Page3: PCI Express



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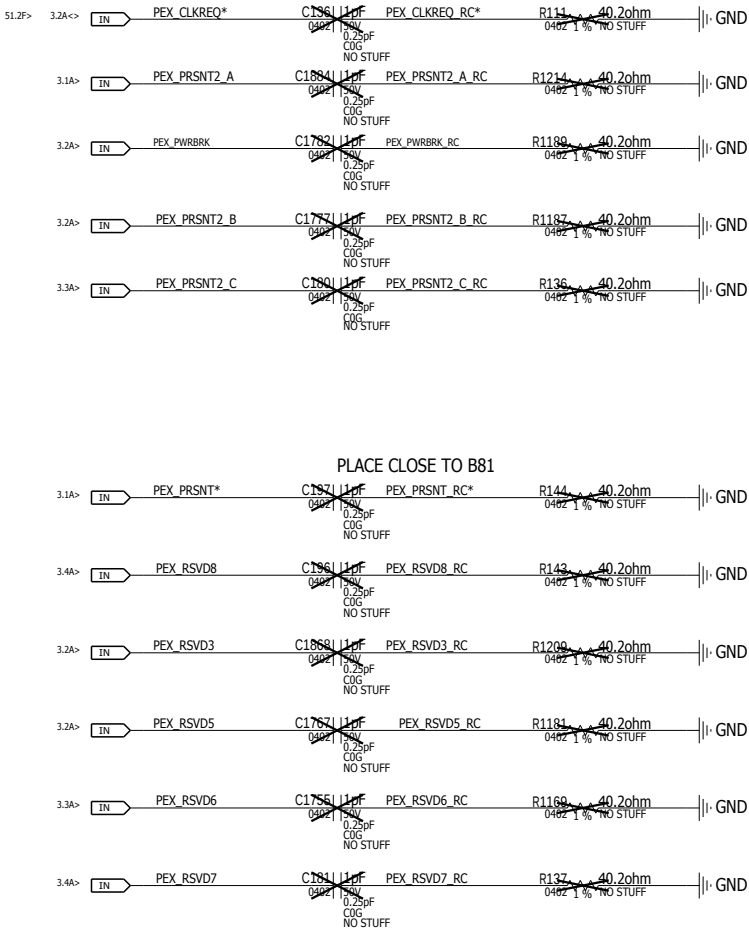
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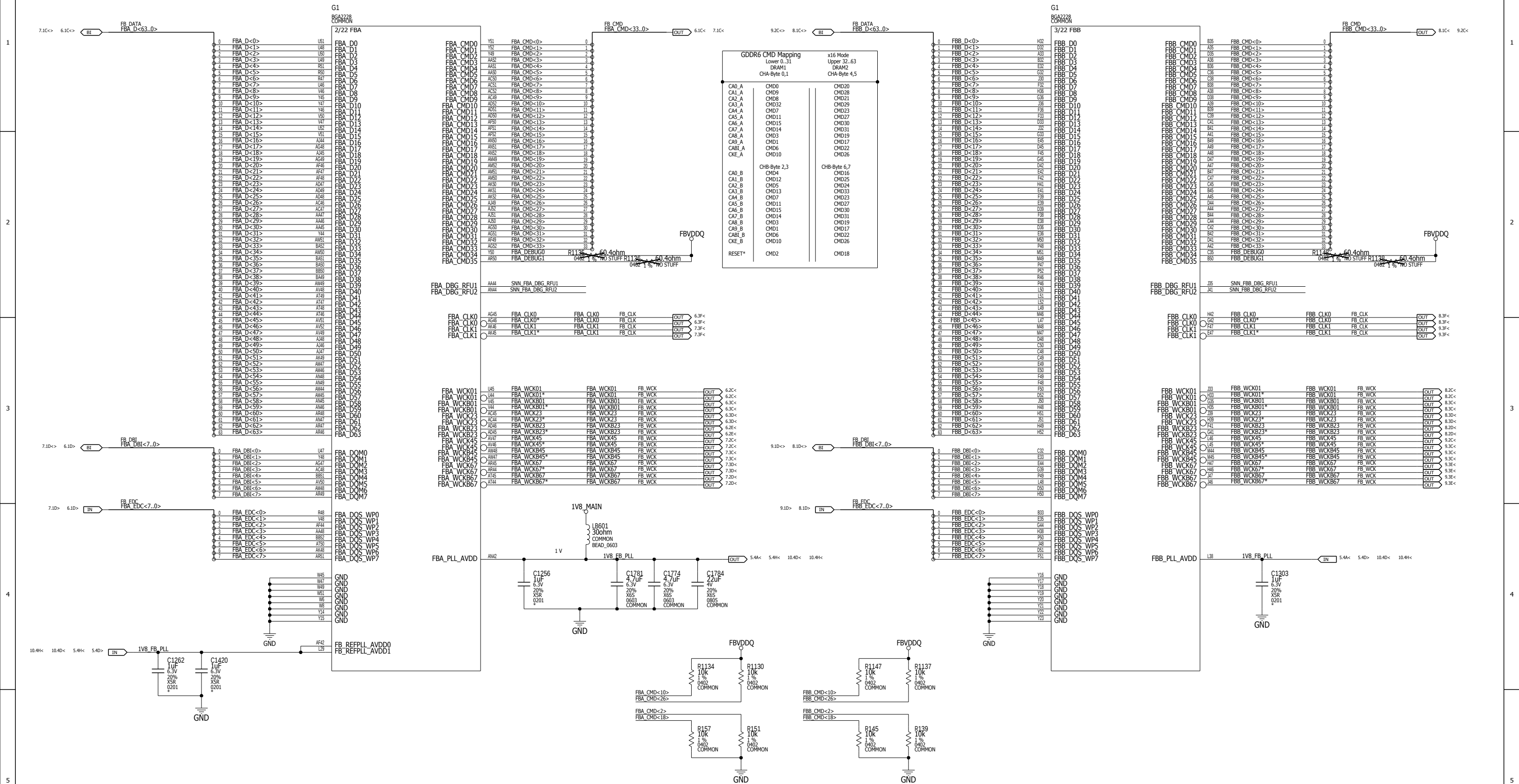
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Page4: PCI Termination

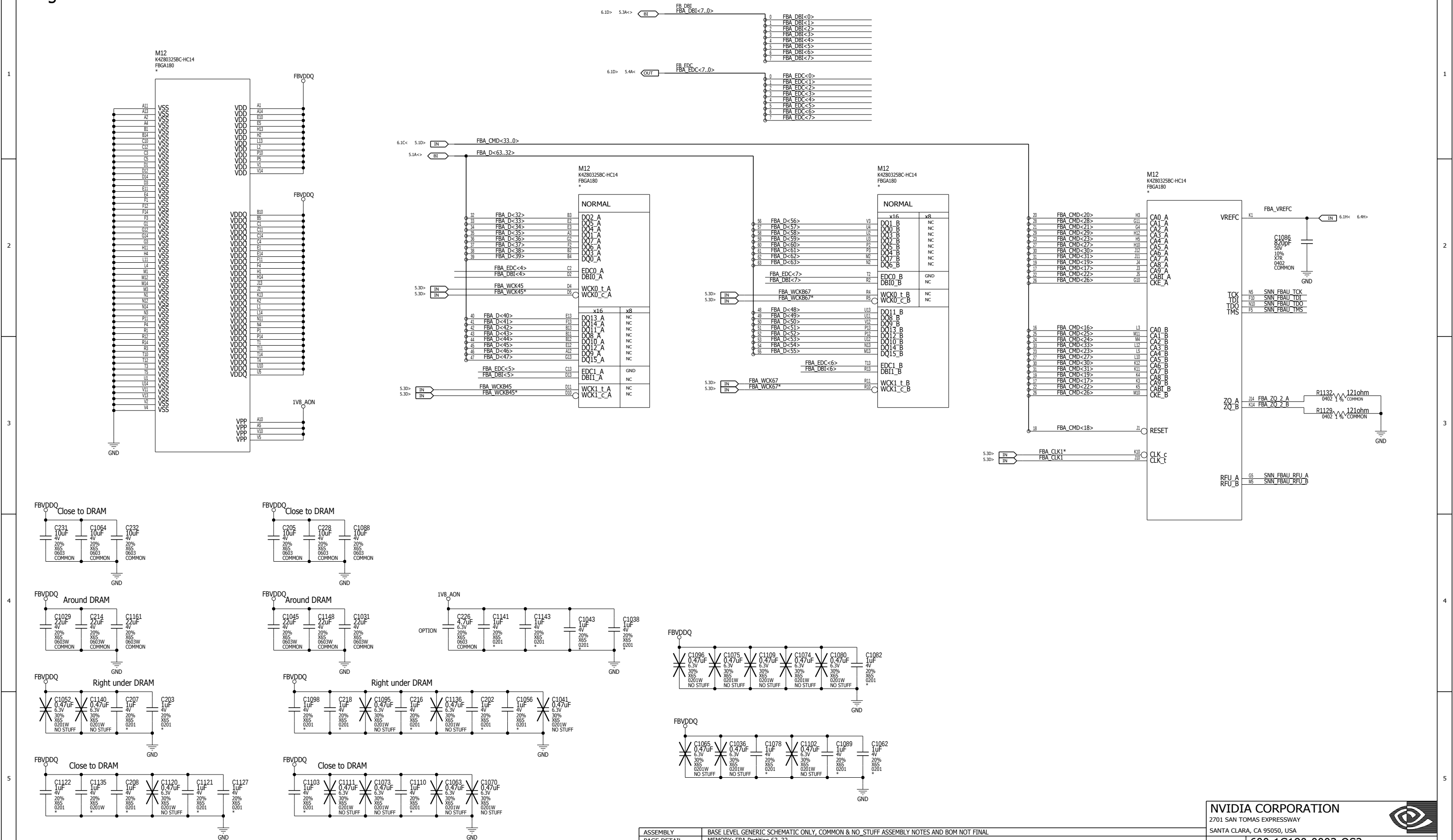


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Page5: MEMORY: GPU Partition A/B



Page7: MEMORY: FBA Partition 63..32

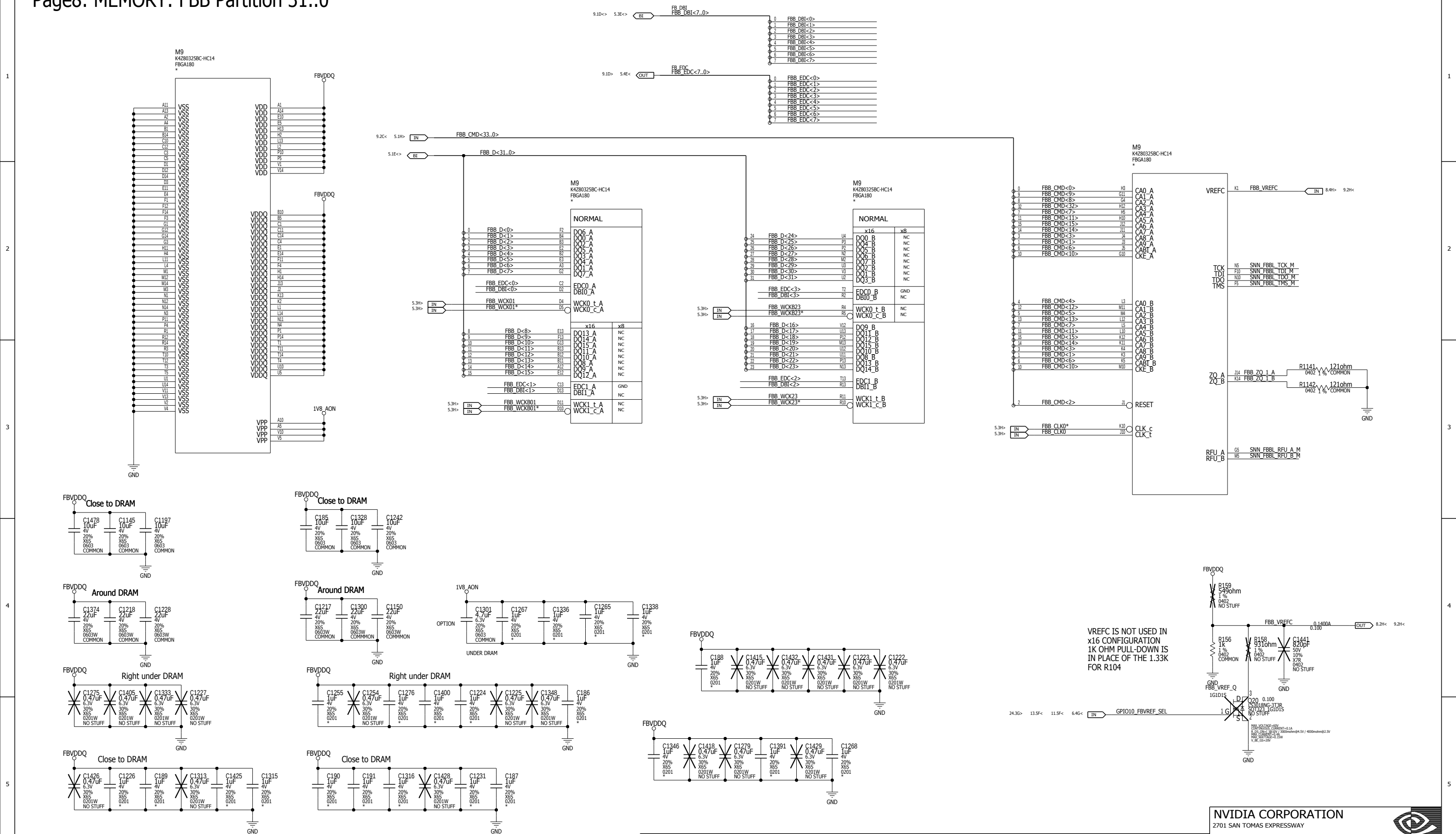


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PAGE DETAIL	MEMORY: FBA Partition 63..32

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Page8: MEMORY: FBB Partition 31..0

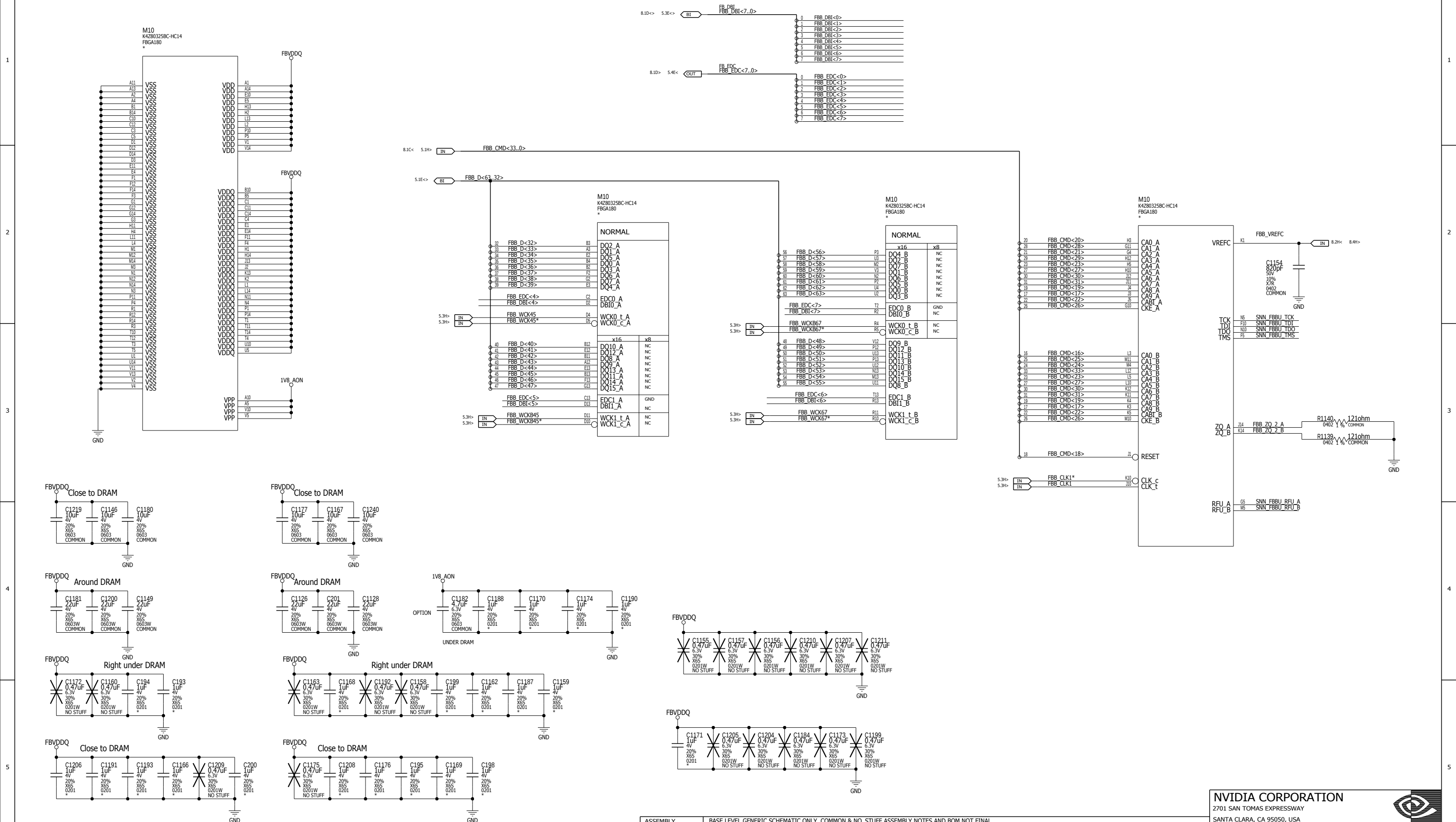


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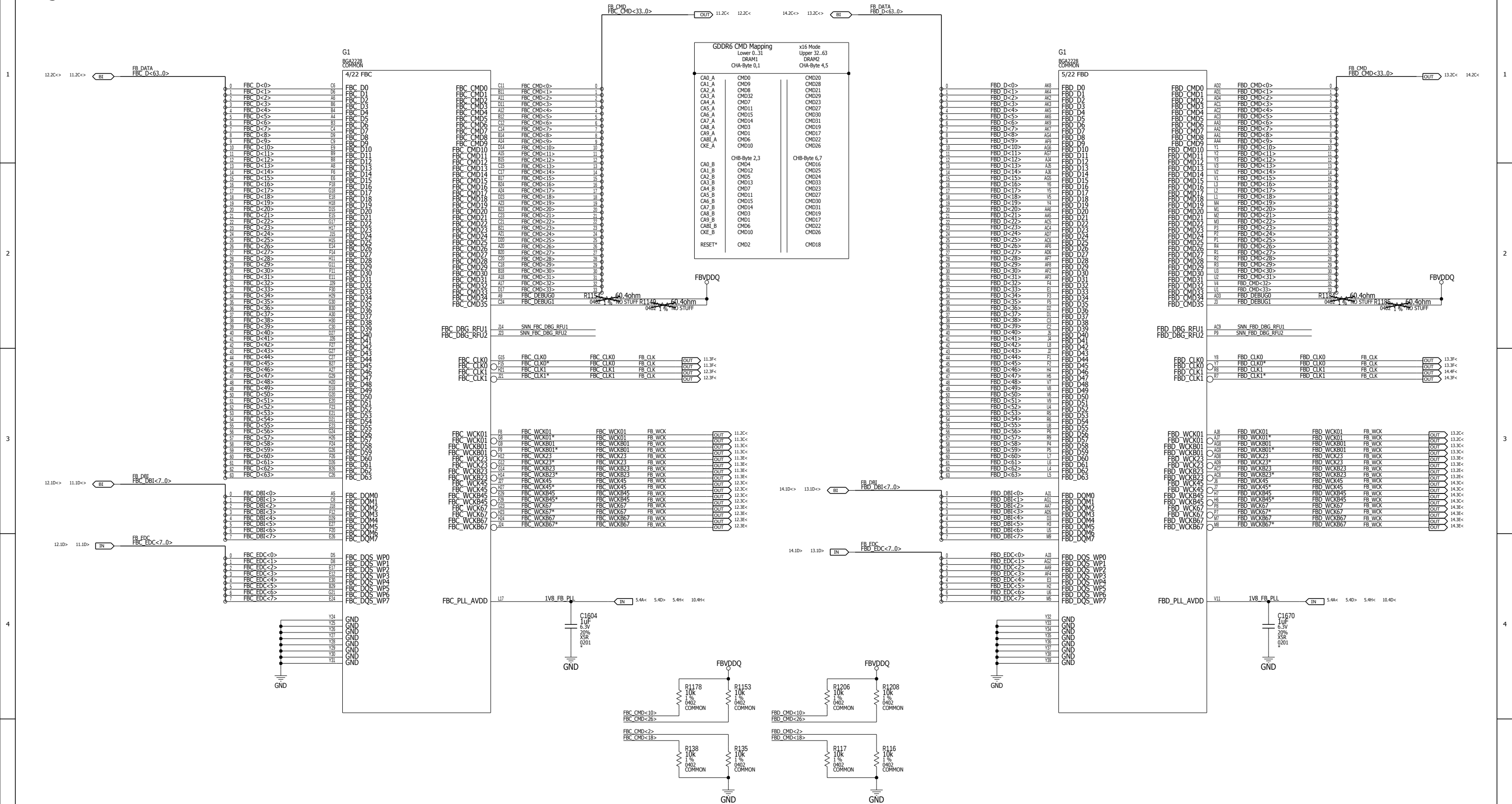
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PAGE DETAIL	MEMORY: FBB Partition 31..0

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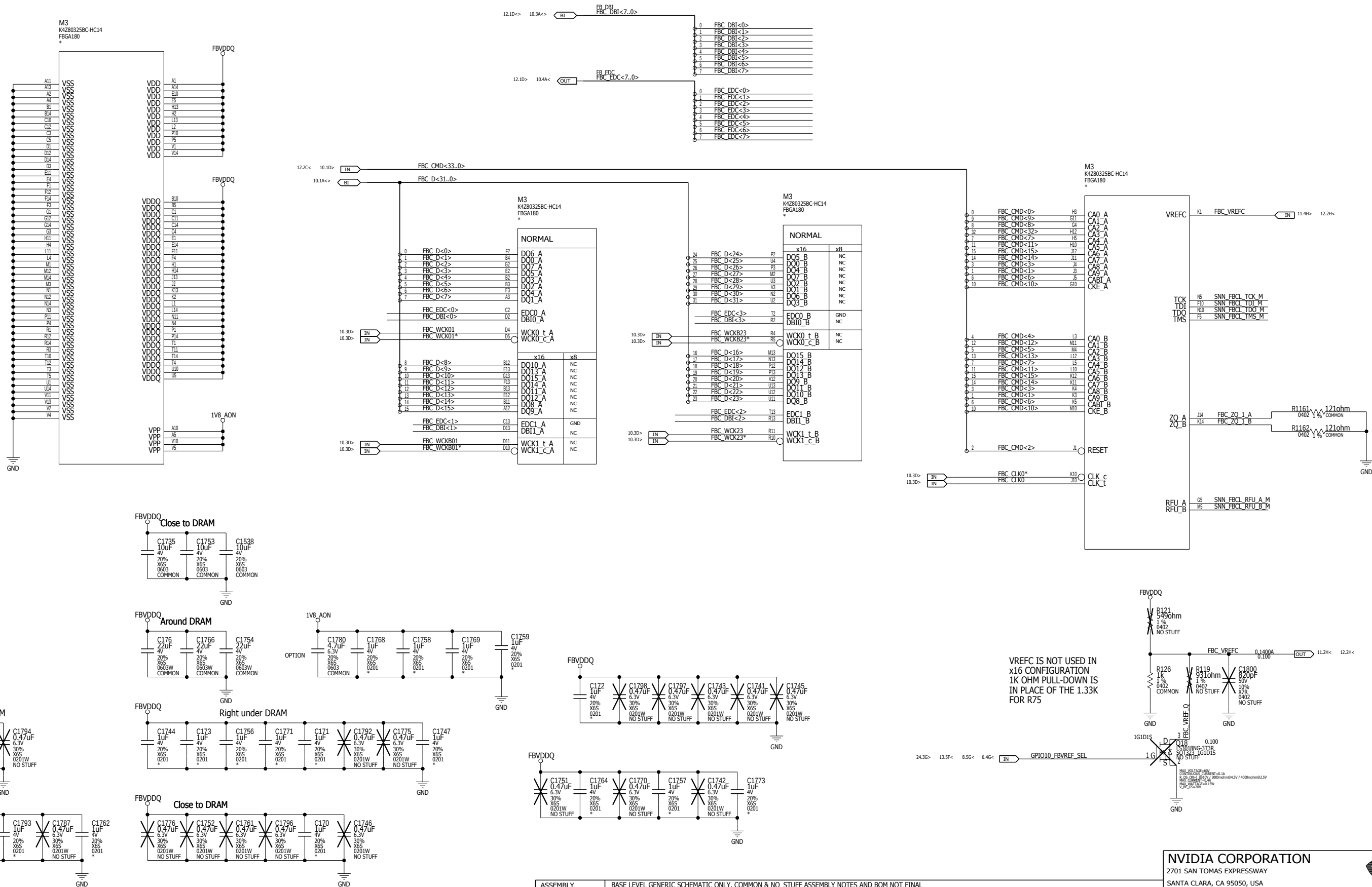
Page9: MEMORY: FBB Partition 63..32



Page10: MEMORY: GPU Partition C/D



Page11: MEMORY: FBC Partition 31..0



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PAGE DETAIL	MEMORY: FBC Partition 31..0

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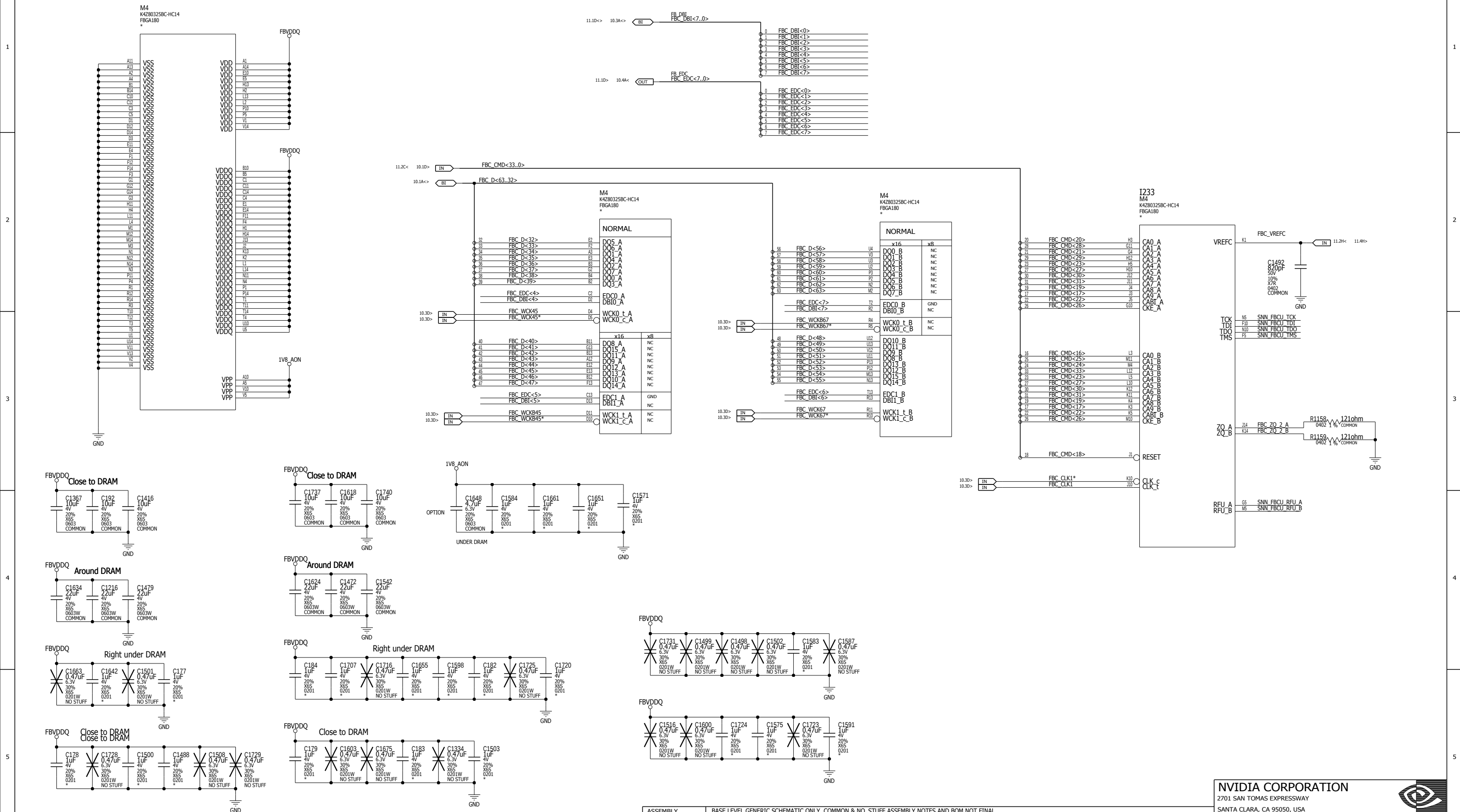
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Page12: MEMORY: FBC Partition 63..32

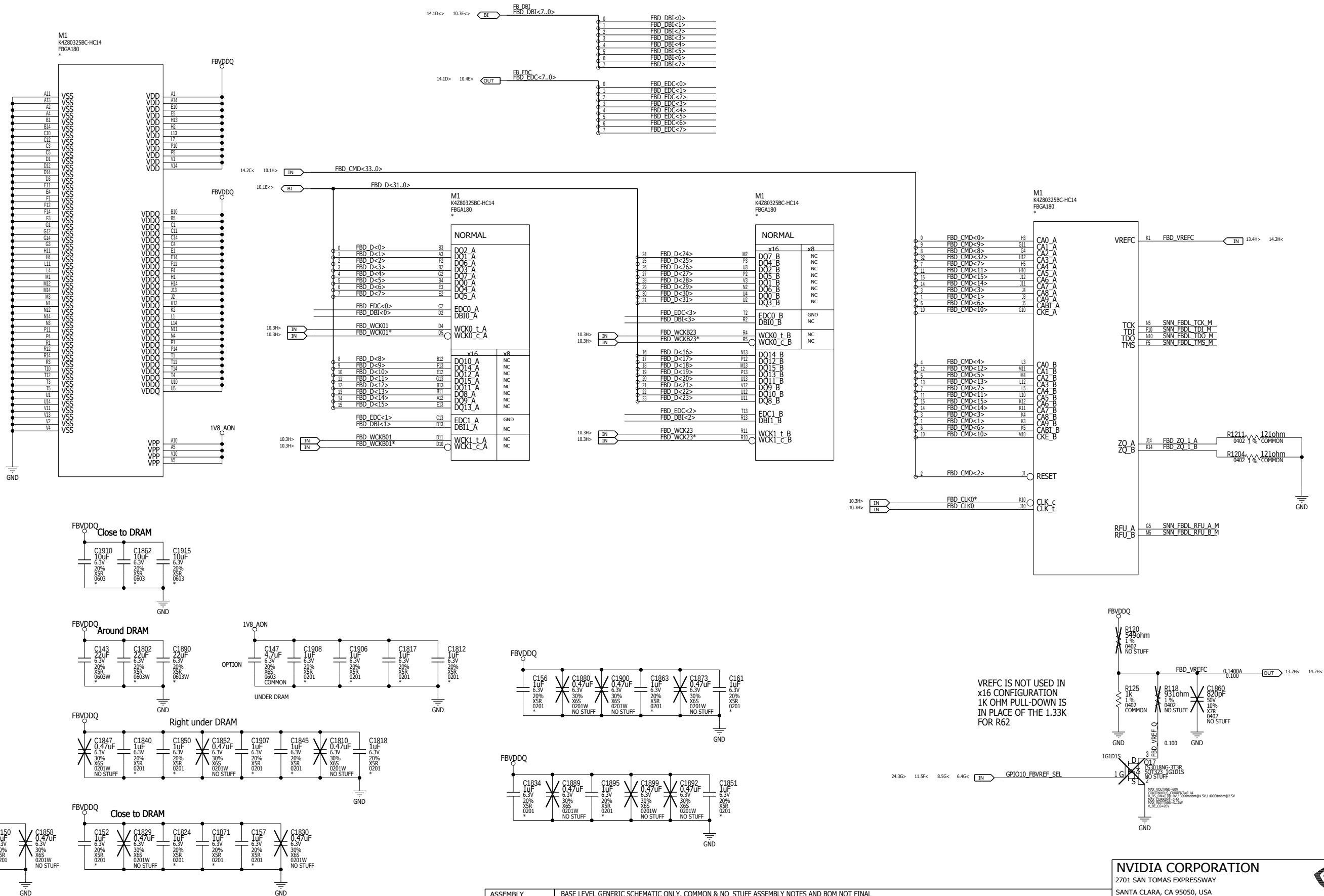


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PAGE DETAIL	MEMORY: FBC Partition 63..32

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Page13: MEMORY: FBD Partition 31..0



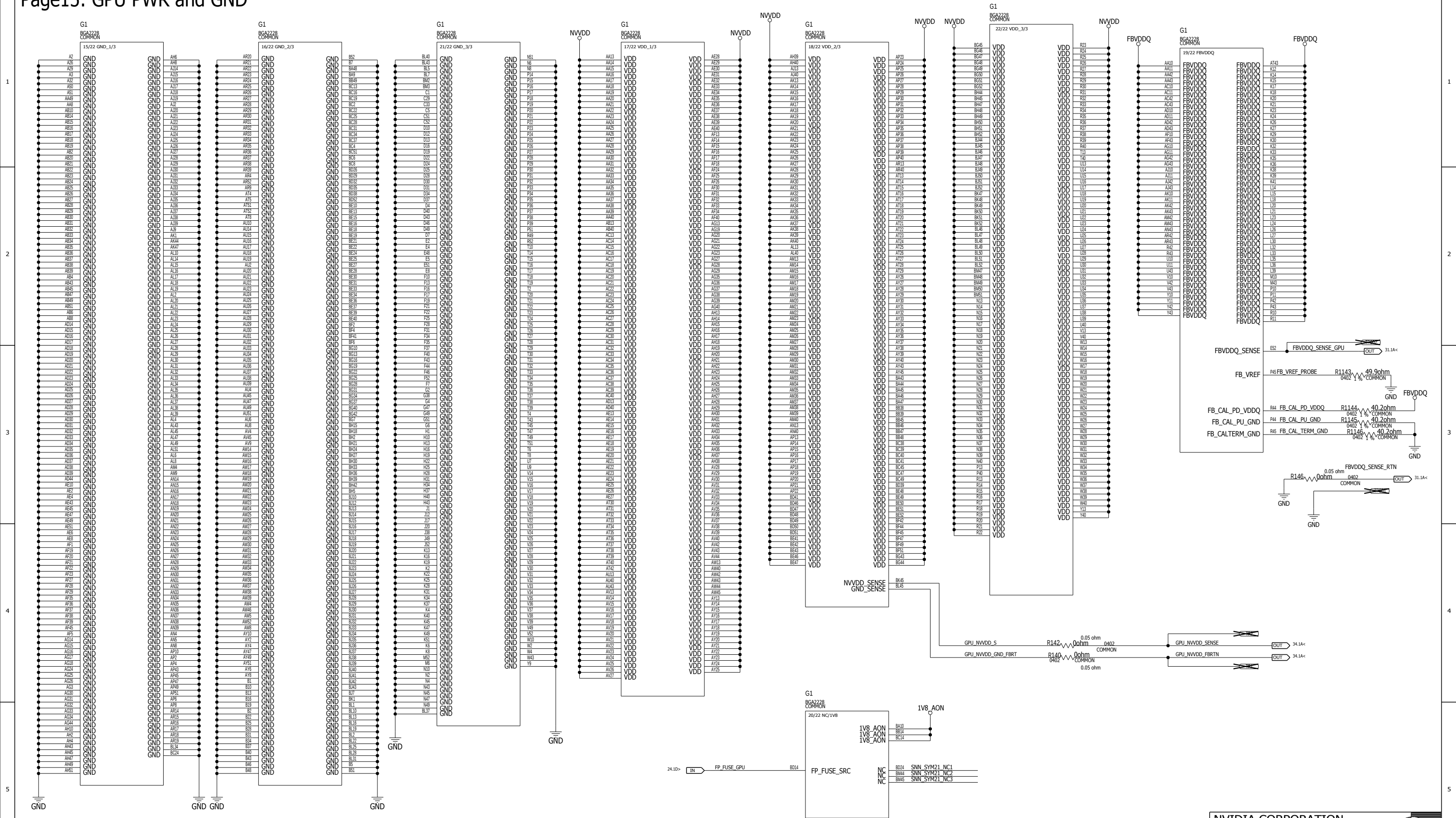
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PAGE DETAIL	MEMORY: FBD Partition 31..0

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Page15: GPU PWR and GND



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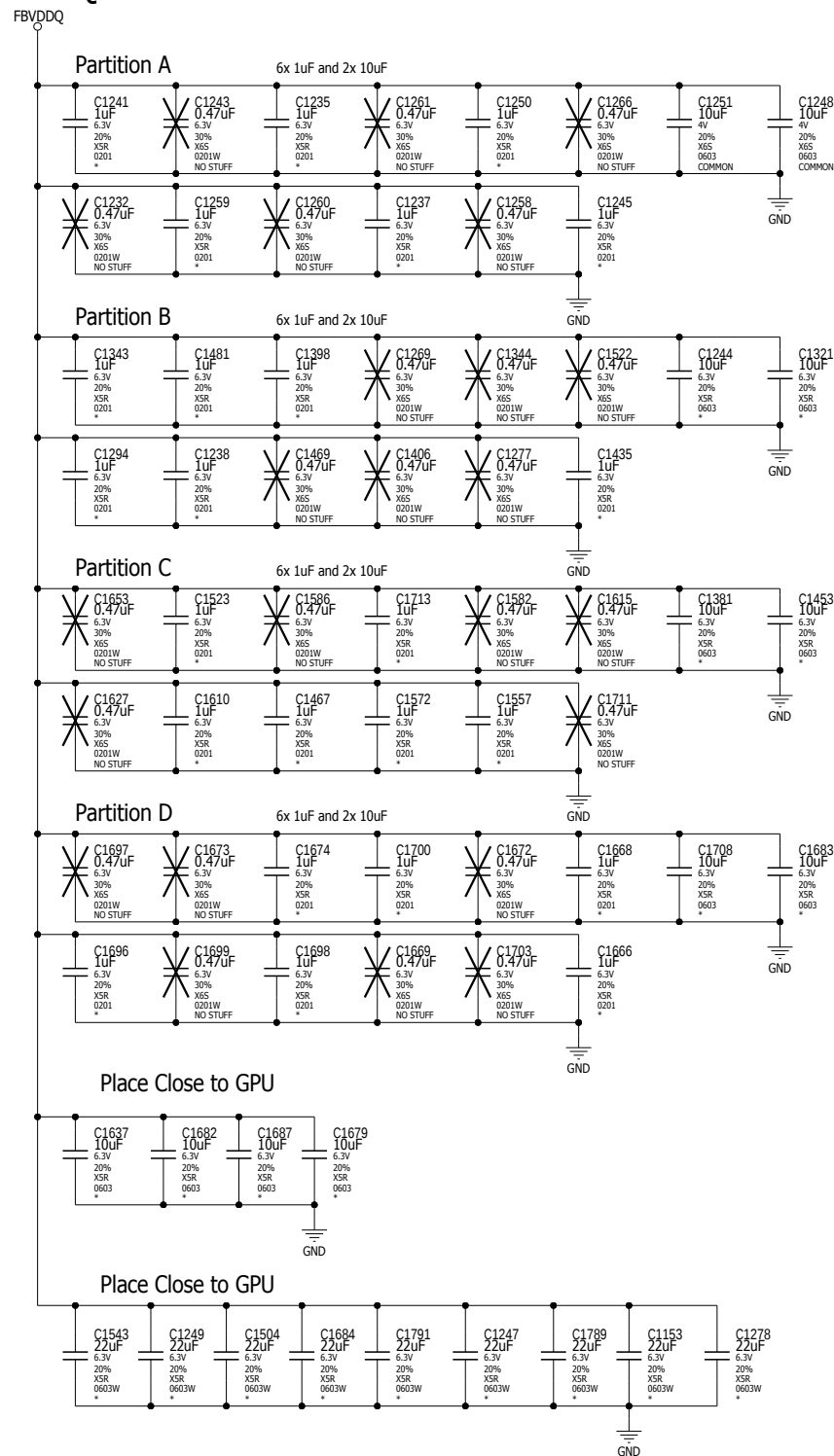
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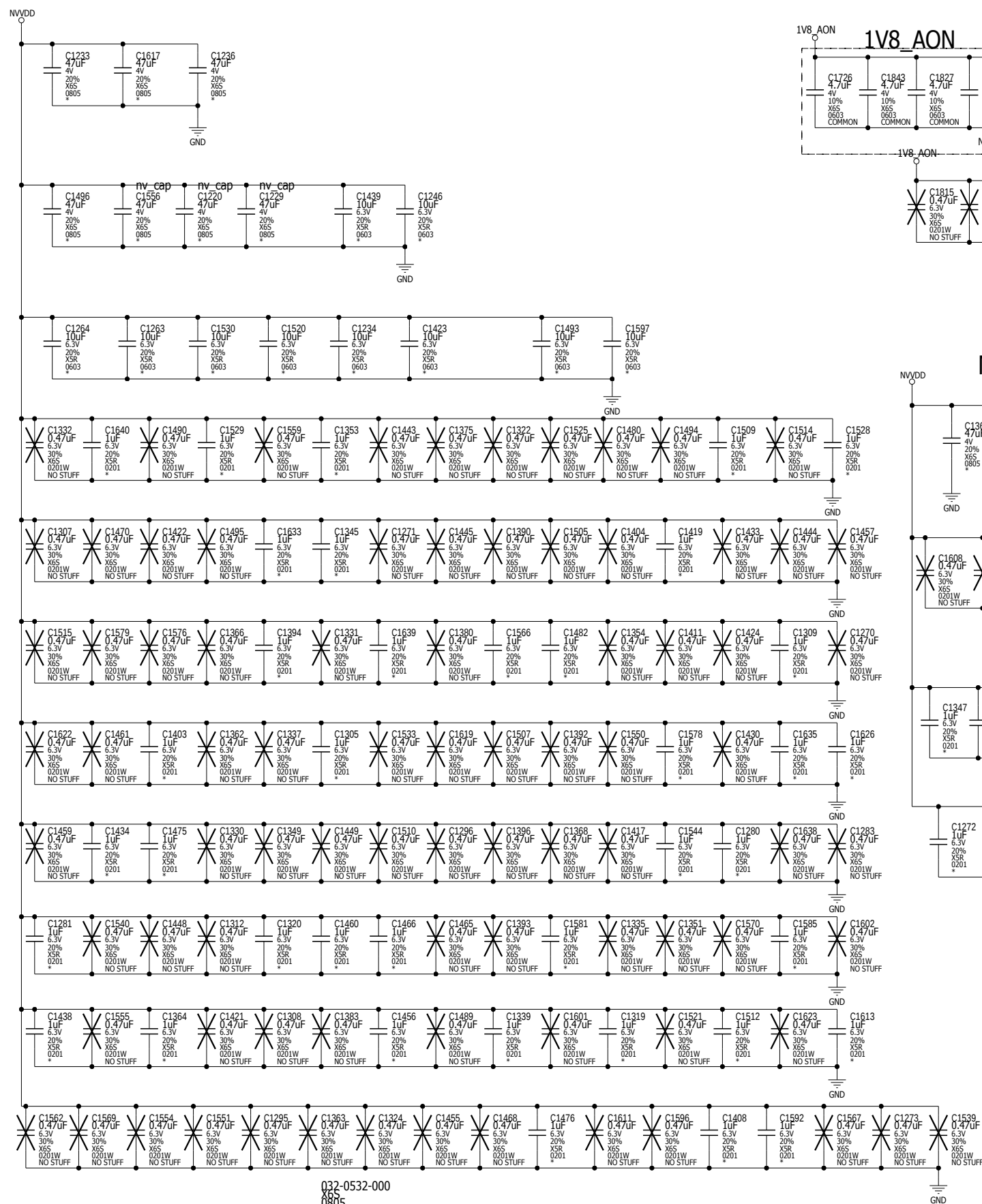
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PAGE DETAIL	GPU PWR and GND

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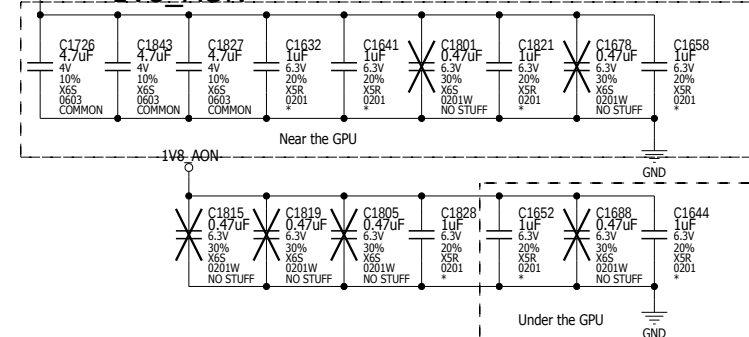
FBVDDQ



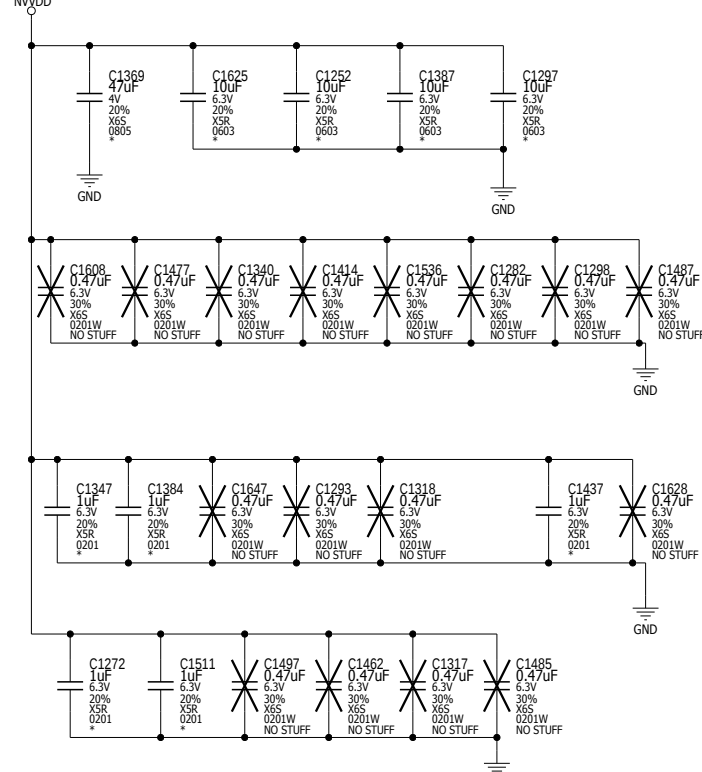
NVVDD



1V8 AON



NVVDD



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PAGE DETAIL	GPU Decoupling

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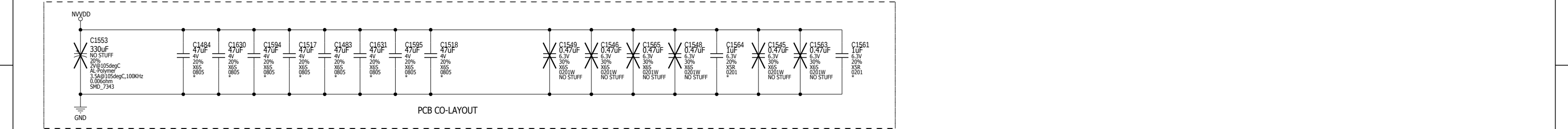
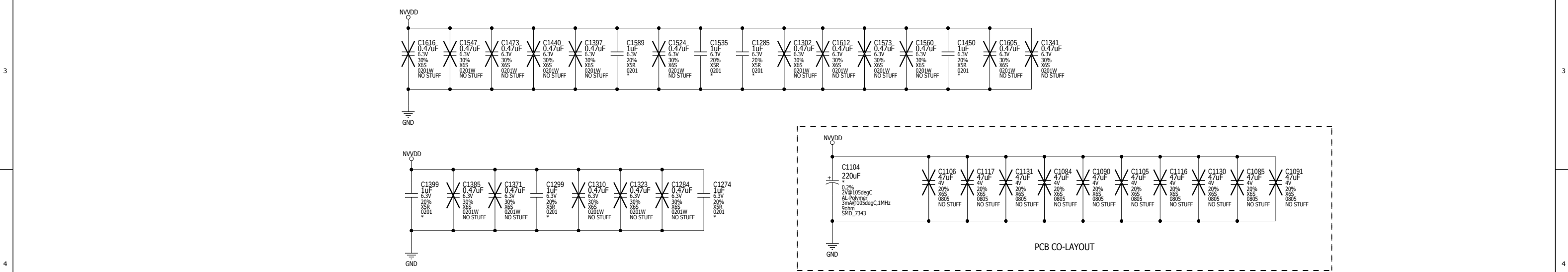
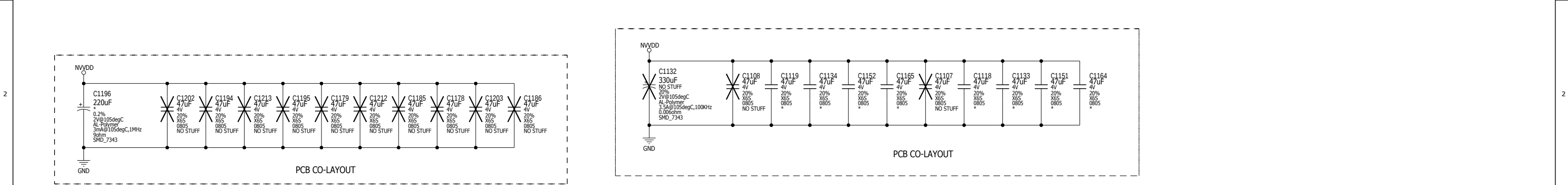
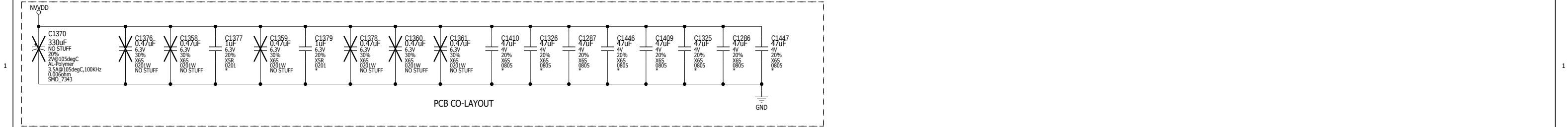
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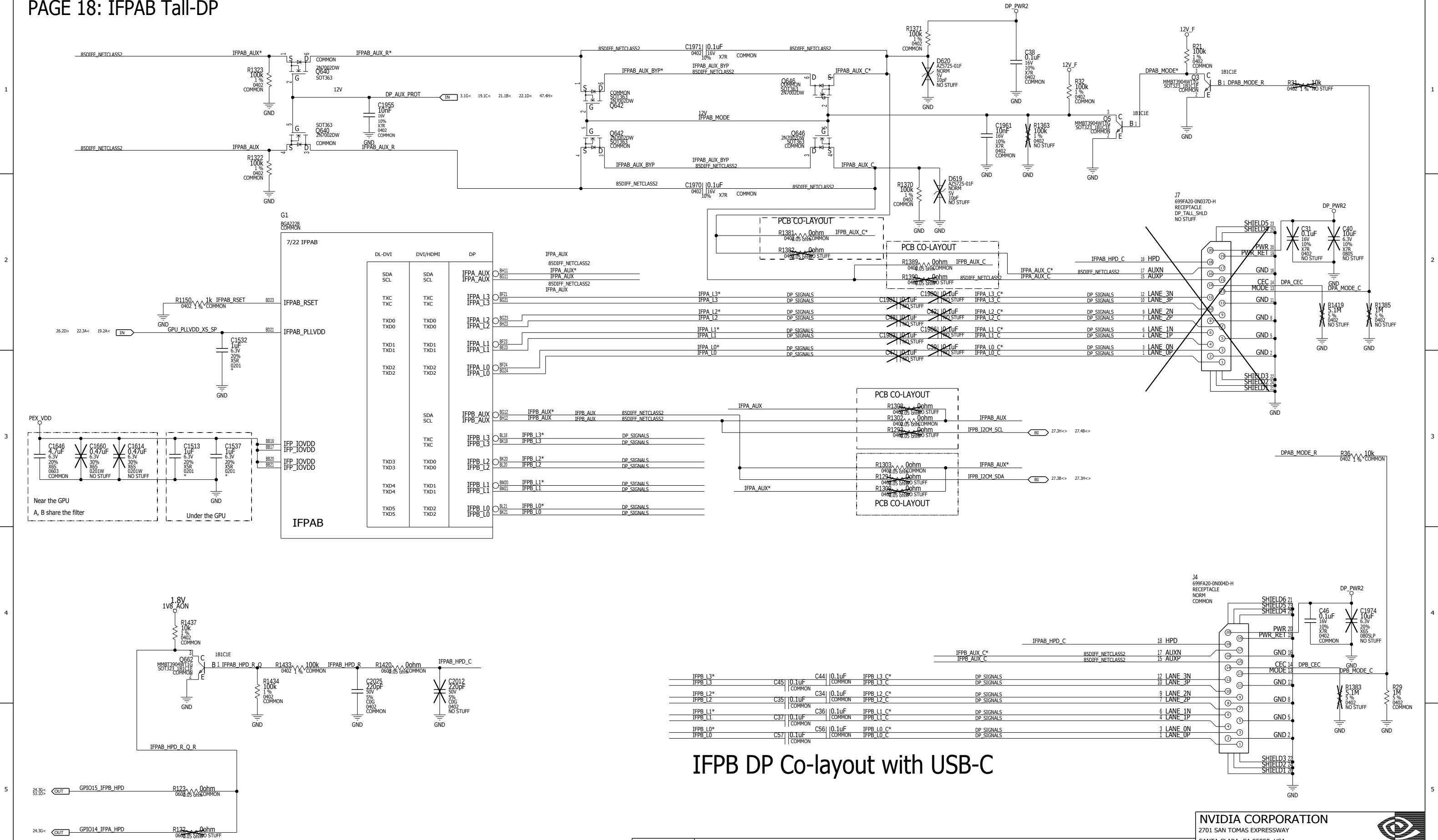
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Page17: GPU Decoupling



PAGE 18: IFPAB Tail-DP



IFPB DP Co-layout with USB-C

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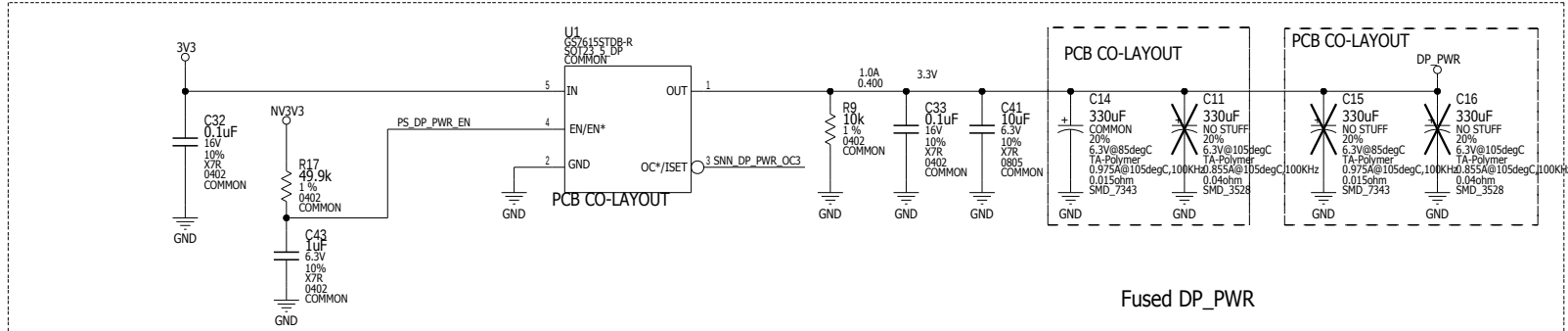
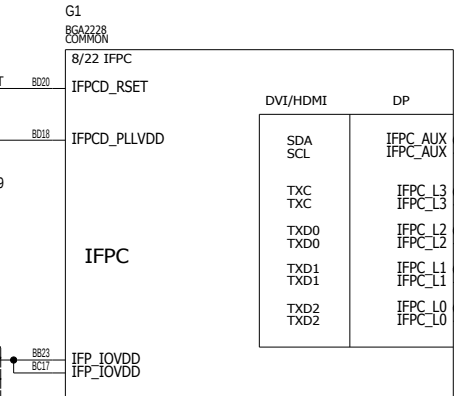
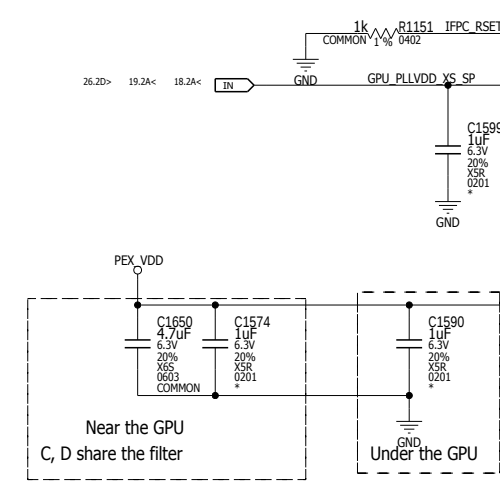
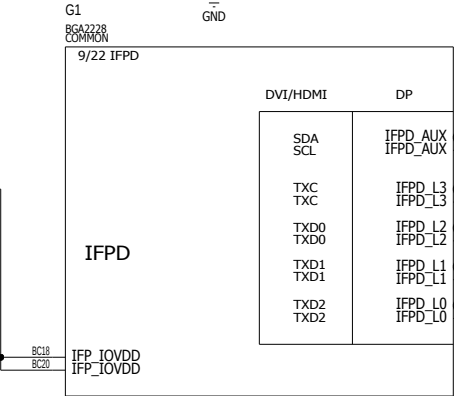
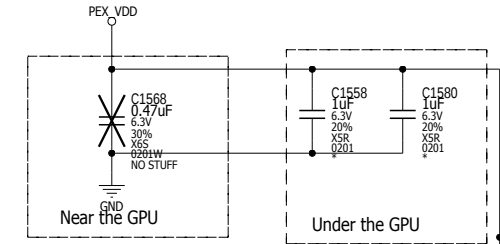
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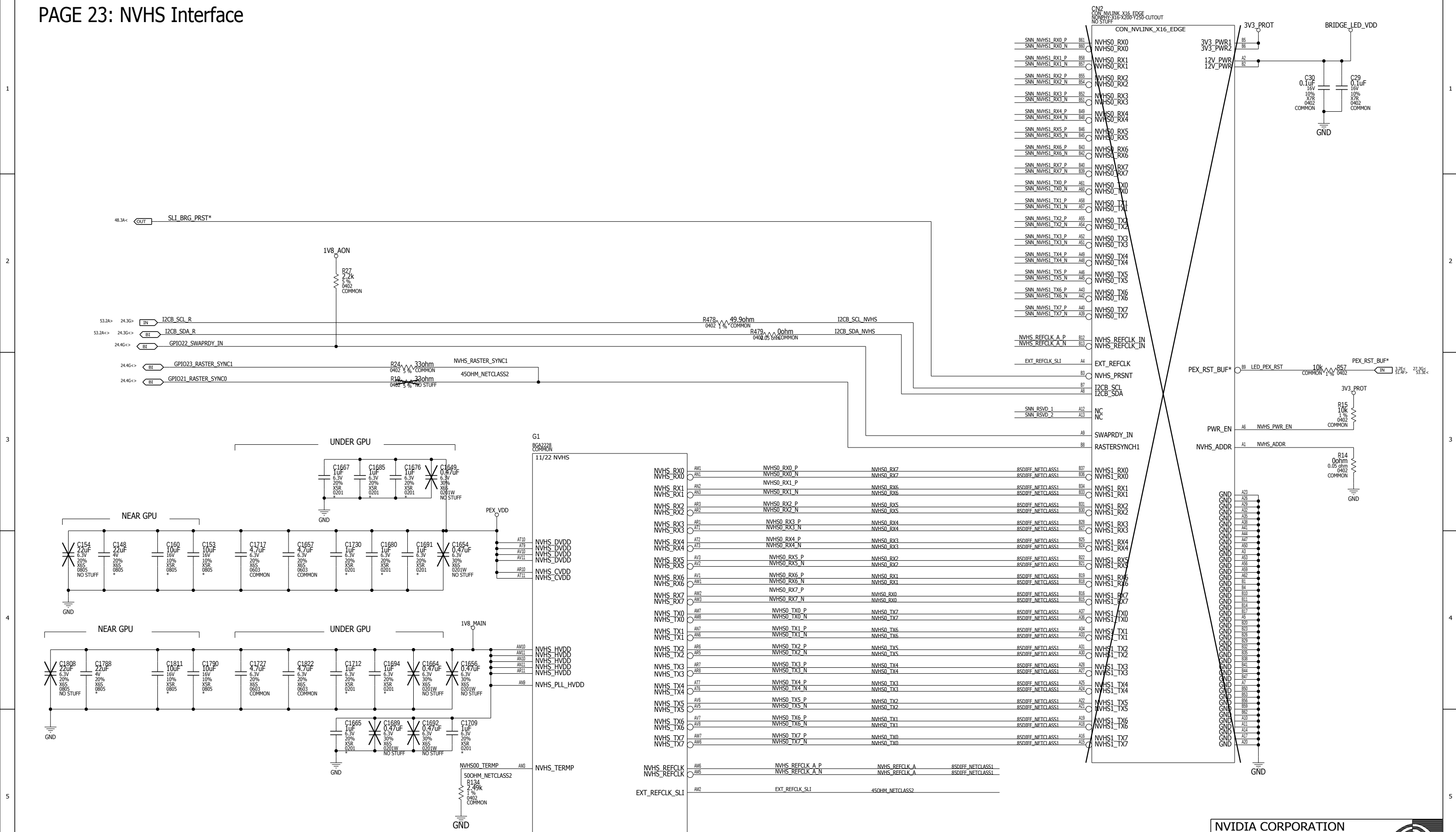


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PAGE DETAIL	IFPD DP

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PAGE 23: NVHS Interface



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PAGE DETAIL	NVHS INTERFACE

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PAGE 25: MISC: ROM, Straps

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

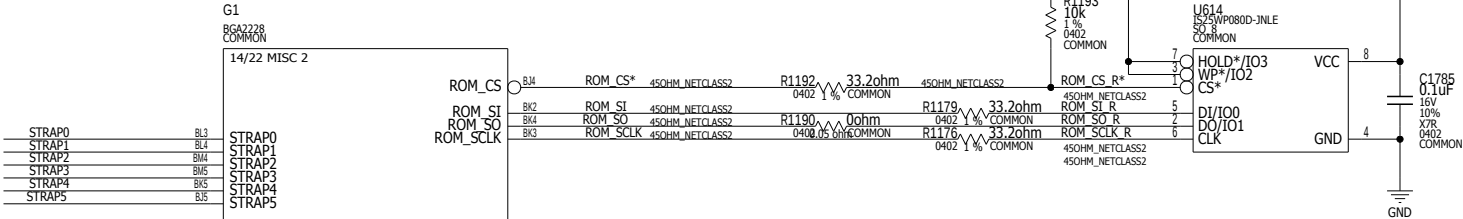
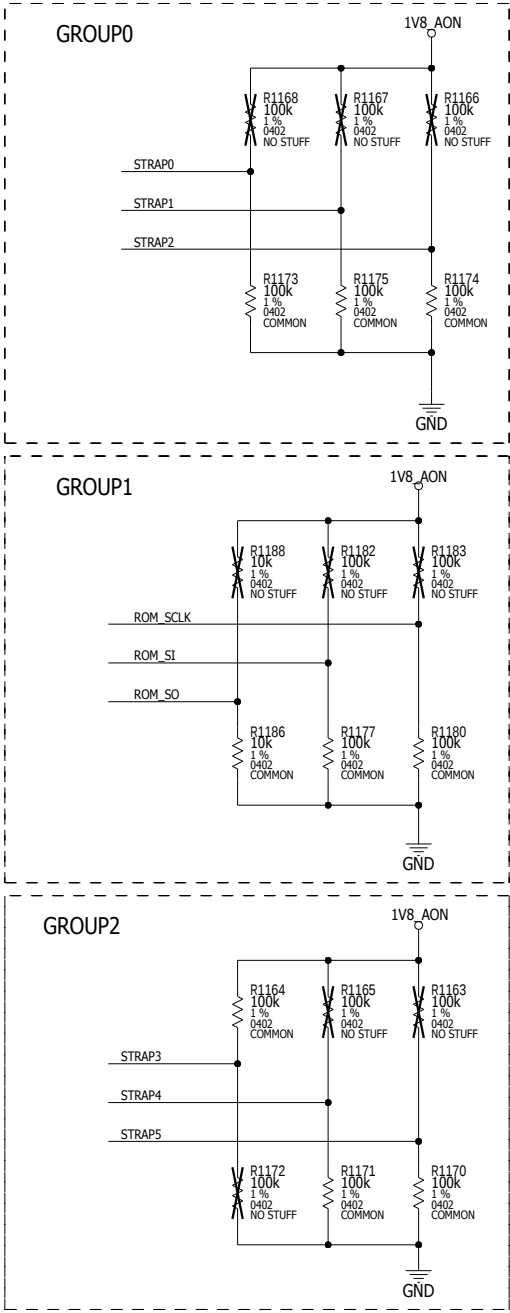
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

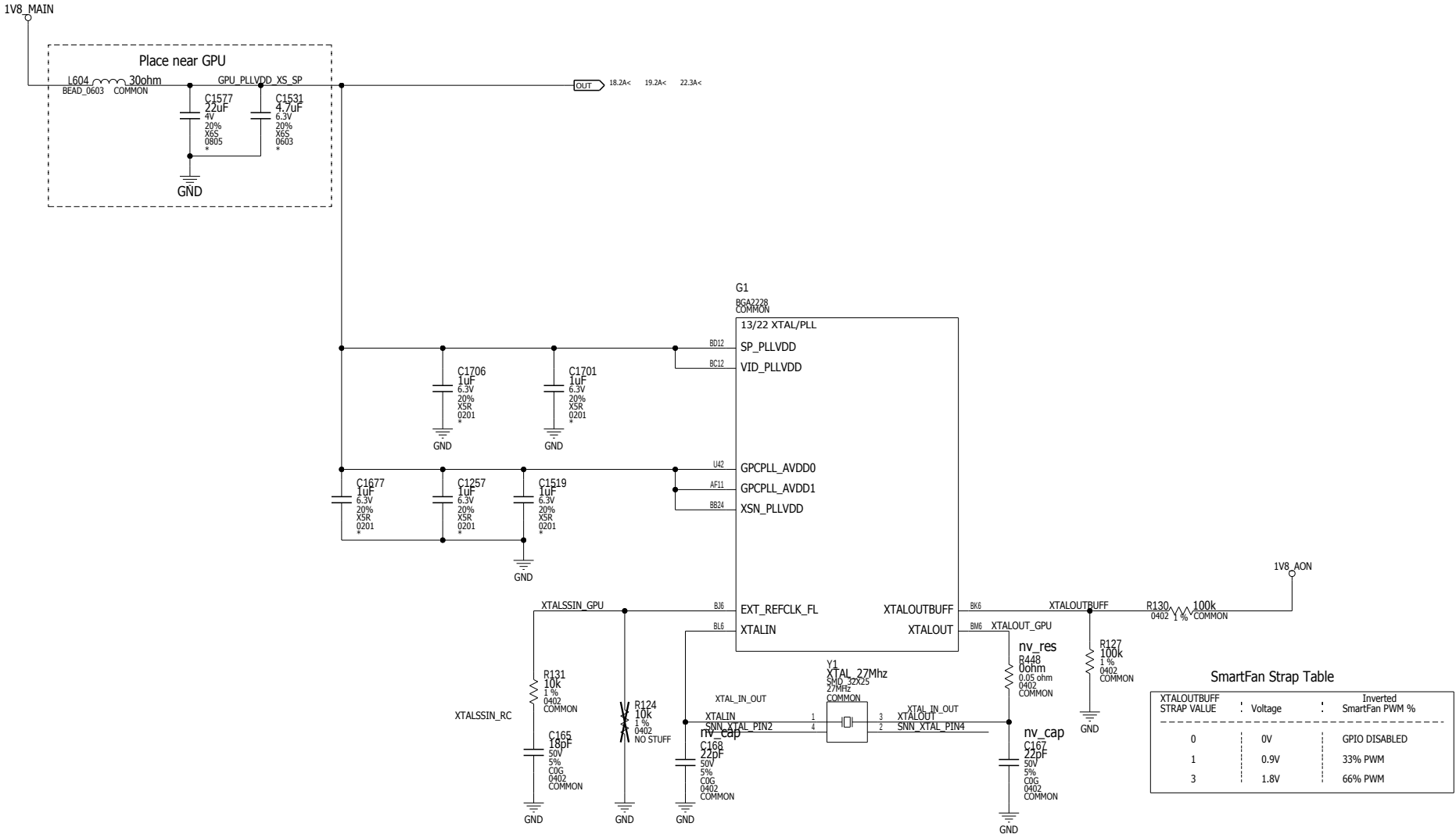
1:VGA_DEVICE ENABLE
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Default

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung

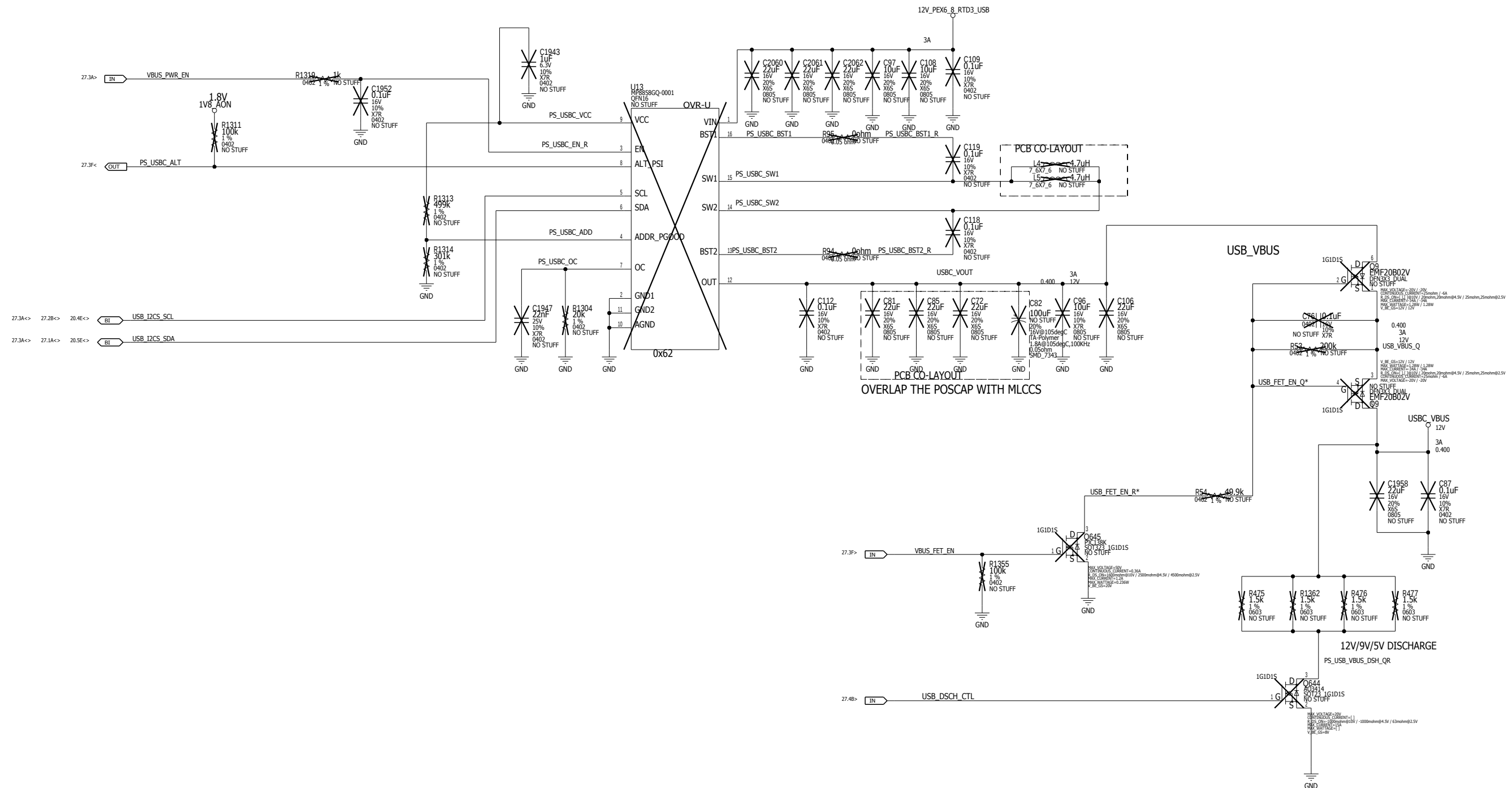


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PAGE 28: PS: USB VR



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PAGE DETAIL	PS: USB VR

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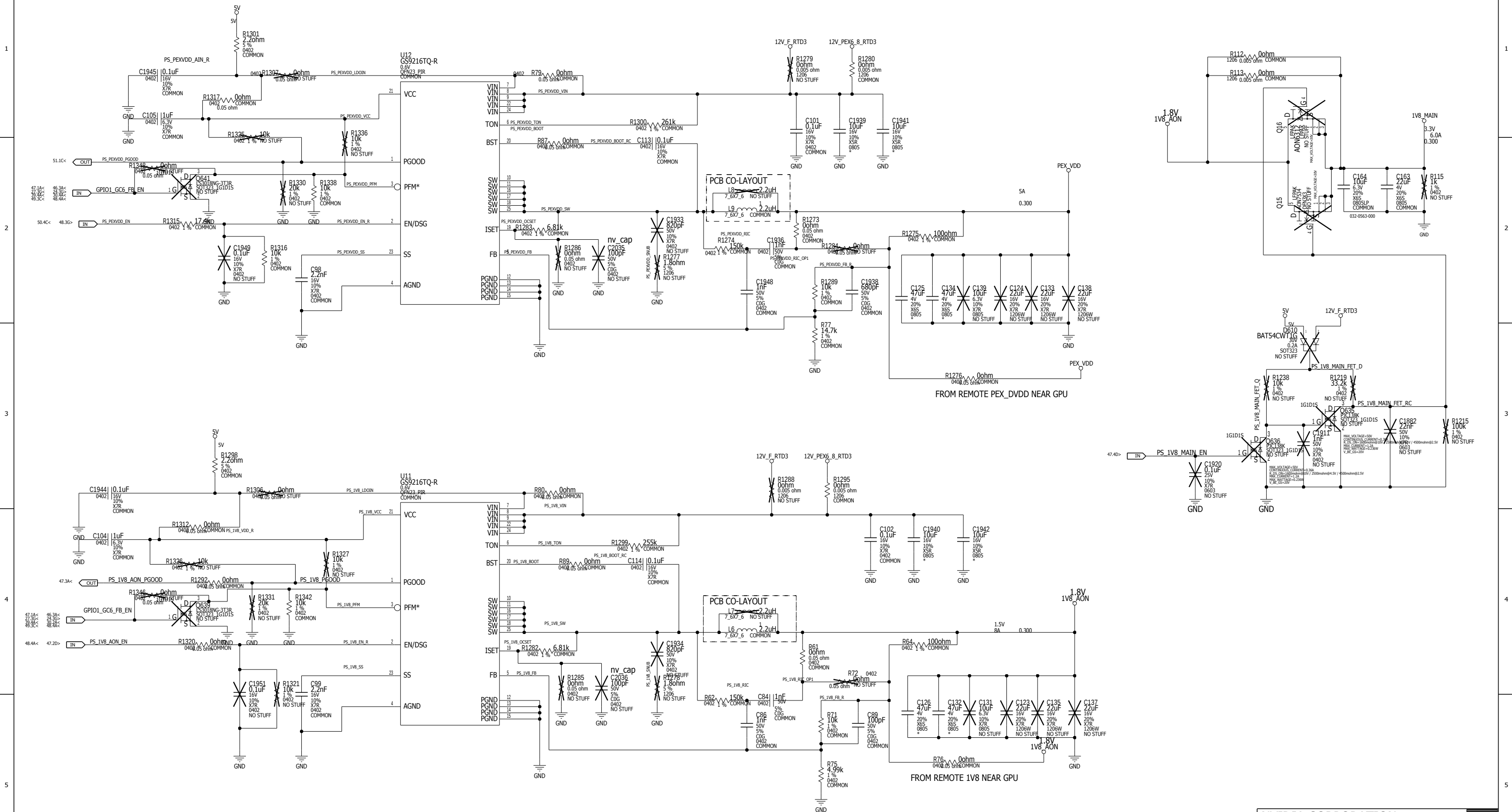
SANTA CLARA, CA 95050, USA

SANTA CLARA, CA 95050, USA	
600 16180 0003 063	

NV_PN	600-1G180-0003-QS2		
PCB REV	PG180-A03	PAGE	28 OF 54
BOM REV	A	DATE	06-FEB-2019



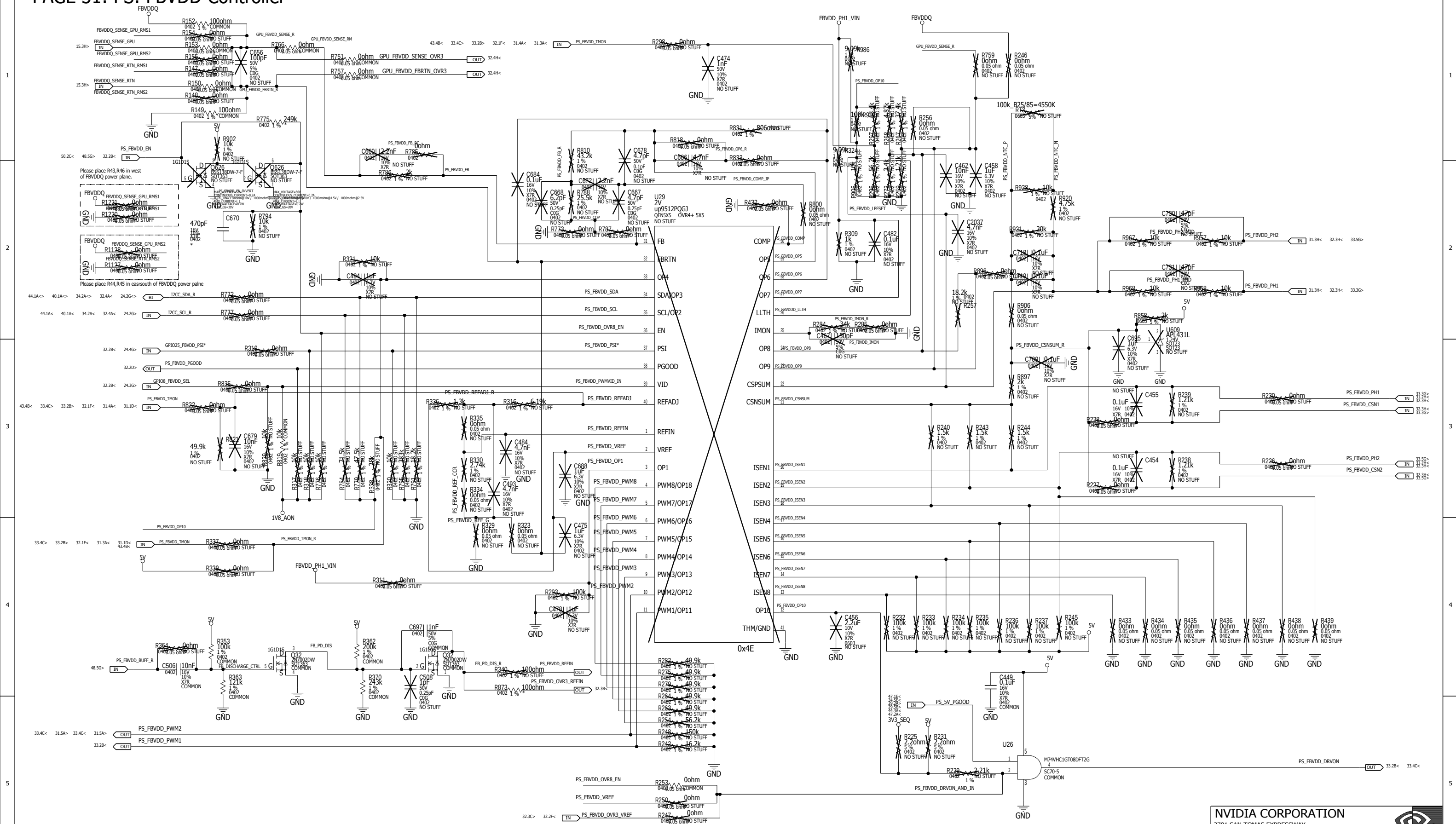
PAGE 30: PS: PEXVDD, 1V8



NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
NV_PN		600-1G180-0003-QS2		
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PAGE 31: PS: FBVDD Controller



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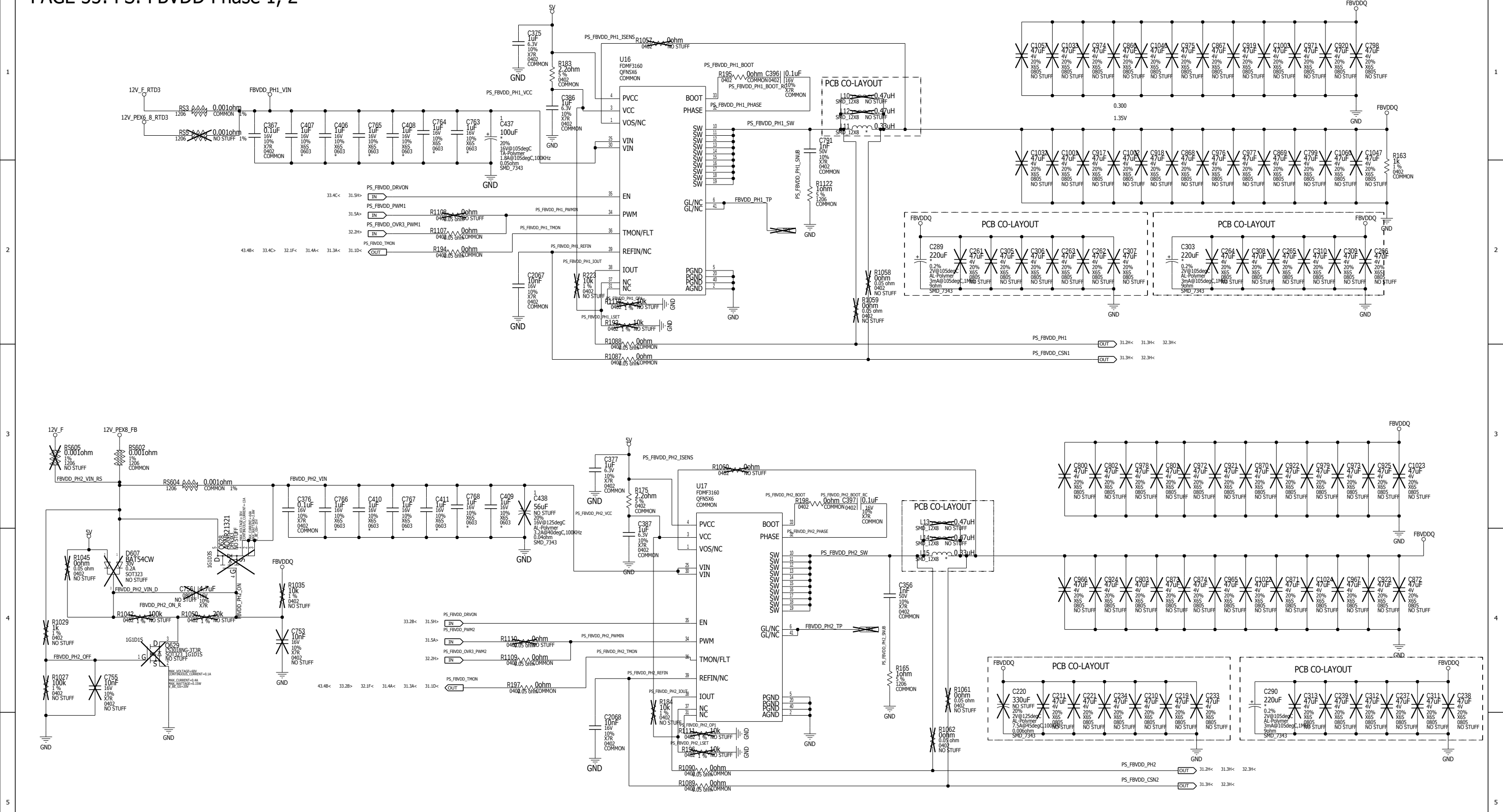


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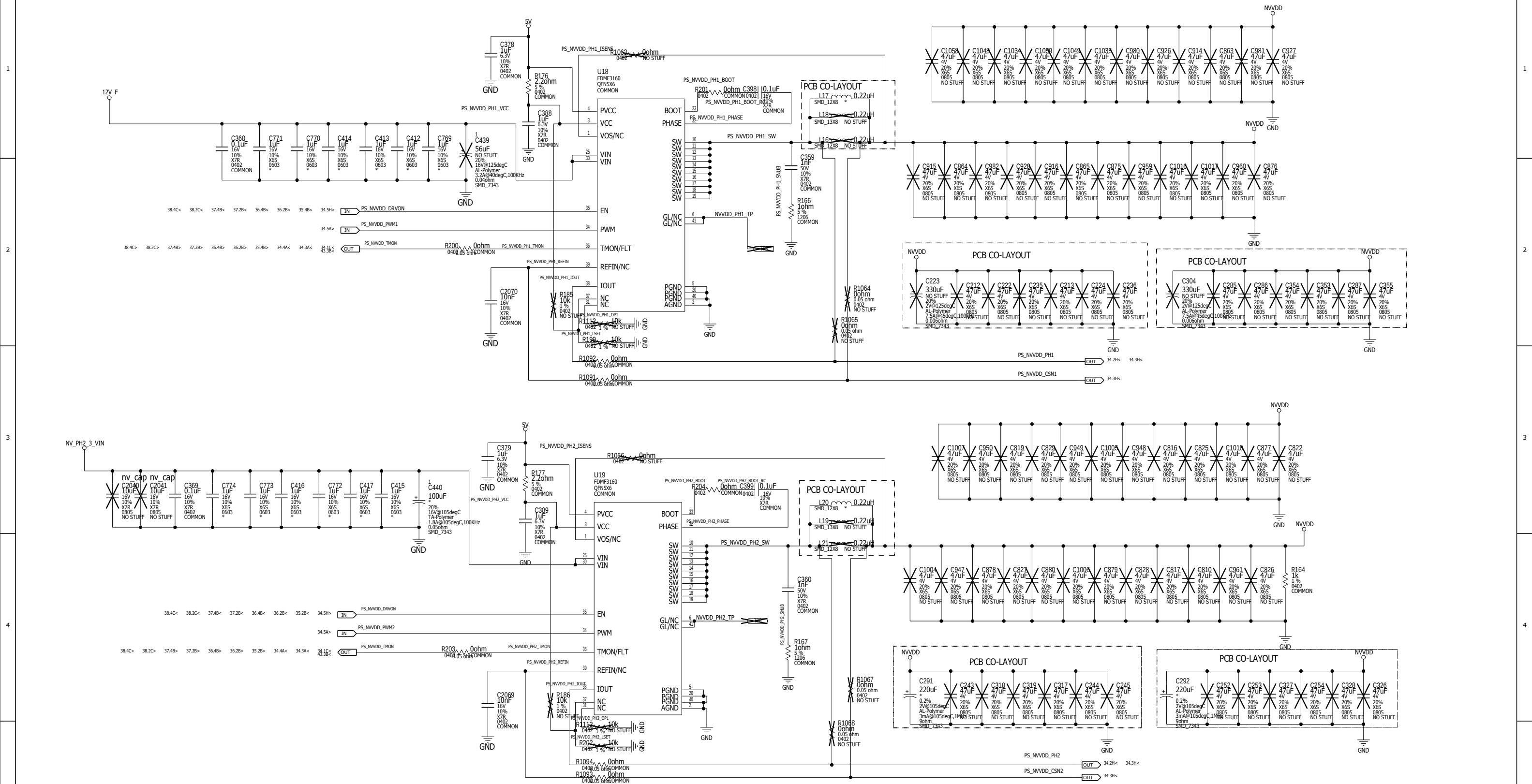
PAGE 33: PS: FBVDD Phase 1, 2



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: FBVDD PHASE 1, 2

PAGE 35: PS: NVVDD Phase 1, 2

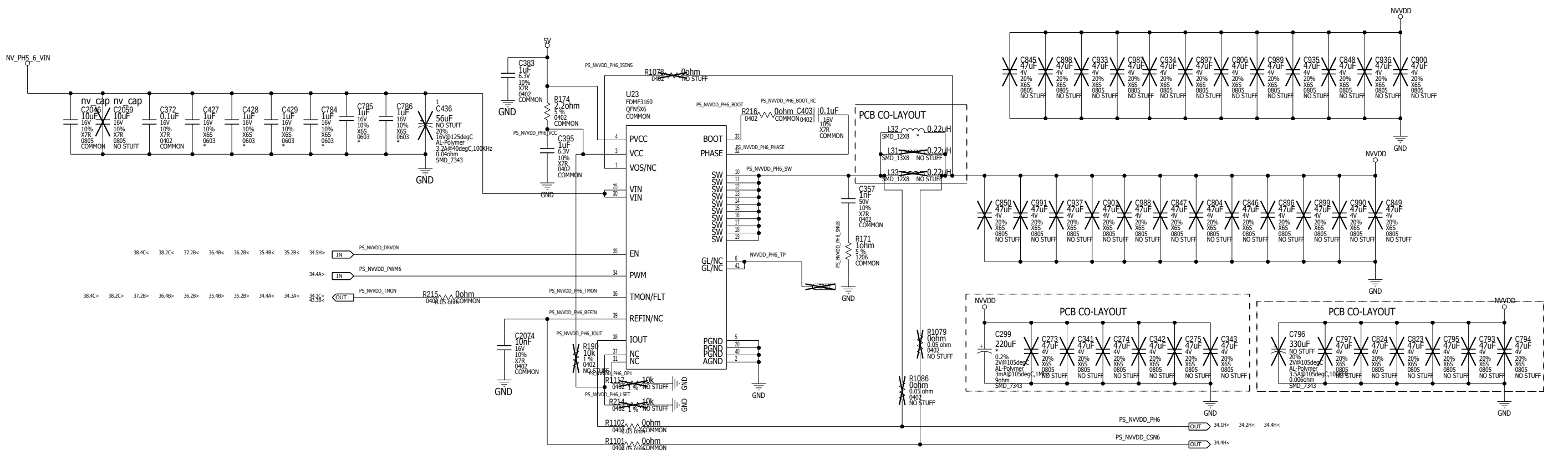
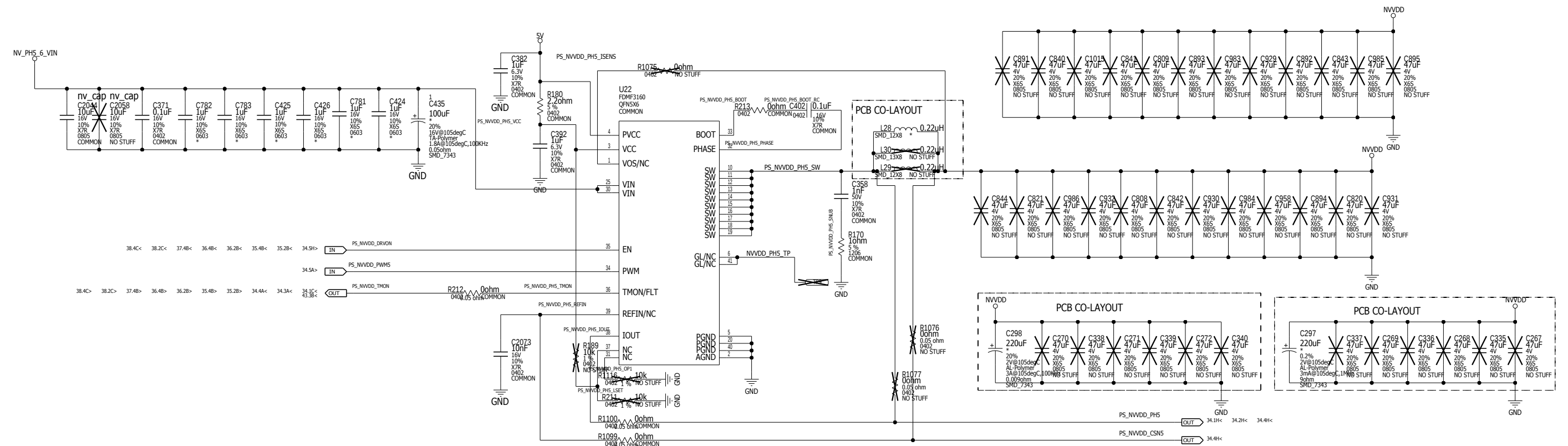


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD Phase 1, 2

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PAGE 37: PS: NVVDD Phase 5, 6



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PCB REV
BOM REV

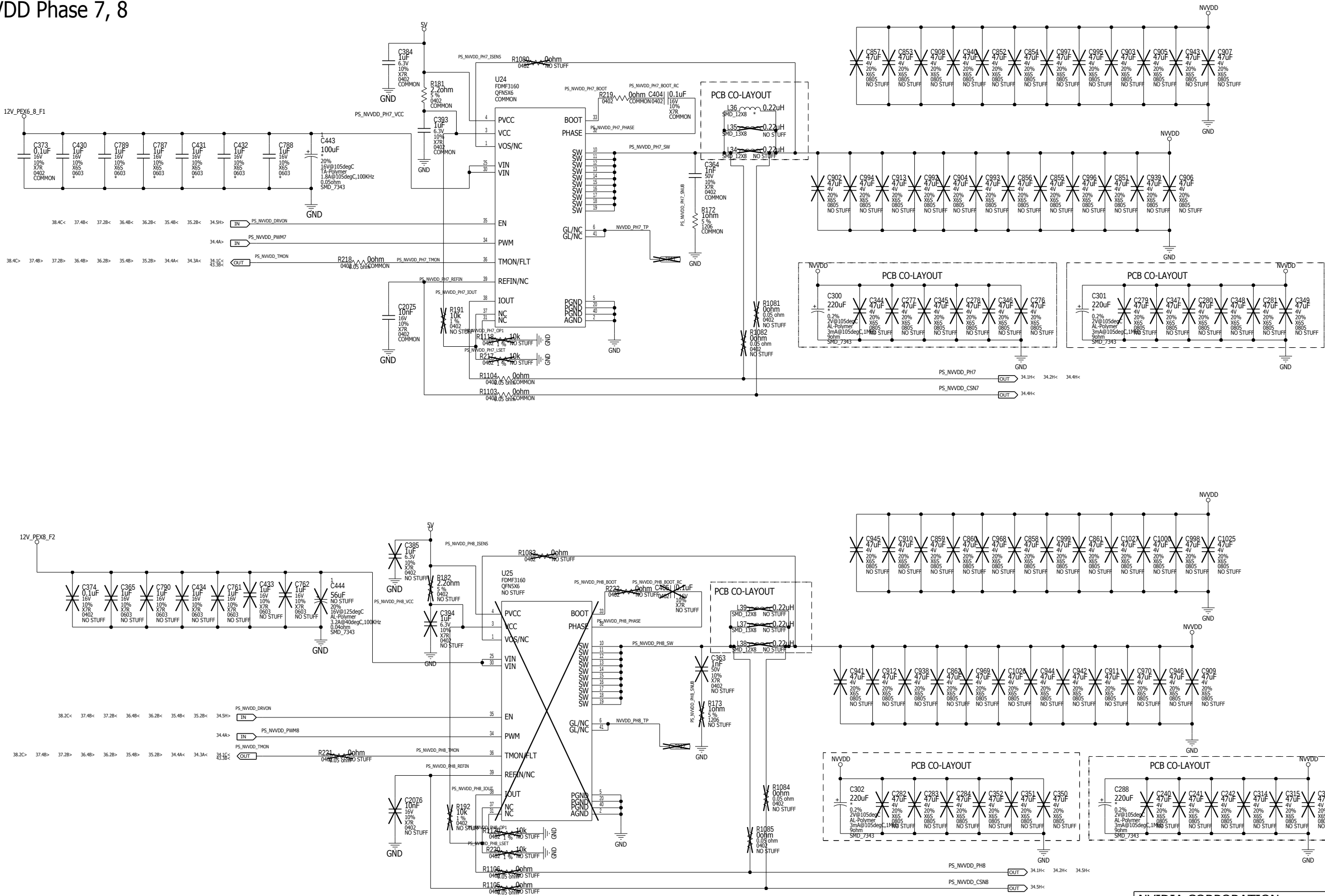
PG100 AUS
A

AGE	37 of 31
DATE	06-FEB-2019

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD Phase 5, 6

PAGE 38: PS:NVVDD Phase 7, 8

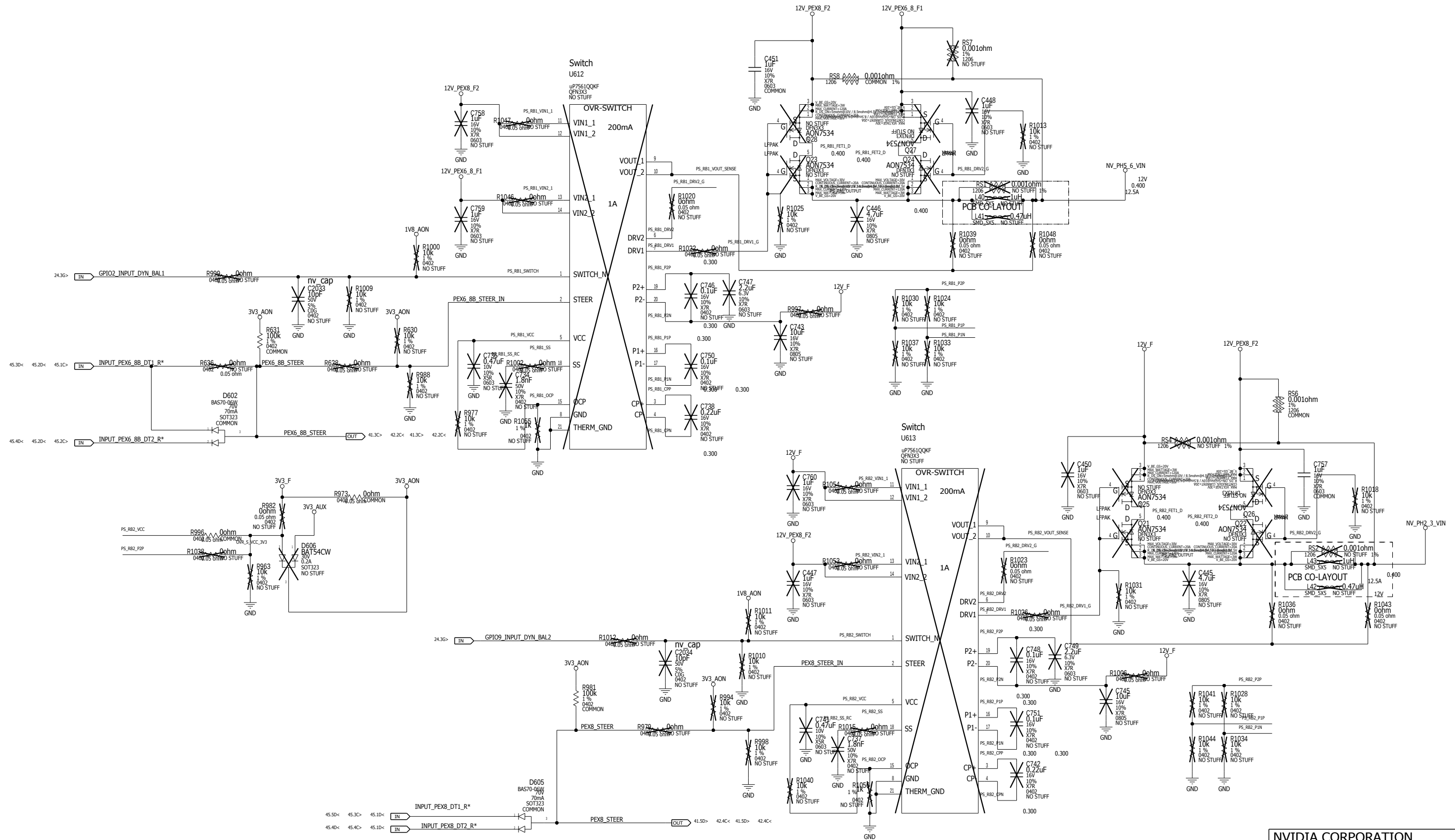


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: NVVDD Phase 7, 8

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NV_PN	600-1G180-0003-QS2		
PCB REV	PG180-A03	PAGE	38 OF 54
BOM REV	A	DATE	06-FEB-2019

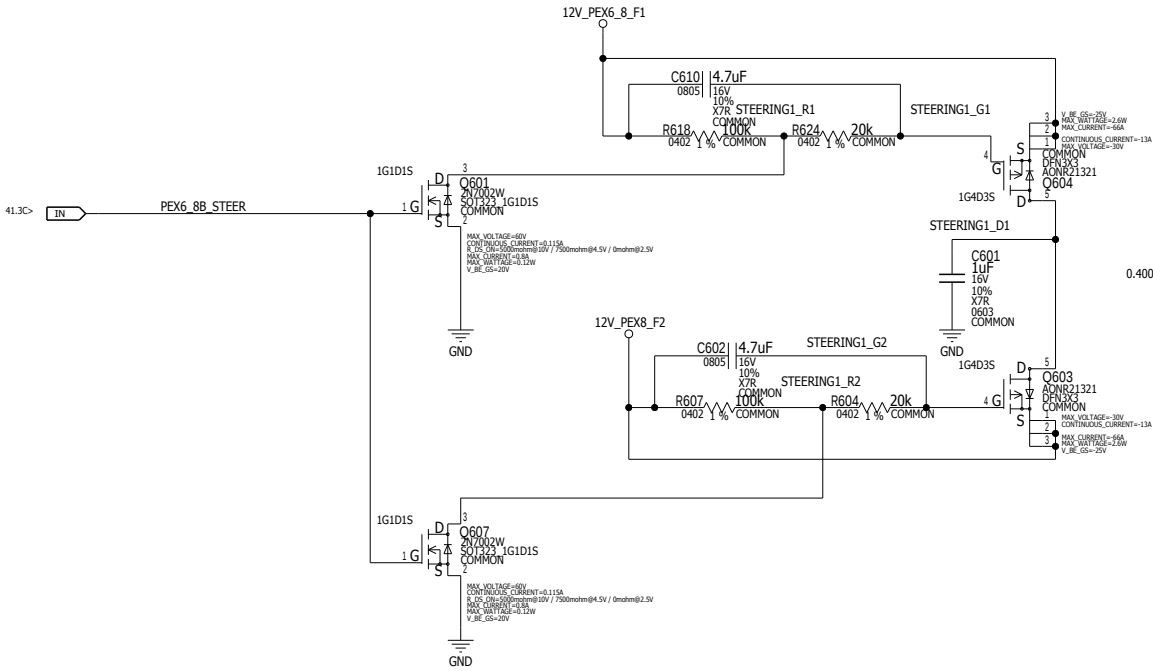
PAGE 41: PS: INPUT SWITCH Rail Balance



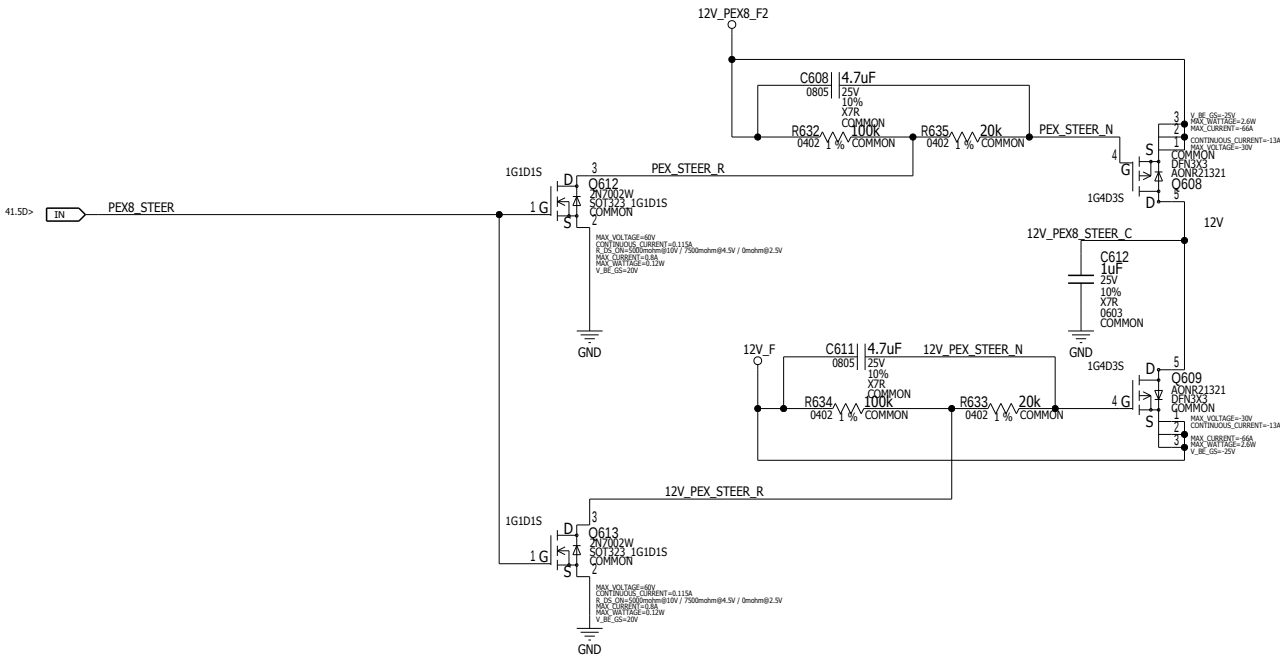
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA				
NV_PN		600-1G180-0003-QS2		
PCB REV	PG180-A03	PAGE	41 OF 54	
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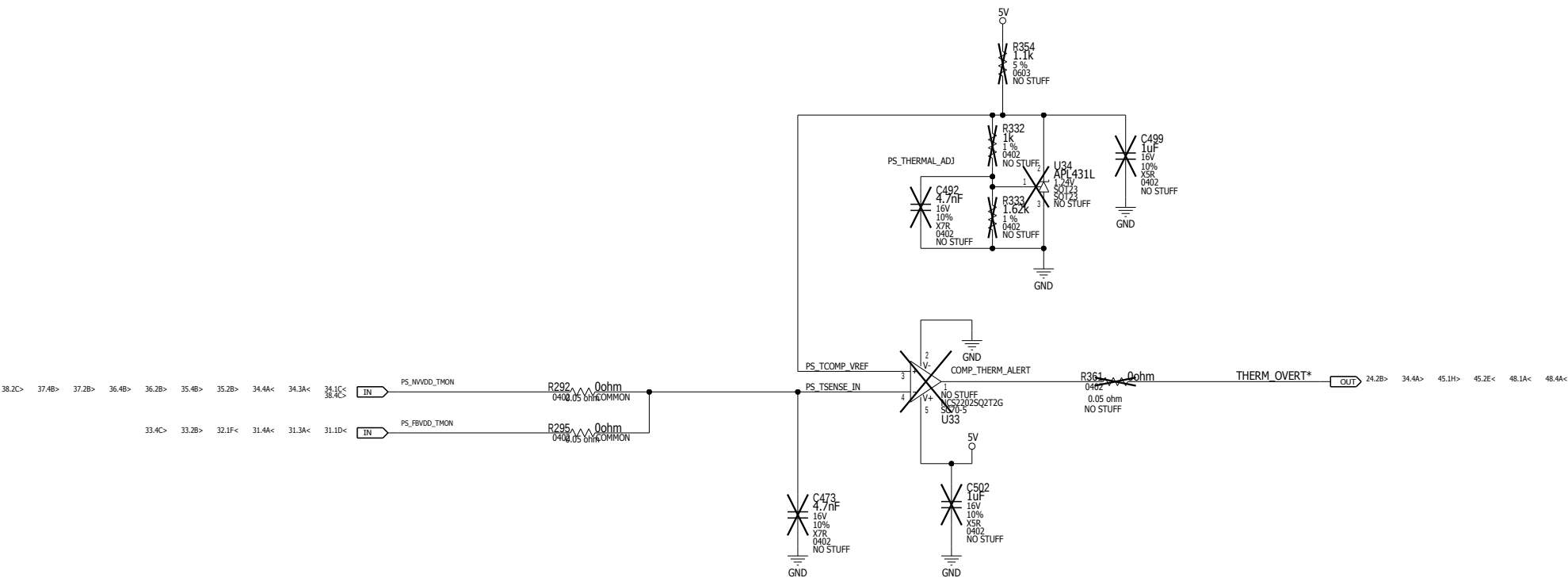
12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

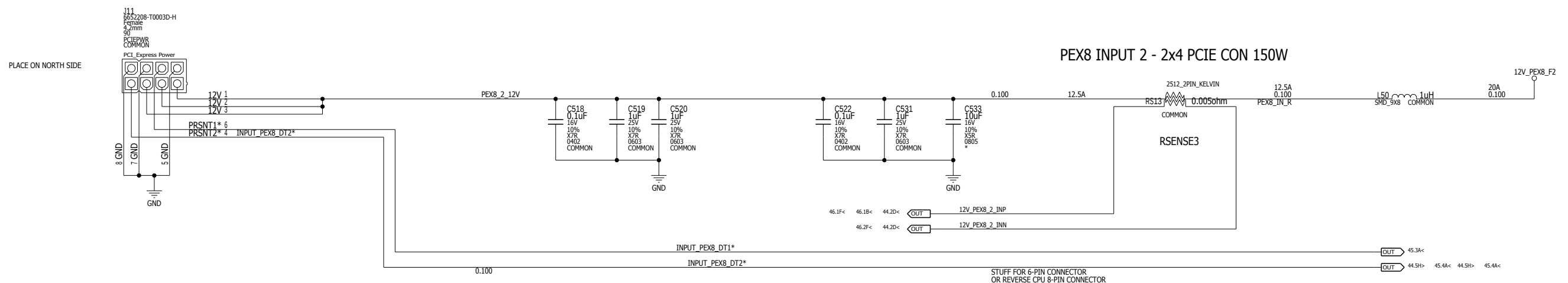
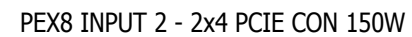
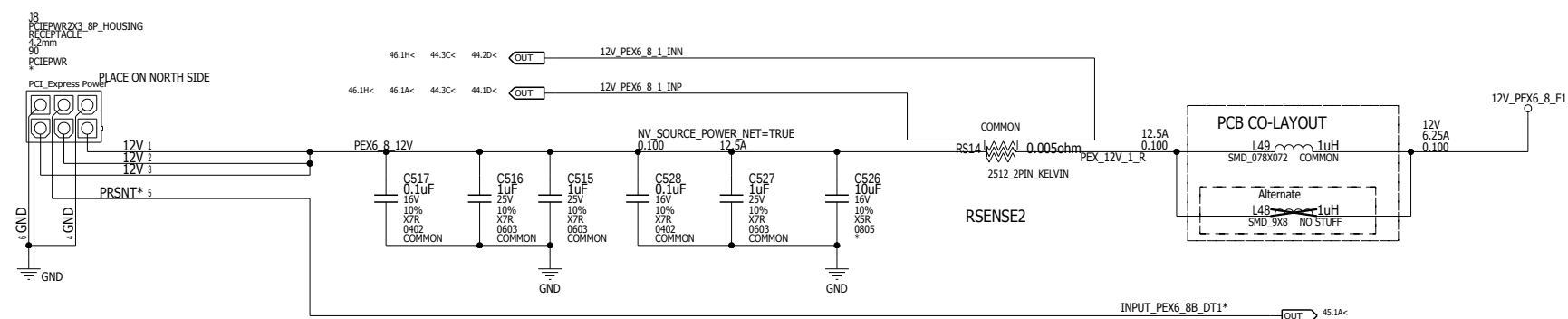
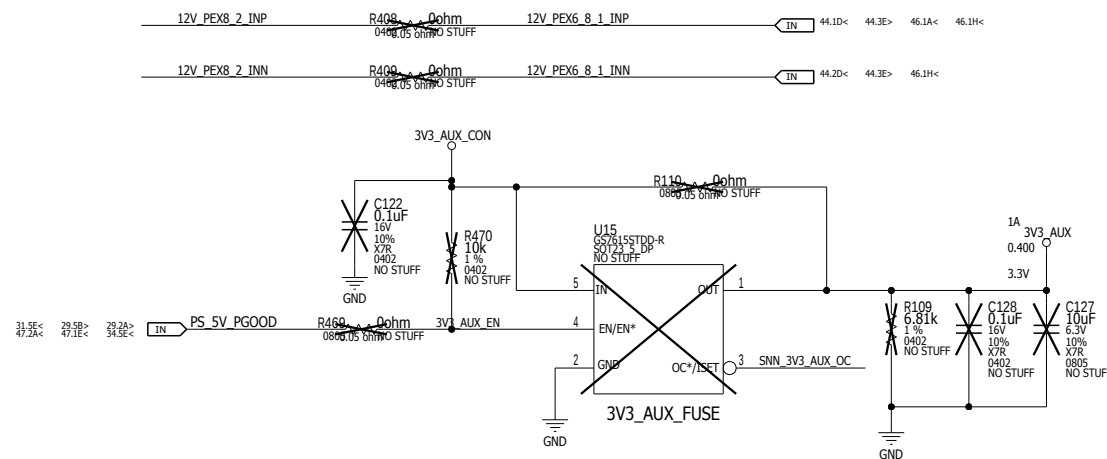
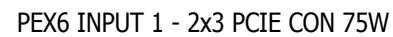
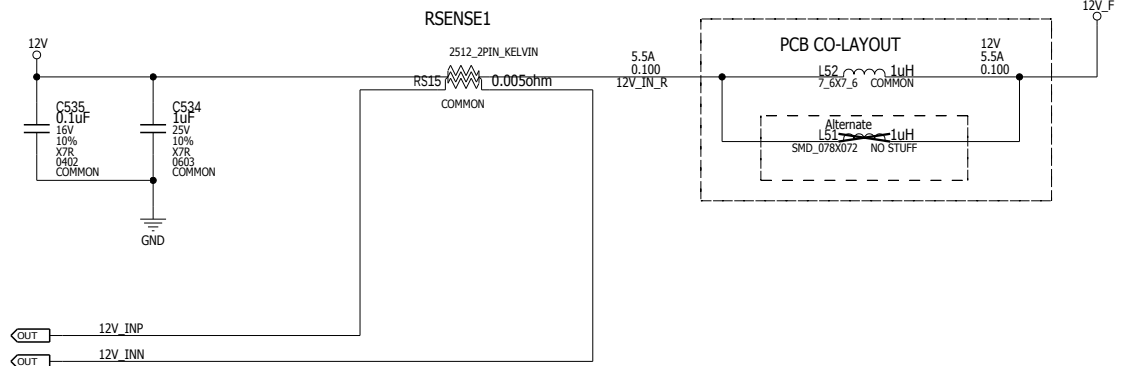
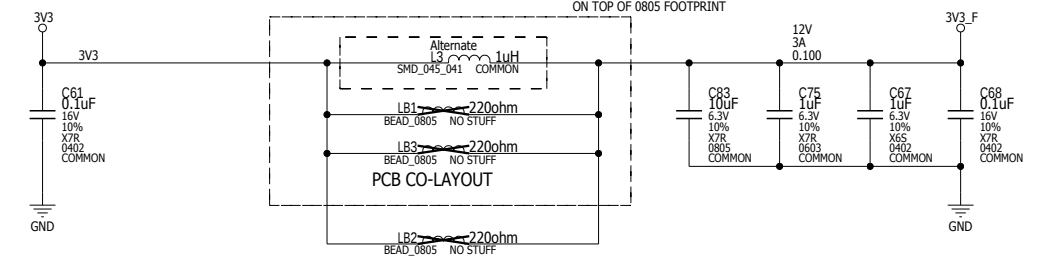
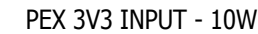
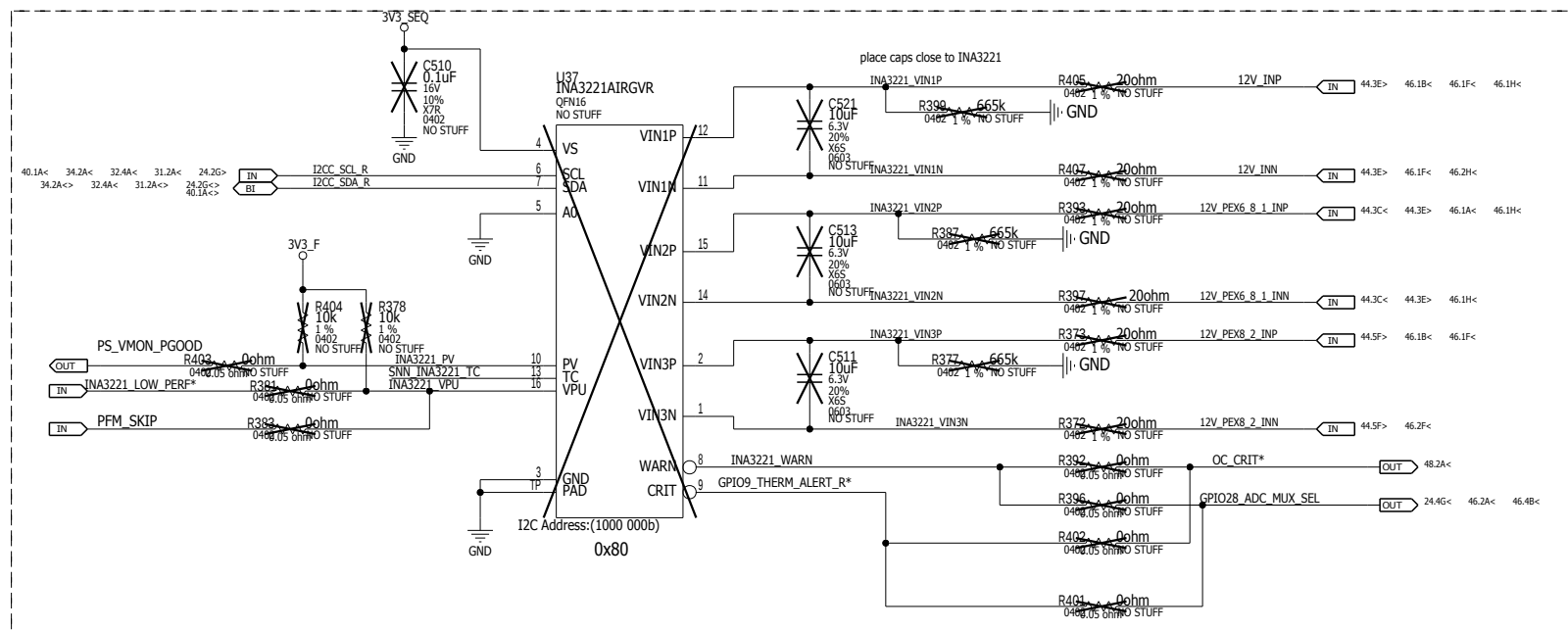


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PAGE 44: PS: Inputs, Filtering, and Monitoring



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	PS: INPUTS, FILTERING AND MONITORING

	PAGE DETAIL	F3: INFO/F3: TOLERANCE AND MONITORING
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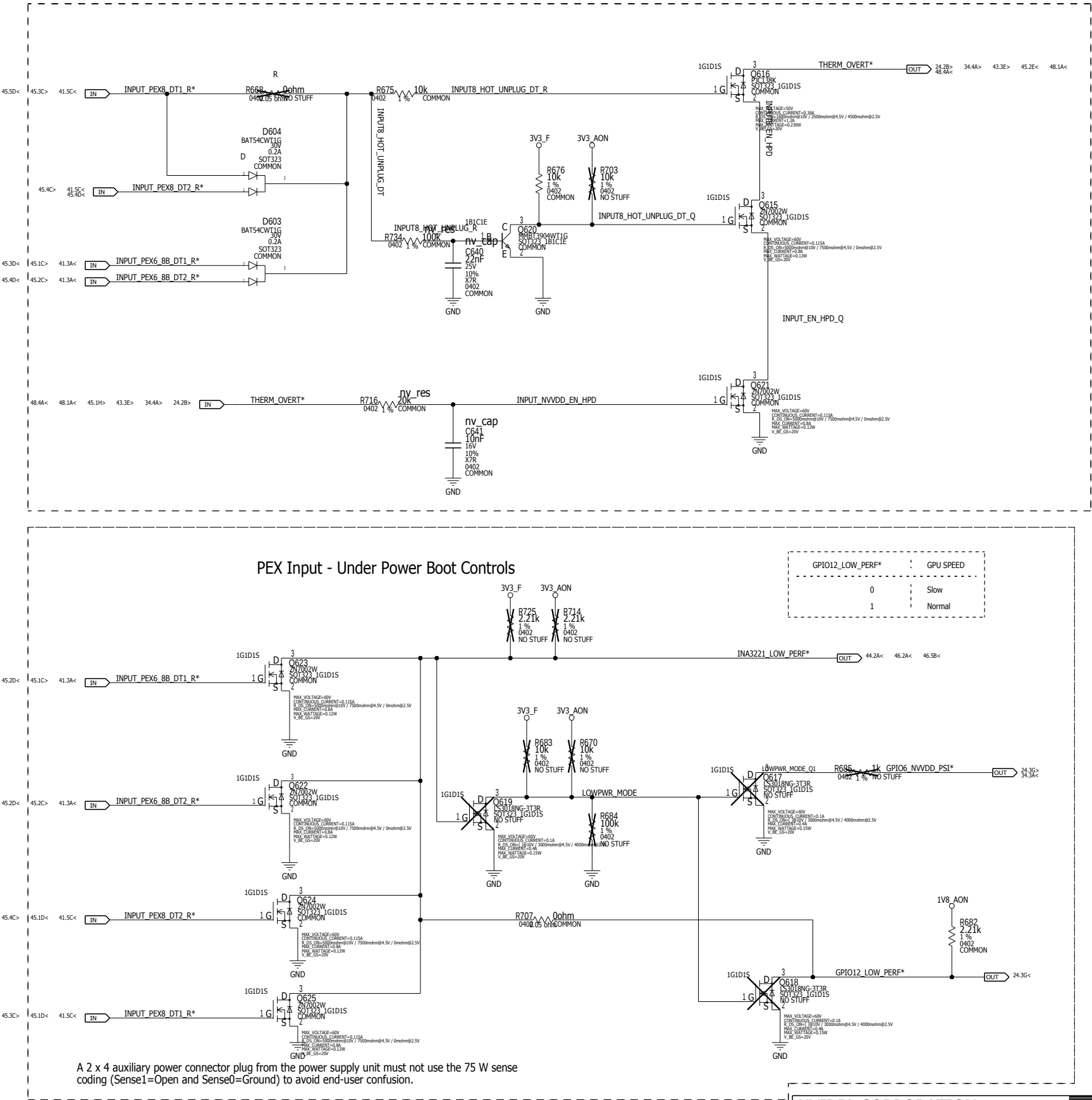
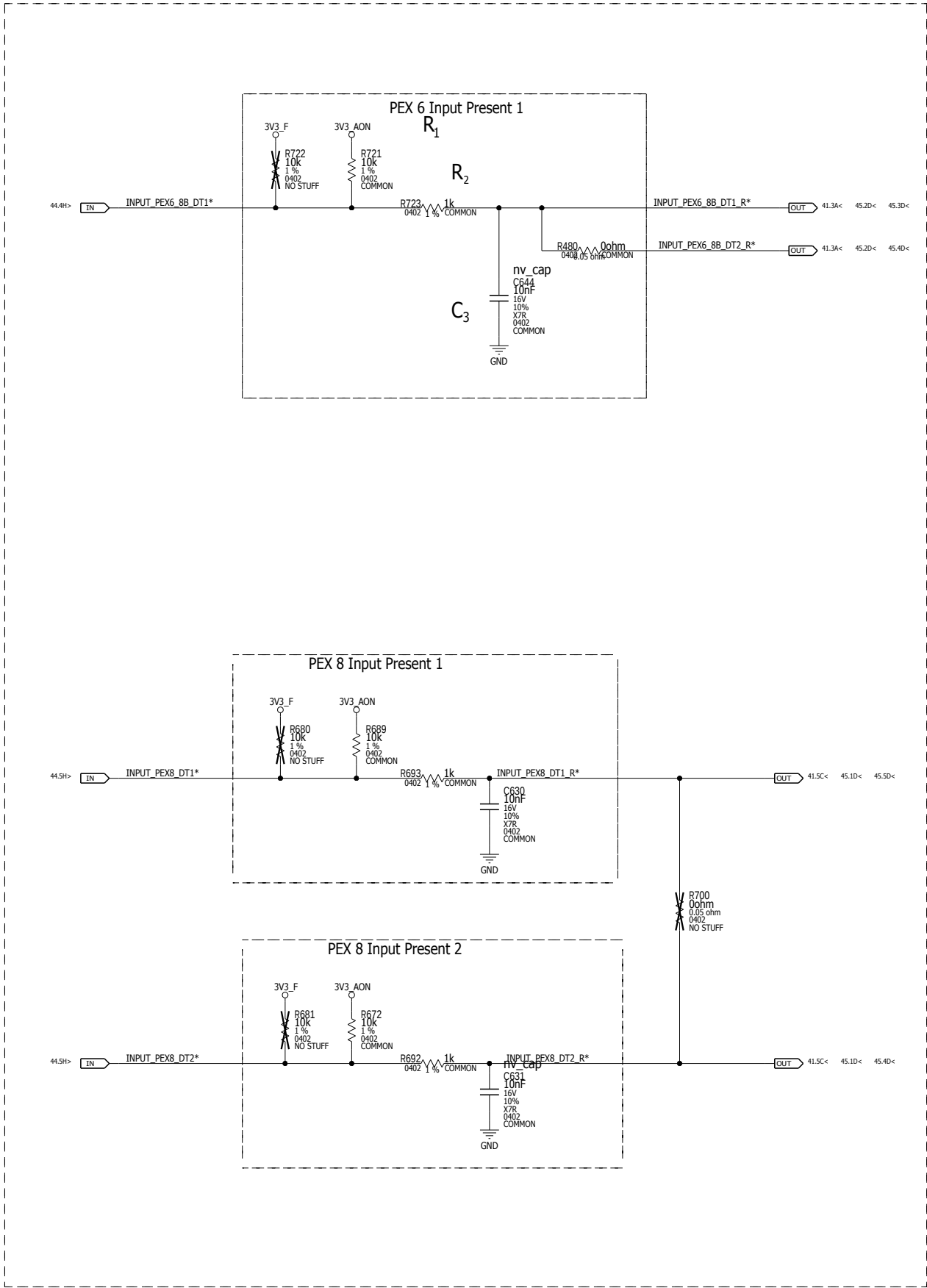
SANTA CLARA, CA 95050, USA

NV_PN	600-1G180-0003-QS2
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PAGE 45: PS: Current Steering, Hot Unplug Detect



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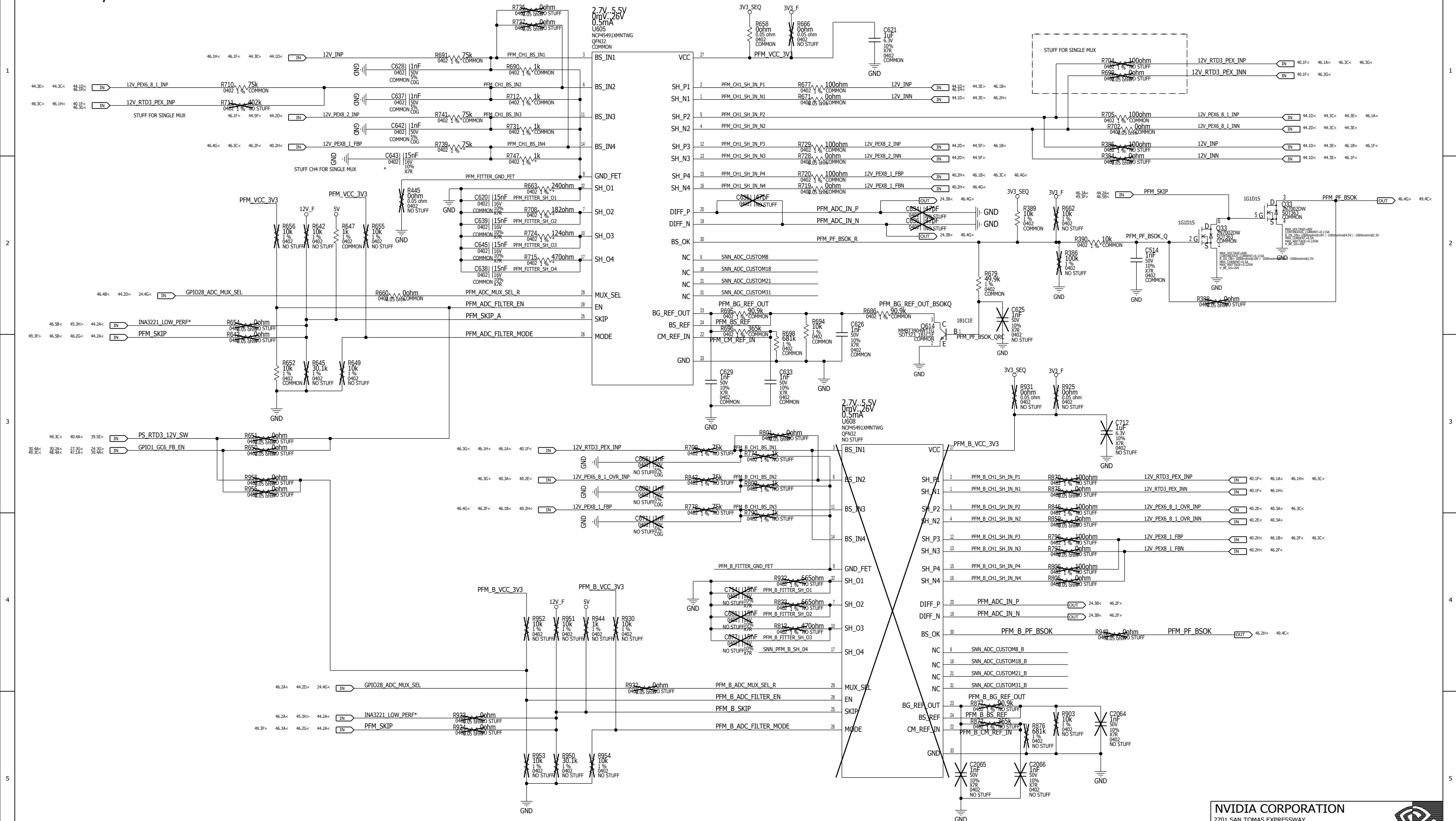
PCB REV PG180-A03

BOM REV A

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PAGE46; PS: Pre-Filter



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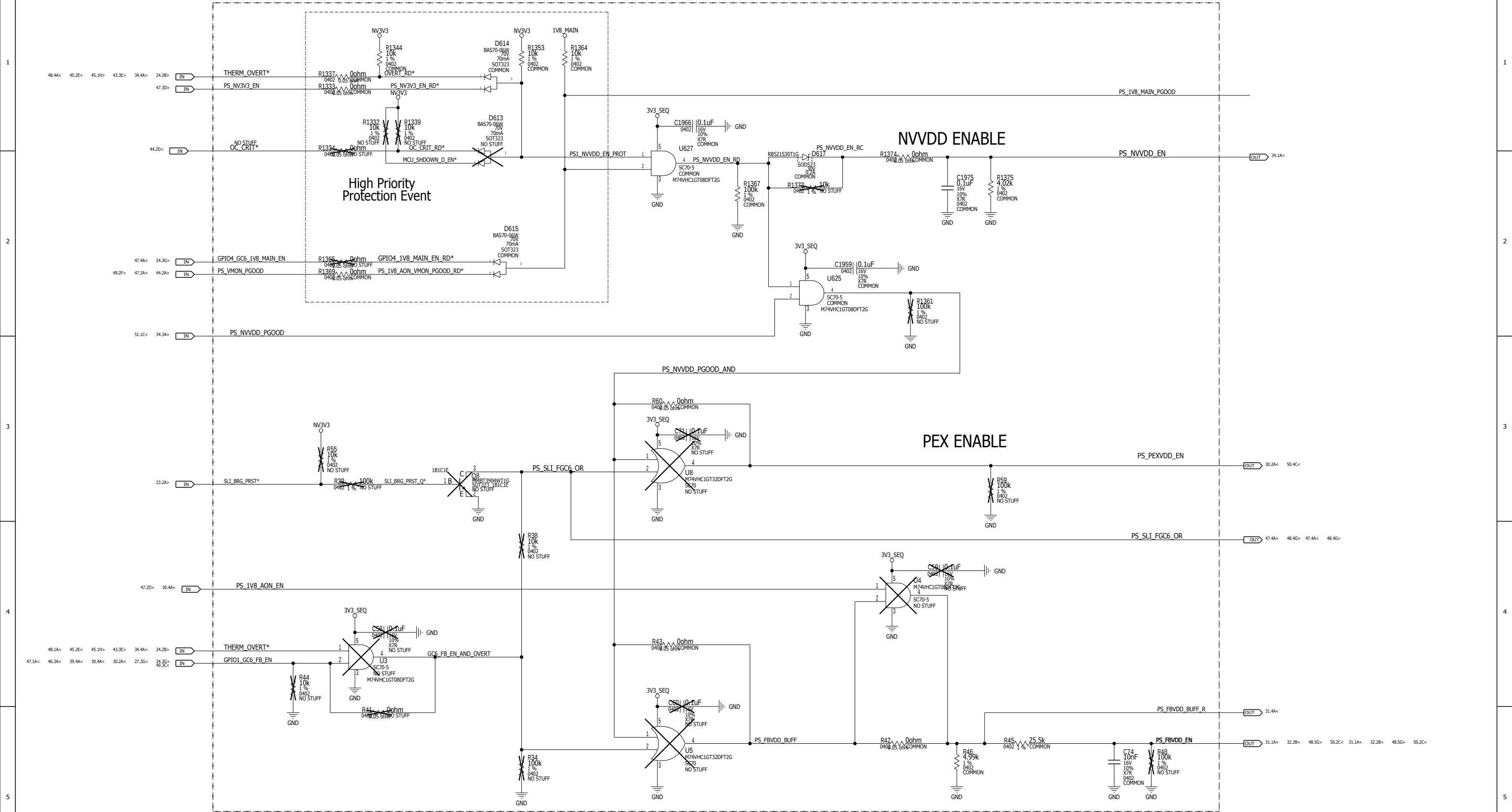


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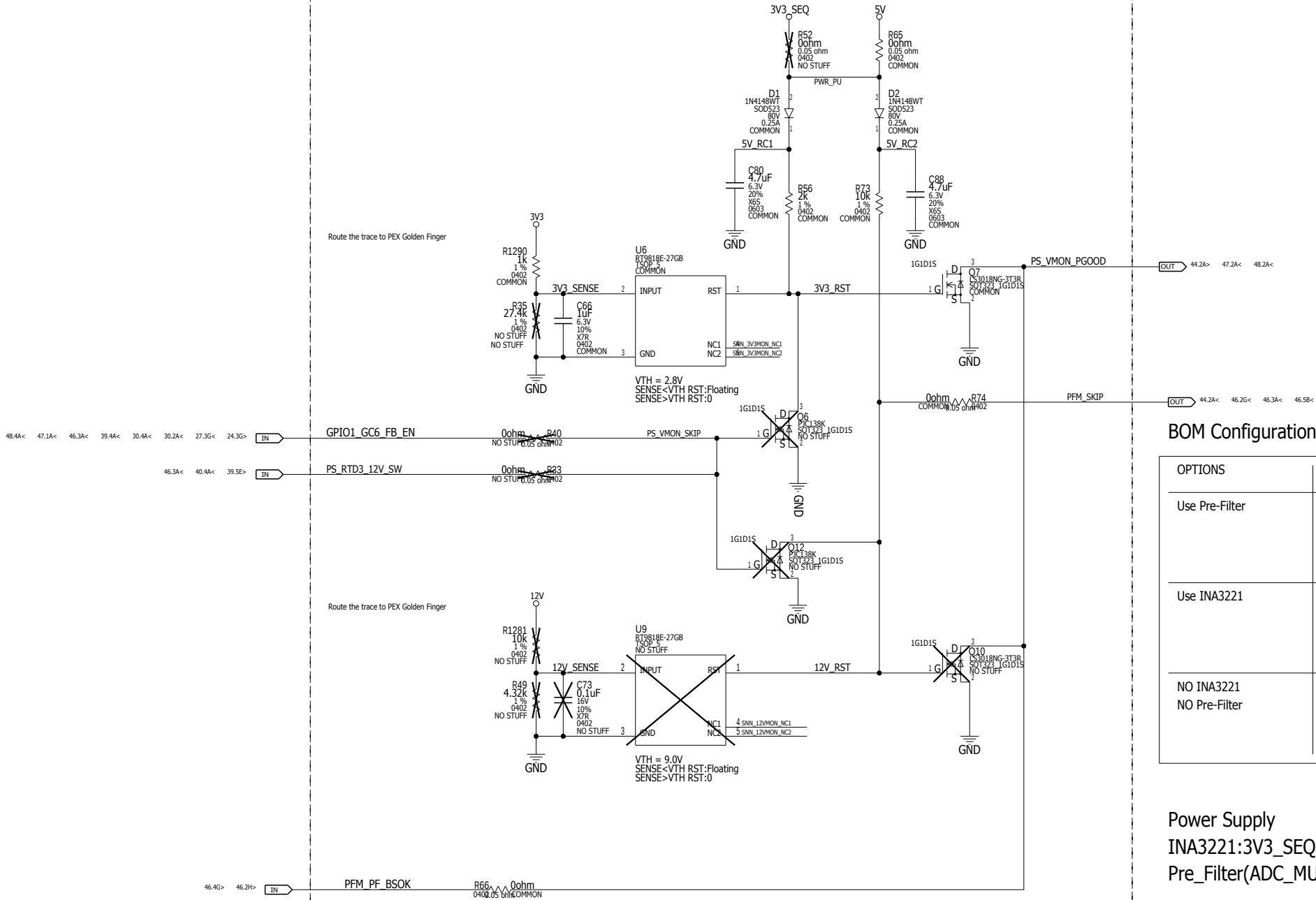
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PAGE 48: SEQUENCE:NV,PEX,FB ENABLE



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PCIE Voltage Monitor



BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

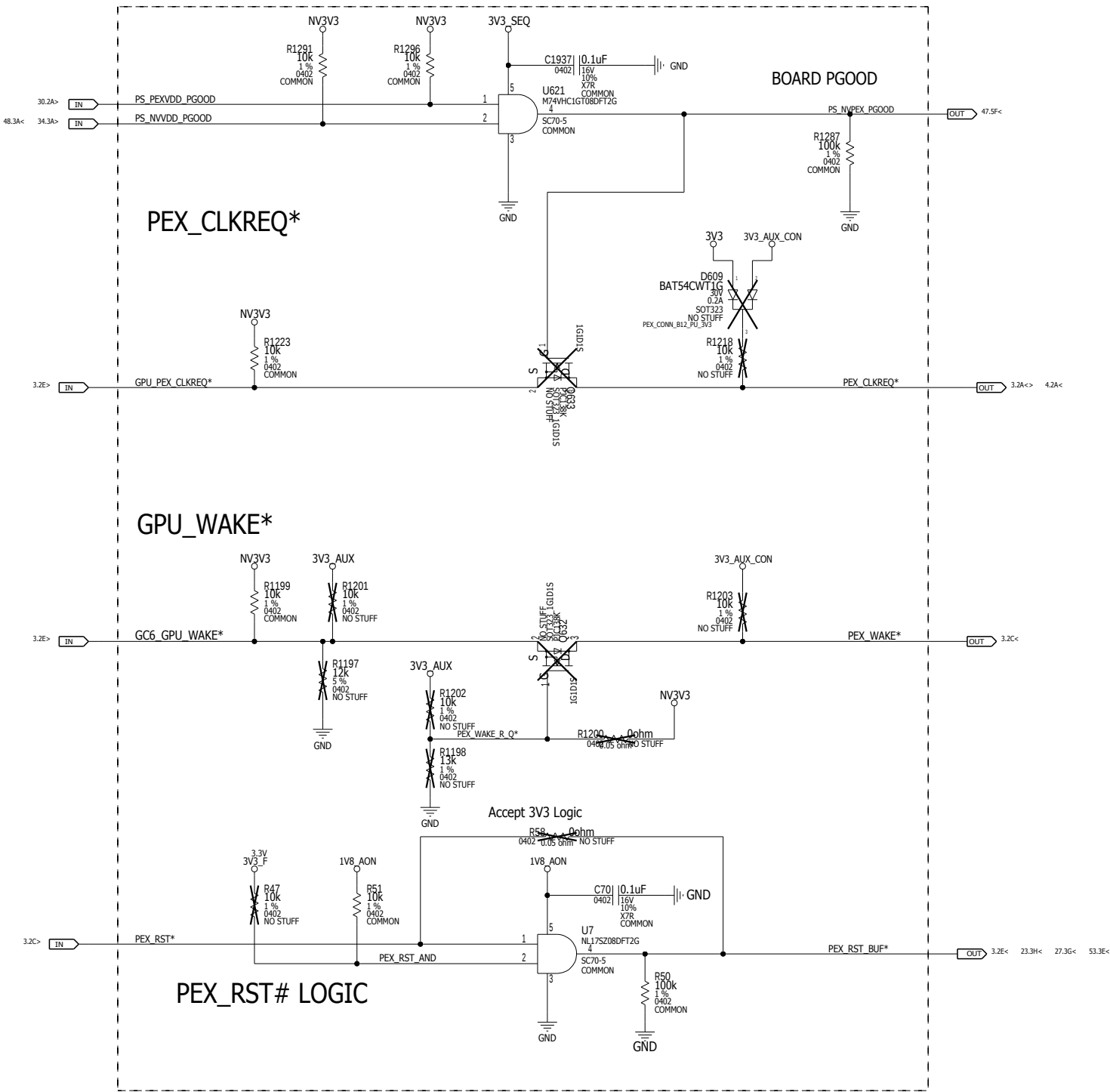
Power Supply
INA3221:3V3_SEQ
Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:
Only use the Primary Pre-Filter to sense 3V3PEX
and All Input 12Vs

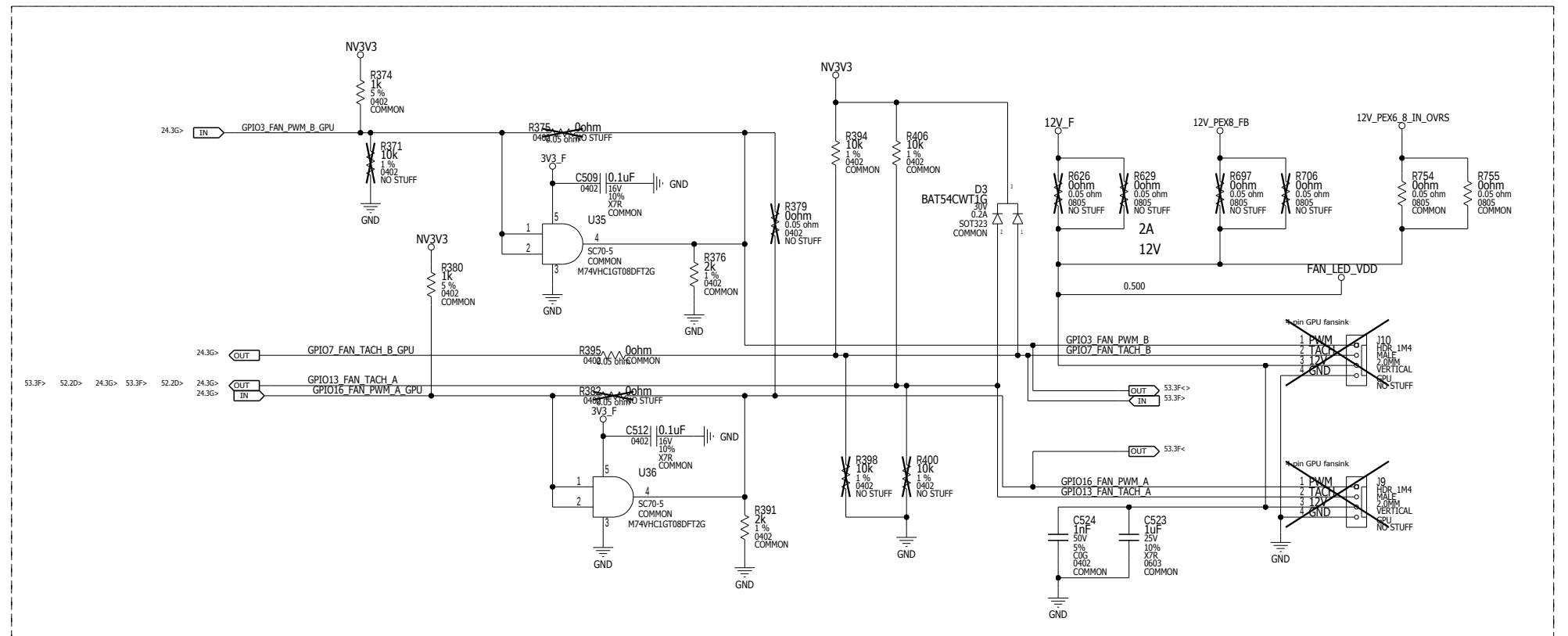
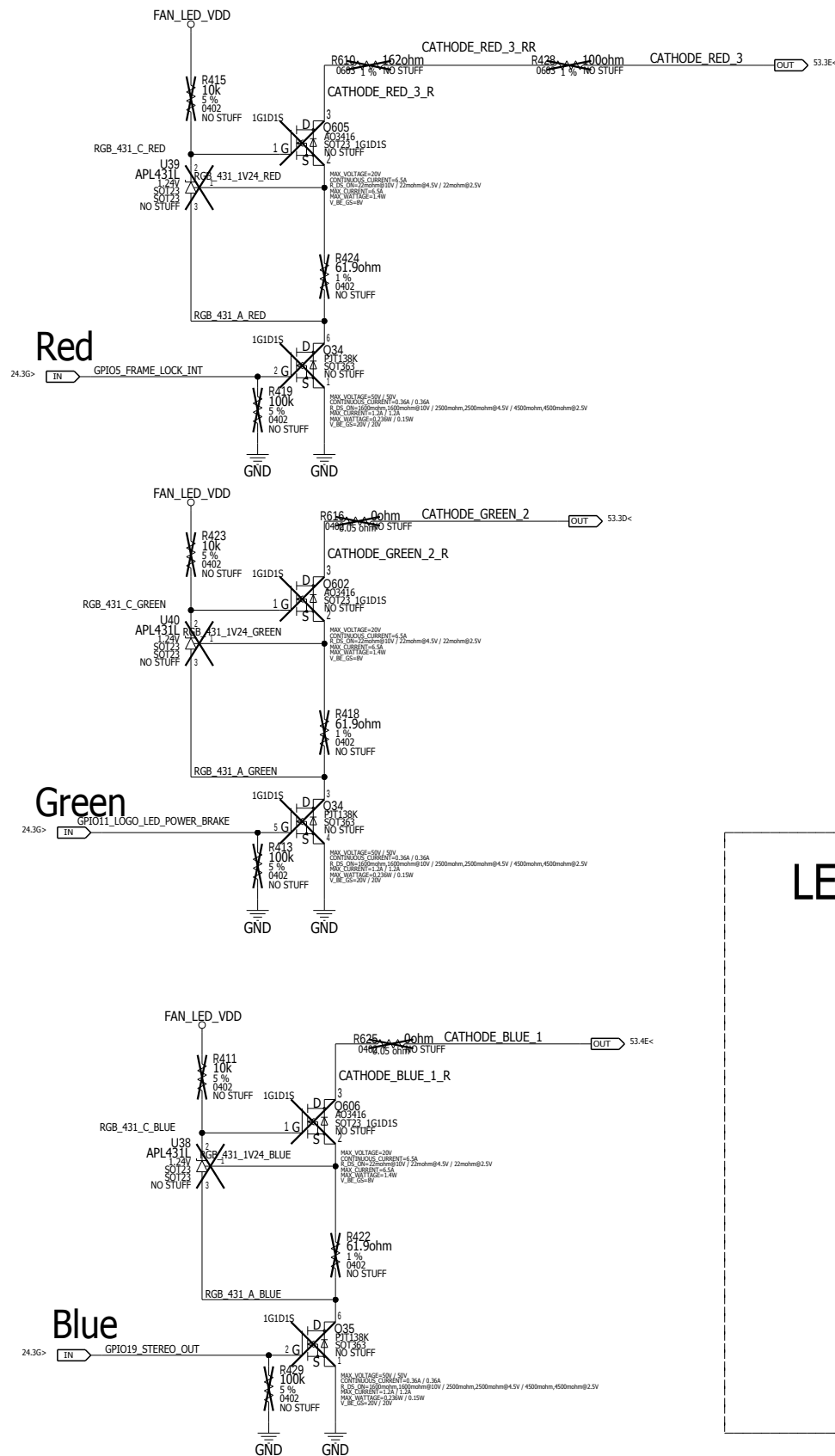
Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

5

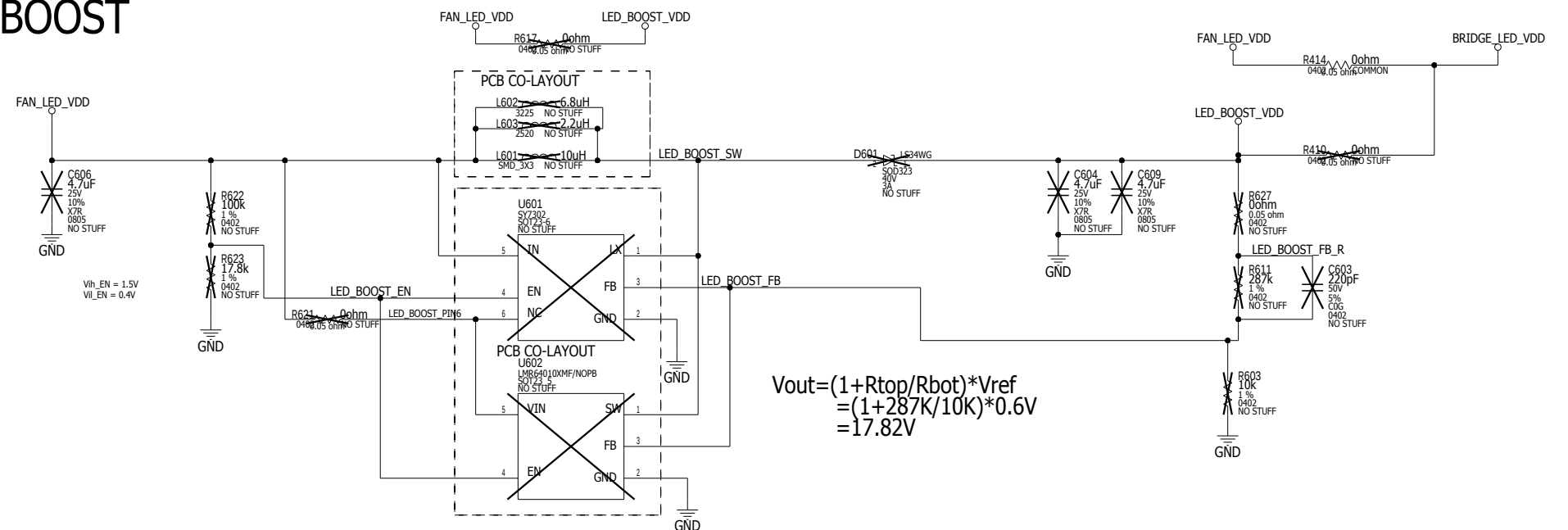




PAGE 52: LED & FAN HEADERS



LED BOOST


$$\begin{aligned} V_{out} &= (1 + R_{top}/R_{bot}) * V_{ref} \\ &= (1 + 287K/10K) * 0.6V \\ &= 17.82V \end{aligned}$$

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY, COMMON & NO_STUFF ASSEMBLY NOTES AND BOM NOT FINAL
PAGE DETAIL	LED & FAN HEADERS

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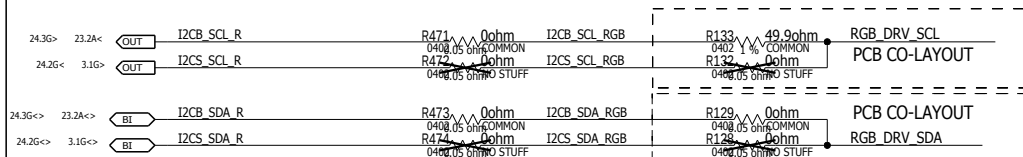
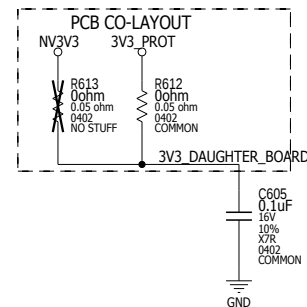
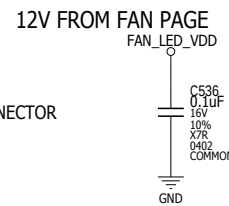
NVIDIA CORPORATION

2701 SAN TOMAS EXPRESSWAY
SANTA CLARA, CA 95050, USA



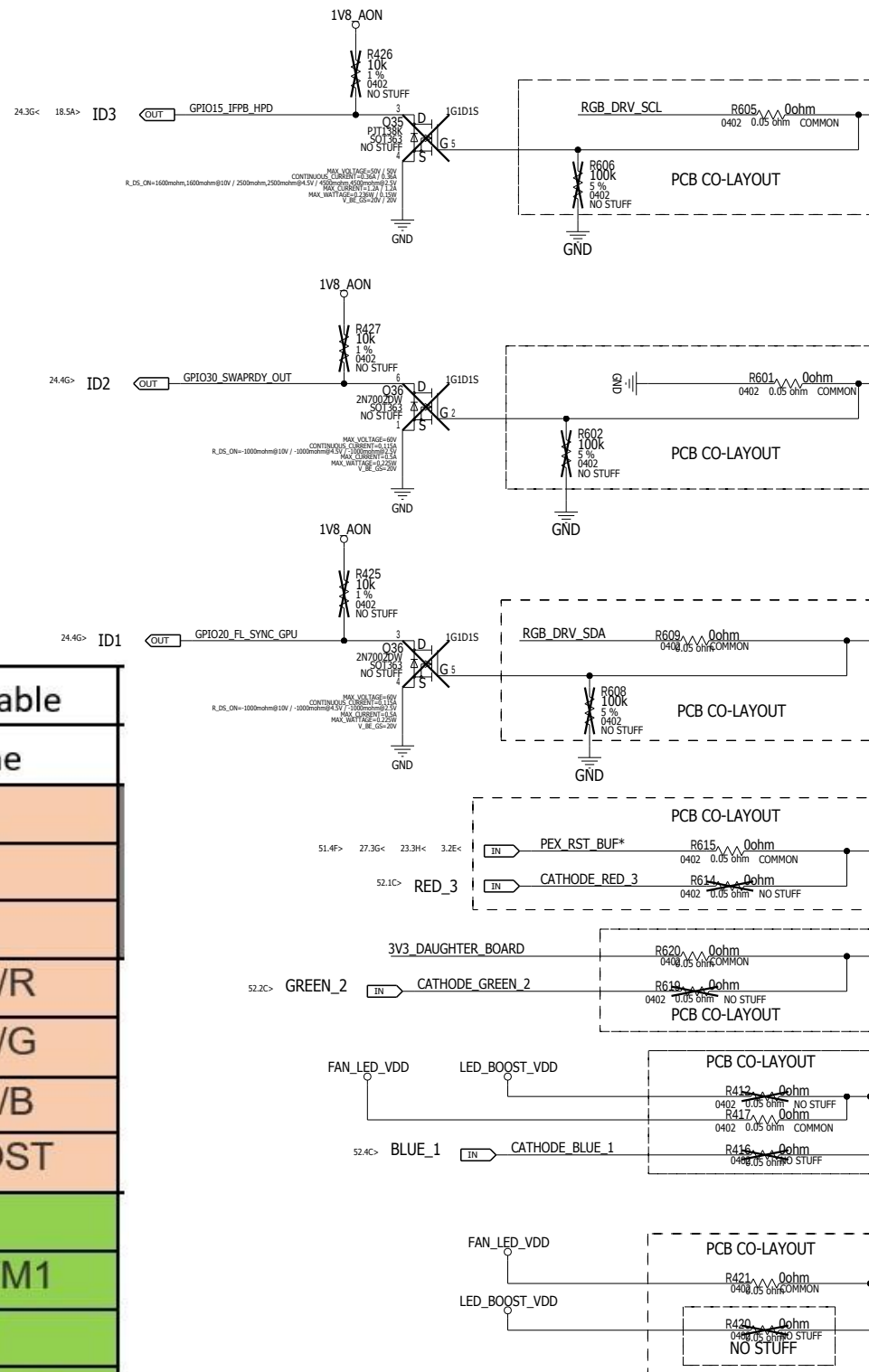
NV_PN	600-1G180-0003-QS2
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PCB REV	PG180-A03	PAGE	52 OF 54
BOM REV	A	DATE	06-FEB-2019



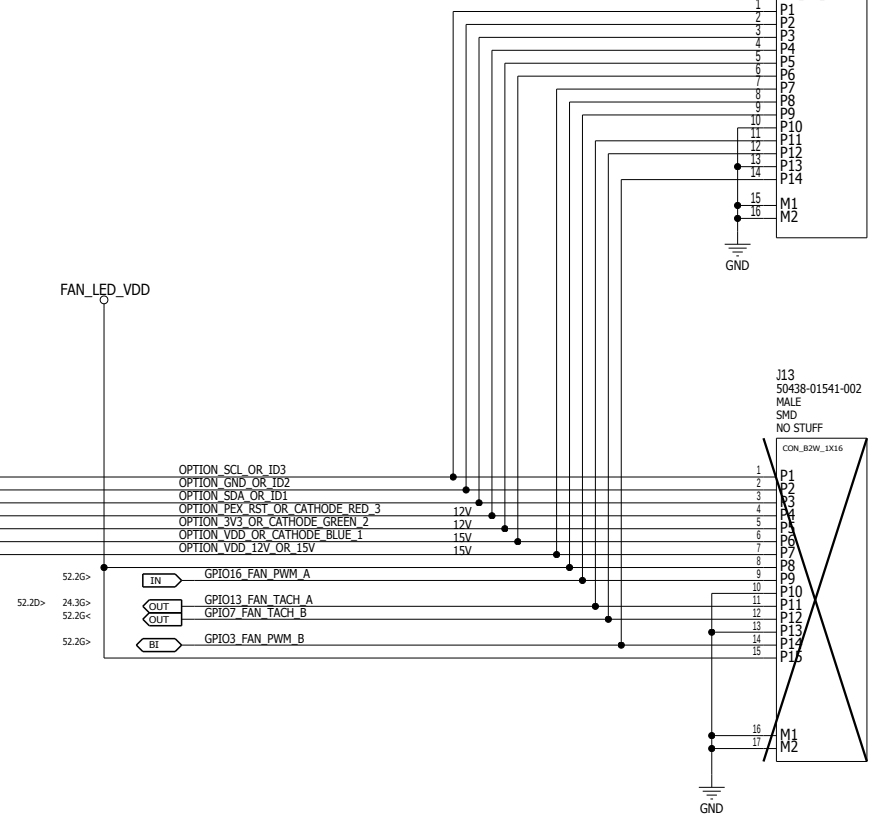
8-bit I2C Address of MCU on Daughter Board: TBD

MCU Solution		For ONE ZONE RGB/cable	
PIN SEQ	Pin Name	PIN SEQ	Pin Name
1	I2C_SCL	1	ID3
2	GND	2	ID2
3	I2C_SDA	3	ID1
4	PEX_RST_BUF*	4	DRIVE3/R
5	NV3V3	5	DRIVE2/G
6	12V/BOOST	6	DRIVE1/B
7	12V	7	12V/BOOST
8	12V	8	12V
9	FAN_PWM1	9	FAN_PWM1
10	GND	10	GND
11	FAN_TACH1	11	FAN_TACH1
12	FAN_TACH2	12	FAN_TACH2
13	GND	13	GND
14	FAN_PWM2	14	FAN_PWM2
		15	12V



14-PIN STRAIGHT PRIMARY SOURCE -> 080-1586-000: ACES \$0.115
14-PIN STRAIGHT SECOND SOURCE -> 080-1600-000: WIESON \$0.2

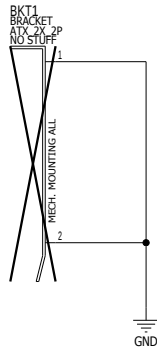
FOR MCU SOLUTION



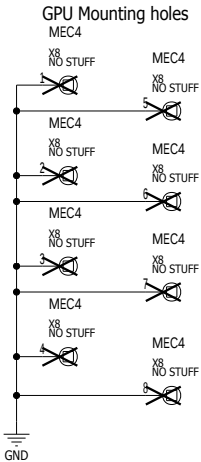
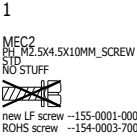
FOR ONE ZONE RGB SOLUTION

15-PIN STRAIGHT PRIMARY SOURCE -> 080-1617-000: ACES \$0.1165
15-PIN STRAIGHT SECOND SOURCE -> 080-1628-000: WIESON \$0.23

Brackets:



Bracket Screw



STIFFENER

