PG180-A02

256b GDDR6 x16
TALL DP + DP + DP + HDMI/DP + USB

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19	Change J3 footprint
20	Remove DP co-layout
21	Remove JTAG & unused GPIO
32	Remove 0031_PS_ FBVDD CONTROLLER OVR3
34	NVVDD CONTROLLER change to MP2888A
35	DRMOS change to 10phases
36	DRMOS change to 10phases
37	Add NVVDD Output CAP
41	Remove INPUT SWITCH Rail Balance
44	J8 change to 8pin
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45	Add Hot Unplug Detect for J8
52	Add Remove LED & Fan Vin_12V option
53	Add MCU IT8295 for RGB LED

V372-3.1 change List

Base on V372-3.0，No changed

V372-3.2 change List

Base on V372-3.0，No changed

V372-3.0 change List

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19	Add DP_PWR bypass resistor
	C12 changed to 560uF Solid CAP
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31	FBVDD controller changed to uP1666QQKF
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44	Remove SLI_BRG_PRST* 、PS_1V8_AON_EN、THERM_OVERT*
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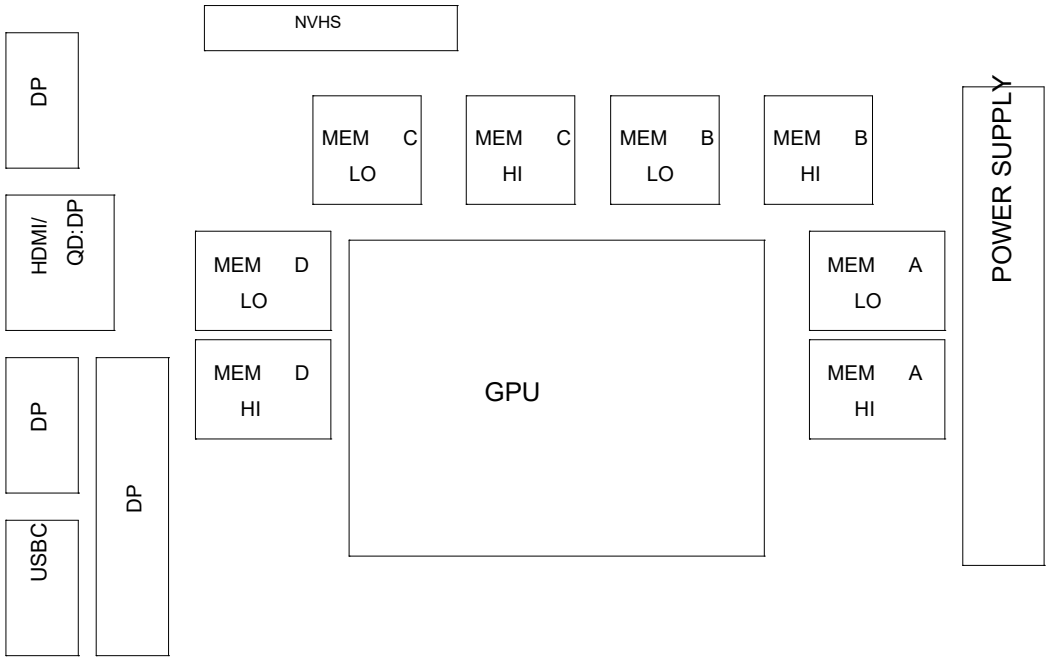
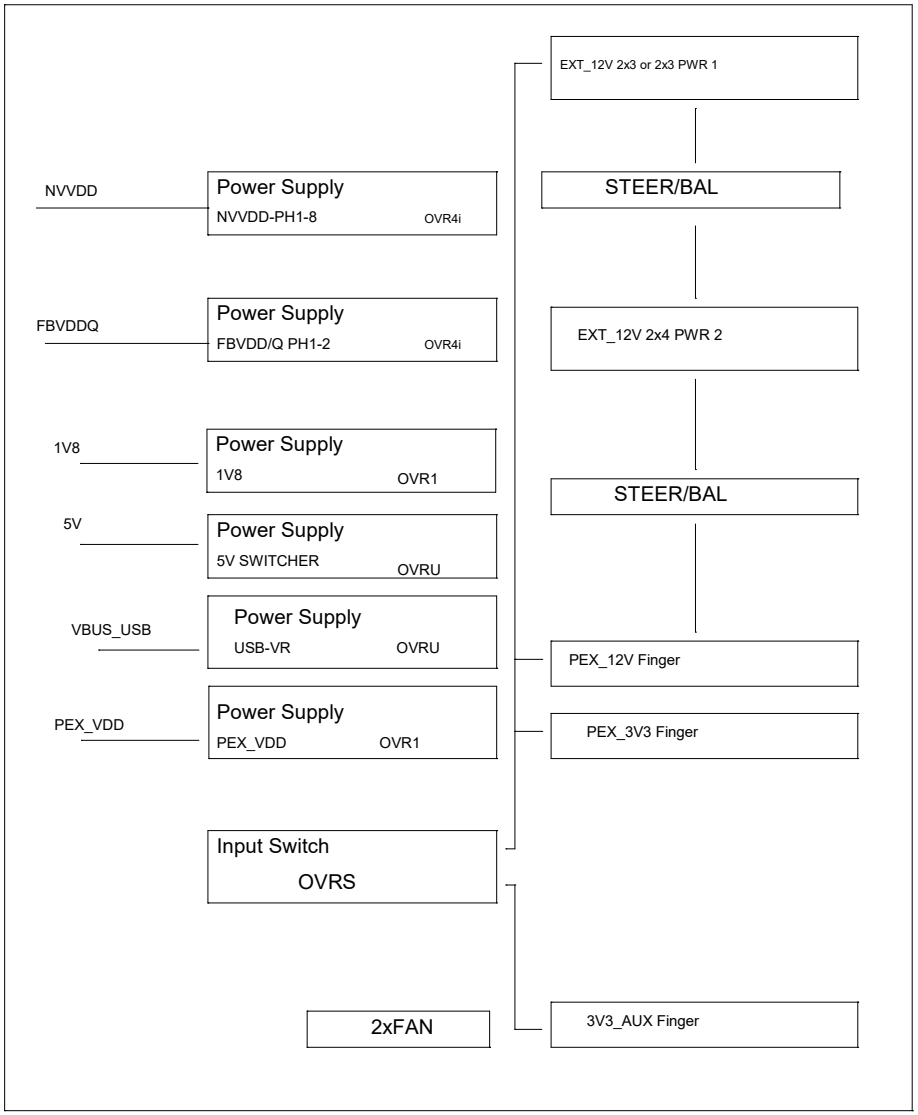
Page2: Block Diagram





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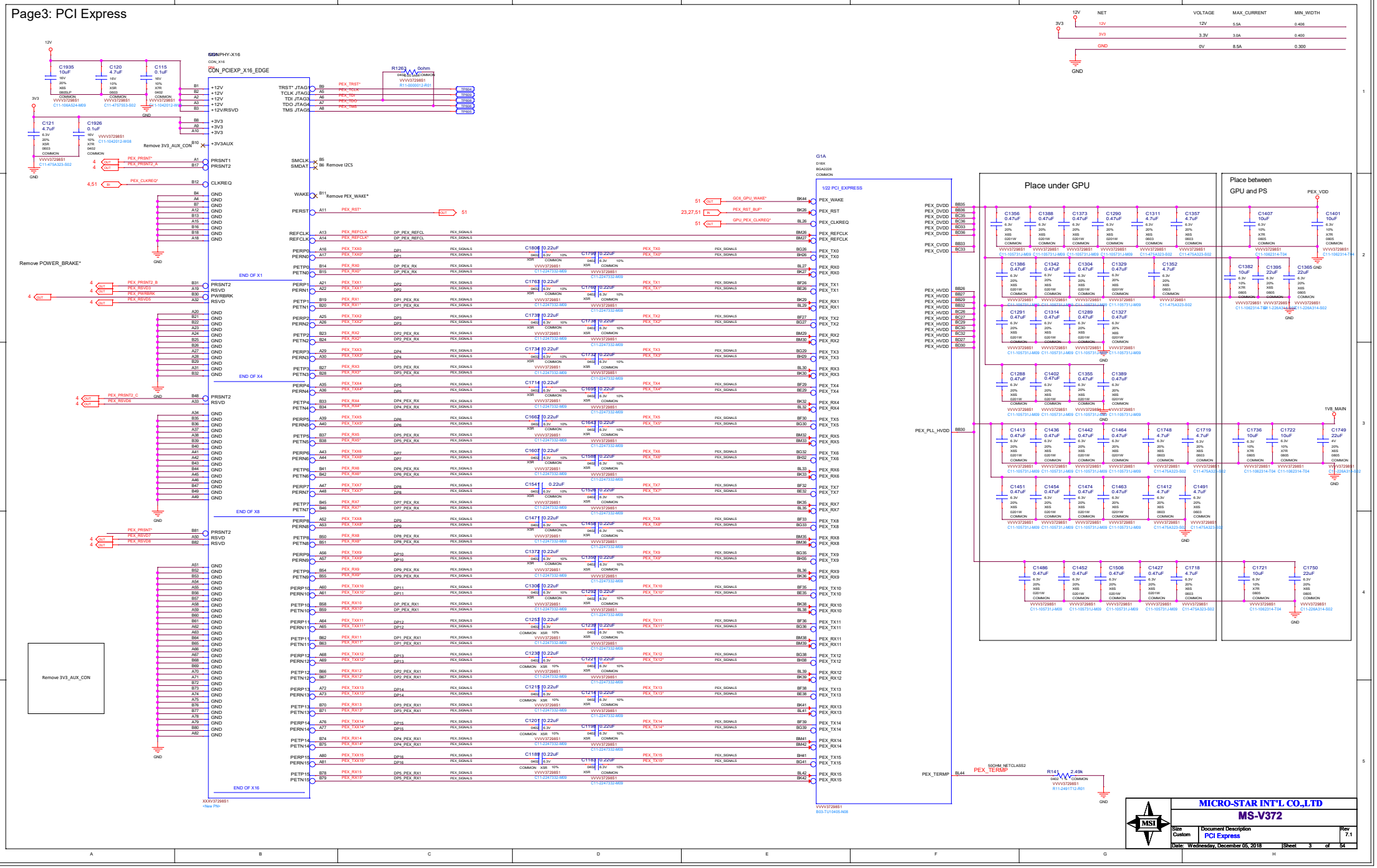
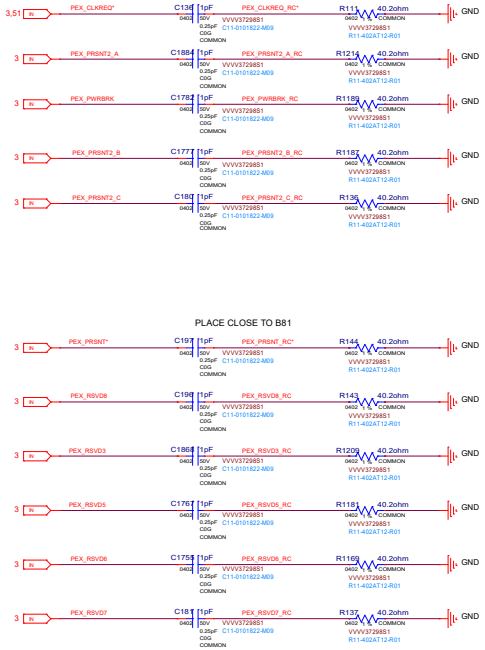
Page3: PCI Express



Page4: PCI Termination



PLACE CLOSE TO B81

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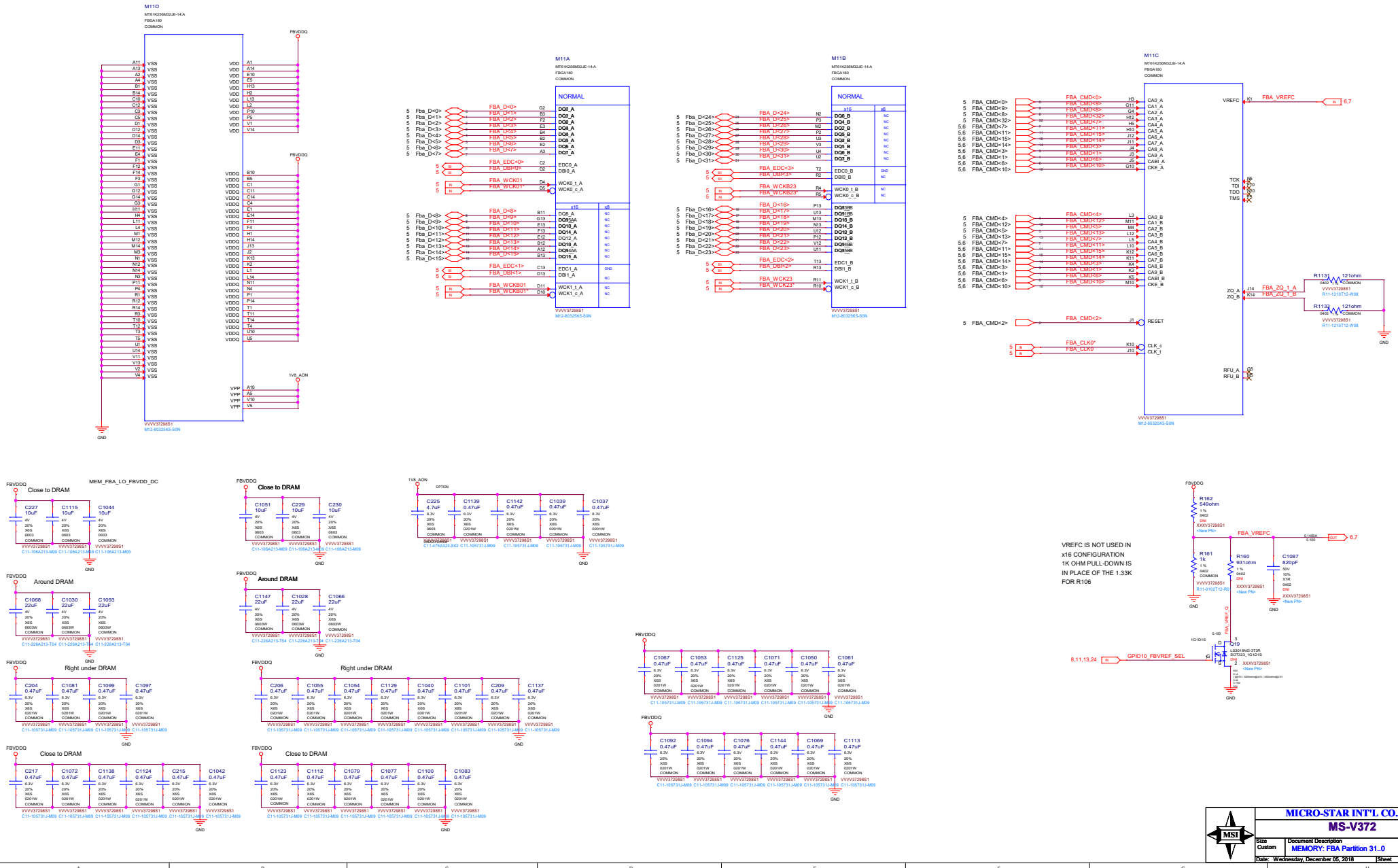
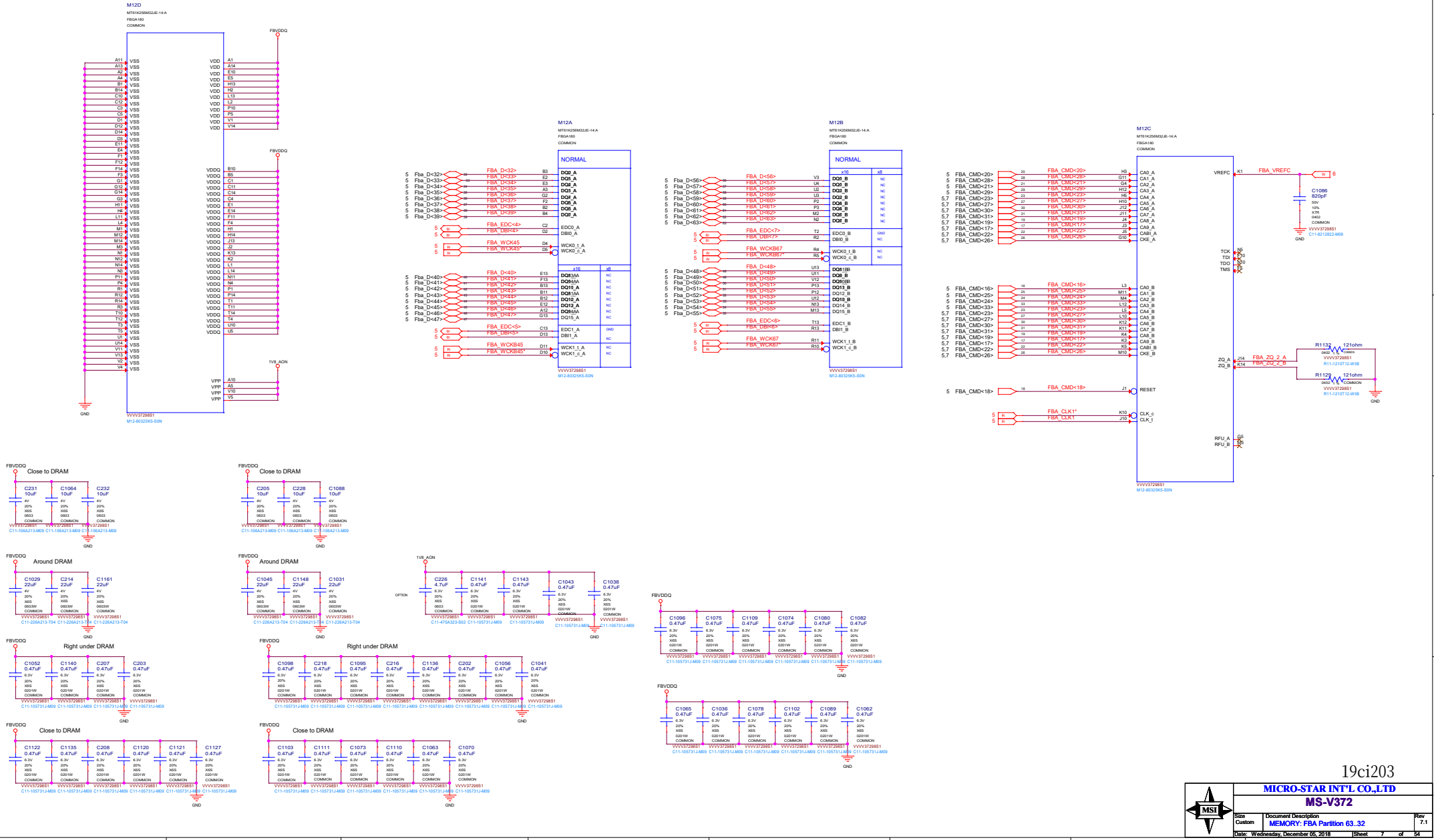
Page5: MEMORY: GPU Partition A/B

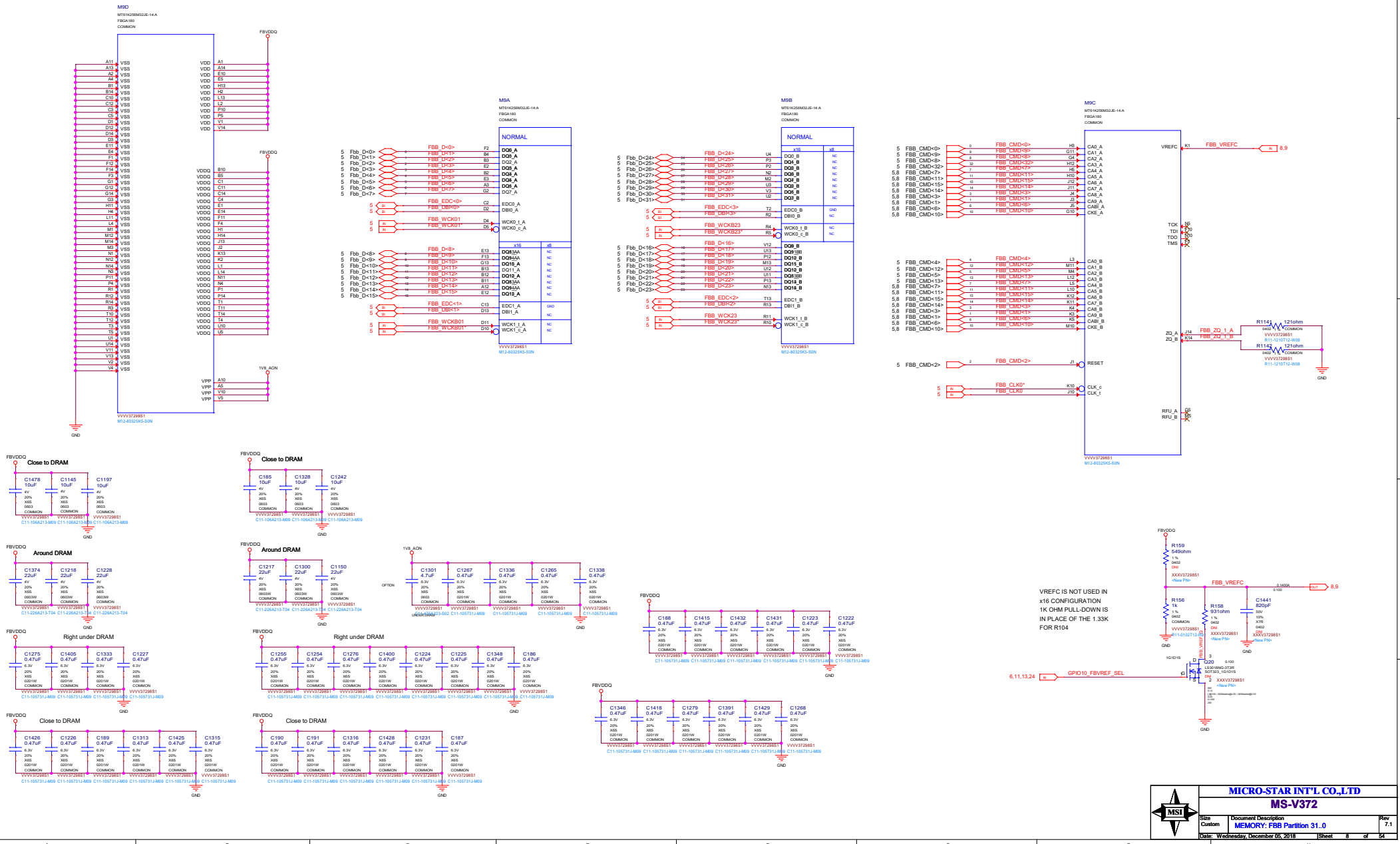
Page6: MEMORY: FBA Partition 31..0



Page7: MEMORY: FBA Partition 63..32



Page8: MEMORY: FBB Partition 31..0



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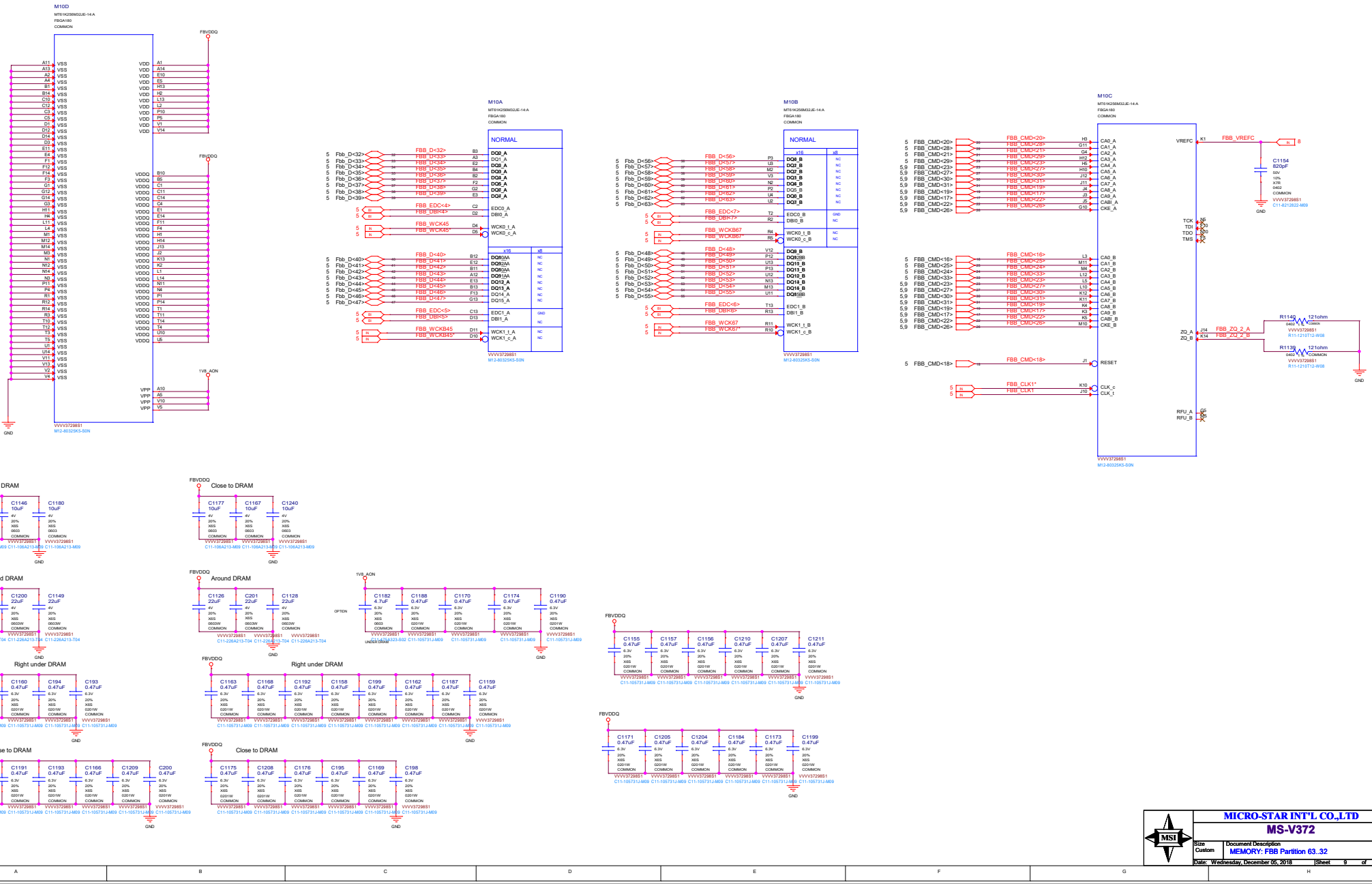

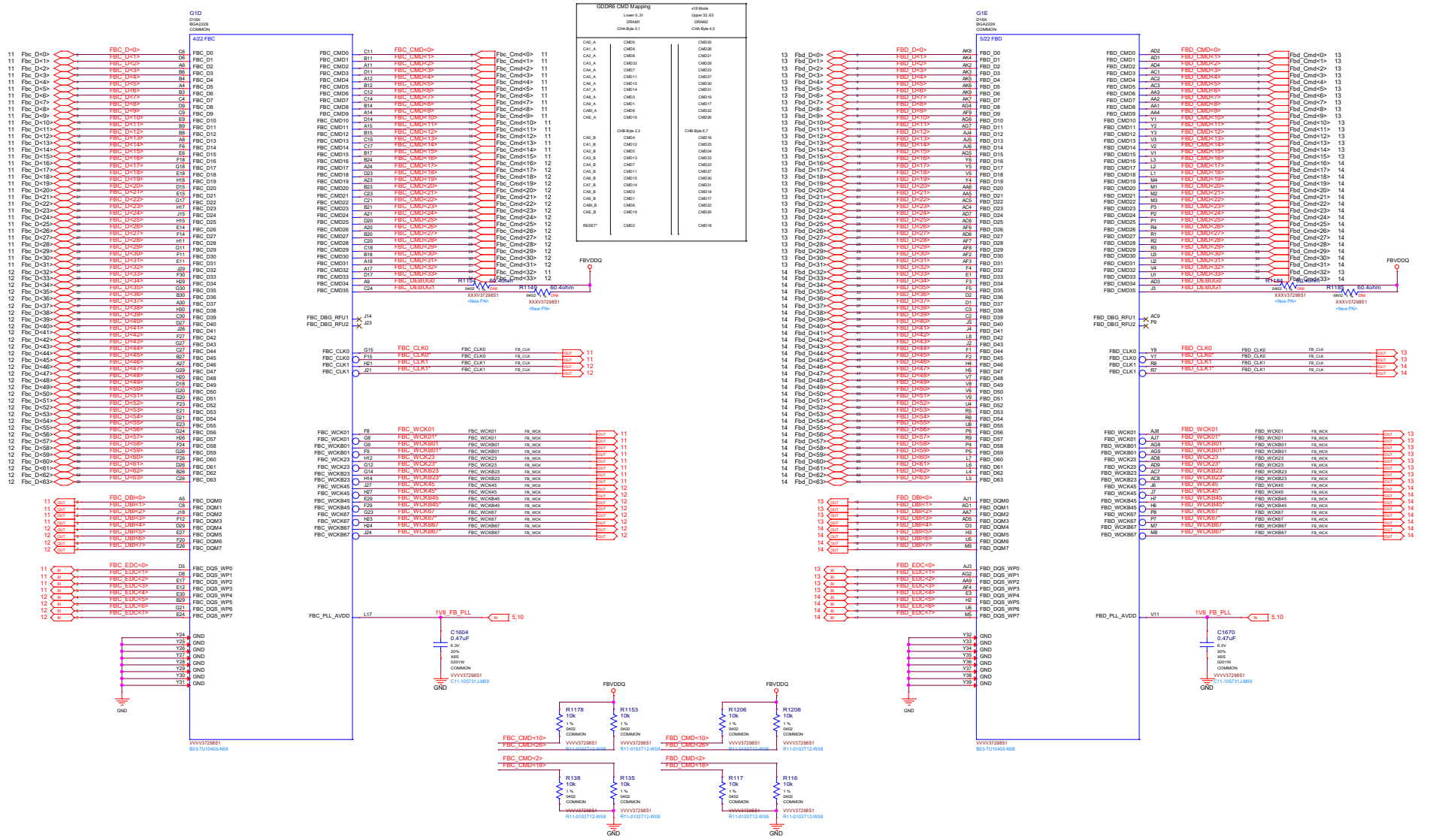

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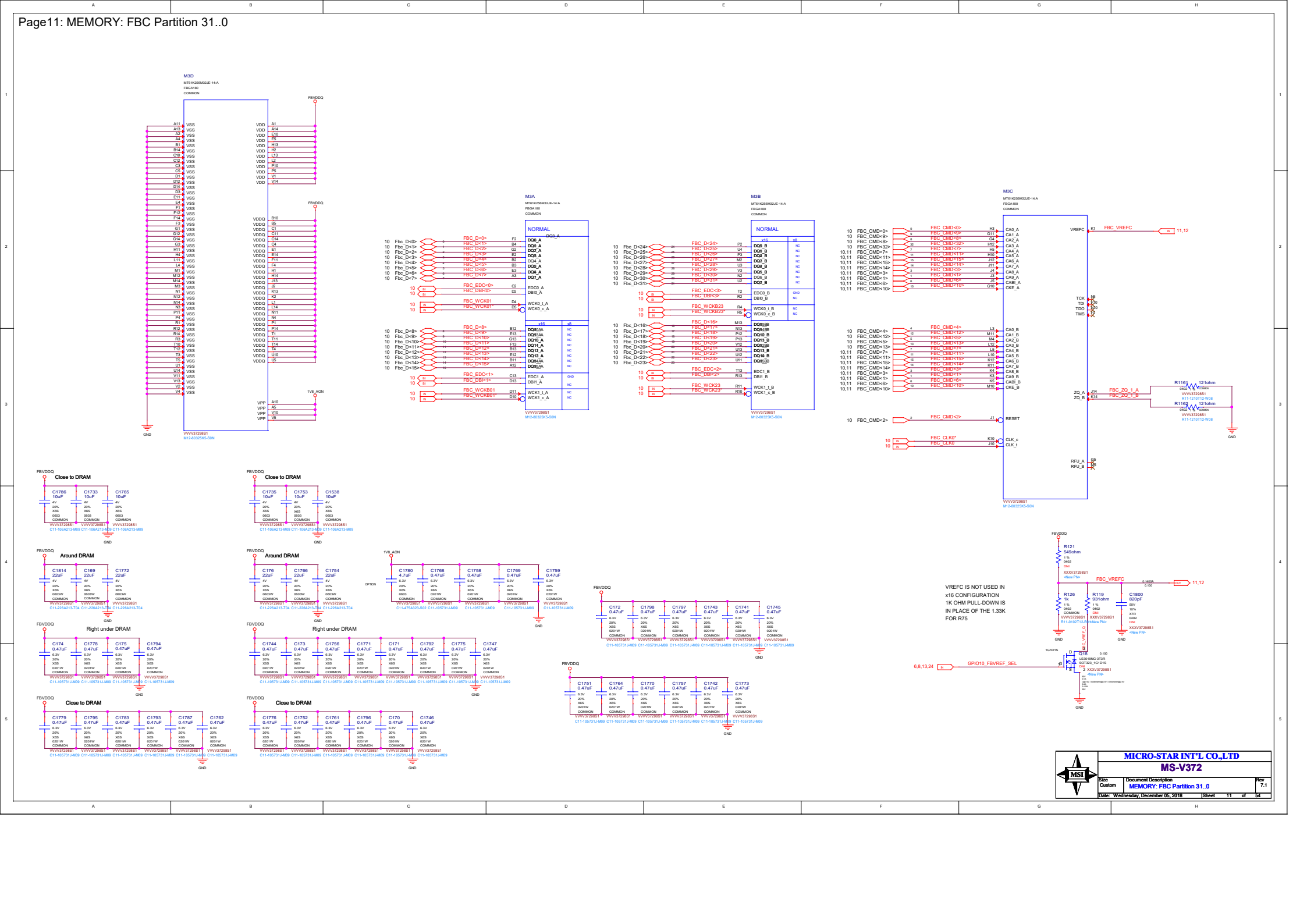
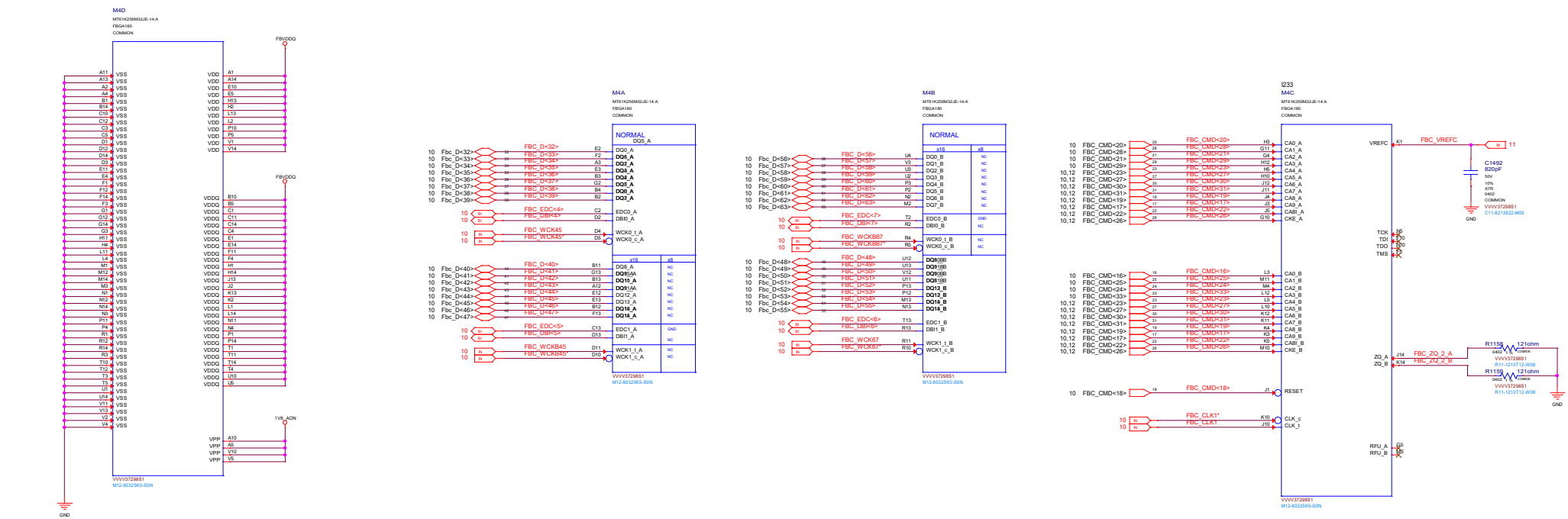
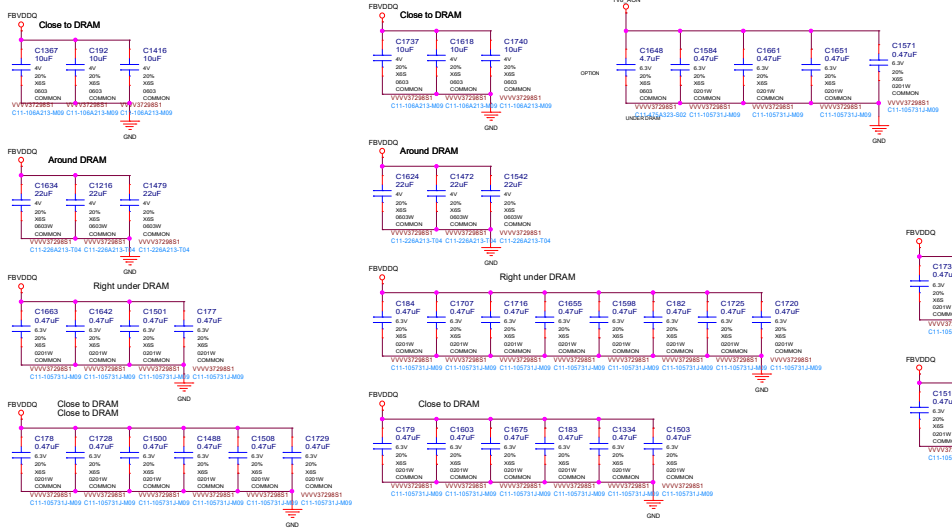
Page11: MEMORY: FBC Partition 31..0



Page12: MEMORY: FBC Partition 63..32





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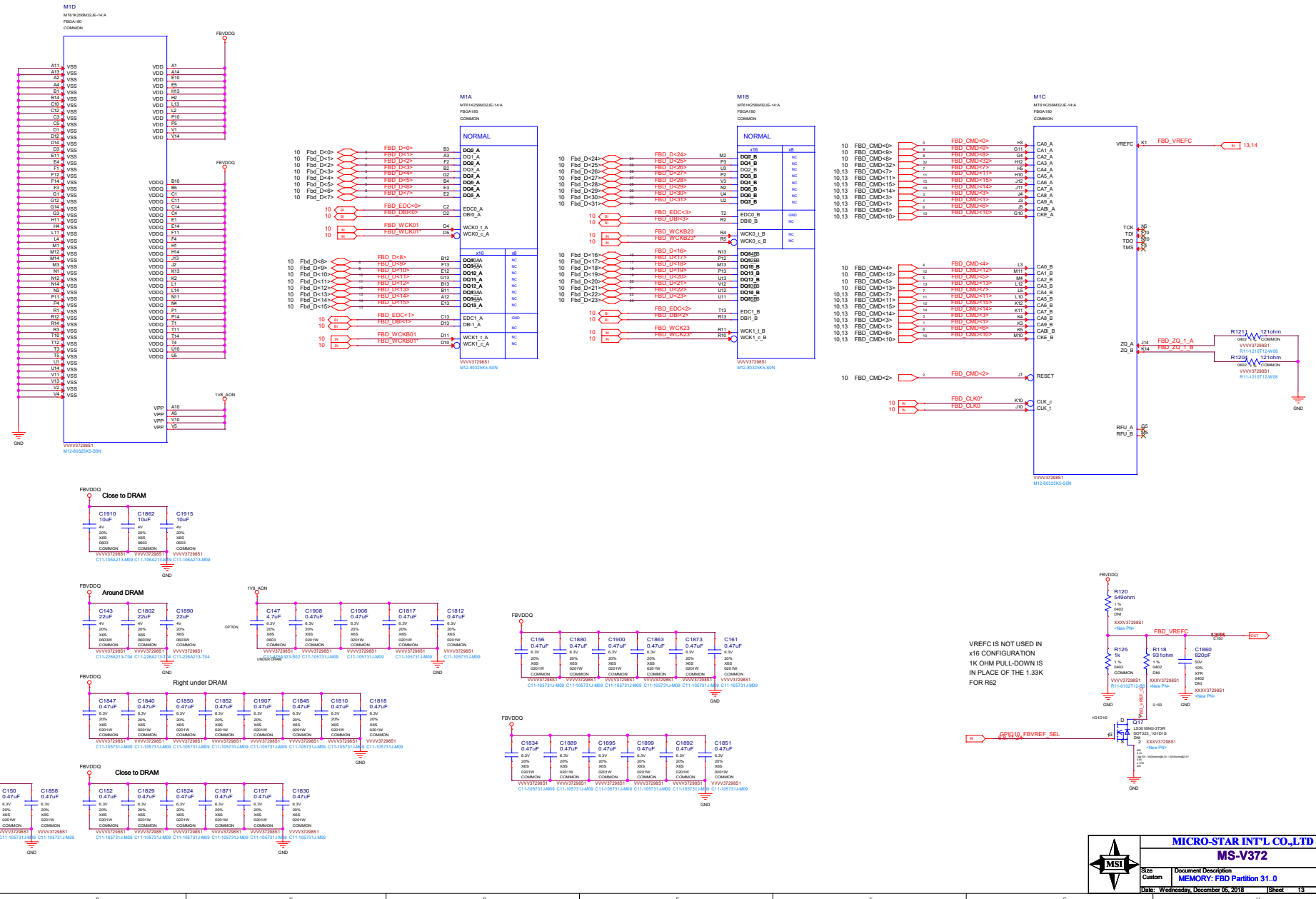

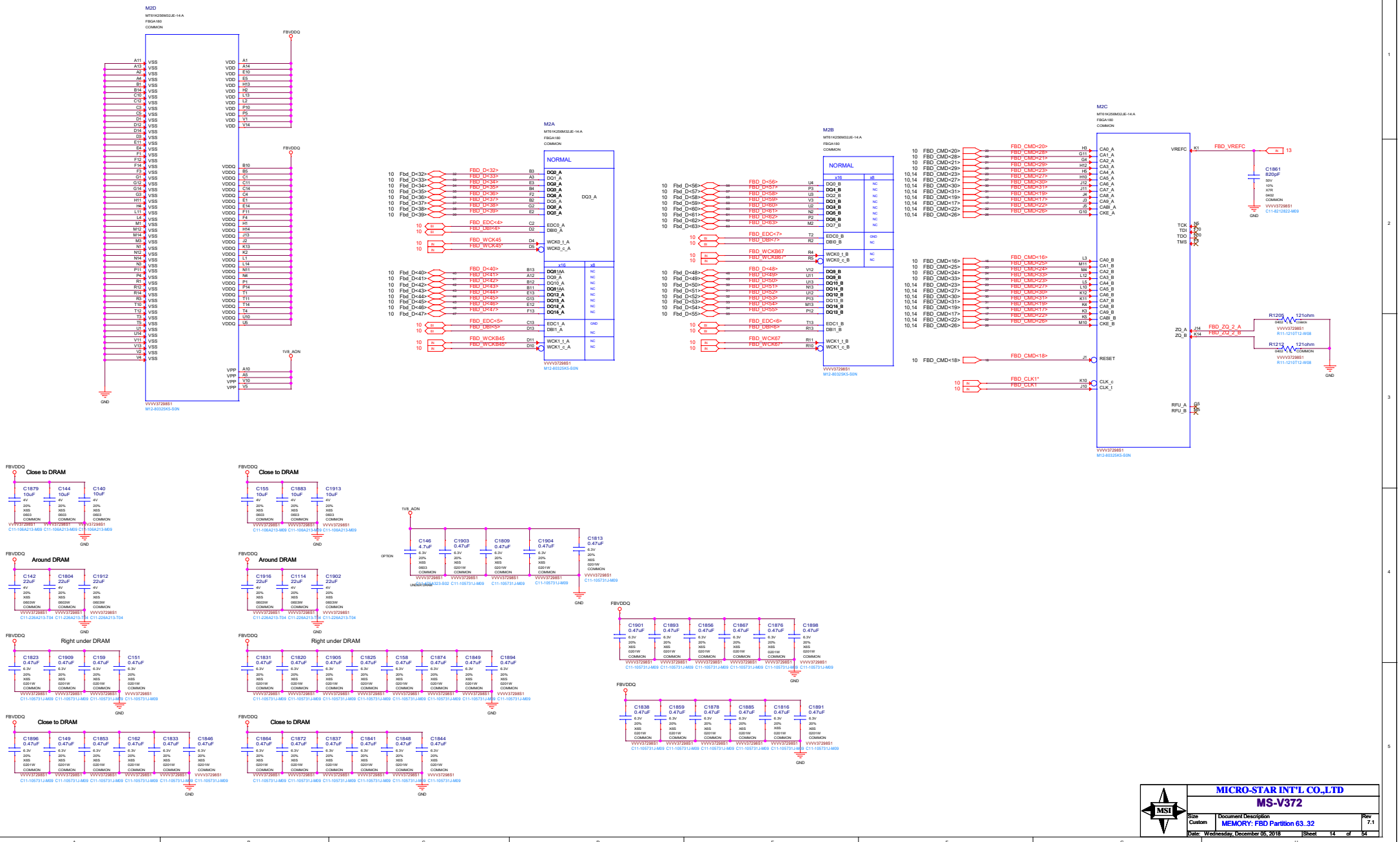

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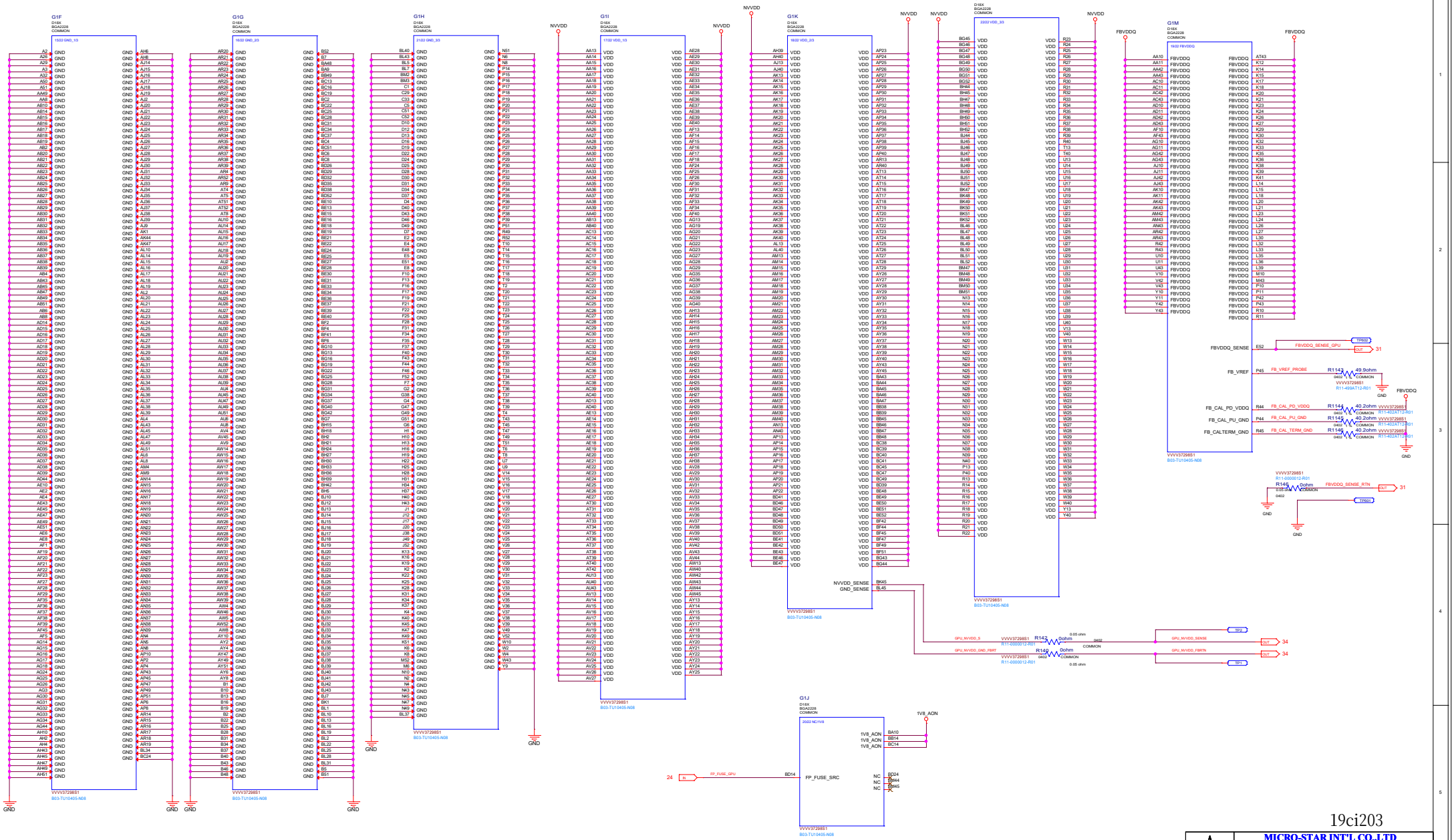

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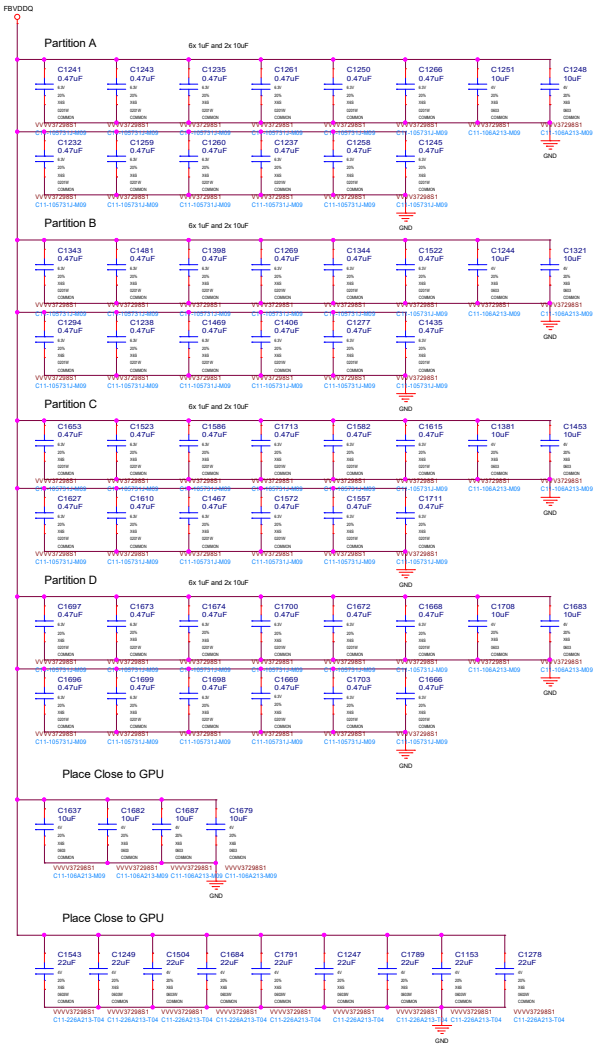
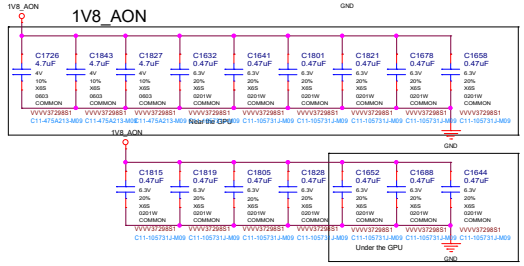
Page16: GPU Decoupling

FBVDDQ

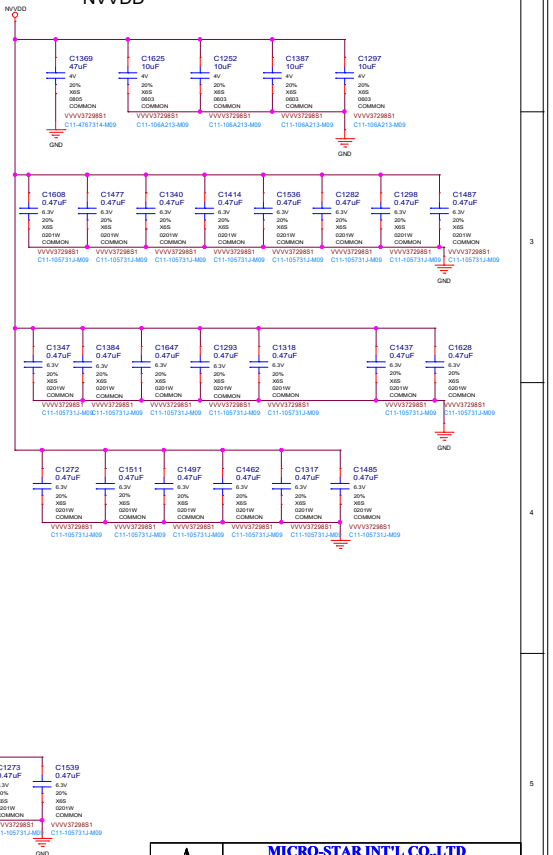


NVVDD

1V8_AON



NVVDD



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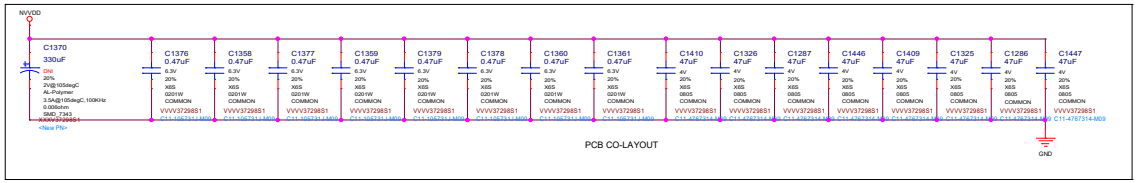

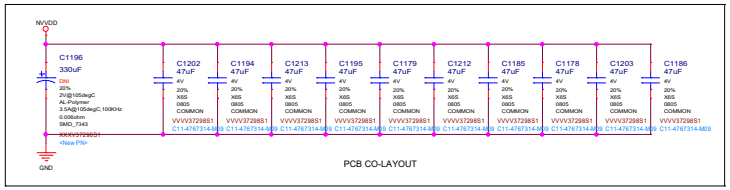

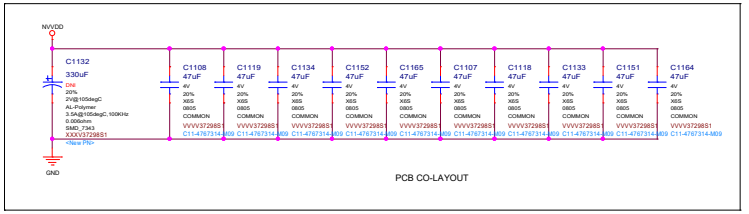

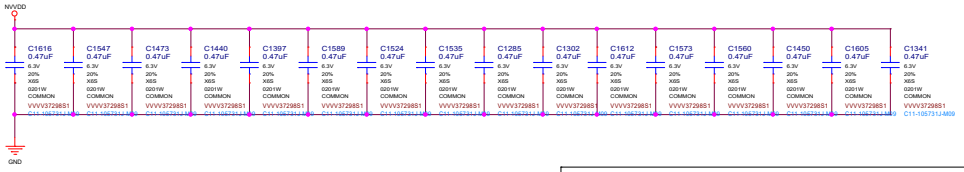

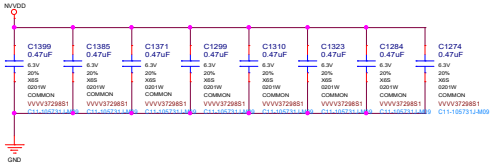

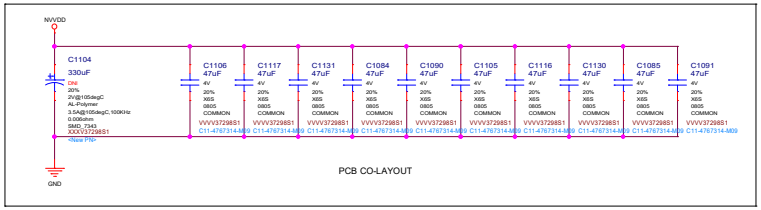

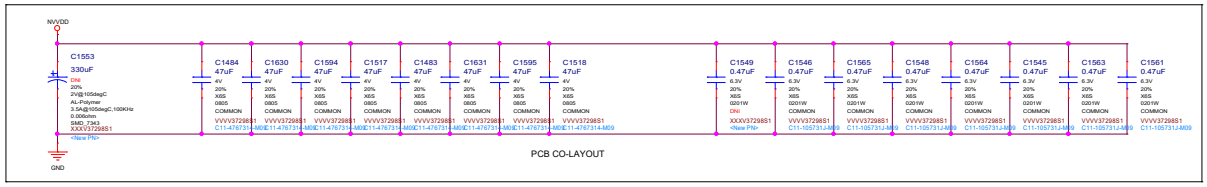

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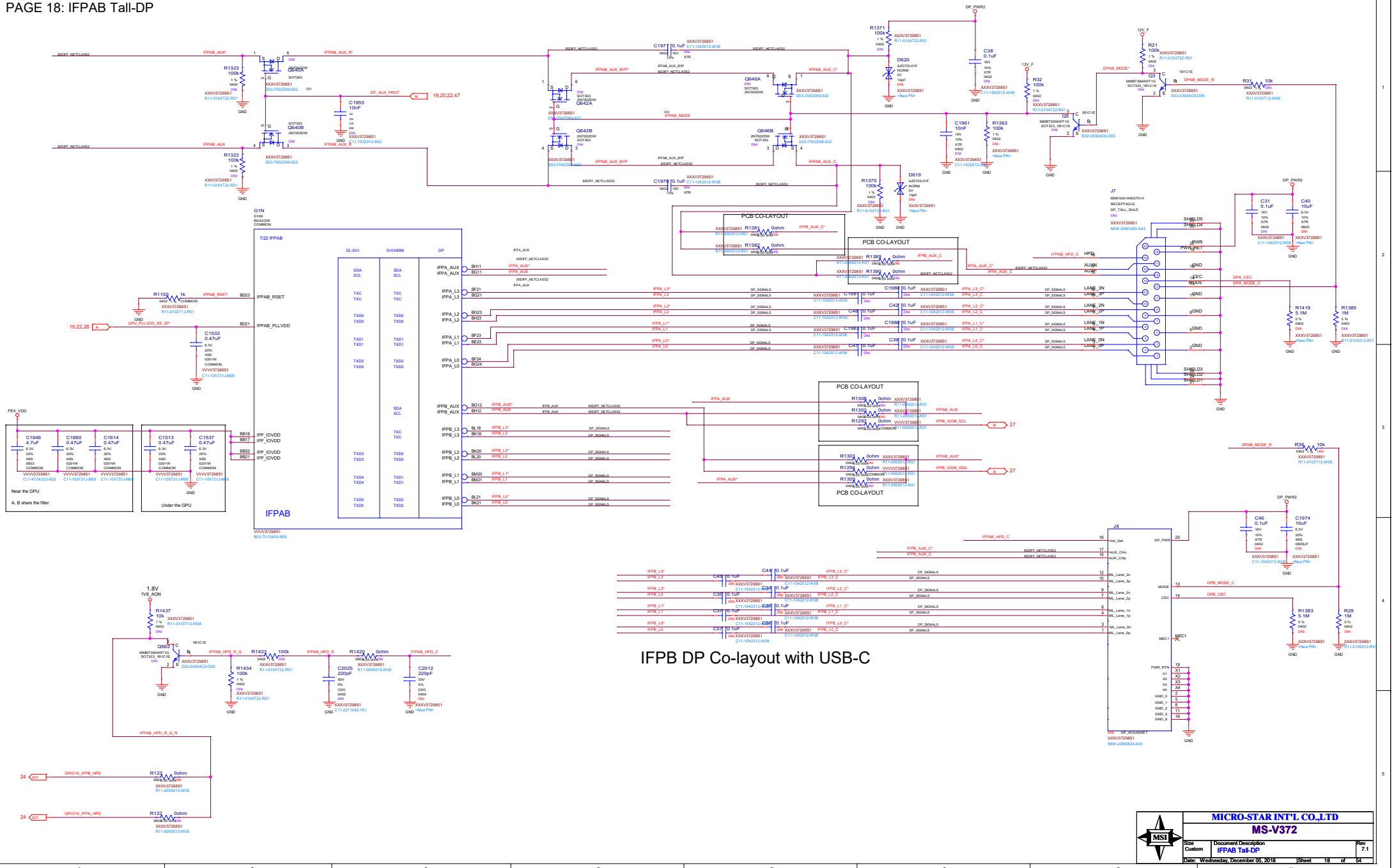
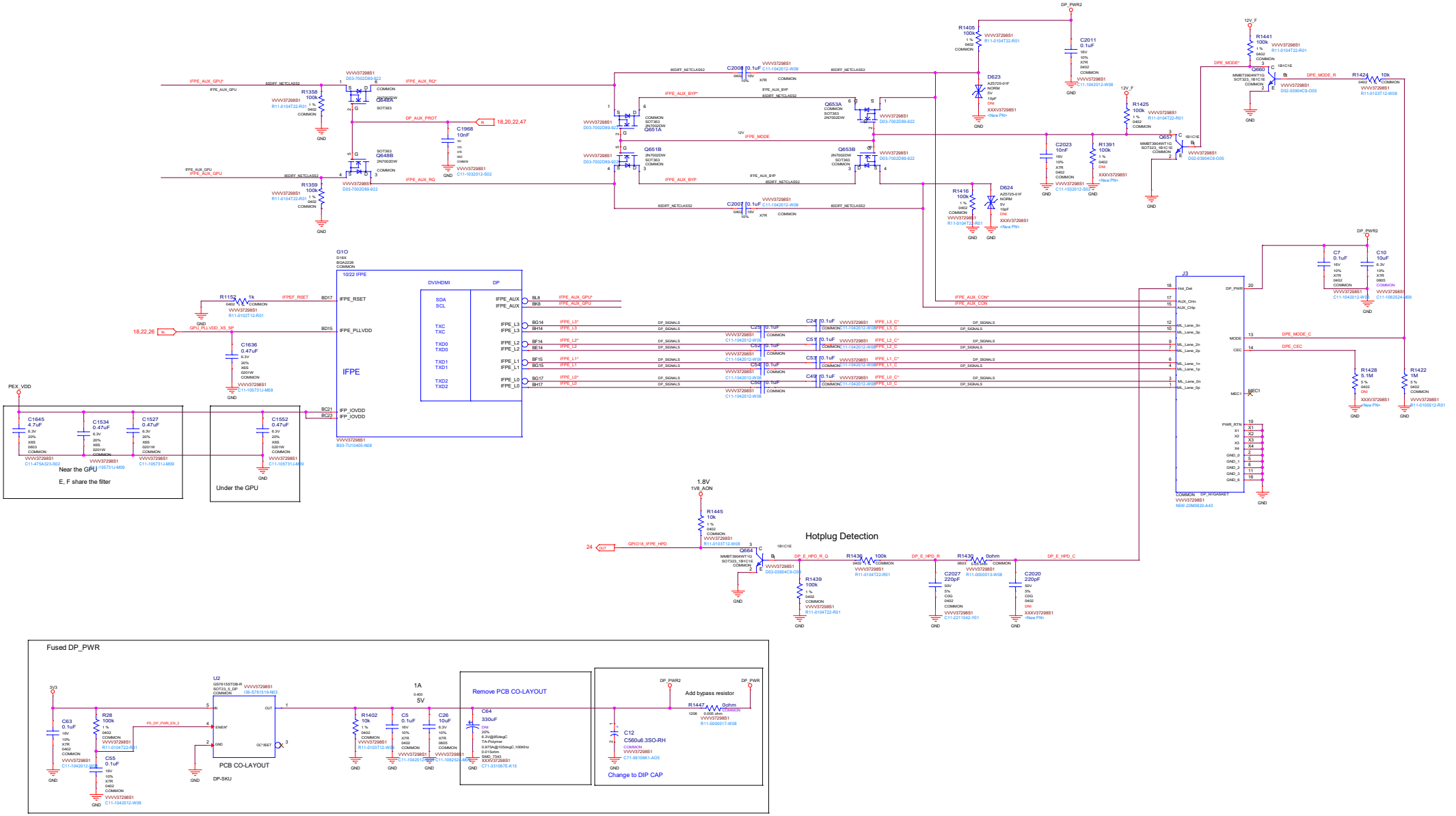
PAGE 18: IFPAB Tall-DP



PAGE 19: IFPE DP



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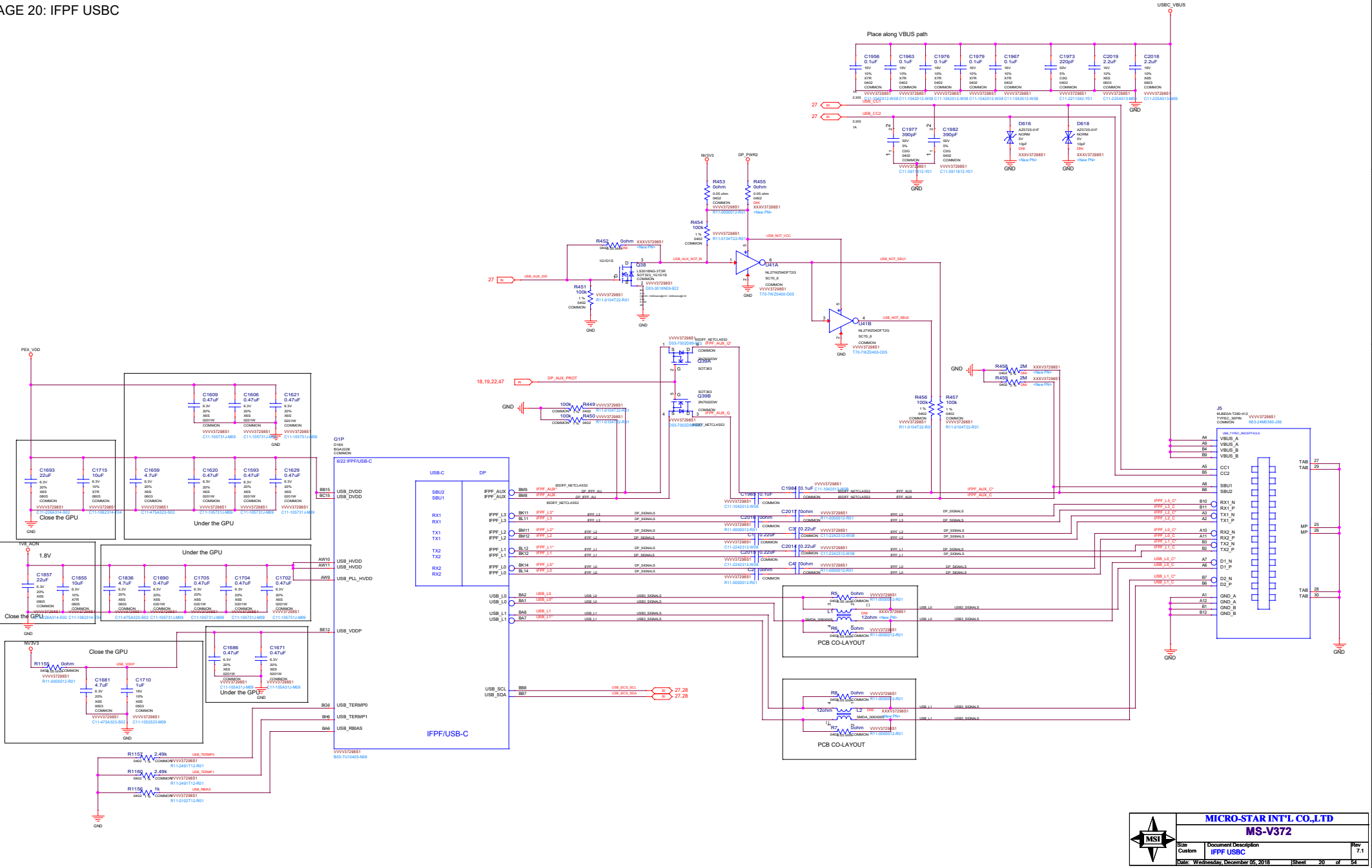
USBC_VBUS
Place along VBUS path
C1956 0.1uF
C1963 0.1uF
C1976 0.1uF
C1979 0.1uF
C1967 0.1uF
C1973 220pF
C2019 2.2uF
C2018 2.2uF
C1977 390pF
C1982 390pF
D616
D618
USB_CC1
USB_CC2
NV3V3
DP_PWR2
R453 0ohm
R455 0ohm
R454 100k
R452 0ohm
R451 100k
Q38
U41A
U41B
USB_AUX_SW
USB_AUX_NOT_IN
USB_NOT_VCC
USB_NOT_SBU1
USB_NOT_SBU2
DP_AUX_PROT
R449 100k
R450 100k
Q39A
Q39B
R456 100k
R457 100k
R458 2M
R459 2M
J5
MUSB3A-T280-412
TYPEC_30PIN
PEX_VDD
C1609 0.47uF
C1606 0.47uF
C1621 0.47uF
C1693 22uF
C1715 10uF
C1659 4.7uF
C1620 0.47uF
C1593 0.47uF
C1629 0.47uF
Close the GPU
Under the GPU
1V8_AON
1.8V
C1857 22uF
C1855 10uF
C1836 4.7uF
C1690 0.47uF
C1705 0.47uF
C1704 0.47uF
C1702 0.47uF
NV3V3
R1155 0ohm
C1681 4.7uF
C1710 1uF
C1686 0.47uF
C1671 0.47uF
R1157 2.49k
R1160 2.49k
R1156 1k
G1P
6/22 IFPF/USB-C
USB-C
DP
IFPF/USB-C
USB_DVDD
USB_HVDD
USB_PLL_HVDD
USB_VDDP
USB_TERMP0
USB_TERMP1
USB_RBIAS
USB_SCL
USB_SDA
IFPF_AUX
IFPF_L3
IFPF_L2
IFPF_L1
IFPF_L0
USB_L0
USB_L1
PCB CO-LAYOUT
R5 0ohm
L1 120ohm
R6 0ohm
R8 0ohm
L2 120ohm
R7 0ohm
GND
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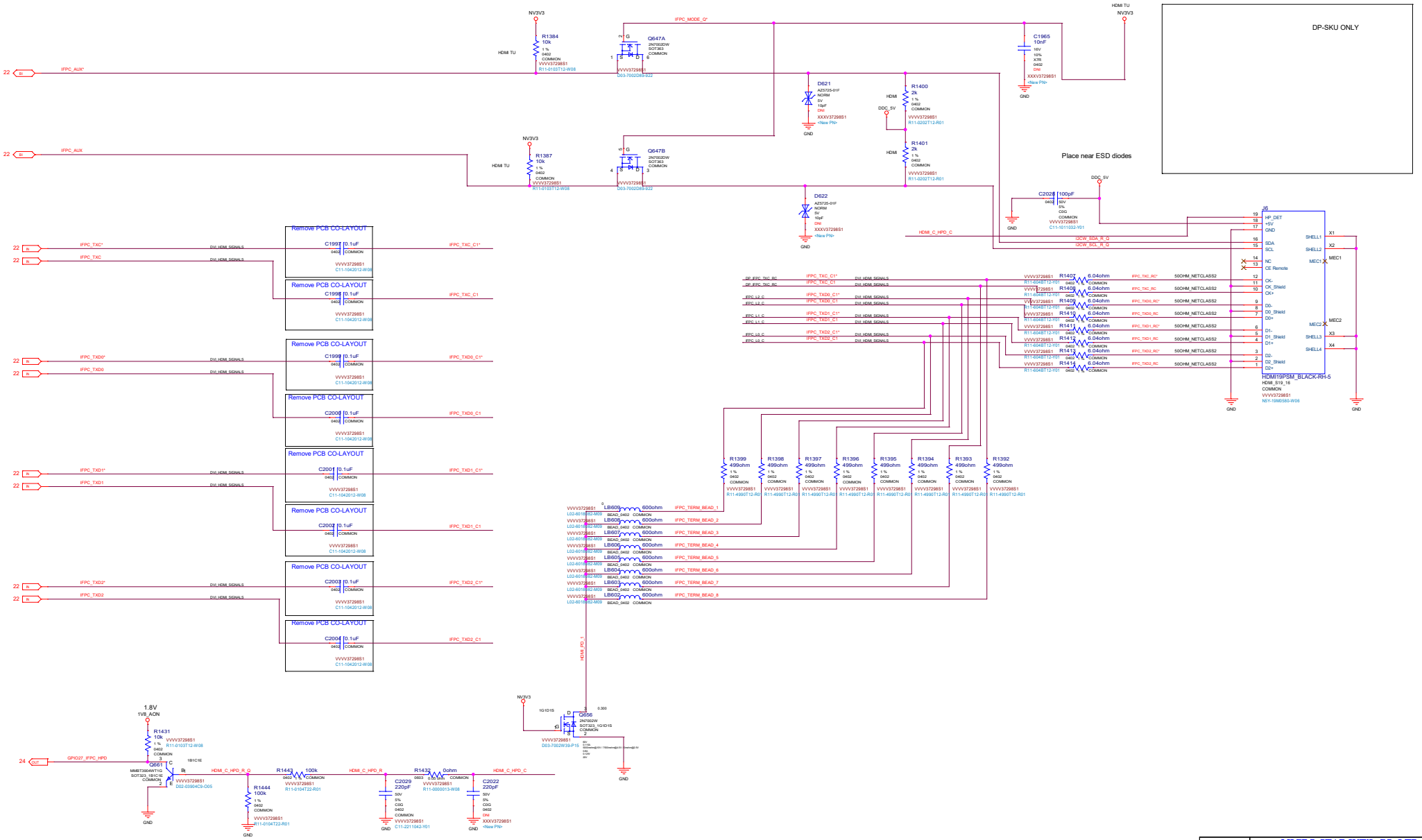
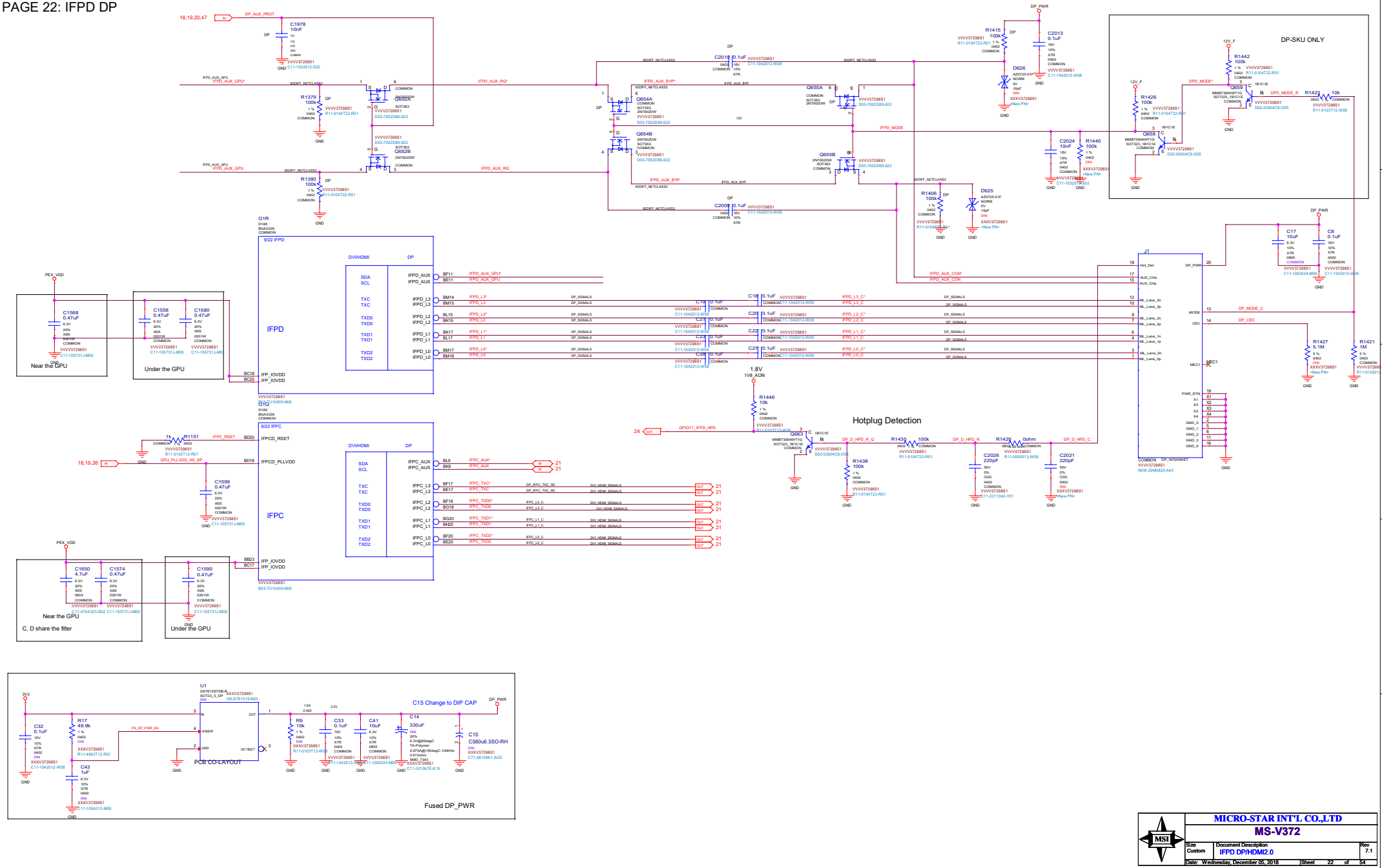
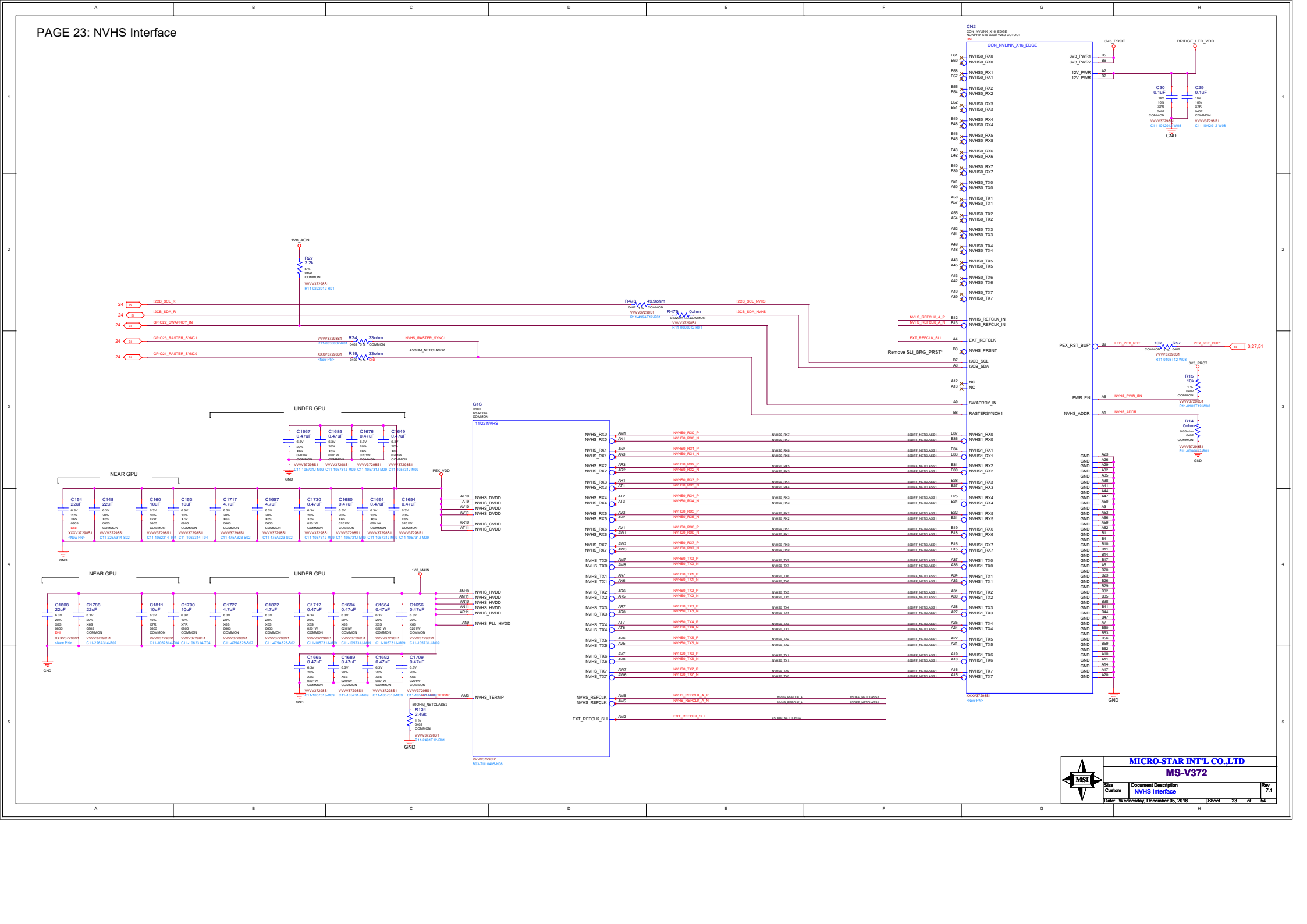
PAGE 21:IFPC HDMI 2.0



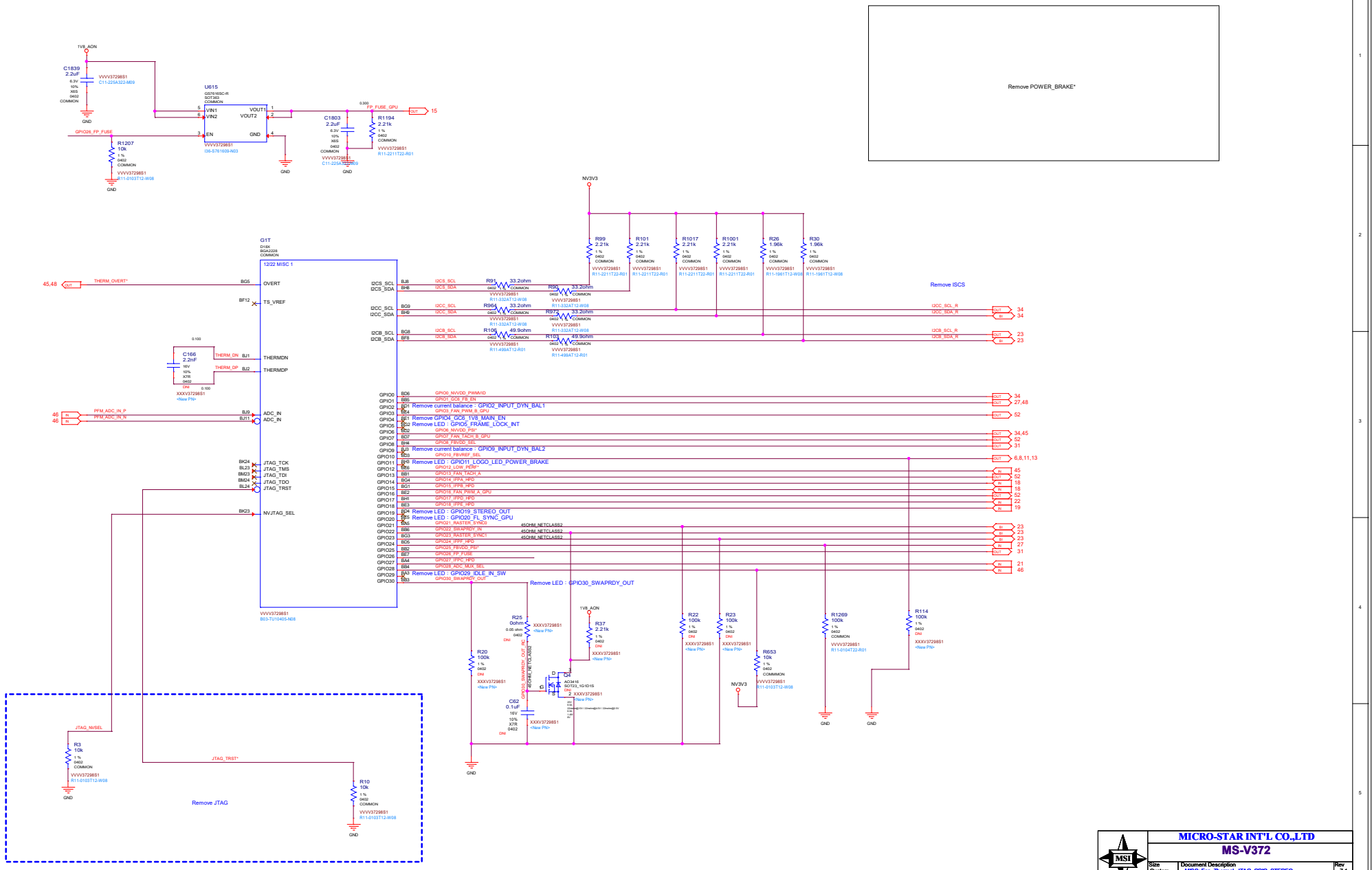
PAGE 22: IFPD DP



PAGE 23: NVHS Interface



PAGE 24: MISC: Fan, Thermal, JTAG, GPIO, STEREO



PAGE 25: MISC: ROM, Straps

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG TBD
L	L	H	00001	RAMCFG TBD
L	H	L	00010	RAMCFG TBD
L	H	H	00011	RAMCFG TBD
H	H	L	00110	RAMCFG TBD
H	H	H	00111	RAMCFG TBD

DEFAULT

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE
L	L	L	XXX1	FS_OVERT ENABLE
L	L	M	XXX0	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

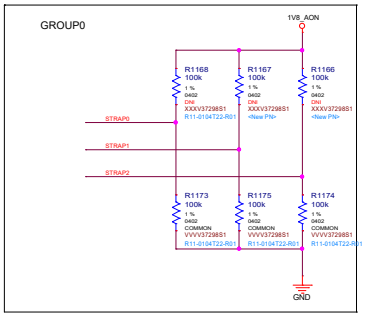
Default

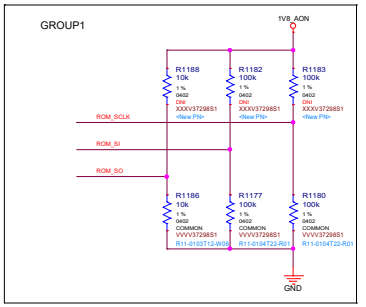
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

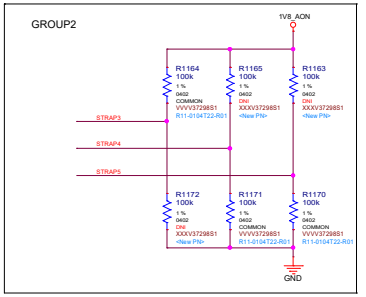
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

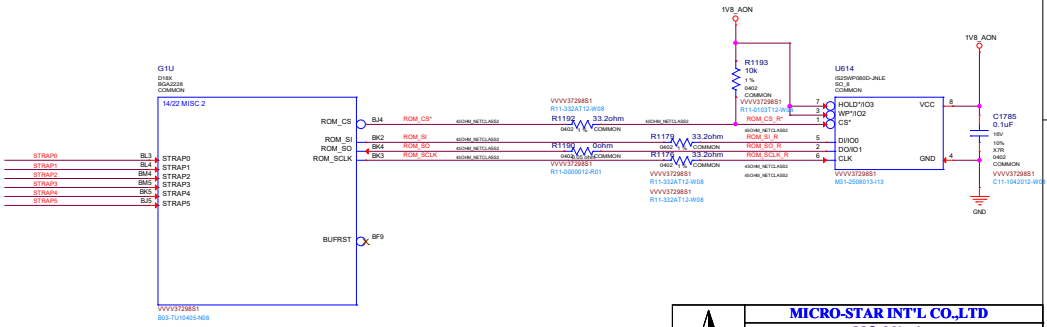
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE









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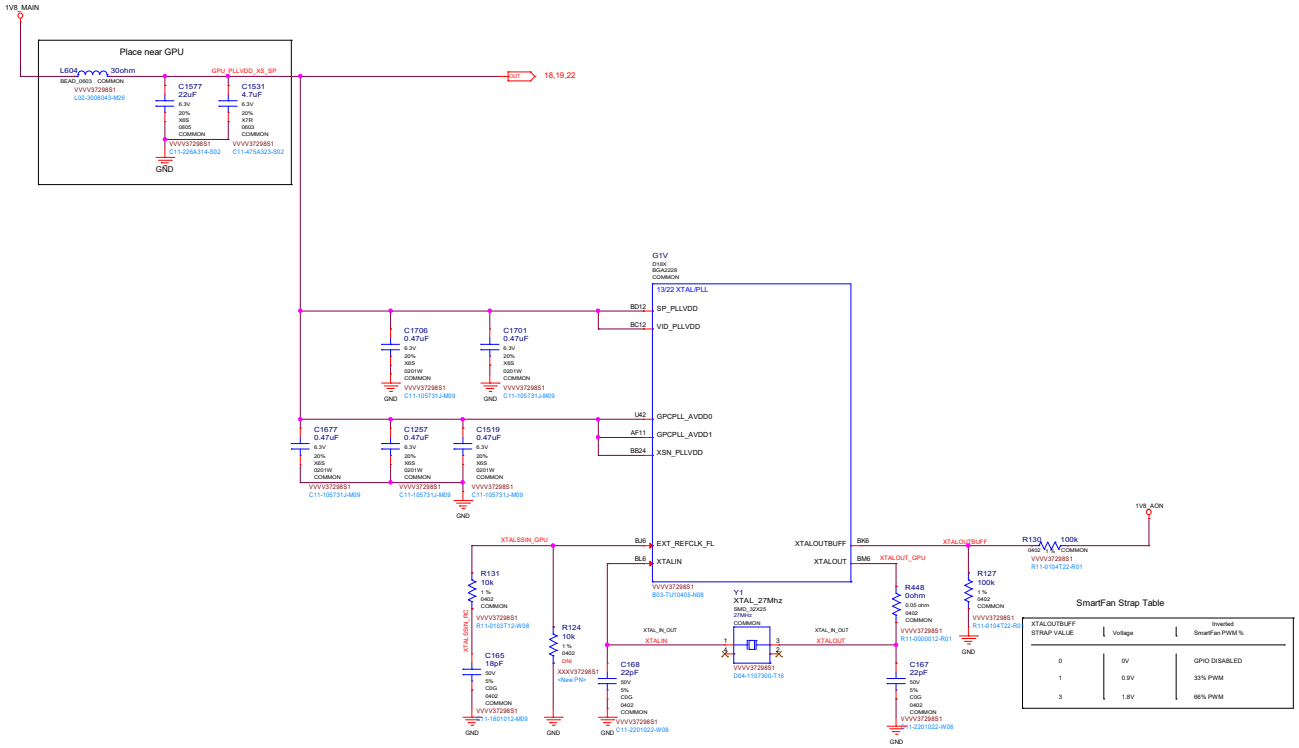
PAGE 26: MISC: XTAL. PLL



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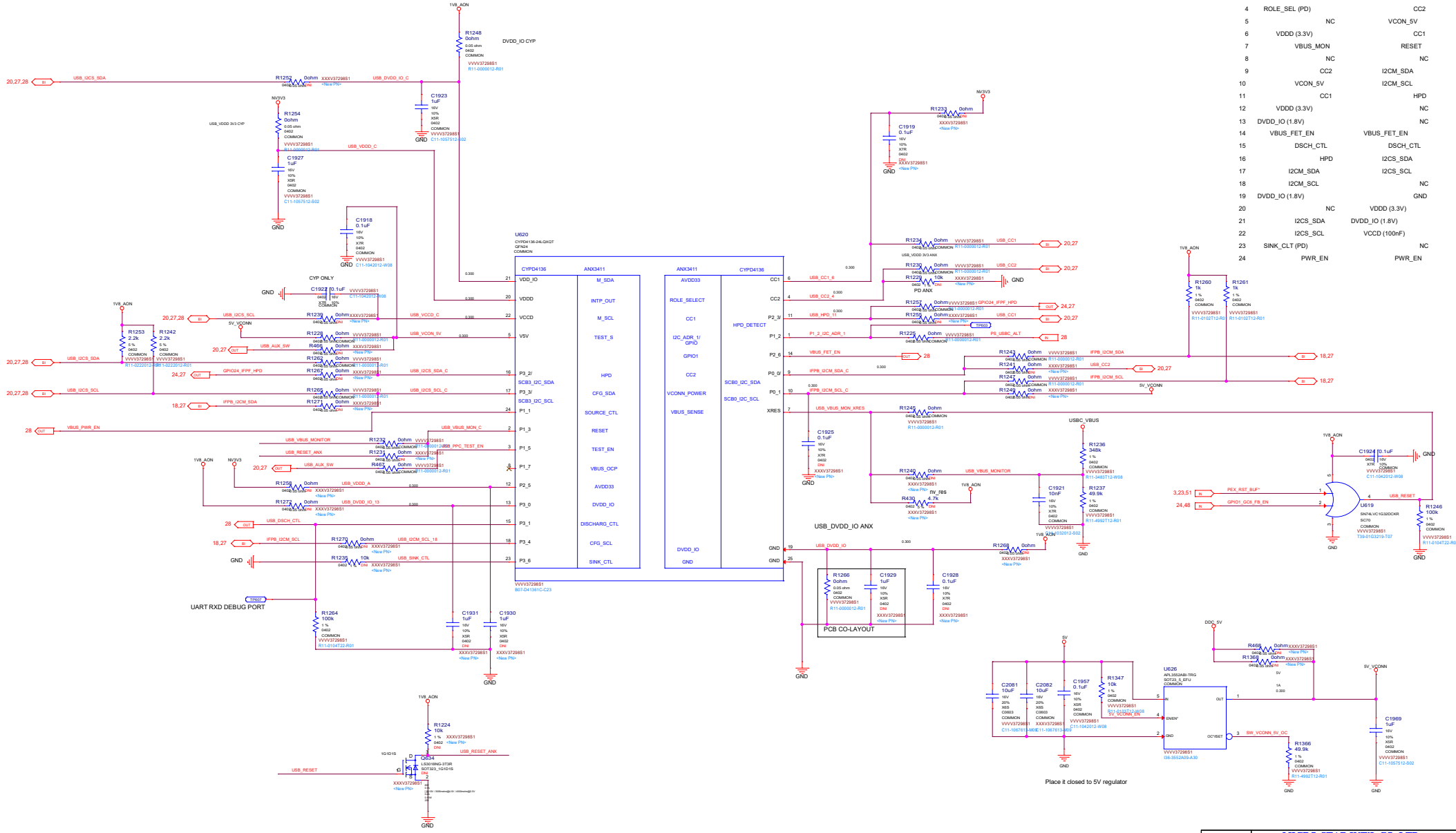
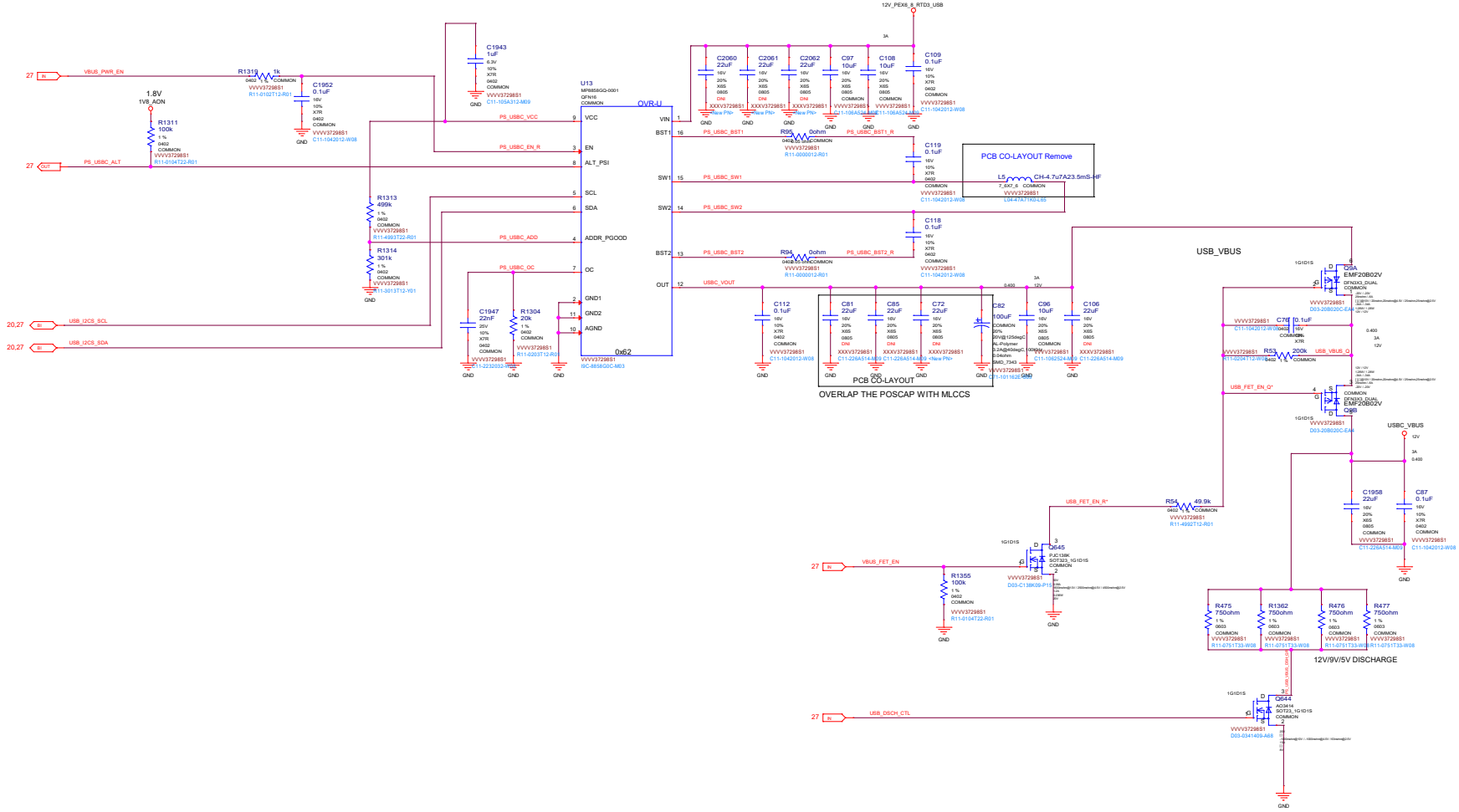
PAGE 27: MISC: USB PPC



PAGE 28: PS: USB VR



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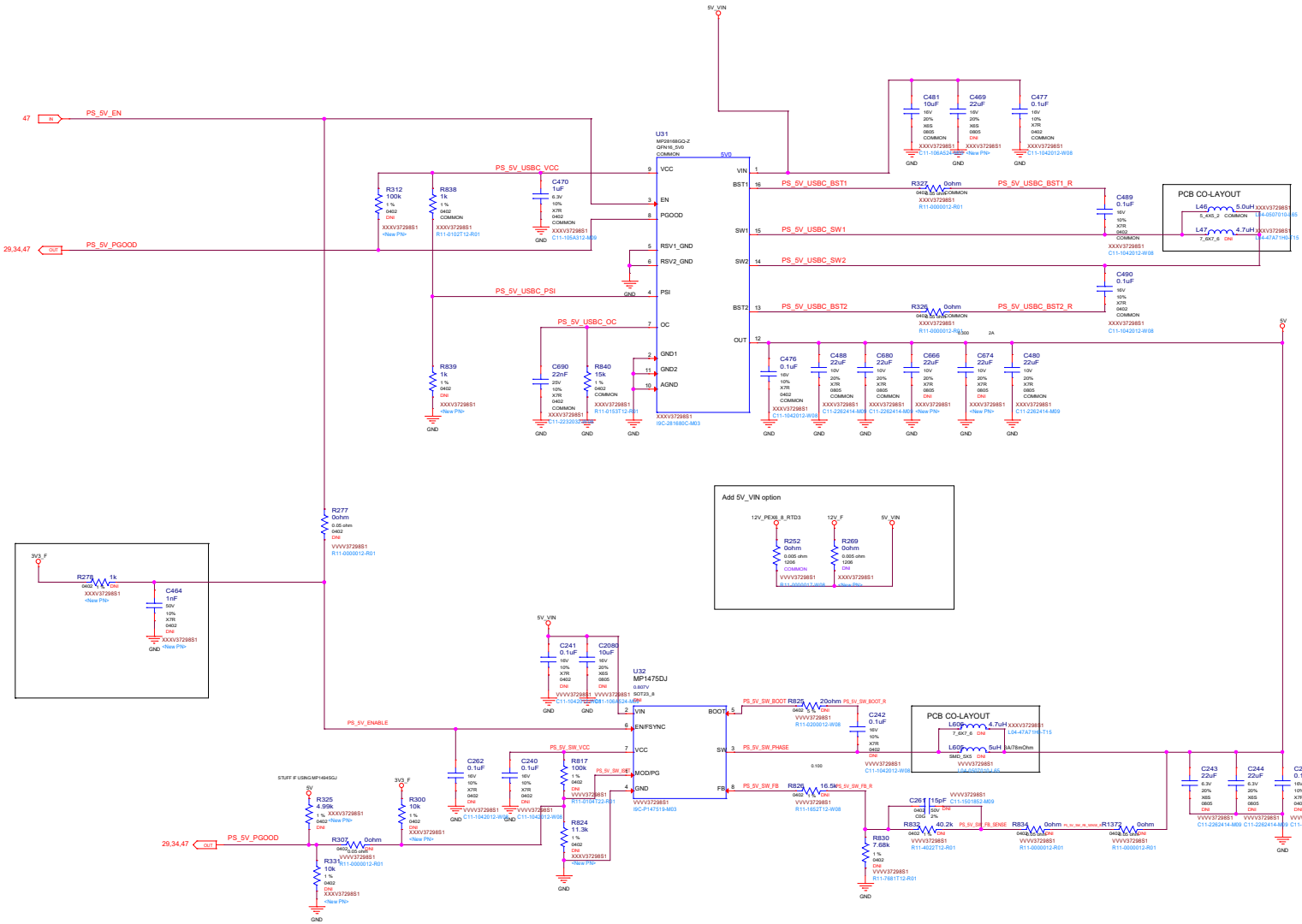
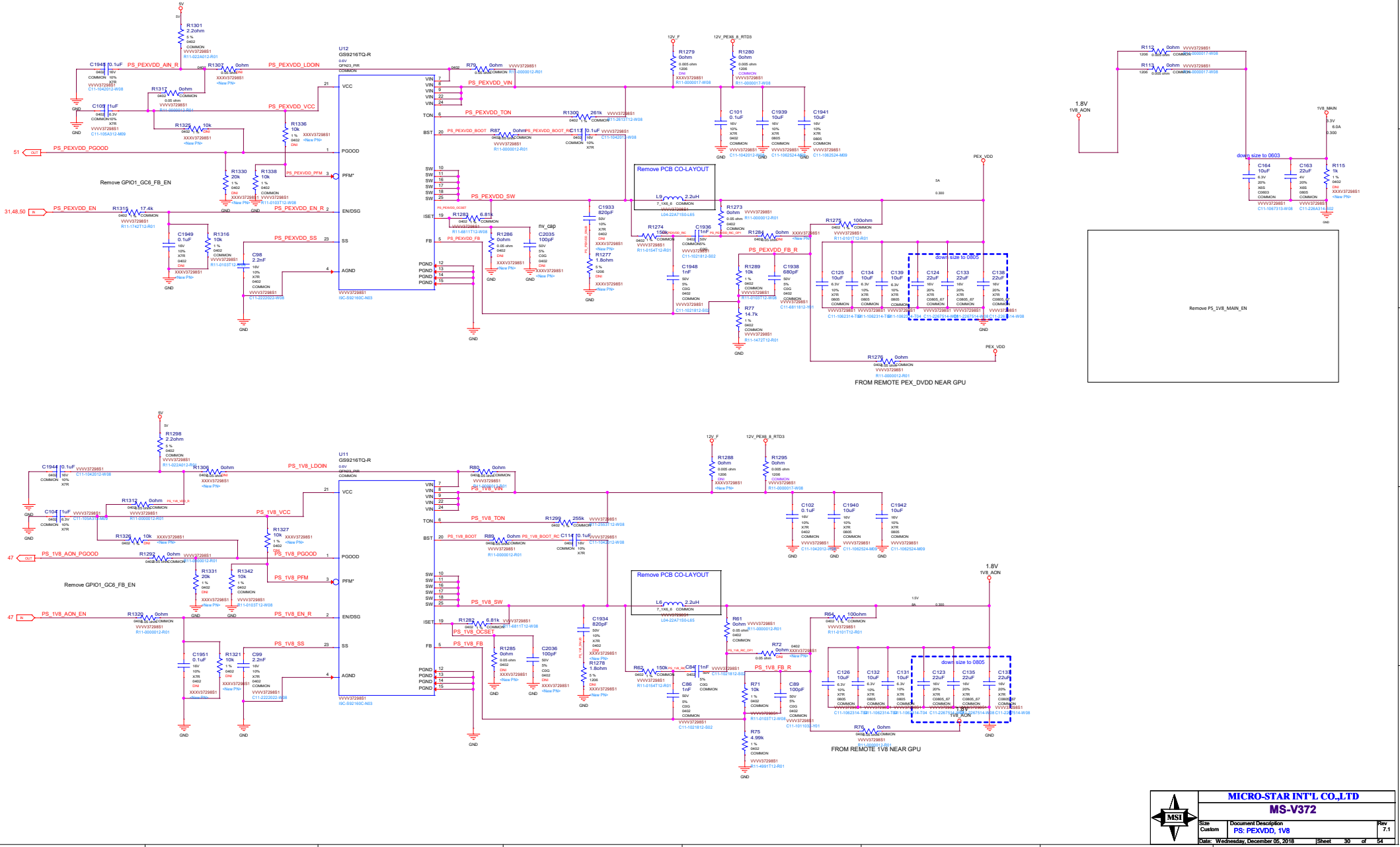
PAGE 29: PS: 5V, 5V_BACKUP



PAGE 30: PS: PEXVDD, 1V8



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Size: Custom	Document Description: PS: PEXVDD, 1V8		Rev: 7.1
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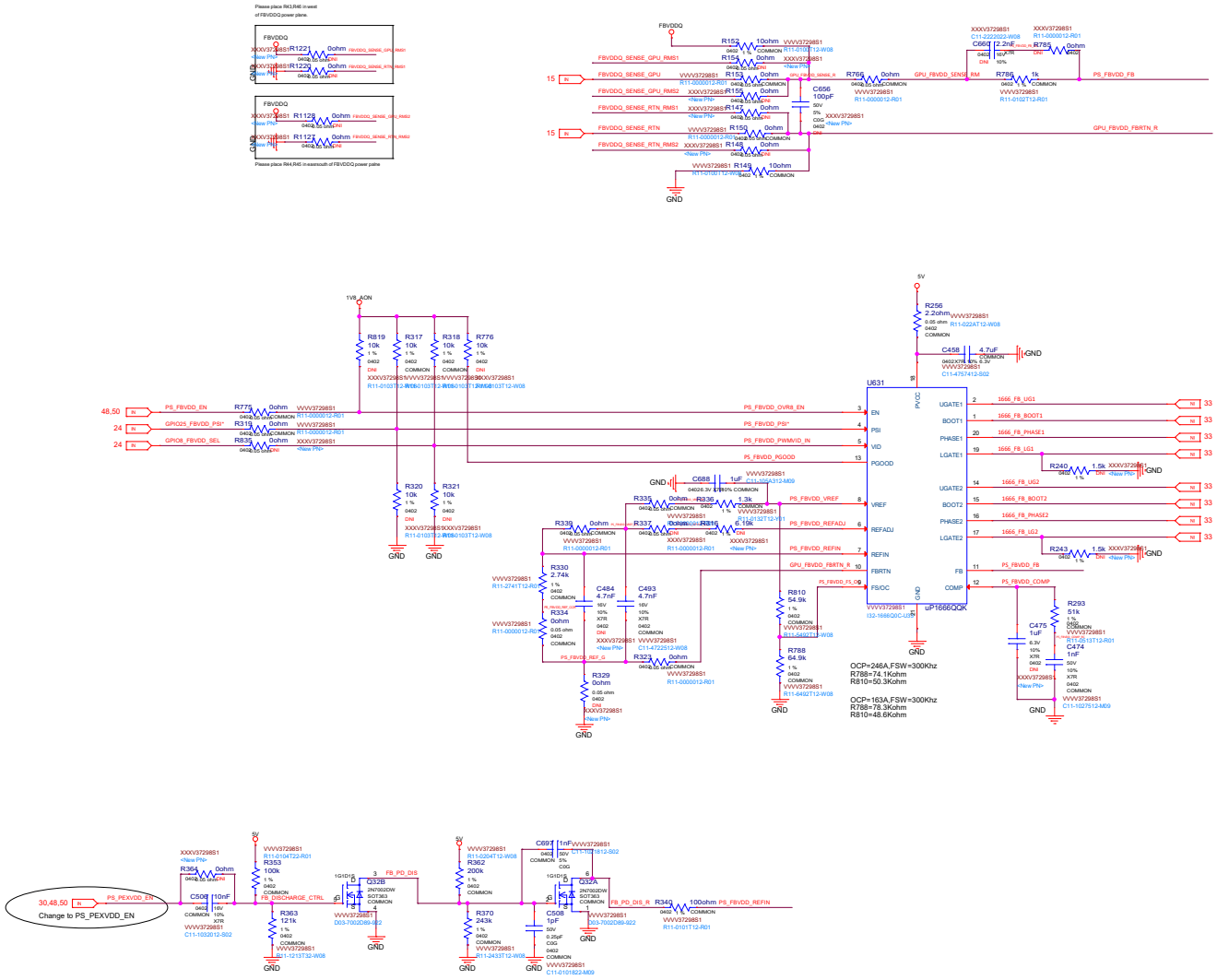
PAGE 31: PS: FBVDD Controller



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PAGE 32: PS: FBVDD Controller OVR3

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Size: Custom	Document Description: PS: FBVDD Controller OVR3 (X)
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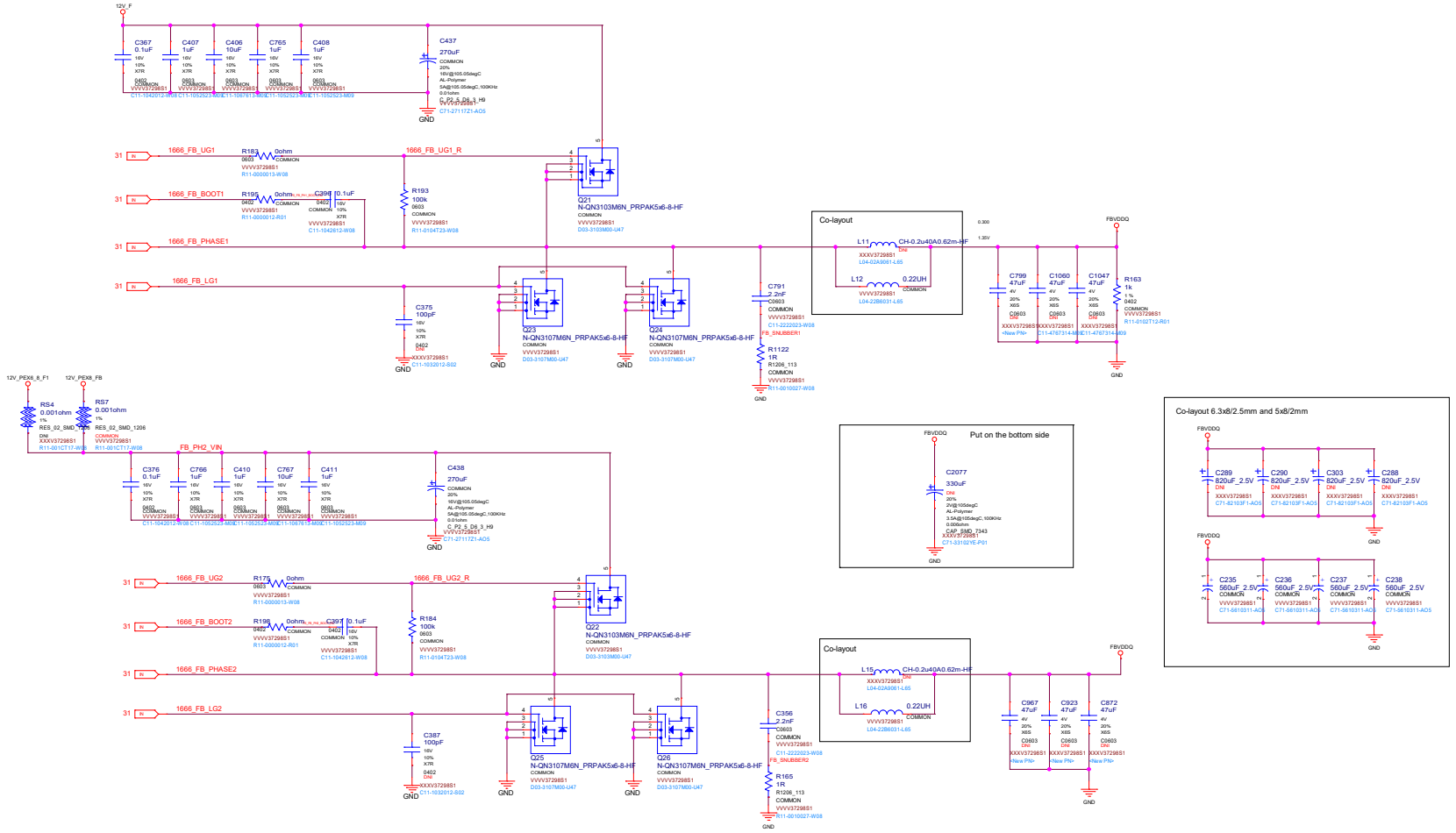
PAGE 33: PS: FBVDD Phase 1, 2



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Page34: PS: NVVDD Controller

EN Type	R3
Open Drain	10k
Push Pull	NS

PSI	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count

PWMVID	Vout
High	VID in 24h
Hi-Z	VID in 21h
Low	VID in 1Fh

NTC1 close to FBVDD MOS

NTC2 close to NVVDD MOS (U51/U52)
NTC3 close to NVVDD MOS (U53/U54)
NTC4 close to NVVDD MOS (U55/U56)

MP2886A

	+NVVDD
TDC	200A
IccMax	330A
Vboot	0.8V
Load Line	0mohm

PMBus Address	Setting Point(V)	R_{ADDR1} (kΩ) 1%	R_{ADDR0} (kΩ) 1%
20h	0	-	0
21h	0.031	3.32	0.059
22h	0.057	3.32	0.11
23h	0.084	3.32	0.162
24h	0.116	3.32	0.226
25h	0.156	3.32	0.316
26h	0.205	3.32	0.43
27h	0.266	3.32	0.576
28h	0.340	3.32	0.768
29h	0.430	3.32	1.05
2Ah	0.540	3.32	1.43
2Bh	0.675	3.32	2
2Ch	0.844	3.32	2.94
2Dh	1.048	3.32	4.64
2Eh	1.301	3.32	8.66
2Fh	1.500	3.32	16.5

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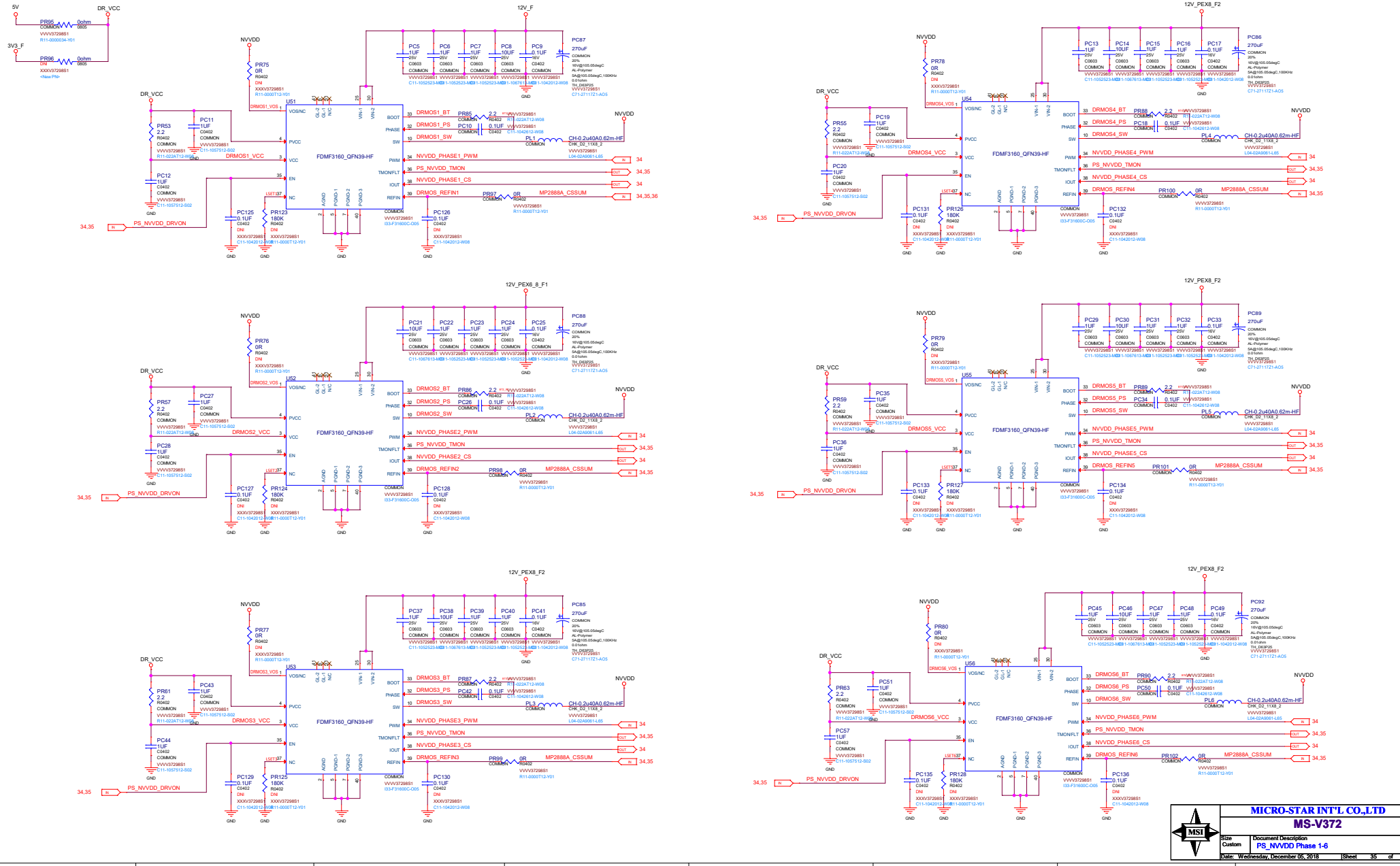
Page35: PS: NVVDD Phase 1-6



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MS-V372			
Size: Custom	Document Description: PS_NVVDD Phase 1-6		Rev: 7.1
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Page36: PS: NVVDD Phase (X)

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Size: Custom	Document Description: PS: NVVDD Phase(X)
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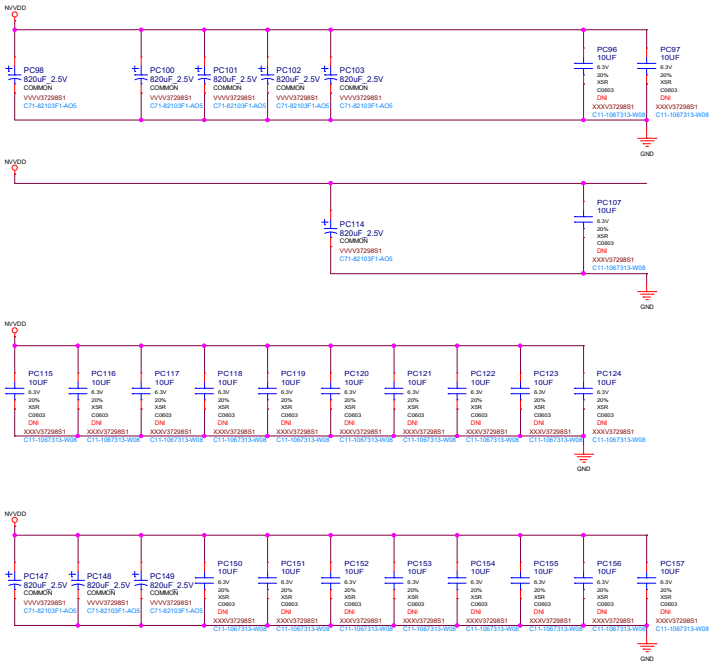
NVVDD Output CAP



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Size: Custom	Document Description: PS: NVVDD Output CAP	Rev: 7.1
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PAGE 38: PS:NVVDD (X)

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Custom	PS:NVVDD (X)	7.1

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PAGE 39: PS: INPUT SWITCH RTD3

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MS-V372							
Size: Custom	Document Description: PS: INPUT SWITCH RTD3						Rev: 7.1
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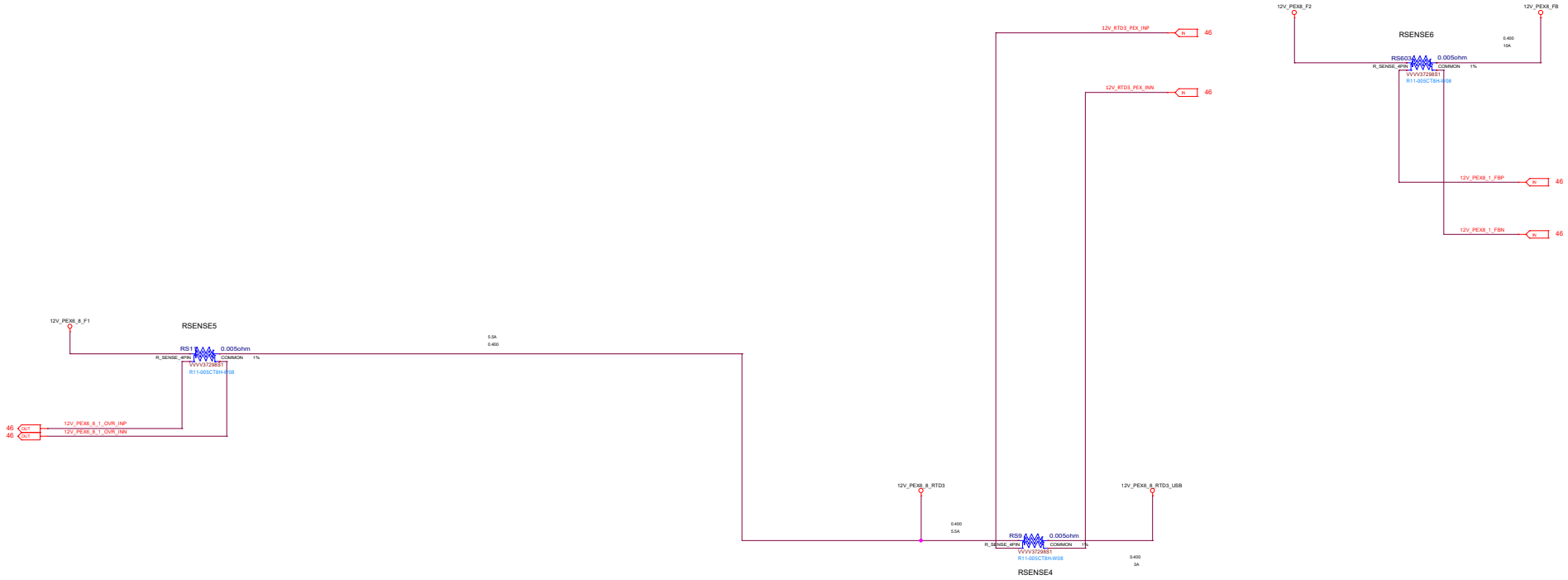
PAGE 40: PS: INPUT SWITCH RTD3 USB



MICRO-STAR INT'L CO.,LTD		
MS-V372		
Size: Custom	Document Description: PS: INPUT SWITCH RTD3 USB	Rev: 7.1
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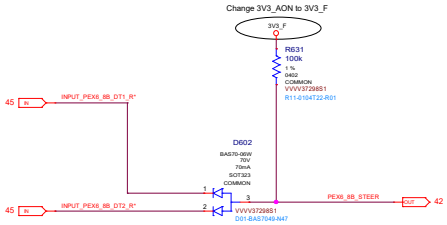
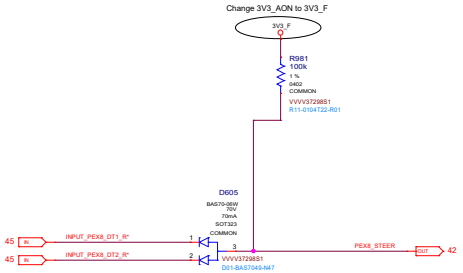
PAGE 41: PS: INPUT SWITCH Rail Balance



Remove 3V3_F byass ro 3V3_AON



MICRO-STAR INT'L CO.,LTD

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Size	Document Description	Rev
Custom	PS: INPUT SWITCH Rail Balance	7.1

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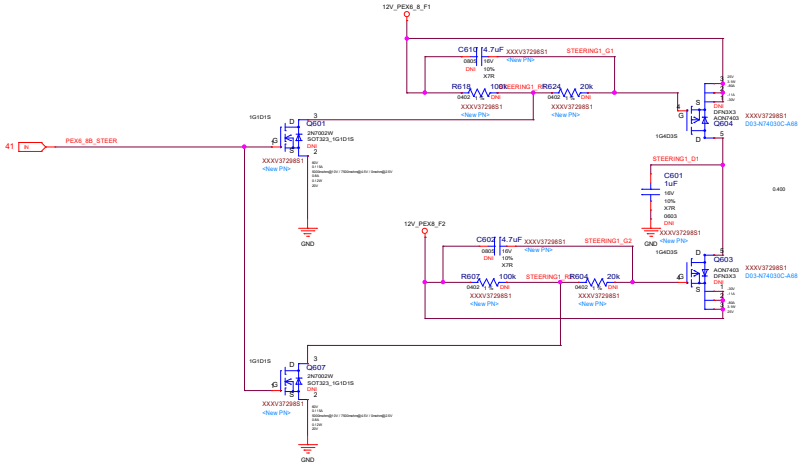
PAGE 42: PS: 12V CURRENT STEERING

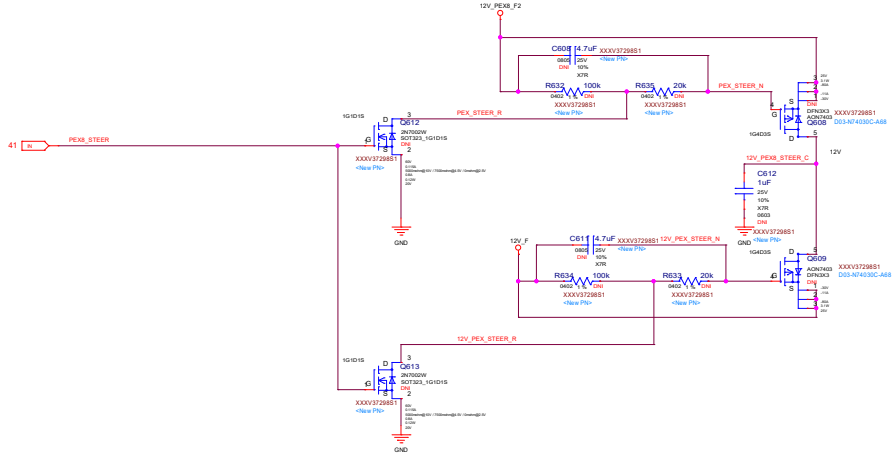
12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



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Size: Custom	Document Description: PS: 12V CURRENT STEERING	Rev: 7.1
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PAGE 43: PS: VR THERMAL PROTECTION

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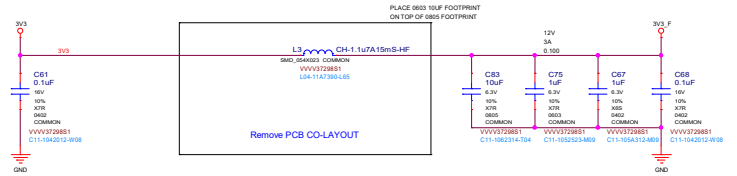
PAGE 44: PS: Inputs, Filtering, and Monitoring

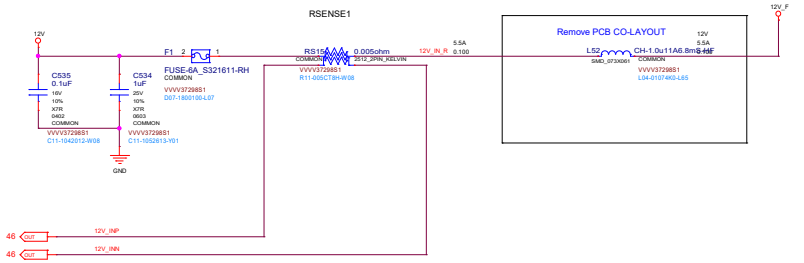
Remove INA3221

Remove 3V3_AUX_FUSE

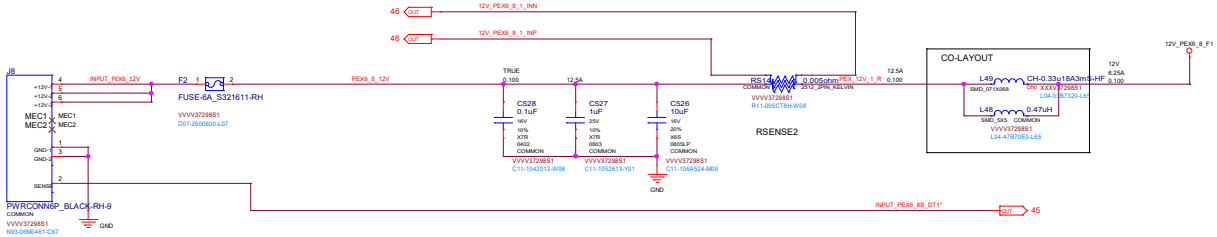
PEX 3V3 INPUT - 10W



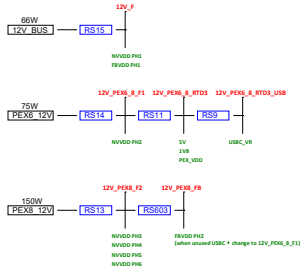
PEX_12V INPUT - 66W



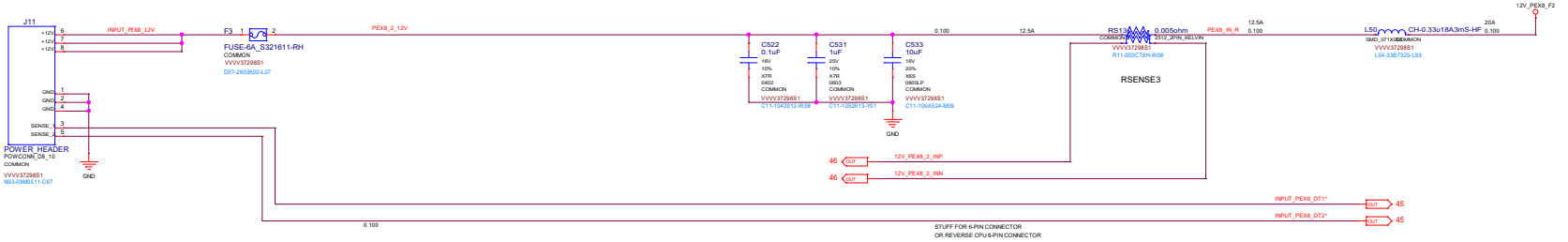
PEX6 INPUT 1 - 2x3 PCIE CON 75W



Power Topology



PEX8 INPUT 2 - 2x4 PCIE CON 150W



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Size: Custom	Document Description: PS: Inputs, Filtering, and Monitoring	Rev: 7.1
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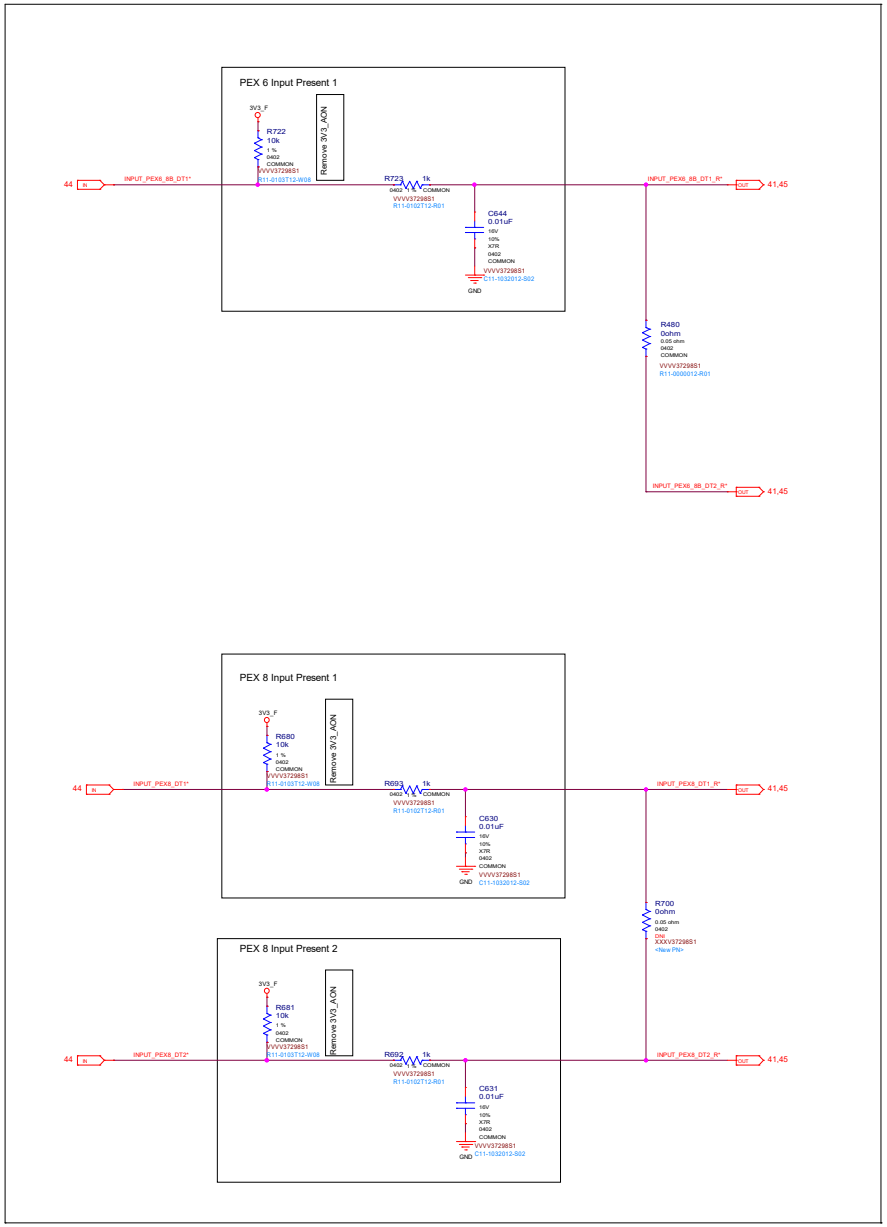
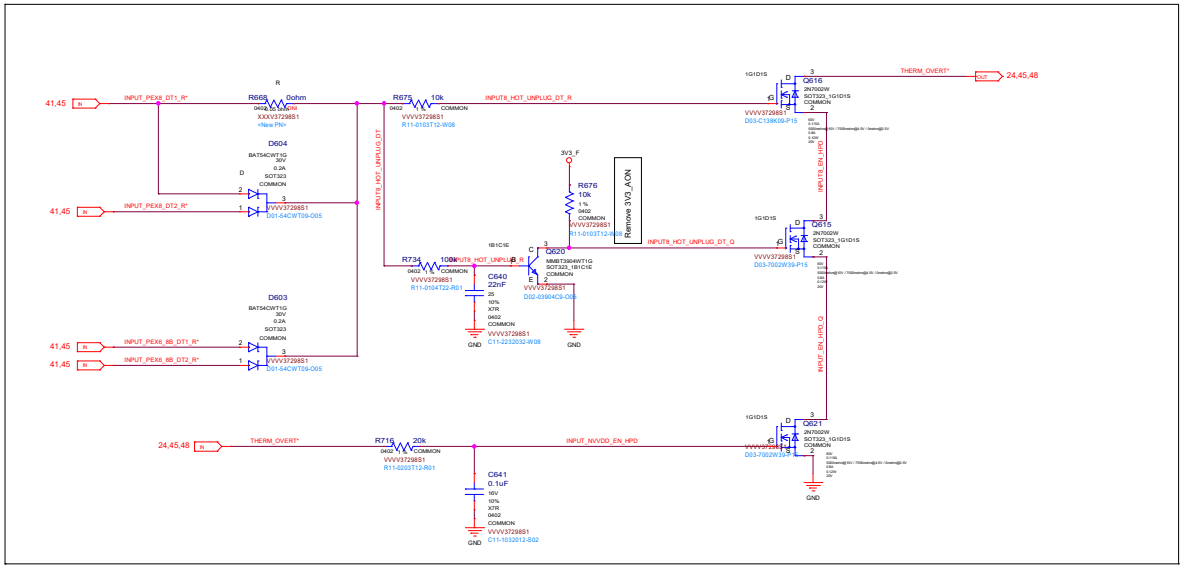
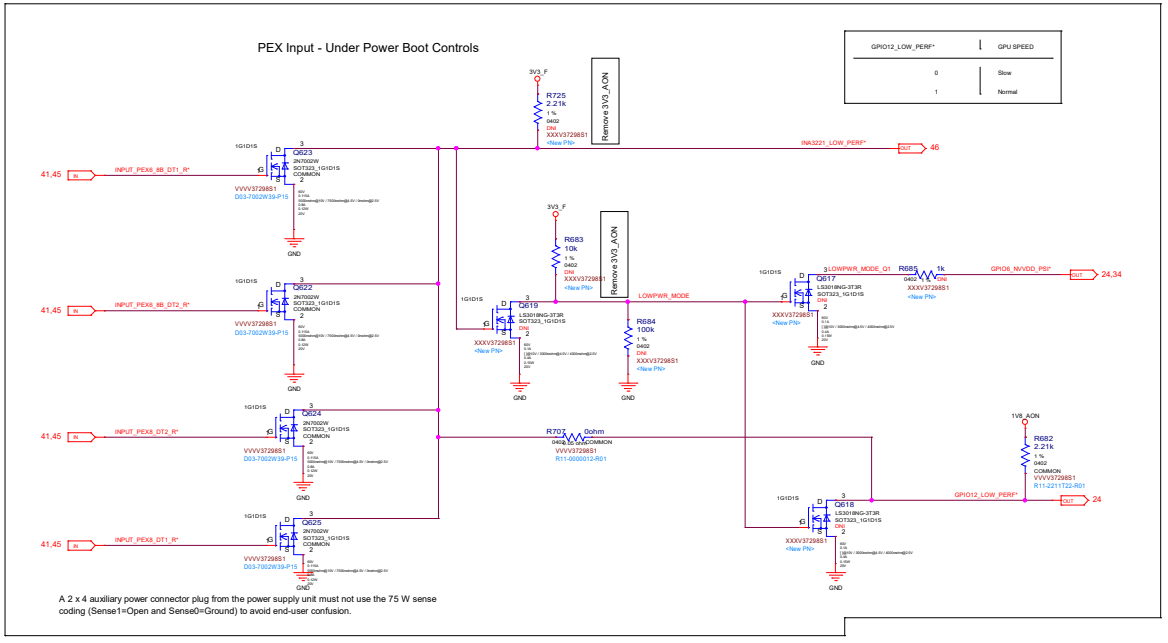
PAGE 45: PS: Current Steering, Hot Unplug Detect







A 2 x 4 auxiliary power connector plug from the power supply unit must not use the 75 W sense coding (Sense1=Open and Sense0=Ground) to avoid end-user confusion.

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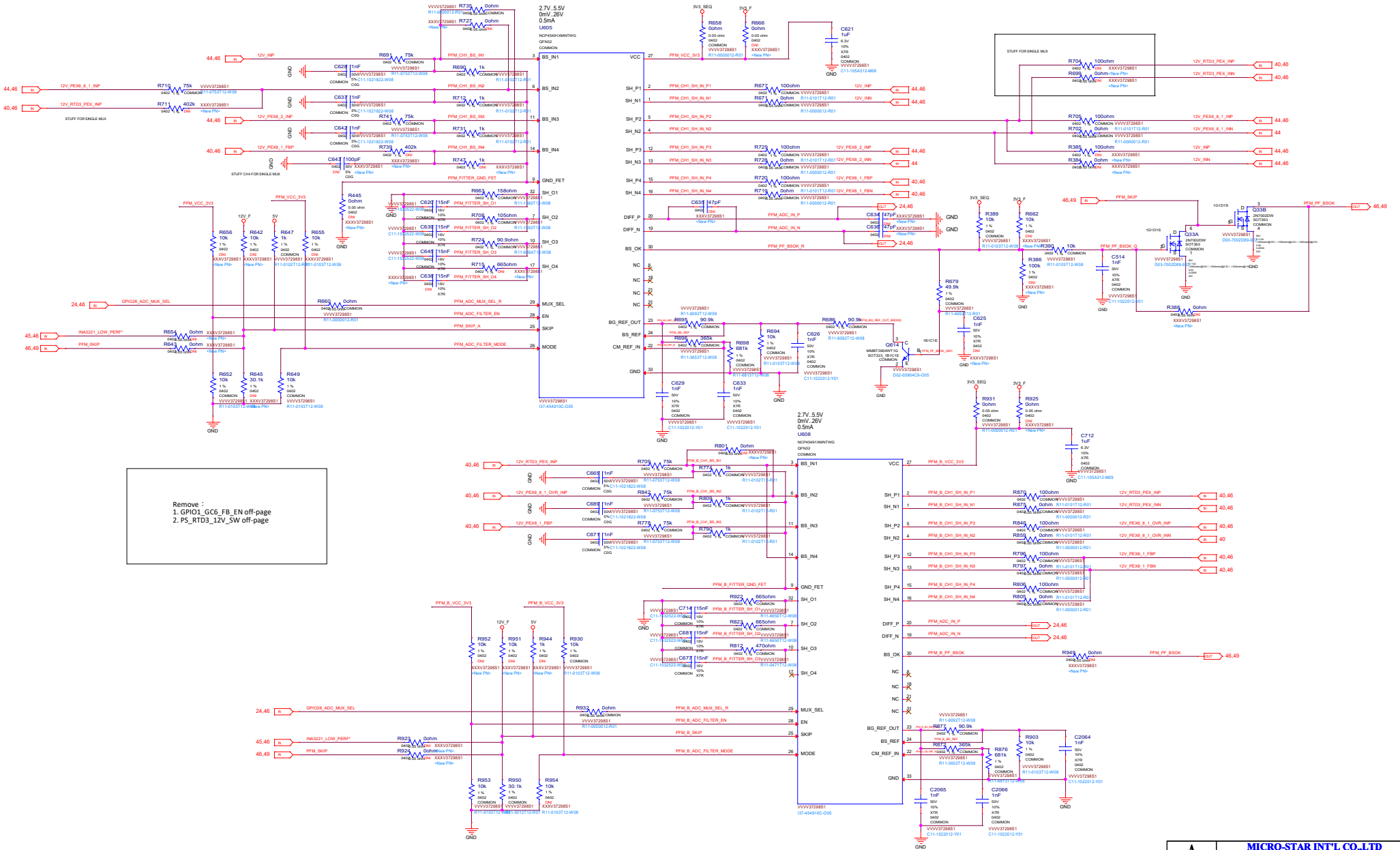
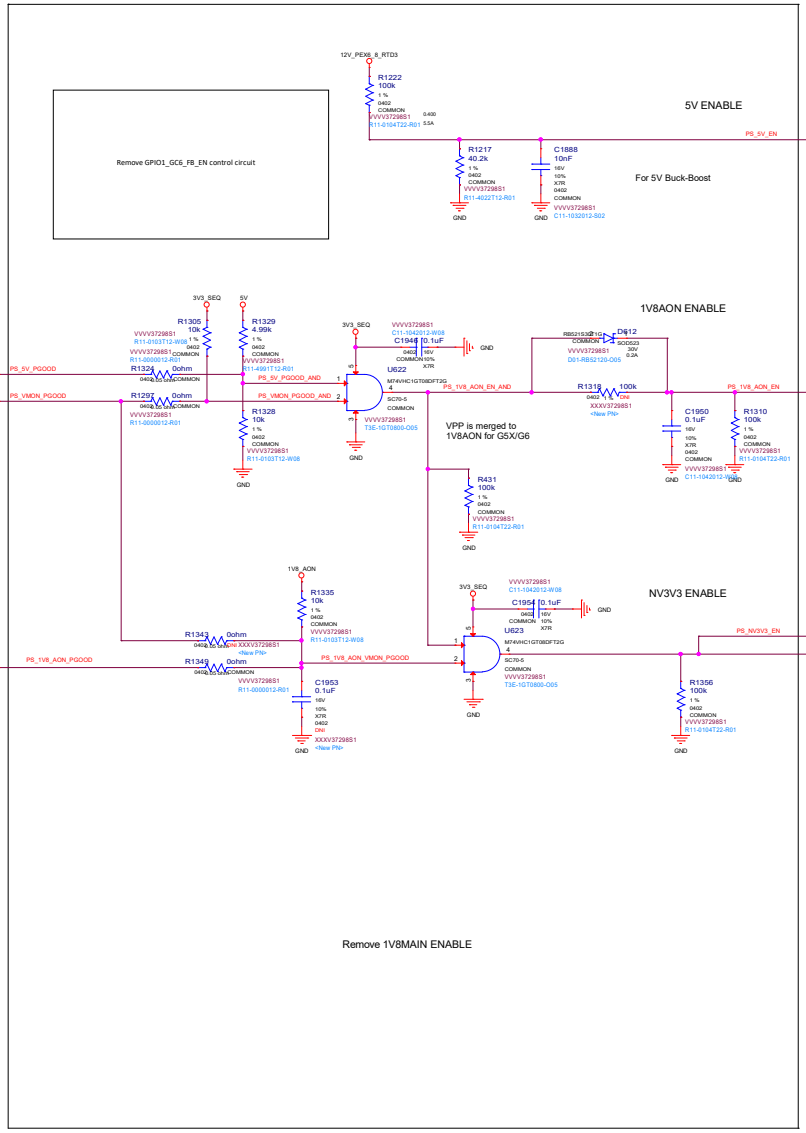
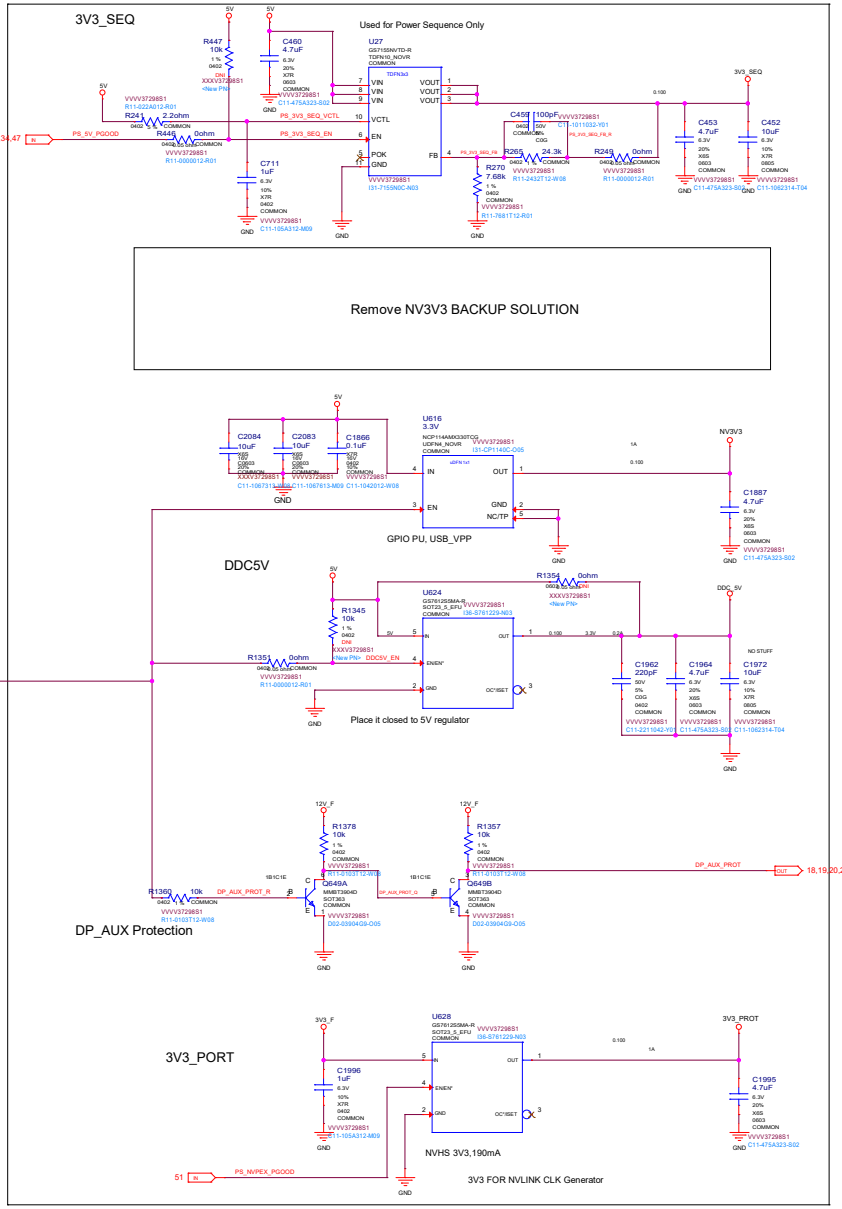
PAGE46; PS: Pre-Filter



PAGE 47: SEQUENCE:5V,1V8,NV3V3 ENABLE





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Size: Custom	Document Description: SEQUENCE:5V,1V8,NV3V3 ENABLE
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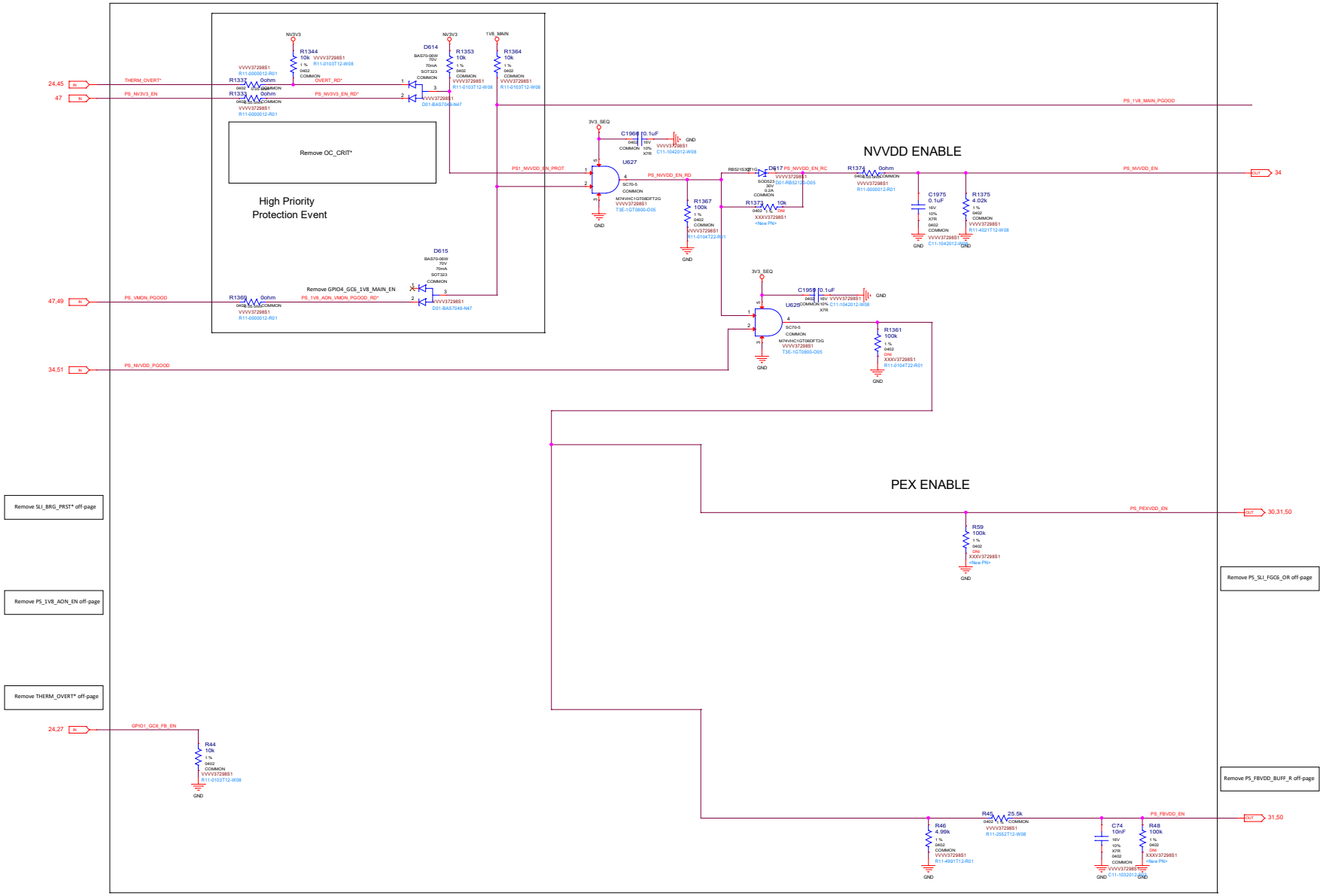
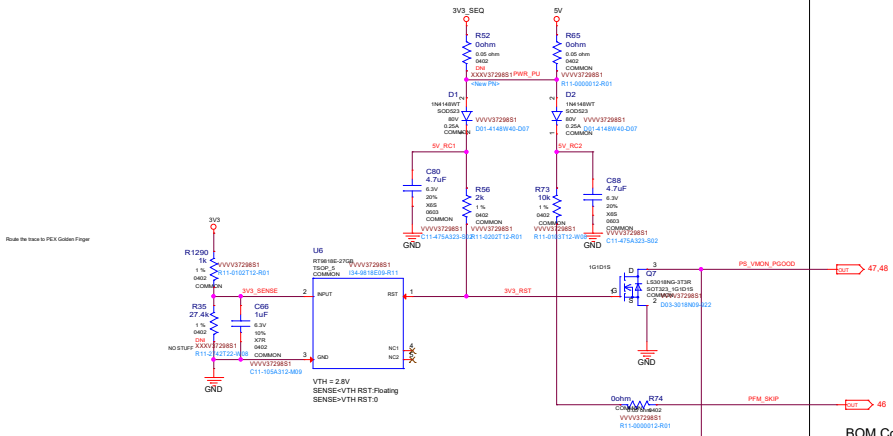
PAGE 48: SEQUENCE:NV,PEX,FB ENABLE



PCIE Voltage Monitor



Remove：
1. GPIO1_GC6_FB_EN off-page
2. PS_RTD3_12V_SW off-page
3. 12V Voltage Monitor

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

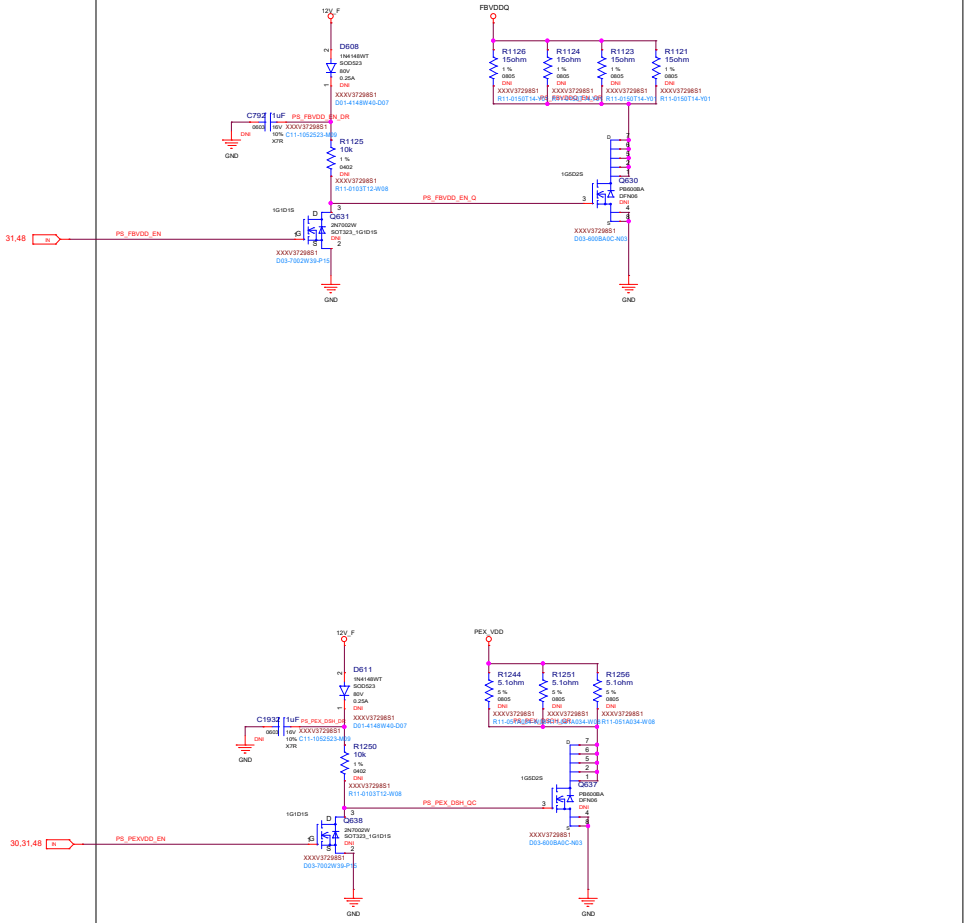
Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX

and All Input 12Vs

PAGE 50: SEQUENCE:DISCHARGE



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Size: Custom	Document Description: SEQUENCE:DISCHARGE	Rev: 7.1
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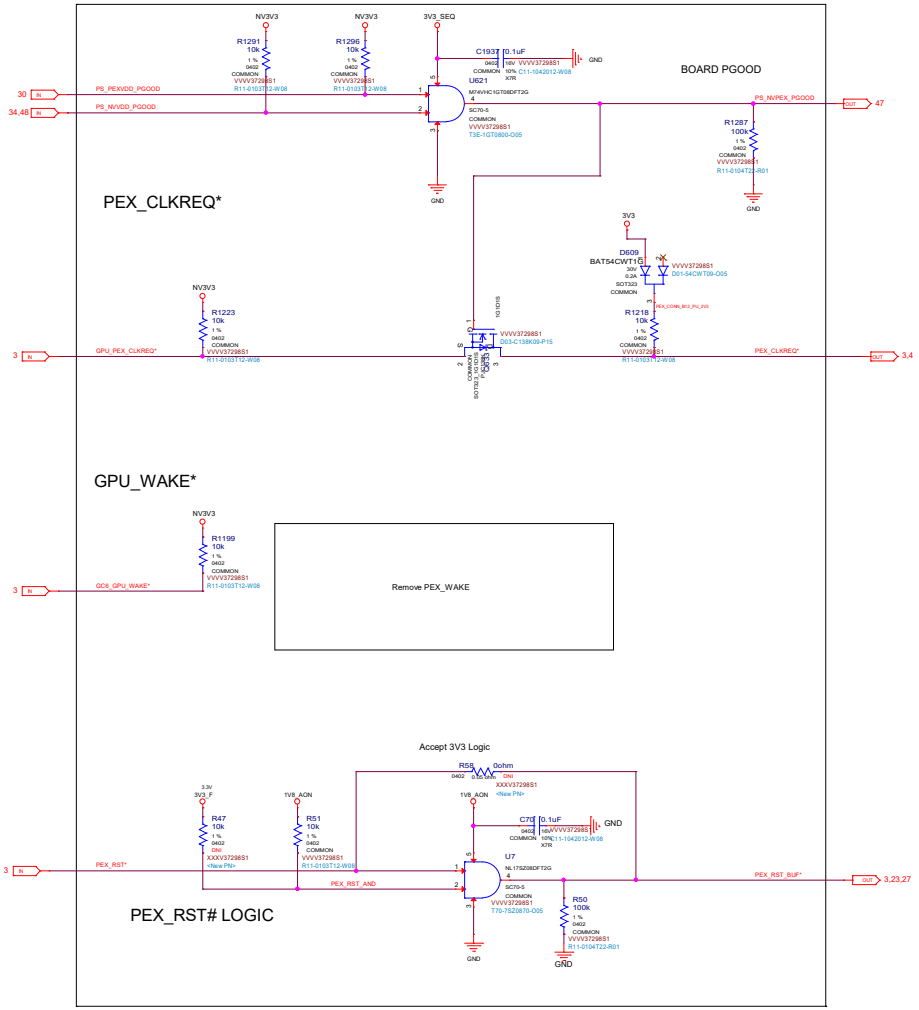
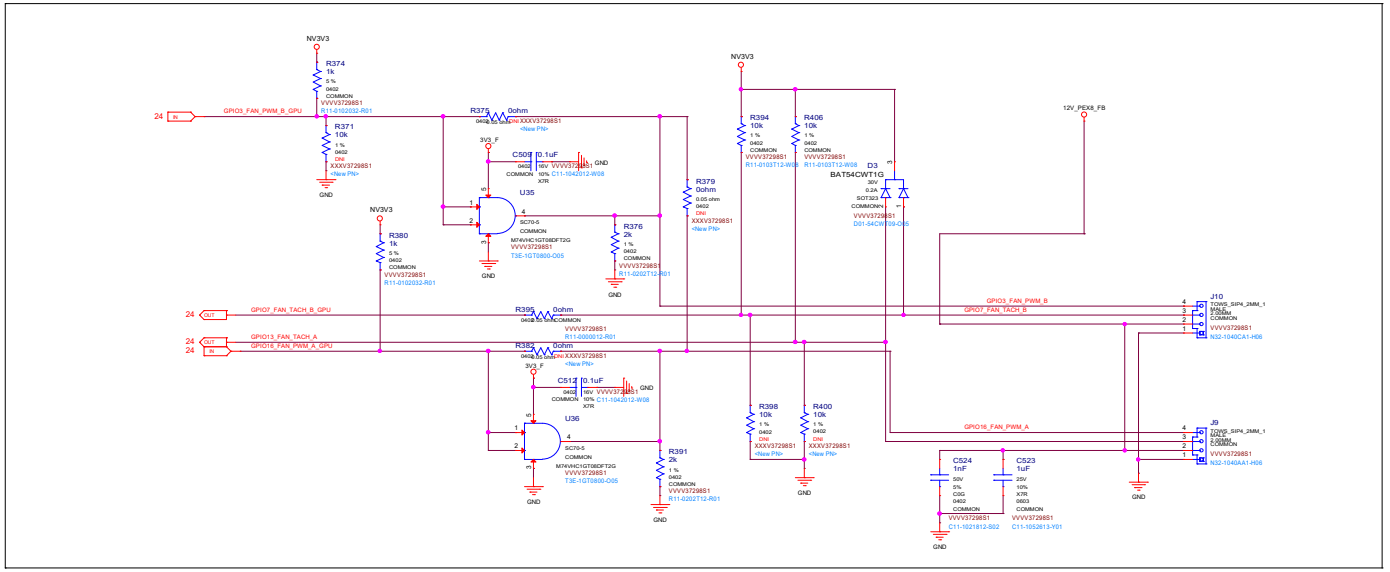

BOARD PGOOD
PEX_CLKREQ*
GPU_WAKE*
Remove PEX_WAKE
Accept 3V3 Logic
PEX_RST# LOGIC

PAGE 52: LED & FAN HEADERS

Remove LED



Remove LED BOOST

MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V372	
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Page53: LED_CONTROLLER_IT8295

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Size: Custom	Document Description: LED_CONTROLLER_IT8295
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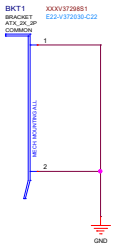
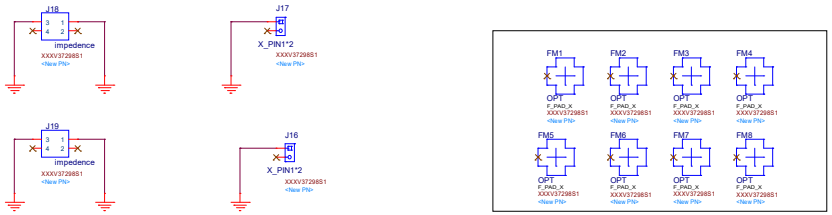
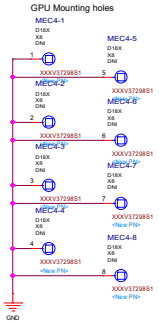
Brackets:



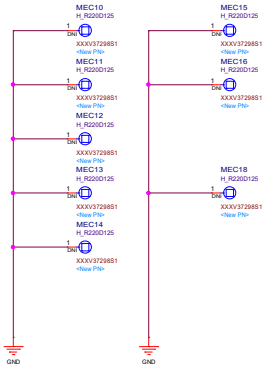
Screw



GPU Mounting holes



Mechanical Holes Symbol



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MS-V372		
Size: Custom	Document Description: MECHANICAL;BRACKET/THERMAL SOLUTION	Rev: 7.1
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