PG180-A02

256b GDDR6 x16
TALL DP + DP + DP + HDMI/DP + USB

TABLE OF CONTENTS

Page	Description
1	Table of Contents
2	Block Diagram
3	PCI Express
4	PCI Termination
5	MEMORY: GPU Partition A/B
6	MEMORY: FBA Partition 31..0
7	MEMORY: FBA Partition 63..32
8	MEMORY: FBB Partition 31..0
9	MEMORY: FBB Partition 63..32
10	MEMORY: GPU Partition C/D
11	MEMORY: FBC Partition 31..0
12	MEMORY: FBC Partition 63..32
13	MEMORY: FBD Partition 31..0
14	MEMORY: FBD Partition 63..32
15	GPU PWR and GND
16	GPU Decoupling
17	GPU DECOUPLING
18	IFPAB TALL-DP
19	IFPE DP
20	IFPF USBC
21	IFPC HDMI 2.0/DP
22	IFPD DP
23	NVHS INTERFACE
24	MISC: FAN,THERMAL,JTAG,GPIO,STEREO
25	MISC3: ROM, STRAPS
26	MISC: XTAL, PLL
27	MISC: USB PPC
28	PS: USB VR
29	PS: 5V, 5V BACKUP
30	PS: PEXVDD, 1V8
31	PS: FBVDD CONTROLLER
32	PS: FBVDD CONTROLLER OVR3
33	PS: FBVDD PHASE 1, 2
34	PS: NVVDD CONTROLLER OVR8
35	PS: NVVDD Phase 1, 2
36	PS: NVVDD Phase 3, 4
37	PS: NVVDD Phase 5, 6
38	PS: NVVDD Phase 7, 8
39	PS: INPUT SWITCH RTD3
40	PS: INPUT SWITCH RTD3 USB
41	PS: INPUT SWITCH RAIL BALANCE
42	PS: 12V CURRENT STEERING
43	PS: VR THERMAL PROTECTION
44	PS: INPUTS, FILTERING AND MONITORING
45	PS: CURRENT STEERING,HOT UNPLUG DETECT
46	PS: PRE-FILTER
47	SEQUENCE: 5V, 1V8, NV3V3 ENABLE
48	SEQUENCE: NV, PEX, FB ENABLE
49	SEQUENCE: PCIE VOLTAGE MONITOR
50	SEQUENCE: DISCHARGE
51	SEQUENCE: MISC
52	LED & FAN HEADERS
53	LED 2
54	Mechanical: Bracket/Thermal Solution

V372-3.0 change List

Page	Description
18	Change J4 footprint
19	Change J3 footprint
20	Remove DP co-layout
21	Remove JTAG & unused GPIO
32	Remove 0031_PS_ FBVDD CONTROLLER OVR3
34	NVVDD CONTROLLER change to MP2888A
35	DRMOS change to 10phases
36	DRMOS change to 10phases
37	Add NVVDD Output CAP
41	Remove INPUT SWITCH Rail Balance
44	J8 change to 8pin
	Add Fuse F1~F3
	Change 12V input choke footprint
45	Add Hot Unplug Detect for J8
52	Add Remove LED & Fan Vin_12V option
53	Add MCU IT8295 for RGB LED

V372-3.1 change List

Base on V372-3.0，No changed

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Size: | Document Description: Table of Contents | Rev: 3.1
Custom
Date: Wednesday, August 08, 2018 | Sheet 1 of 54

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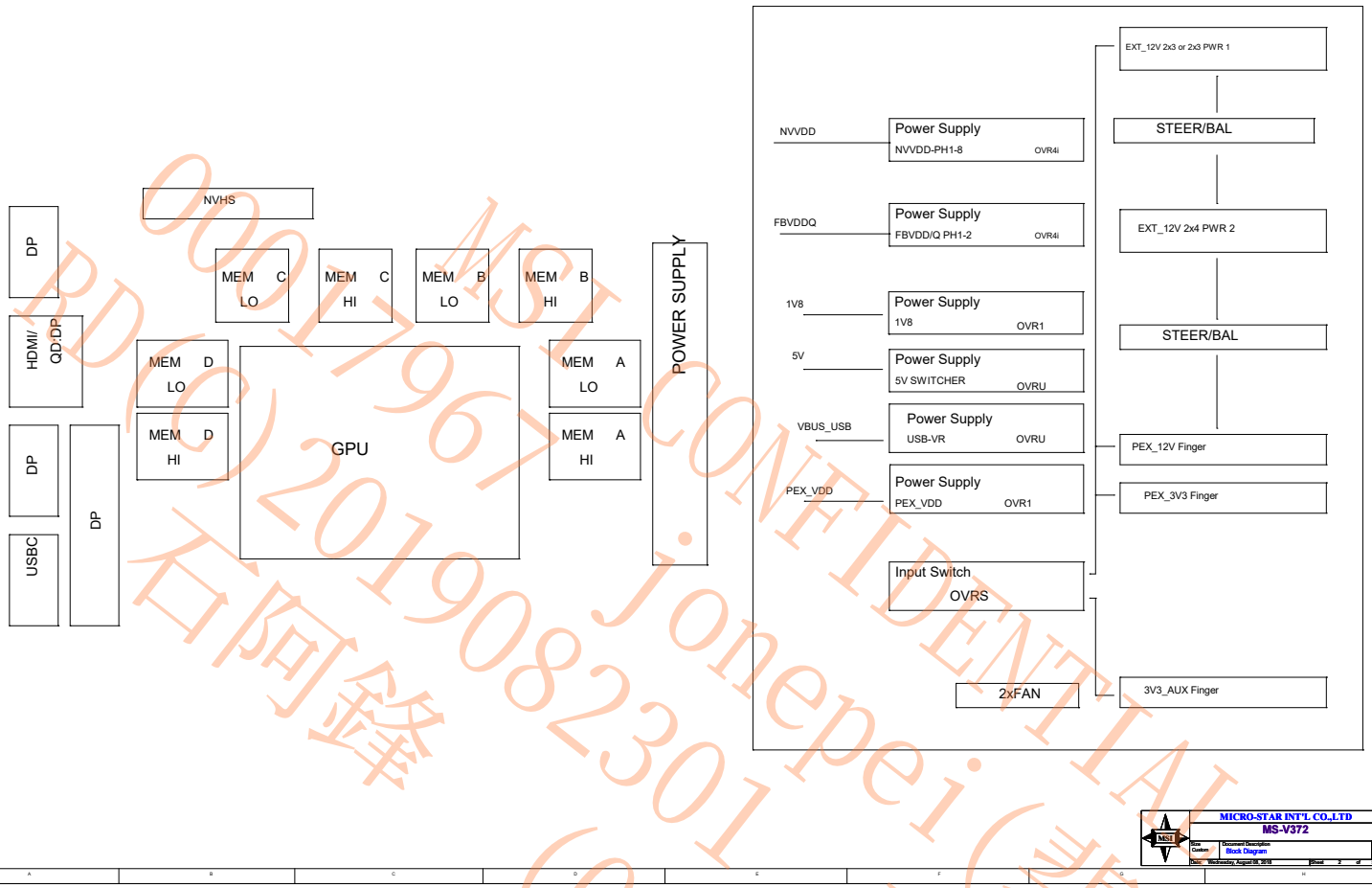
Page2: Block Diagram



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Custom: Block Diagram
Date: Wednesday, August 08, 2018 Sheet 2 of 34

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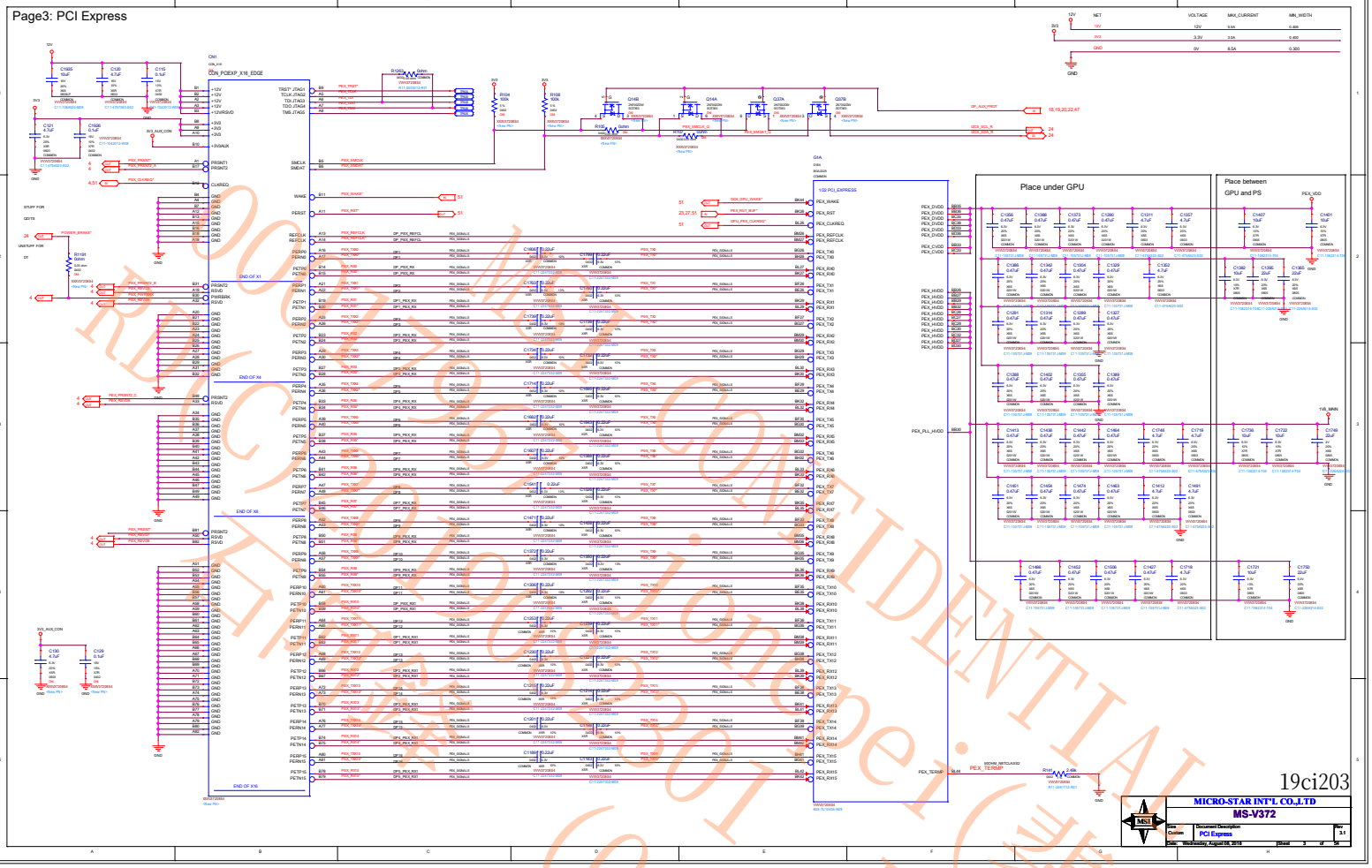
Page3: PCI Express



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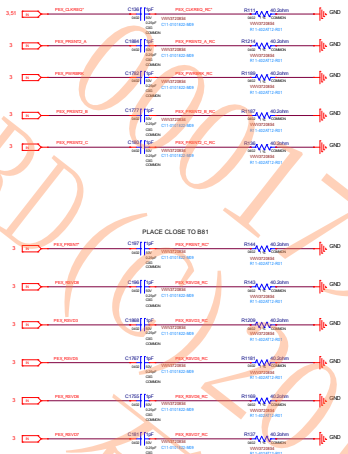
Page4: PCI Termination



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MS-V372	
Size: Custom	Document Description: PCI Termination
Rev: 3.1	
Date: Wednesday, August 08, 2018	Sheet 4 of 54

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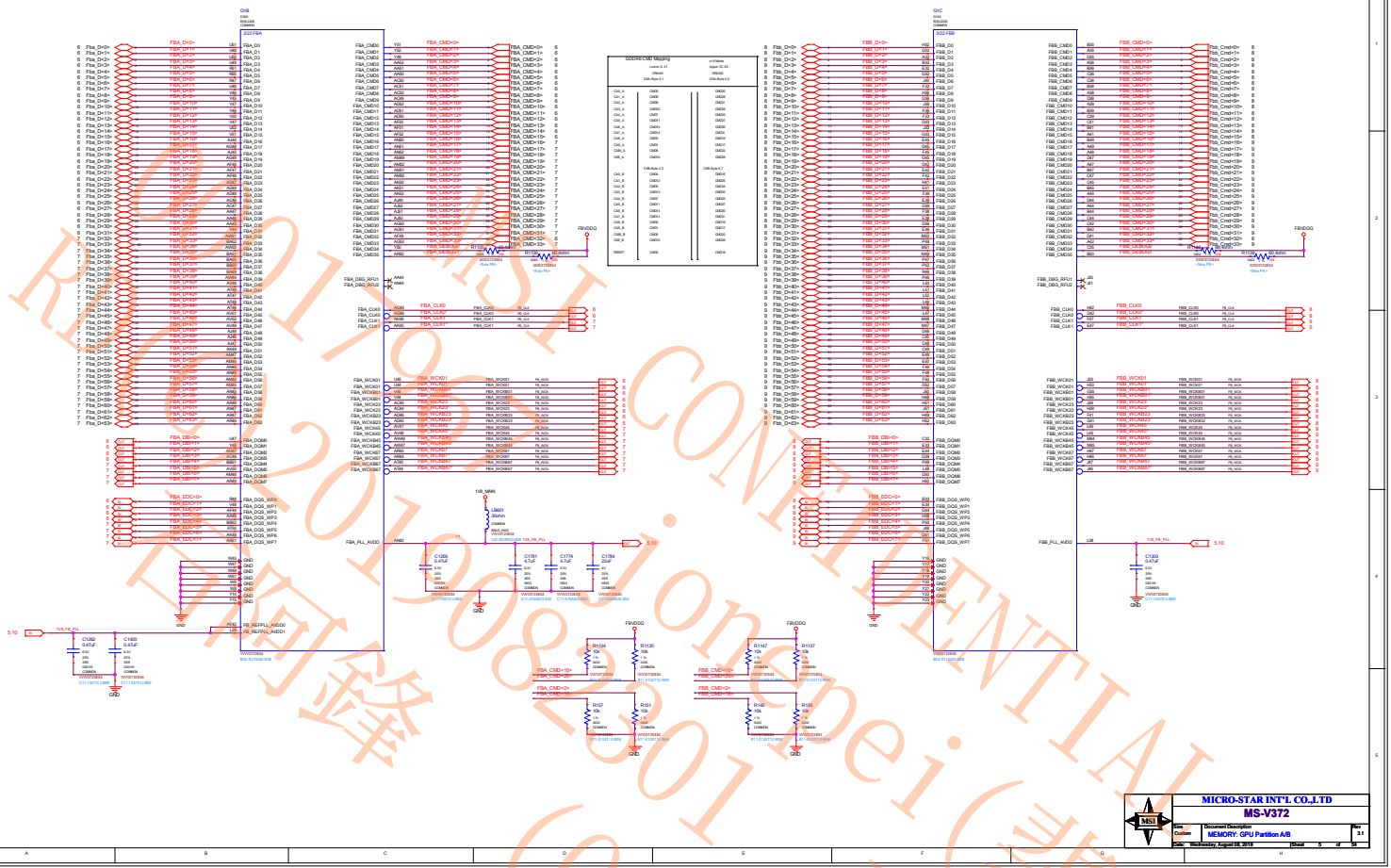
Page5: MEMORY: GPU Partition A/B



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Date: Wednesday, August 08, 2018 | Sheet 5 of 54

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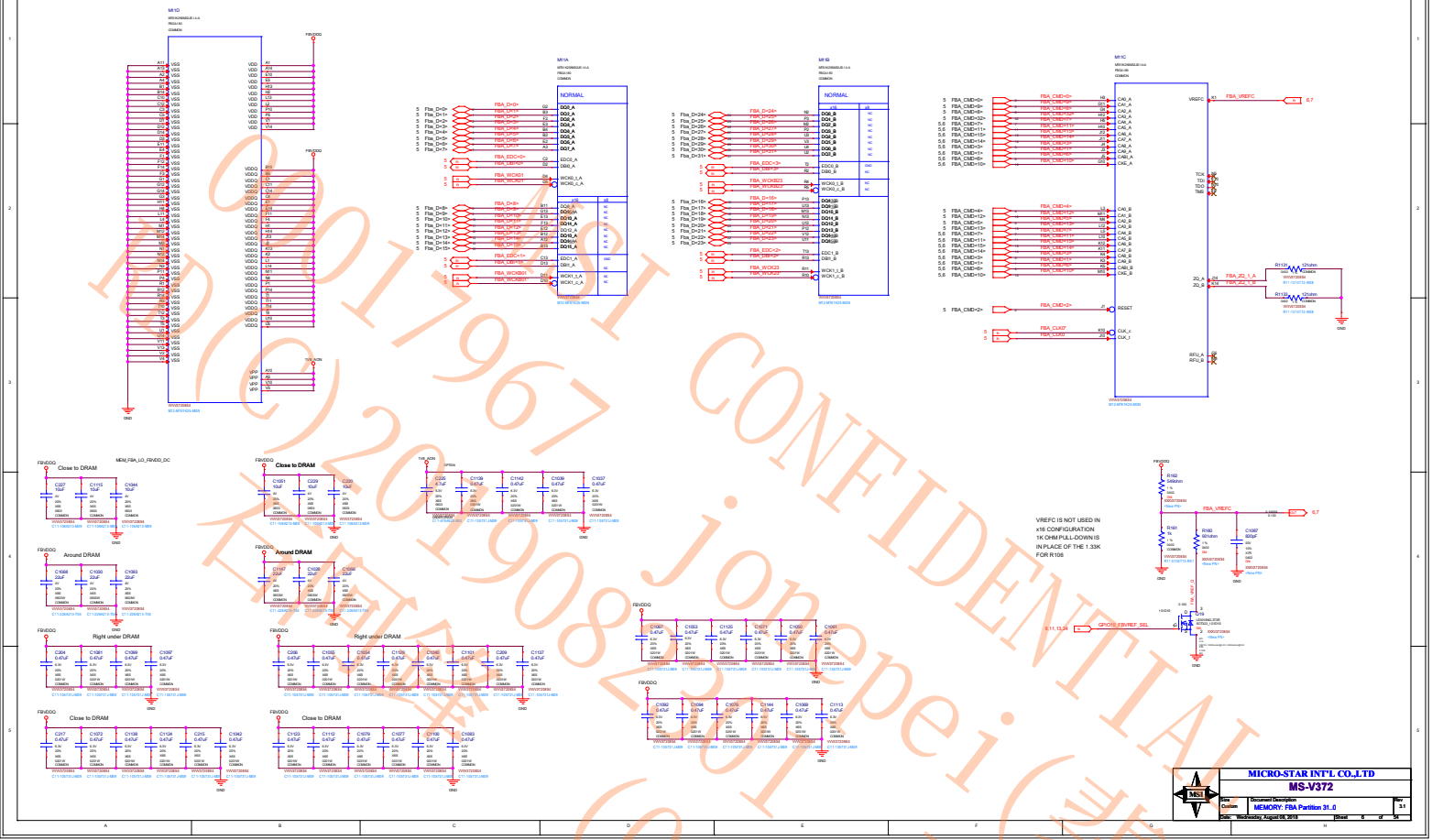
Page6: MEMORY: FBA Partition 31..0



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Size: Custom
Document Description: MEMORY: FBA Partition 31..0
Rev: 3.1
Date: Wednesday, August 08, 2018
Sheet 6 of 54

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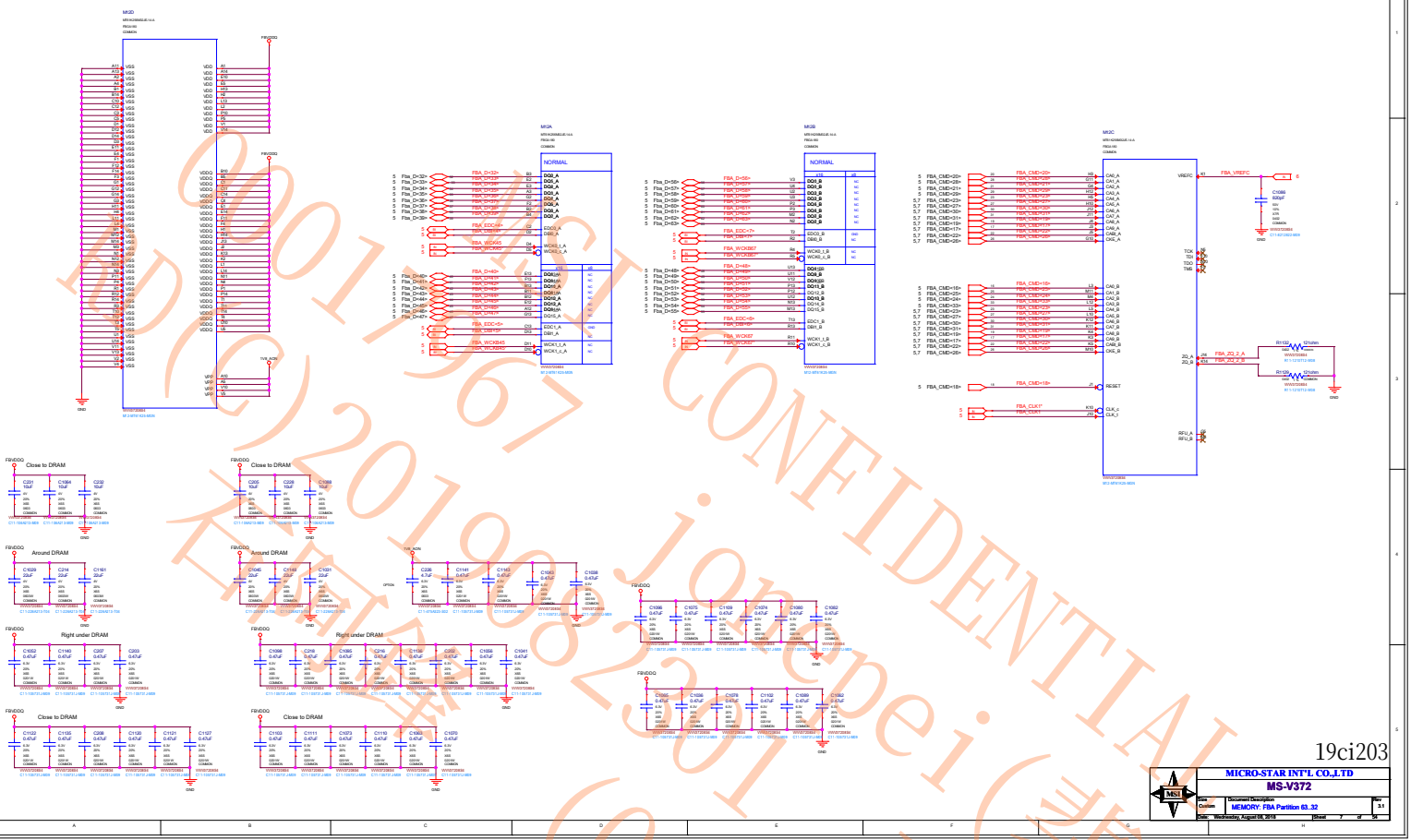

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Size: Custom
Document Description: MEMORY: FBA Partition 63..32
Rev: 3.1
Date: Wednesday, August 08, 2018
Sheet 7 of 54

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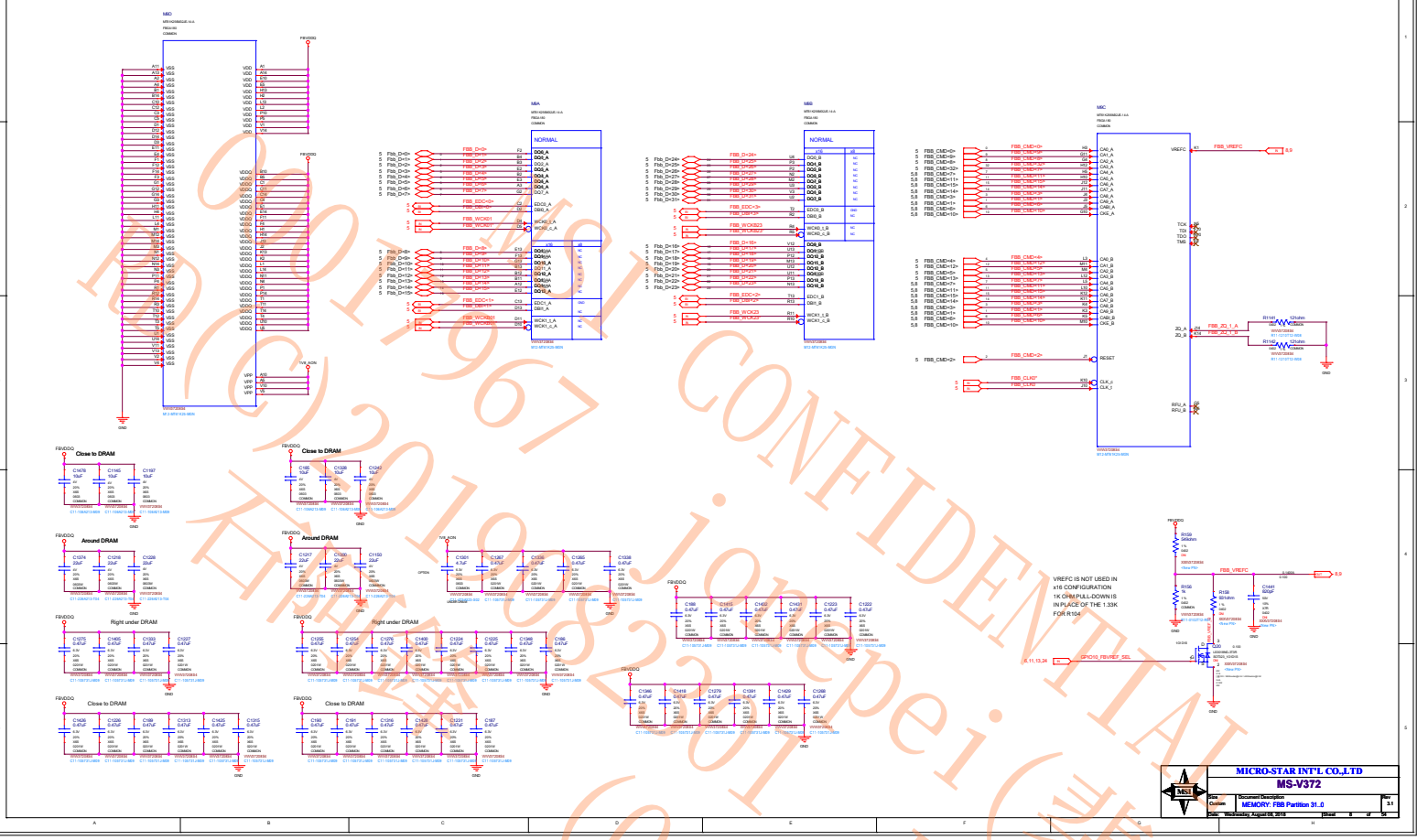
Page8: MEMORY: FBB Partition 31..0



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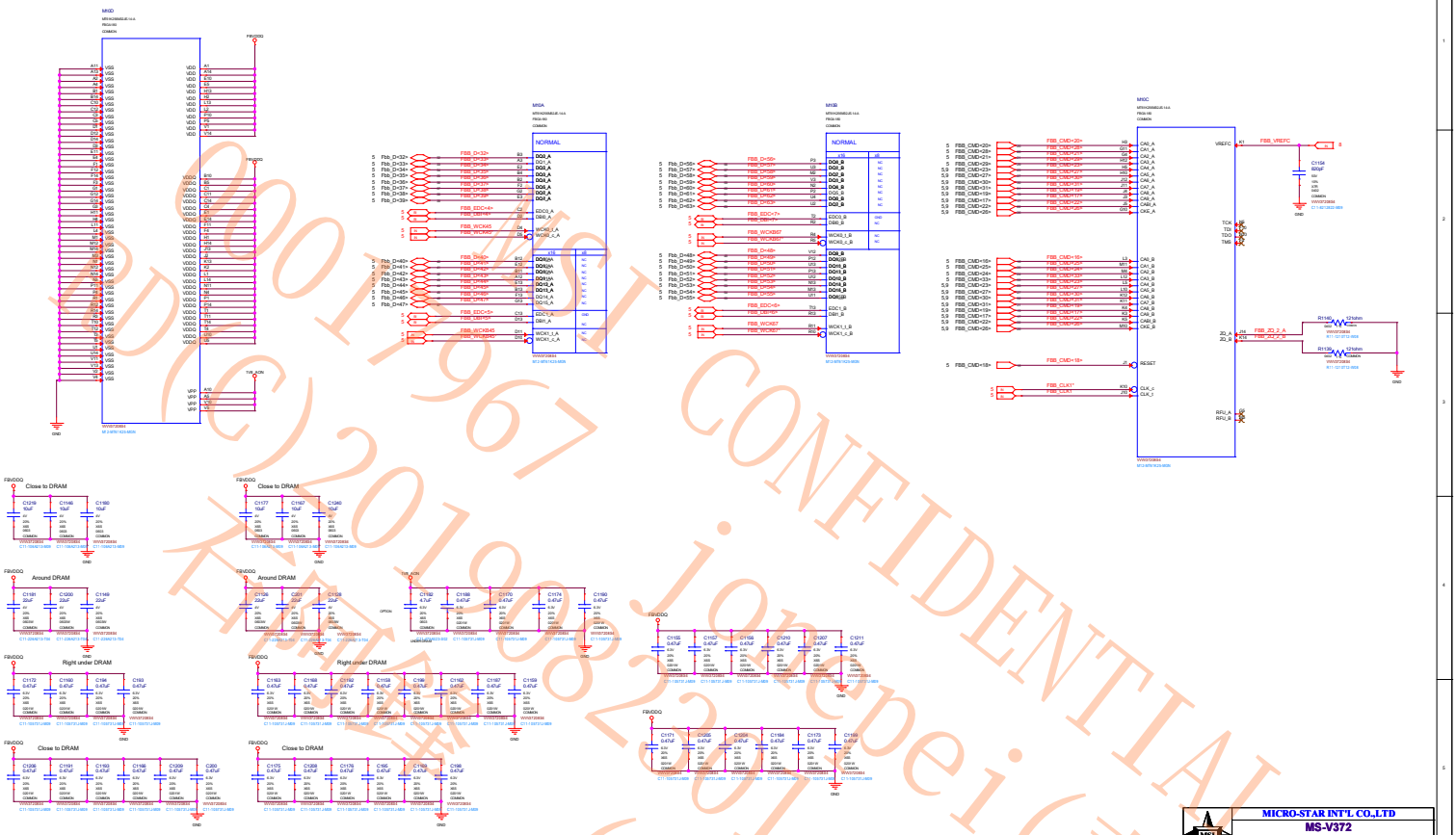
Page9: MEMORY: FBB Partition 63..32



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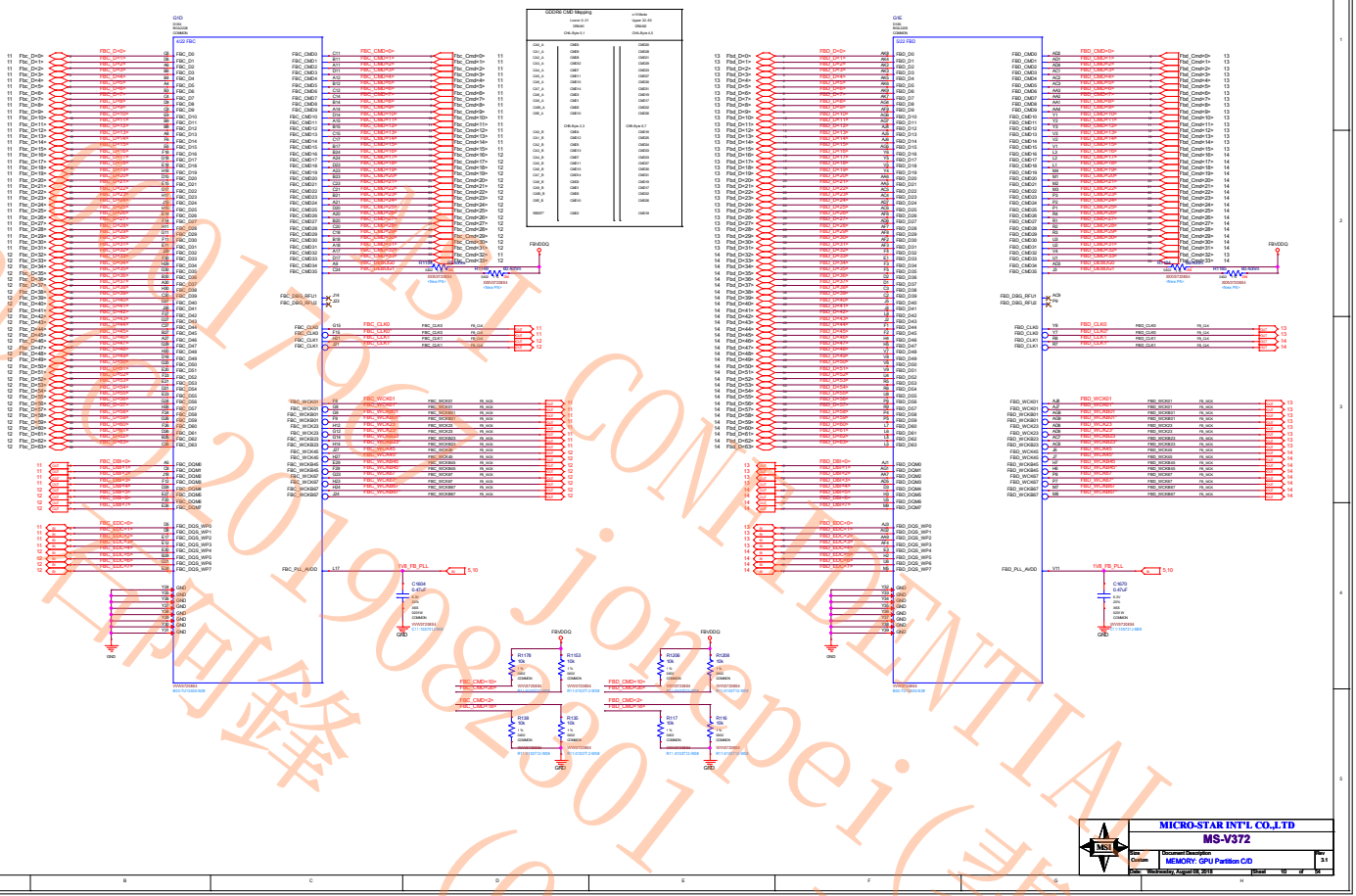

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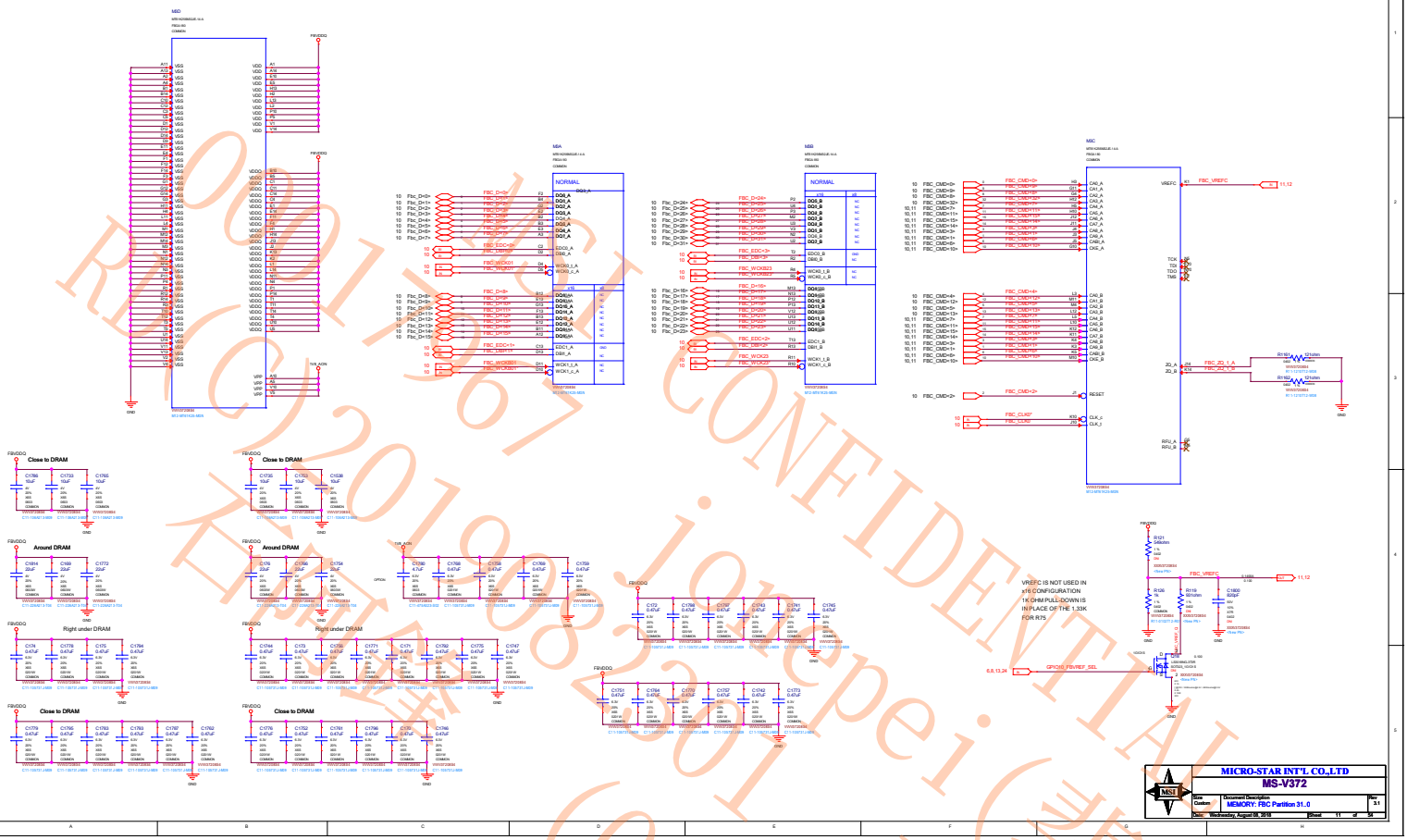

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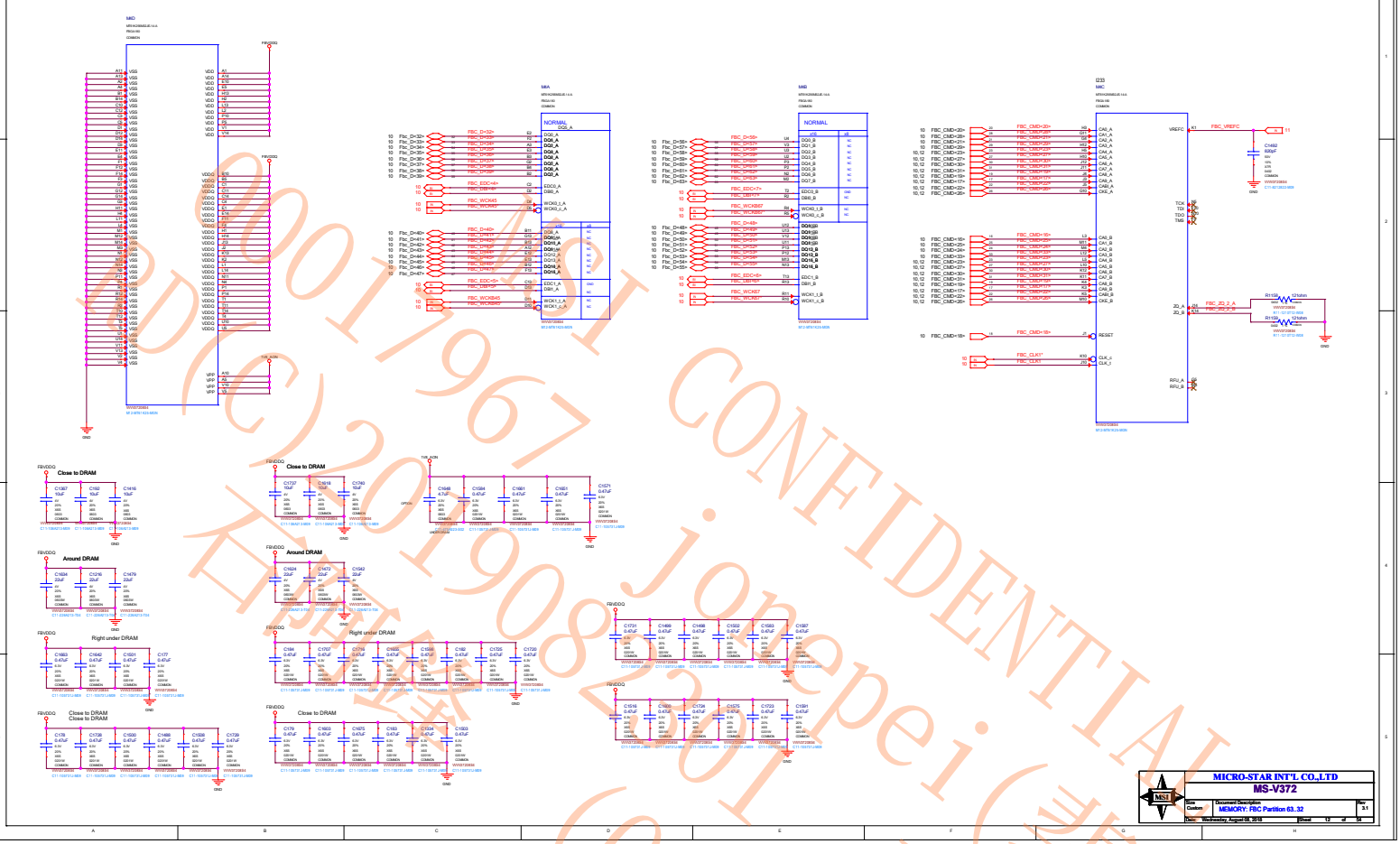
Page12: MEMORY: FBC Partition 63..32



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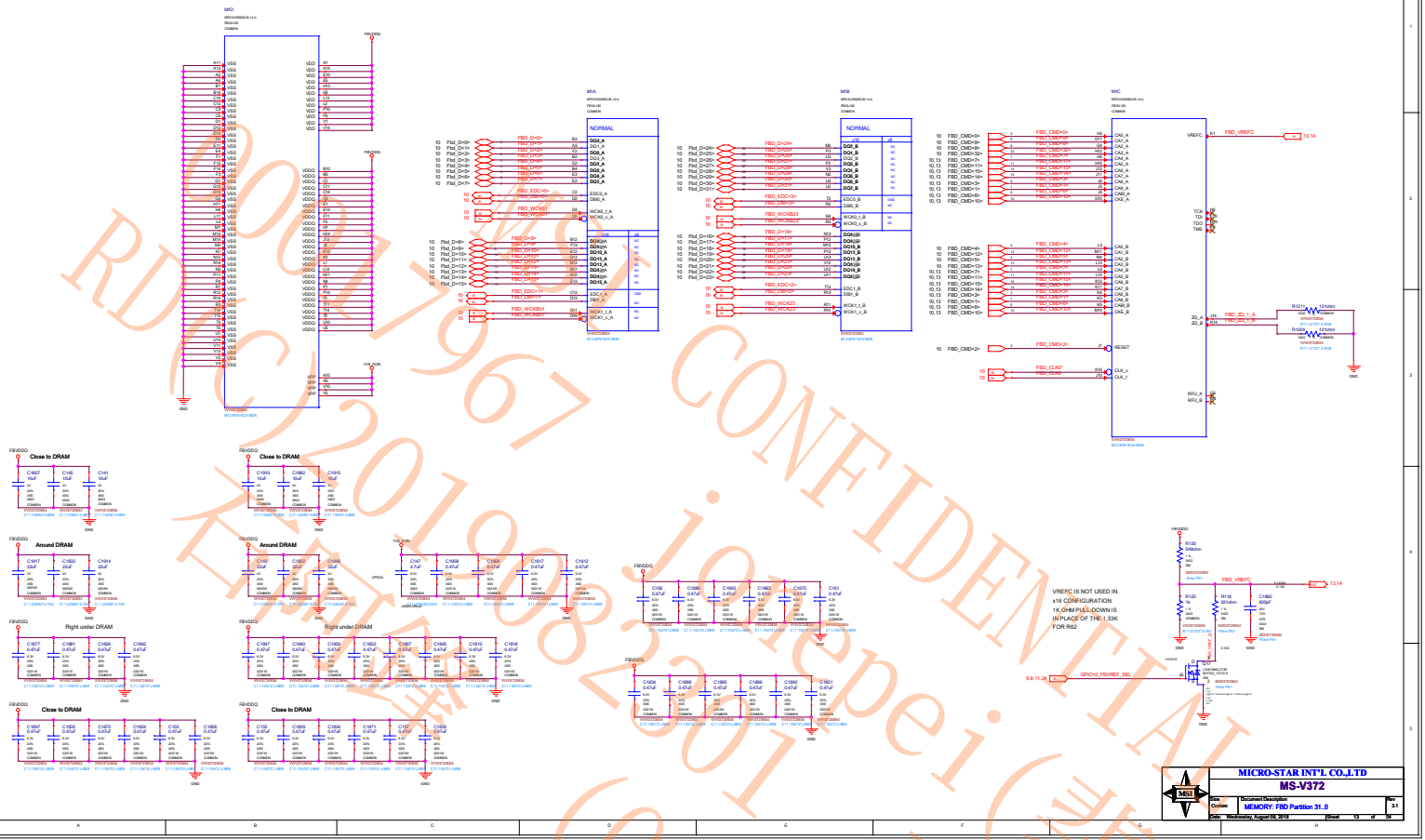
Size:	Document Description: MEMORY: FBC Partition 63..32
Rev: 3.1	
Date: Wednesday, August 08, 2018	Sheet 12 of 34



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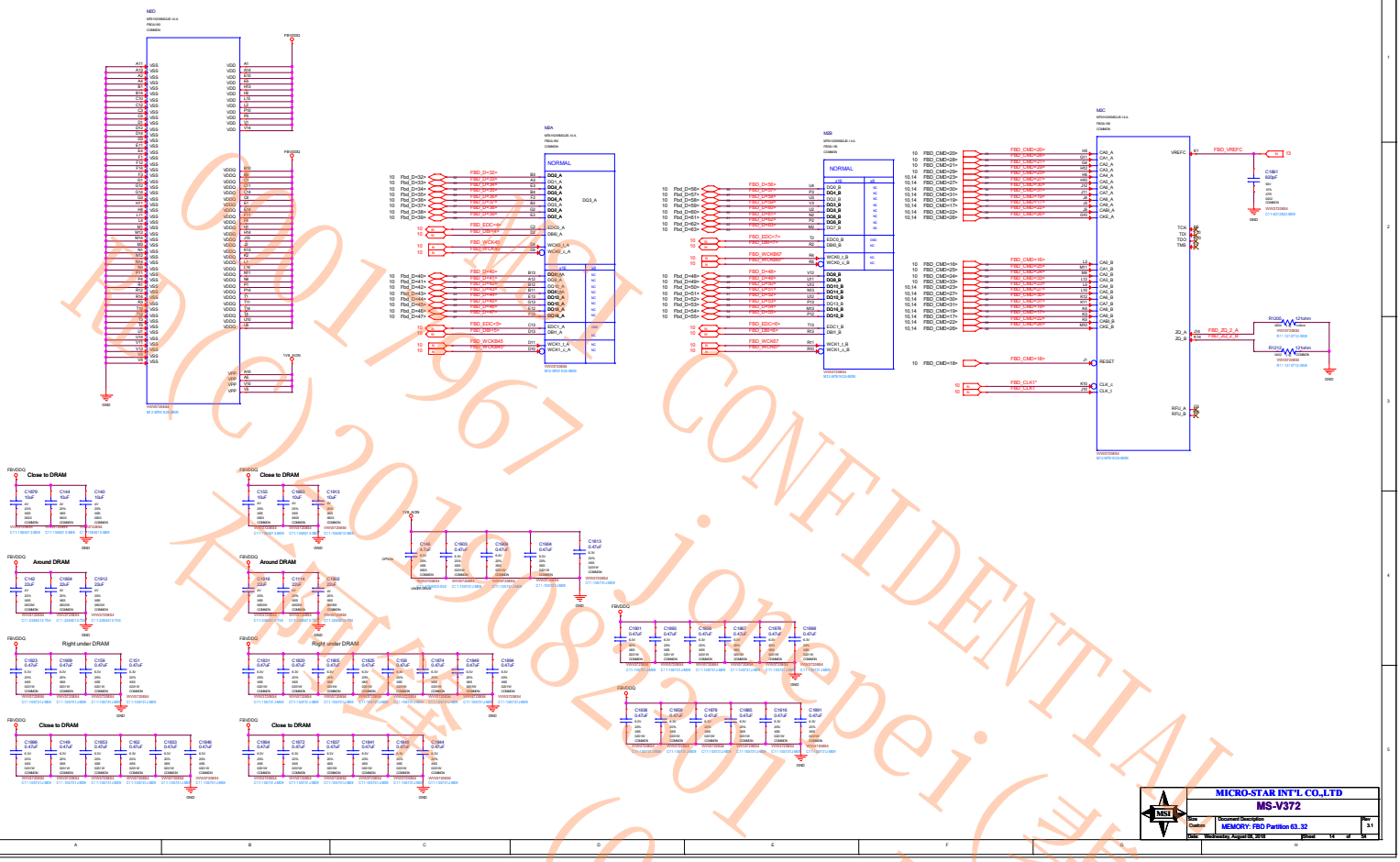
Page14: MEMORY: FBD Partition 63..32



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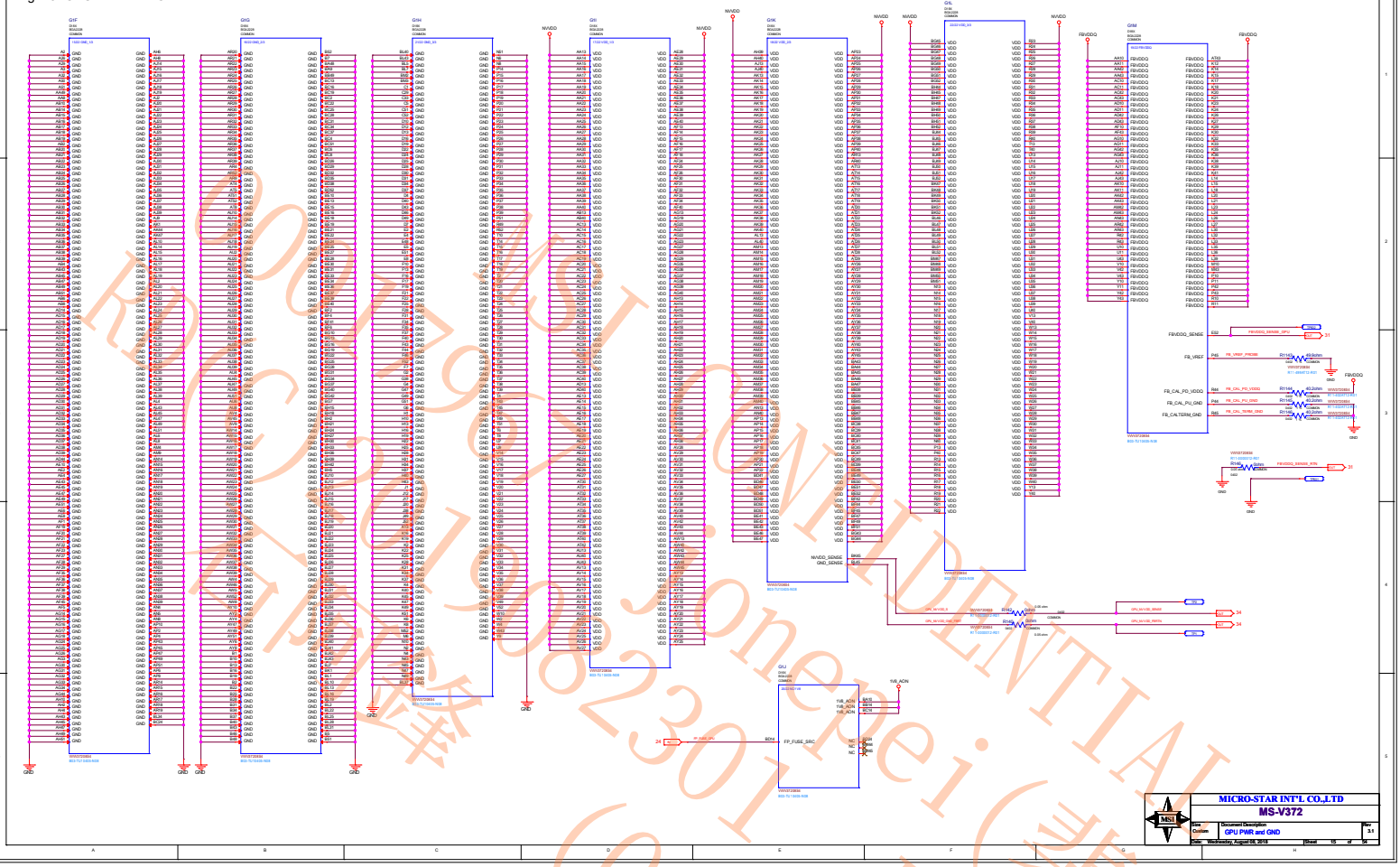
Date: Wednesday, August 05, 2010	Sheet 14 of 54	

Page15: GPU PWR and GND



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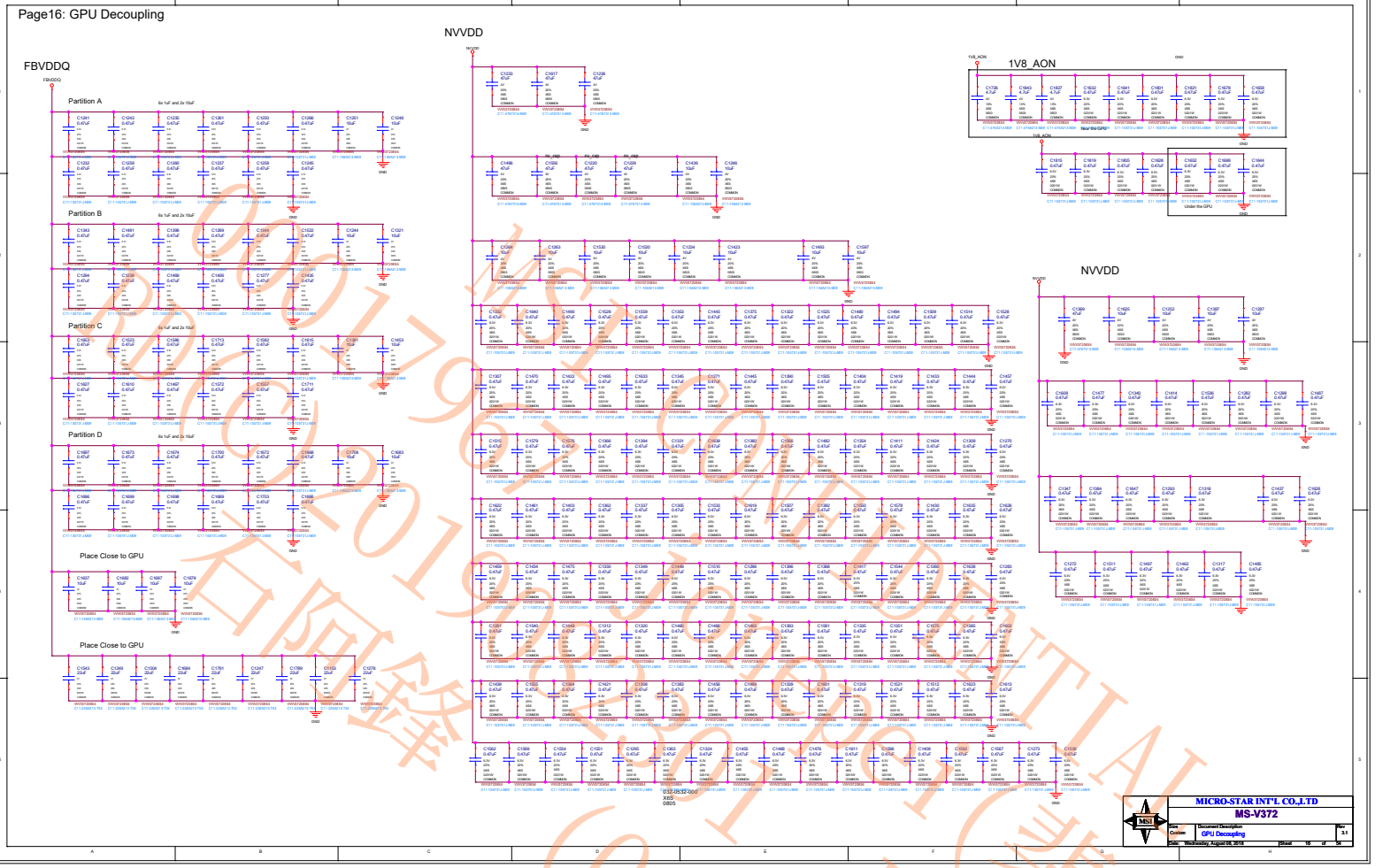
Page16: GPU Decoupling



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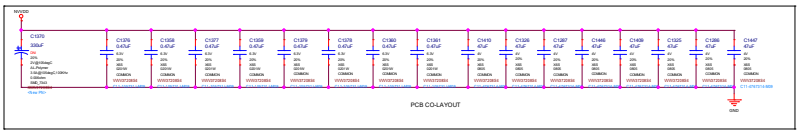
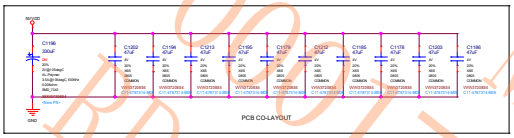
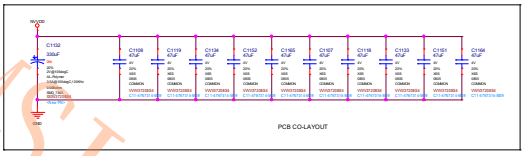
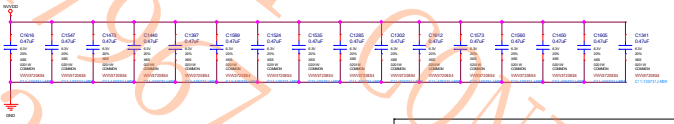
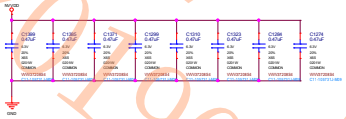
Page17: GPU Decoupling

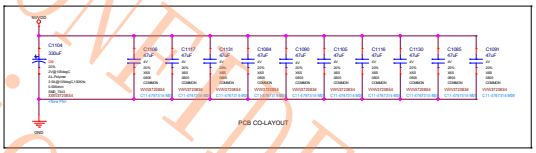


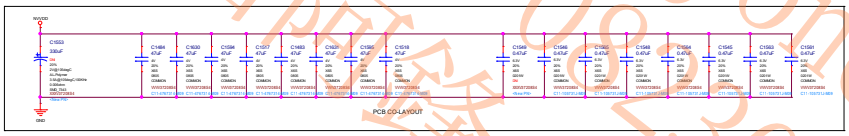












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Size / Custom	Document Description: GPU Decoupling
	Rev: 3.1
Date: Wednesday, August 08, 2018	Sheet 17 of 54

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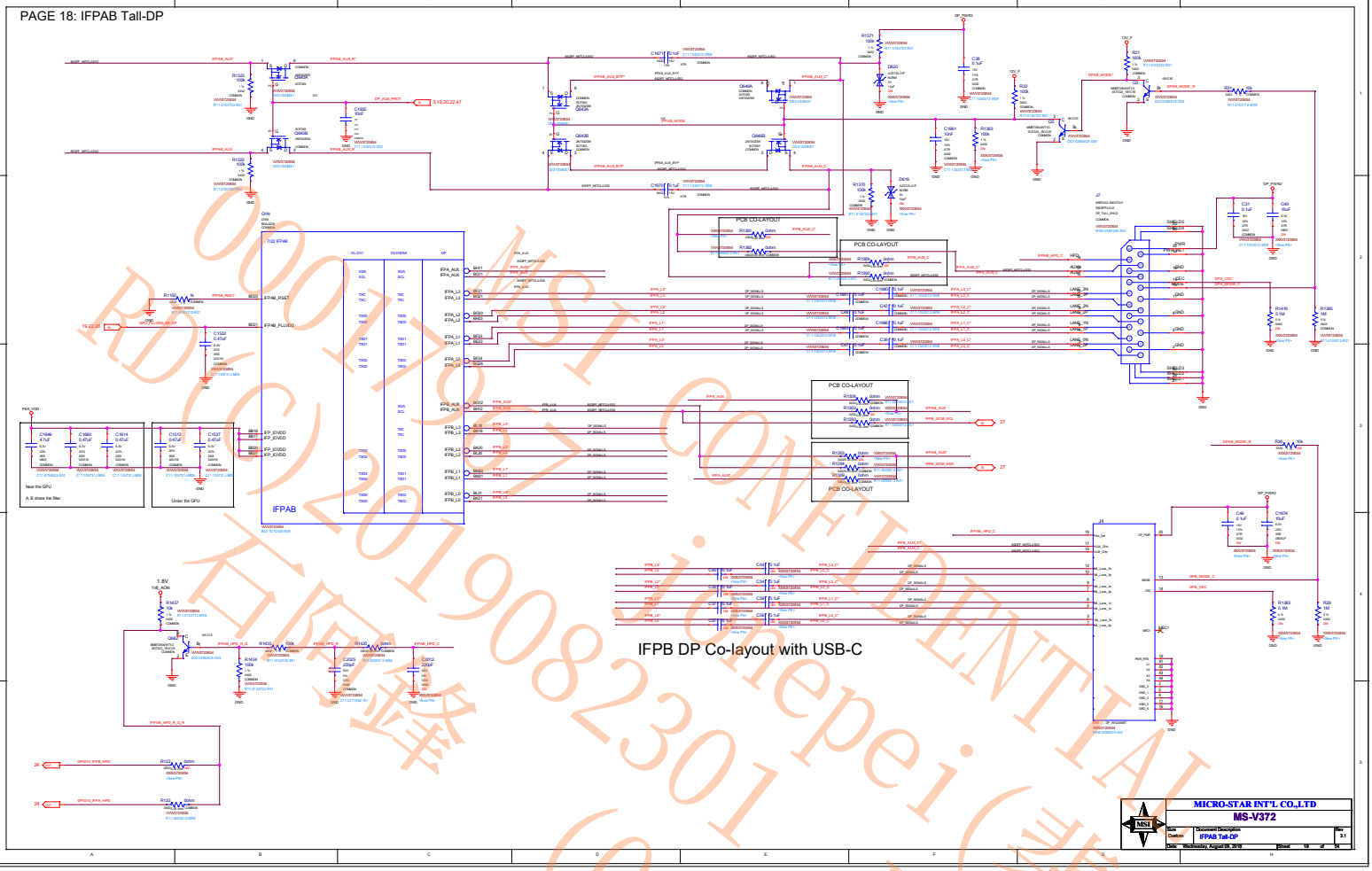
PAGE 18: IFPAB Tall-DP



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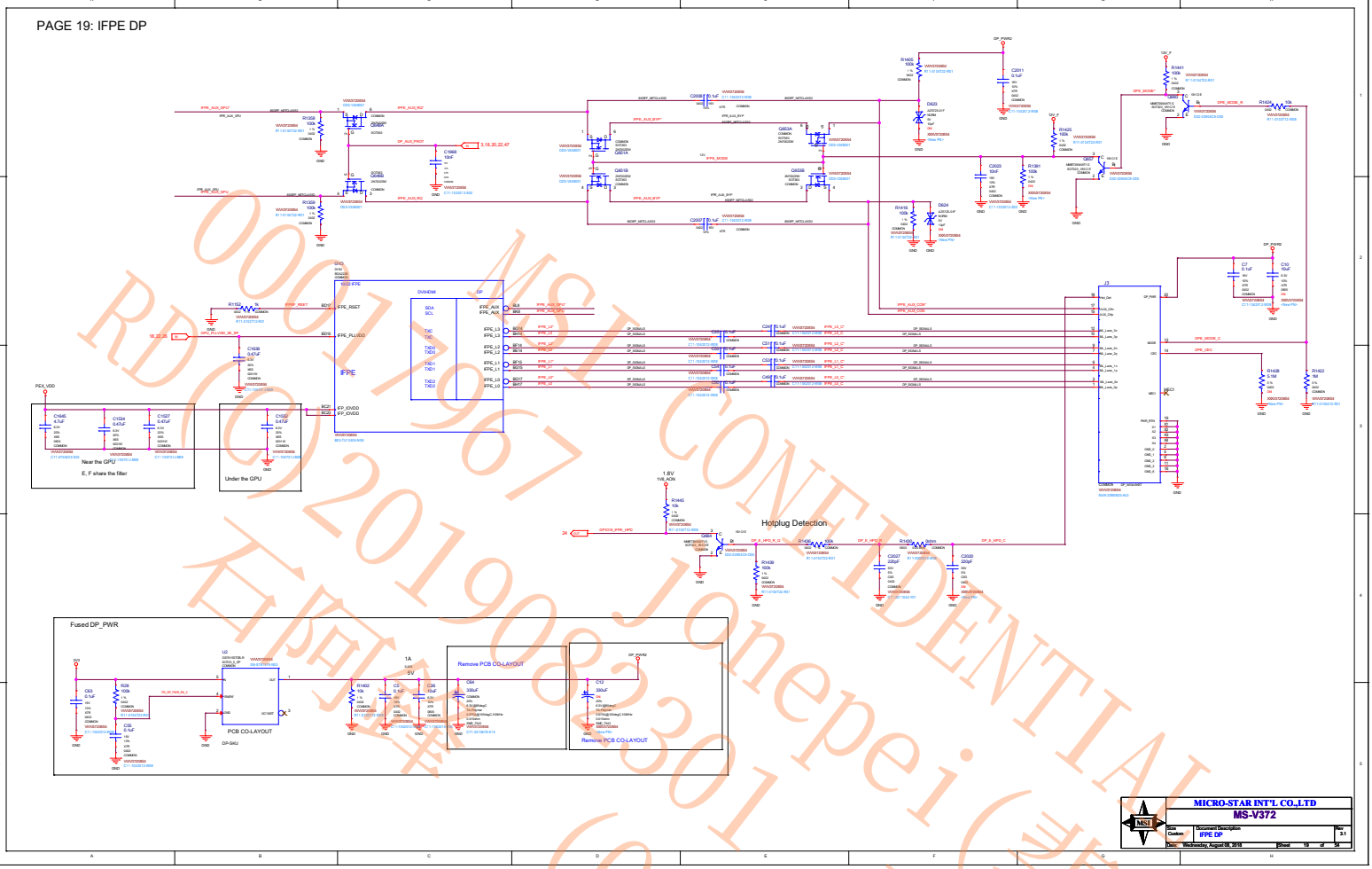
PAGE 19: IFPE DP



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石阿裴
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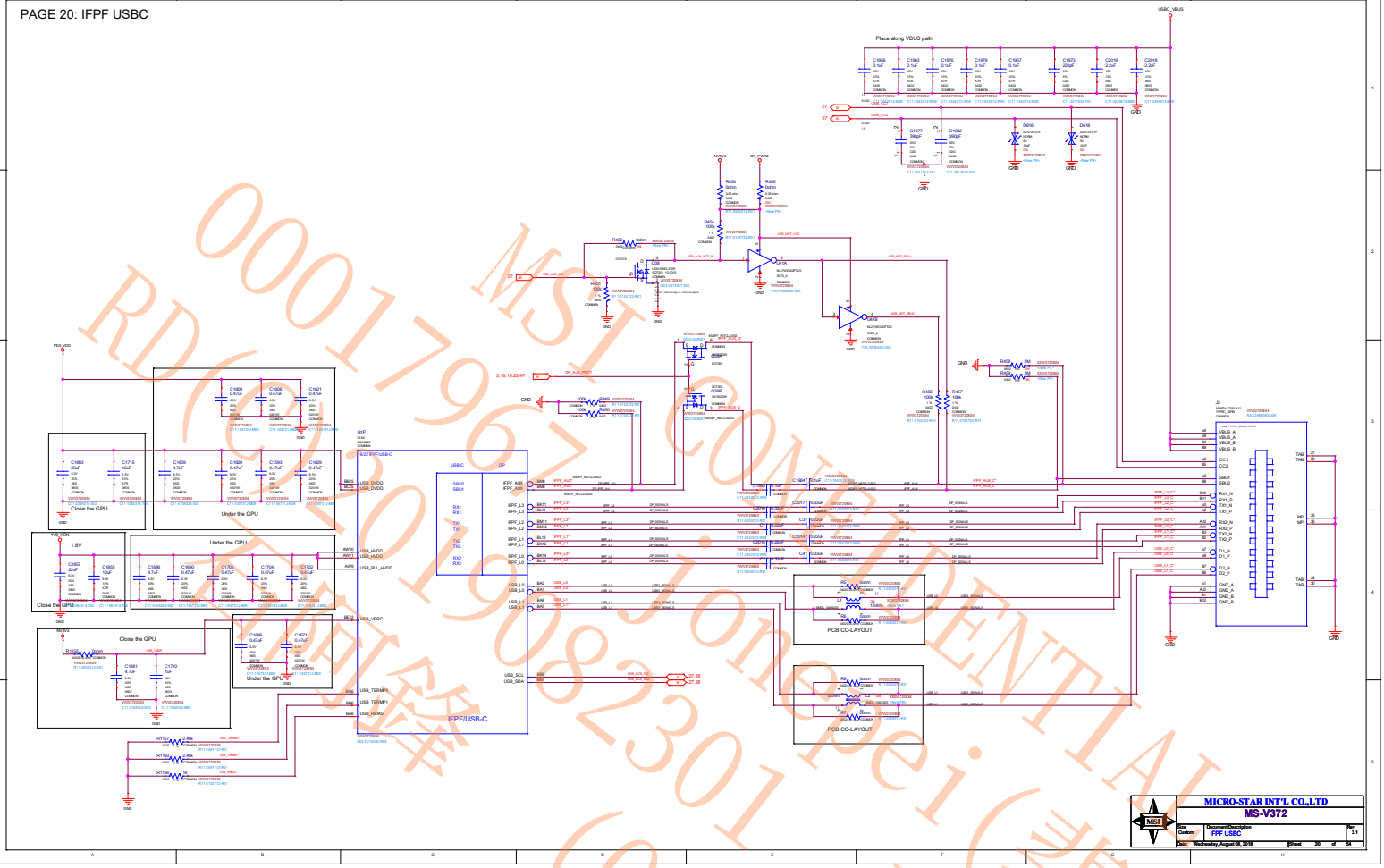
PAGE 20: IFPF USBC



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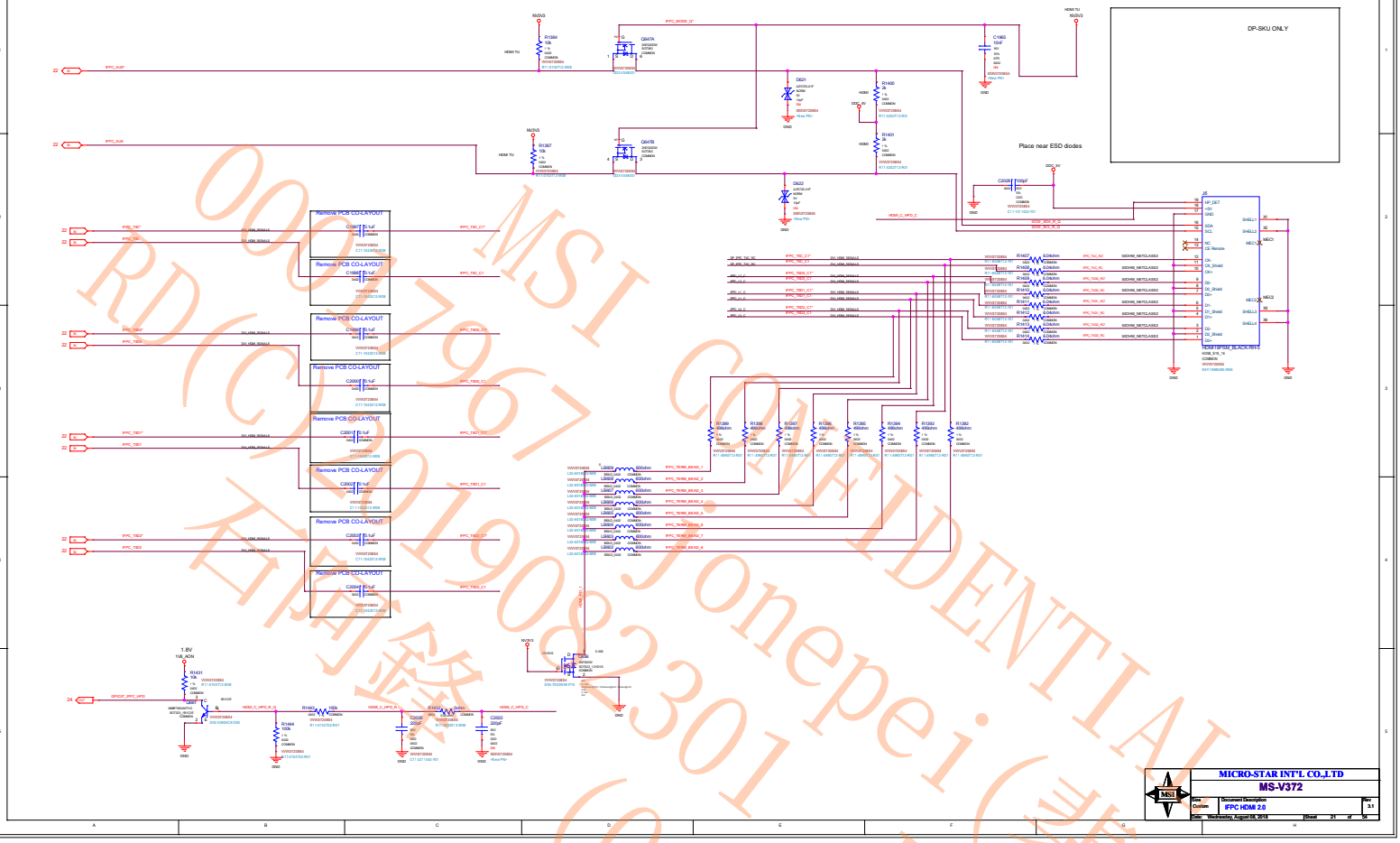
PAGE 21:IFPC HDMI 2.0



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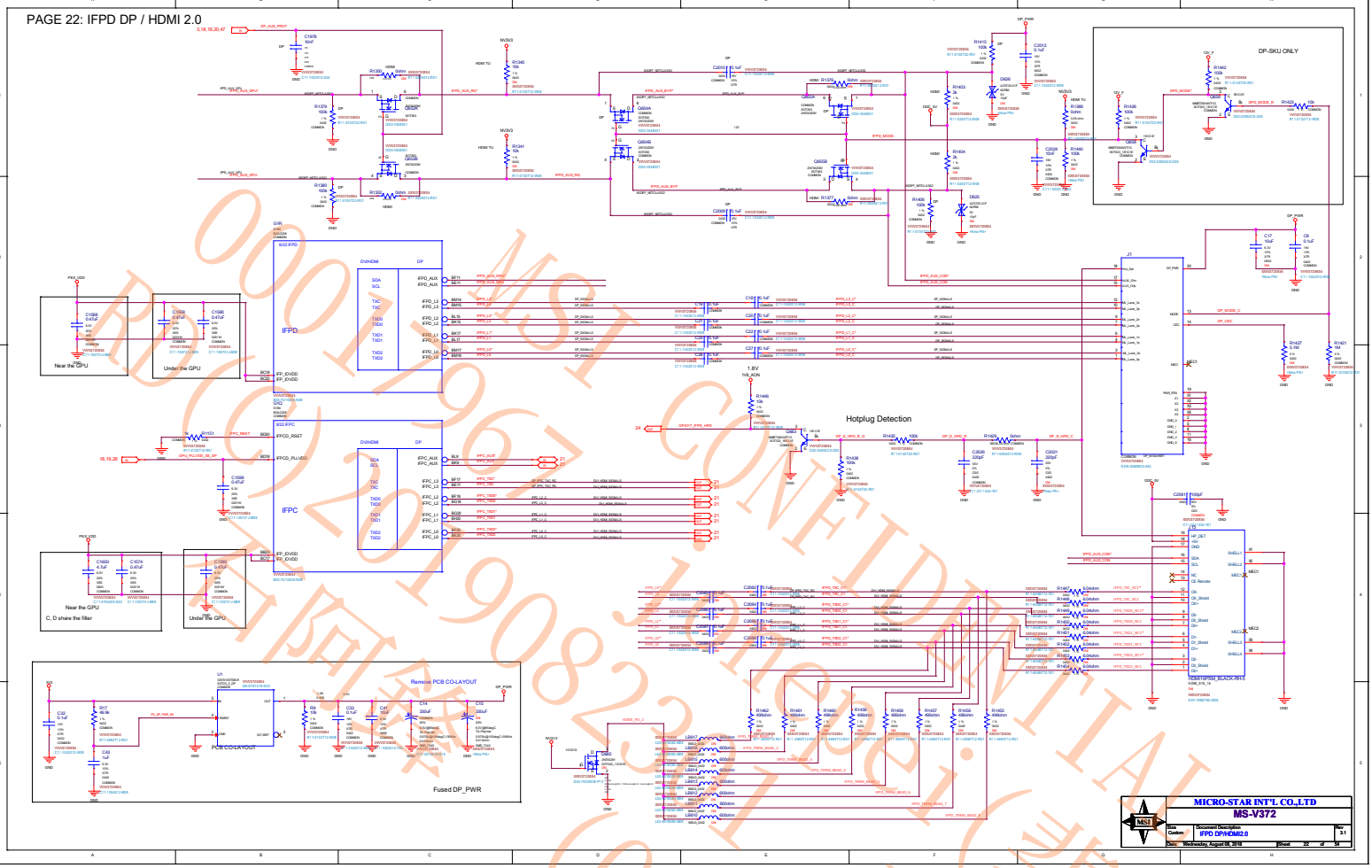

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PC(C)2019908231 Jim Lee (黃亮樂)
(00068760) RMA工程課
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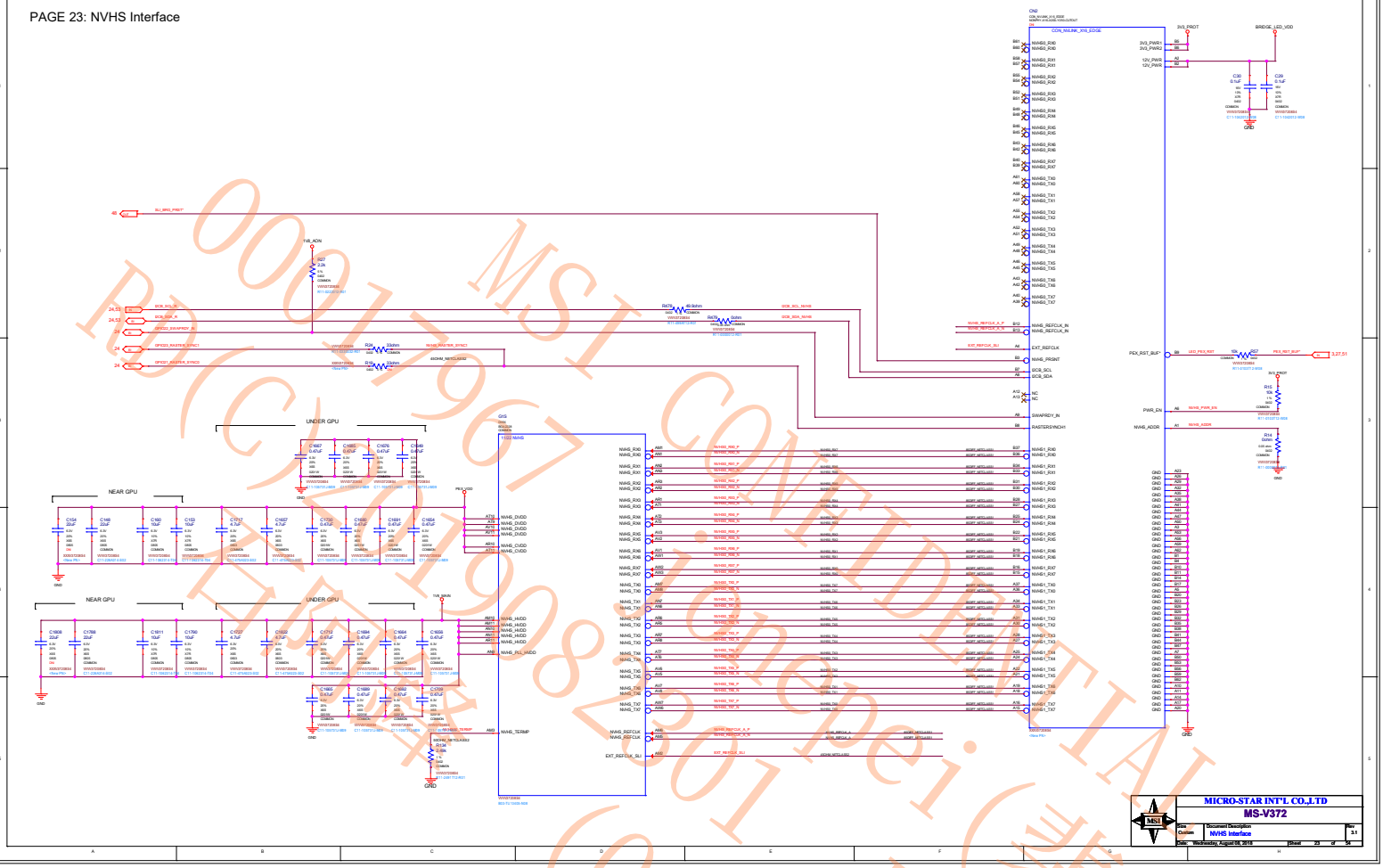
PAGE 23: NVHS Interface



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Date: Wednesday, August 08, 2018 | Sheet 23 of 54

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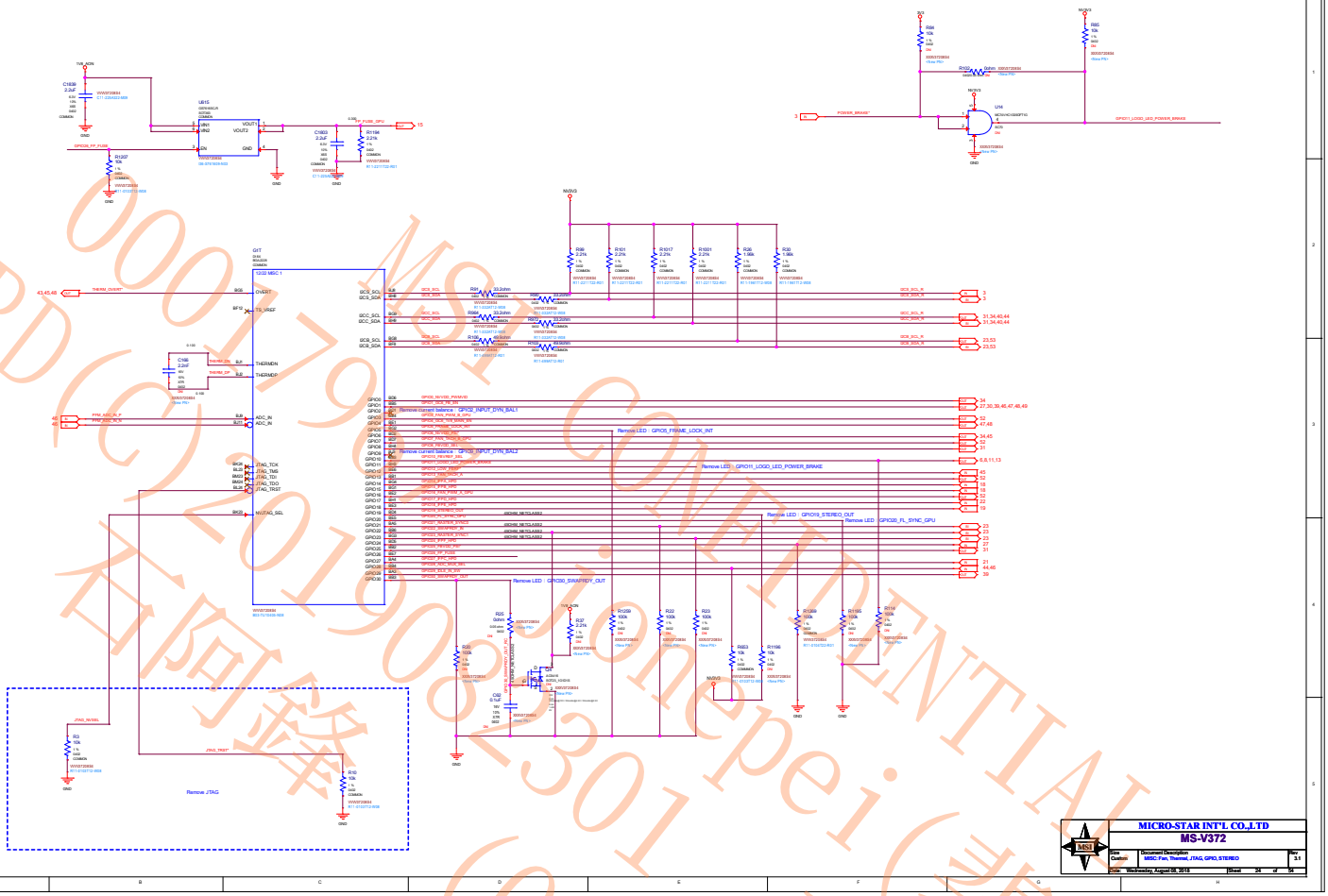
PAGE 24: MISC: Fan, Thermal, JTAG, GPIO, STEREO



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PAGE 25: MISC: ROM, Straps

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]		
L	L	L	00000	RAMCFG TBD	
L	L	H	00001	RAMCFG TBD	DEFAULT
L	H	L	00010	RAMCFG TBD	
L	H	H	00011	RAMCFG TBD	
H	H	L	00110	RAMCFG TBD	
H	H	H	00111	RAMCFG TBD	

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

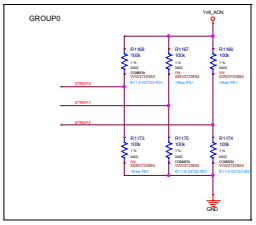
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	

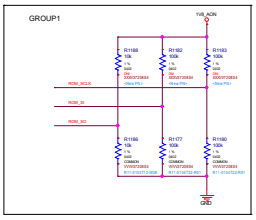
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

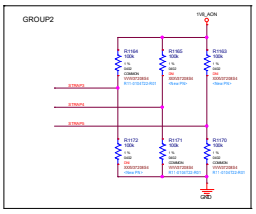
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

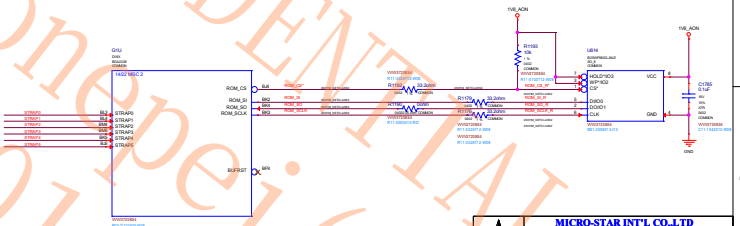
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE









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Size	Document Description	Rev
Custom	MISC: ROM, Straps	3.1
Date: Wednesday, August 08, 2018	Sheet 25 of 50	

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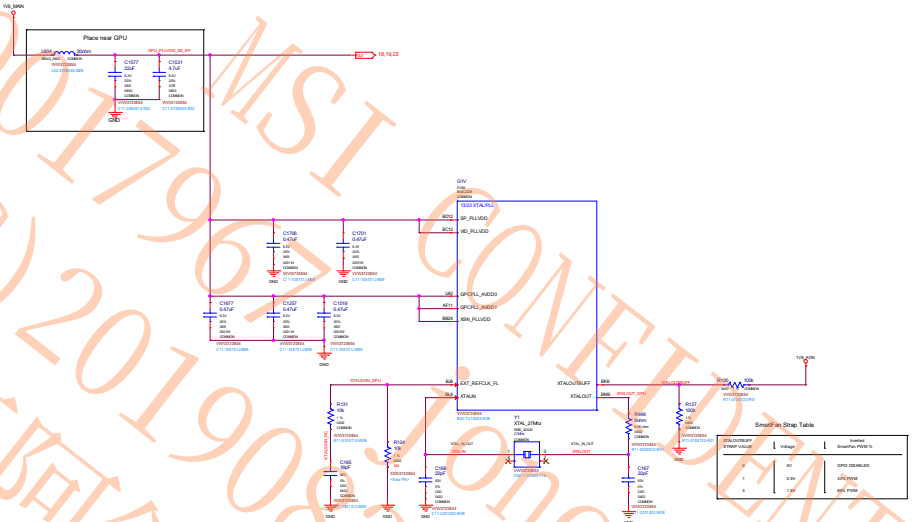

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(00068760)
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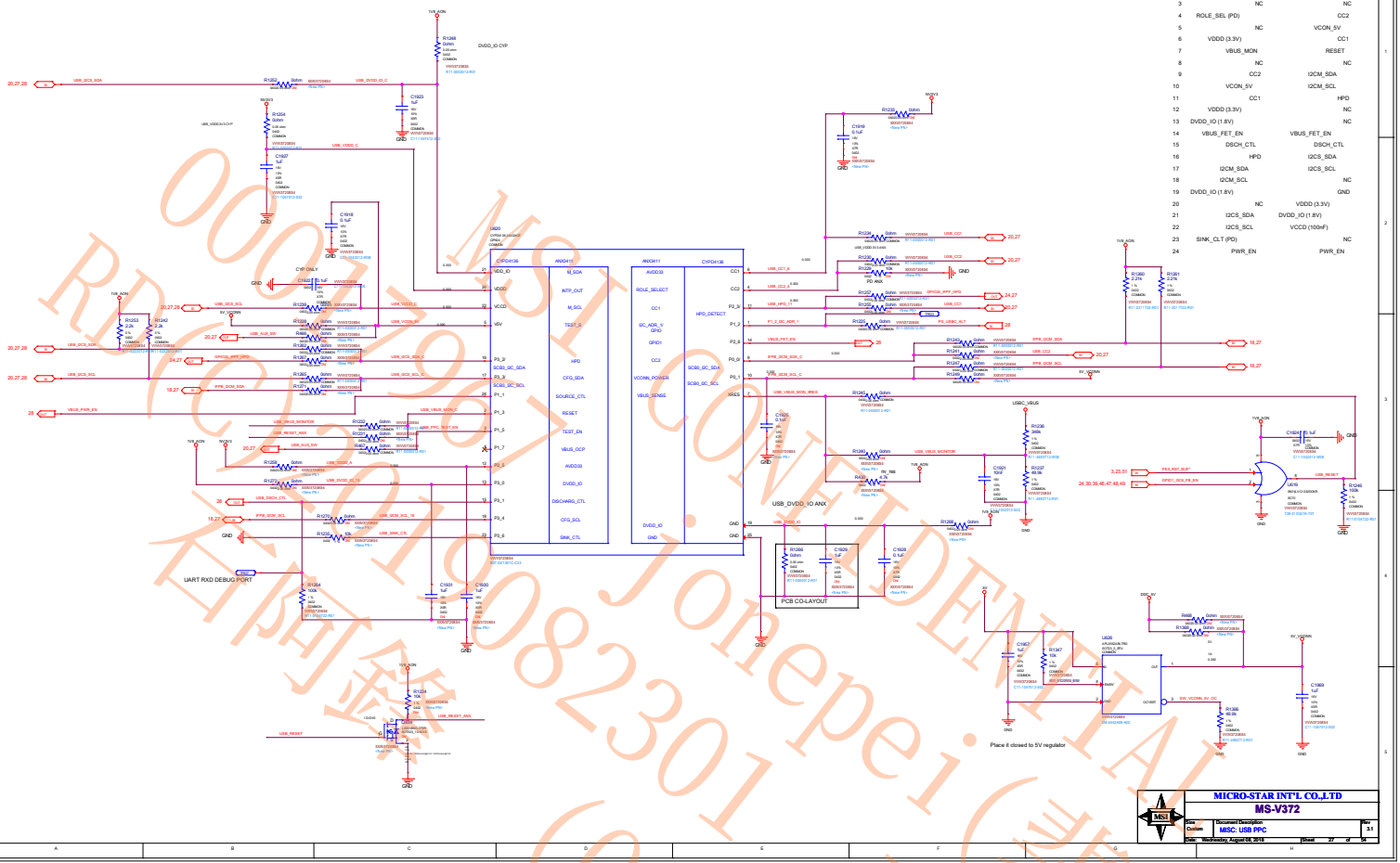
PAGE 27: MISC: USB PPC



PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN

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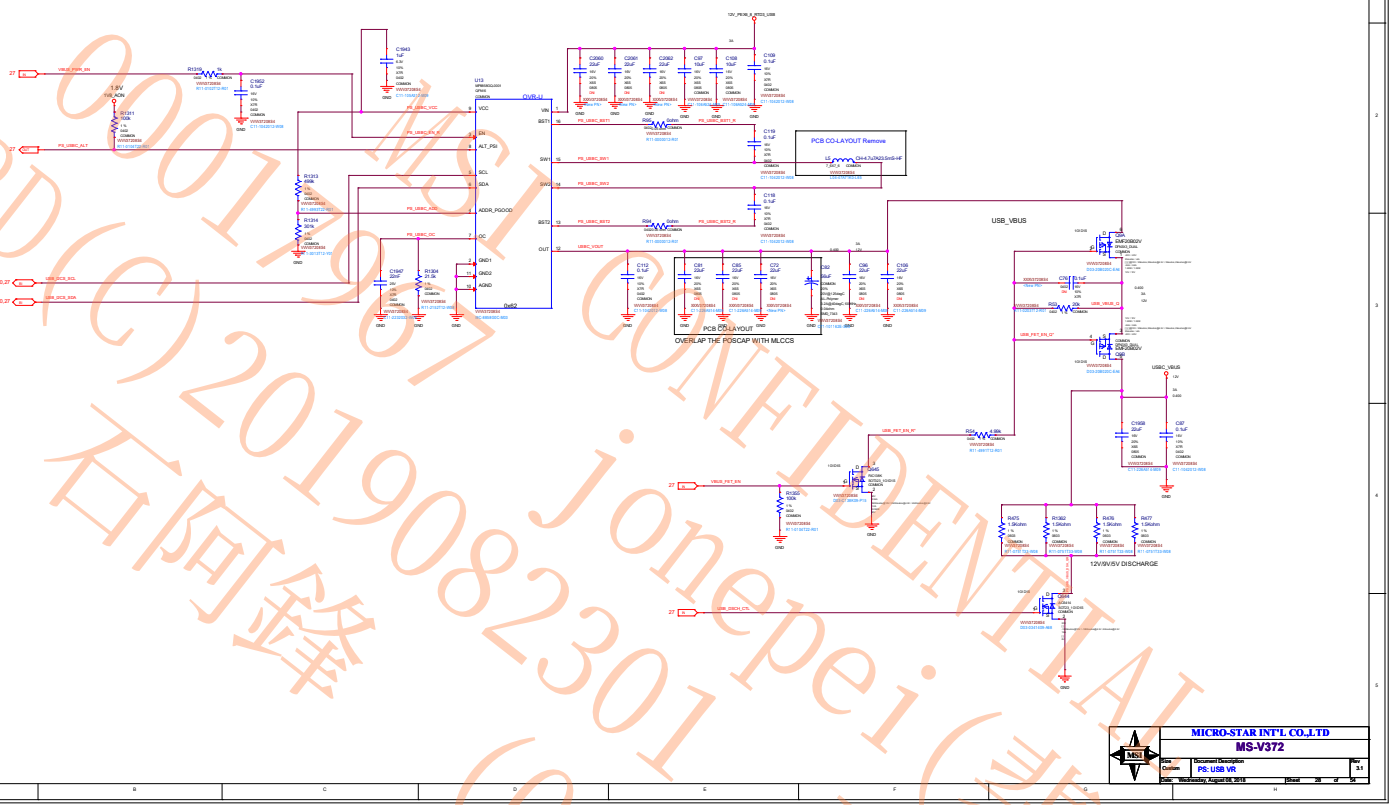
PAGE 28: PS: USB VR



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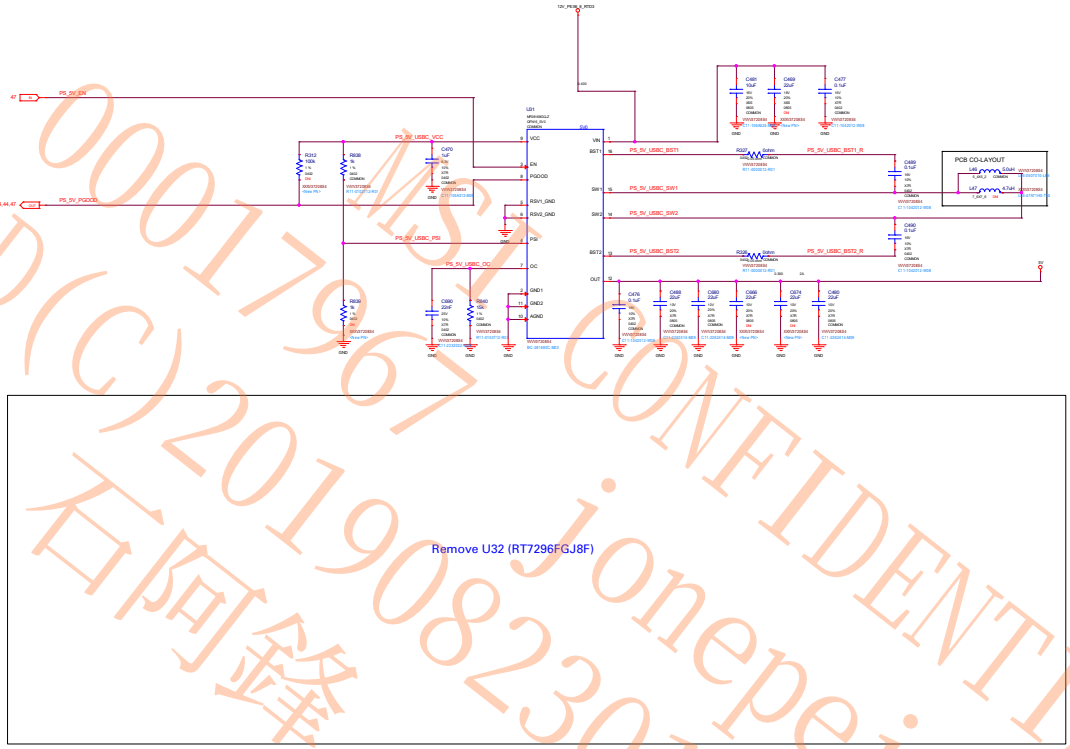
PAGE 29: PS: 5V, 5V_BACKUP



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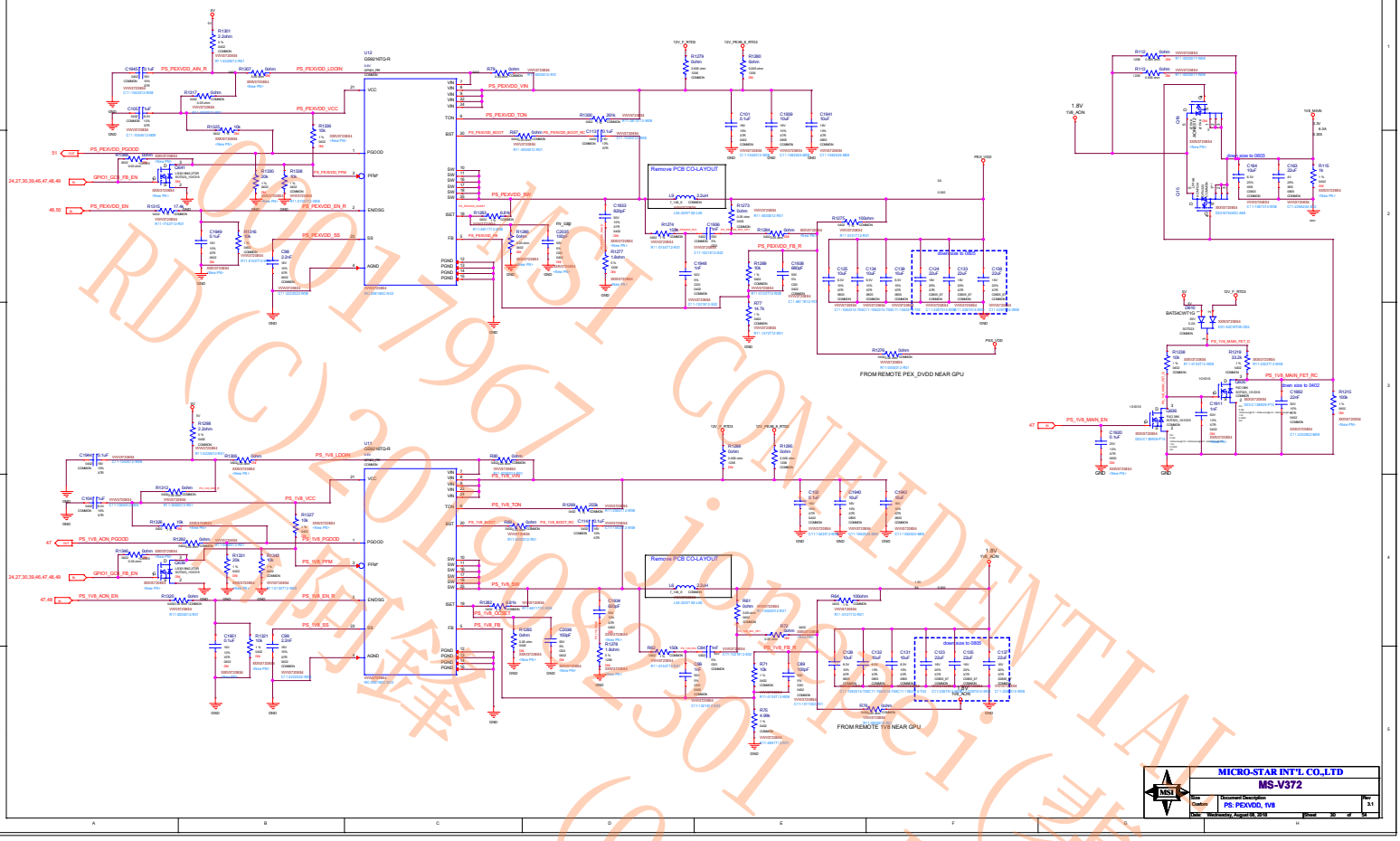
MS-V372

Size	Document Description	Rev
Custom	PS: 5V, 5V_BACKUP	3.1

Date: Wednesday, August 08, 2018 Sheet 29 of 54

PAGE 30: PS: PEXVDD, 1V8



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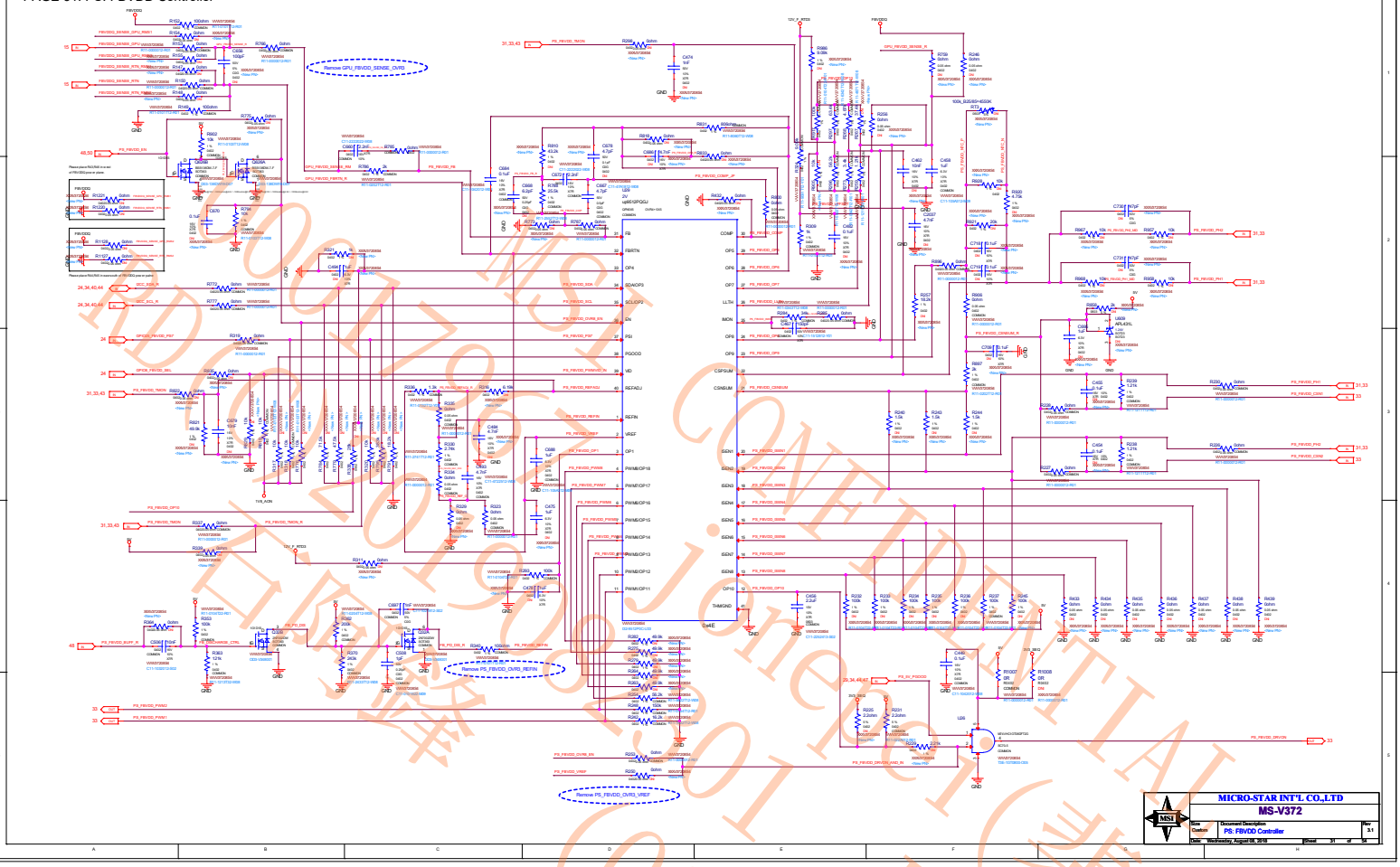
PAGE 31: PS: FBVDD Controller



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PAGE 32: PS: FBVDD Controller OVR3

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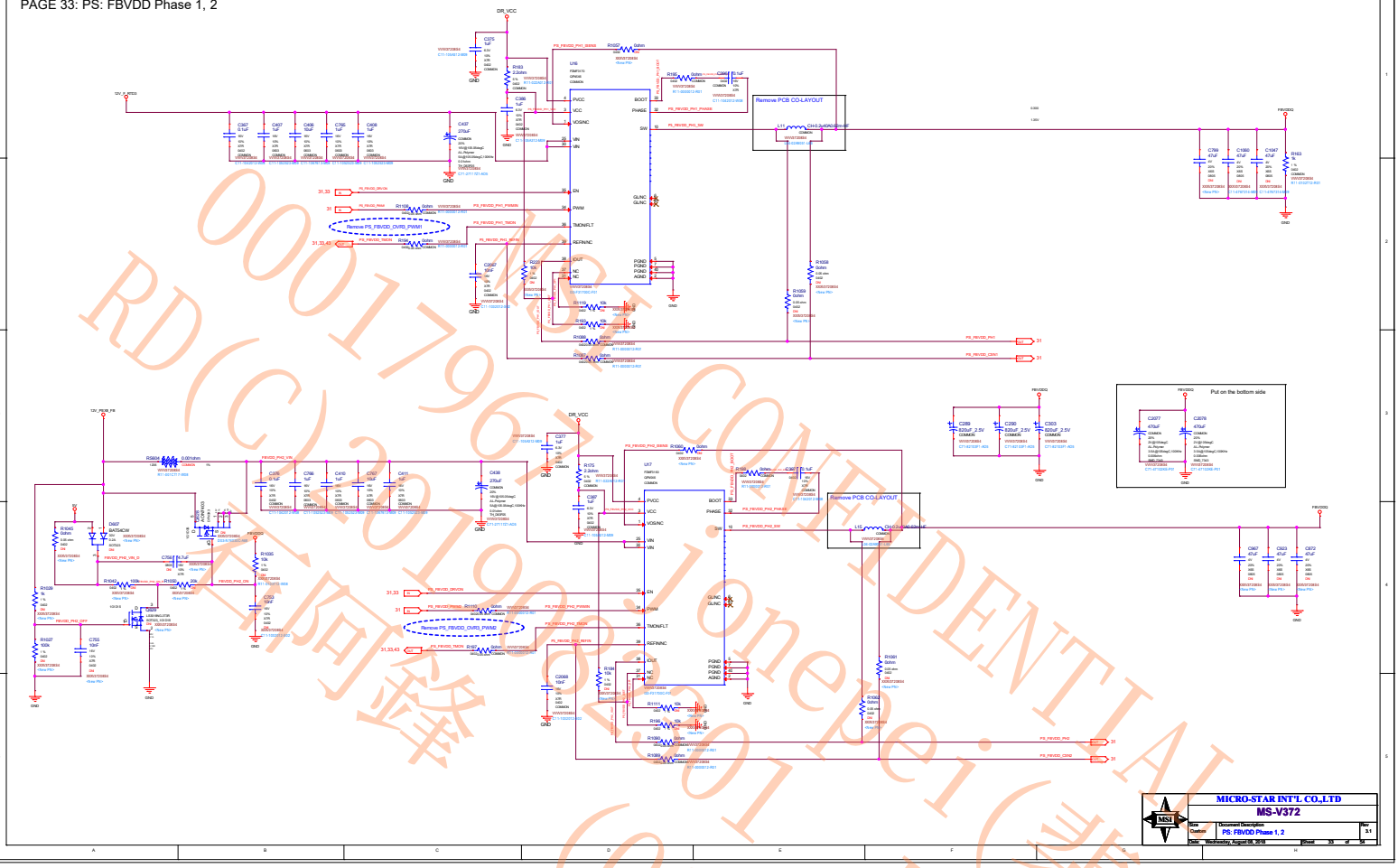
	MS-V372		
Size:	Document Description: PS: FBVDD Controller OVR3 (X)		Rev: 3.1
Date: Wednesday, August 08, 2018		Sheet 32 of 34	

PAGE 33: PS: FBVDD Phase 1, 2



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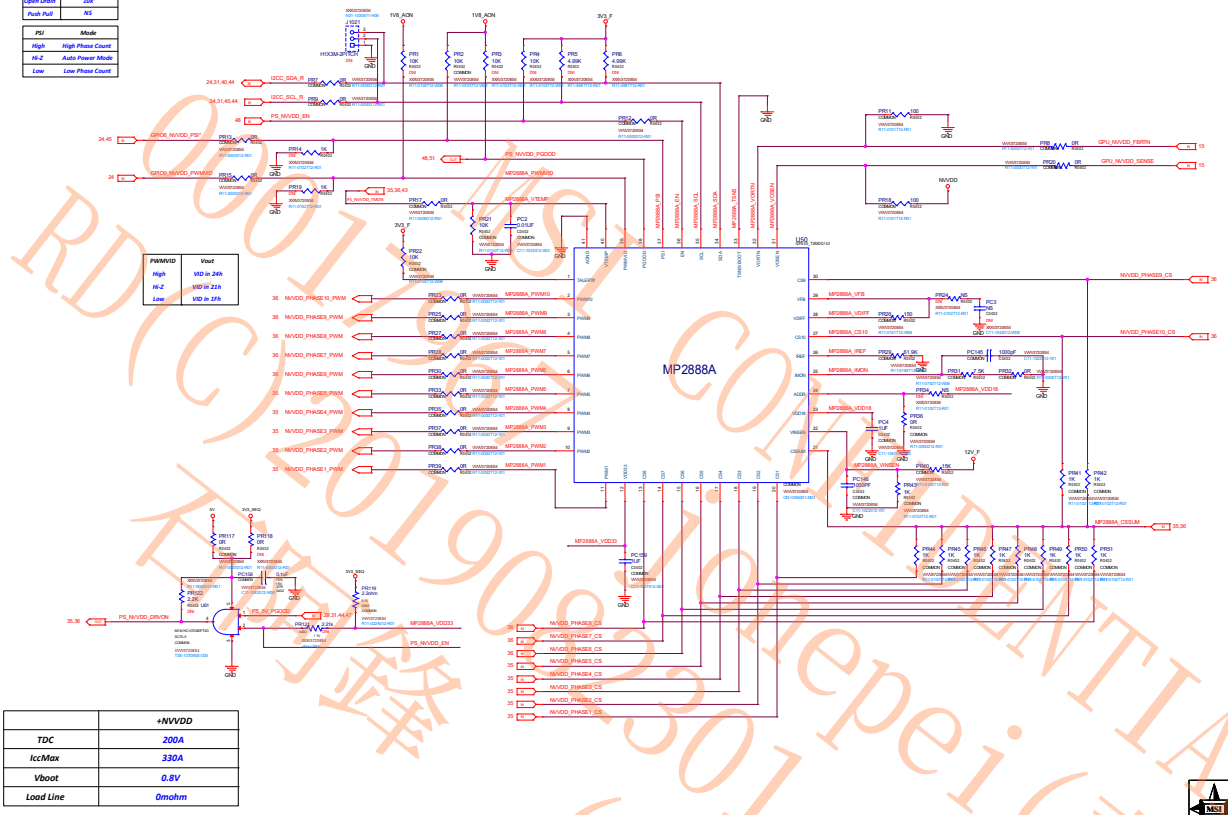
EN Type	R3
Open Drain	10k
Push Pull	NS

PSI	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count

PWMVID	Vout
High	VID in 24h
Hi-Z	VID in 21h
Low	VID in 1Fh



	+NVVDD
TDC	200A
IccMax	330A
Vboot	0.8V
Load Line	0mohm

PMBus Address	Setting Point(V)	R_{upper} (kΩ) 1%	R_{lower} (kΩ) 1%
20h	0	0	0
21h	0.031	3.32	0.059
22h	0.057	3.32	0.11
23h	0.084	3.32	0.162
24h	0.116	3.32	0.226
25h	0.156	3.32	0.316
26h	0.205	3.32	0.43
27h	0.266	3.32	0.576
28h	0.340	3.32	0.768
29h	0.430	3.32	1.05
2Ah	0.540	3.32	1.43
2Bh	0.675	3.32	2
2Ch	0.844	3.32	2.94
2Dh	1.048	3.32	4.64
2Eh	1.301	3.32	8.66
2Fh	1.500	3.32	16.5

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Size: Custom
Document Description: PS: NVVDD - MP2888A
Rev: 3.1
Date: Wednesday, August 08, 2018
Sheet 34 of 34

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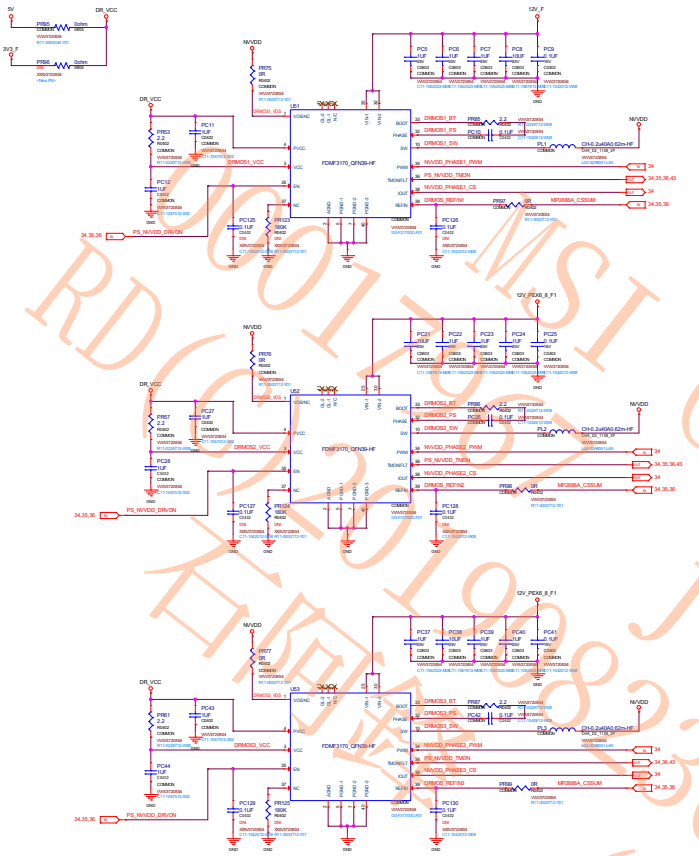
RD(C)20190823001 Jonepei(裴亮樂)
不可外傳 (00068760) RMA工程課

Page35: PS: NVVDD Phase 1-5



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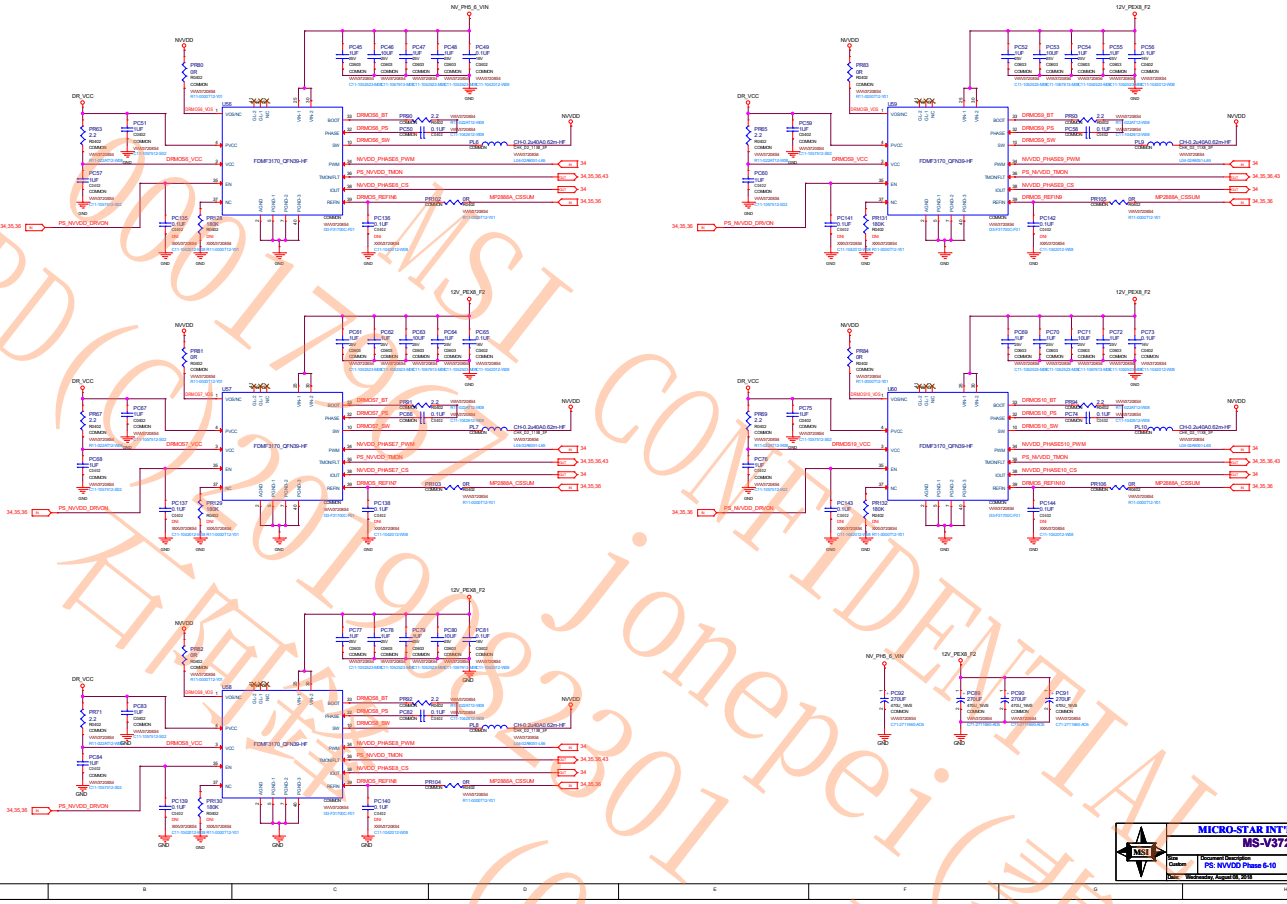
Size: Document Description: PS_NVVDD Phase 1-5
Rev: 3.1
Date: Wednesday, August 08, 2018 Sheet 35 of 54



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Size	Document Description	Rev
Custom	PS: NVVDD Phase 6-10	3.1

Date: Wednesday, August 08, 2018 Sheet 36 of 54

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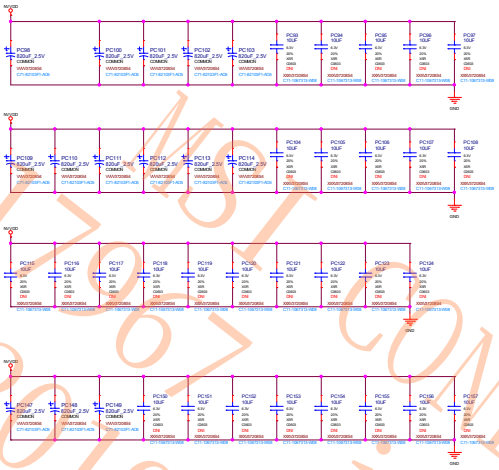
NVVDD Output CAP



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Size:	Document Description: PS: NVVDD Output CAP
Custom:	Rev: 3.1
Date: Wednesday, August 08, 2018	Sheet 37 of 54

PAGE 38: PS:NVVDD (X)

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Size	Document Description	Rev
Custom	PS:NVVDD (X)	3.1

Date: Wednesday, August 08, 2018 Sheet 38 of 54

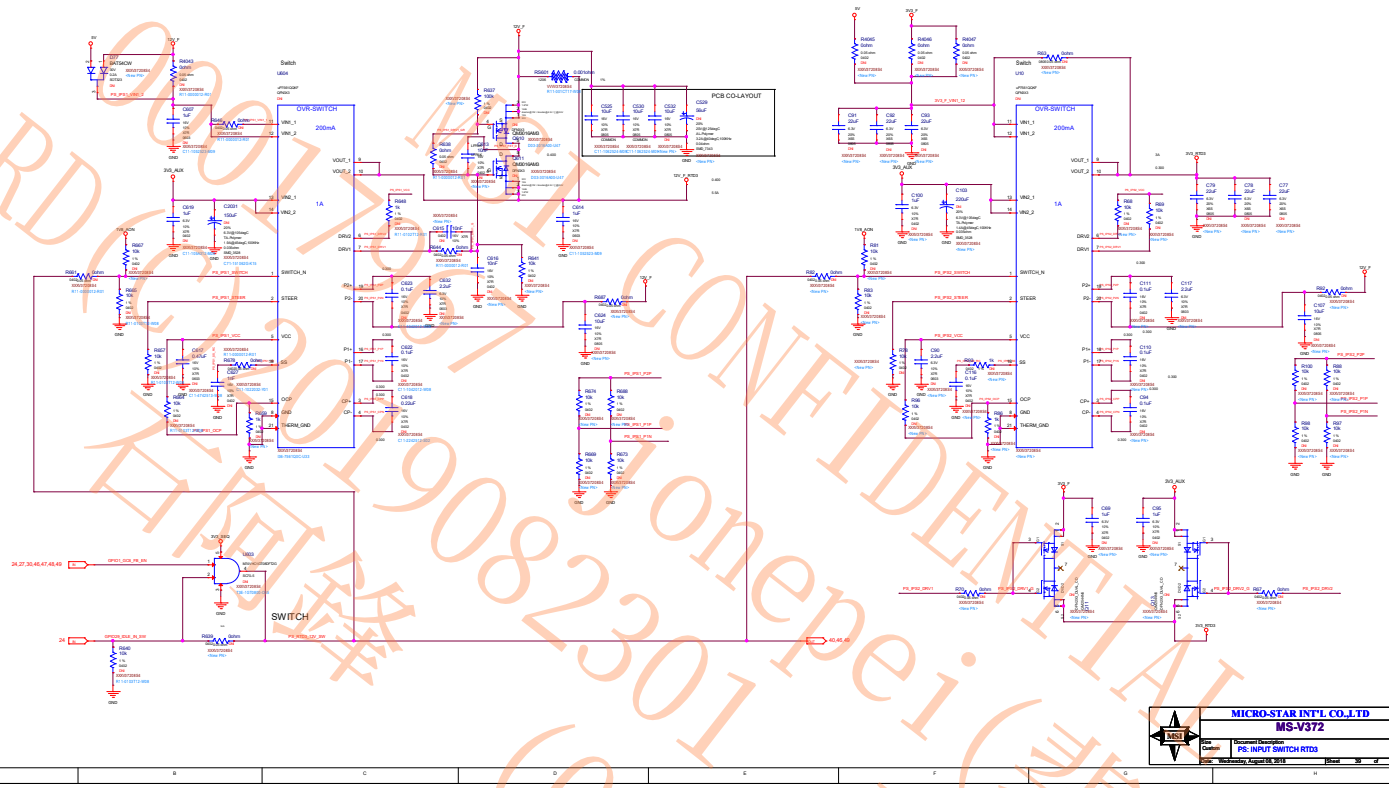
PAGE 39: PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A



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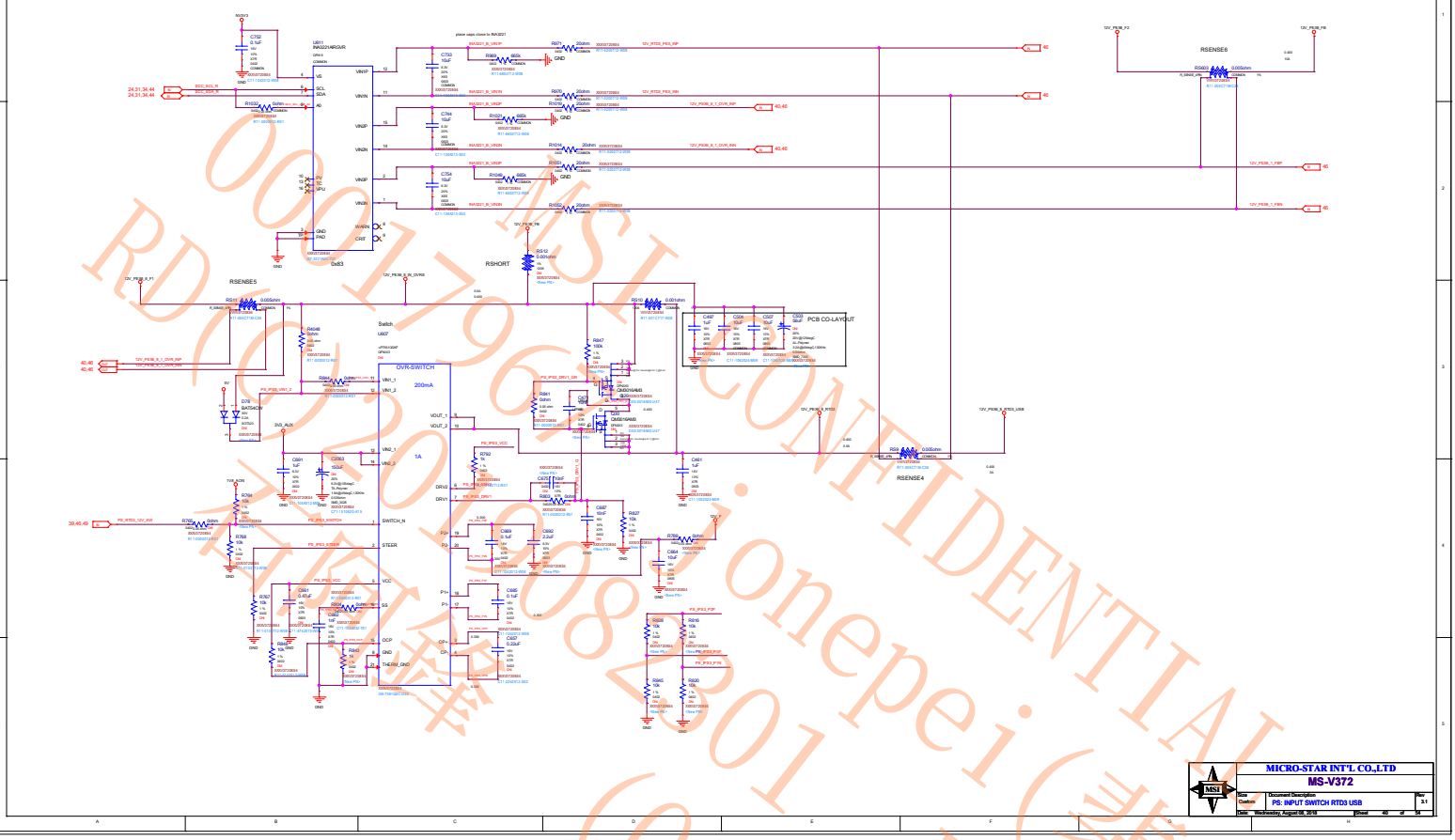
PAGE 40: PS: INPUT SWITCH RTD3 USB



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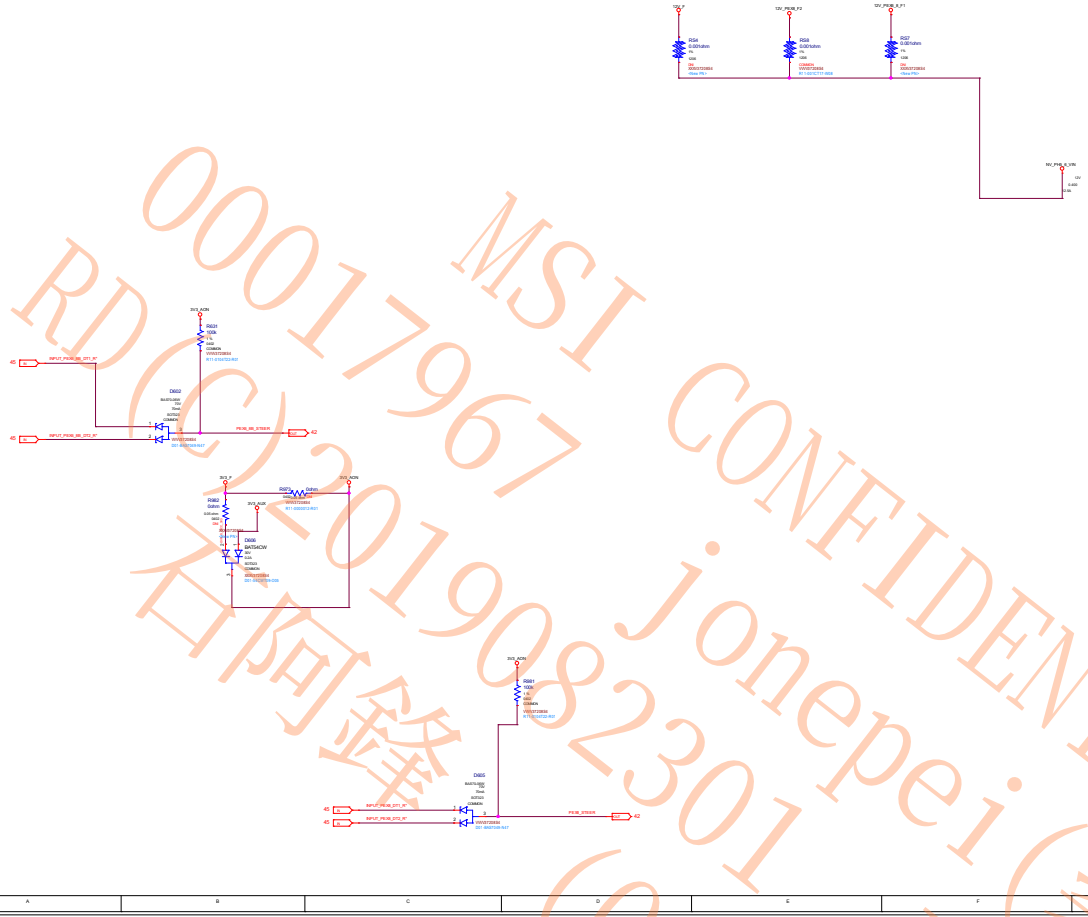
0001796 20160801
(00068760)
RMA工程課

PAGE 41: PS: INPUT SWITCH Rail Balance



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Size
Document Description
PS: INPUT SWITCH Rail Balance
Rev
3.1
Date: Wednesday, August 08, 2018
Sheet 41 of 54

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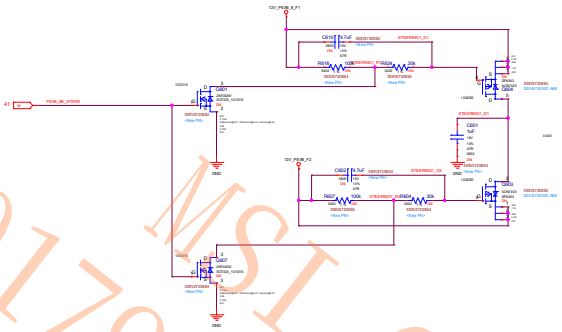
PAGE 42: PS: 12V CURRENT STEERING

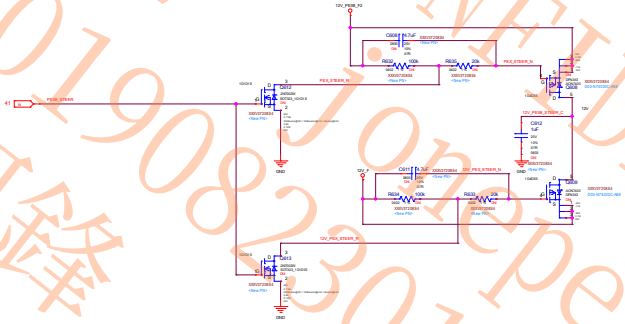
12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: PS: 12V CURRENT STEERING
Rev: 3.1	
Date: Wednesday, August 08, 2018	Sheet 42 of 56

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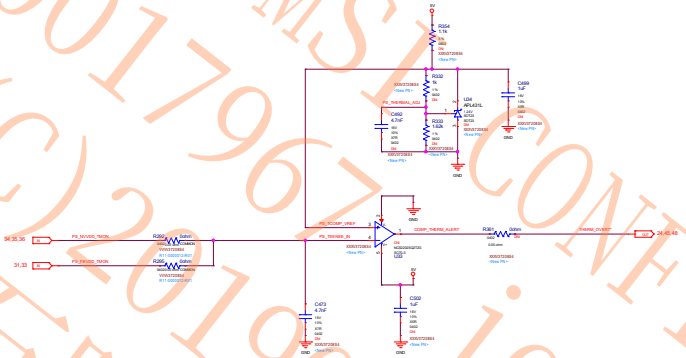
PAGE 43: PS: VR THERMAL PROTECTION



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Size Custom	Document Description PS: VR THERMAL PROTECTION	Rev 3.1
Date: Wednesday, August 08, 2018	Sheet 43 of 54	

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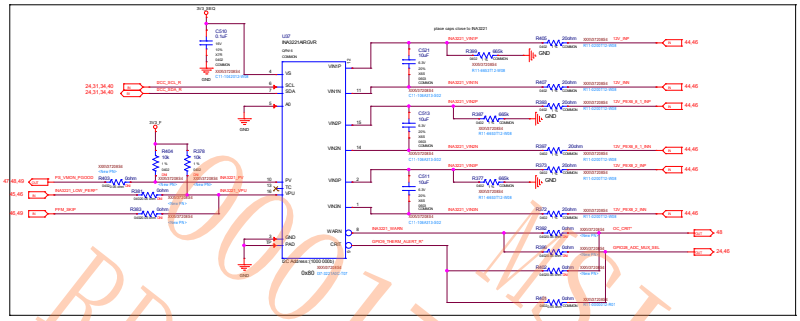
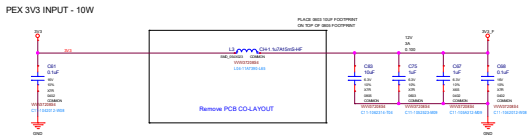
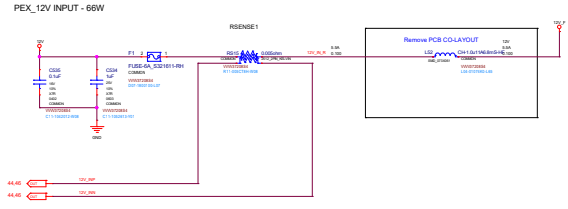
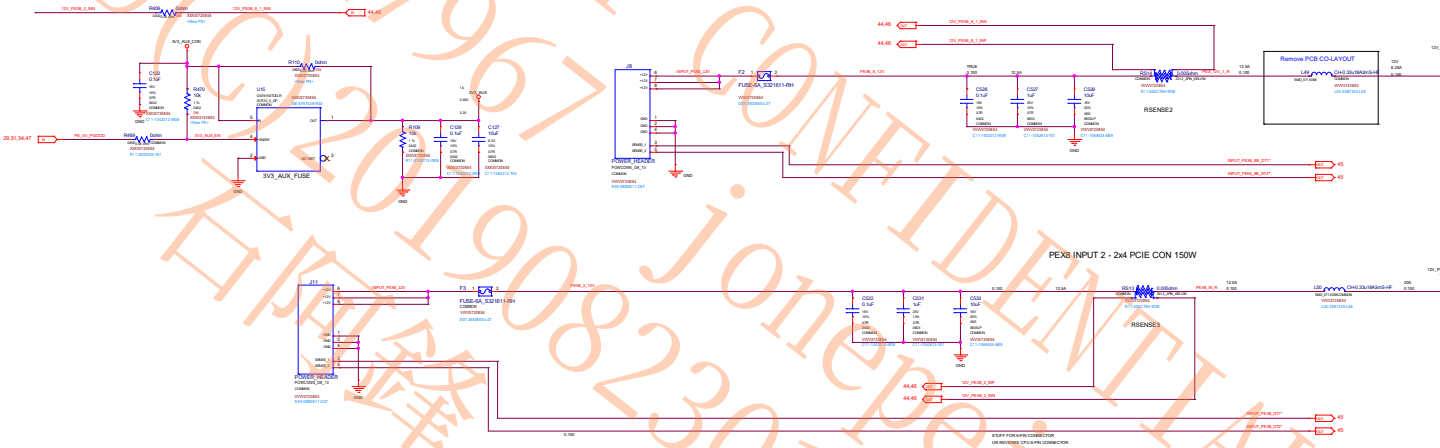
PAGE 44: PS: Inputs, Filtering, and Monitoring









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Size: Custom
Document Description: PS: Inputs, Filtering, and Monitoring
Rev: 3.1
Date: Wednesday, August 08, 2018
Sheet 44 of 55

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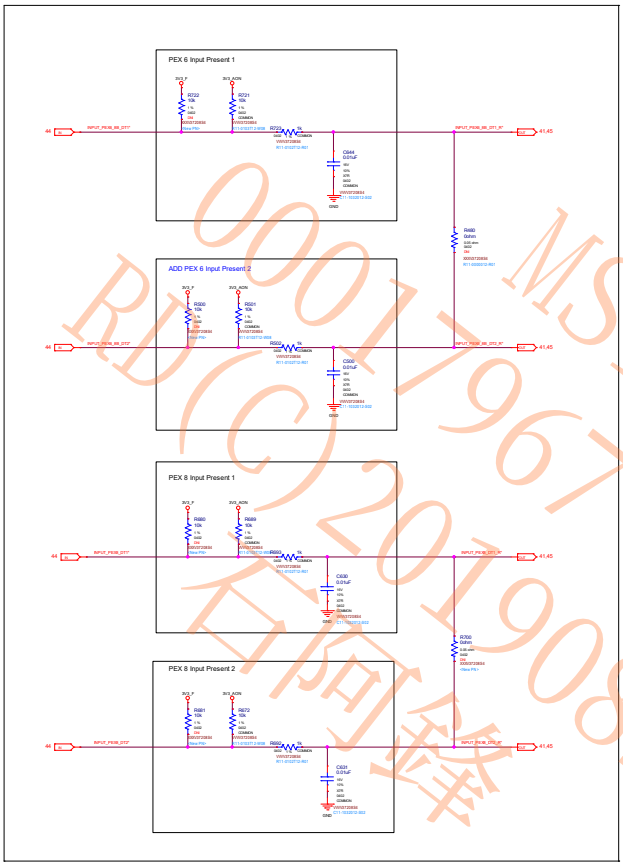
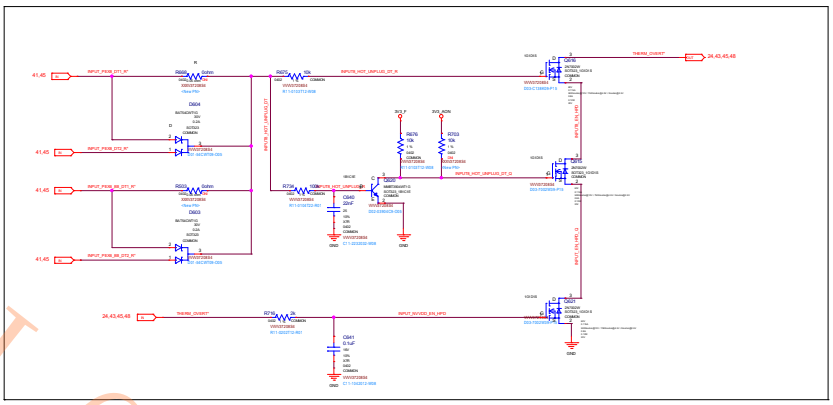
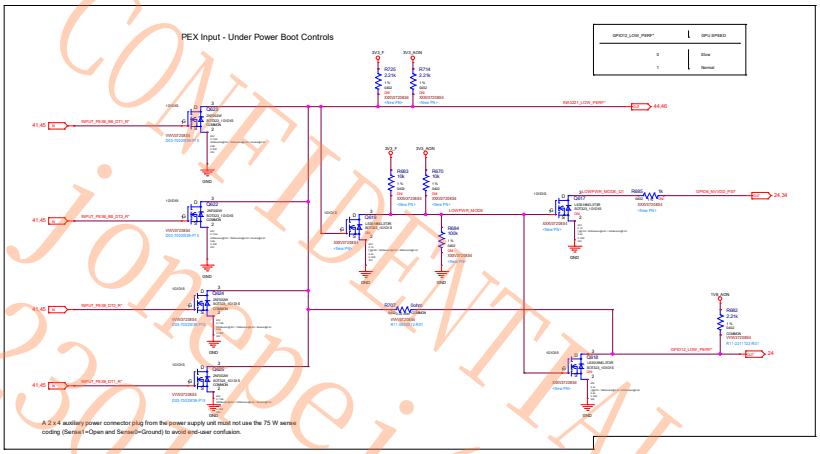
PAGE 45: PS: Current Steering, Hot Unplug Detect







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Size Custom	Document Description PS: Current Steering, Hot Unplug Detect	Rev 3.1
Date: Wednesday, August 08, 2018	Sheet 45 of 54	

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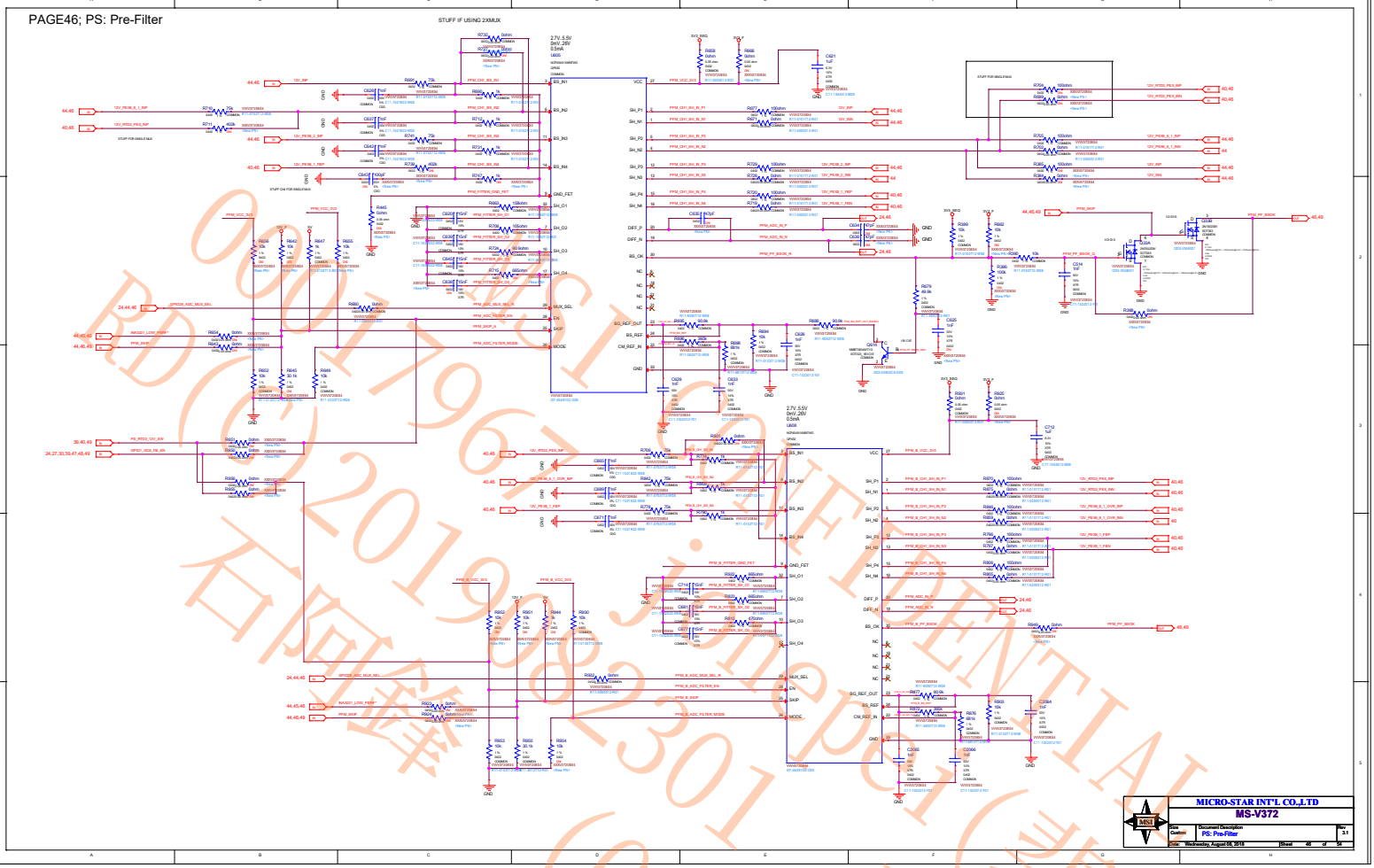

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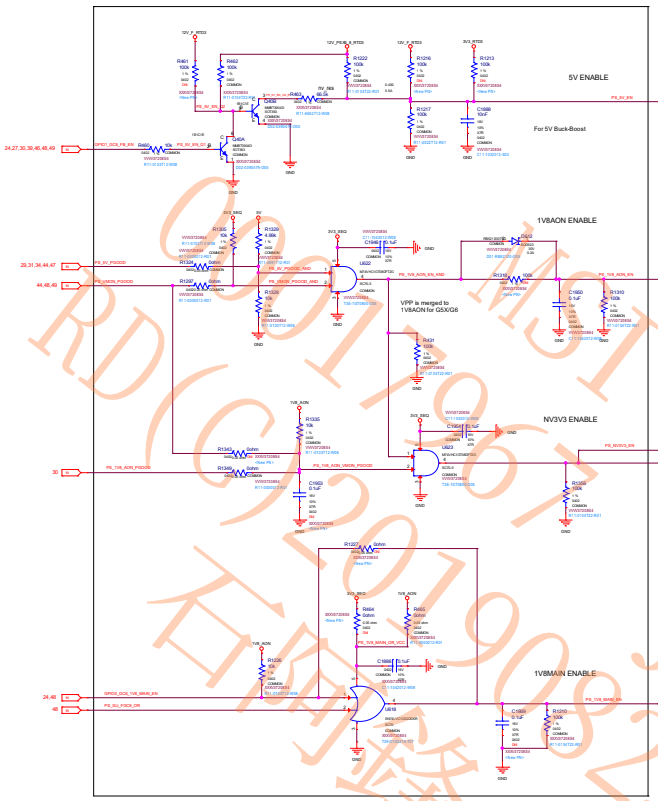
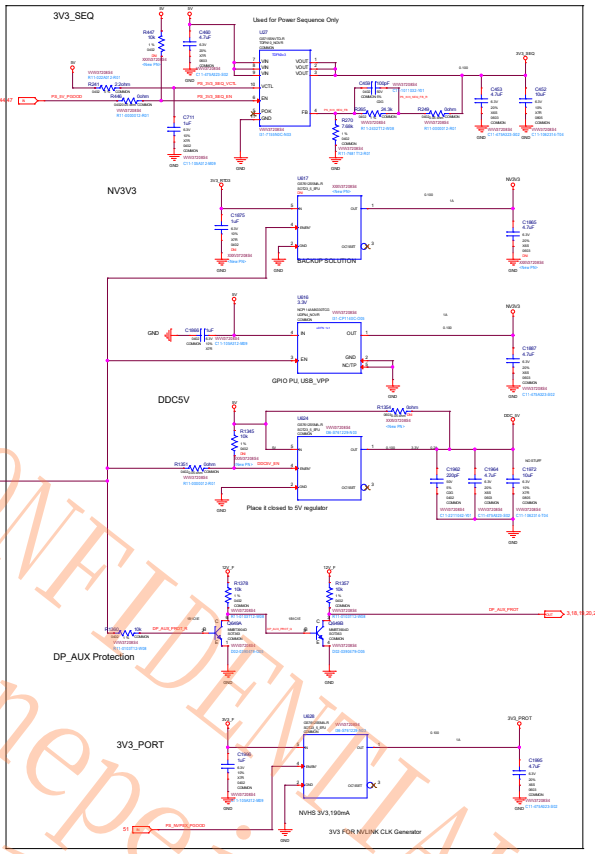
PAGE 47: SEQUENCE:5V,1V8,NV3V3 ENABLE





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MS-V372	
Size: Custom	Document Description: SEQUENCE:5V,1V8,NV3V3 ENABLE
Rev: 3.1	
Date: Wednesday, August 08, 2018	Sheet 47 of 55

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RD(G)2019082301 Jonepei(裴亮樂)
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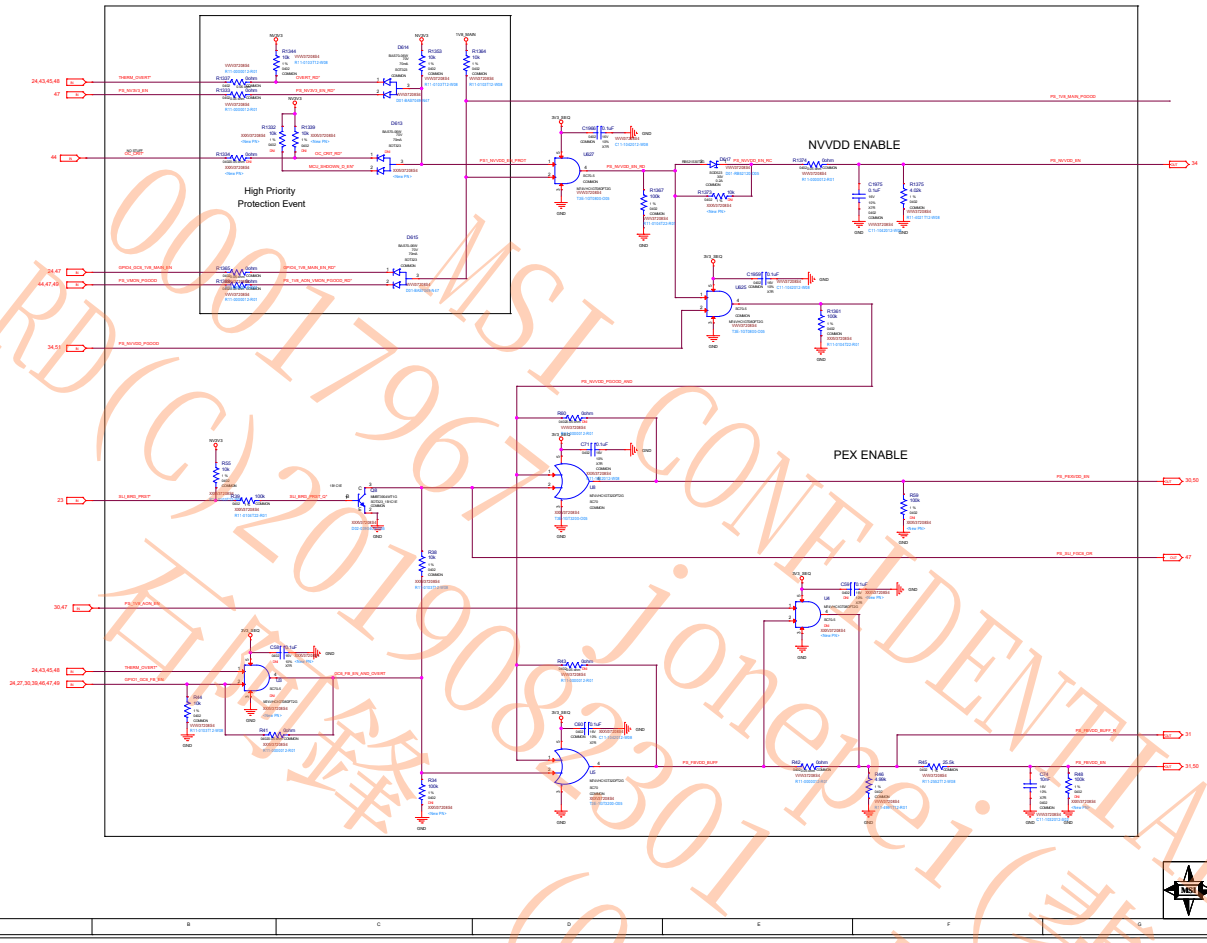
PAGE 48: SEQUENCE:NV,PEX,FB ENABLE



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MS-V372	
Size: Custom	Document Description: SEQUENCE:NV,PEX,FB ENABLE
Rev: 3.1	
Date: Wednesday, August 08, 2018	Sheet 48 of 54

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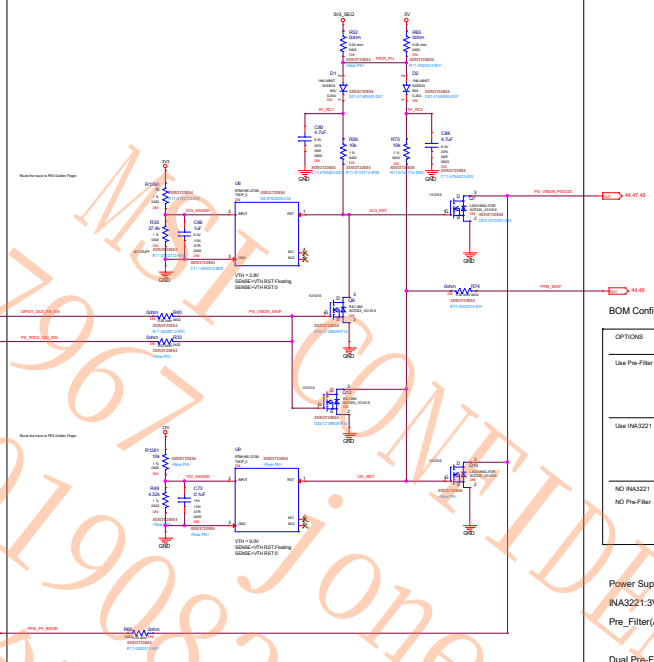
PCIE Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence.Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VIPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX

and All Input 12Vs

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Size	Document Description	Rev
Custom	SEQUENCE:PCIE VOLTAGE MONITOR	3.1

Date: Wednesday, August 08, 2018 Sheet 49 of 54

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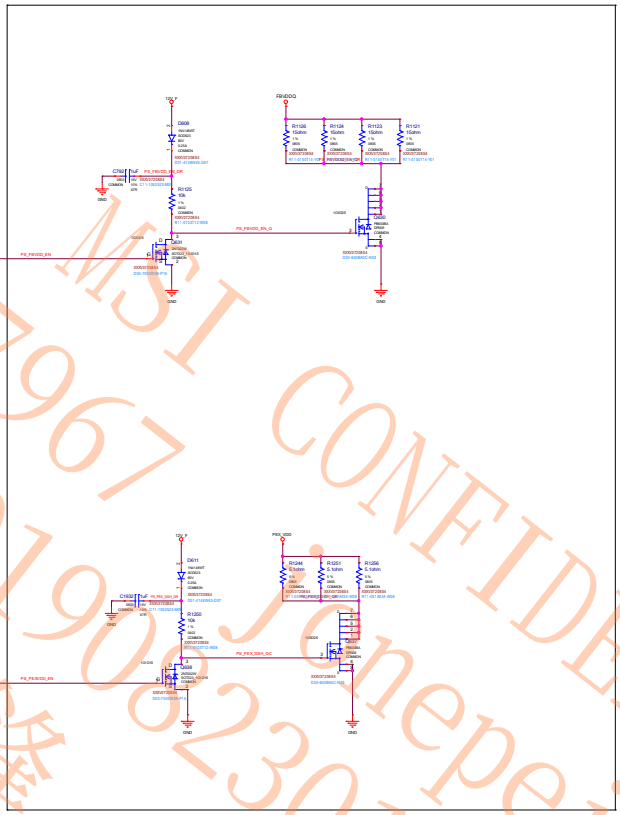
PAGE 50: SEQUENCE:DISCHARGE



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Size: Custom	Document Description: SEQUENCE:DISCHARGE	Rev: 3.1
Date: Wednesday, August 08, 2018	Sheet 50 of 50	

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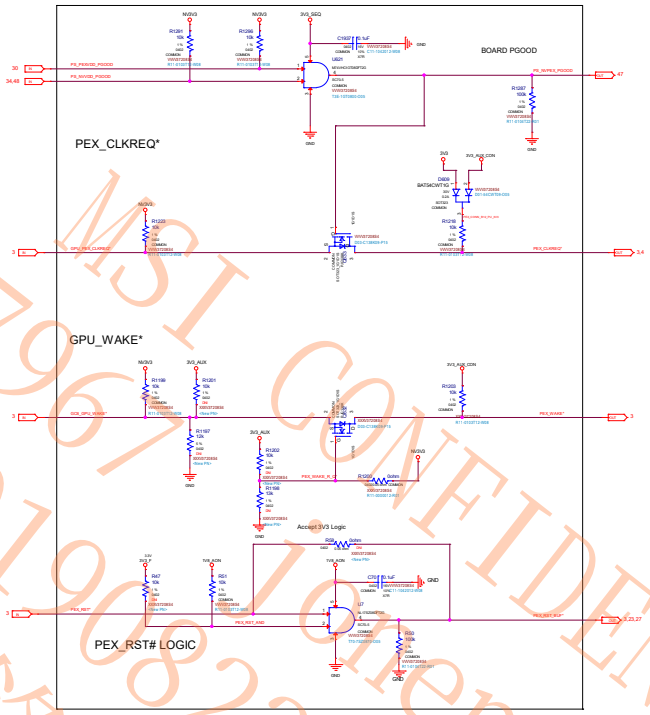

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Size:	Document Description: SEQUENCE:MISC
Custom	Rev: 3.1
Date: Wednesday, August 08, 2018	Sheet 51 of 54

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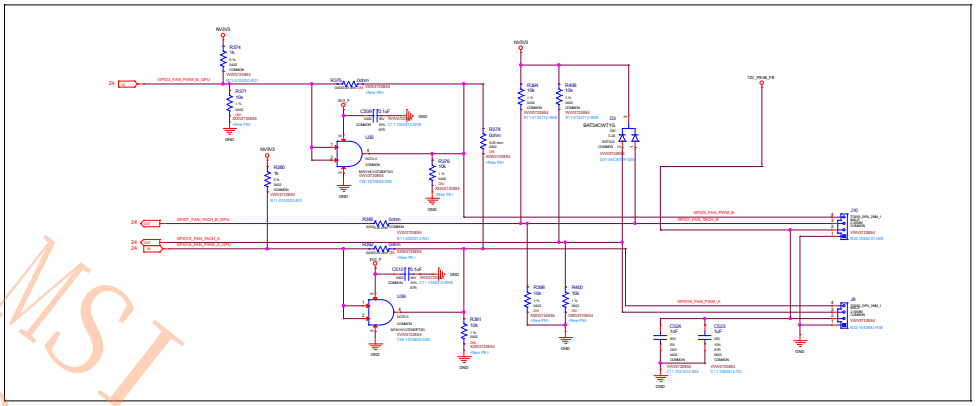
PAGE 52: LED & FAN HEADERS

Remove LED



Remove LED BOOST

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Size:	Document Description: LED & FAN HEADERS — Rev: 3.1
Custom:	
Date: Wednesday, August 08, 2018	Sheet 52 of 54

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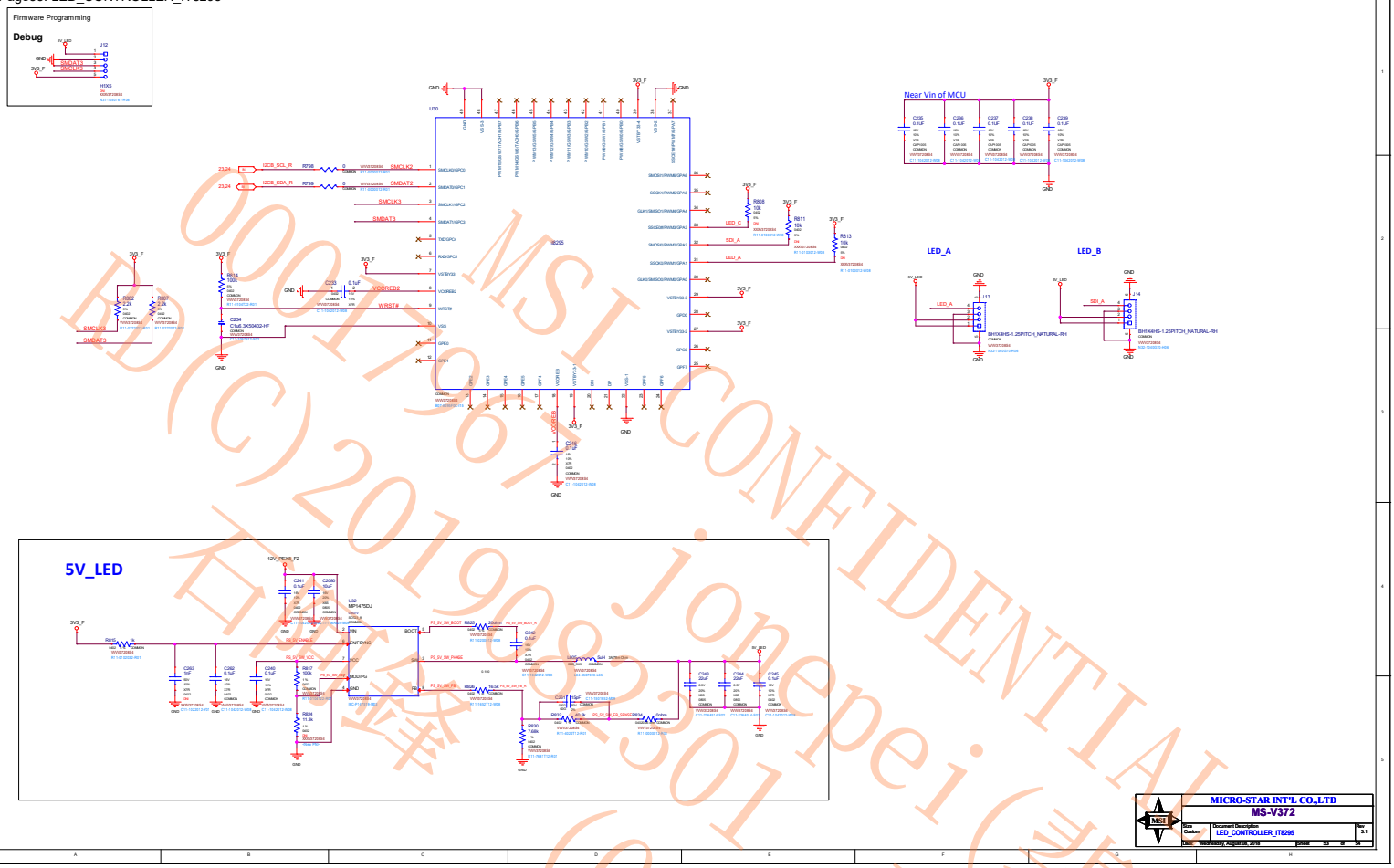
Page53: LED_CONTROLLER_IT8295



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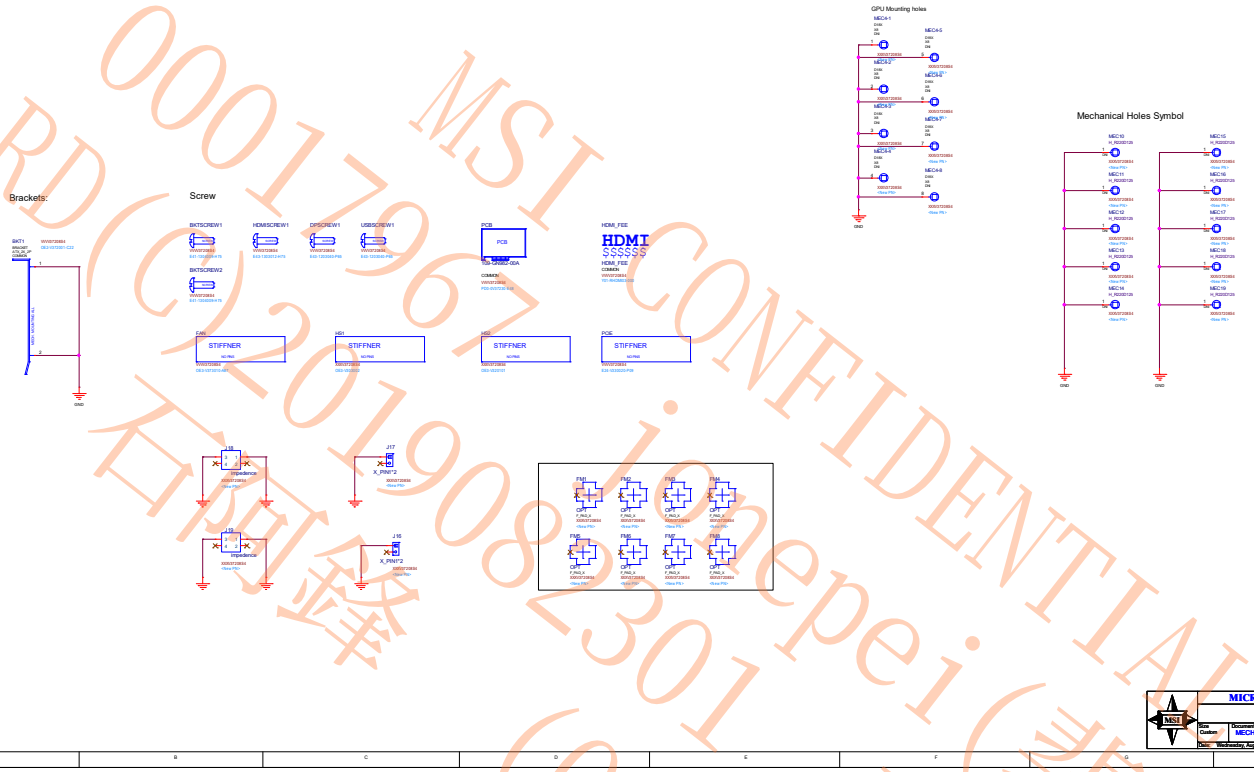
Size: Document Description: LED_CONTROLLER_IT8295 Rev: 3.1
Date: Wednesday, August 08, 2018 Sheet 53 of 54



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Custom:		
Date: Wednesday, August 08, 2018	Sheet 54 of 54	

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