PG180-A02

256b GDDR6 x16
TALL DP + DP + DP + HDMI/DP + USB

TABLE OF CONTENTS

Page	Description
1	Table of Contents
2	Block Diagram
3	PCI Express
4	PCI Termination
5	MEMORY: GPU Partition A/B
6	MEMORY: FBA Partition 31..0
7	MEMORY: FBA Partition 63..32
8	MEMORY: FBB Partition 31..0
9	MEMORY: FBB Partition 63..32
10	MEMORY: GPU Partition C/D
11	MEMORY: FBC Partition 31..0
12	MEMORY: FBC Partition 63..32
13	MEMORY: FBD Partition 31..0
14	MEMORY: FBD Partition 63..32
15	GPU PWR and GND
16	GPU Decoupling
17	GPU DECOUPLING
18	IFPAB TALL-DP
19	IFPE DP
20	IFPF USBC
21	IFPC HDMI 2.0/DP
22	IFPD DP
23	NVHS INTERFACE
24	MISC: FAN,THERMAL,JTAG,GPIO,STEREO
25	MISC3: ROM, STRAPS
26	MISC: XTAL, PLL
27	MISC: USB PPC
28	PS: USB VR
29	PS: 5V, 5V BACKUP
30	PS: PEXVDD, 1V8
31	PS: FBVDD CONTROLLER
32	PS: FBVDD CONTROLLER OVR3
33	PS: FBVDD PHASE 1, 2
34	PS: NVVDD CONTROLLER OVR8
35	PS: NVVDD Phase 1, 2
36	PS: NVVDD Phase 3, 4
37	PS: NVVDD Phase 5, 6
38	PS: NVVDD Phase 7, 8
39	PS: INPUT SWITCH RTD3
40	PS: INPUT SWITCH RTD3 USB
41	PS: INPUT SWITCH RAIL BALANCE
42	PS: 12V CURRENT STEERING
43	PS: VR THERMAL PROTECTION
44	PS: INPUTS, FILTERING AND MONITORING
45	PS: CURRENT STEERING,HOT UNPLUG DETECT
46	PS: PRE-FILTER
47	SEQUENCE: 5V, 1V8, NV3V3 ENABLE
48	SEQUENCE: NV, PEX, FB ENABLE
49	SEQUENCE: PCIE VOLTAGE MONITOR
50	SEQUENCE: DISCHARGE
51	SEQUENCE: MISC
52	LED & FAN HEADERS
53	LED 2
54	Mechanical: Bracket/Thermal Solution

base on V372-02S change for D18 Z
1. P.23 remove SLI & BRIDGE_LED_VDD & SLI_BRG_PRST*
2. P.52 remove LED change FAN connector
3. P.53 remove LED
4. P.38&44 add FUSE
5. P.5~14 mem add <>
6. P.53 LED use V336-0D
7. P.32 remove
8. P.35~38 dual MOS
9. P.33 change dual MOS
10. P.43 remove
11. P.31 change to UP1666
12. P.21 remove colay DP

0727:

page 24: REMOVE GPIO29_IDLE_IN_SW
remove GPIO9_INPUT_DYN_BAL2

page 29: 12V_F RTD3 change to 12V_F

page 30: 12V_F RTD3 change to 12V_F

page 33: 12V_F RTD3 change to 12V_F
移除保護線路

page 39: remove INPUT SWITCH RTD3

page 40: remove INPUT SWITCH RTD3 USB

page 44: remove INA3221

page 46: remove PFM_SKIP net
remove PS_RTD3_12V_SW net

page 47: remove PS_VMON_PGOOD net
12V_F RTD3 change to 12V_F
remove 3V3_PORT
remove 3V3_RTD3 change to nv3v3

page 48: remove OC_CRIT* NET from ina3221
remove PS_VMON_PGOOD net

page 49: PCIE Voltage Monitor1

page 52: REMOVE VIN =>12V_PEX6_8_IN_OVRS

page 54: change GPU scrow holes to small size

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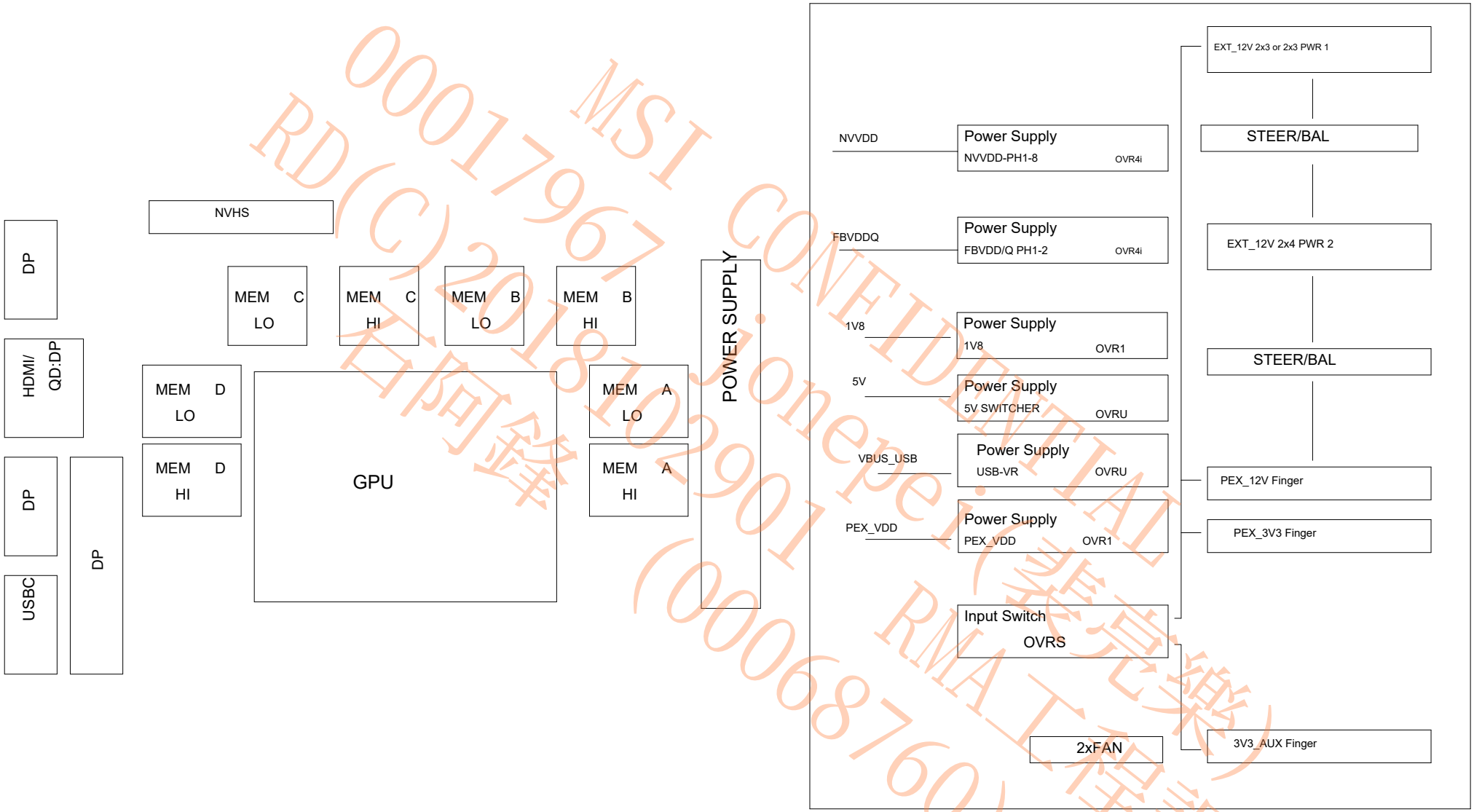
Size	Document Description	Rev
Custom	Page1:Table of Contents	7.1

Date: Tuesday, October 23, 2018 Sheet 1 of 54

Page2: Block Diagram



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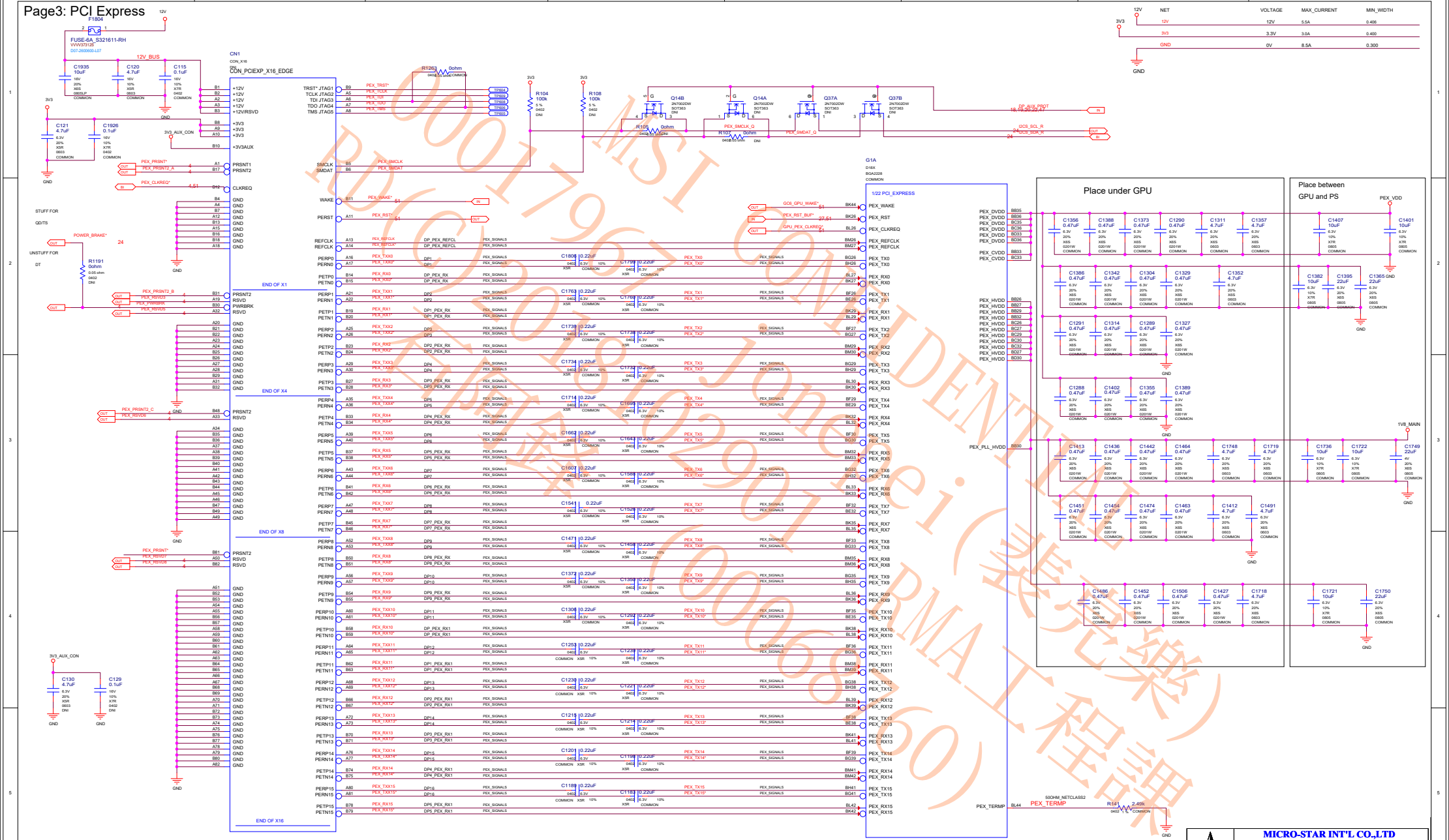
Size: Custom	Document Description: Page2:Block Diagram	Rev: 7.1
Date: Tuesday, October 23, 2018	Sheet 2 of 54	

Page3: PCI Express

NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
12V	12V	5.5A	0.406
3V3	3.3V	3.0A	0.400
GND	0V	8.5A	0.300



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Size	Document Description	Rev
Custom	Page3:PCI Express	7.1

Date: Tuesday, October 23, 2018 Sheet 3 of 54

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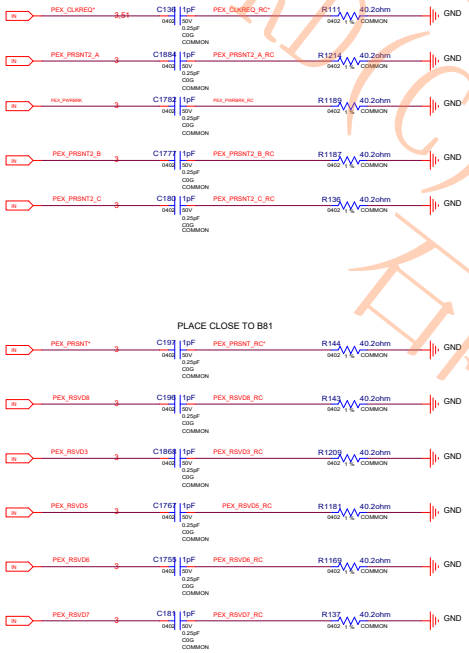
Page4: PCI Termination



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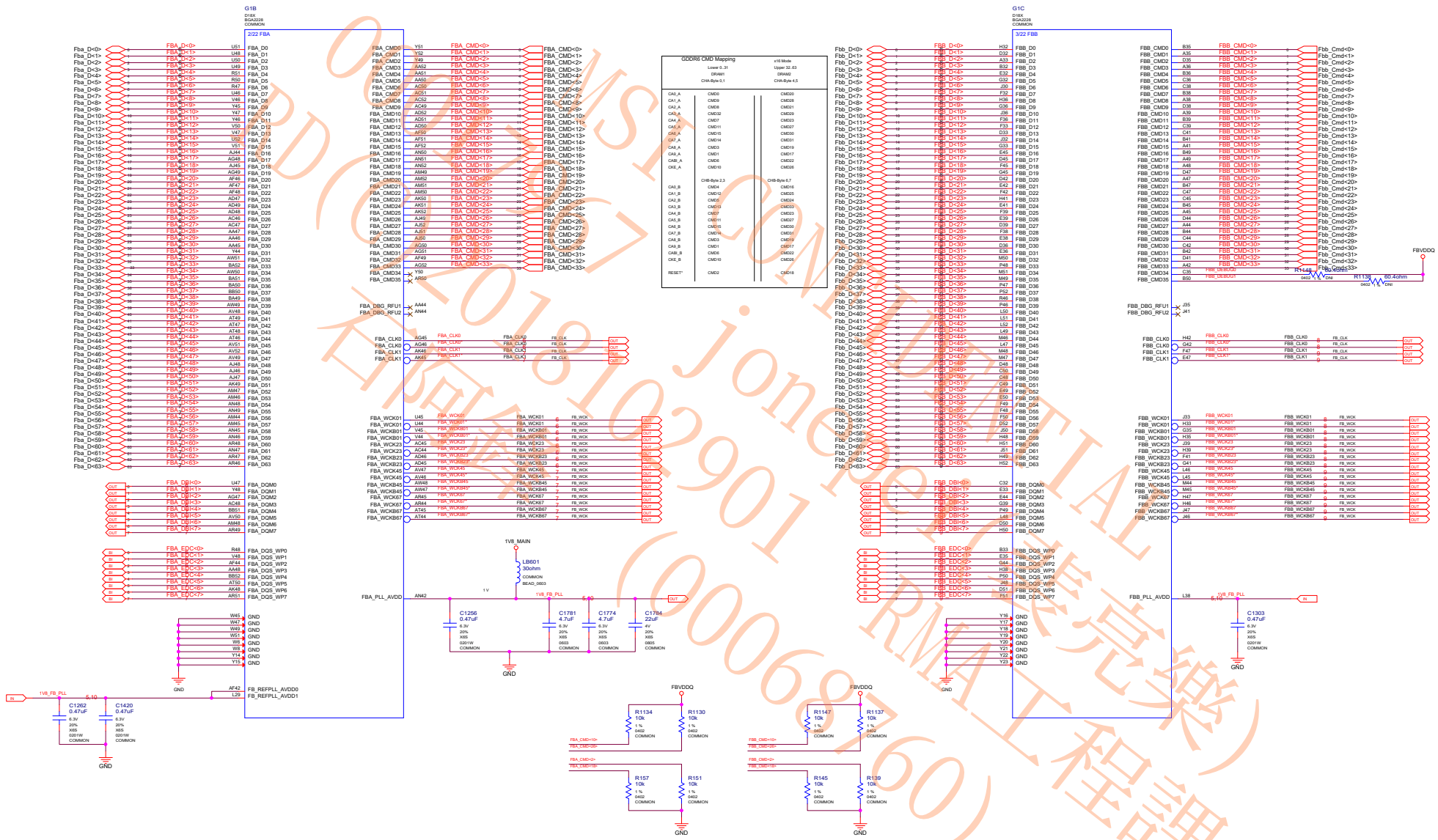
Size: Custom	Document Description: Page4:PCI Termination	Rev: 7.1
Date: Tuesday, October 23, 2018	Sheet 4 of 54	

Page5: MEMORY: GPU Partition A/B



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Size: Custom	Document Description: Page5:MEMORY_ GPU Partition A_B
Rev: 7.1	
Date: Tuesday, October 23, 2018	Sheet 5 of 54

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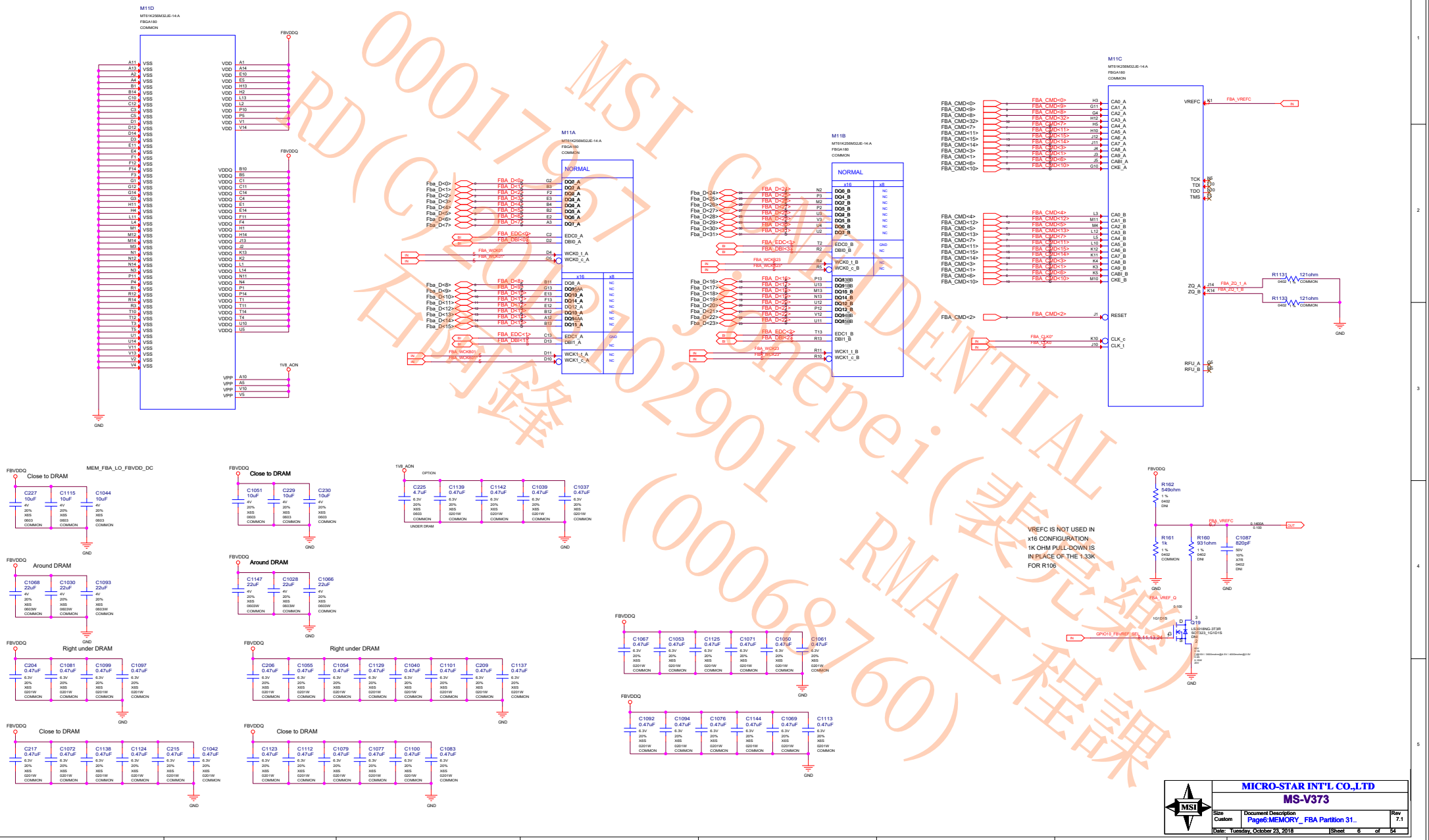
Page6: MEMORY: FBA Partition 31..0



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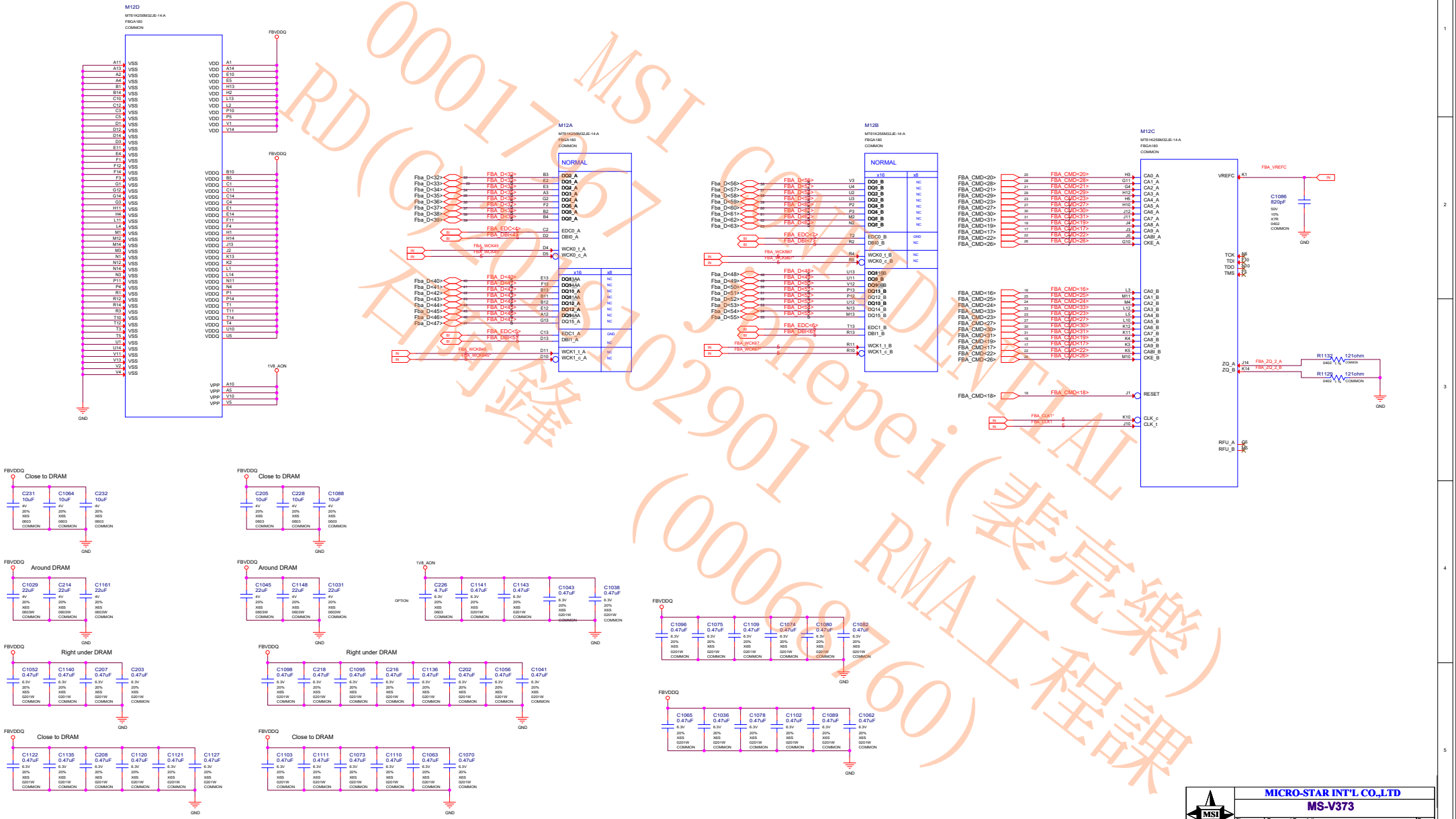
Page7: MEMORY: FBA Partition 63..32



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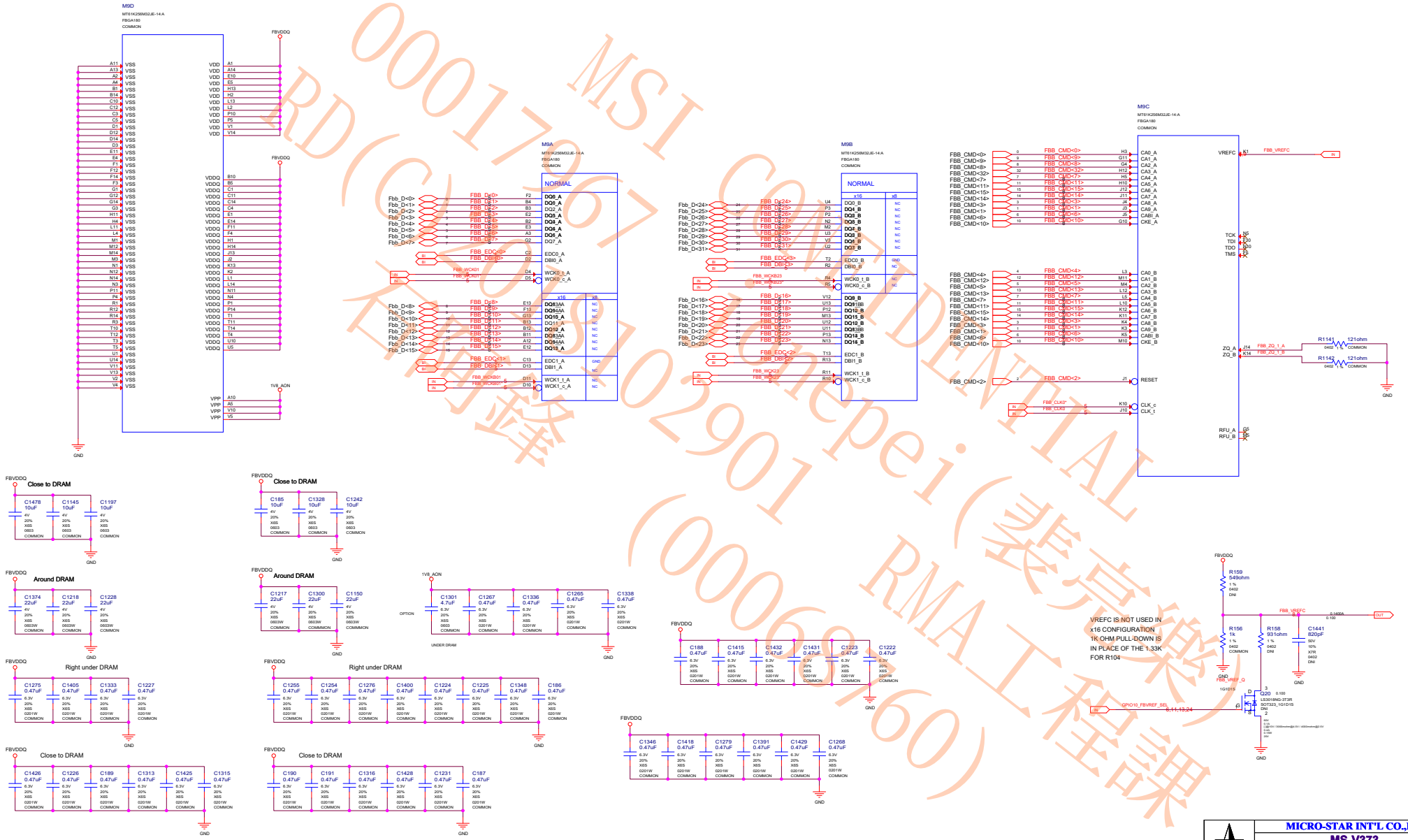
Size	Document Description	Rev
Custom	Page7:MEMORY_ FBA Partition 63..	7.1

Date: Tuesday, October 23, 2018 Sheet 7 of 54

Page8: MEMORY: FBB Partition 31..0



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Size: Custom	Document Description: Page8:MEMORY_ FBB Partition 31..
Rev: 7.1	
Date: Tuesday, October 23, 2018	Sheet 8 of 54

Page9: MEMORY: FBB Partition 63..32

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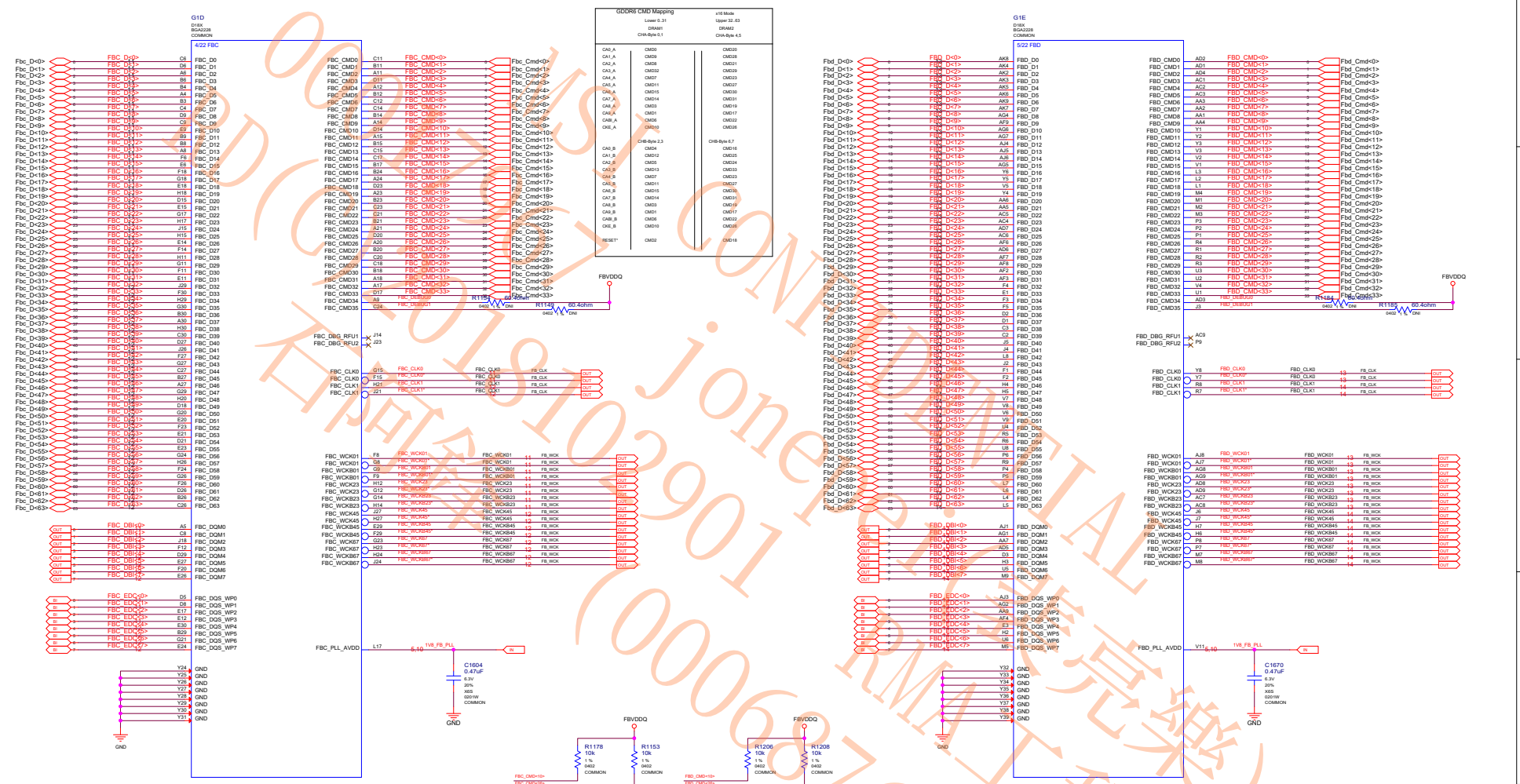
Size: Custom	Document Description: Page9:MEMORY_ FBB Partition 63..
Rev: 7.1	
Date: Tuesday, October 23, 2018	Sheet 9 of 54



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Size: Custom	Document Description: Page10:MEMORY_ GPU Partition C_D
Rev: 7.1	
Date: Tuesday, October 23, 2018	Sheet 10 of 54

Page11: MEMORY: FBC Partition 31..0

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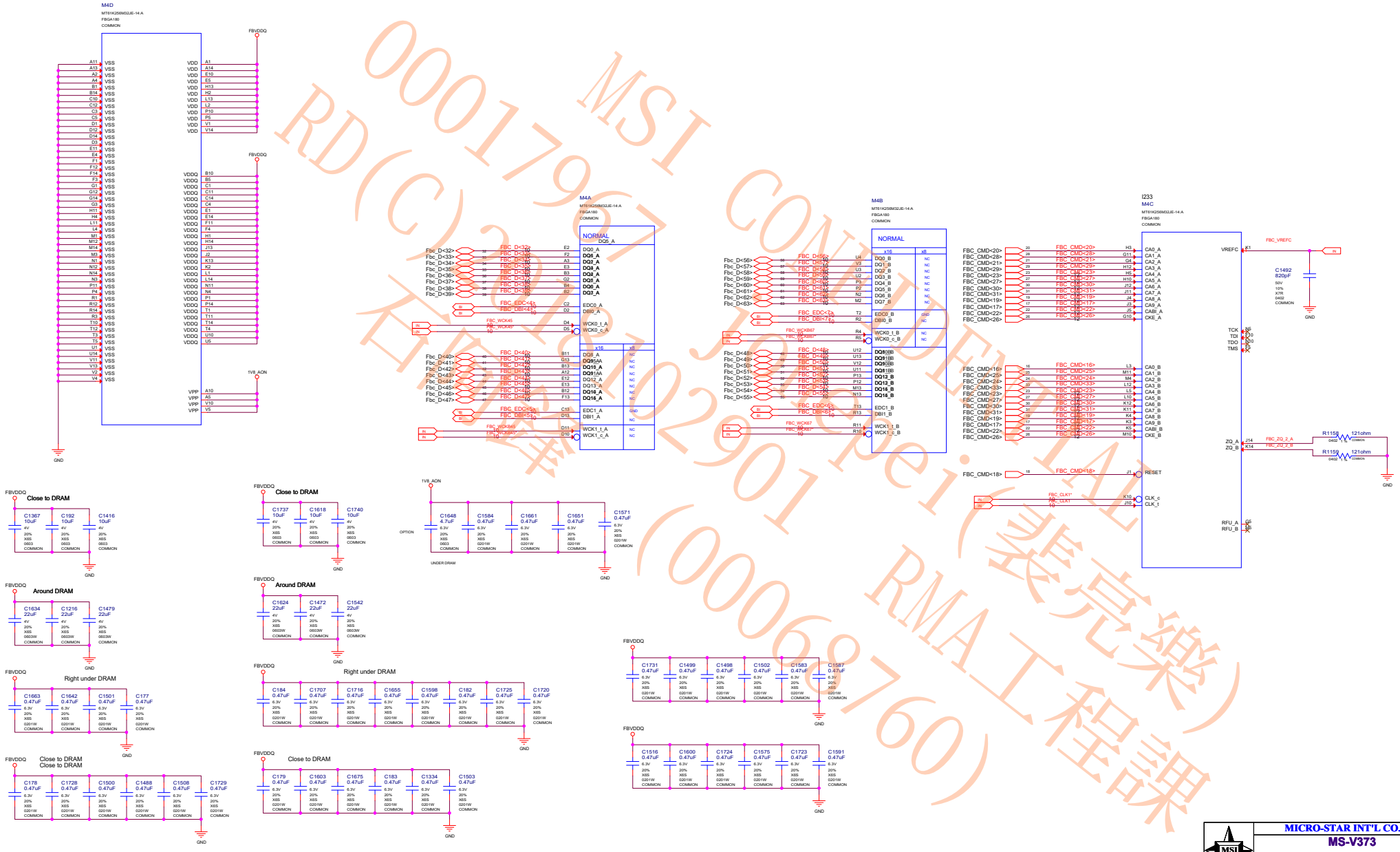
Page12: MEMORY: FBC Partition 63..32



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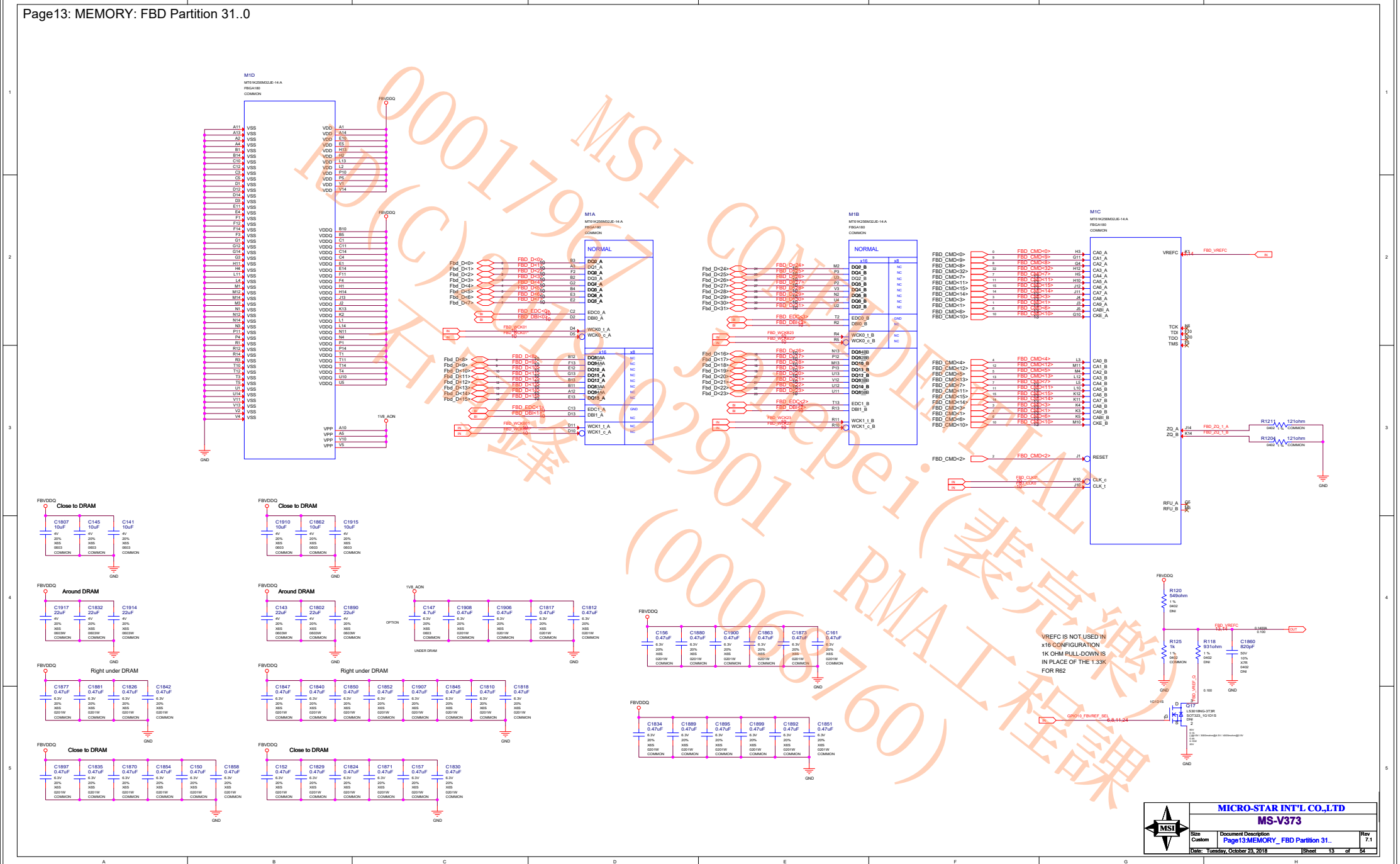
Size: Custom | Document Description: Page12:MEMORY_ FBC Partition 63.. | Rev 7.1

Date: Tuesday, October 23, 2018 | Sheet 12 of 54

Page13: MEMORY: FBD Partition 31..0



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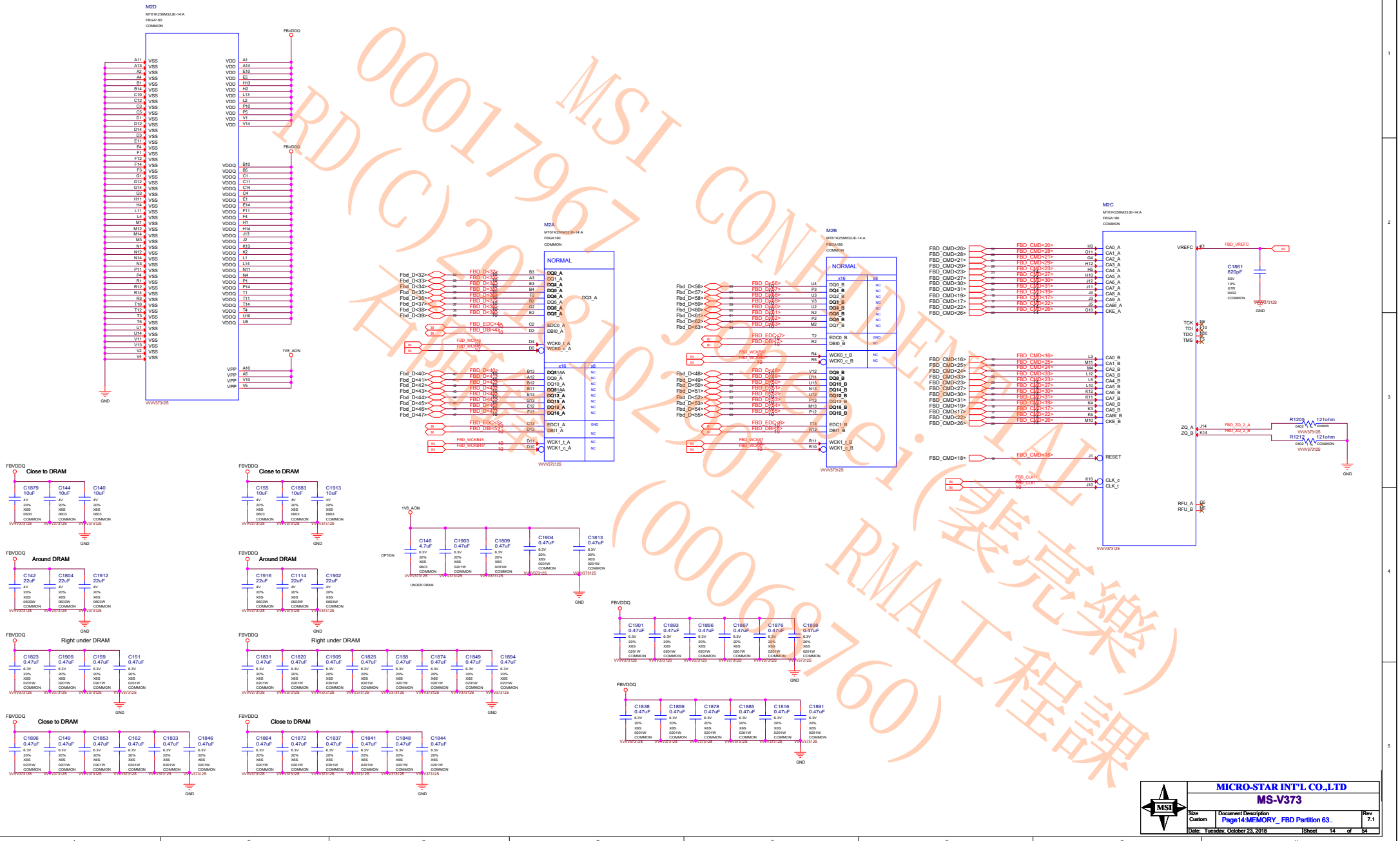
Page14: MEMORY: FBD Partition 63..32



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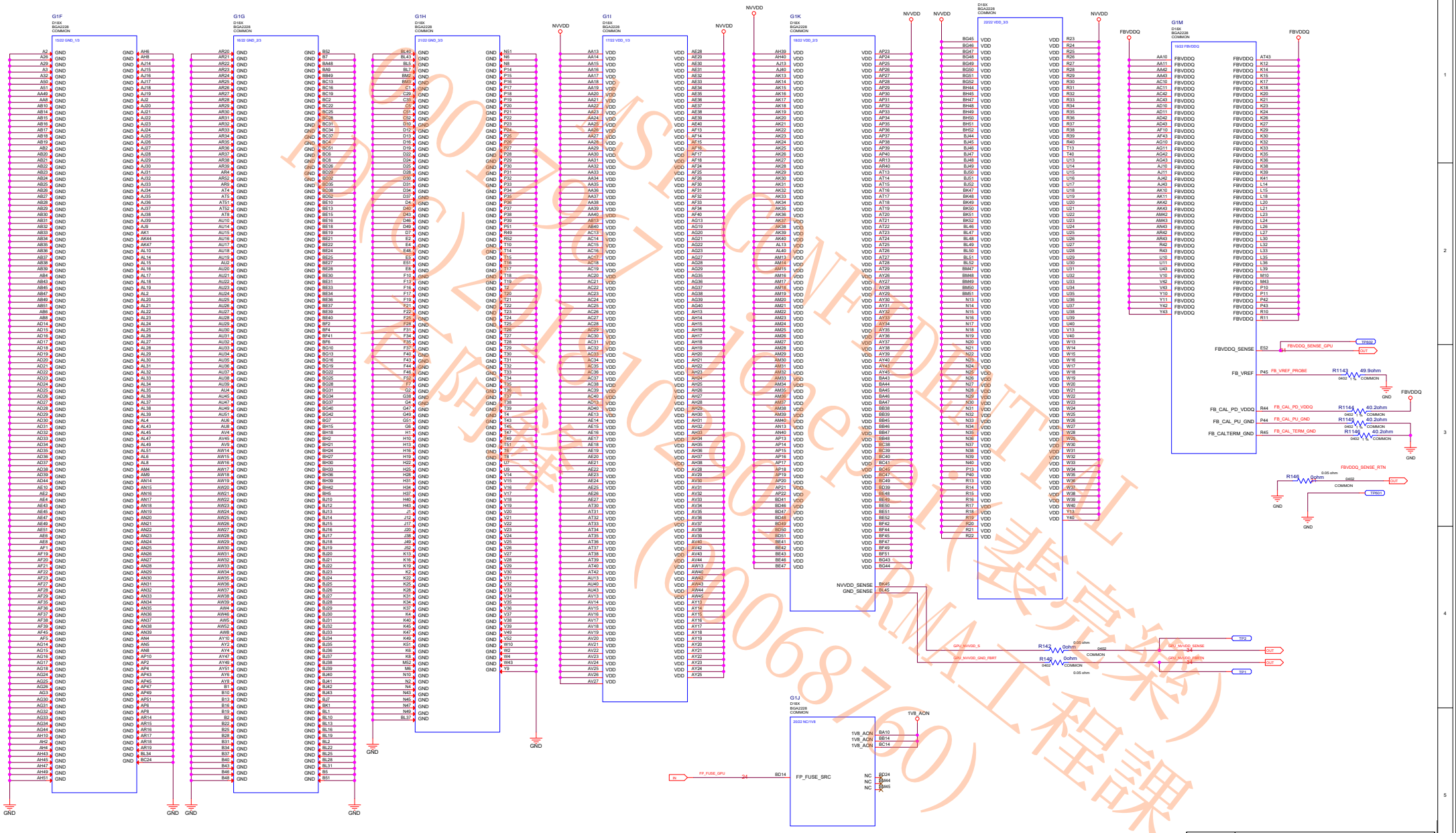
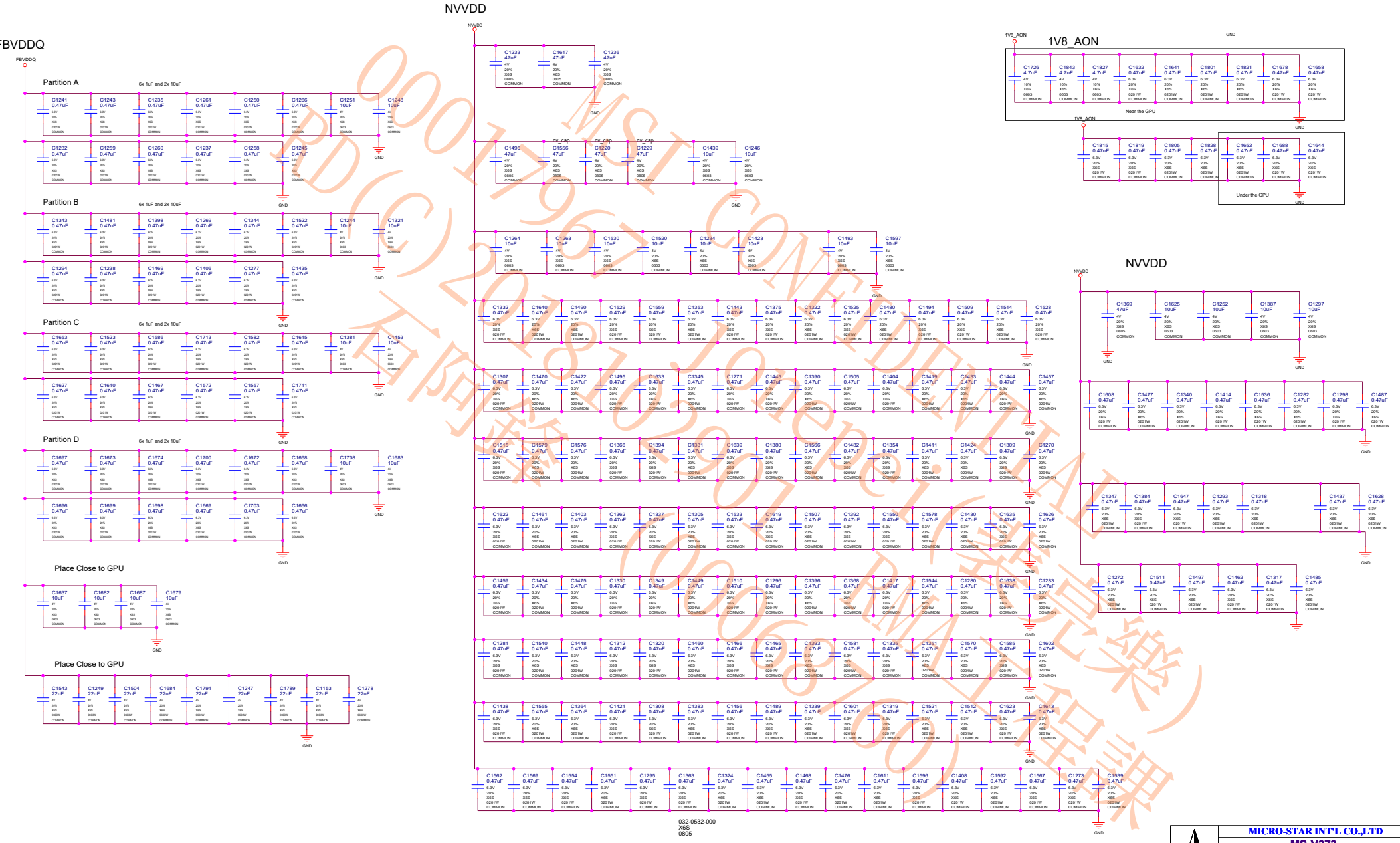
Page15: GPU PWR and GND



Page16: GPU Decoupling



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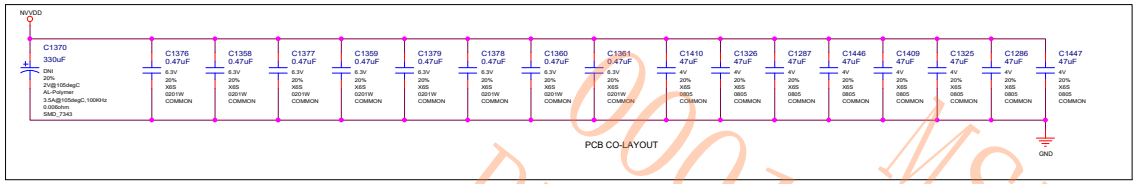
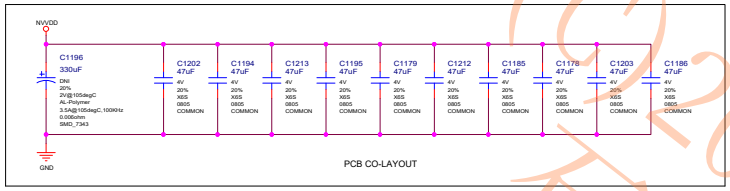
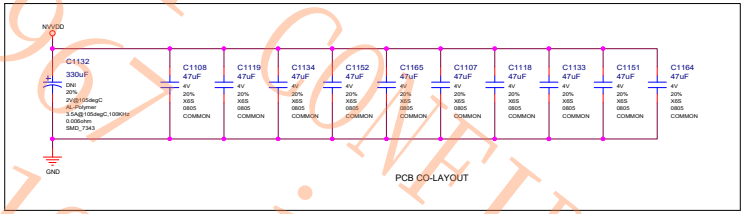
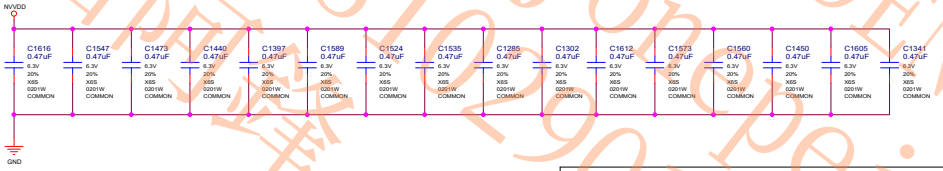
Size: Custom	Document Description: Page16:GPU Decoupling
Rev: 7.1	
Date: Tuesday, October 23, 2018	Sheet 16 of 54

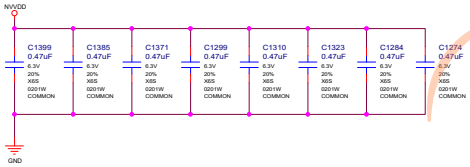
Page17: GPU Decoupling

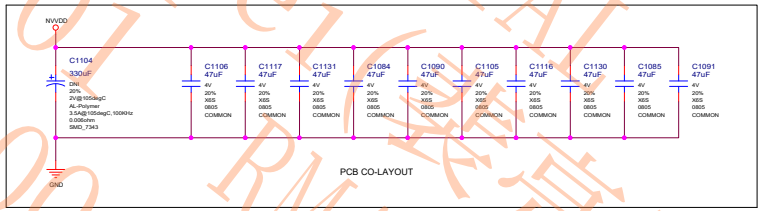


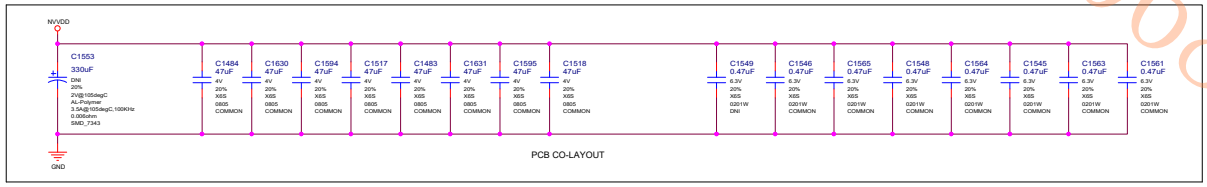












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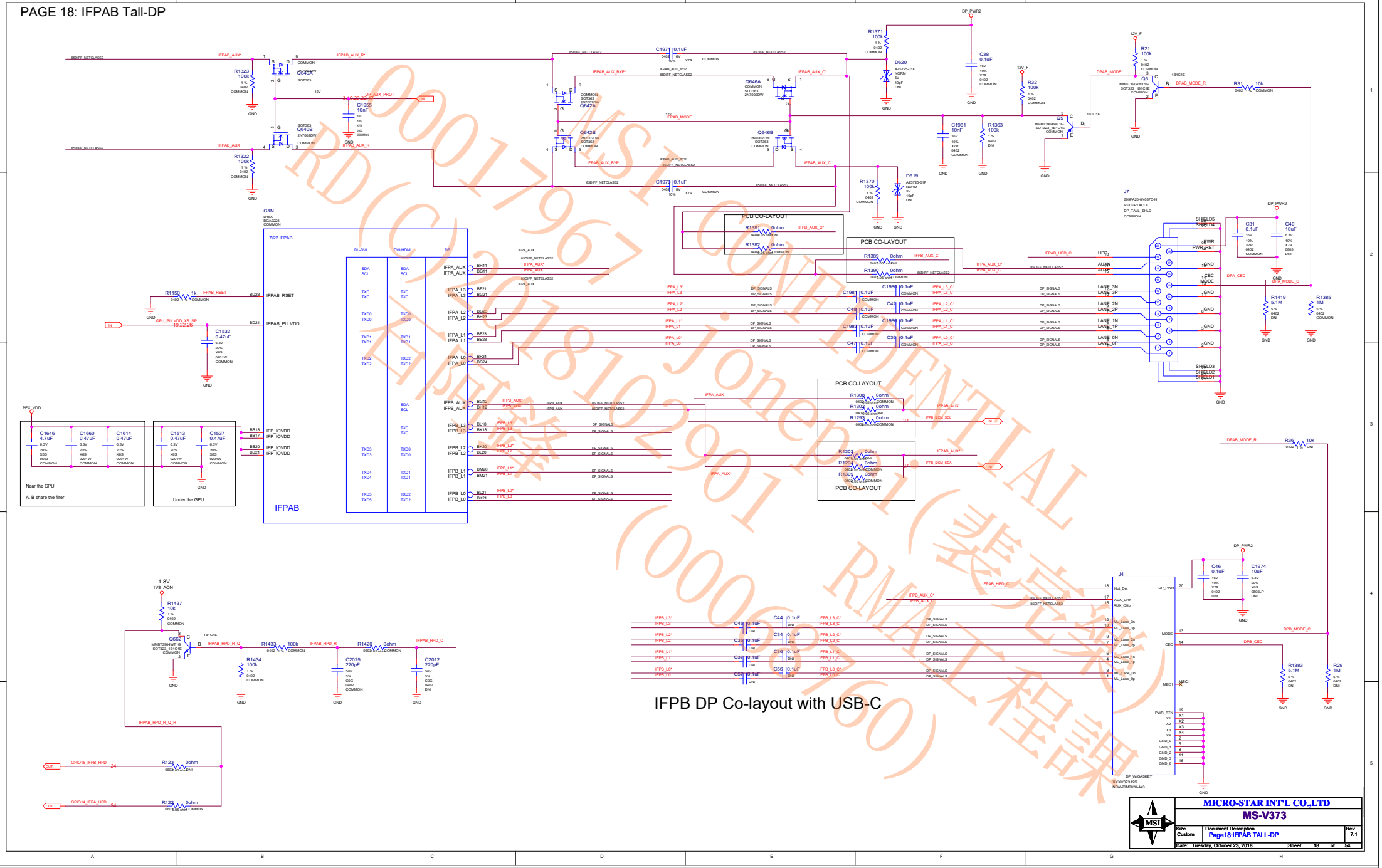
Rev: 7.1	
Date: Tuesday, October 23, 2018	Sheet 17 of 54



IFPB DP Co-layout with USB-C

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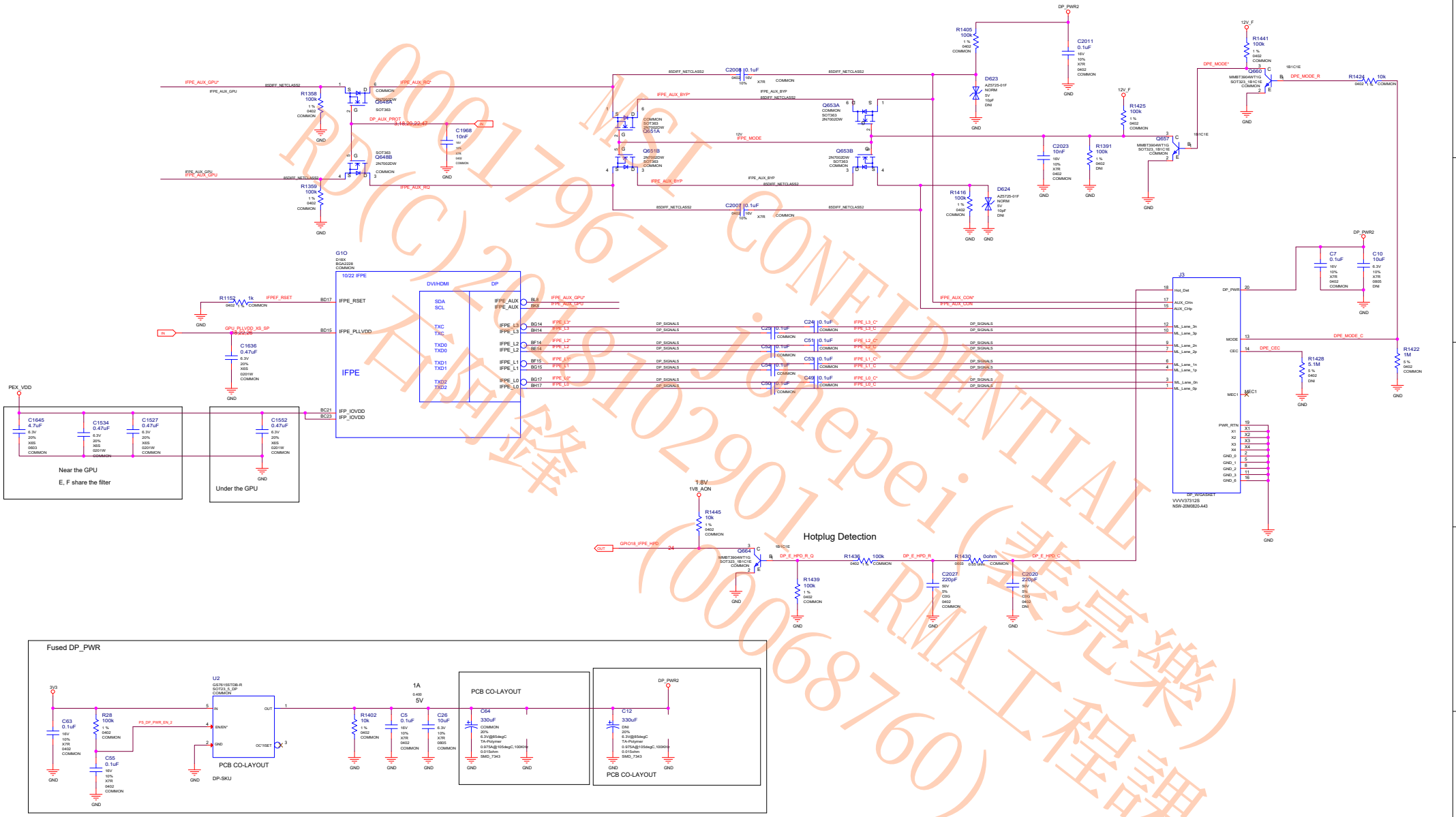
PAGE 19: IFPE DP



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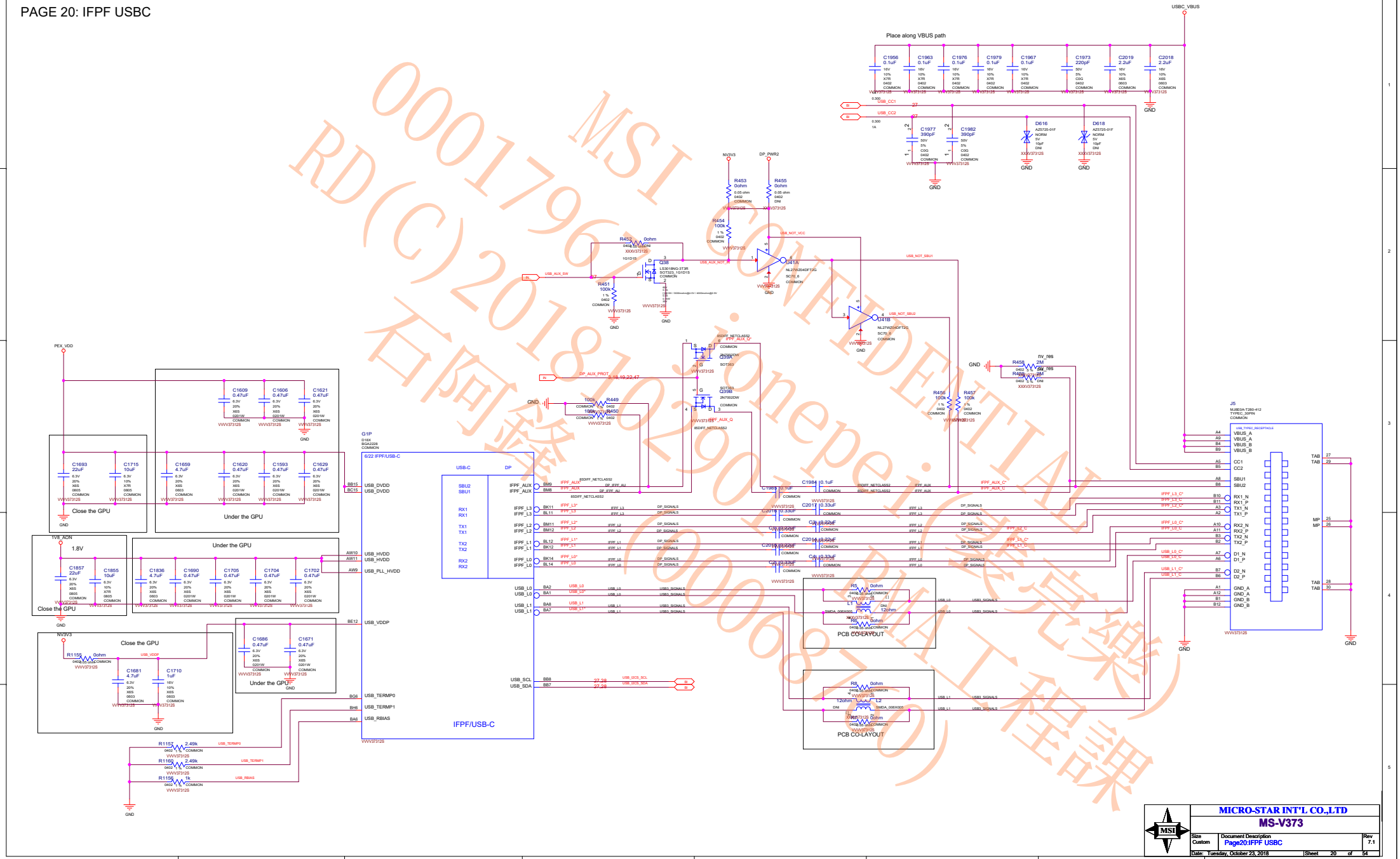
Size: Custom | Document Description: Page19:IFPE DP | Rev 7.0

Date: Tuesday, October 23, 2018 | Sheet 19 of 54

PAGE 20: IFPF USBC



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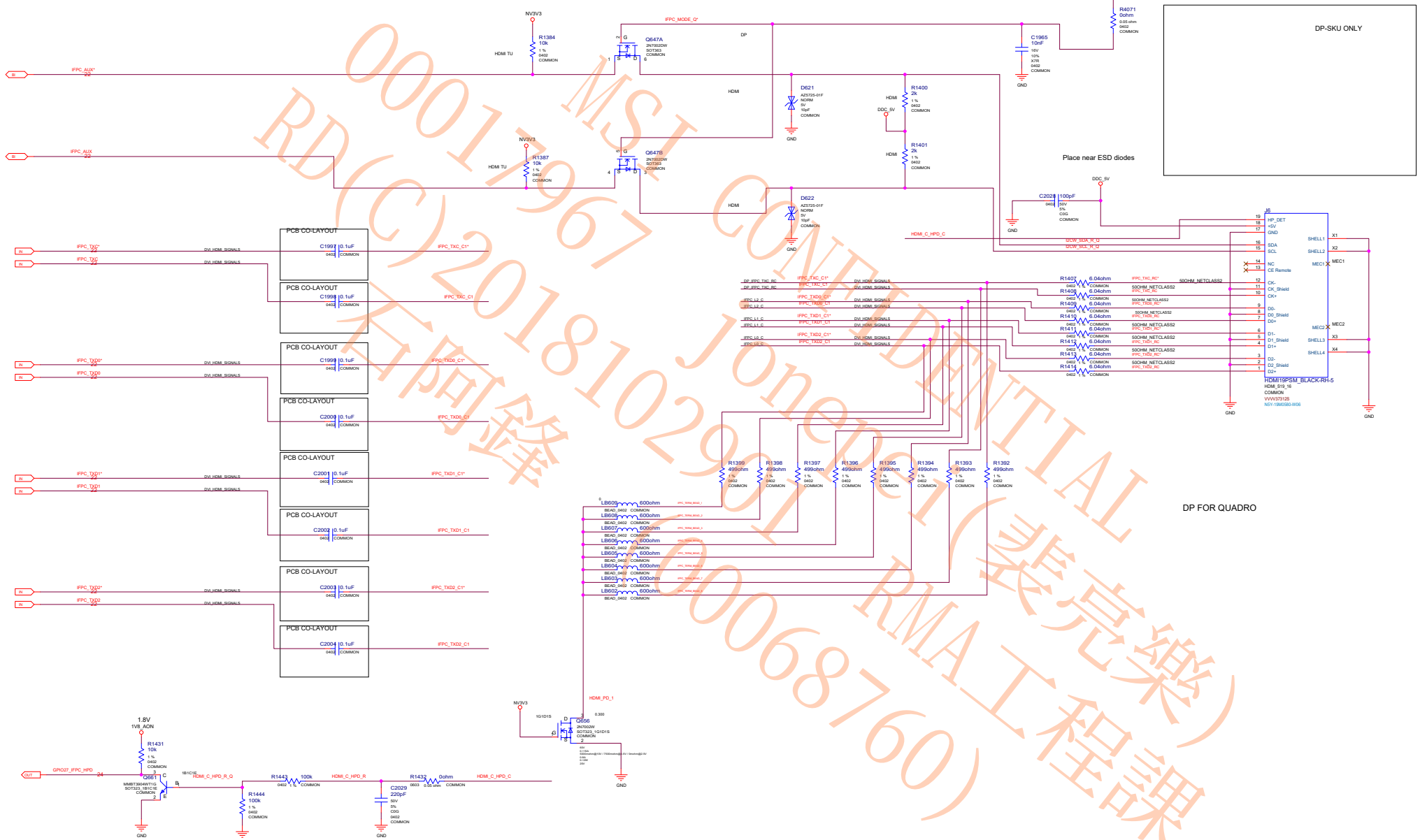
PAGE 21:IFPC HDMI 2.0/DP



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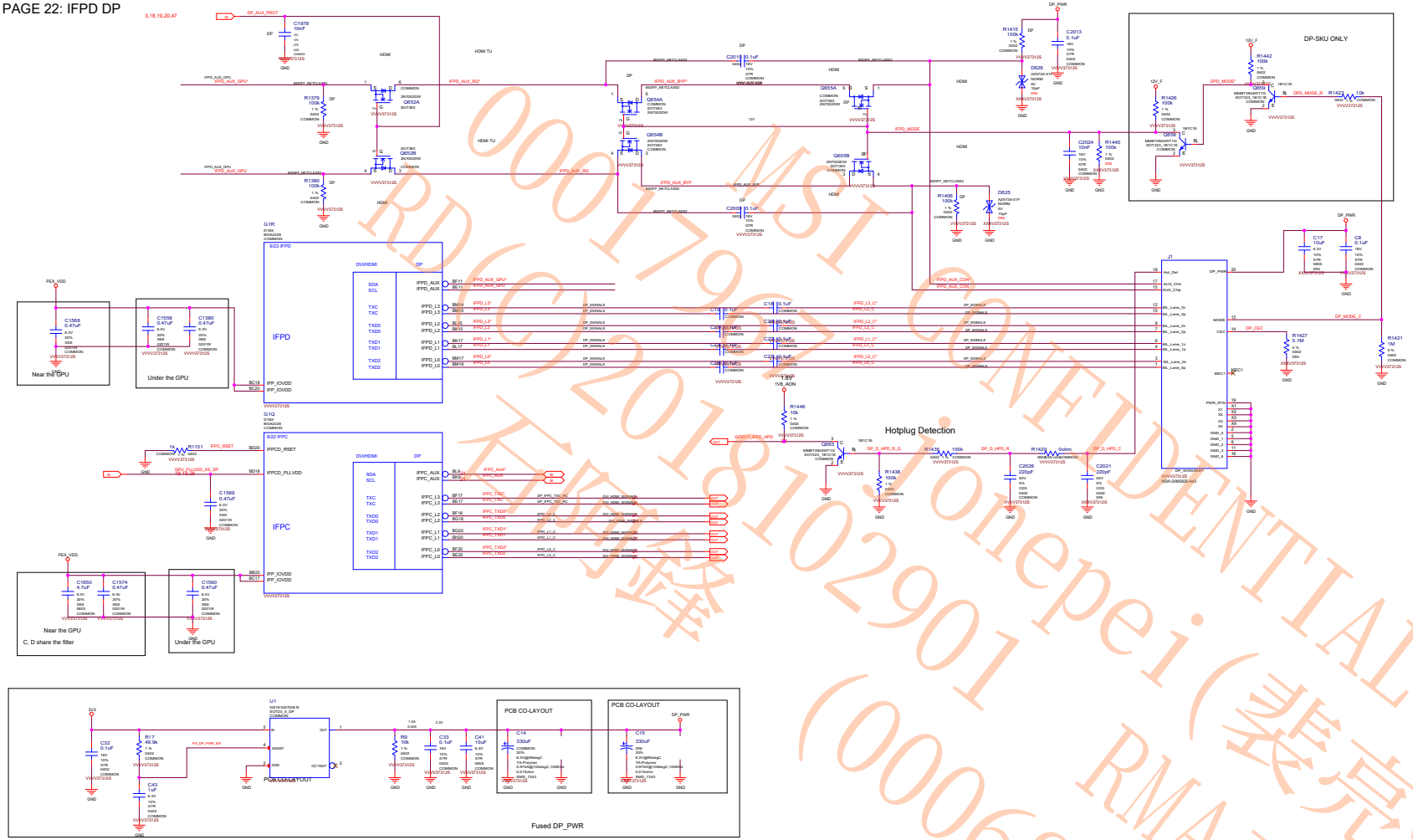
Size: Custom	Document Description: Page21:IFPC HDMI 2.0_DP
Rev: 7.1	
Date: Tuesday, October 23, 2018	Sheet 21 of 54

PAGE 22: IFPD DP



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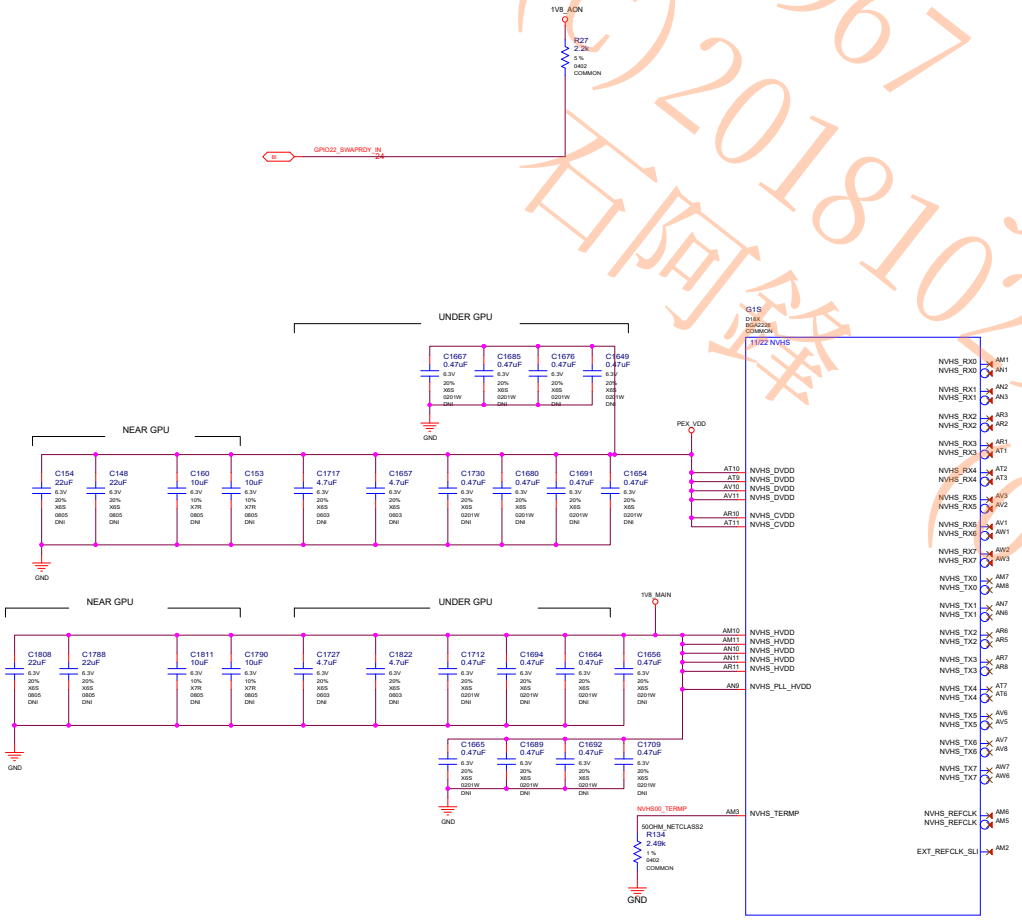
Size: Custom	Document Description: Page22:IFPD DP	Rev: 7.1
Date: Tuesday, October 23, 2018	Sheet 22 of 54	

PAGE 23: NVHS Interface



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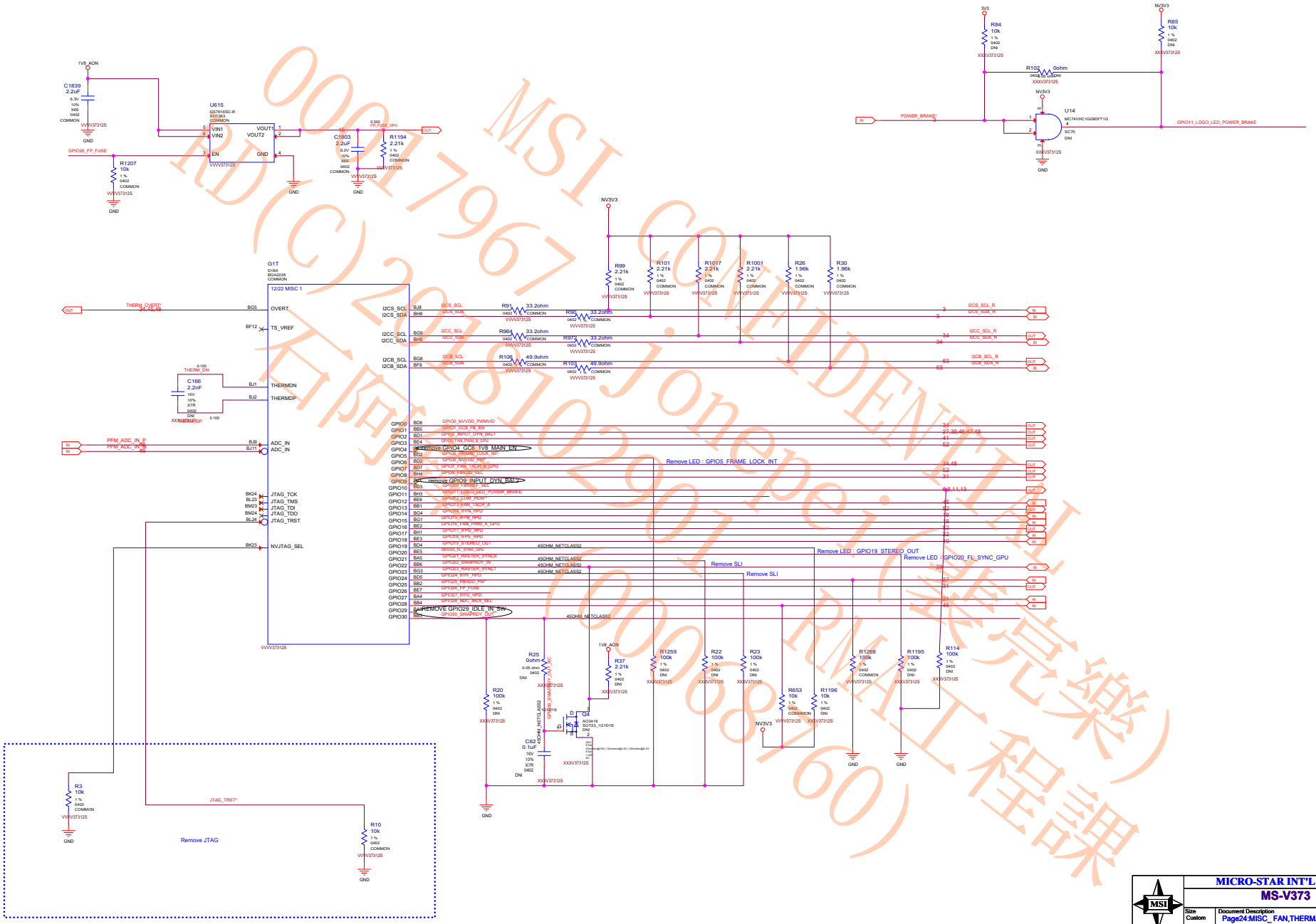
Size	Document Description	Rev
Custom	Page23:NVHS INTERFACE	7.1

Date: Tuesday, October 23, 2018 Sheet 23 of 54

PAGE 24: MISC: Fan, Thermal, JTAG, GPIO, STEREO



MICRO-STAR INT'L CO.,LTD		
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Size Custom	Document Description Page24:MISC_ FAN,THERMAL,JTAG,GPI	Rev 7.1
Date: Tuesday, October 23, 2018	Sheet 24 of 54	

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PAGE 25: MISC: ROM, Straps

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]		
L	L	L	00000	RAMCFG TBD	
L	L	H	00001	RAMCFG TBD	DEFAULT
L	H	L	00010	RAMCFG TBD	
L	H	H	00011	RAMCFG TBD	
H	H	L	00110	RAMCFG TBD	
H	H	H	00111	RAMCFG TBD	

RAMCFG[4:0]	DENSITY	WIDTH	VENDOR
00000	8Gb	256-bit	Samsung
00001	8Gb	256-bit	Micron
00010	8Gb	256-bit	Hynix
00110	16Gb	256-bit	Samsung
00111	16Gb	256-bit	Samsung

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	M	XXX0	FS_OVERT DISABLE	

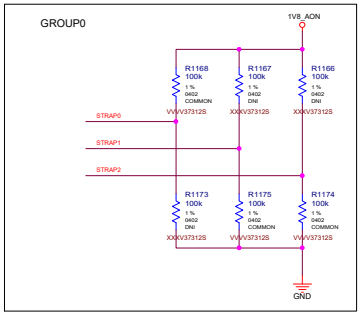
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	

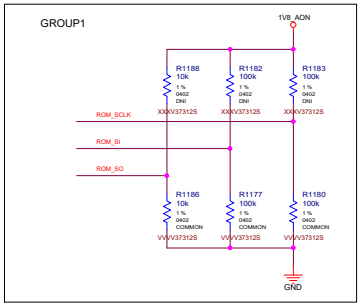
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

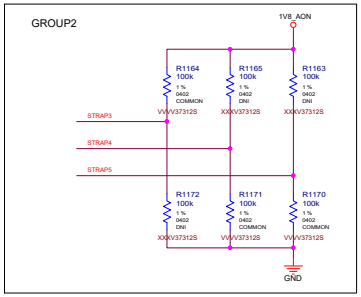
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

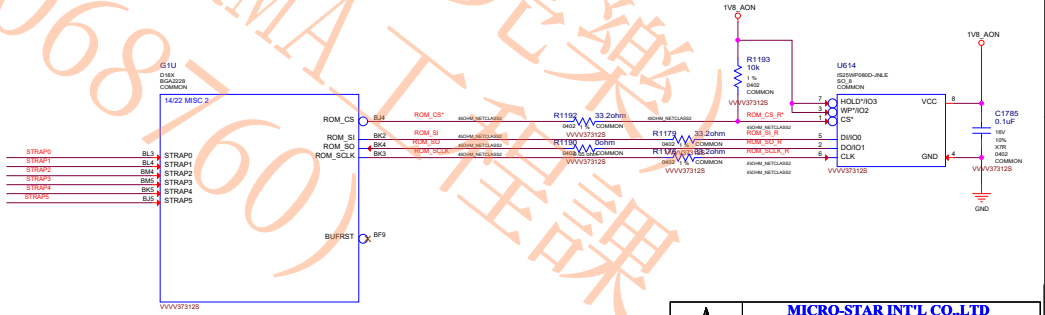
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE









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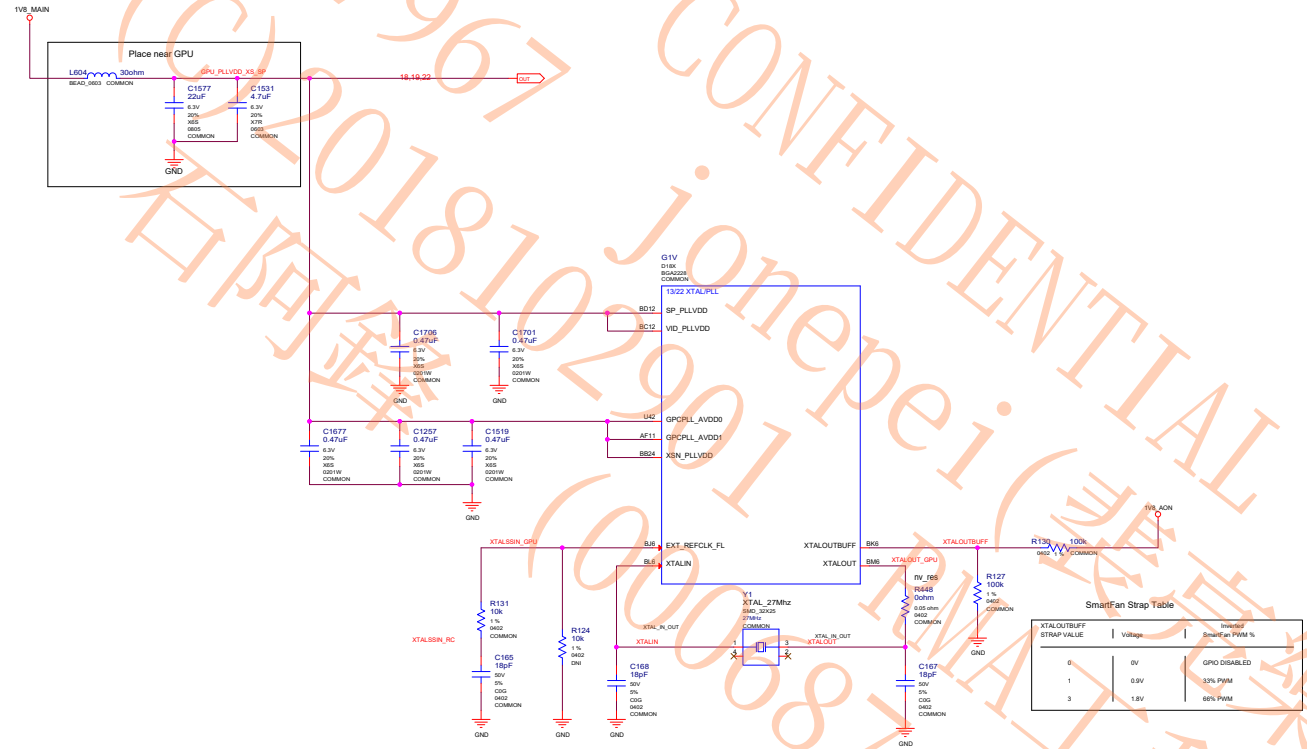
Size	Document Description	Rev
Custom	Page25:MISC3_ ROM, STRAPS	7.1

Date: Tuesday, October 23, 2018 Sheet 25 of 54

PAGE 26: MISC: XTAL. PLL



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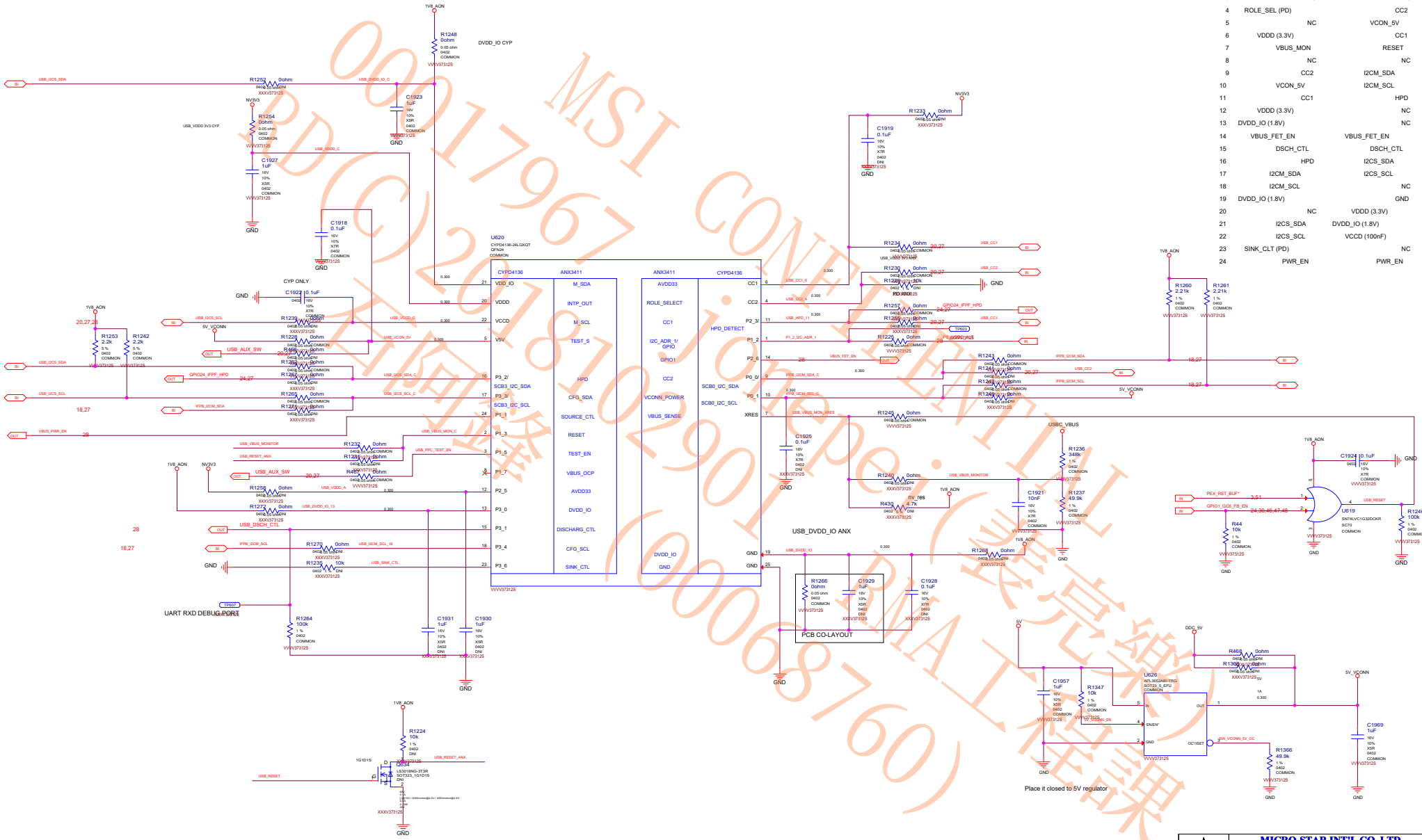
Size	Document Description	Rev
Custom	Page26:MISC_ XTAL, PLL	7.1

Date: Tuesday, October 23, 2018 Sheet 26 of 54

PAGE 27: MISC: USB PPC

PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN



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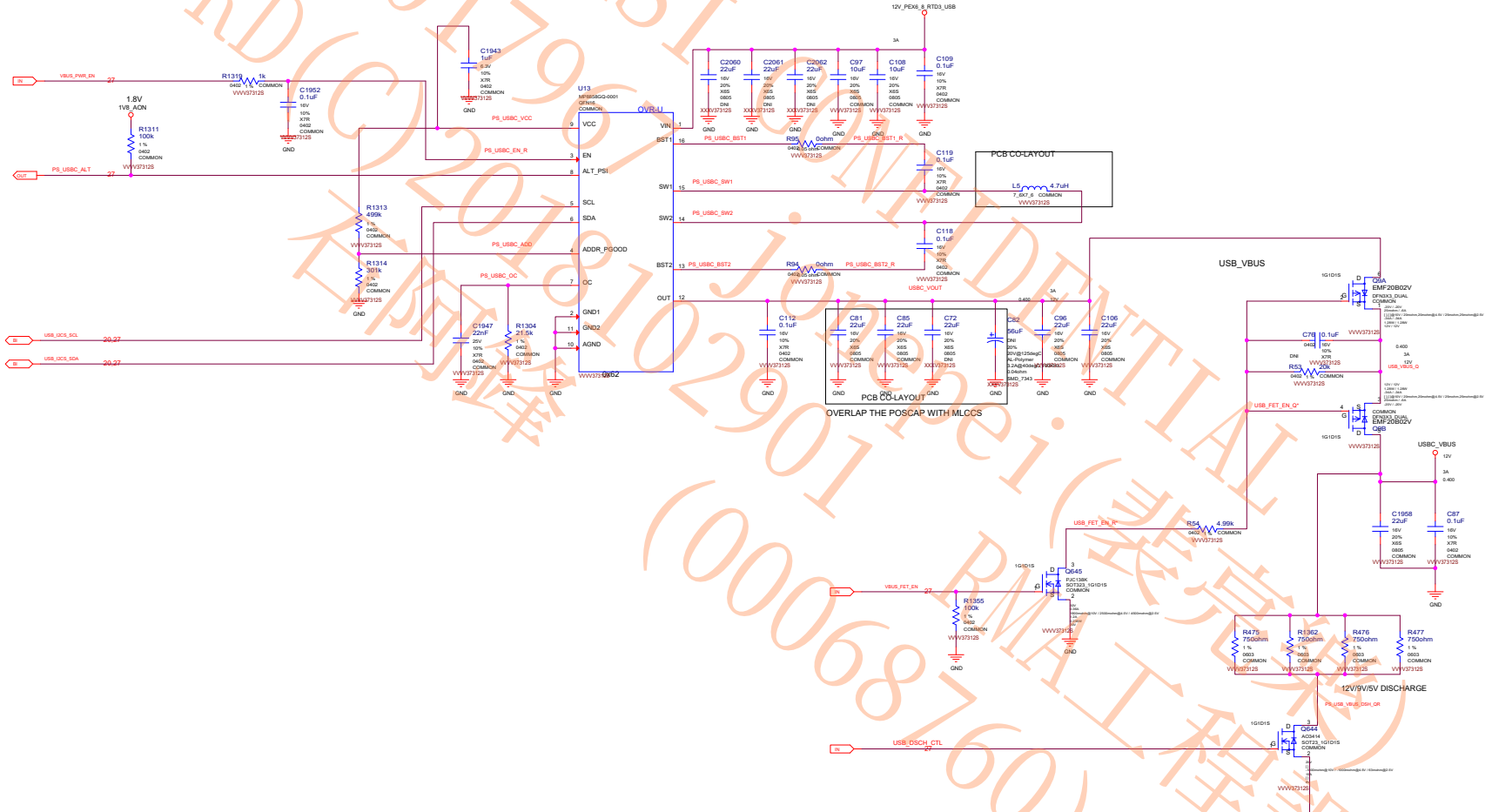
PAGE 28: PS: USB VR



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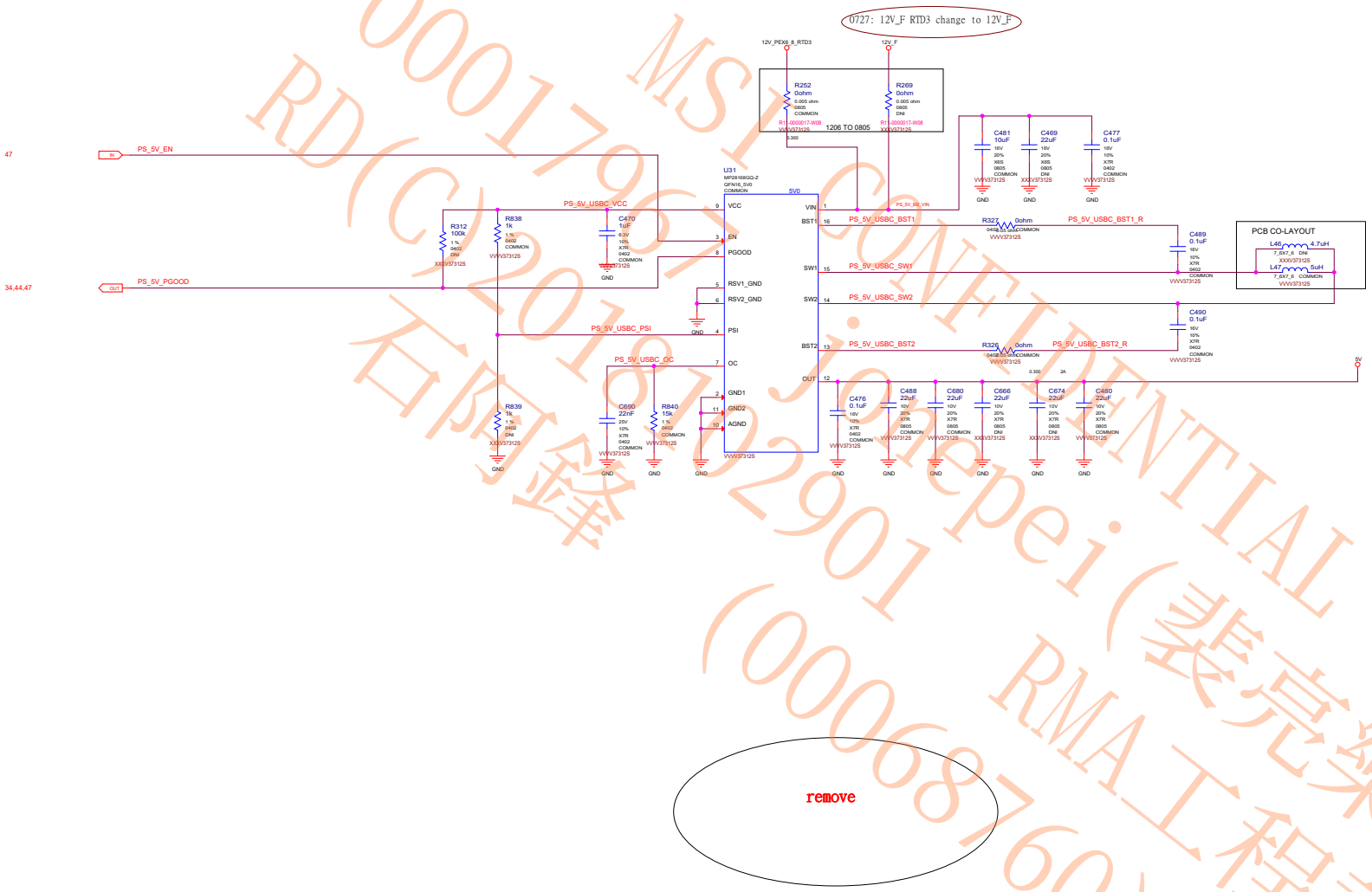
Size	Document Description	Rev
Custom	Page28:PS_USB VR	7.1

Date: Tuesday, October 23, 2018 Sheet 28 of 54

PAGE 29: PS: 5V, 5V_BACKUP



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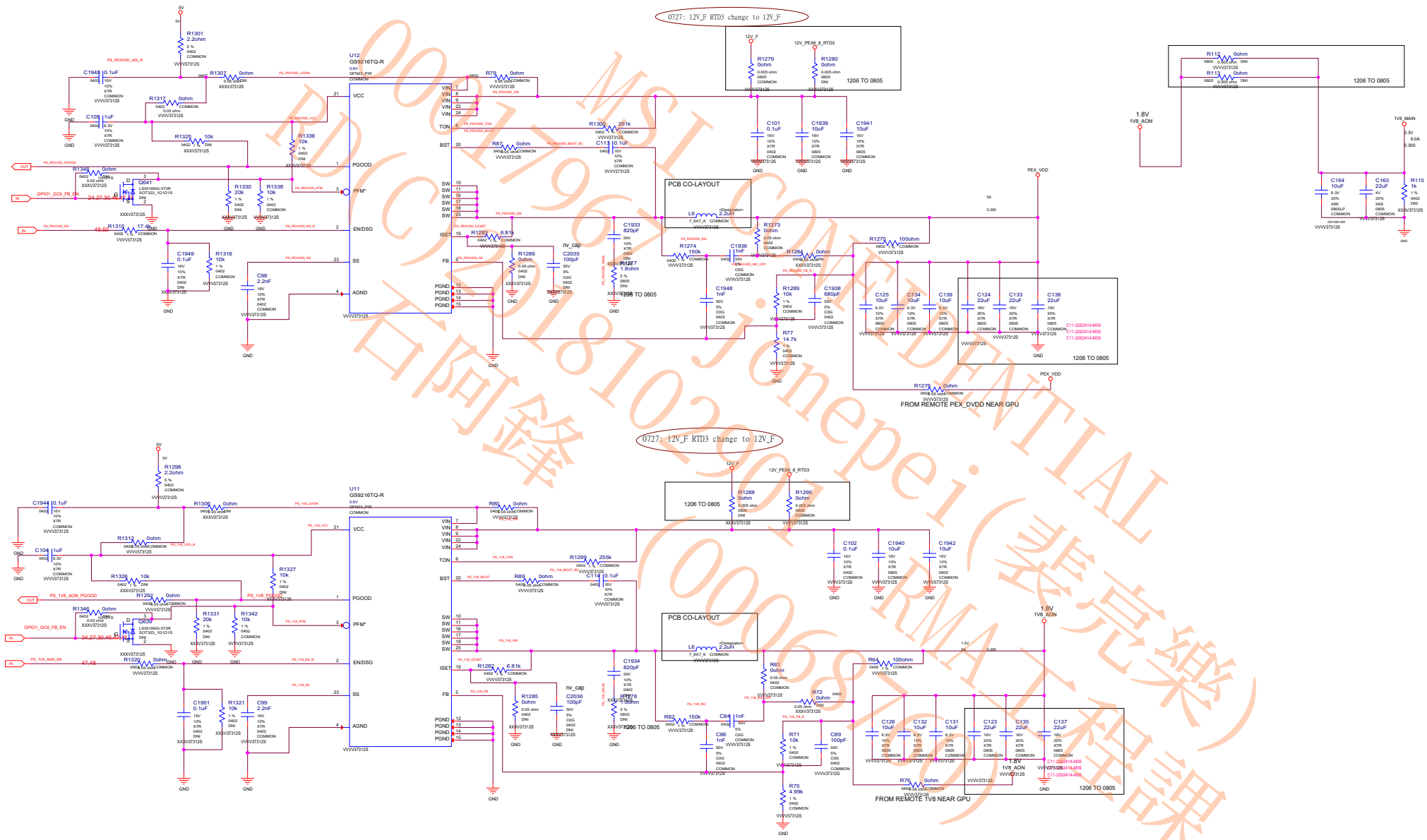
MS-V373	
Size: Custom	Document Description: Page29:PS_ 5V, 5V BACKUP
Rev: 7.1	
Date: Tuesday, October 23, 2018	Sheet 29 of 54

PAGE 30: PS: PEXVDD, 1V8



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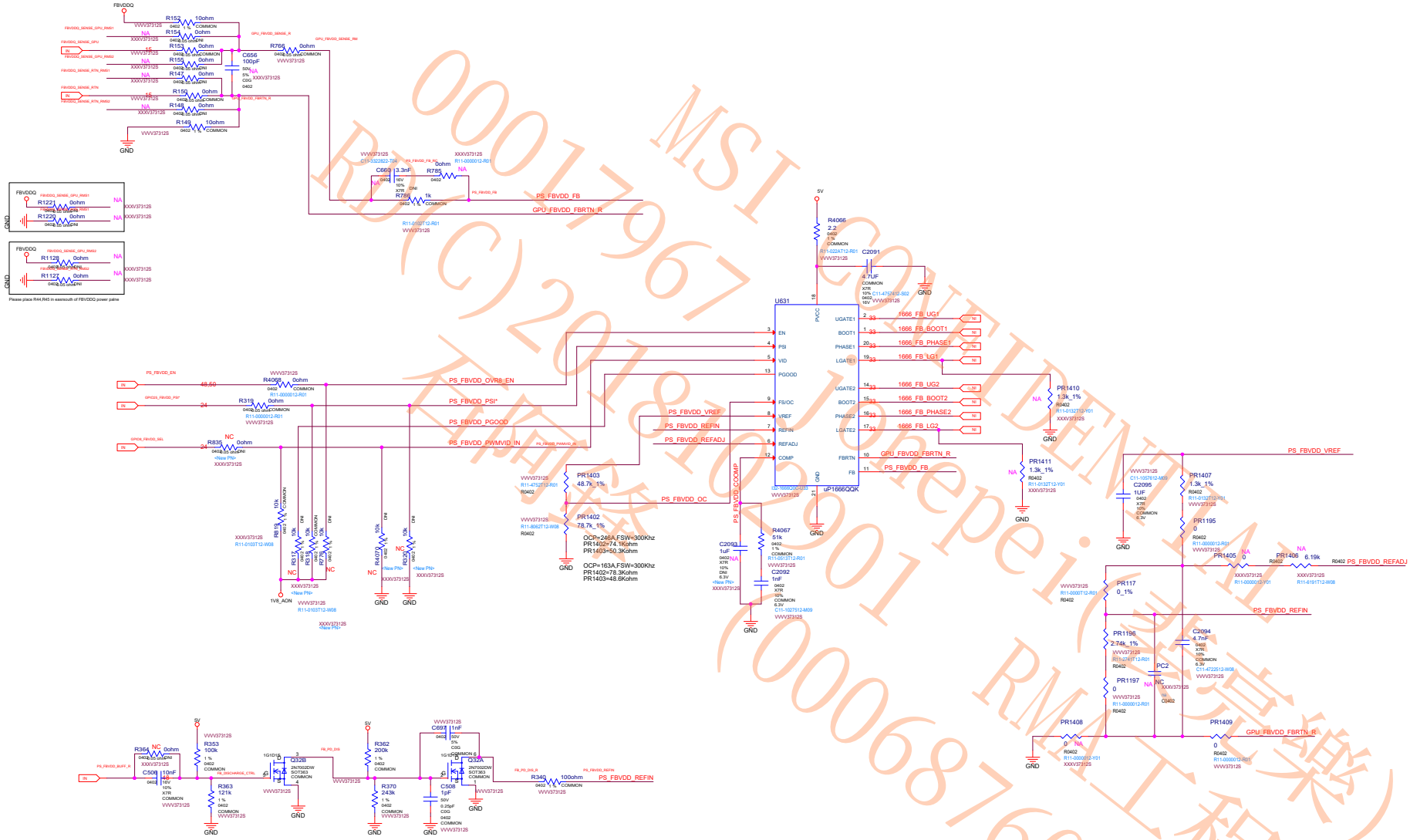
Size: Custom	Document Description: Page30:PS_ PEXVDD, 1V8
Rev: 7.1	
Date: Tuesday, October 23, 2018	Sheet 30 of 54

PAGE 31: PS: FBVDD Controller



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Size	Document Description	Rev
Custom	Page31:PS_ FBVDD CONTROLLER	7.1

Date: Tuesday, October 23, 2018 Sheet 31 of 54

PAGE 32: PS: FBVDD Controller OVR3

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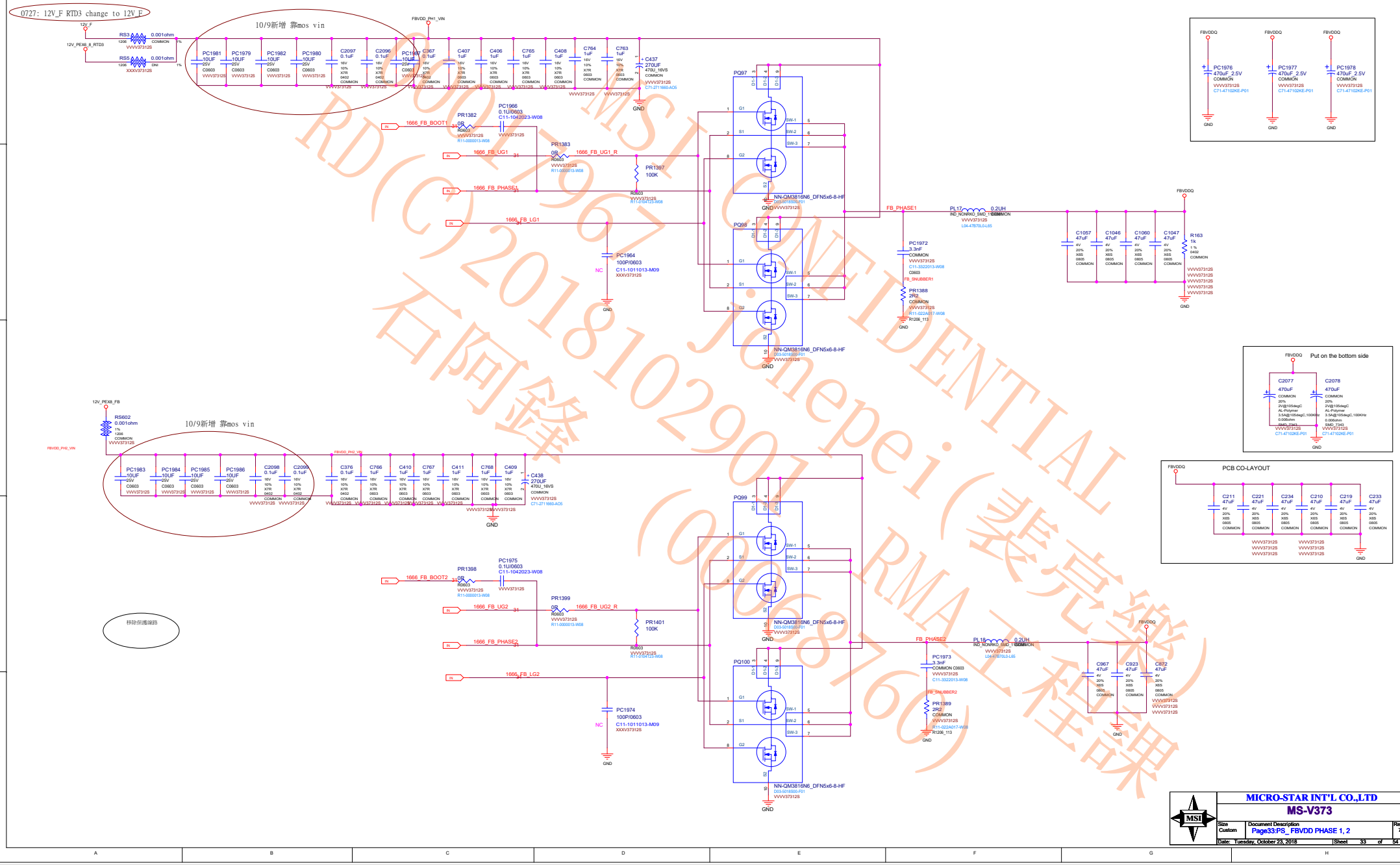
Size Custom	Document Description Page32:PS_ FBVDD CONTROLLER OVR3	Rev 7.1
Date: Tuesday, October 23, 2018	Sheet 32 of 54	

PAGE 33: PS: FBVDD Phase 1, 2



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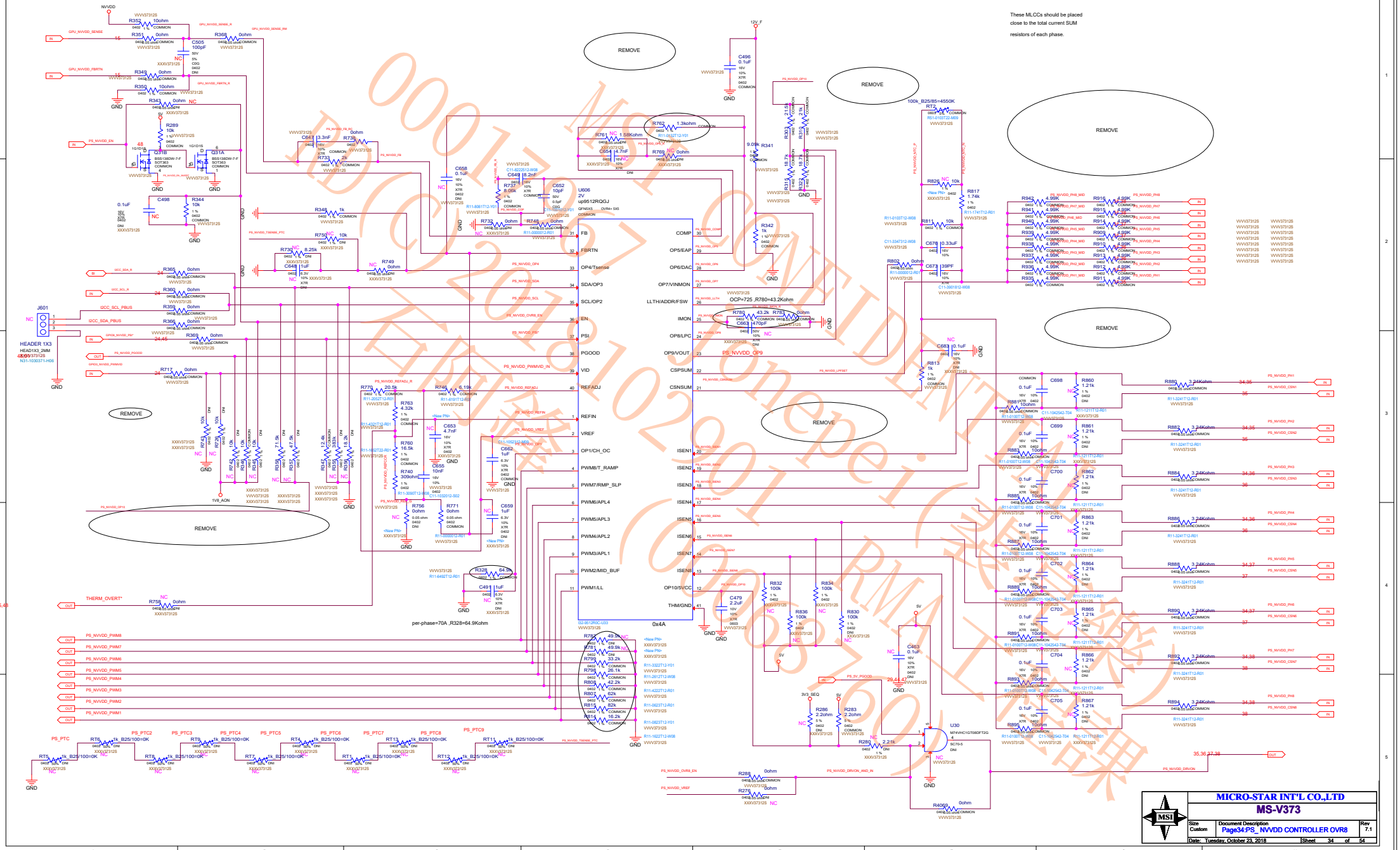
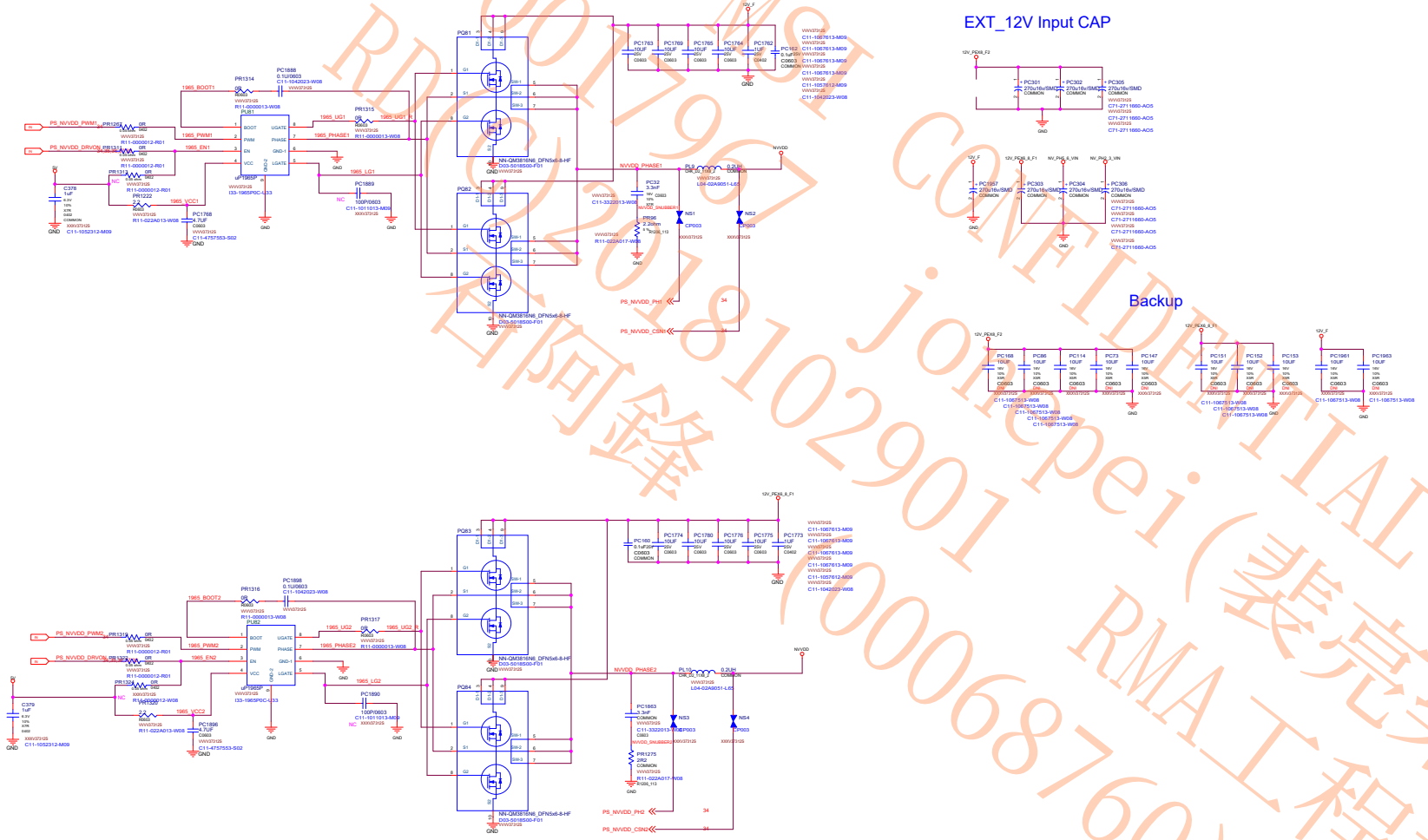
PAGE 34: PS: NVVDD Controller OVR8



PAGE 35: PS: NVVDD Phase 1, 2



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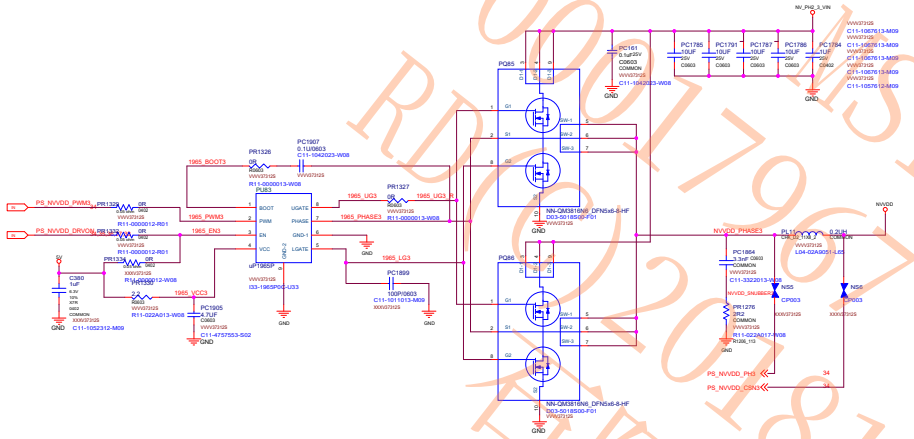
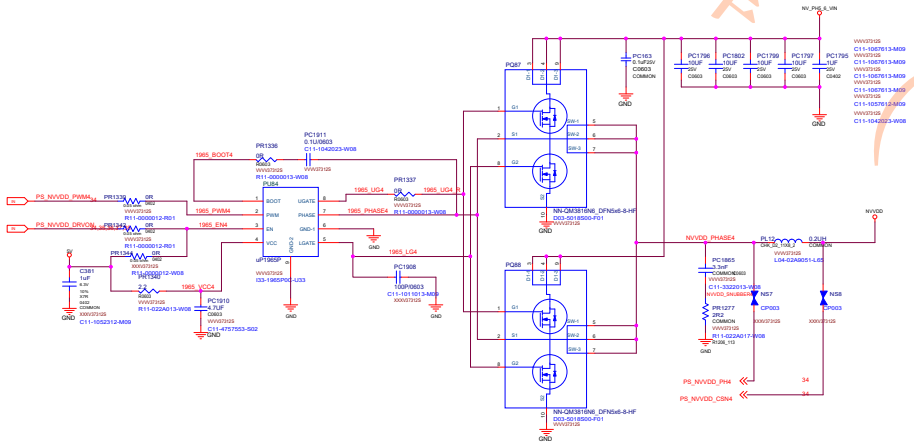
Size D
Document Description Page35:PS_ NVVDD Phase 1, 2
Rev 7.1
Date: Tuesday, October 23, 2018
Sheet 35 of 54

PAGE 36: PS: NVVDD Phase 3, 4





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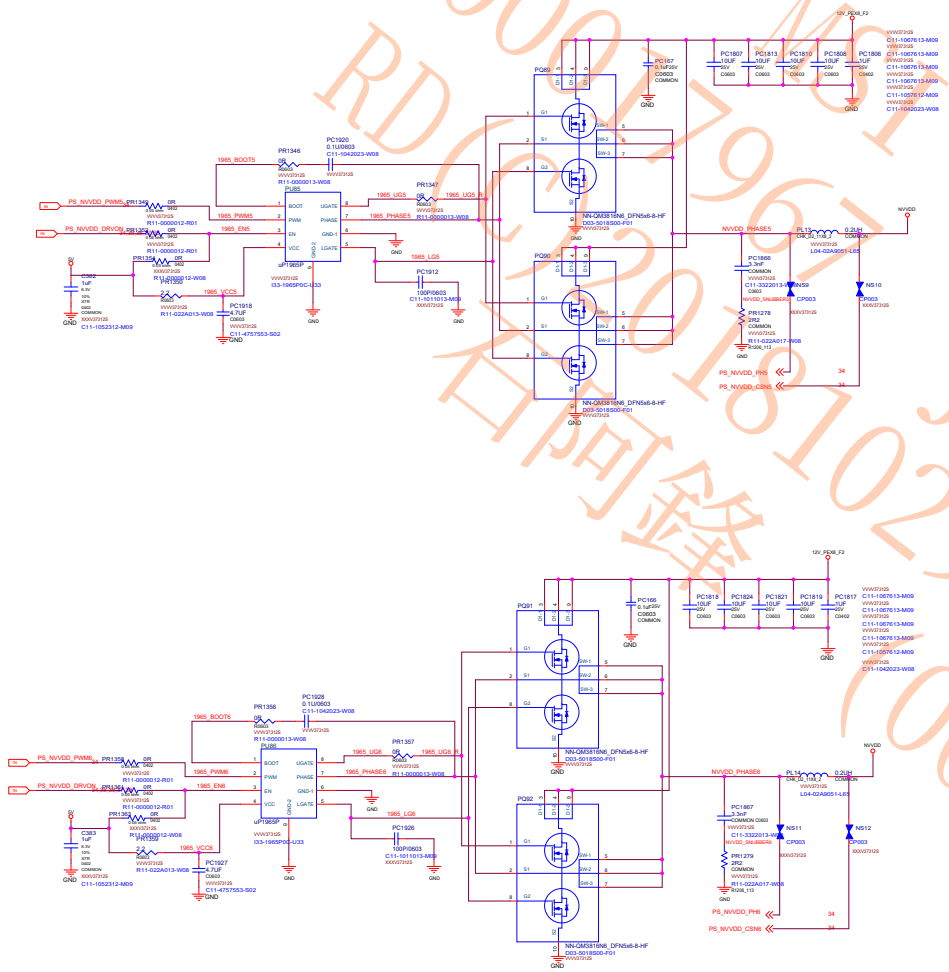
Size: D	Document Description: Page36:PS_ NVVDD Phase 3, 4		Rev: 7.1
Date: Tuesday, October 23, 2018		Sheet 36 of 54	



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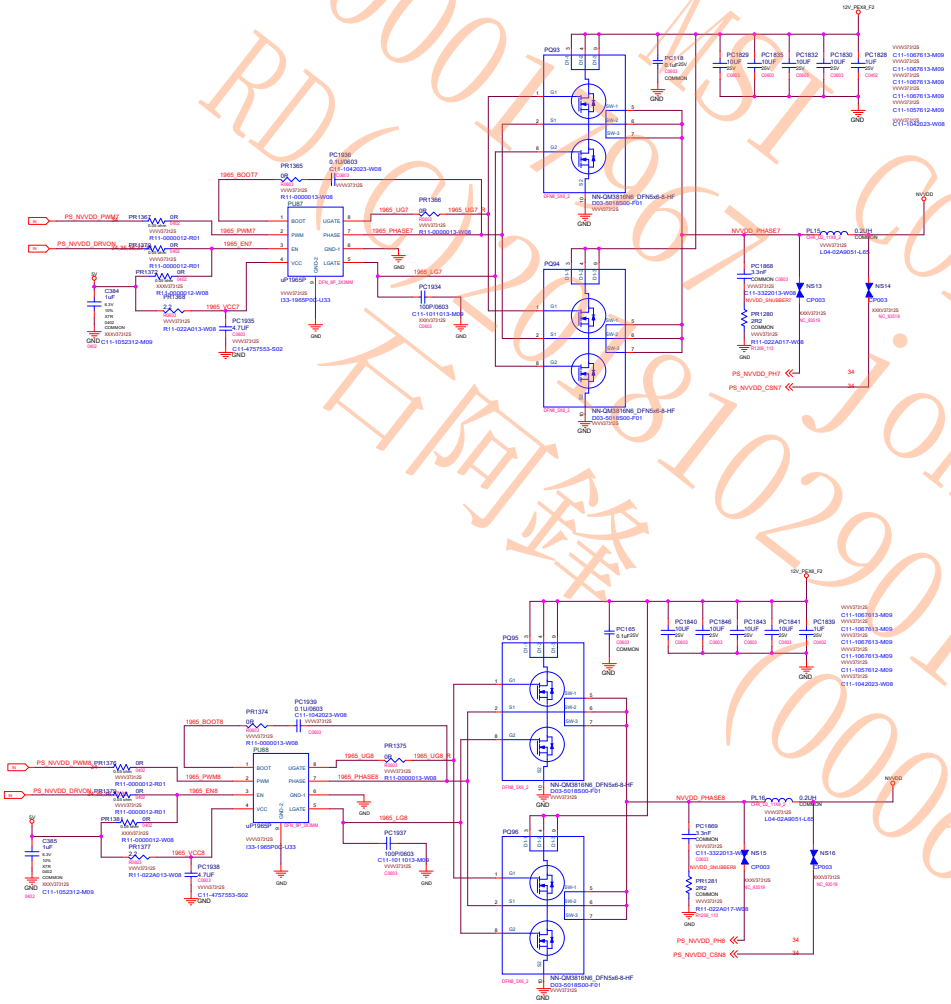
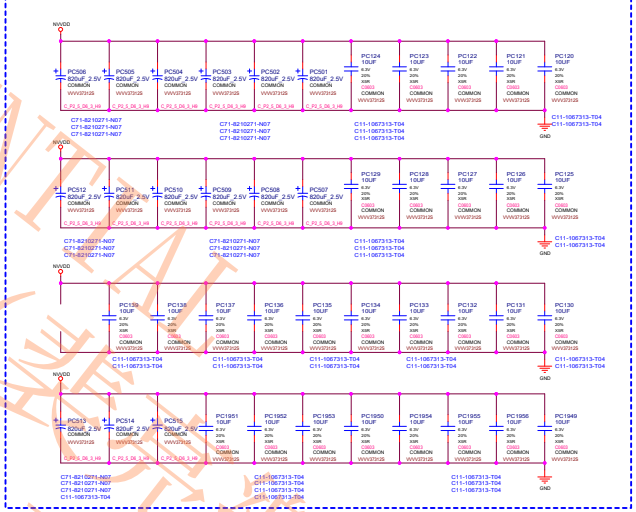
Size: D | Document Description: Page37:PS_ NVVDD Phase 5, 6 | Rev: 7.1
Date: Tuesday, October 23, 2018 | Sheet 37 of 54



NVVDD Output CAP



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Size D	Document Description Page38:PS_ NVVDD Phase 7, 8	Rev 7.1
Date: Tuesday, October 25, 2016	Sheet 38 of 54	

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

0727: remove

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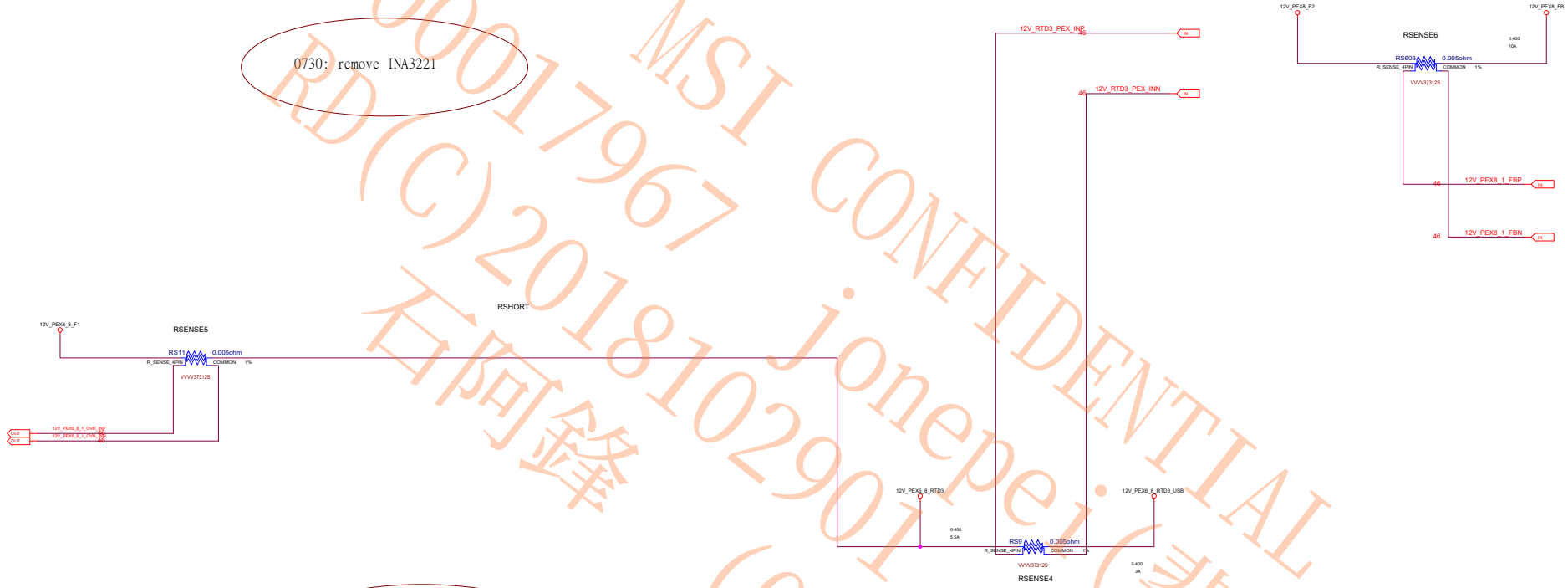
PAGE 40: PS: INPUT SWITCH RTD3 USB

0730: remove INA3221

0727: remove OVR-SWITCH==>U607



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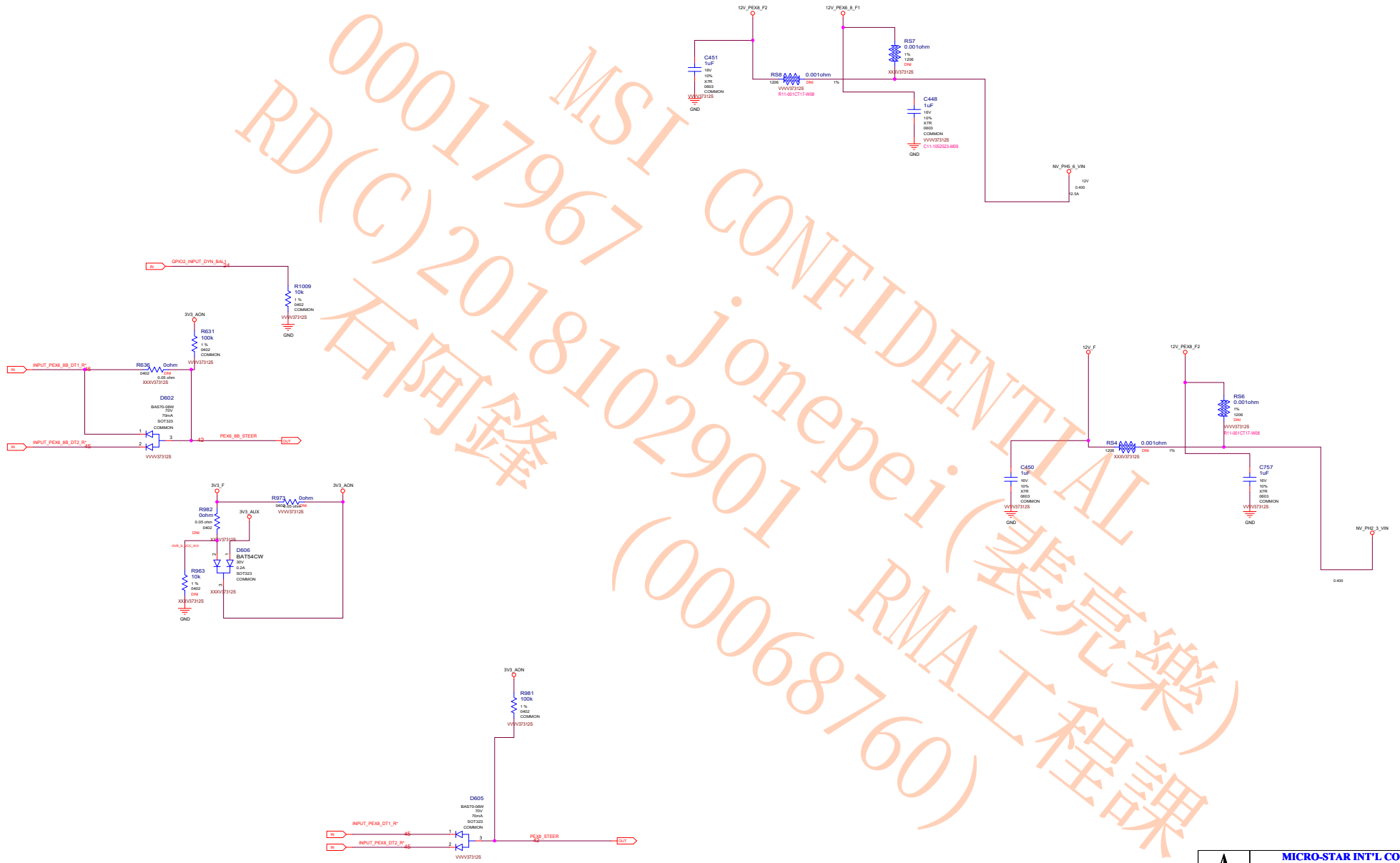
Size	Document Description	Rev
Custom	Page40:PS_ INPUT SWITCH RTD3 USB	7.1

Date: Tuesday, October 23, 2018 Sheet 40 of 54

PAGE 41: PS: INPUT SWITCH Rail Balance



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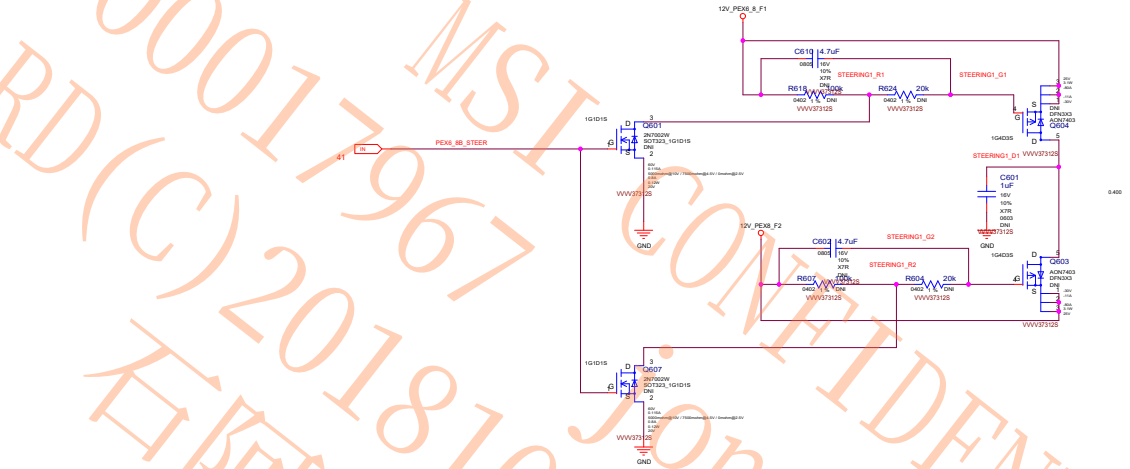
Size	Document Description	Rev
Custom	Page41:PS_ INPUT SWITCH RAIL BALA	7.1

Date: Tuesday, October 23, 2018 Sheet 41 of 54

PAGE 42: PS: 12V CURRENT STEERING

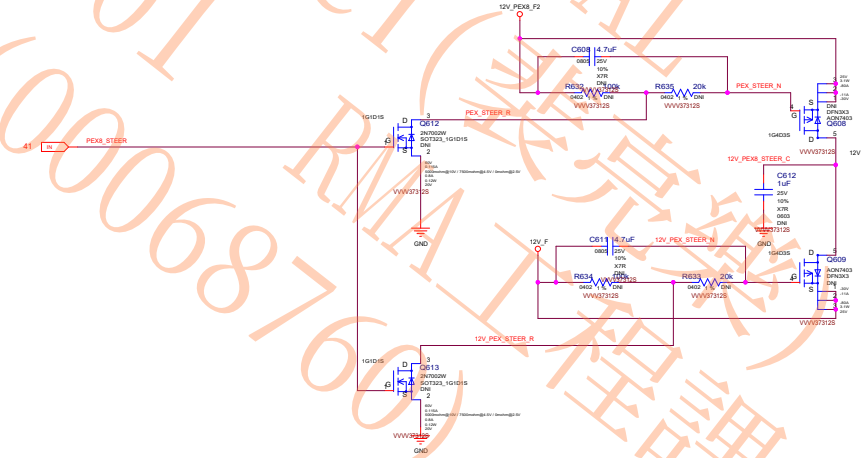
12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA



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Size Custom	Document Description Page42:PS_ 12V CURRENT STEERING	Rev 7.1
Date: Tuesday, October 23, 2018	Sheet 42 of 54	

PAGE 43: PS: VR THERMAL PROTECTION

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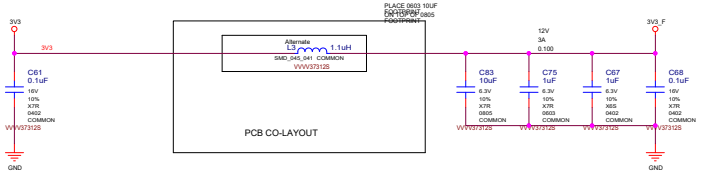
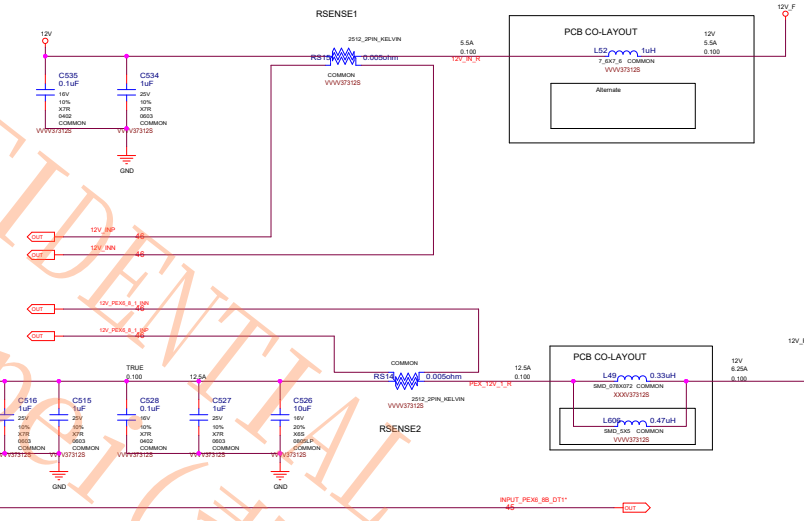
Size: Custom	Document Description: Page43:PS_ VR THERMAL PROTECTION
Rev: 7.1	
Date: Tuesday, October 23, 2018	Sheet 43 of 54

0727: remove U37

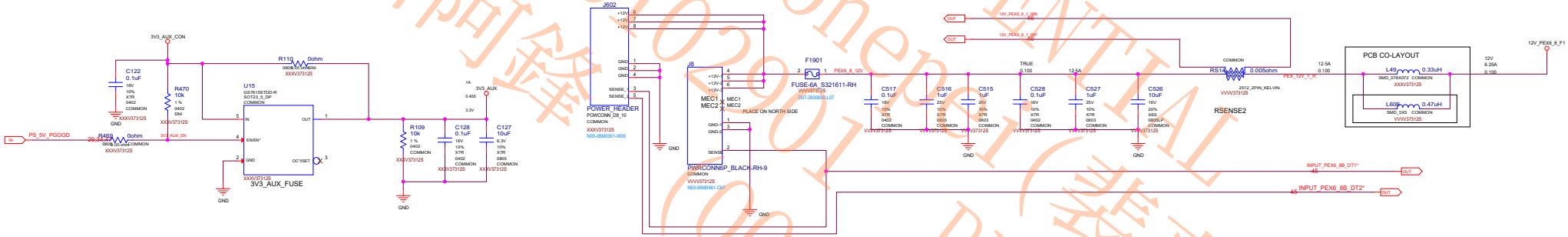
PEX 3V3 INPUT - 10W



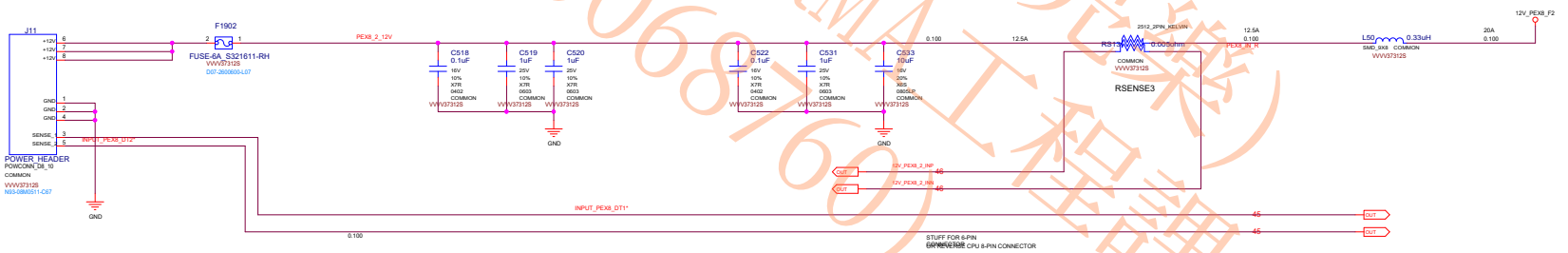
PEX_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



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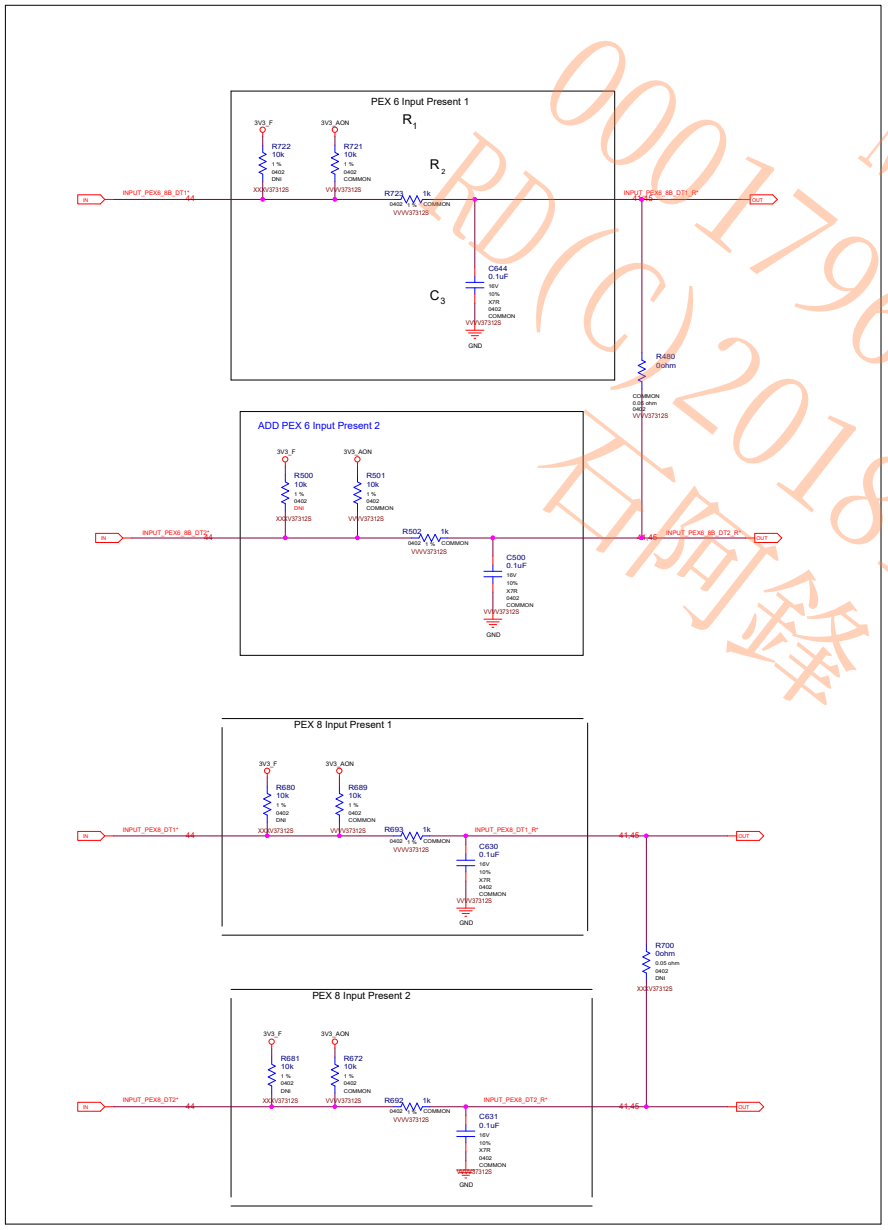
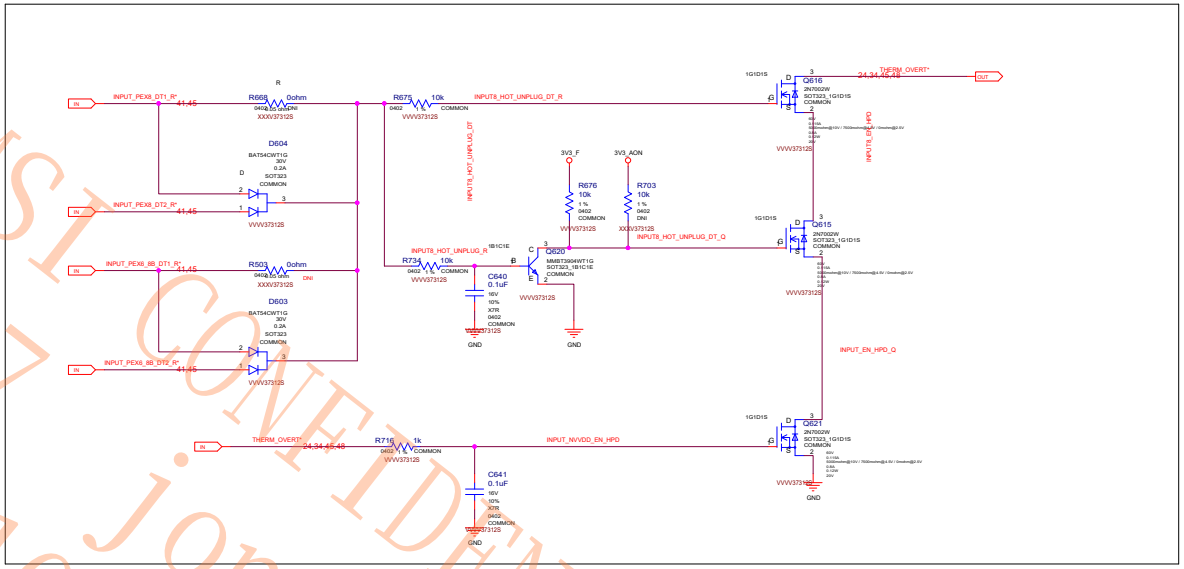
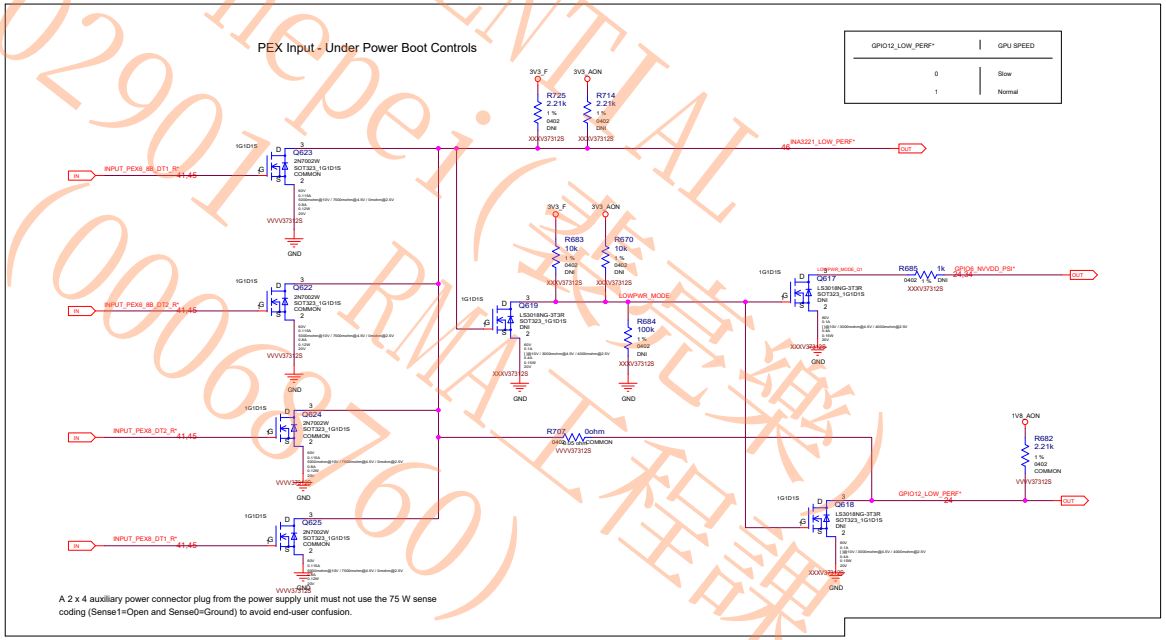
Size Custom	Document Description Page44:PS_ INPUTS, FILTERING AND	Rev 7.1
Date: Tuesday, October 23, 2018	Sheet 44 of 54	

PAGE 45: PS: Current Steering, Hot Unplug Detect







GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

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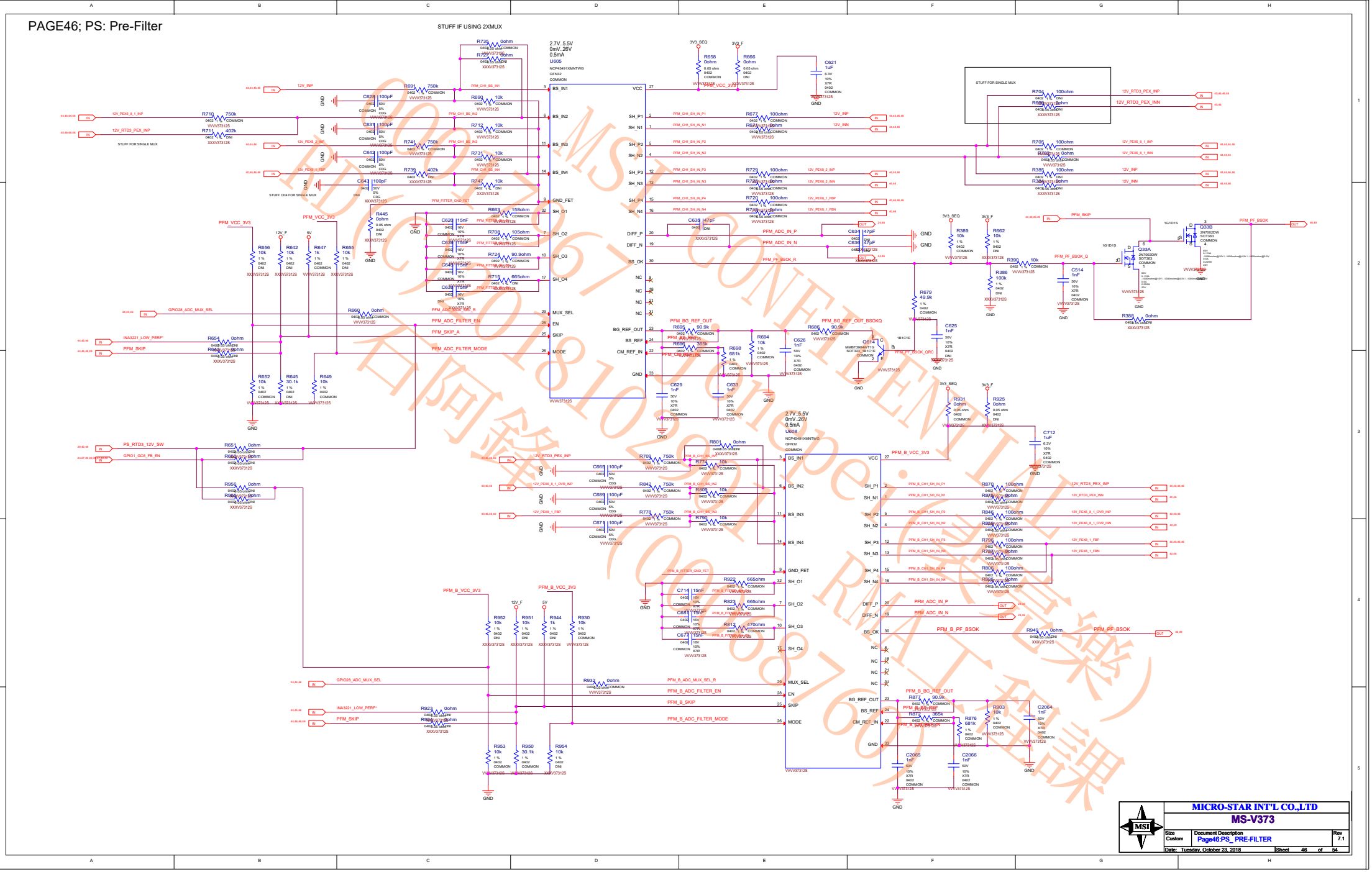
Size	Document Description	Rev
Custom	Page45;PS_ CURRENT STEERING,HOT U	7.1

Date: Tuesday, October 23, 2018 Sheet 45 of 54



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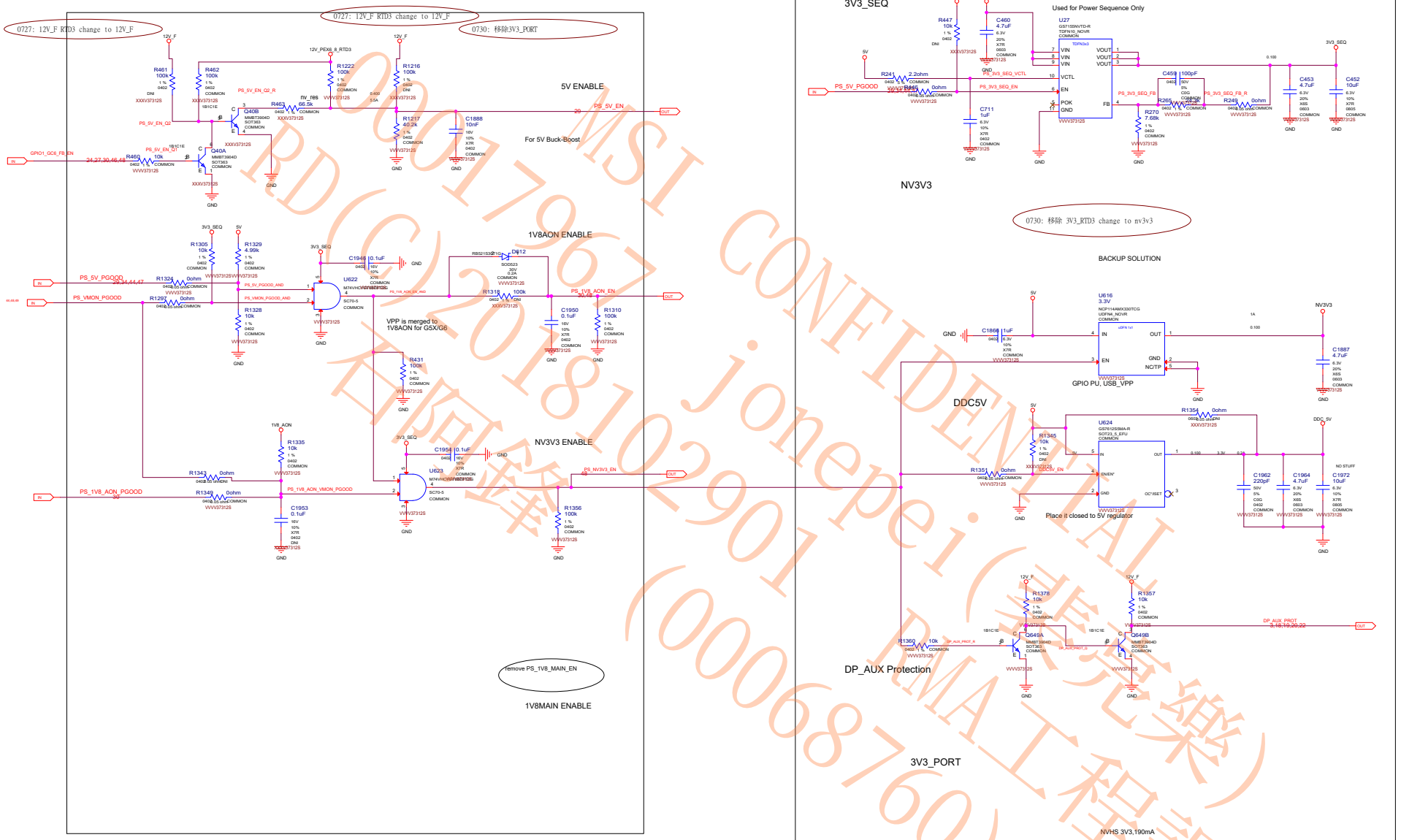
Size	Document Description	Rev
Custom	Page46:PS_ PRE-FILTER	7.1

Date: Tuesday, October 23, 2018 Sheet 46 of 54

PAGE 47: SEQUENCE:5V,1V8,NV3V3 ENABLE



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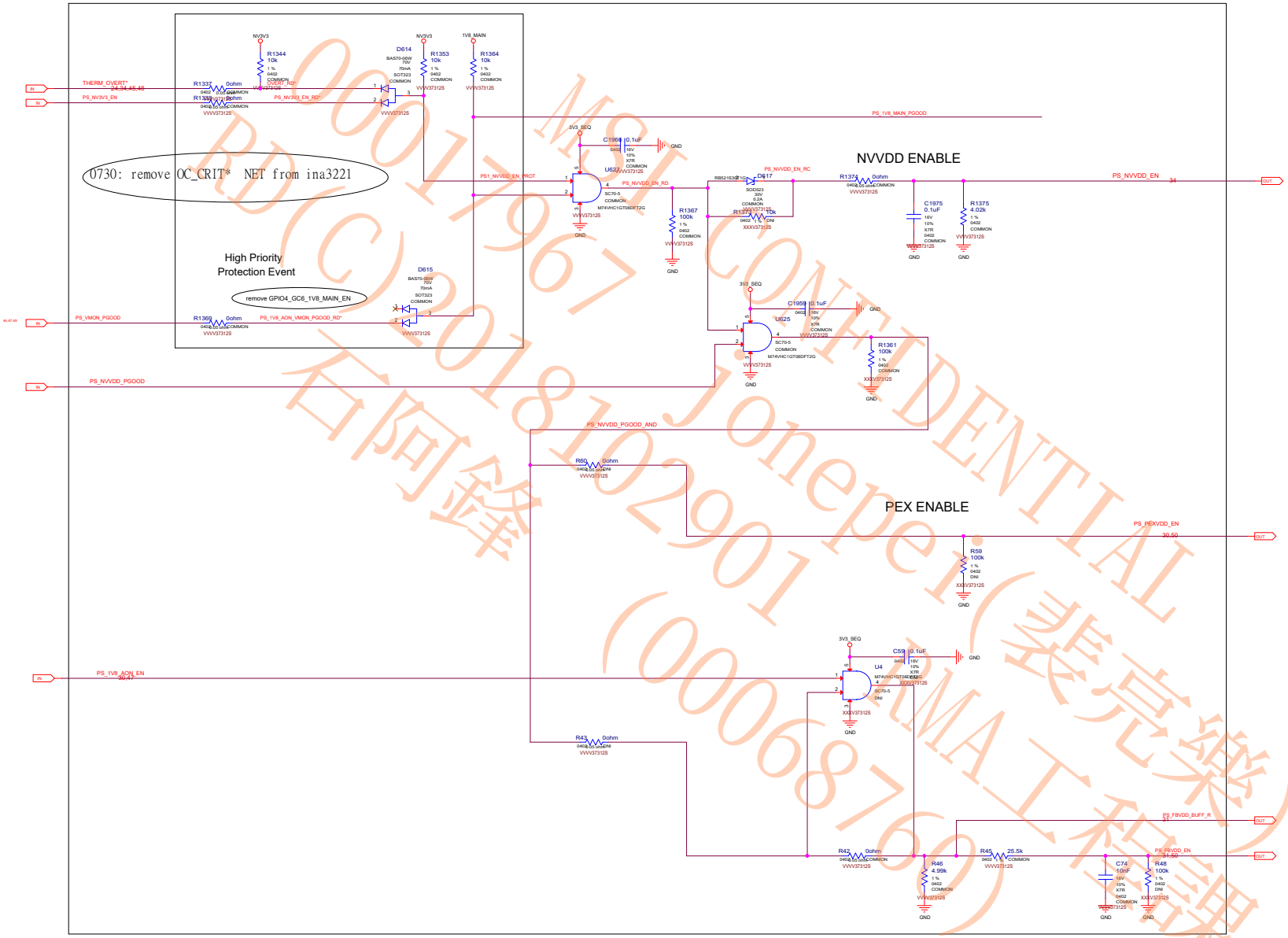
Size Custom	Document Description Page47:SEQUENCE_ 5V, 1V8, NV3V3 E	Rev 7.1
Date: Tuesday, October 23, 2018	Sheet 47 of 54	

PAGE 48: SEQUENCE:NV,PEX,FB ENABLE



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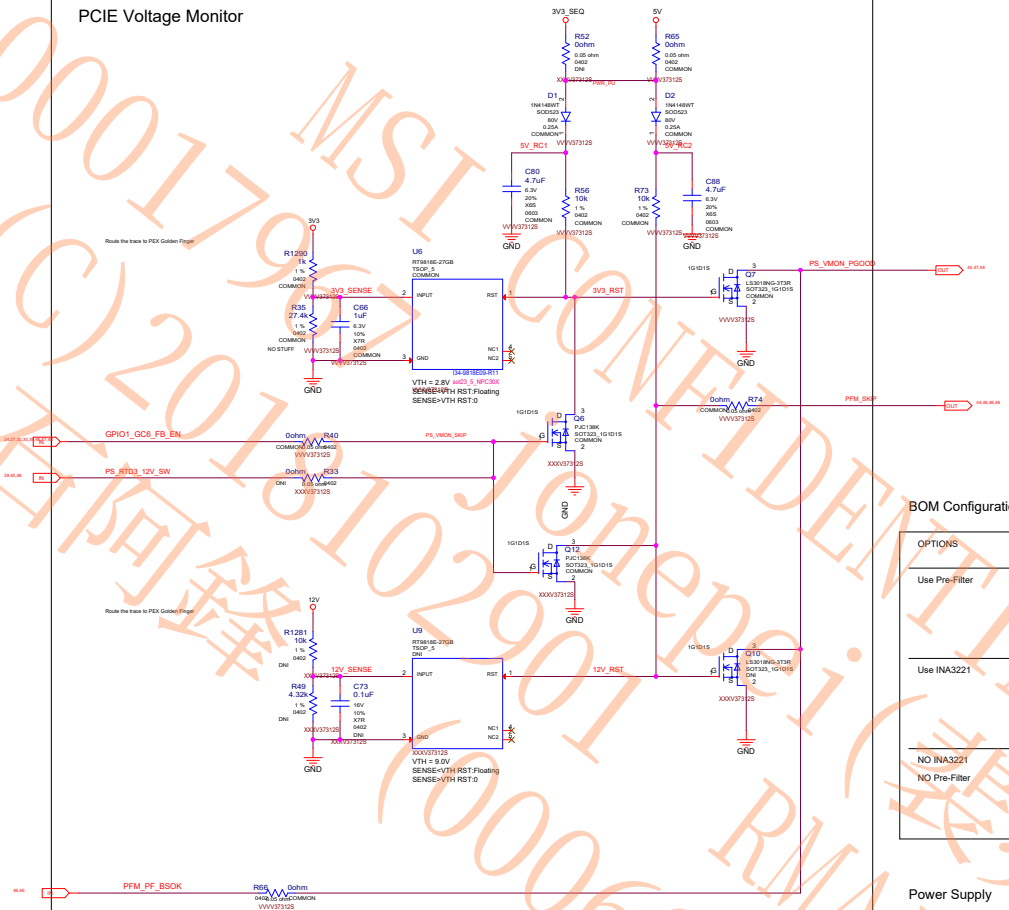
Size	Document Description	Rev
Custom	Page48:SEQUENCE_ NV, PEX, FB ENAB	7.1

Date: Tuesday, October 23, 2018 Sheet 48 of 54

PCIE Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX

and All Input 12Vs

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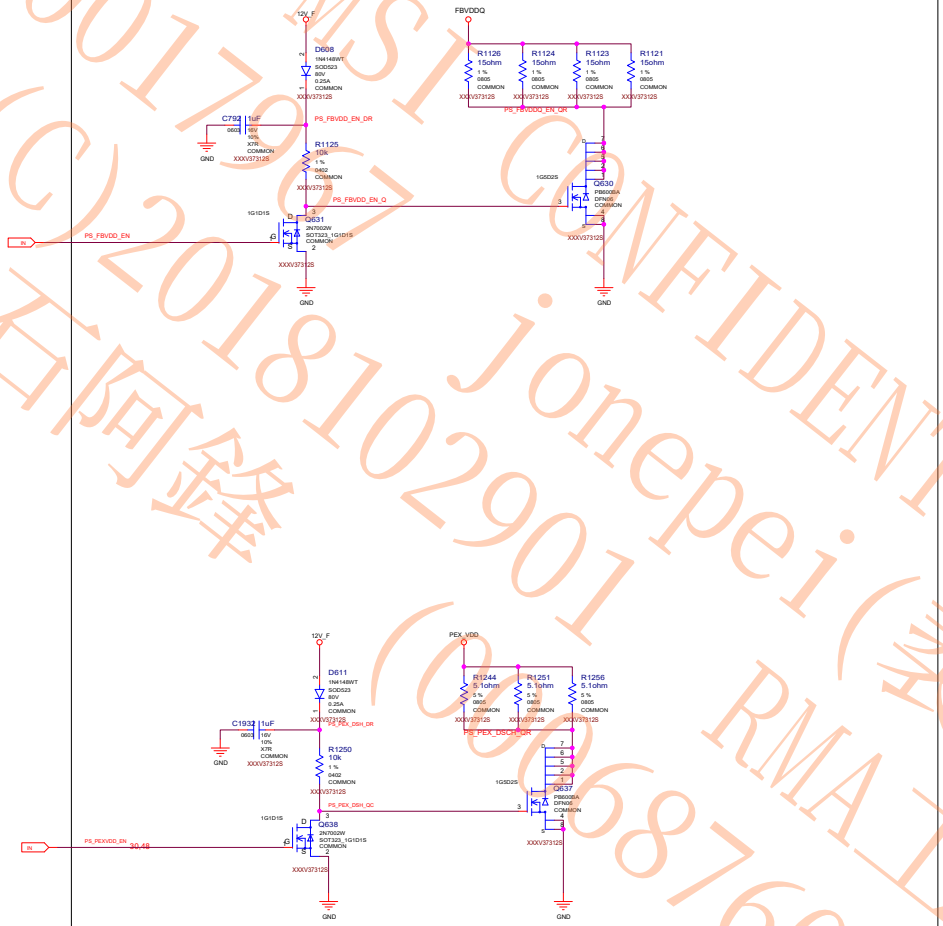
Size: Custom | Document Description: Page49:SEQUENCE_ PCIE VOLTAGE MON | Rev: 7.1
Date: Tuesday, October 23, 2018 | Sheet 49 of 54

PAGE 50: SEQUENCE:DISCHARGE



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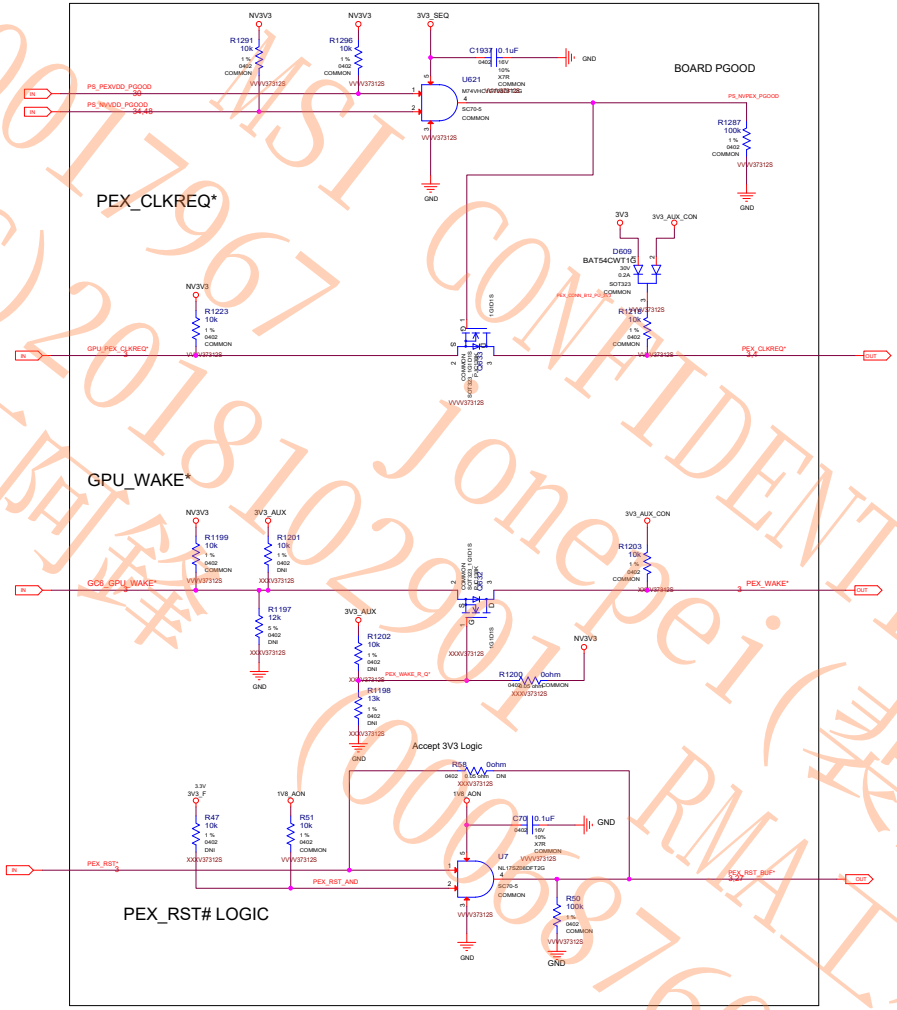
Size: Custom	Document Description: Page50:SEQUENCE_ DISCHARGE
Rev: 7.1	
Date: Tuesday, October 23, 2018	Sheet 50 of 54

PAGE 51: SEQUENCE:MISC



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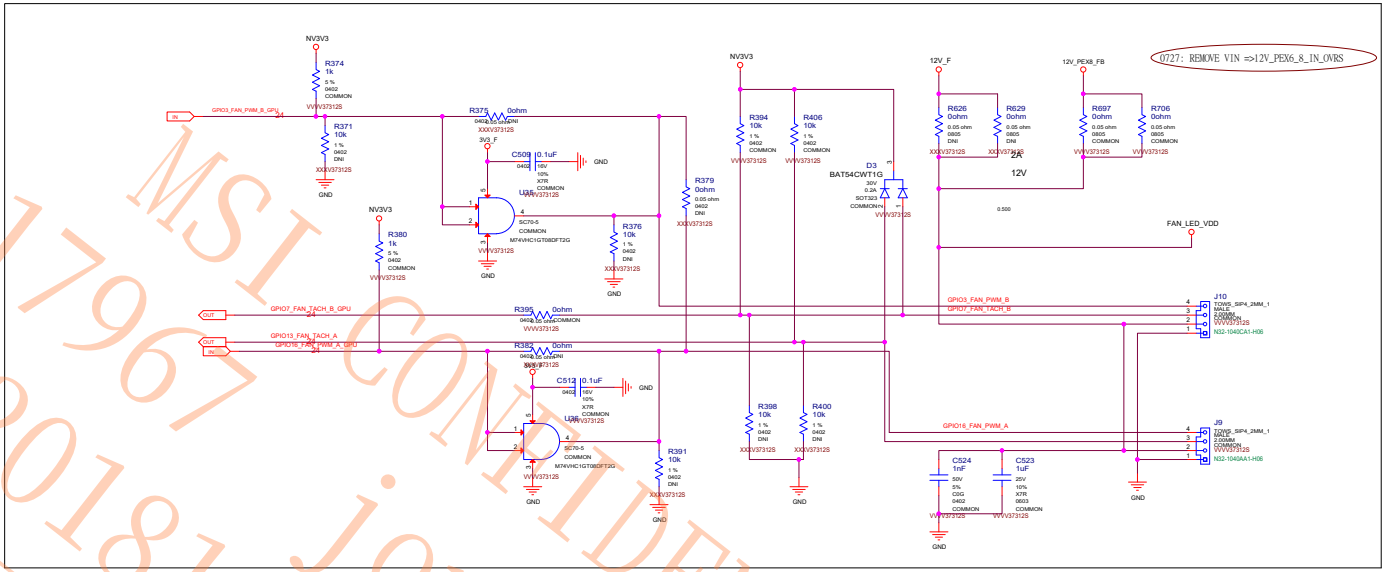
Size	Document Description	Rev
Custom	Page51:SEQUENCE_ MISC	7.1

Date: Tuesday, October 23, 2018 Sheet 51 of 54

PAGE 52: LED & FAN HEADERS



LED BOOST

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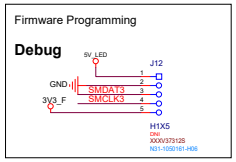
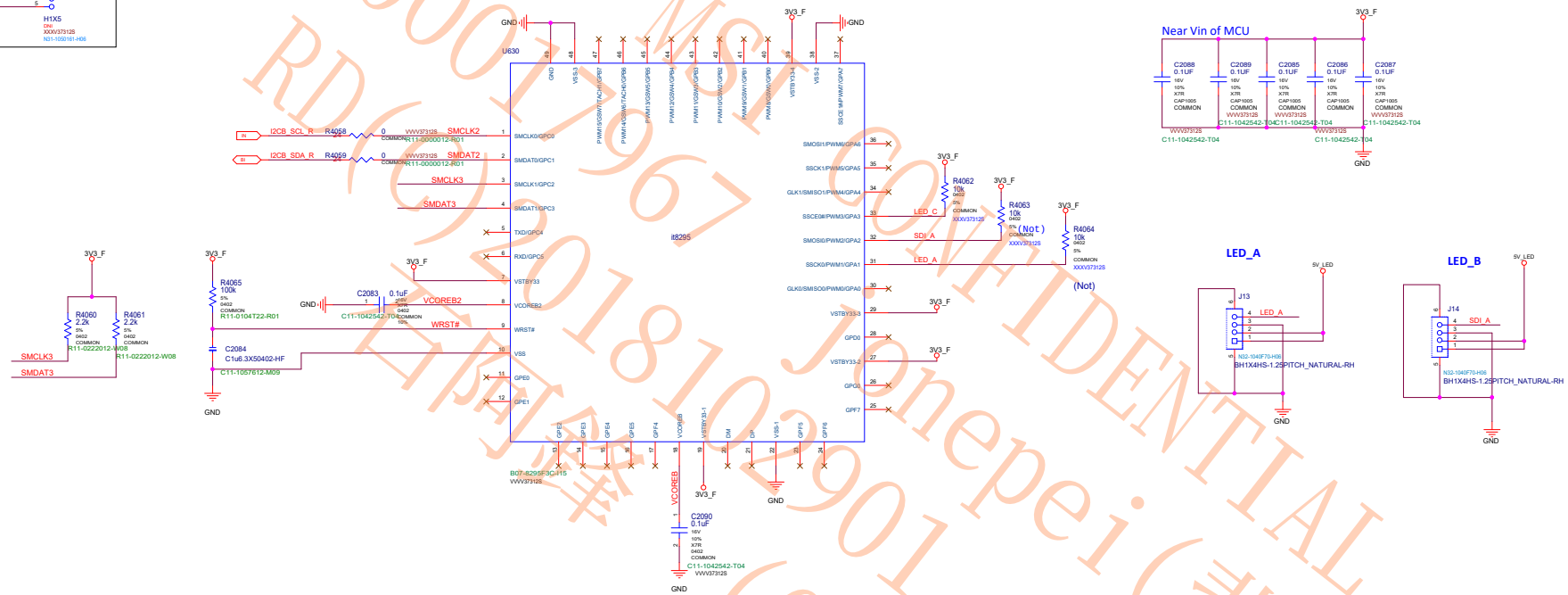
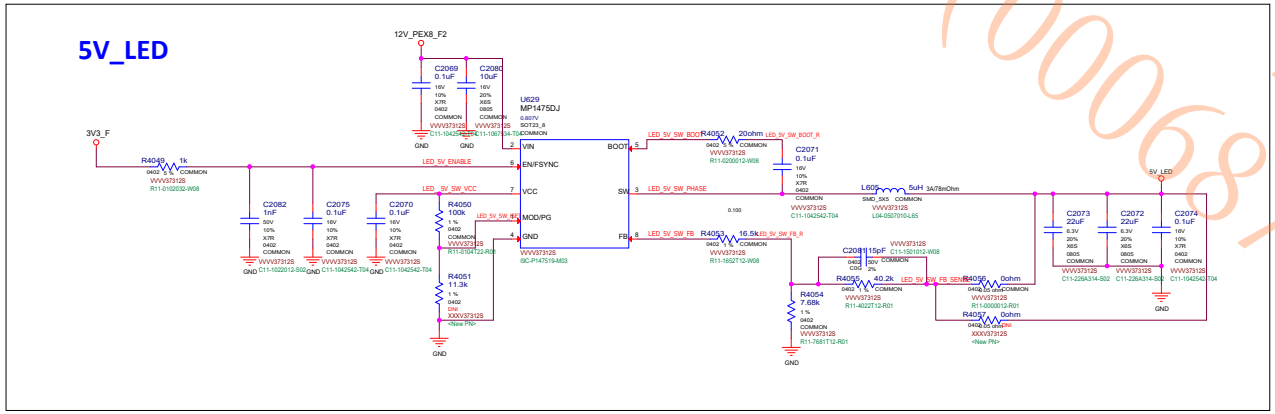
	MS-V373	
Size Custom	Document Description Page52:LED & FAN HEADERS	Rev 7.1
Date: Tuesday, October 23, 2018	Sheet 52 of 54	







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Size: Custom	Document Description: Page53:LED_CONTROLLER_IT8295
Rev: 7.1	
Date: Tuesday, October 23, 2018	Sheet 53 of 54

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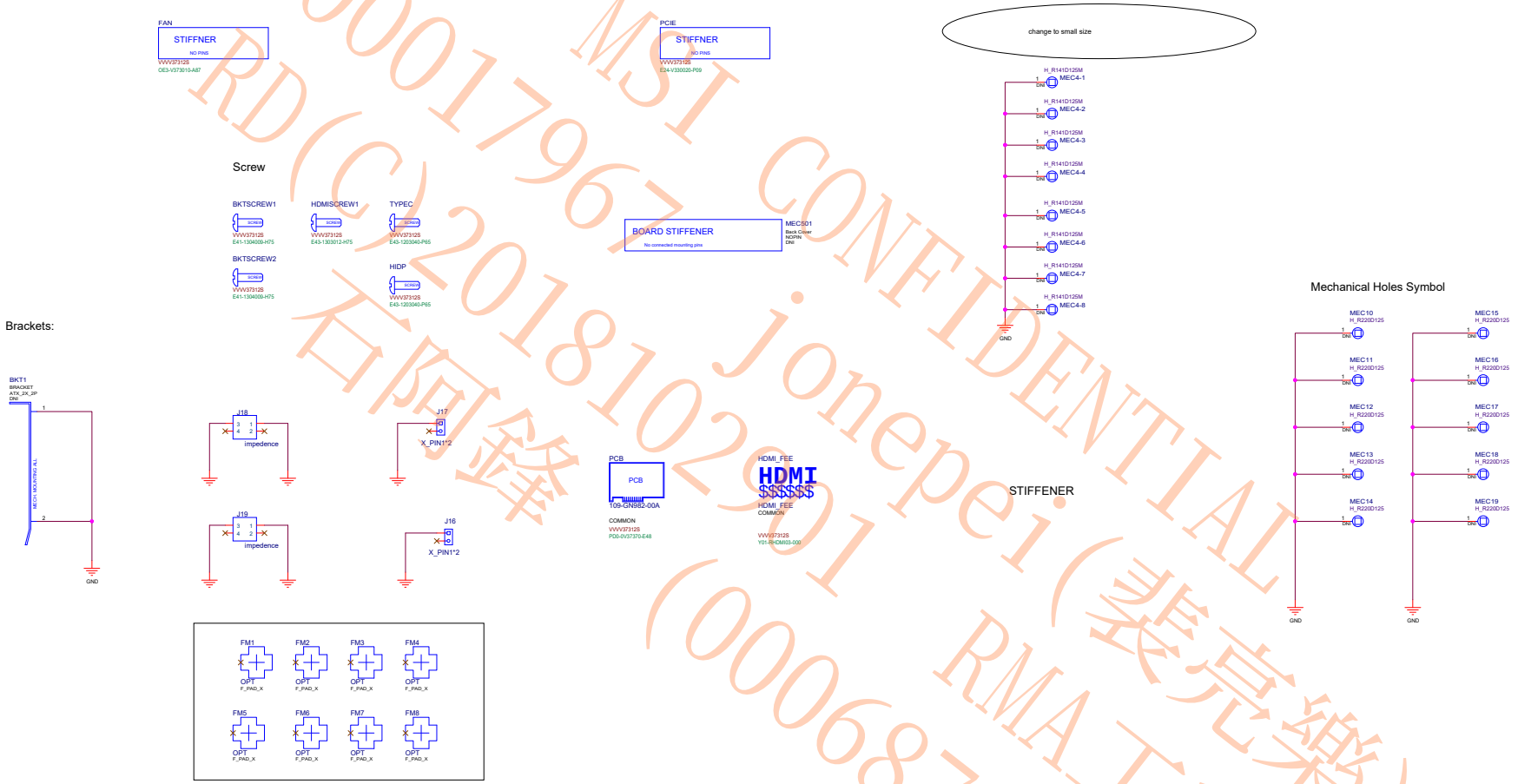
PAGE 54:MECHANICAL;BRACKET/THERMAL SOLUTION



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Size Custom	Document Description Page54:Mechanical_ Bracket_Therma	Rev 7.1
Date: Tuesday, October 23, 2018	Sheet 54 of 54	