PG150-C03

384b GDDR6 x16
TALL DP + DP + DP + HDMI/DP + USB

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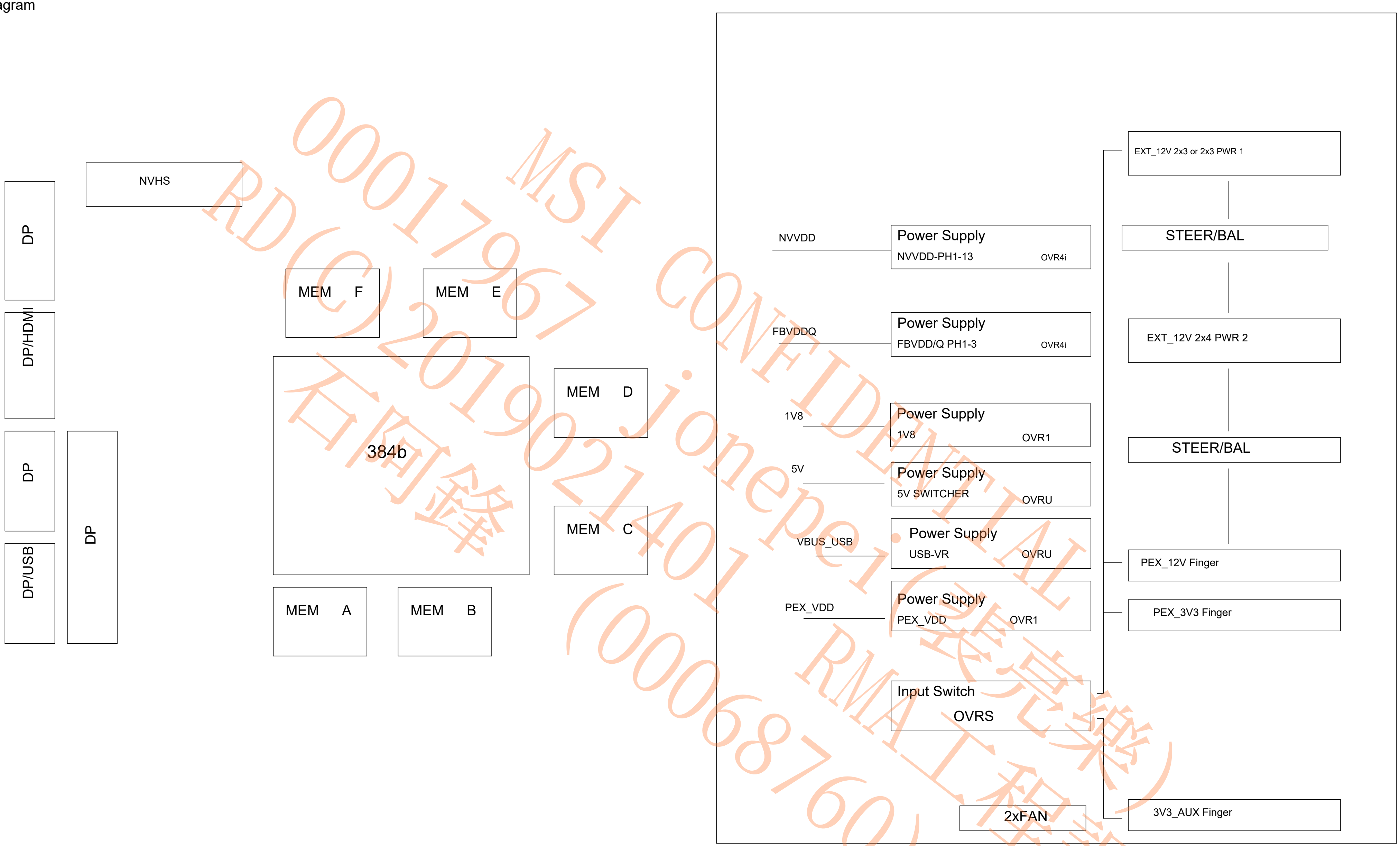
Block Diagram



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PCI Express

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PCI TERM

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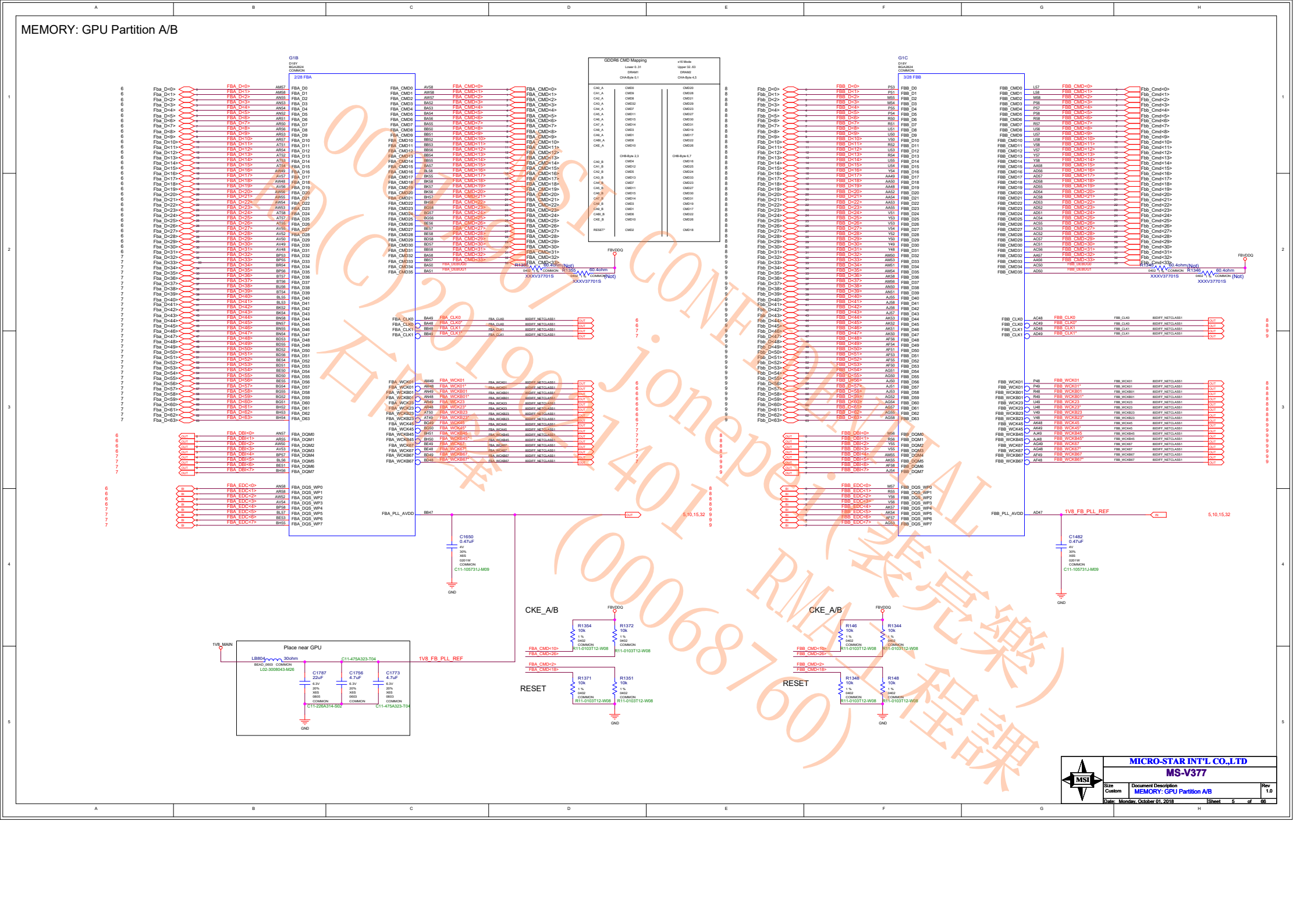
MEMORY: GPU Partition A/B



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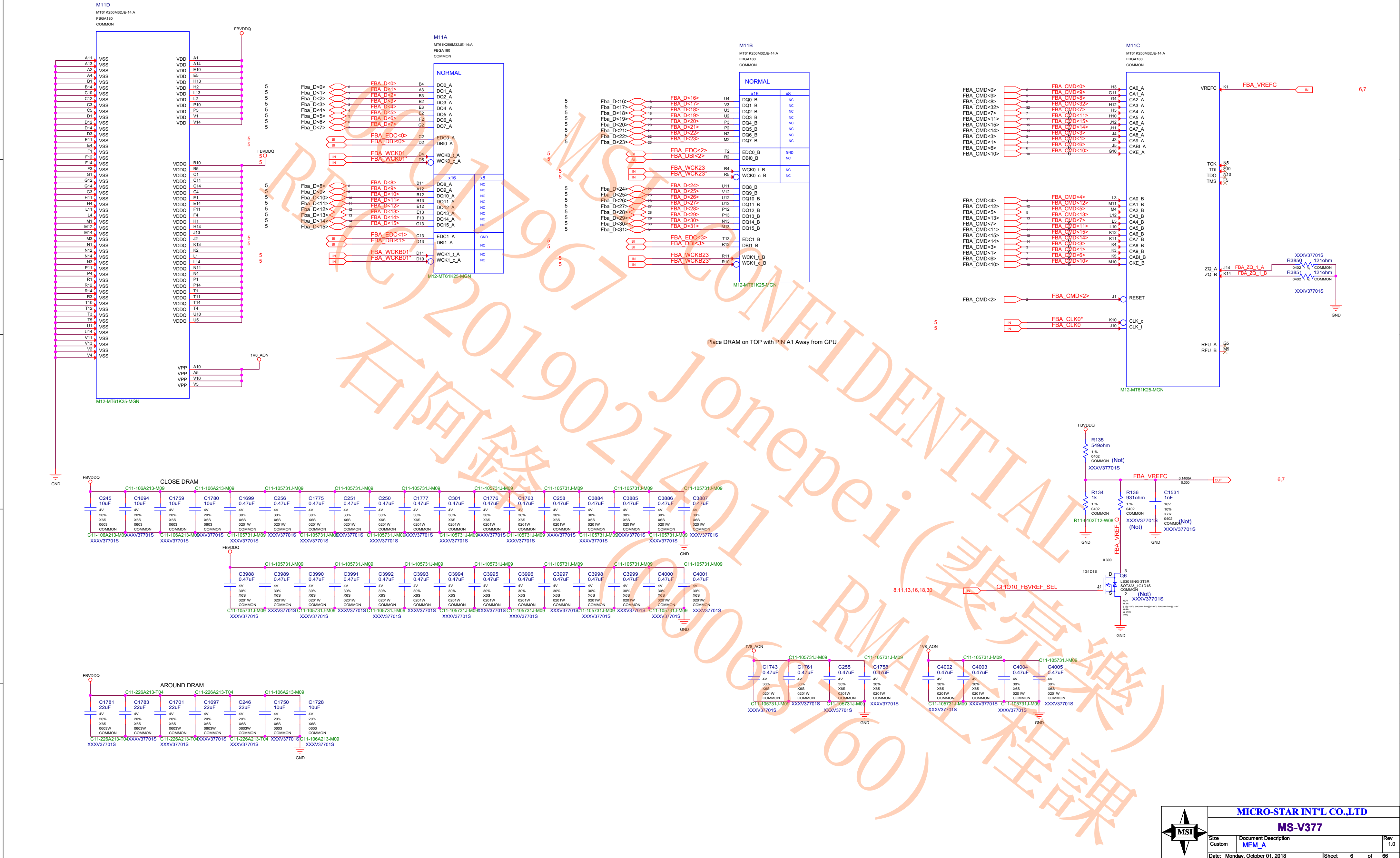

M11D
MT61K256M32JE-14:A
FBGA180
COMMON
M12-MT61K25-MGN
M11A
NORMAL
M11B
M11C
FBVDDQ
1V8_AON
GND
FBA_VREFC
GPIO10_FBVREF_SEL
FBA_CMD<2>
FBA_CLK0*
FBA_CLK0
RESET
Place DRAM on TOP with PIN A1 Away from GPU
CLOSE DRAM
AROUND DRAM
R135 549ohm
R134 1k
R136 931ohm
C1531 1nF
Q6 LS3018NG-3T3R
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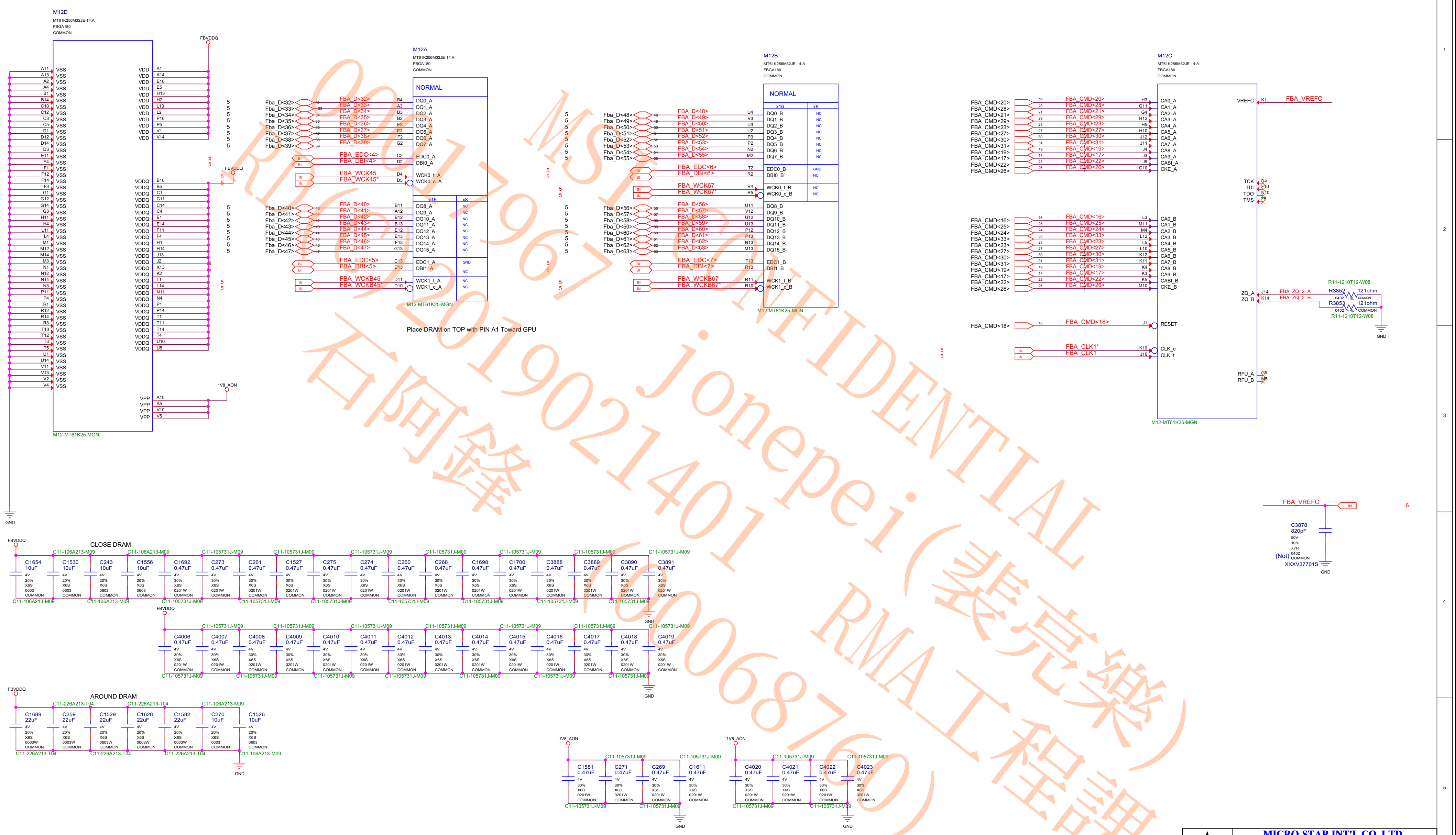
MEMORY: FBA Partition 63..32



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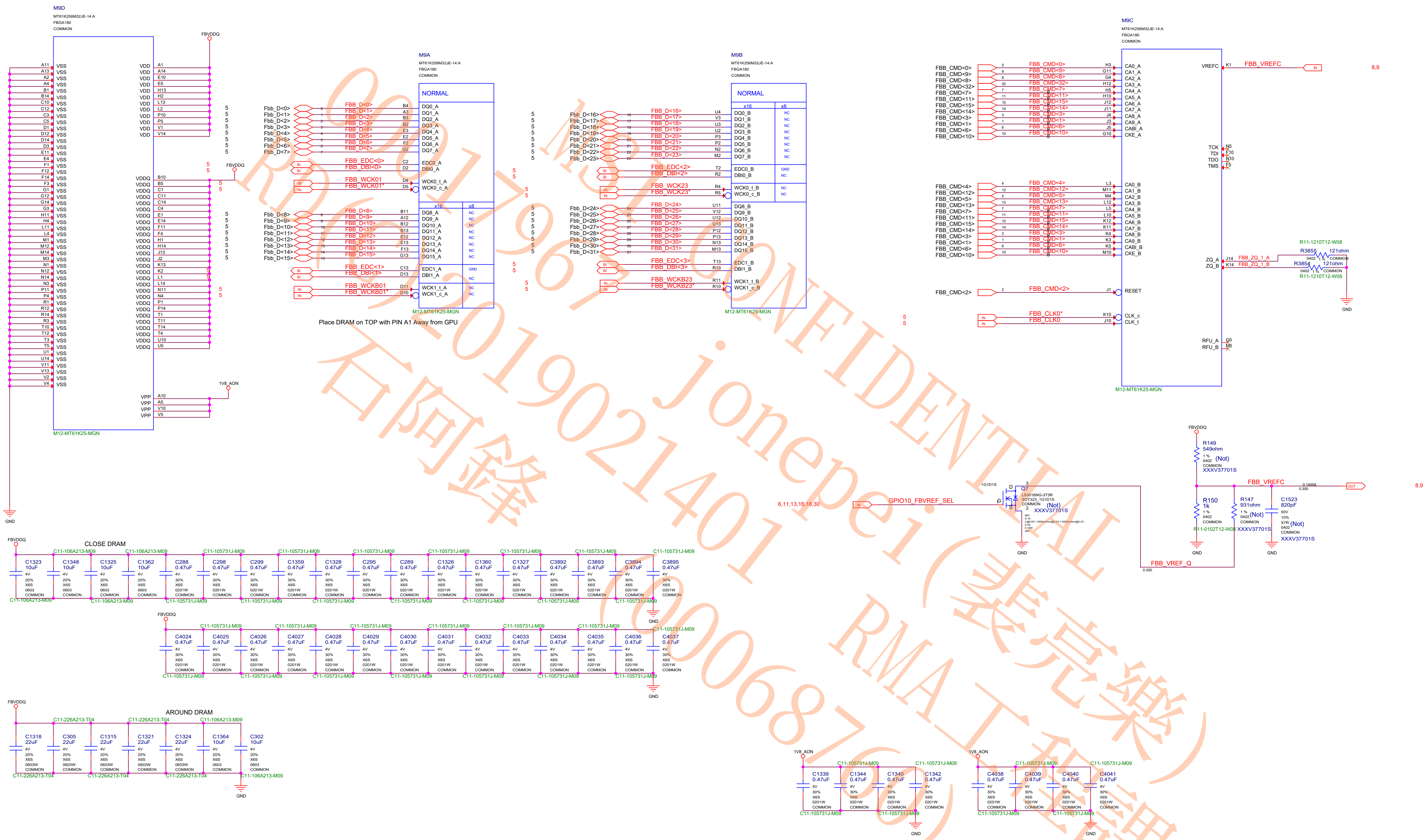
MEMORY: FBB Partition 31..0



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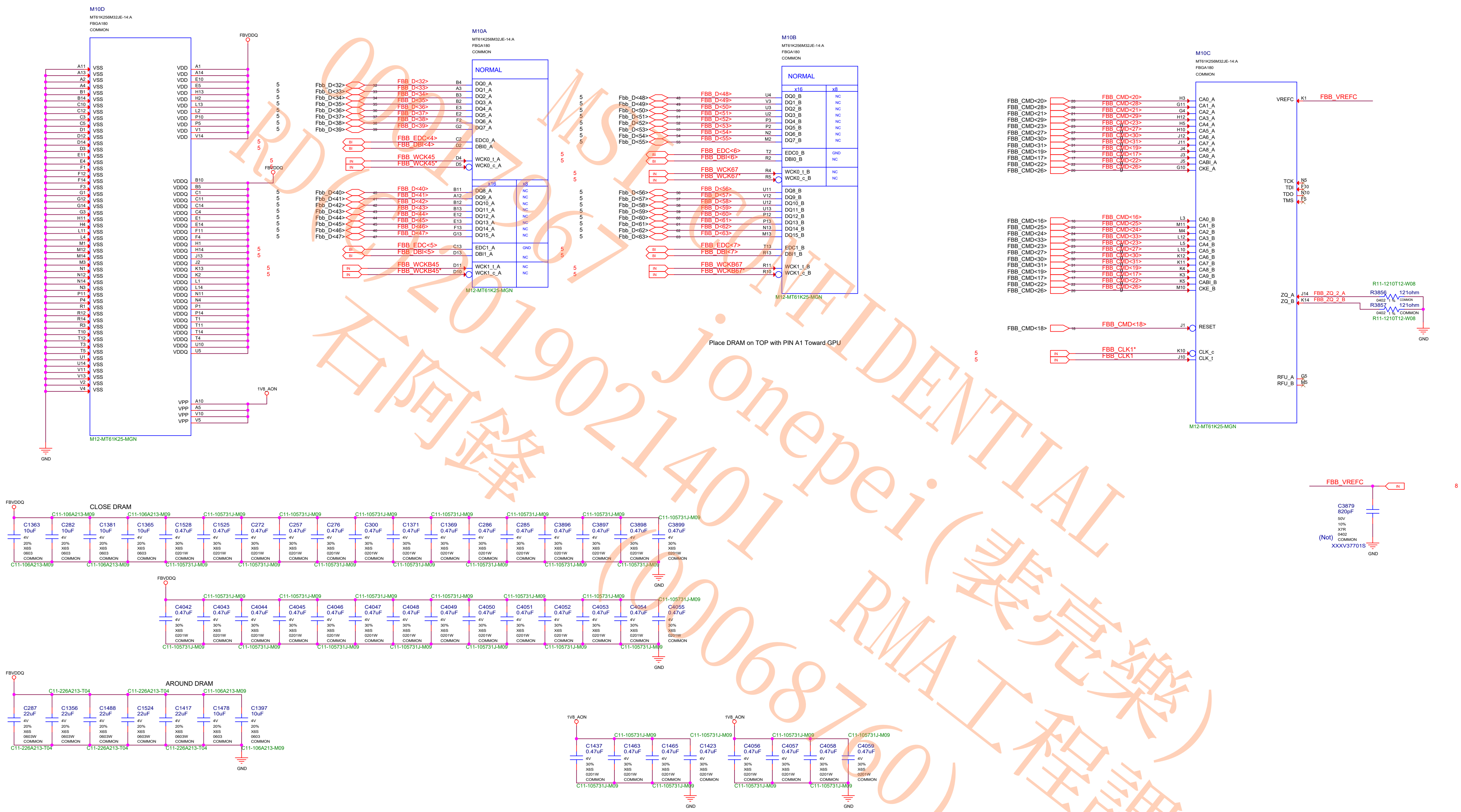
MEMORY: FBB Partition 63..32



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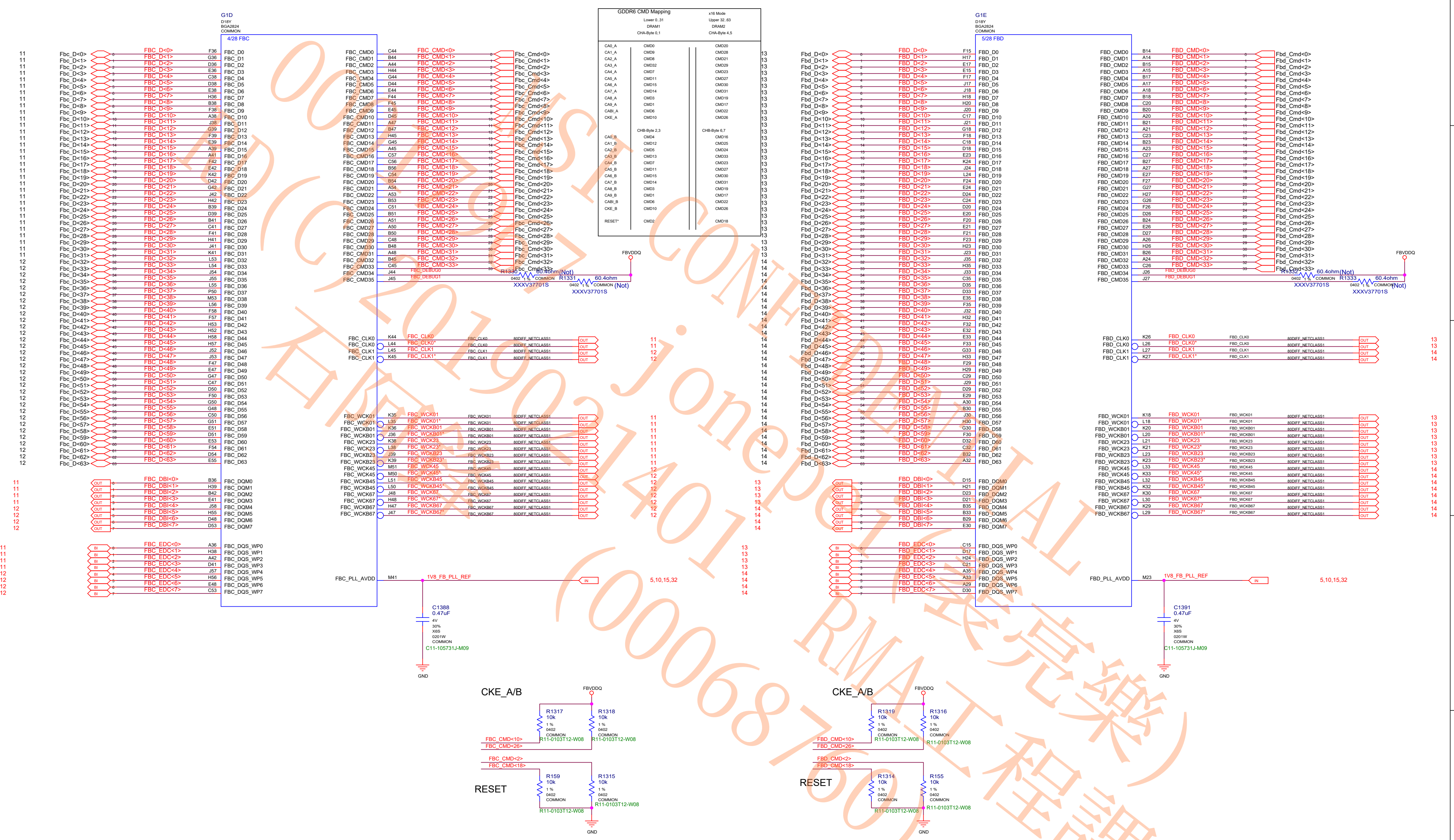

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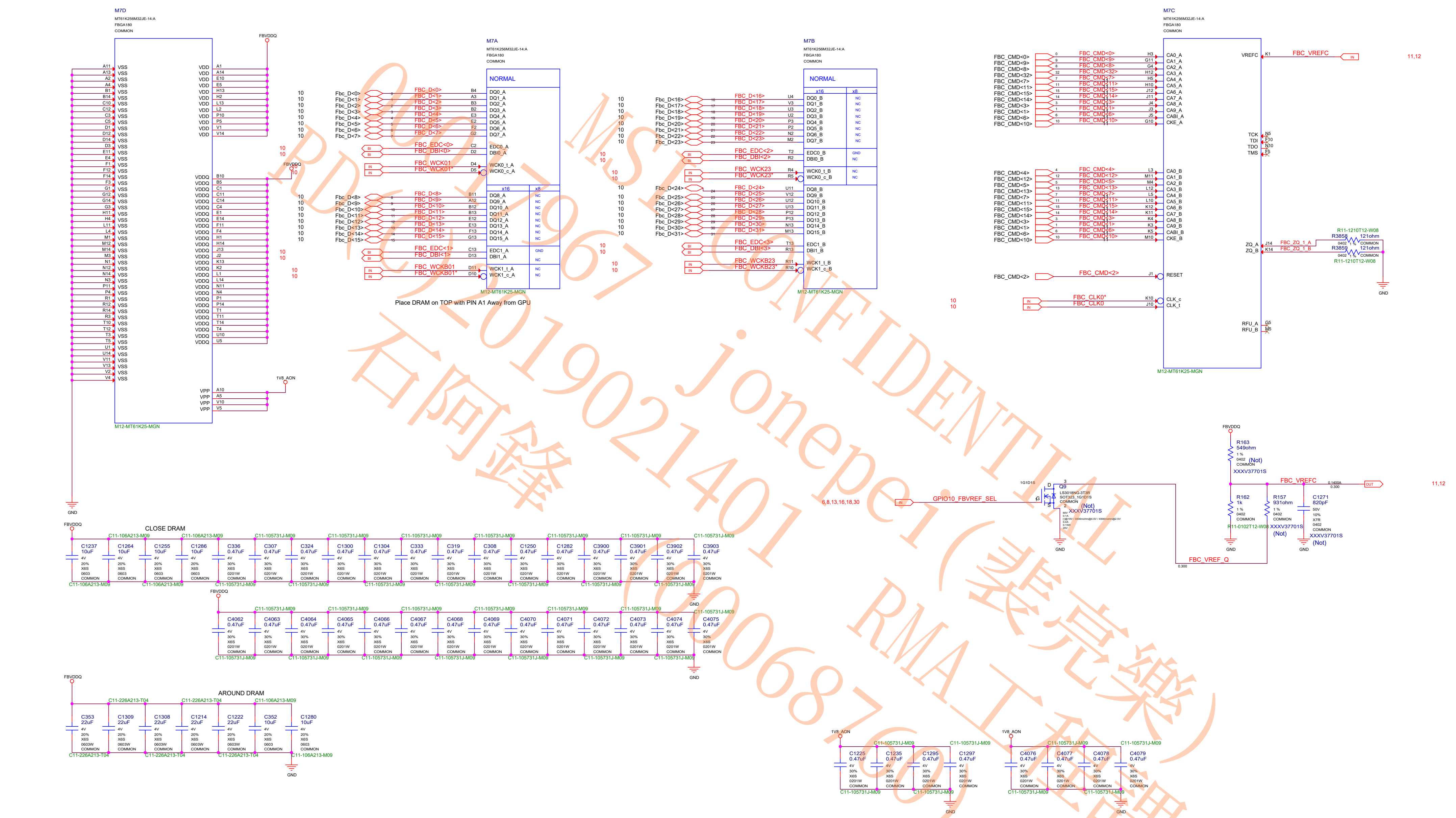
MEMORY: FBC Partition 31..0



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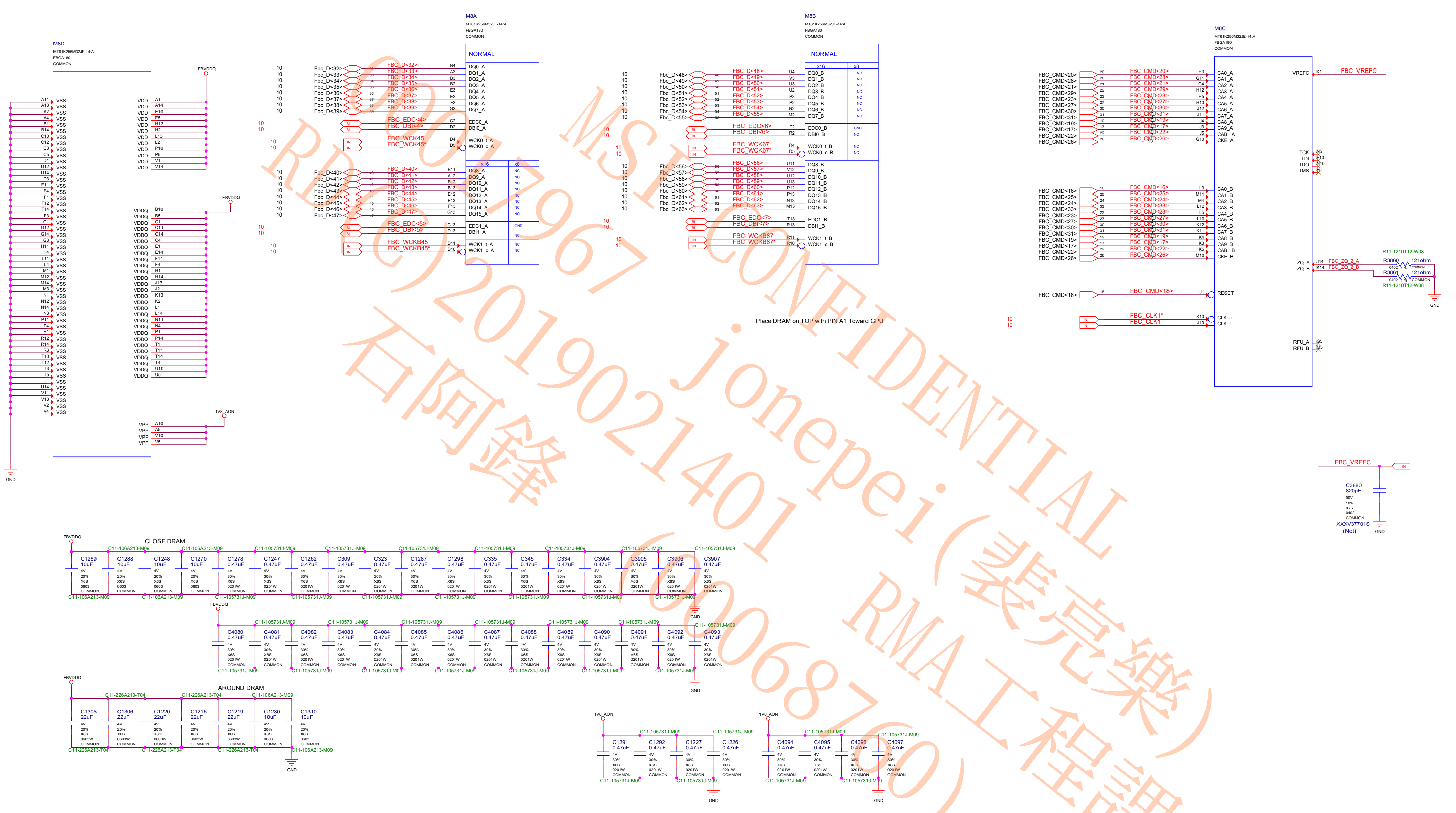
MEMORY: FBC Partition 63..32



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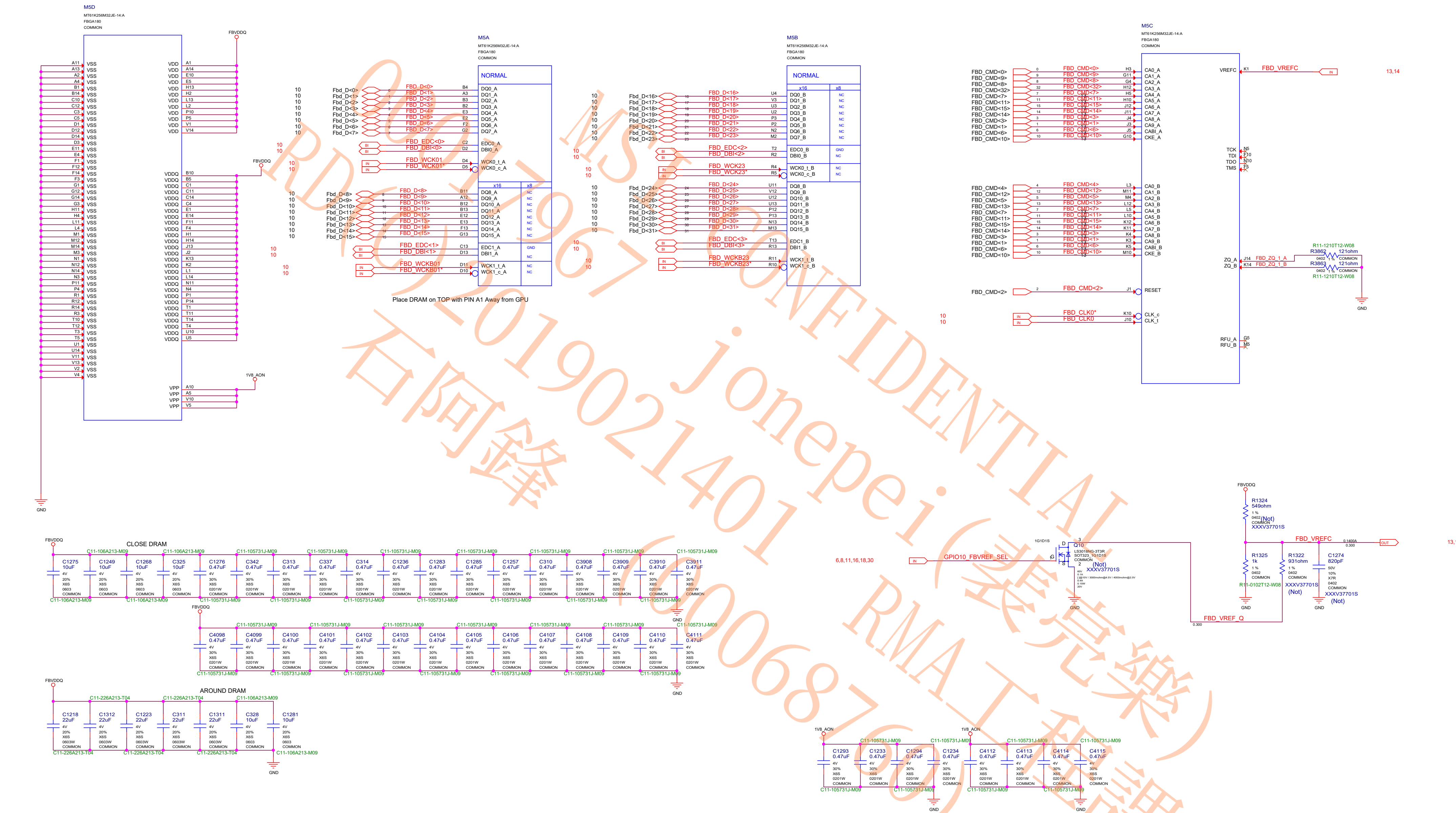

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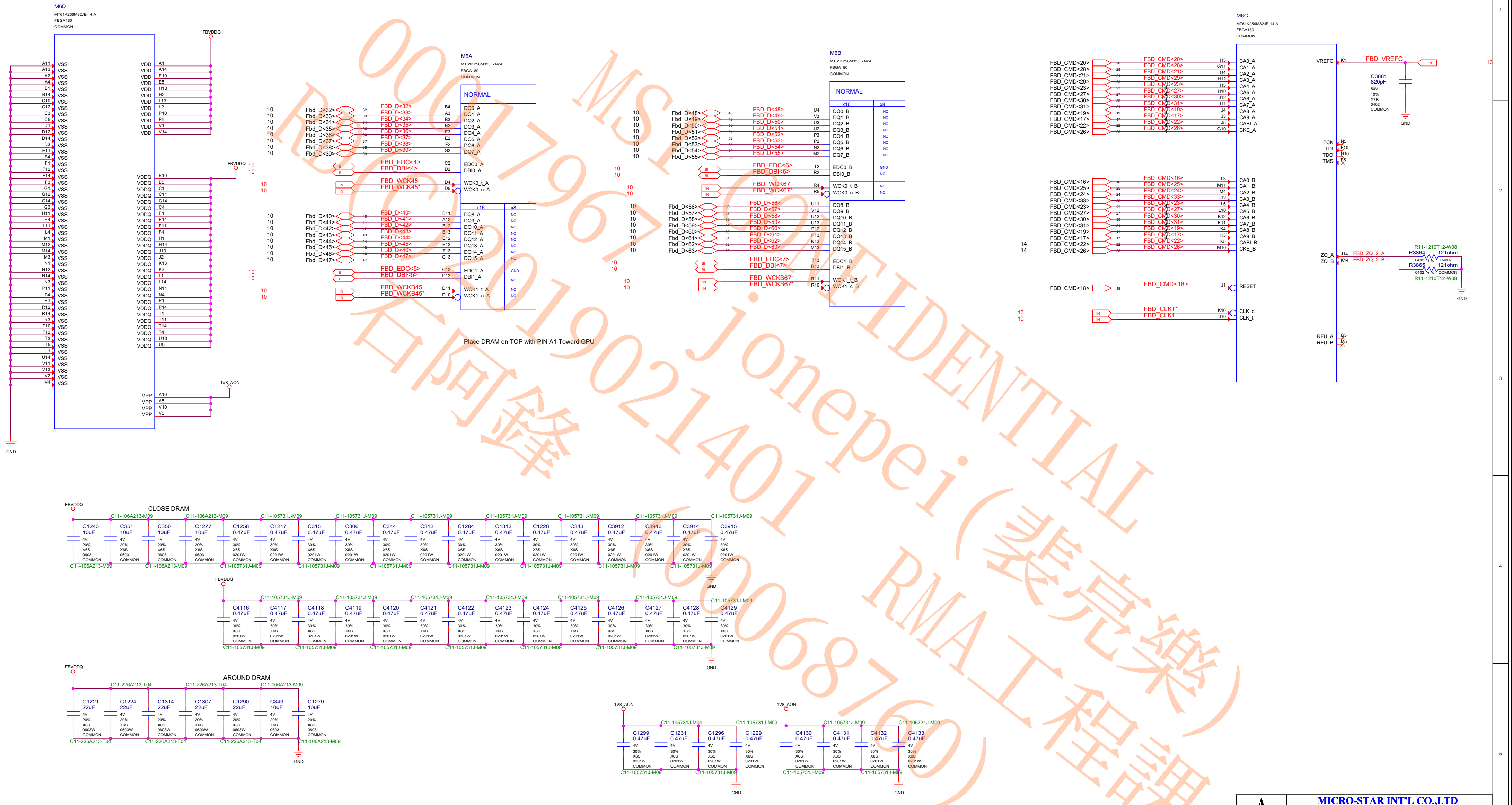
MEMORY: FBD Partition 63..32



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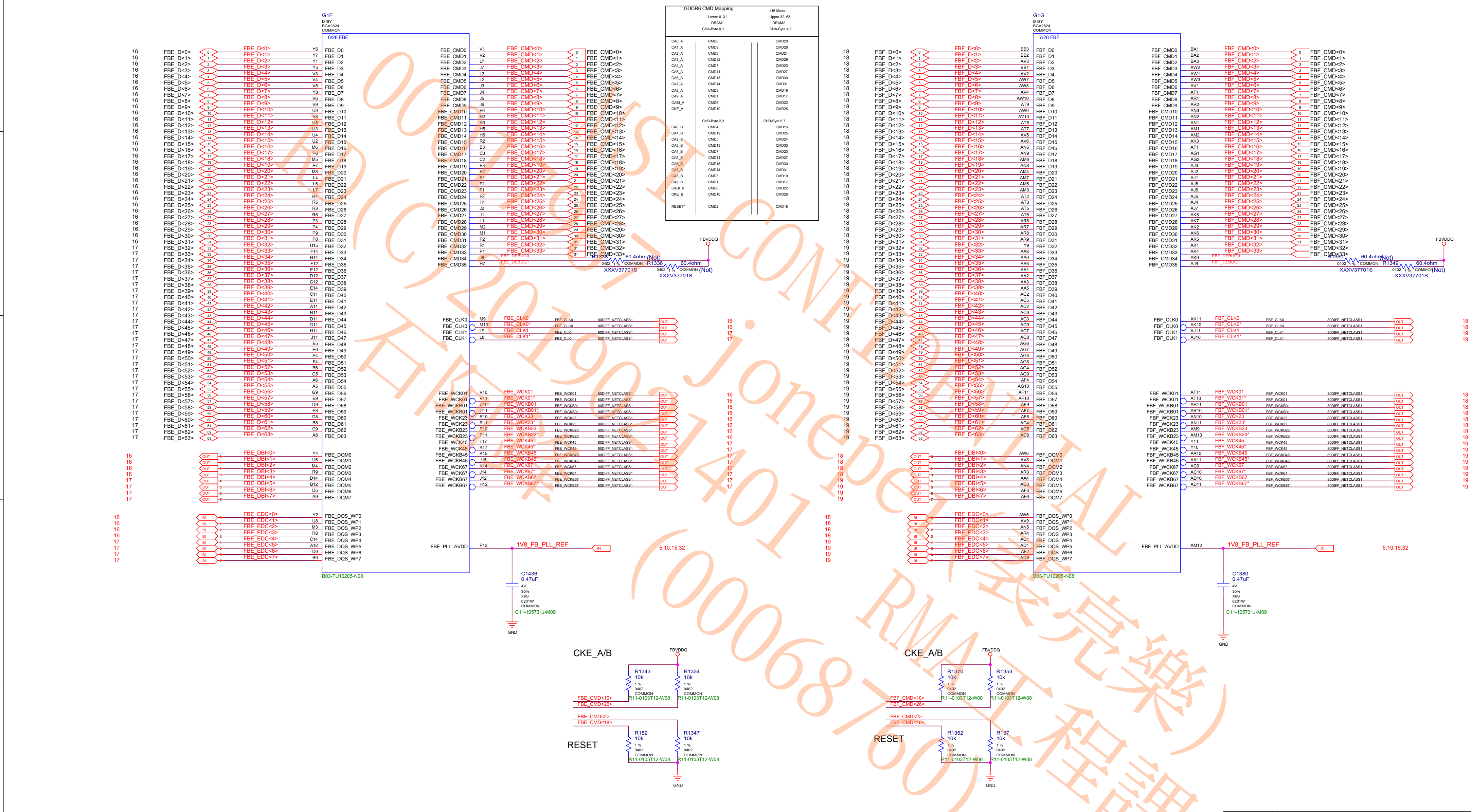

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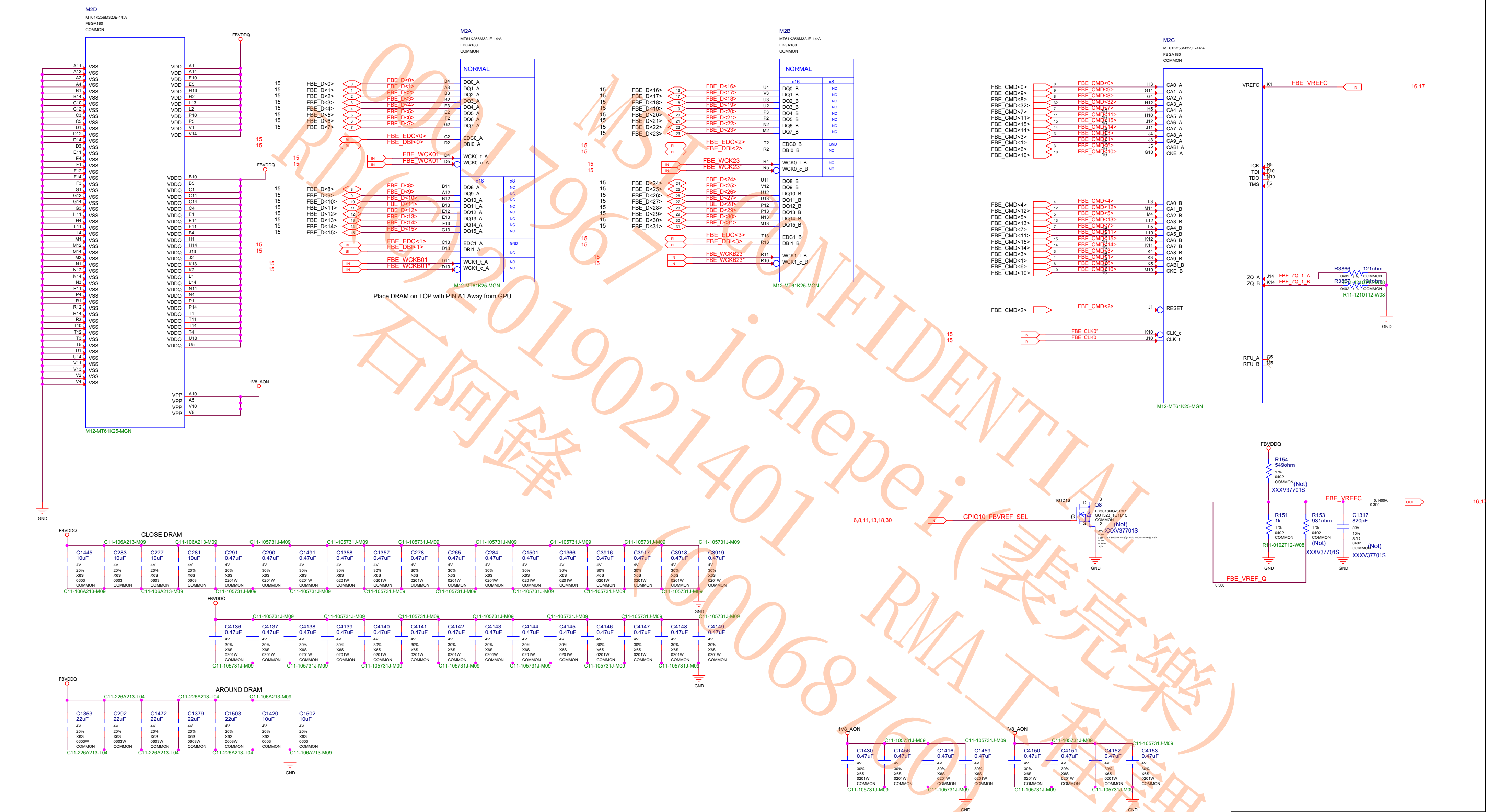
MEMORY: FBE Partition 31..0



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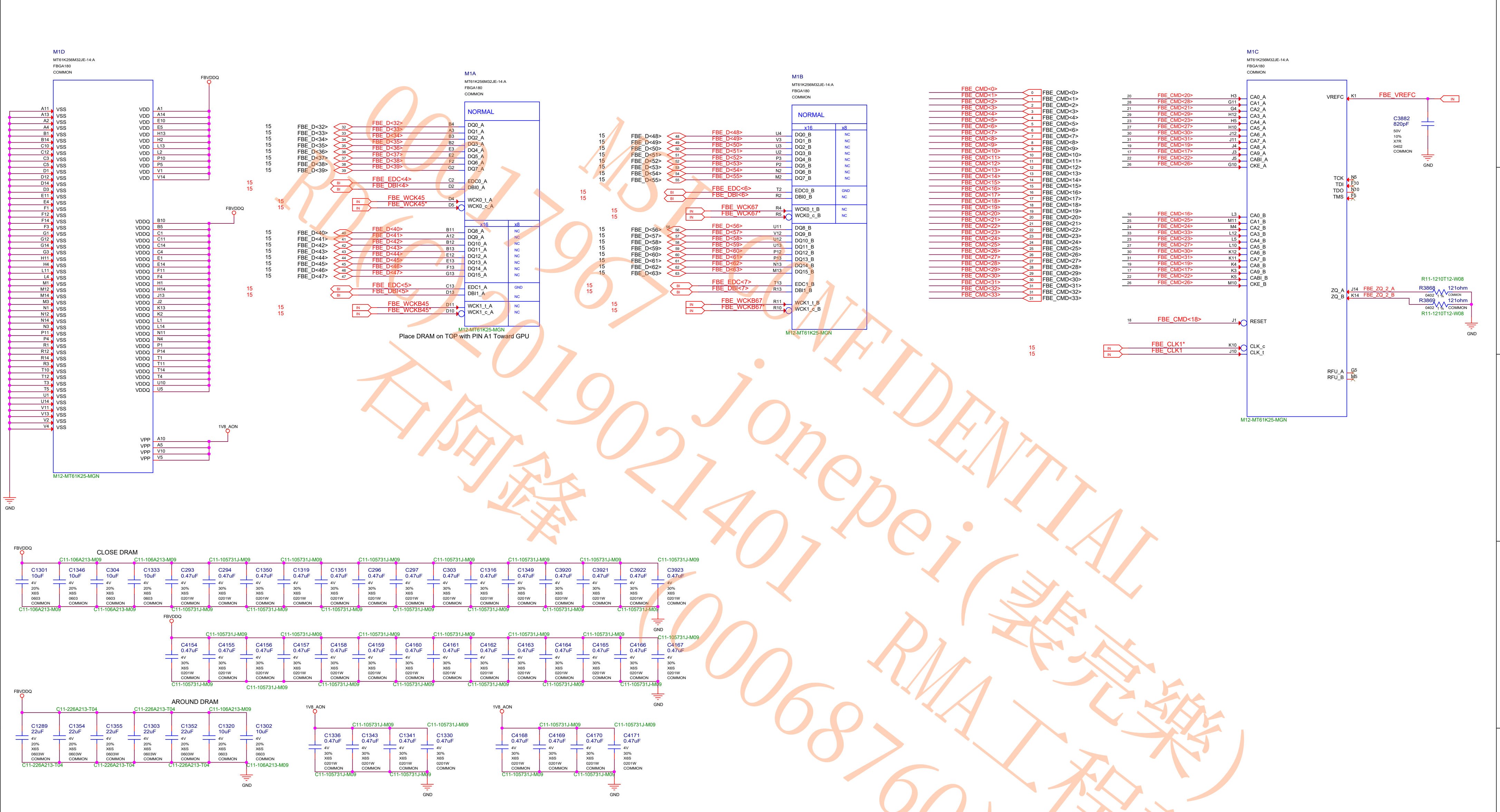
MEMORY: FBE Partition 63..32



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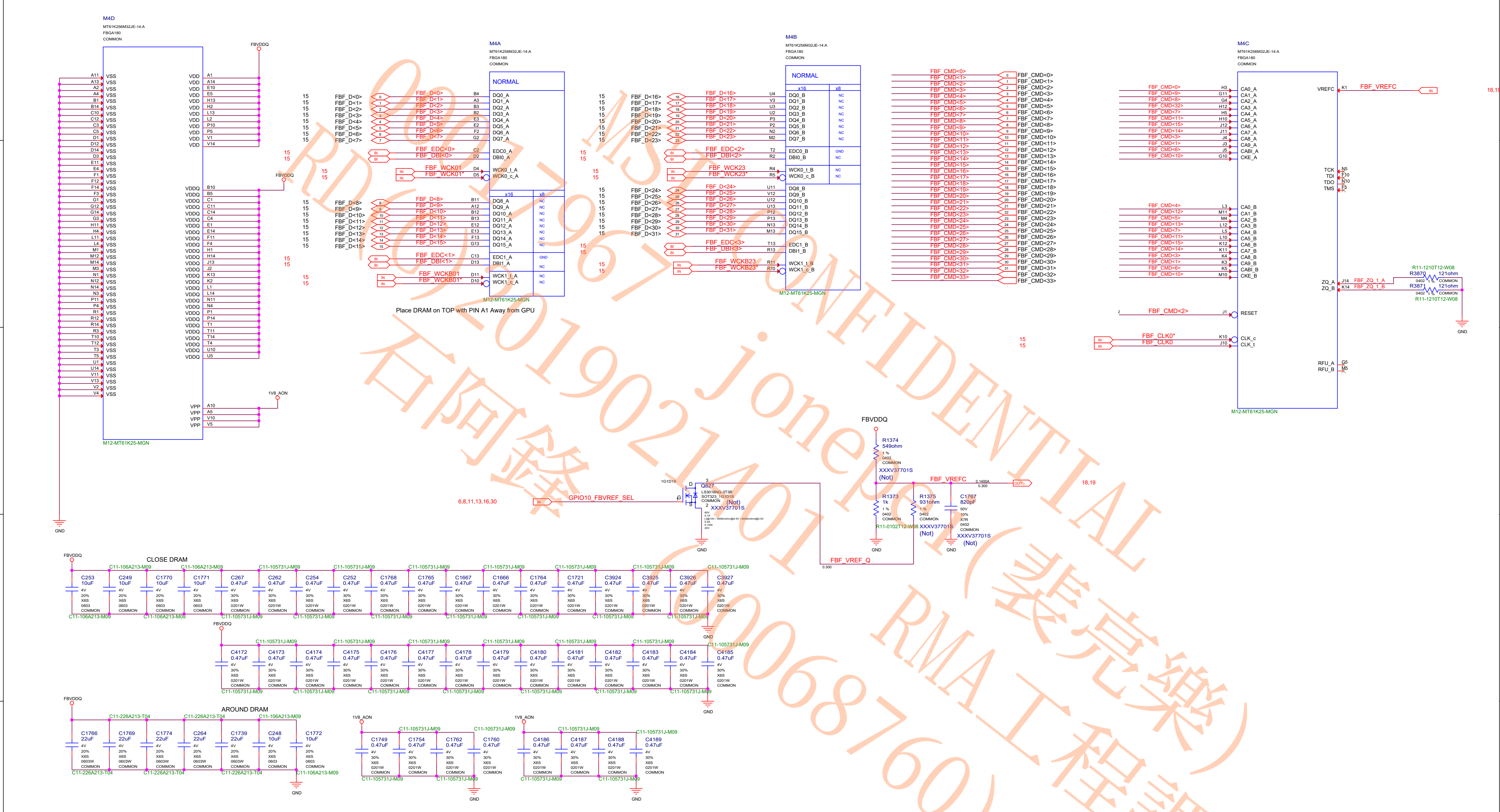
MEMORY: FBF Partition 31..0



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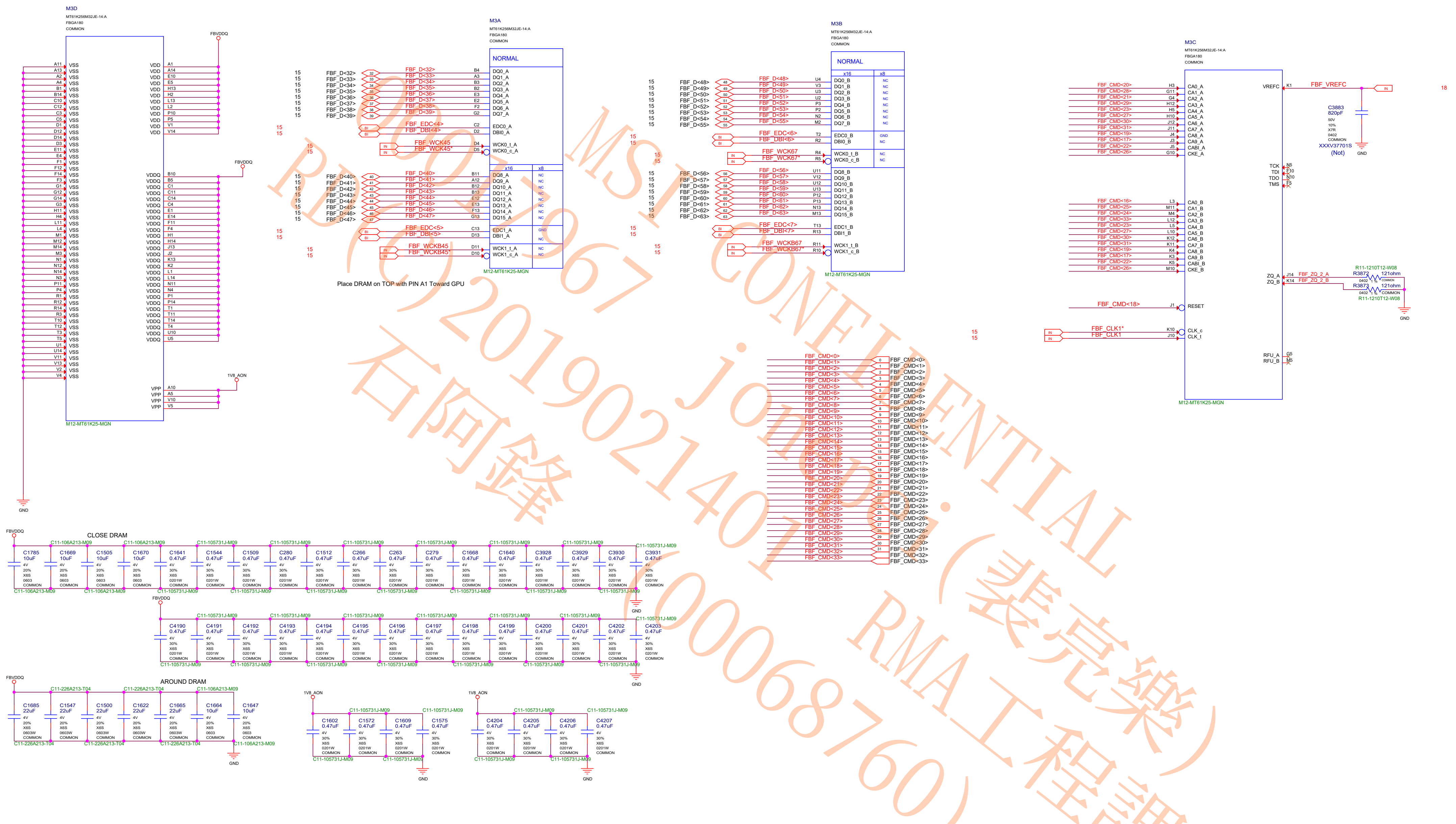

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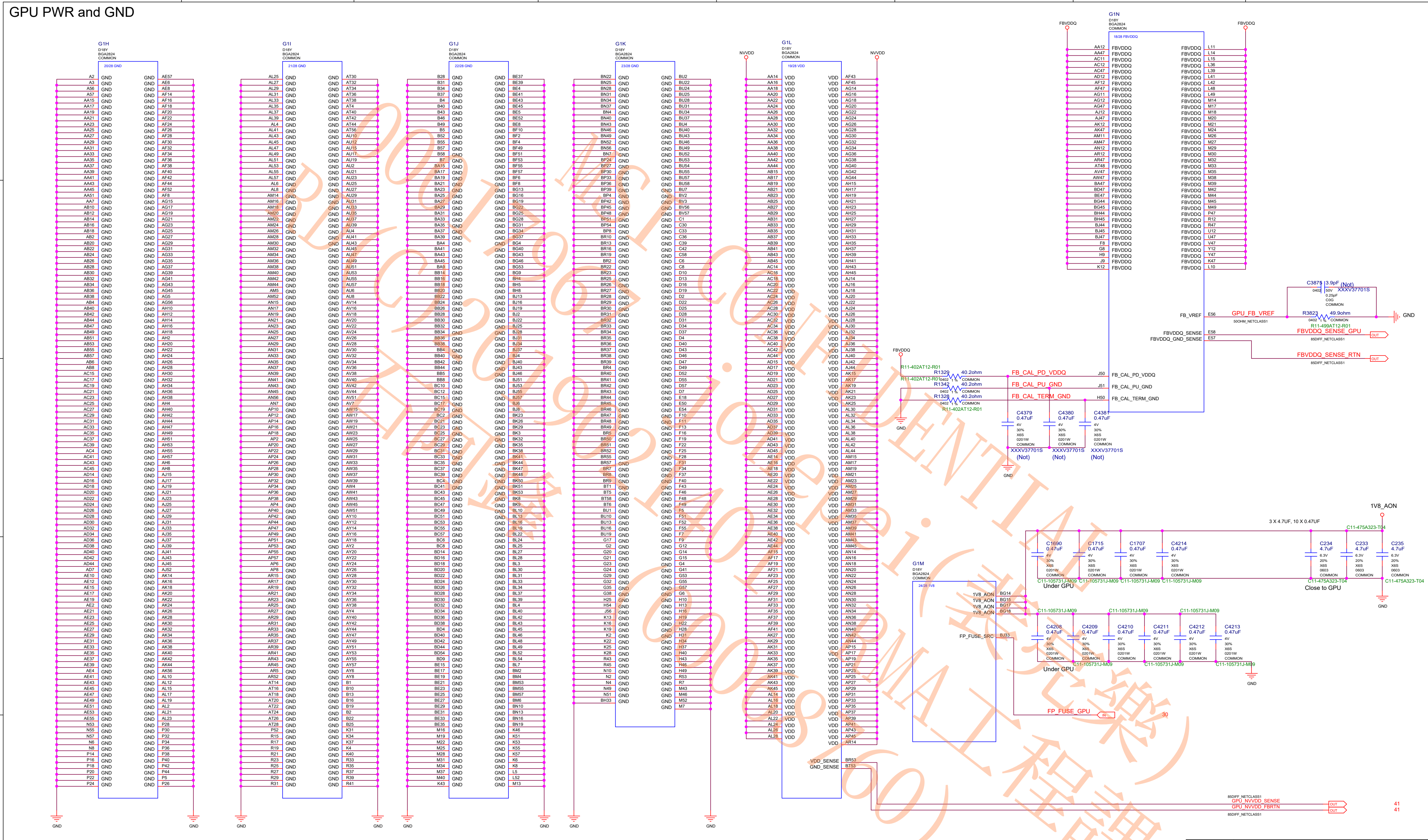
GPU PWR and GND



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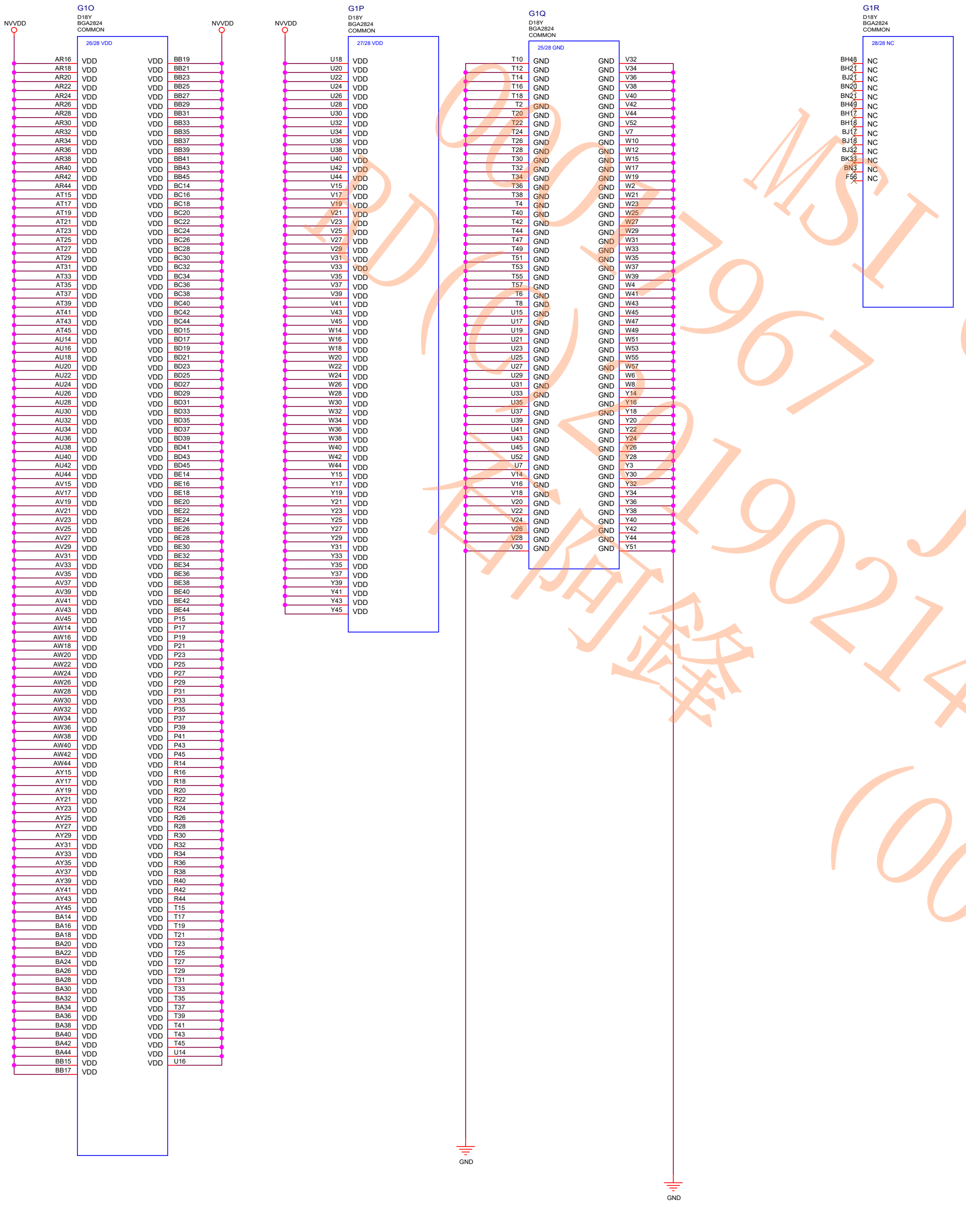
GPU PWR GND NCs



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GPU Decoupling

FBVDDQ

FBVDDQ

Partition A
2 X 10UF, 6 X 0.47UF

C1616 0.47uF, C1704 0.47uF, C1583 0.47uF, C1599 0.47uF, C1557 0.47uF, C1555 0.47uF, C1639 10uF, C1734 10uF

Partition B
2 X 10UF, 6 X 0.47UF

C1508 0.47uF, C1438 0.47uF, C1386 0.47uF, C1457 0.47uF, C1497 0.47uF, C1468 0.47uF, C1534 10uF, C1428 10uF

Partition C
2 X 10UF, 6 X 0.47UF

C1387 0.47uF, C1374 0.47uF, C1383 0.47uF, C1401 0.47uF, C1375 0.47uF, C1411 0.47uF, C1361 10uF, C1376 10uF

Partition D
2 X 10UF, 6 X 0.47UF

C1392 0.47uF, C1368 0.47uF, C1373 0.47uF, C1367 0.47uF, C1382 0.47uF, C1385 0.47uF, C1378 10uF, C1384 10uF

Partition E
2 X 10UF, 6 X 0.47UF

C1427 0.47uF, C1443 0.47uF, C1418 0.47uF, C1458 0.47uF, C1393 0.47uF, C1370 0.47uF, C1398 10uF, C1464 10uF

Partition F
2 X 10UF, 6 X 0.47UF

C1568 0.47uF, C1473 0.47uF, C1587 0.47uF, C1507 0.47uF, C1545 0.47uF, C1489 0.47uF, C1629 10uF, C1579 10uF

Place close to GPU
6 X 10UF

C1377 10uF, C1331 10uF, C1372 10uF, C1576 10uF, C1744 10uF, C1347 10uF

Place close to GPU
14 x 22UF

C1684 22uF, C1334 22uF, C1337 22uF, C1511 22uF, C1553 22uF, C1332 22uF, C1421 22uF

C1470 22uF, C1338 22uF, C1399 22uF, C1439 22uF, C1335 22uF, C1610 22uF, C1607 22uF

NVVDD

NVVDD

1 X 470UF + 10 x 47UF overlap

C1577 470uF, C1561 47uF, C1562 47uF, C1592 47uF, C1564 47uF, C1593 47uF, C1567 47uF, C1595 47uF, C1566 47uF, C1596 47uF, C1597 47uF

PCB CO-LAYOUT

1 X 470UF + 10 x 47UF overlap

C1467 470uF, C1479 47uF, C1480 47uF, C1447 47uF, C1485 47uF, C1448 47uF, C1486 47uF, C1452 47uF, C1449 47uF, C1481 47uF, C1450 47uF

PCB CO-LAYOUT

12 X 47UF

C1590 22uF, C1591 22uF, C1446 47uF, C1559 47uF, C1563 47uF, C1565 22uF, C1589 47uF, C1487 22uF, C1453 22uF, C1484 22uF, C1451 22uF, C1483 47uF

6 X 22UF

C1455 22uF, C1624 22uF, C1422 22uF, C1434 22uF, C1594 22uF, C1623 22uF

30 X 10UF

C1653 10uF, C1652 10uF, C1651 10uF, C1642 10uF, C1403 10uF, C1514 10uF, C1521 10uF, C1400 10uF, C1515 10uF, C1517 10uF, C1686 10uF, C1615 10uF, C1614 10uF, C1638 10uF, C1636 10uF, C1516 10uF, C1520 10uF, C1519 10uF, C1518 10uF, C1513 10uF

C1645 10uF, C1644 10uF, C1643 10uF, C1677 10uF, C1543 10uF, C1432 10uF, C1620 10uF, C1433 10uF, C1407 10uF, C1536 10uF

16 X 4.7UF

C1541 4.7uF, C1424 4.7uF, C1619 4.7uF, C1429 4.7uF, C1634 4.7uF, C1539 4.7uF, C1617 4.7uF, C1425 4.7uF, C1535 4.7uF, C1537 4.7uF, C1626 4.7uF, C1431 4.7uF, C1542 4.7uF, C1404 4.7uF, C1540 4.7uF, C1538 4.7uF

80 X 0.47UF

C1442 0.47uF, C1462 0.47uF, C1419 0.47uF, C1660 0.47uF, C1510 0.47uF, C1631 0.47uF, C1569 0.47uF, C1532 0.47uF, C1406 0.47uF, C1414 0.47uF, C1627 0.47uF, C1548 0.47uF, C1490 0.47uF, C1408 0.47uF, C1656 0.47uF, C1549 0.47uF, C1454 0.47uF, C1469 0.47uF, C1552 0.47uF, C1533 0.47uF

C1426 0.47uF, C1588 0.47uF, C1410 0.47uF, C1499 0.47uF, C1649 0.47uF, C1655 0.47uF, C1496 0.47uF, C1554 0.47uF, C1475 0.47uF, C1474 0.47uF, C1394 0.47uF, C1676 0.47uF, C1466 0.47uF, C1460 0.47uF, C1635 0.47uF, C1498 0.47uF, C1494 0.47uF, C1570 0.47uF, C1440 0.47uF, C1413 0.47uF

C1412 0.47uF, C1476 0.47uF, C1598 0.47uF, C1603 0.47uF, C1477 0.47uF, C1585 0.47uF, C1571 0.47uF, C1671 0.47uF, C1495 0.47uF, C1573 0.47uF, C1625 0.47uF, C1409 0.47uF, C1461 0.47uF, C1396 0.47uF, C1402 0.47uF, C1441 0.47uF, C1560 0.47uF, C1580 0.47uF, C1613 0.47uF, C1605 0.47uF

C1405 0.47uF, C1658 0.47uF, C1493 0.47uF, C1578 0.47uF, C1435 0.47uF, C1522 0.47uF, C1551 0.47uF, C1444 0.47uF, C1550 0.47uF, C1471 0.47uF, C1604 0.47uF, C1492 0.47uF, C1415 0.47uF, C1546 0.47uF, C1395 0.47uF, C1673 0.47uF, C1601 0.47uF, C1637 0.47uF, C1657 0.47uF, C1584 0.47uF

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GPU Decoupling

FBVDDQ

FBVDDQ

0.47uF ---->1uF

Partition A

2 X 10UF, 6 X 0.47UF

C4254 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4260 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4266 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4272 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4278 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4284 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09

GND

Partition B

2 X 10UF, 6 X 0.47UF

C4255 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4261 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4267 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4273 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4279 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4285 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09

GND

Partition C

2 X 10UF, 6 X 0.47UF

C4256 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4262 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4268 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4274 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4280 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4286 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09

GND

Partition D

2 X 10UF, 6 X 0.47UF

C4257 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4263 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4269 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4275 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4281 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4287 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09

GND

Partition E

2 X 10UF, 6 X 0.47UF

C4258 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4264 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4270 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4276 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4282 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4288 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09

GND

Partition F

2 X 10UF, 6 X 0.47UF

C4259 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4265 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4271 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4277 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4283 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09
C4289 0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09

GND

NVVDD

NVVDD

80 X 0.47UF

C4290 C4294 C4298 C4302 C4306 C4310 C4314 C4318 C4322 C4326 C4330 C4334 C4338 C4342 C4346 C4350 C4354 C4358 C4362 C4366
C4291 C4295 C4299 C4303 C4307 C4311 C4315 C4319 C4323 C4327 C4331 C4335 C4339 C4343 C4347 C4351 C4355 C4359 C4363 C4367
C4292 C4296 C4300 C4304 C4308 C4312 C4316 C4320 C4324 C4328 C4332 C4336 C4340 C4344 C4348 C4352 C4356 C4360 C4364 C4368
C4293 C4297 C4301 C4305 C4309 C4313 C4317 C4321 C4325 C4329 C4333 C4337 C4341 C4345 C4349 C4353 C4357 C4361 C4365 C4369

0.47uF 4V 30% X6S 0201W COMMON C11-105731J-M09

GND

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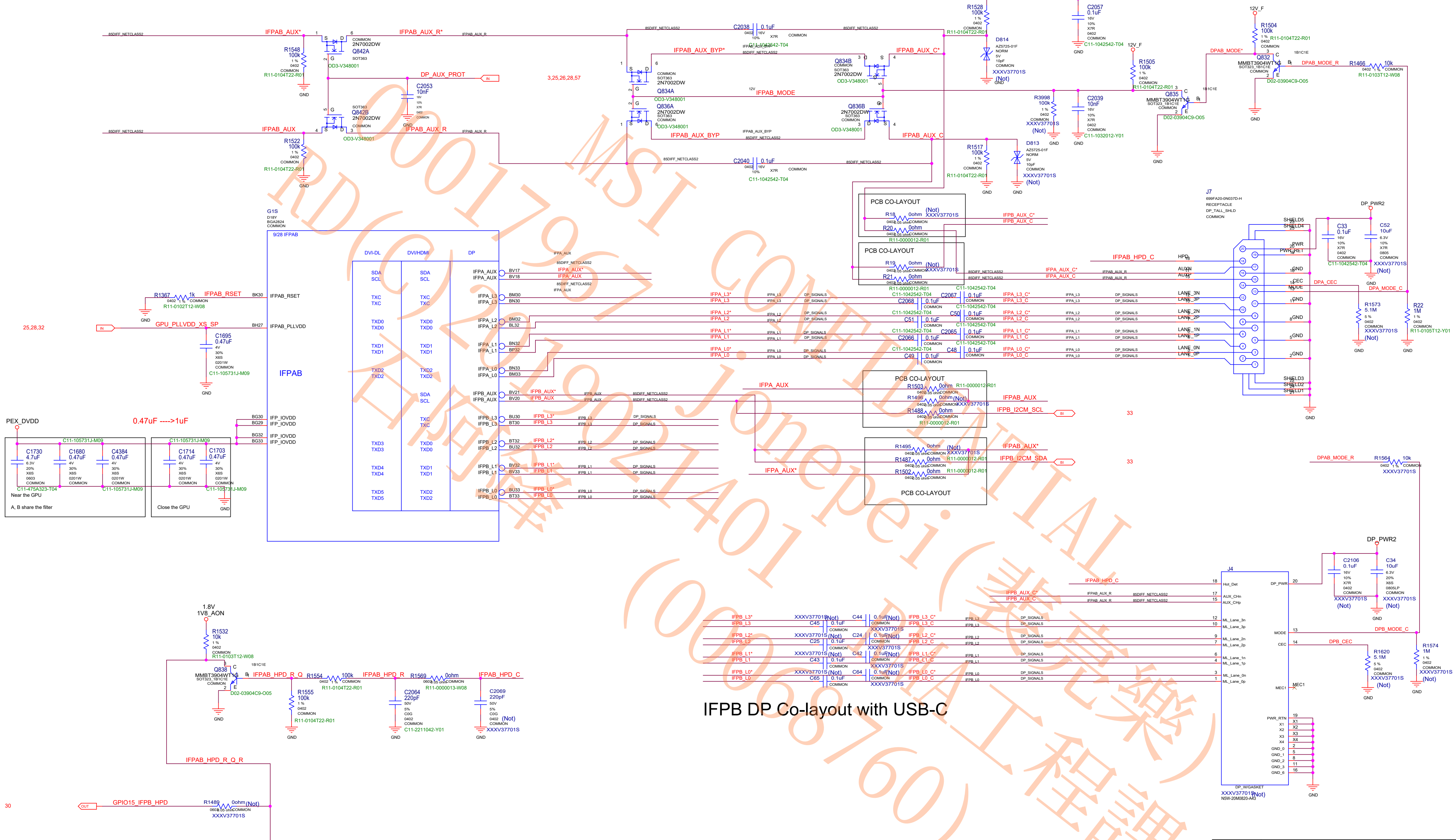
IFPAB TALL-DP



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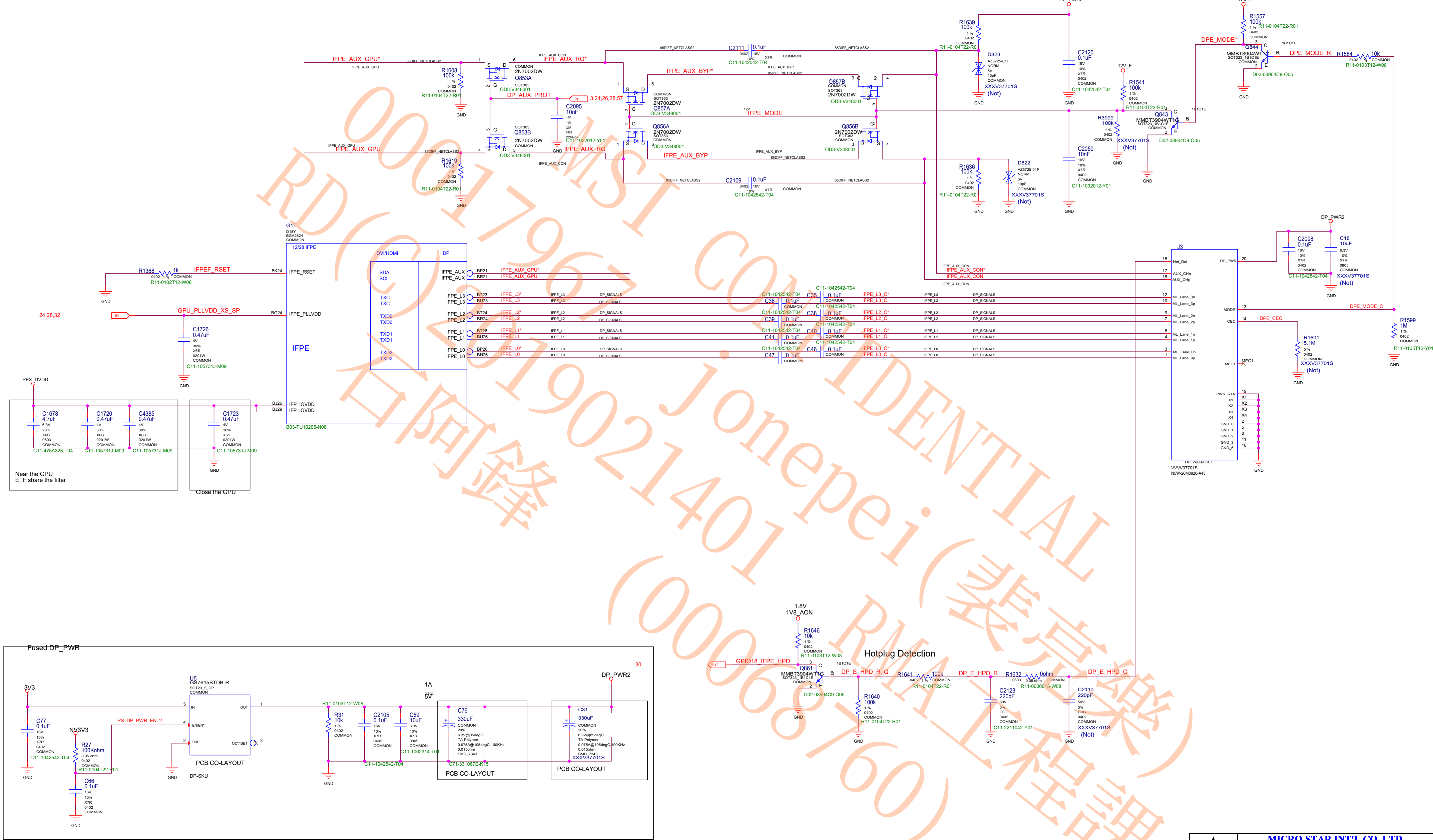
IFPE DP



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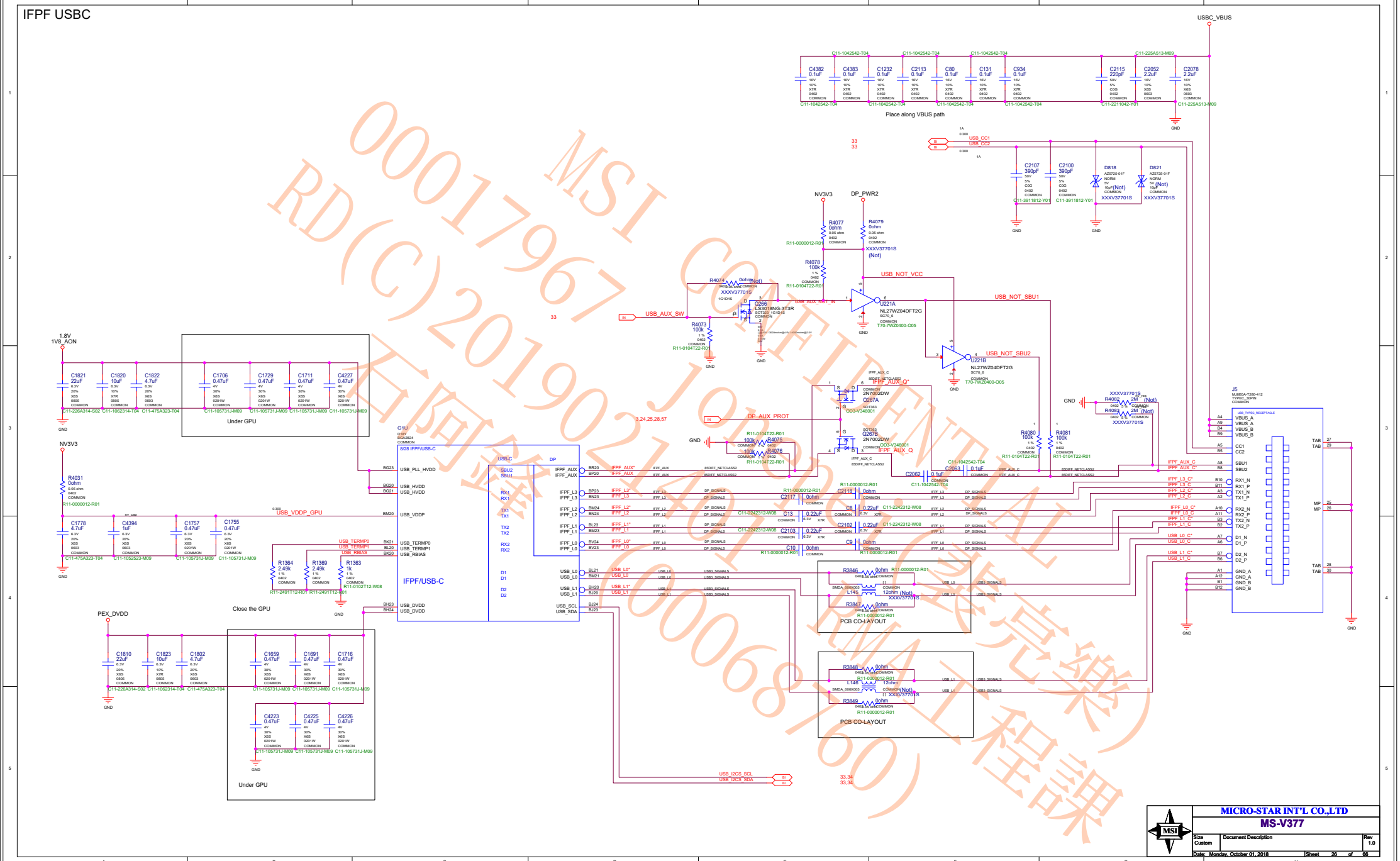
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USBC_VBUS
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NV3V3
DP_PWR2
USB_NOT_VCC
USB_NOT_SBU1
USB_NOT_SBU2
USB_AUX_SW
DP_AUX_PROT
IFPF_AUX_Q
IFPF_AUX_Q*
1.8V
1V8_AON
Under GPU
Close the GPU
PEX_DVDD
USB_VDDP_GPU
IFPF/USB-C
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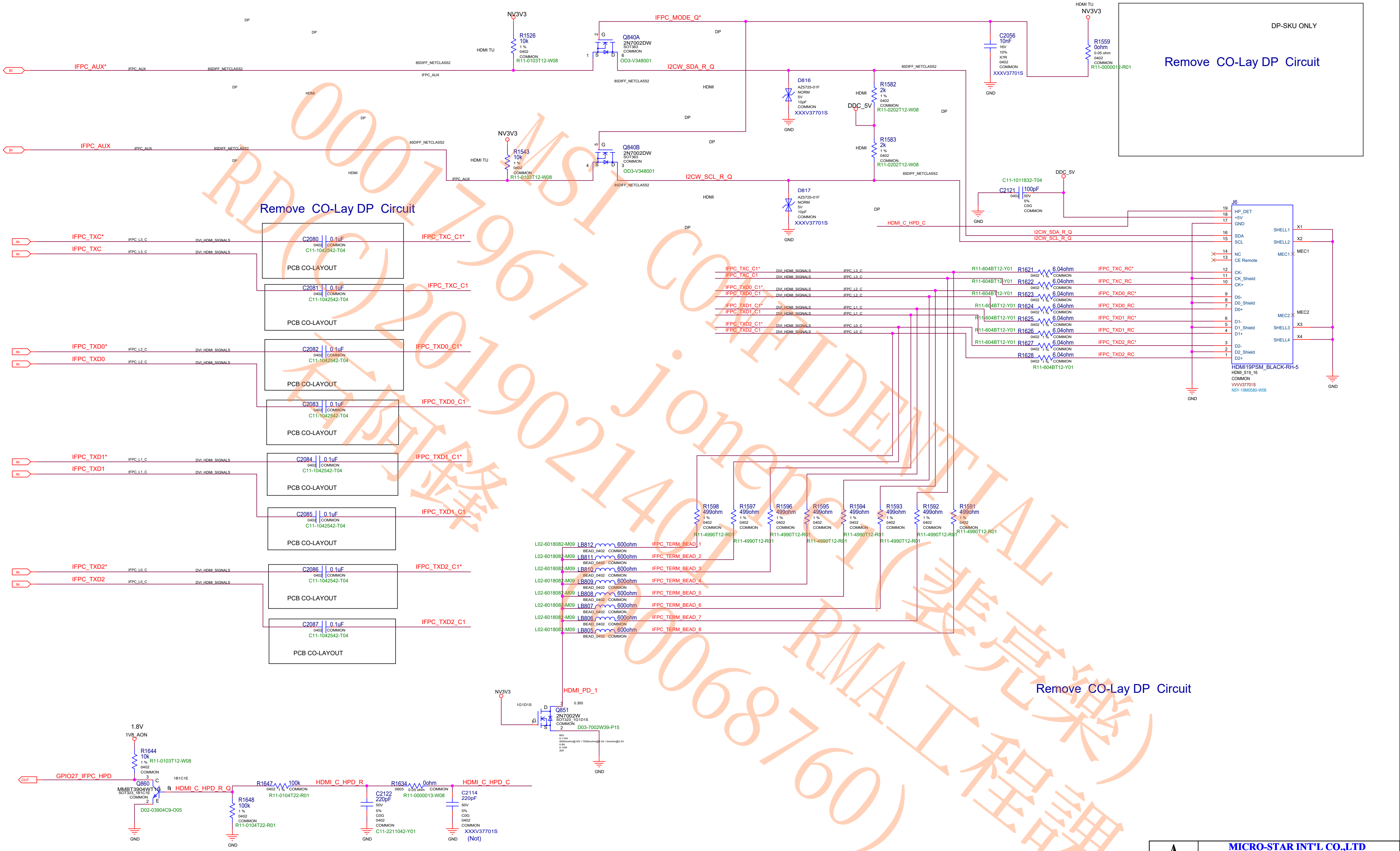
IFPC HDMI 2.0/DP



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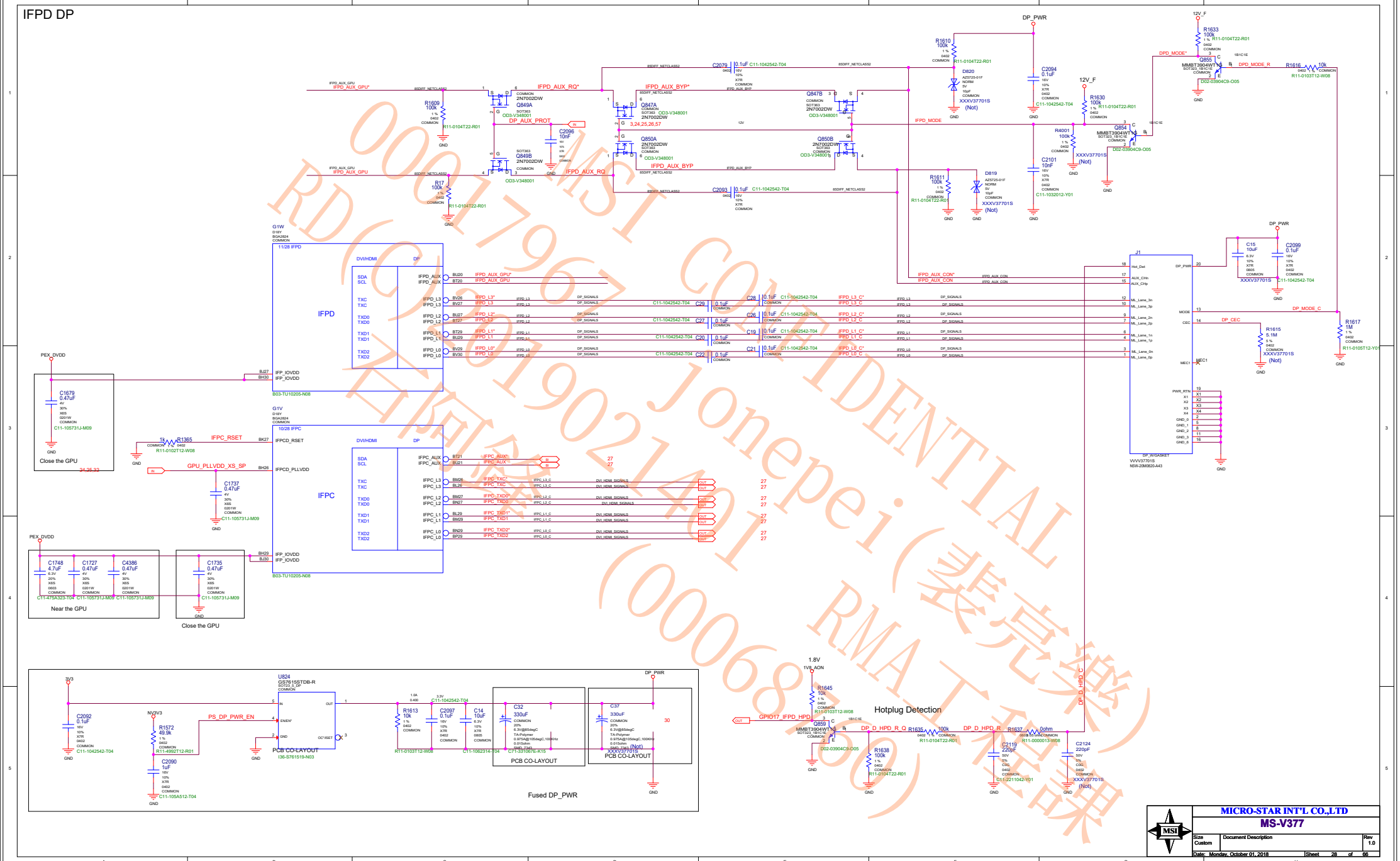
IFPD DP
IFPD_AUX_RQ*
IFPD_AUX_BYP*
DP_AUX_PROT
IFPD_AUX_BYP
IFPD_AUX_RQ
IFPD_MODE
IFPD_AUX_CON*
IFPD_AUX_CON
IFPD
IFPC
DP_PWR
12V_F
DPD_MODE*
DPD_MODE_R
DP_MODE_C
DP_CEC
Hotplug Detection
GPIO17_IFPD_HPD
DP_D_HPD_R_Q
DP_D_HPD_R
DP_D_HPD_C
PEX_DVDD
Close the GPU
Near the GPU
Close the GPU
PS_DP_PWR_EN
PCB CO-LAYOUT
Fused DP_PWR
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NVHS Interface and FRAME LOCK

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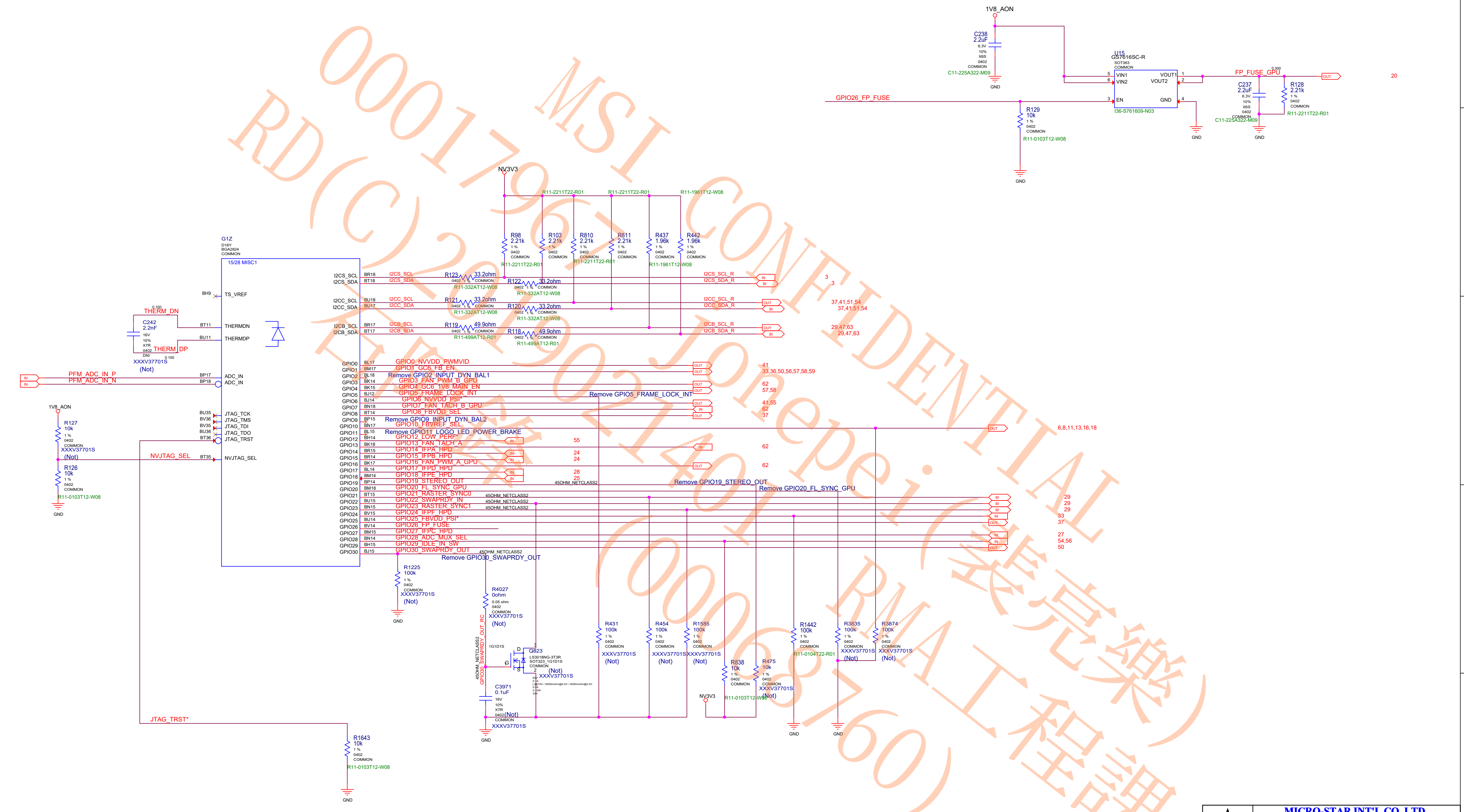
MISC1: Fan, Thermal, JTAG, GPIO, STEREO



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MISC2: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	
L	L	H	00001	DEFAULT
L	H	L	00010	
L	H	H	00011	
H	L	L	00100	
H	L	H	00101	
H	H	L	00110	
H	H	H	00111	
L	L	M	01000	
L	M	L	01001	

ROM_SO	ROM_SI	ROM_SCLK	DUMMY[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
L	L	L	XXX1	FS_OVERT ENABLE	DEFAULT
L	L	H	XXX0	FS_OVERT DISABLE	

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
L	H	L	0	0	1	0	
L	L	H	0	0	0	1	Default
L	L	L	0	0	0	0	SKU 200

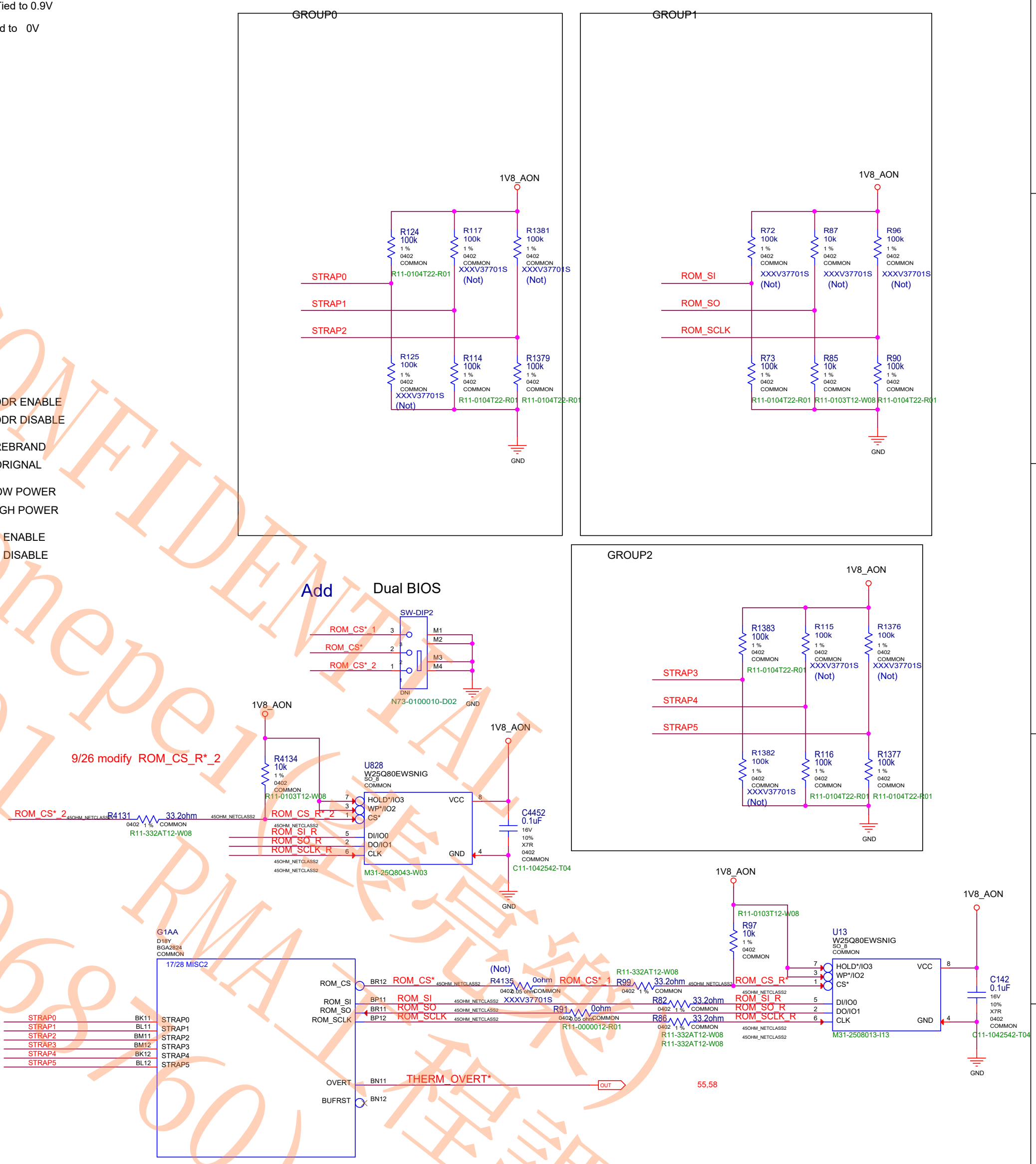
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



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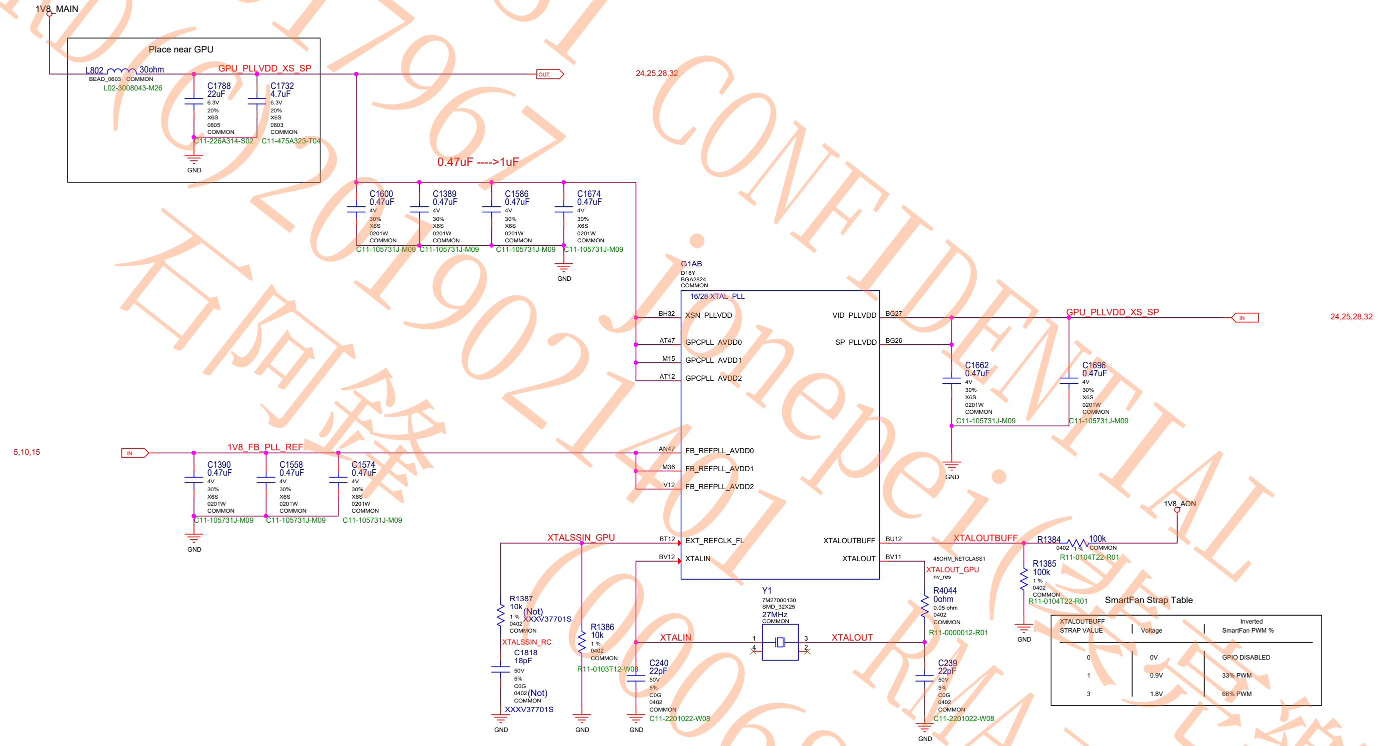
MISC2: XTAL. PLL



SmartFan Strap Table

XTALOUTBUFF STRAP VALUE	Voltage	Inverted SmartFan PWM %
0	0V	GPIO DISABLED
1	0.9V	33% PWM
3	1.8V	66% PWM

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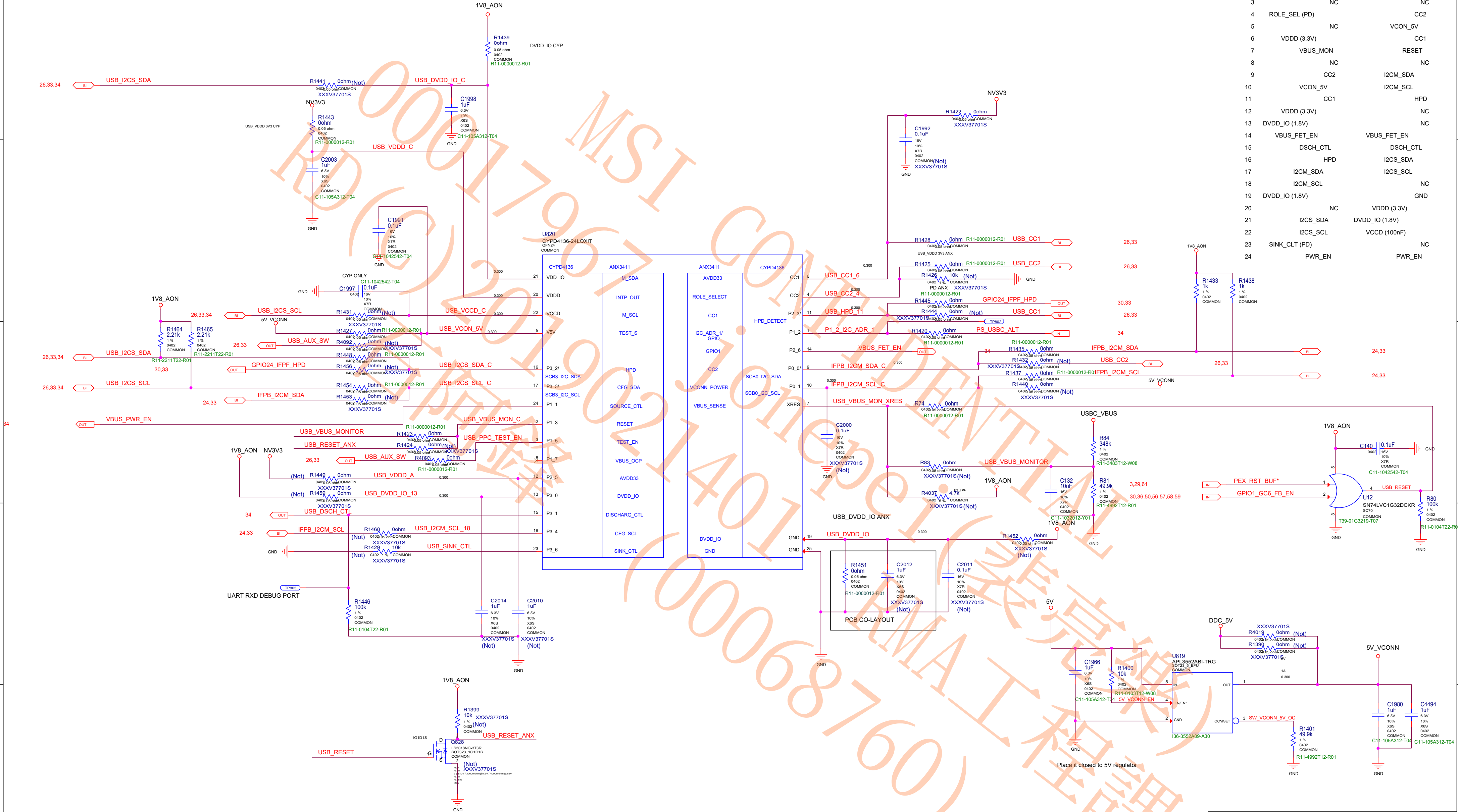
MISC: USB PPC



PIN	ANX	CYP
1	TP	TP
2	RESET	VBUS_MON
3	NC	NC
4	ROLE_SEL (PD)	CC2
5	NC	VCON_5V
6	VDDD (3.3V)	CC1
7	VBUS_MON	RESET
8	NC	NC
9	CC2	I2CM_SDA
10	VCON_5V	I2CM_SCL
11	CC1	HPD
12	VDDD (3.3V)	NC
13	DVDD_IO (1.8V)	NC
14	VBUS_FET_EN	VBUS_FET_EN
15	DSCH_CTL	DSCH_CTL
16	HPD	I2CS_SDA
17	I2CM_SDA	I2CS_SCL
18	I2CM_SCL	NC
19	DVDD_IO (1.8V)	GND
20	NC	VDDD (3.3V)
21	I2CS_SDA	DVDD_IO (1.8V)
22	I2CS_SCL	VCCD (100nF)
23	SINK_CLT (PD)	NC
24	PWR_EN	PWR_EN

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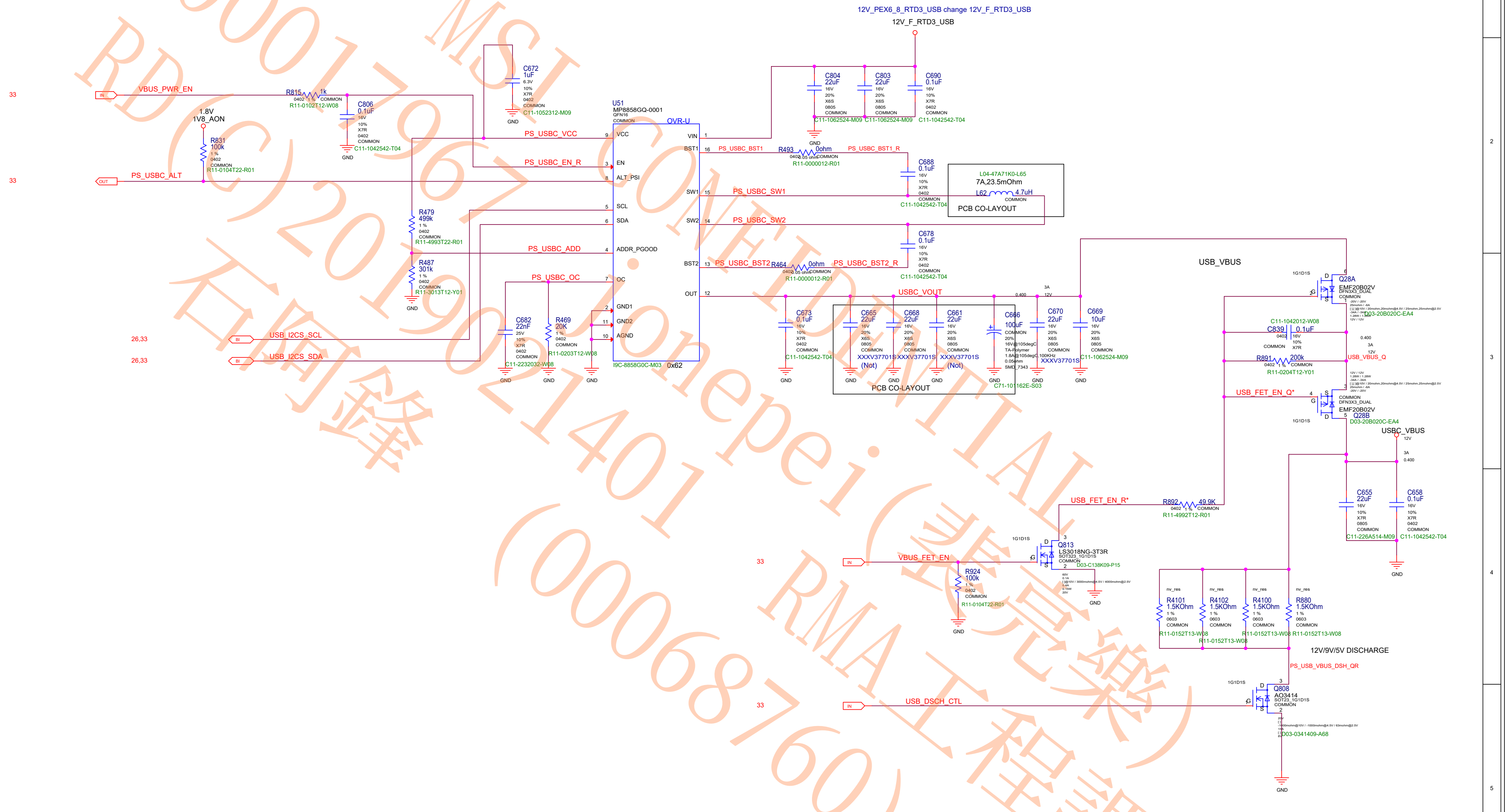
PS: USB VR



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Custom	GPU Decoupling	1.0

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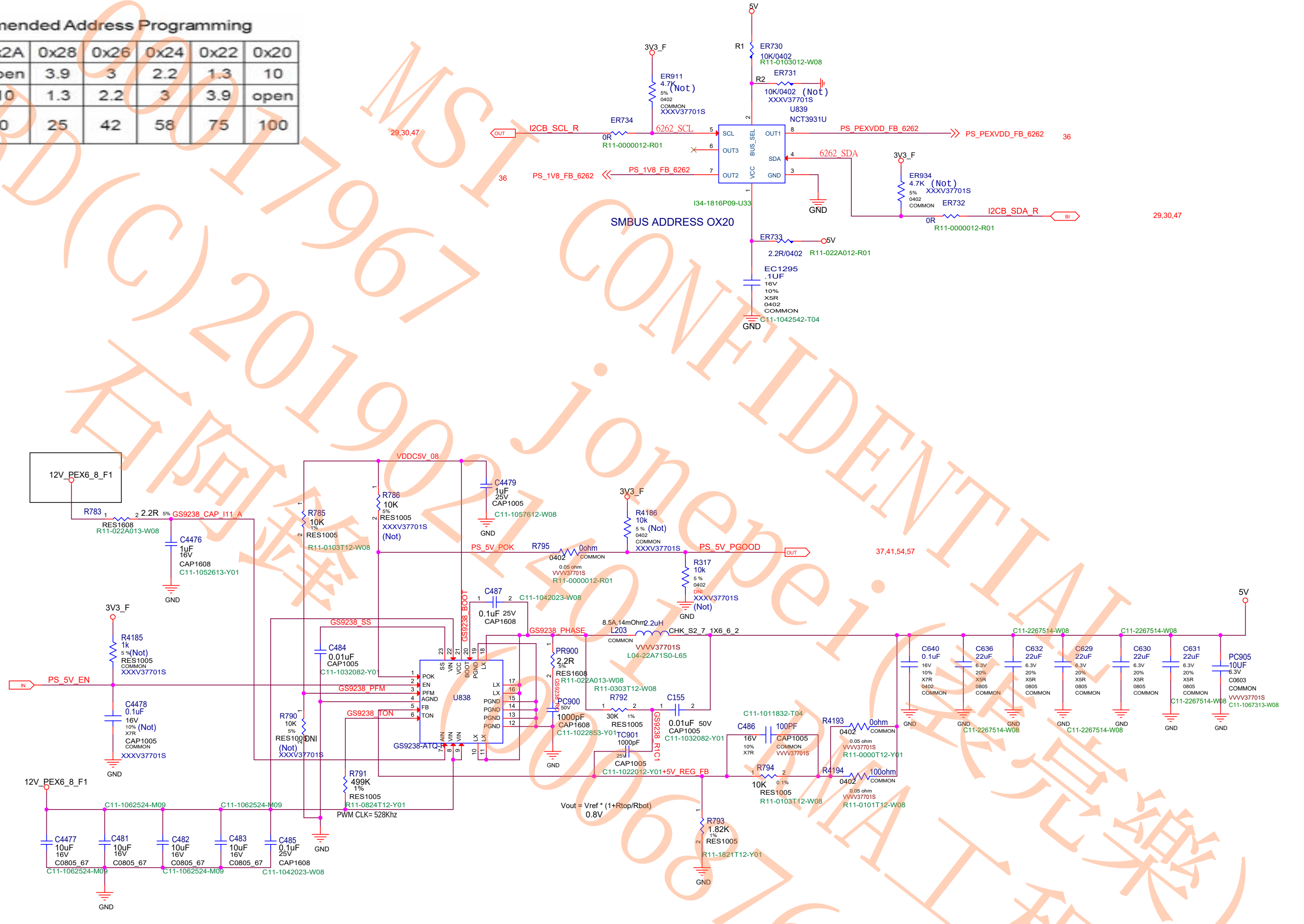
PS: 5V, 5V_BACKUP

Table 1. Recommended Address Programming

Address	0x2A	0x28	0x26	0x24	0x22	0x20
R1 (kΩ)	open	3.9	3	2.2	1.3	10
R2 (kΩ)	10	1.3	2.2	3	3.9	open
BUS_SEL Voltage (% of VCC)	0	25	42	58	75	100



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Custom	GPU Decoupling	1.0

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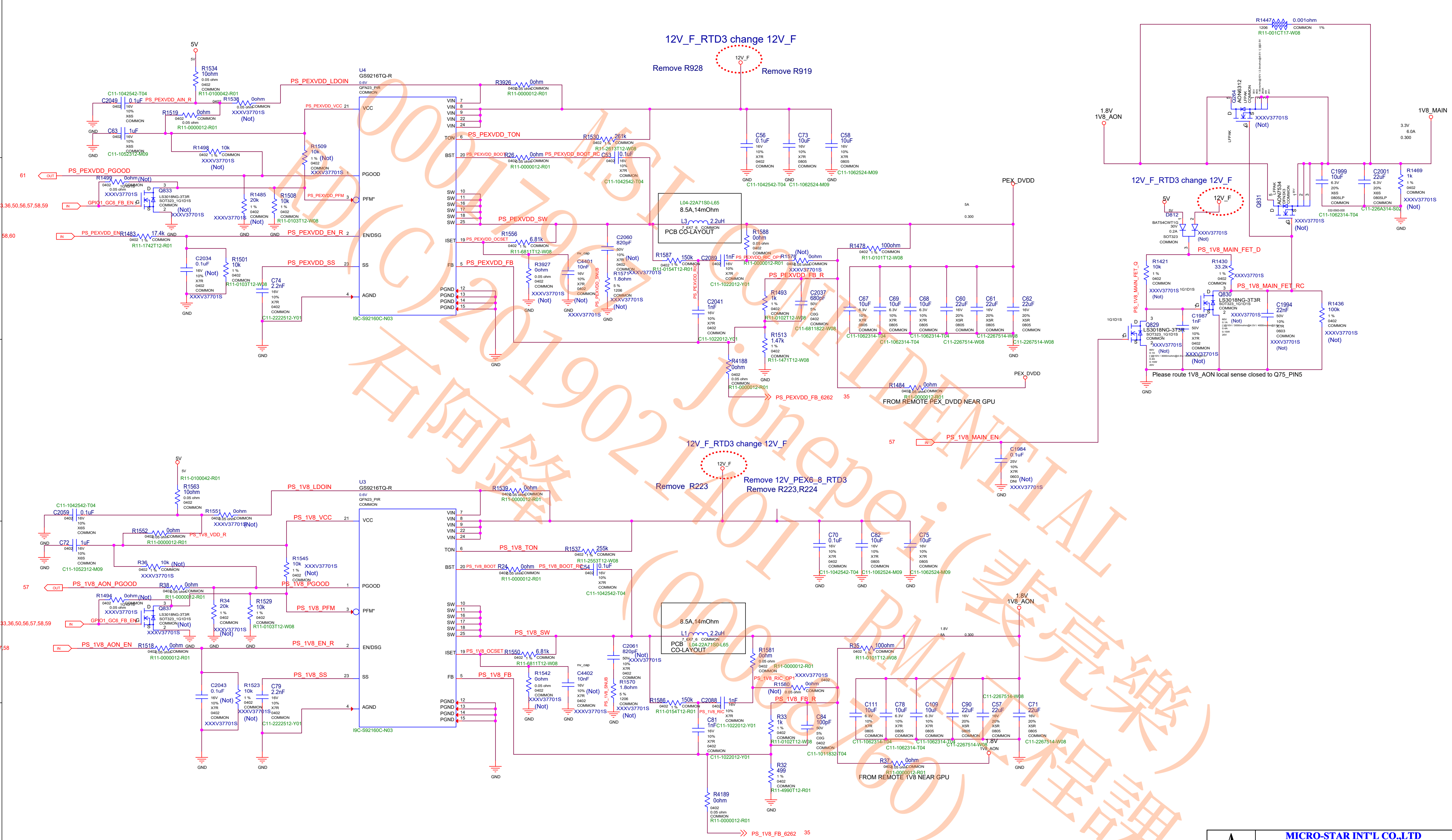
PS: PEXVDD 1V8 Rail



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Size	Document Description	Rev
Custom	PS: PEXVDD 1V8 Rail	1.0

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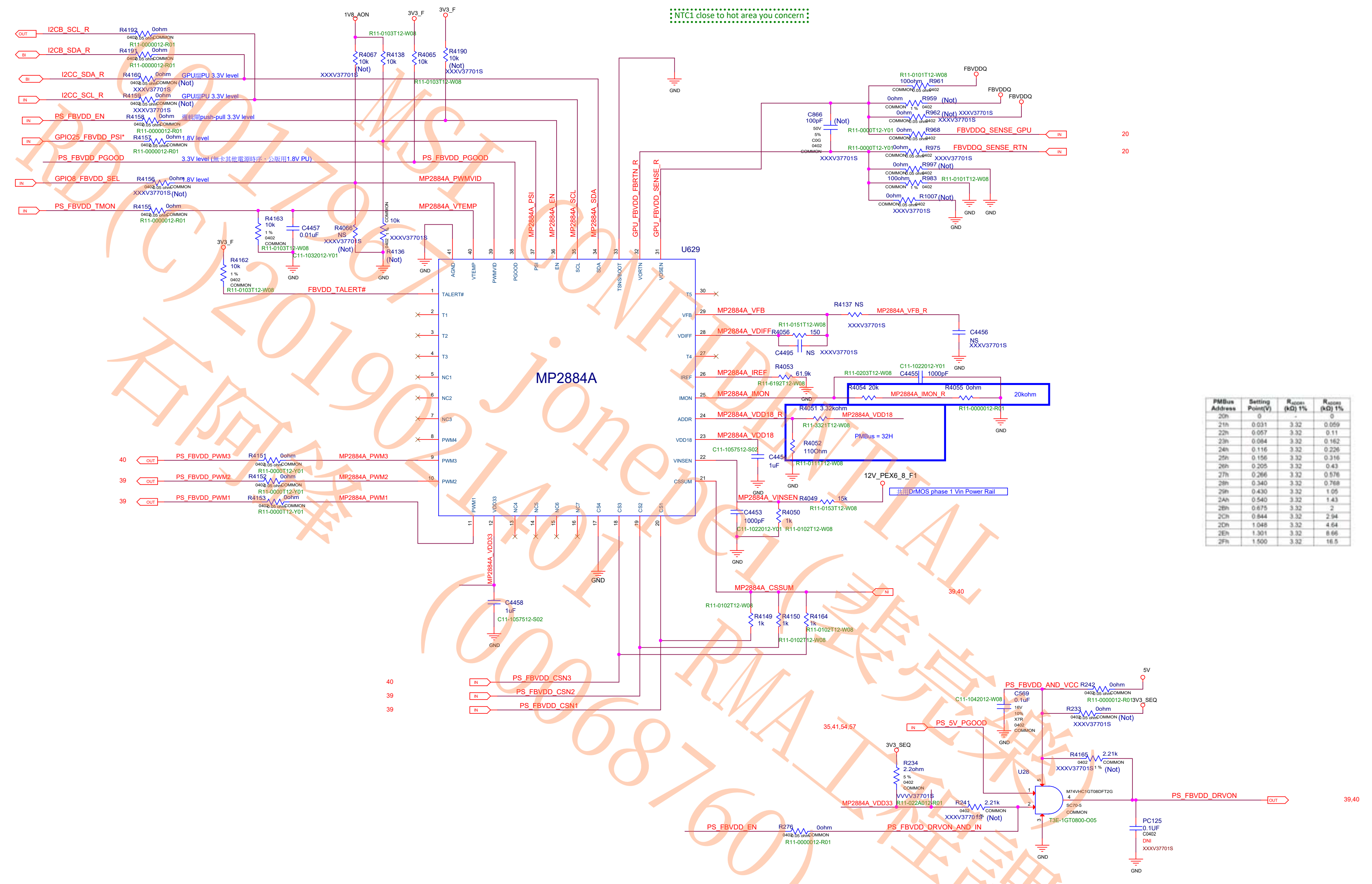
PS: FBVDD Controller

EN Type	R3
Open Drain	10k
Push Pull	NS

PSI	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count

PWMVID	Vout
High	VID in 24h
Hi-Z	VID in 21h
Low	VID in 1Fh

	+NVVDD
TDC	??A
IccMax	??A
Vboot	1.35V
Load Line	0mohm



PMBus Address	Setting Point(V)	R_{ADDR1} (kΩ) 1%	R_{ADDR2} (kΩ) 1%
20h	0	-	0
21h	0.031	3.32	0.059
22h	0.057	3.32	0.11
23h	0.084	3.32	0.162
24h	0.116	3.32	0.226
25h	0.156	3.32	0.316
26h	0.205	3.32	0.43
27h	0.266	3.32	0.576
28h	0.340	3.32	0.768
29h	0.430	3.32	1.05
2Ah	0.540	3.32	1.43
2Bh	0.675	3.32	2
2Ch	0.844	3.32	2.94
2Dh	1.048	3.32	4.64
2Eh	1.301	3.32	8.66
2Fh	1.500	3.32	16.5

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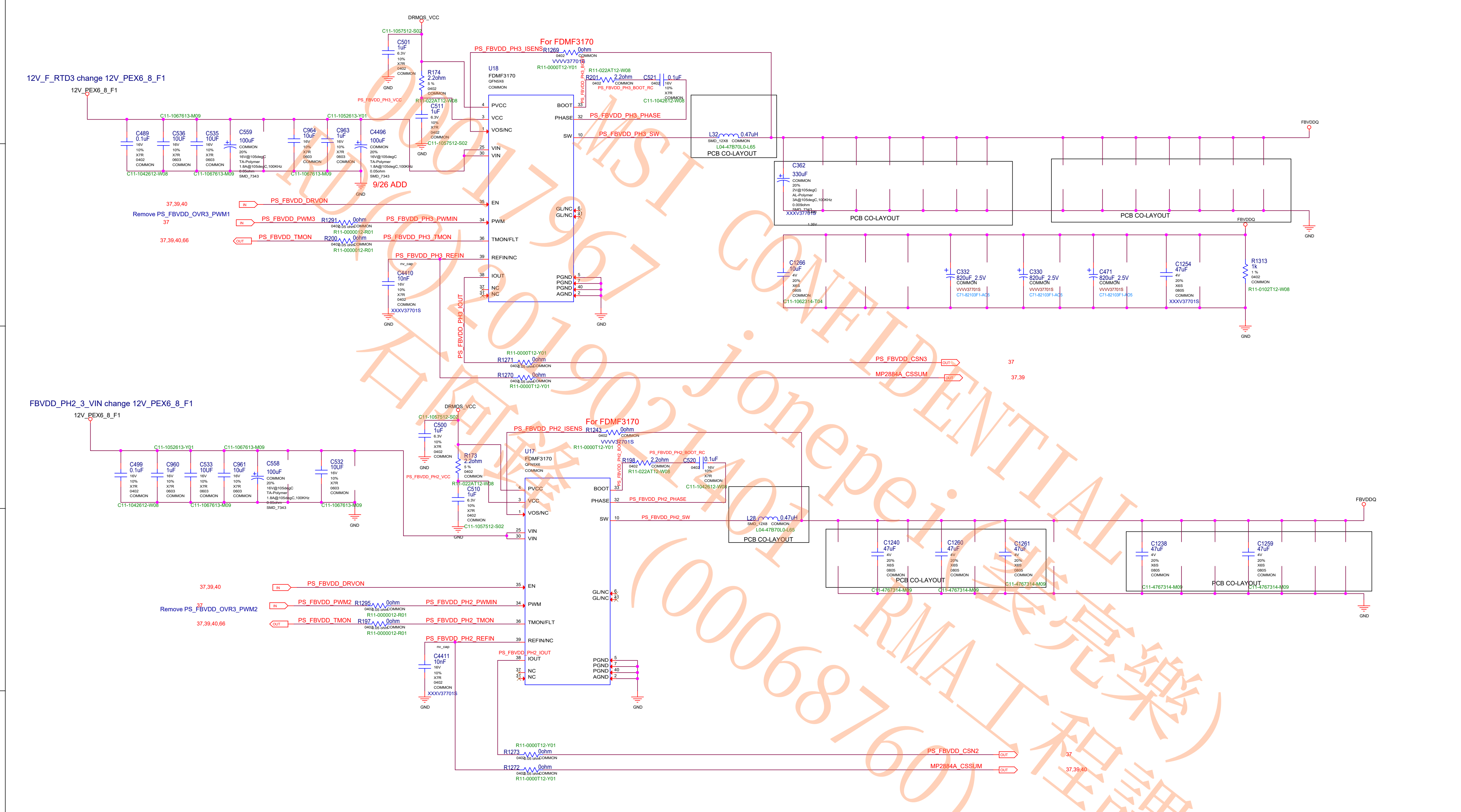
PS: FBVDD Controller OVR3

PS: FBVDD PH2,3



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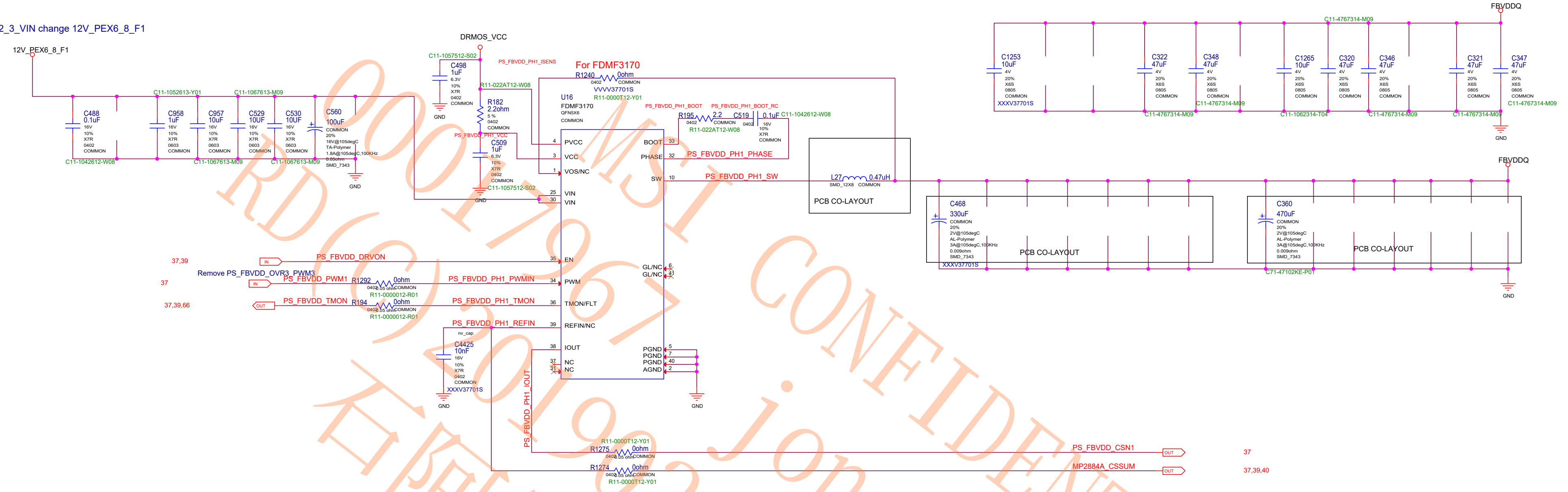
PS: FBVDD PH1

FBVDD_PH2_3_VIN change 12V_PEX6_8_F1



Remove 12V_PEX_FB --->FBVDD_PH2_3_VIN circuit

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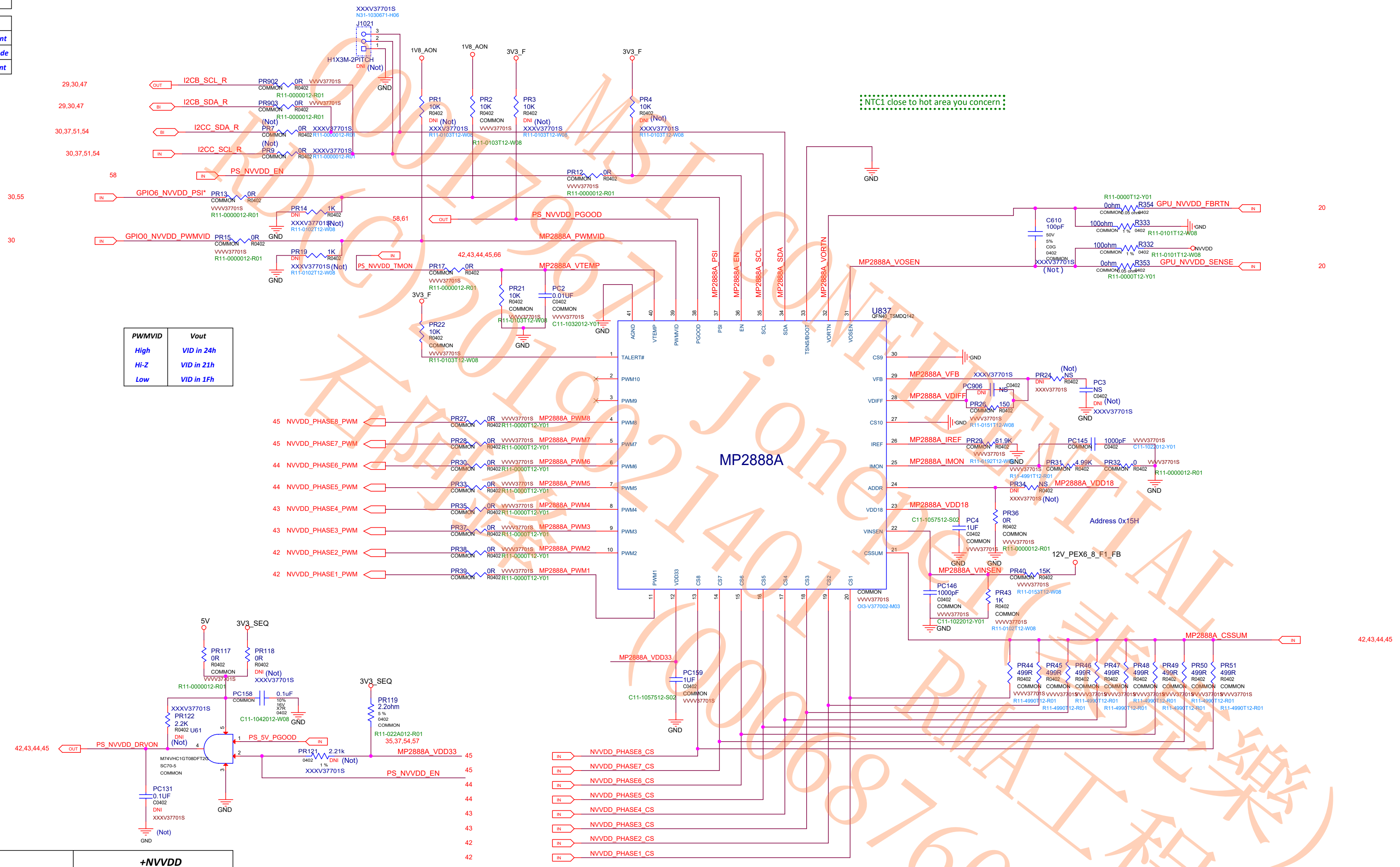
Page34: PS: NVVDD - MP2888A

EN Type	R3
Open Drain	10k
Push Pull	NS

PSI	Mode
High	High Phase Count
Hi-Z	Auto Power Mode
Low	Low Phase Count

PWMVID	Vout
High	VID in 24h
Hi-Z	VID in 21h
Low	VID in 1Fh



	+NVVDD
TDC	200A
IccMax	330A
Vboot	0.8V
Load Line	0mohm

PMBus Address	Setting Point(V)	R_{ADDR1} (kΩ) 1%	R_{ADDR2} (kΩ) 1%
20h	0	-	0
21h	0.031	3.32	0.059
22h	0.057	3.32	0.11
23h	0.084	3.32	0.162
24h	0.116	3.32	0.226
25h	0.156	3.32	0.316
26h	0.205	3.32	0.43
27h	0.266	3.32	0.576
28h	0.340	3.32	0.768
29h	0.430	3.32	1.05
2Ah	0.540	3.32	1.43
2Bh	0.675	3.32	2
2Ch	0.844	3.32	2.94
2Dh	1.048	3.32	4.64
2Eh	1.301	3.32	8.66
2Fh	1.500	3.32	16.5

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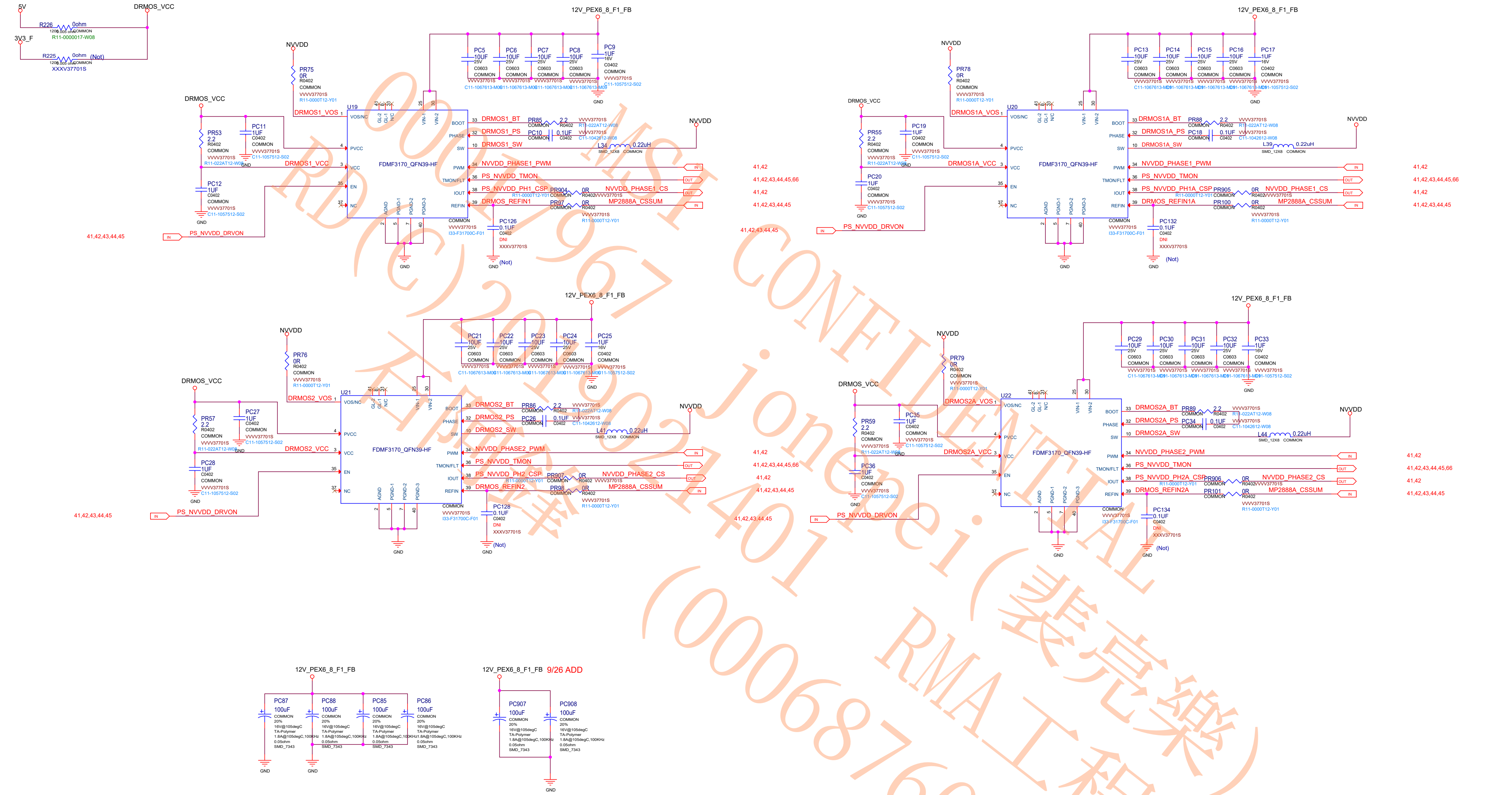
PS: NVVDD Phase 1~4



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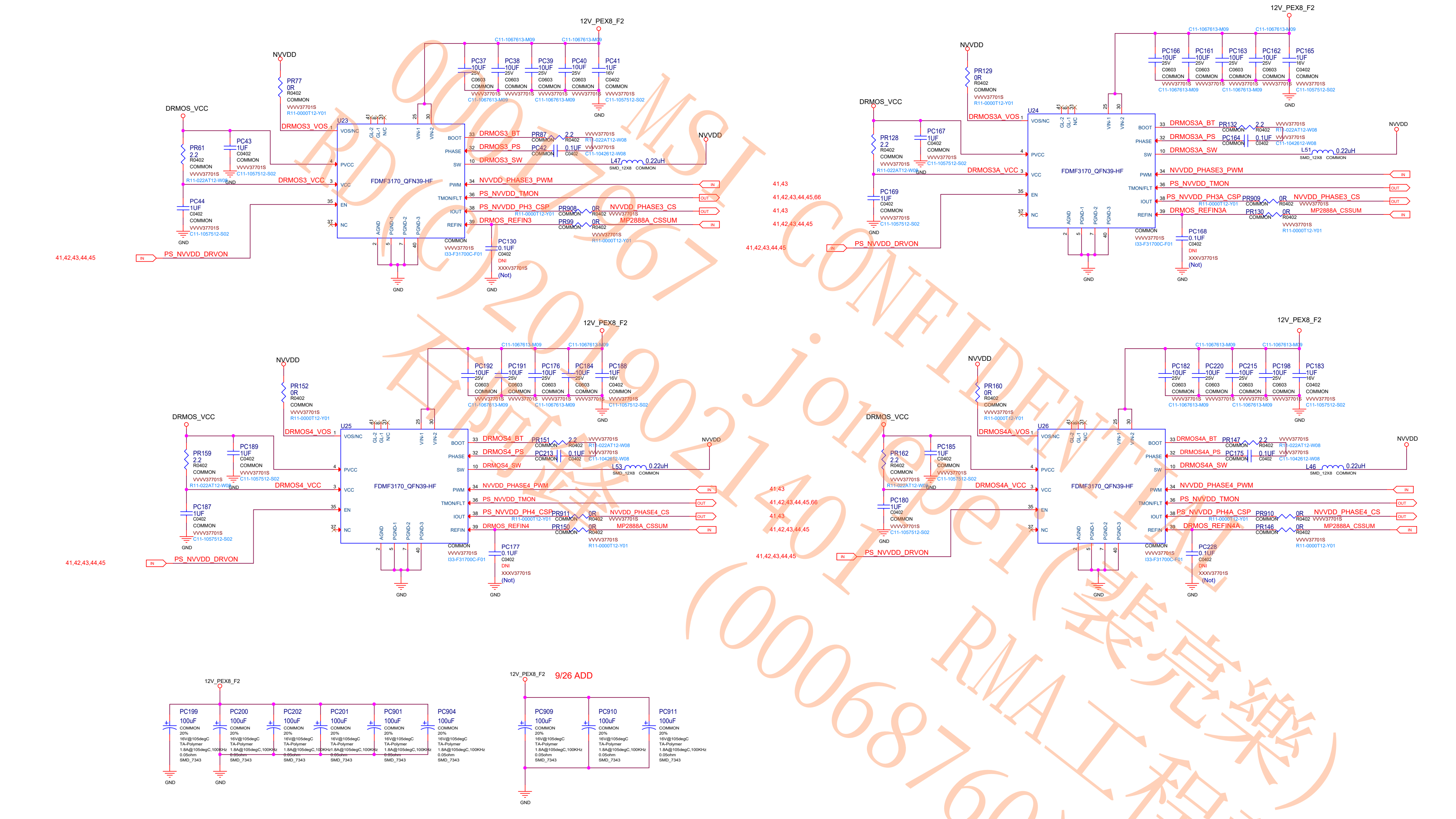
PS: NVVDD Phase 5~8



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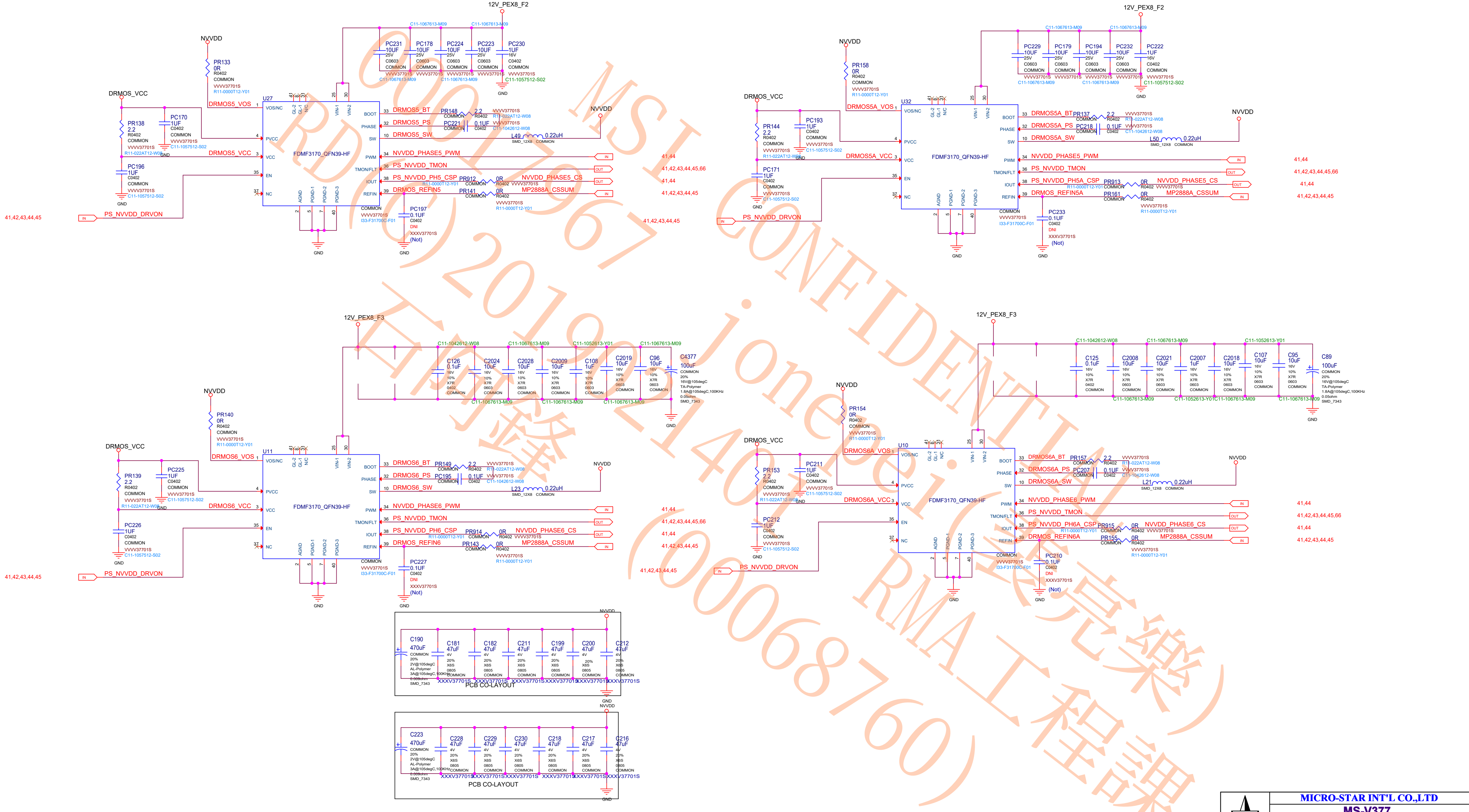
PS: NVVDD Phase 9~12



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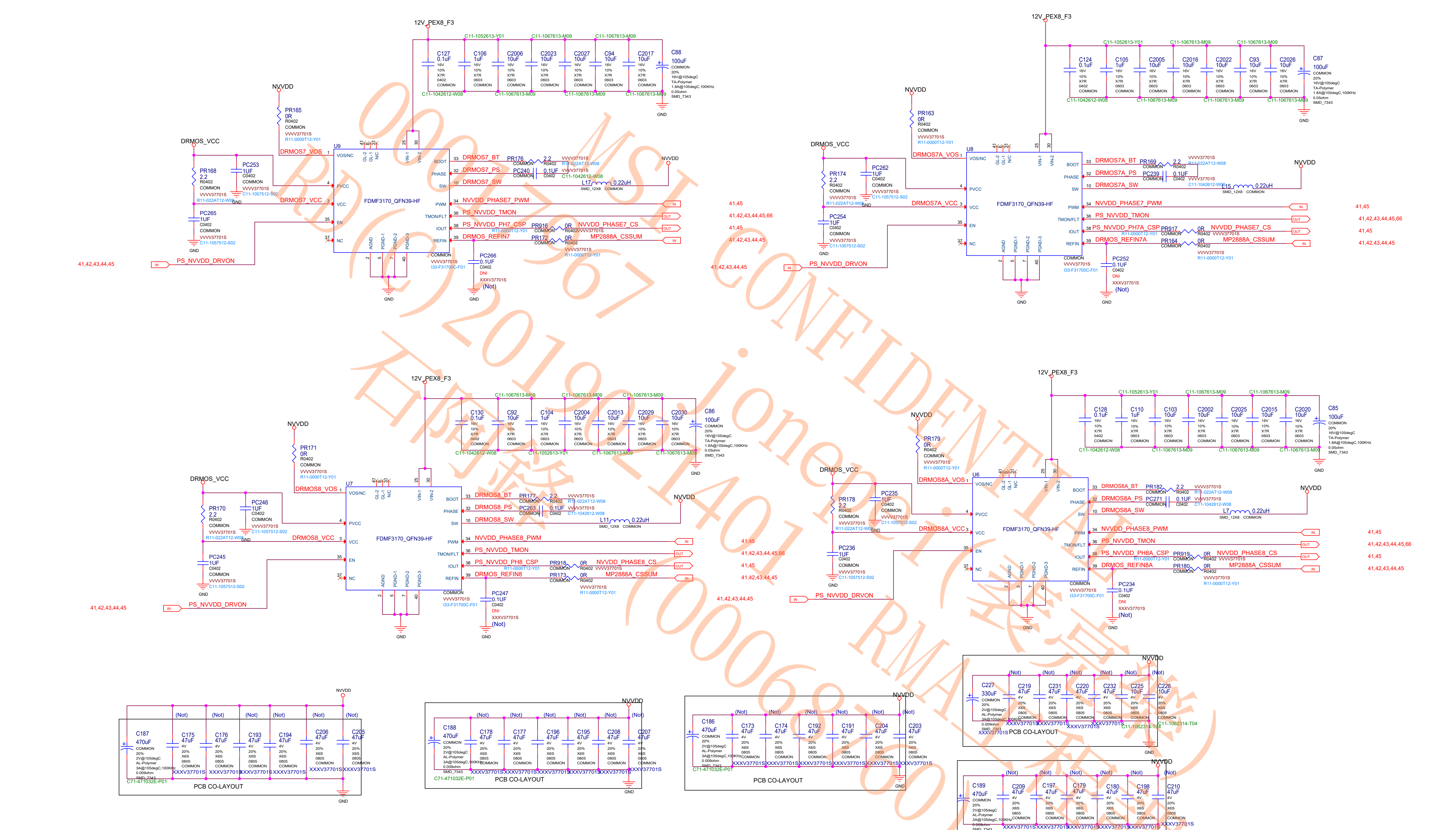
PS: NVVDD Phase 13~16



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PS:NVVDD Phase 7, 8

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Custom	PS: NVVDD - MP2888A	1.0

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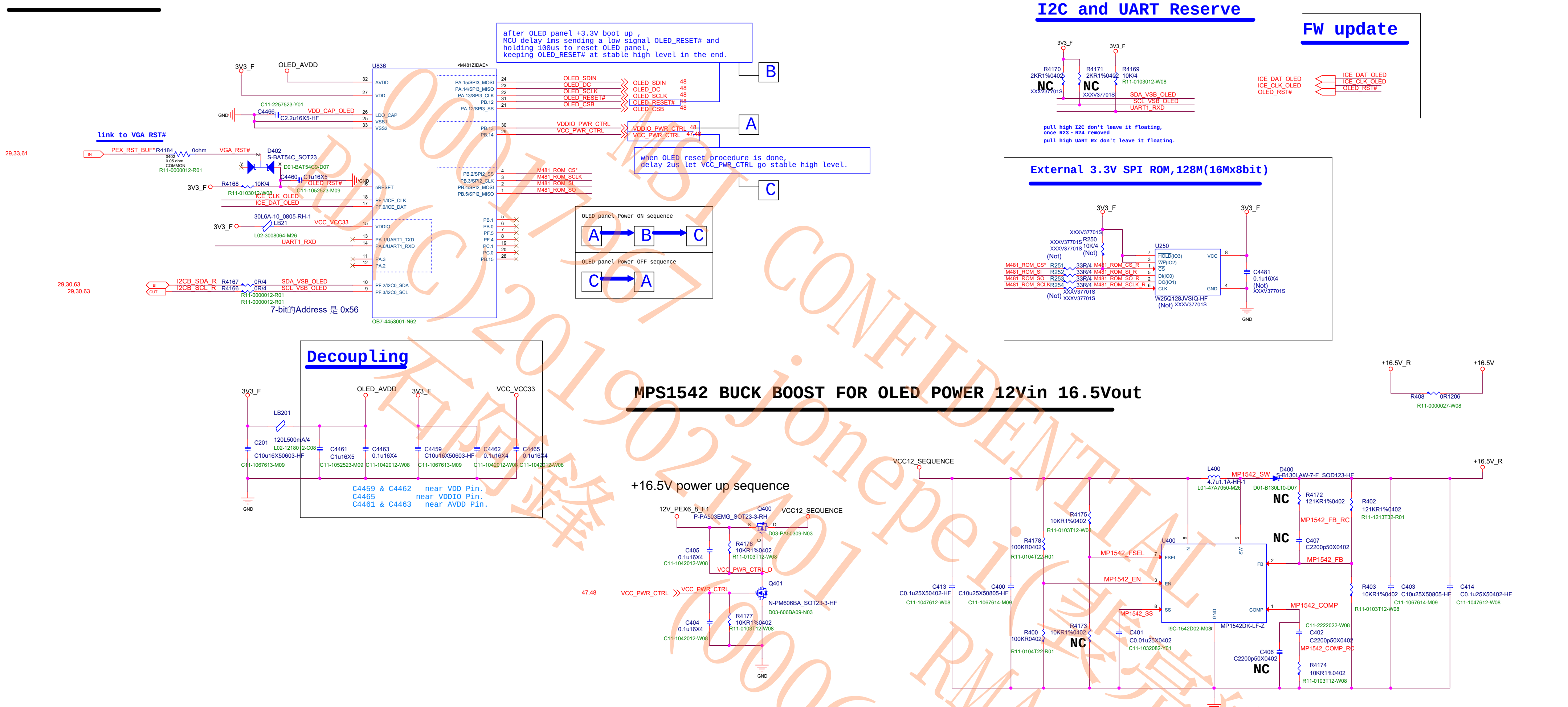
PS: NVVDD PH 9,10

32 PIN OLED MCU



PIN FUNCTIONS

Pin #	Name	Description
1	COMP	Compensation Pin. Connect a capacitor and resistor in series to ground for loop stability.
2	FB	Feedback Input. Reference voltage is 1.25V. Connect a resistor divider to this pin.
3	EN	Regulator On/Off Control Input. A high input at EN turns on the converter, and a low input turns it off. When not used, connect EN to the input source (through a 100kΩ pull-up resistor if V_{IN} > 6V) for automatic startup. EN cannot be left floating.
[illegible]	[illegible]	[illegible]

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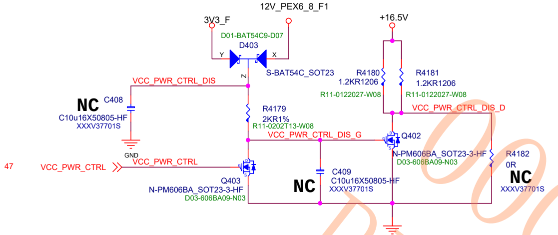
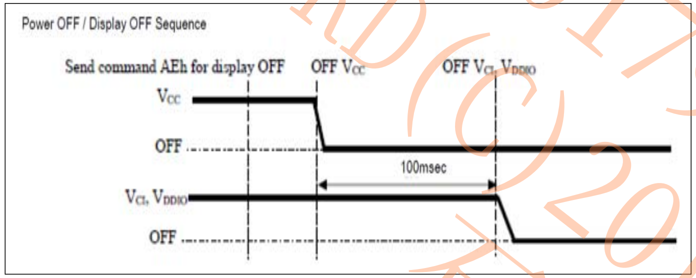
+16.5V Discharge



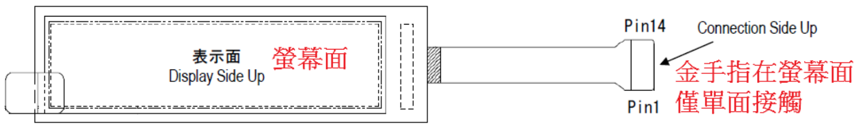
100mS time interval is counting from 2 voltages rating 10% to 10% or lower level.



12-2) 入力端子名称　Pin Assignment

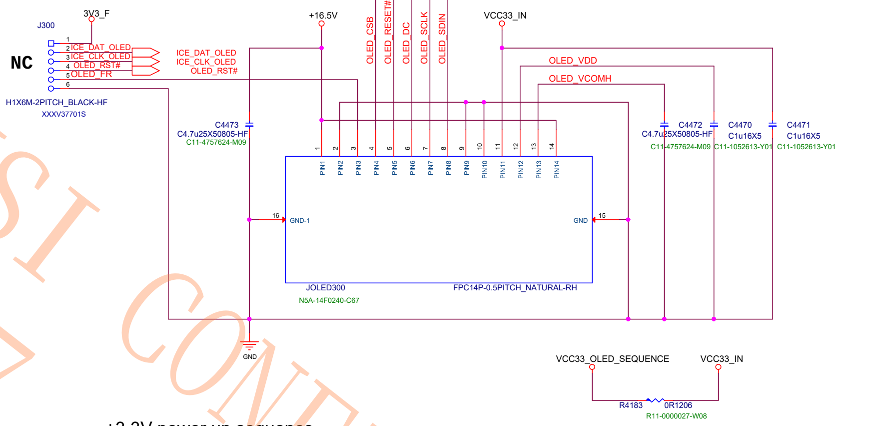
I:Input, O:Output, P:Power

PIN No	名称 Pin Name	機能	Function Description	I/O
1	VCC	OLED駆動電源	OLED Driving Voltage	P
2	AGND	グランド	Analog Ground	P
3	FR	同期信号	Synchronization Signal	O
4	CSB	チップセレクト	Chip Select	I
5	RSTB	リセット	Reset	I
6	DC	データ/コマンド選択	Data/Command Selection	I
7	SCLK	シリアルクロック	Serial Clock	I
8	SDIN	データ	Data Input	I
9	GND	グランド	Ground Pin	P
10	AGND	グランド	Analog Ground	P
11	VCI	ロジック電源	Logic Power Voltage	P
12	VDD	コア電源	Core Voltage	P
13	VCOMH	COMH 電源	COMH Voltage	P
14	VCC	OLED駆動電源	OLED Driving Voltage	P

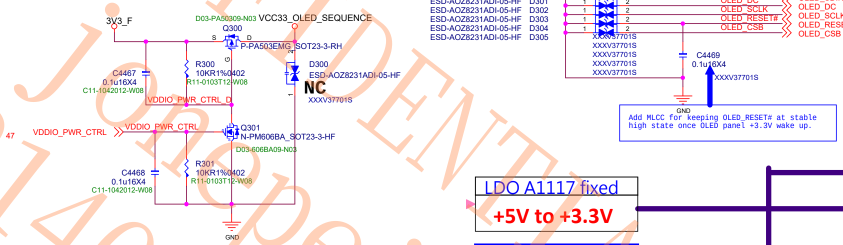


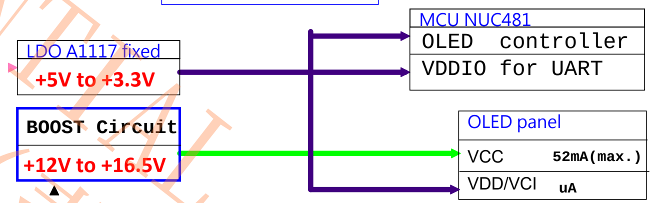
形名 Type No.　ELW2106AA

OLED housing

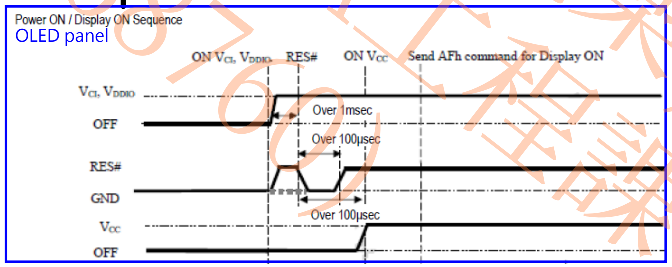


+3.3V power up sequence





1. after OLED panel +3.3V boot up , delay 1ms sending a low signal OLED_RESET# and holding 100us to reset OLED panel, keeping OLED_RESET# at stable high level in the end.
2. when OLED reset procedure is done, delay 2us let VCC_PWR_CTRL go stable high level.



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PS: NVVDD PH 13,14

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PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A

Remove 12V_F_RTD3 circuit

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	3V3
0	1	0	3V3
1	0	0	3V3
1	1	1	3V3A

Remove 3V3_RTD3 circuit

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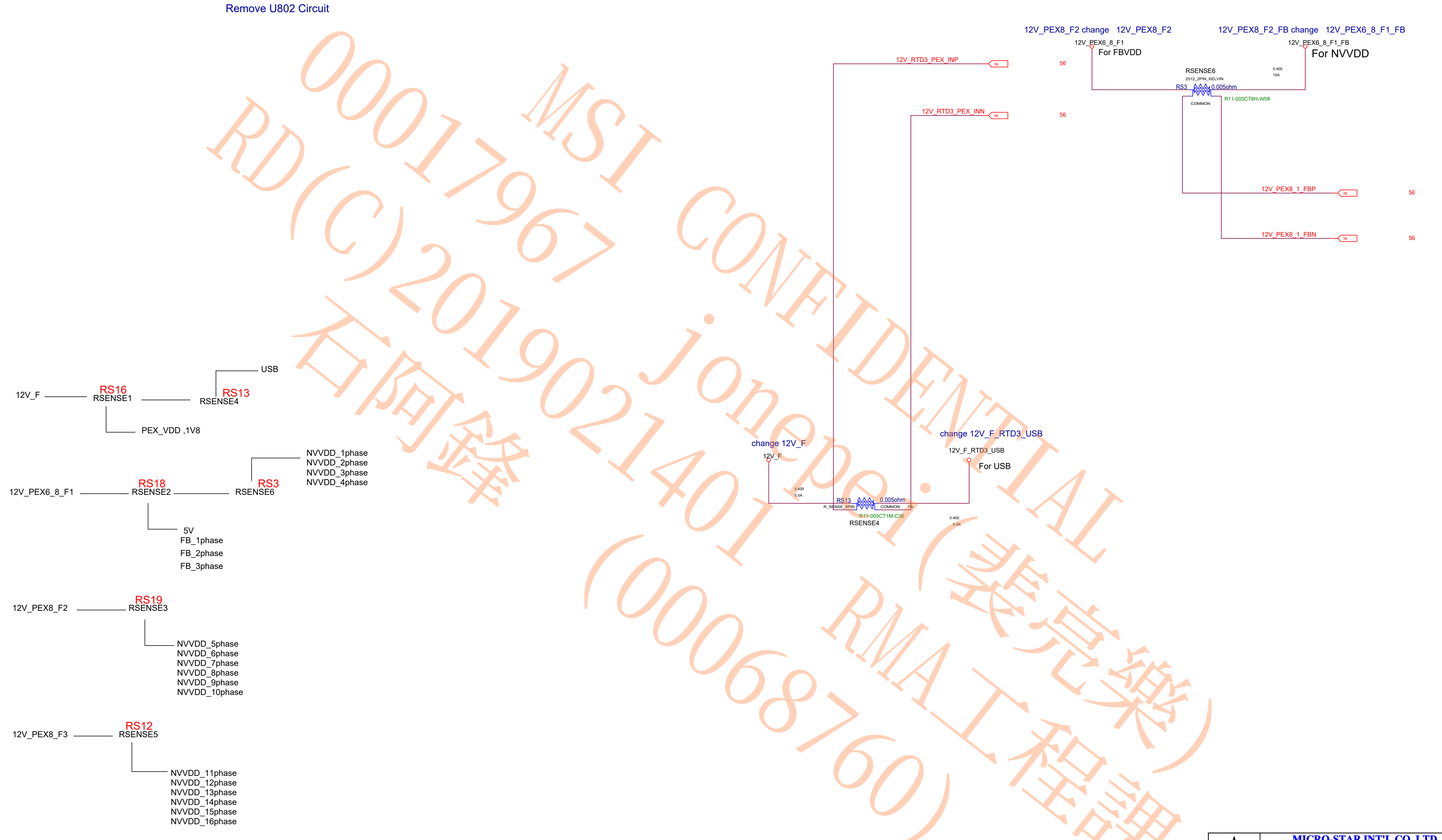

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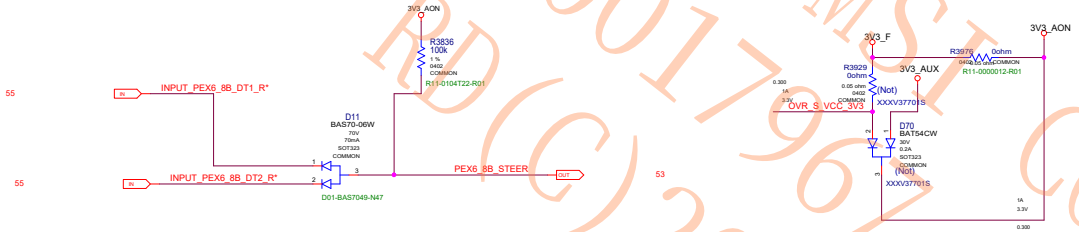
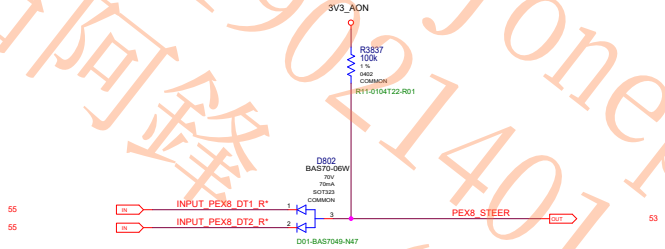
PS: Input Switch Rail Balance





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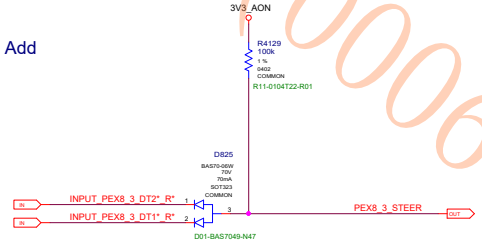

Remove NVVDD VIN change circuit

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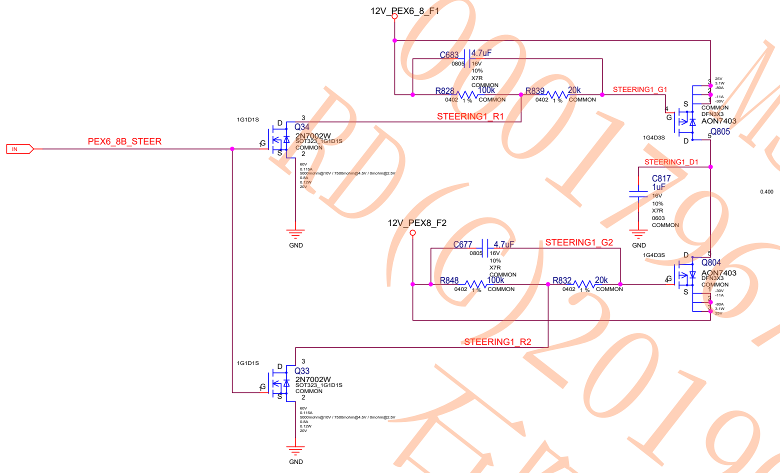
12V CURRENT STEERING (UNDER POWER BOOT):

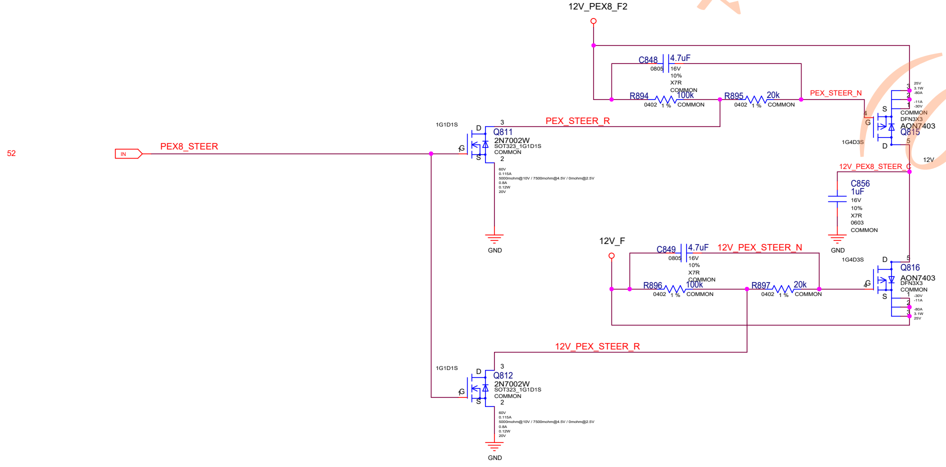
GUIDES CURRENT FROM PEX EDGE TO PEX 6/8 PIN INPUT AREA



12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



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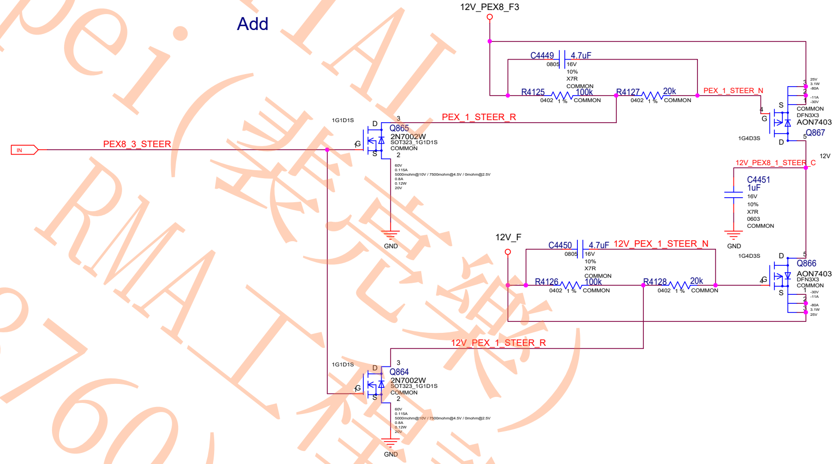

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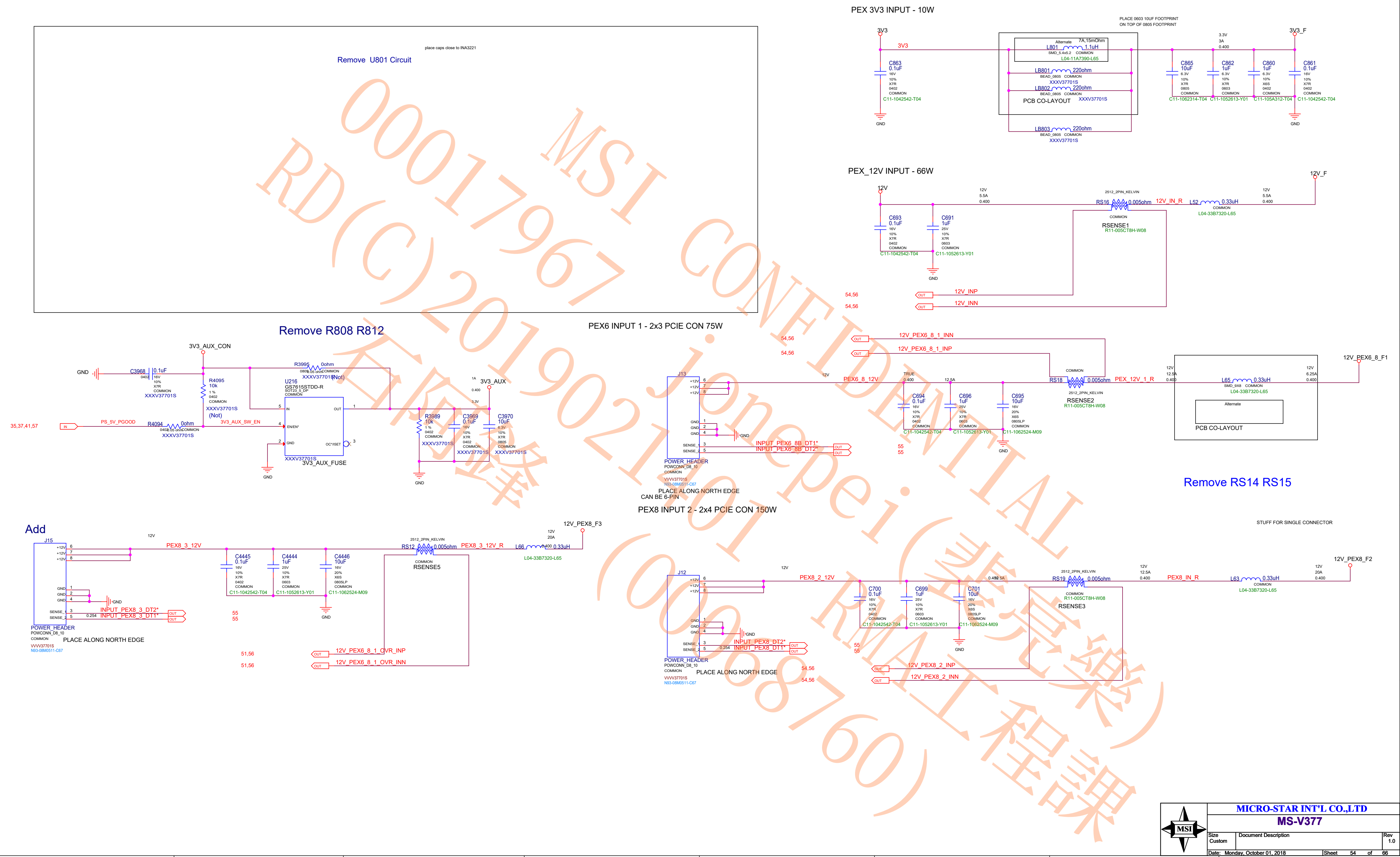
PS: Inputs, Filtering, and Monitoring



PEX 3V3 INPUT - 10W
3V3
3V3_F
PLACE 0603 10UF FOOTPRINT ON TOP OF 0805 FOOTPRINT
L801 1.1uH
LB801 220ohm
LB802 220ohm
LB803 220ohm
PCB CO-LAYOUT
C863 0.1uF
C865 10uF
C862 1uF
C860 1uF
C861 0.1uF
GND
PEX_12V INPUT - 66W
12V
12V_F
RS16 0.005ohm
12V_IN_R
L52 0.33uH
RSENSE1
C693 0.1uF
C691 1uF
12V_INP
12V_INN
place caps close to INA3221
Remove U801 Circuit
Remove R808 R812
3V3_AUX_CON
C3968 0.1uF
R4095 10k
R3995 0ohm
U216
3V3_AUX
PS_5V_PGOOD
R4094 0ohm
3V3_AUX_SW_EN
3V3_AUX_FUSE
R3989 10k
C3969 0.1uF
C3970 10uF
PEX6 INPUT 1 - 2x3 PCIE CON 75W
12V_PEX6_8_1_INN
12V_PEX6_8_1_INP
J13
PEX6_8_12V
RS18 0.005ohm
PEX_12V_1_R
RSENSE2
L65 0.33uH
12V_PEX6_8_F1
C694 0.1uF
C696 1uF
C695 10uF
INPUT_PEX6_8B_DT1*
INPUT_PEX6_8B_DT2*
POWER_HEADER
PLACE ALONG NORTH EDGE
CAN BE 6-PIN
PCB CO-LAYOUT
Remove RS14 RS15
PEX8 INPUT 2 - 2x4 PCIE CON 150W
STUFF FOR SINGLE CONNECTOR
Add
J15
PEX8_3_12V
C4445 0.1uF
C4444 1uF
C4446 10uF
RS12 0.005ohm
PEX8_3_12V_R
L66 0.33uH
12V_PEX8_F3
RSENSE5
INPUT_PEX8_3_DT2*
INPUT_PEX8_3_DT1*
12V_PEX6_8_1_OVR_INP
12V_PEX6_8_1_OVR_INN
J12
PEX8_2_12V
C700 0.1uF
C699 1uF
C701 10uF
RS19 0.005ohm
PEX8_IN_R
L63 0.33uH
12V_PEX8_F2
RSENSE3
INPUT_PEX8_DT2*
INPUT_PEX8_DT1*
12V_PEX8_2_INP
12V_PEX8_2_INN
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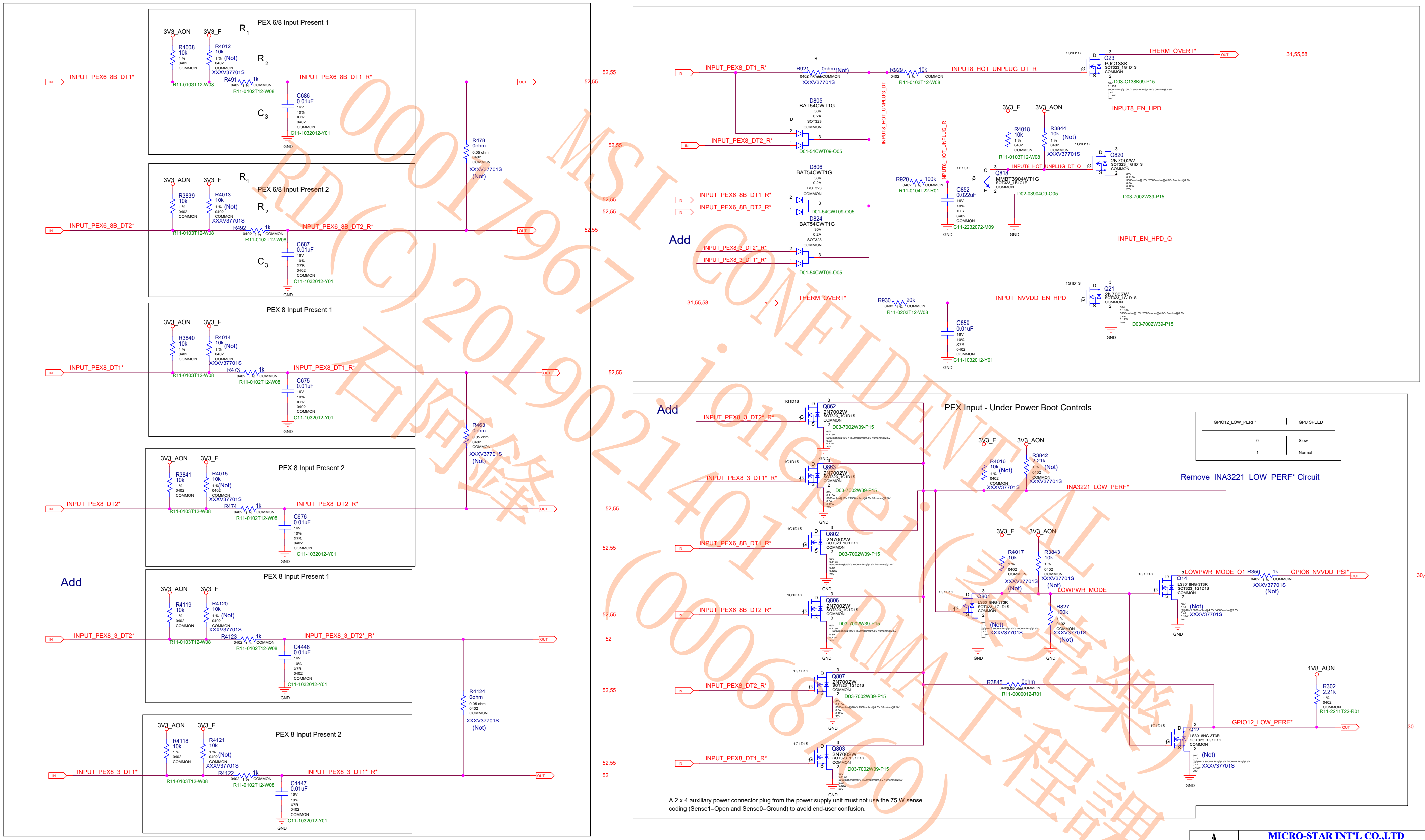
PS: 12V Current Steering & Hot Unplug Detect



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Size: Custom	Document Description: 12V Current Steering & Hot Unplug Detect	Rev 1.0
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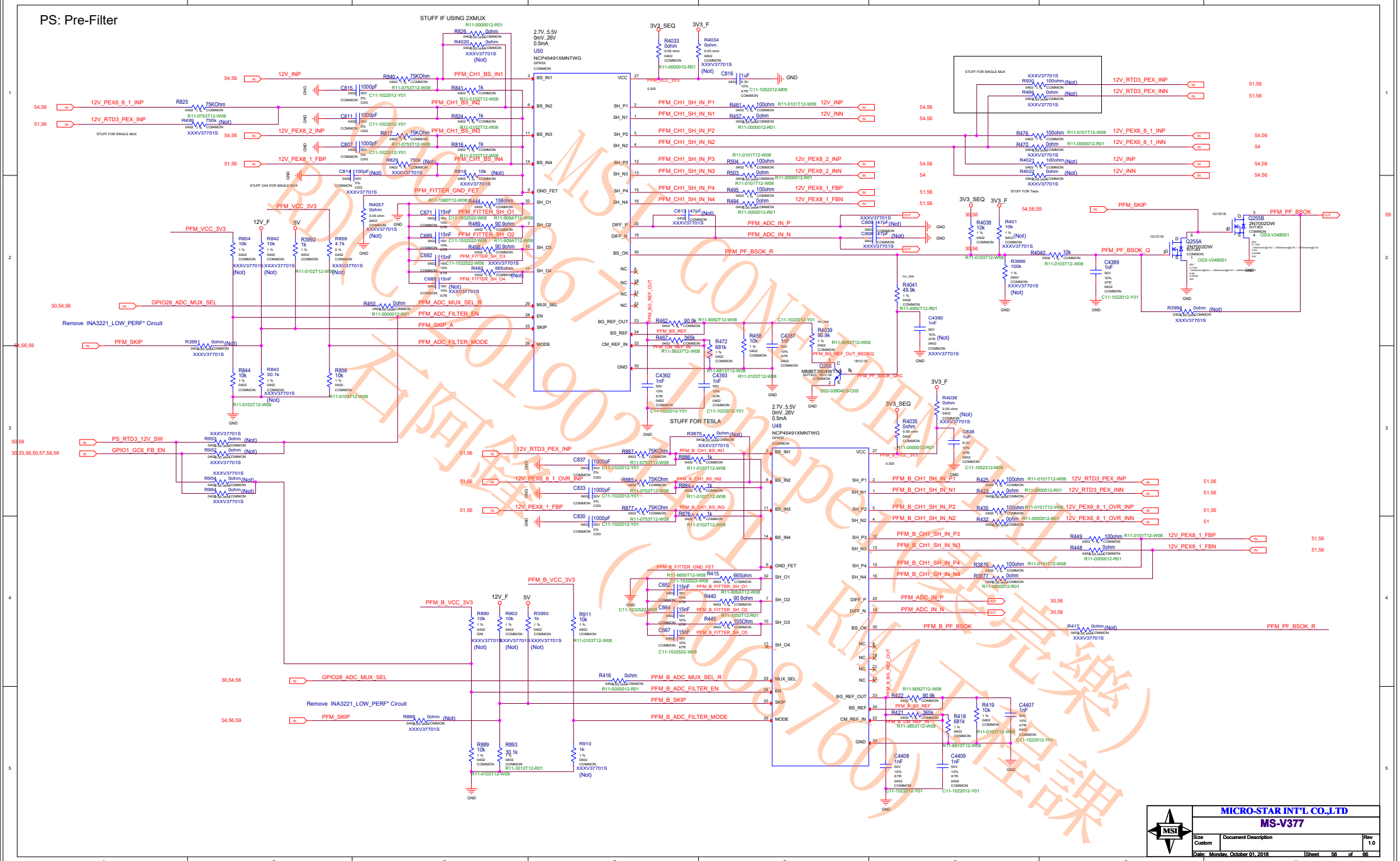
PS: Pre-Filter
STUFF IF USING 2XMUX
U50
NCP45491XMNTWG
U48
NCP45491XMNTWG
STUFF FOR TESLA
Remove INA3221_LOW_PERF* Circuit
Remove INA3221_LOW_PERF* Circuit
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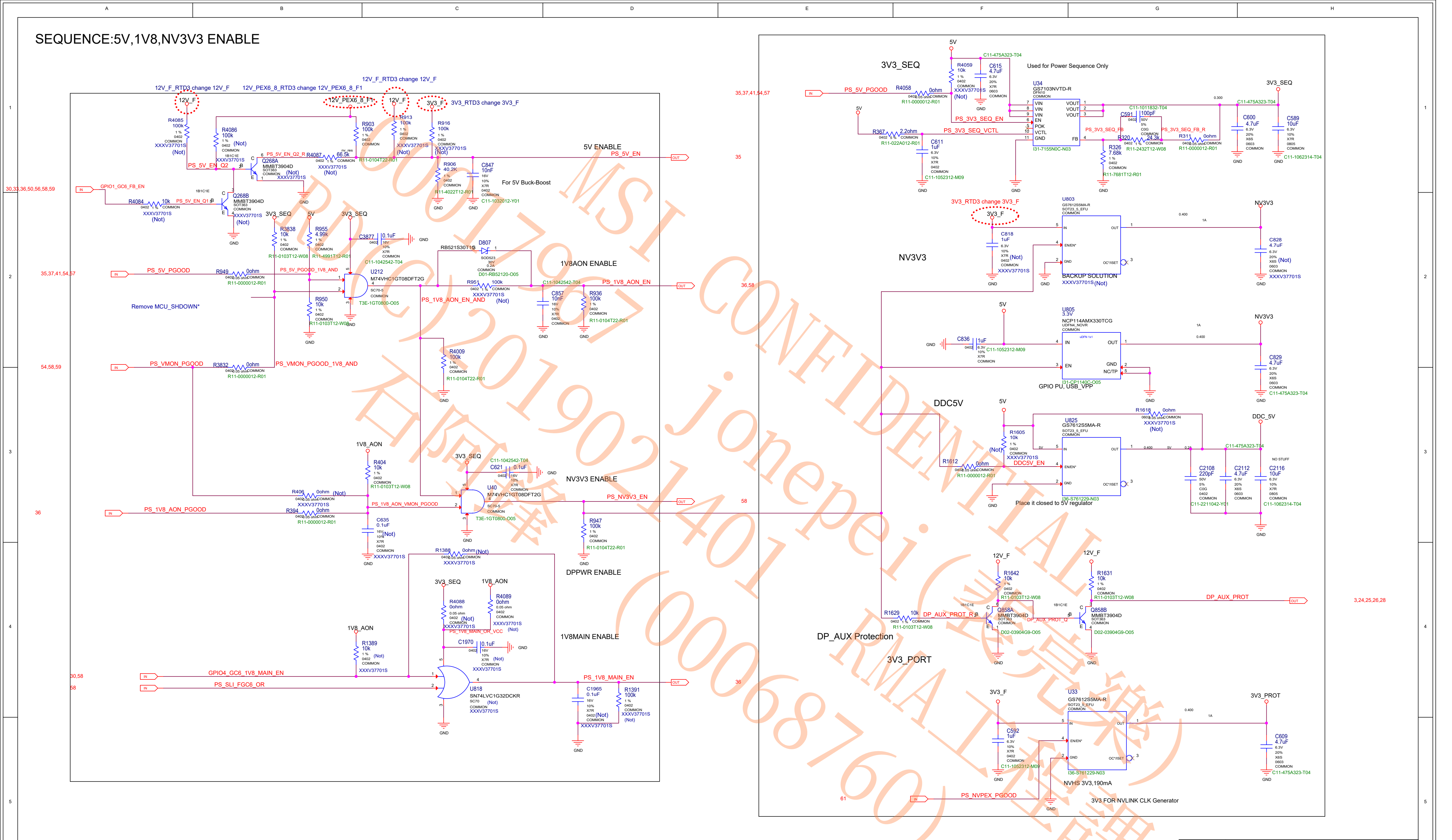

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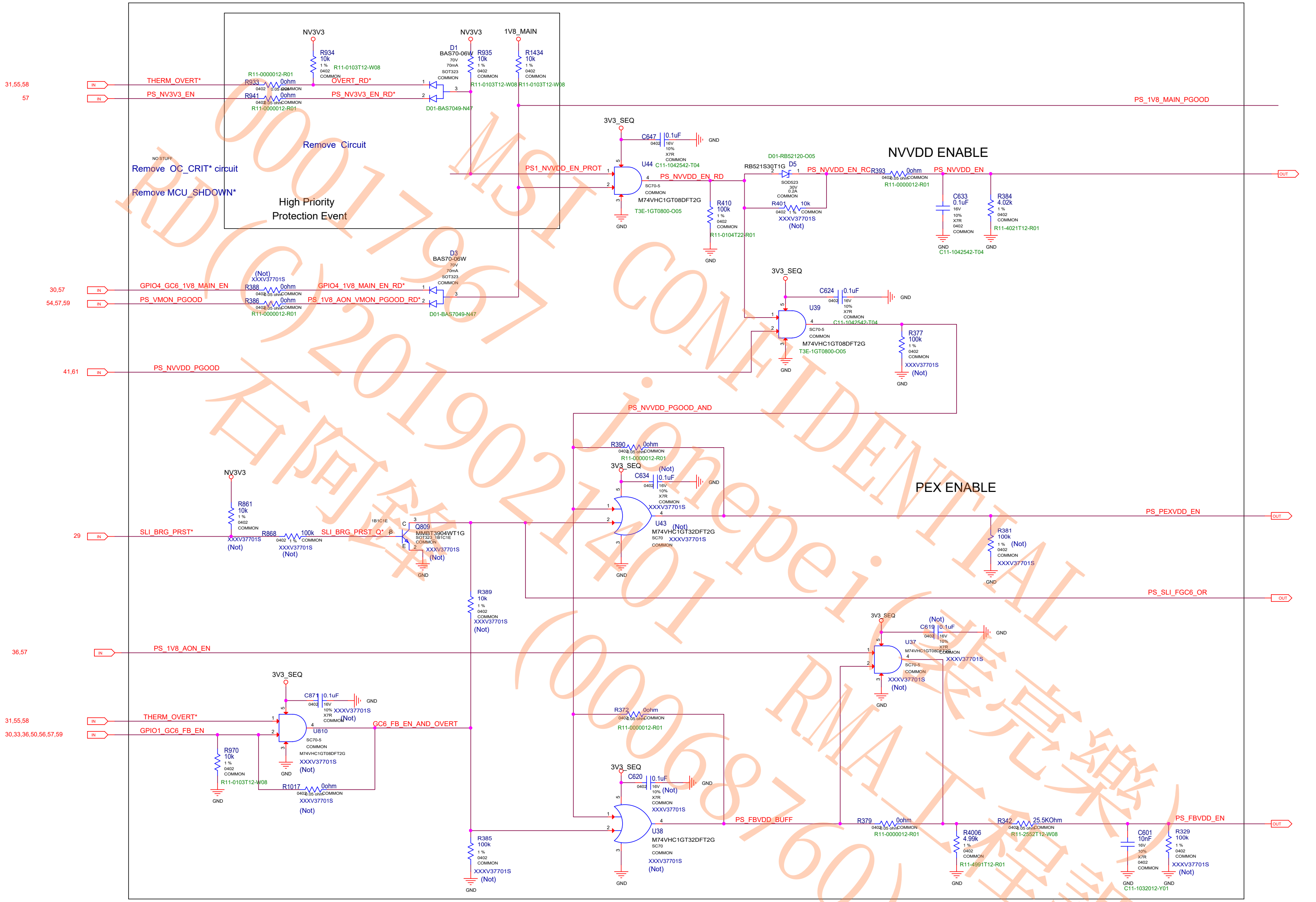
SEQUENCE:NV,PEX,FB ENABLE



MICRO-STAR INT'L CO.,LTD			
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Size: Custom	Document Description: NV,PEX,FB ENABLE		Rev: 1.0
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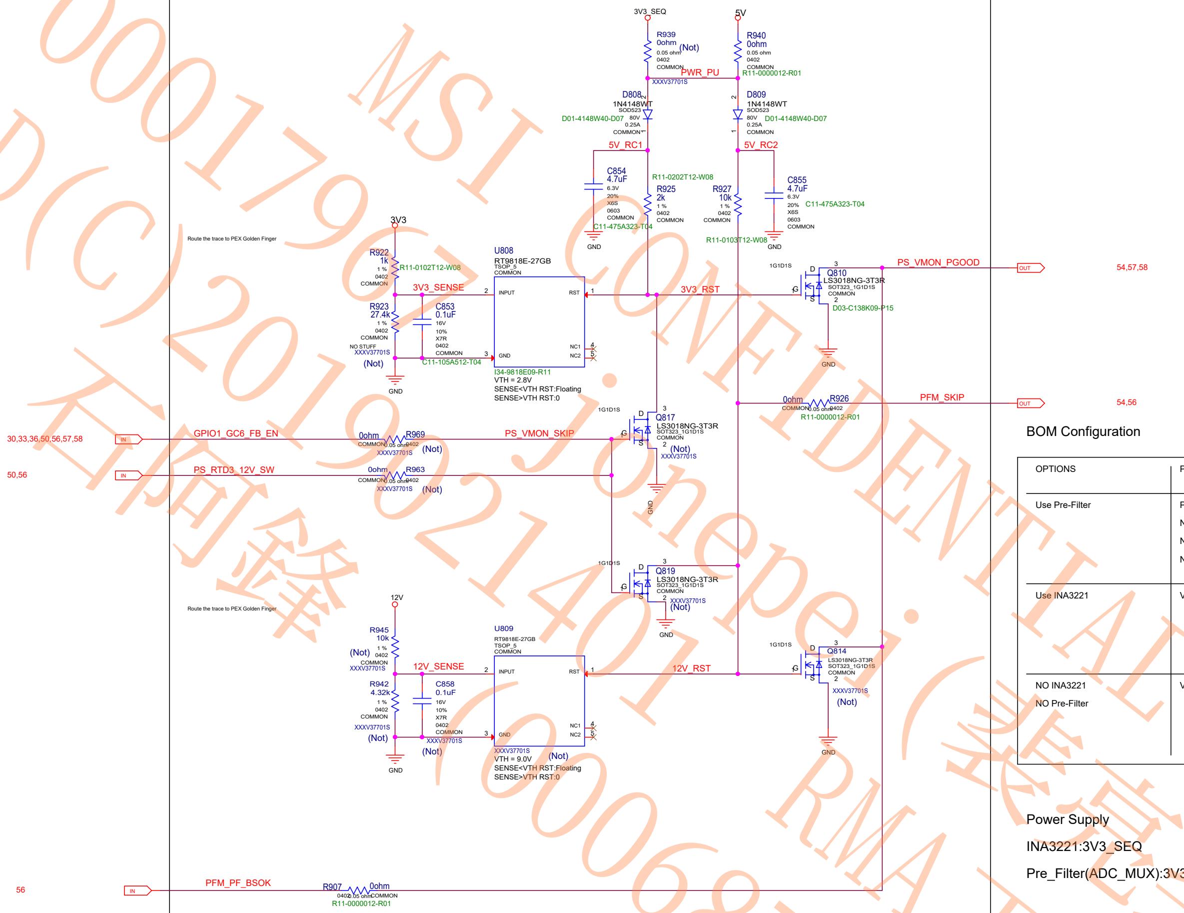
SEQUENCE:PCIE Voltage Monitor

PCIE Voltage Monitor



Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)
PS_RTD3_12V_SW	INPUT	GC6_FB_EN && IDLE_IN_SW

BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	Pre-Filter NO STUFF U12 NO STUFF Q3,Q5 NO STUFF D15	Pre-Filter NO STUFF U13 NO STUFF Q4	Pre-Filter
Use INA3221	Voltage_Monitor	INA3221 NO STUFF U12 NO STUFF Q4	INA3221
NO INA3221 NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Power Supply

INA3221:3V3_SEQ

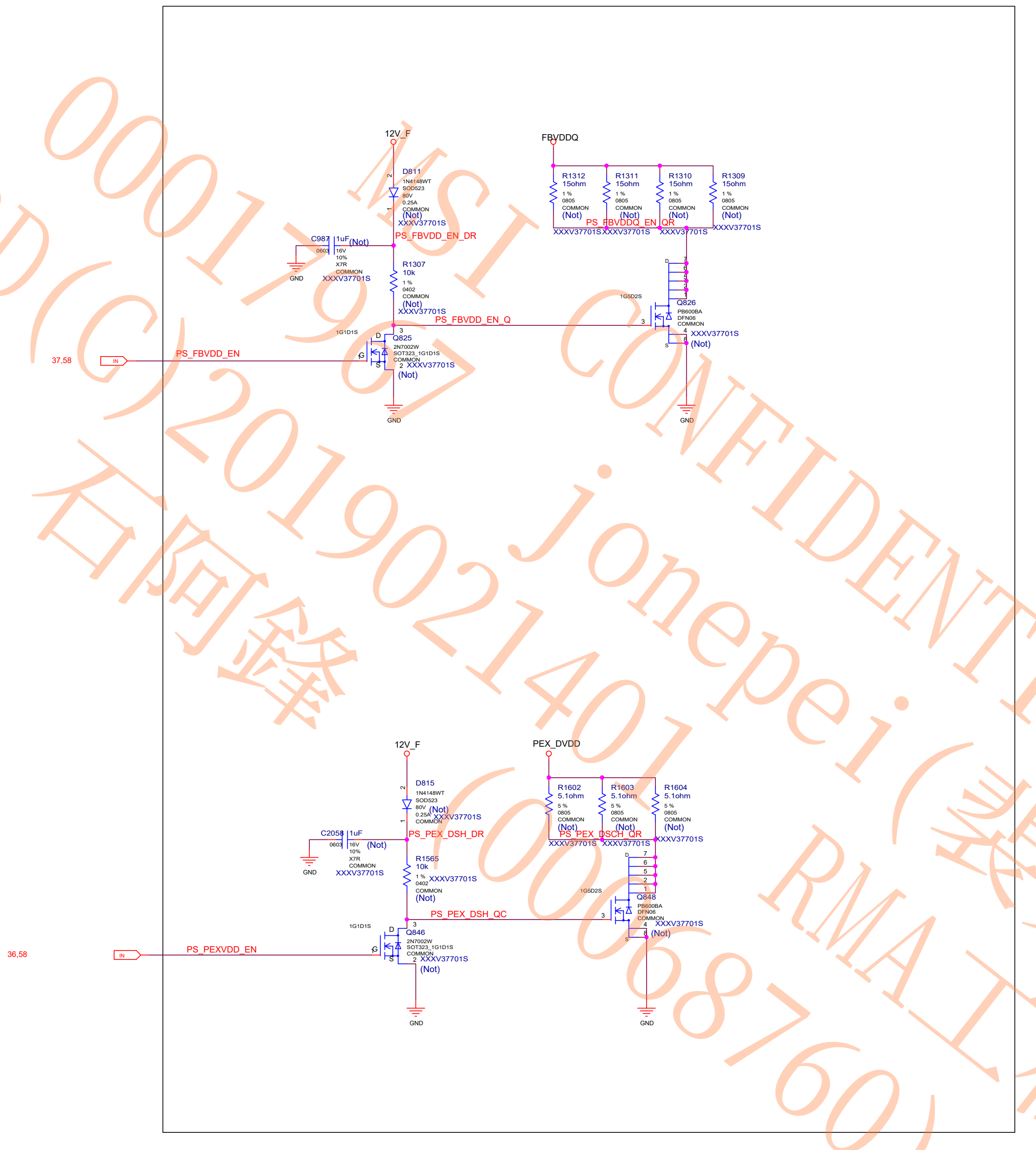
Pre_Filter(ADC_MUX):3V3(PEX)

Dual Pre-Filter case:

Only use the Primary Pre-Filter to sense 3V3PEX

and All Input 12Vs

SEQUENCE:Discharge



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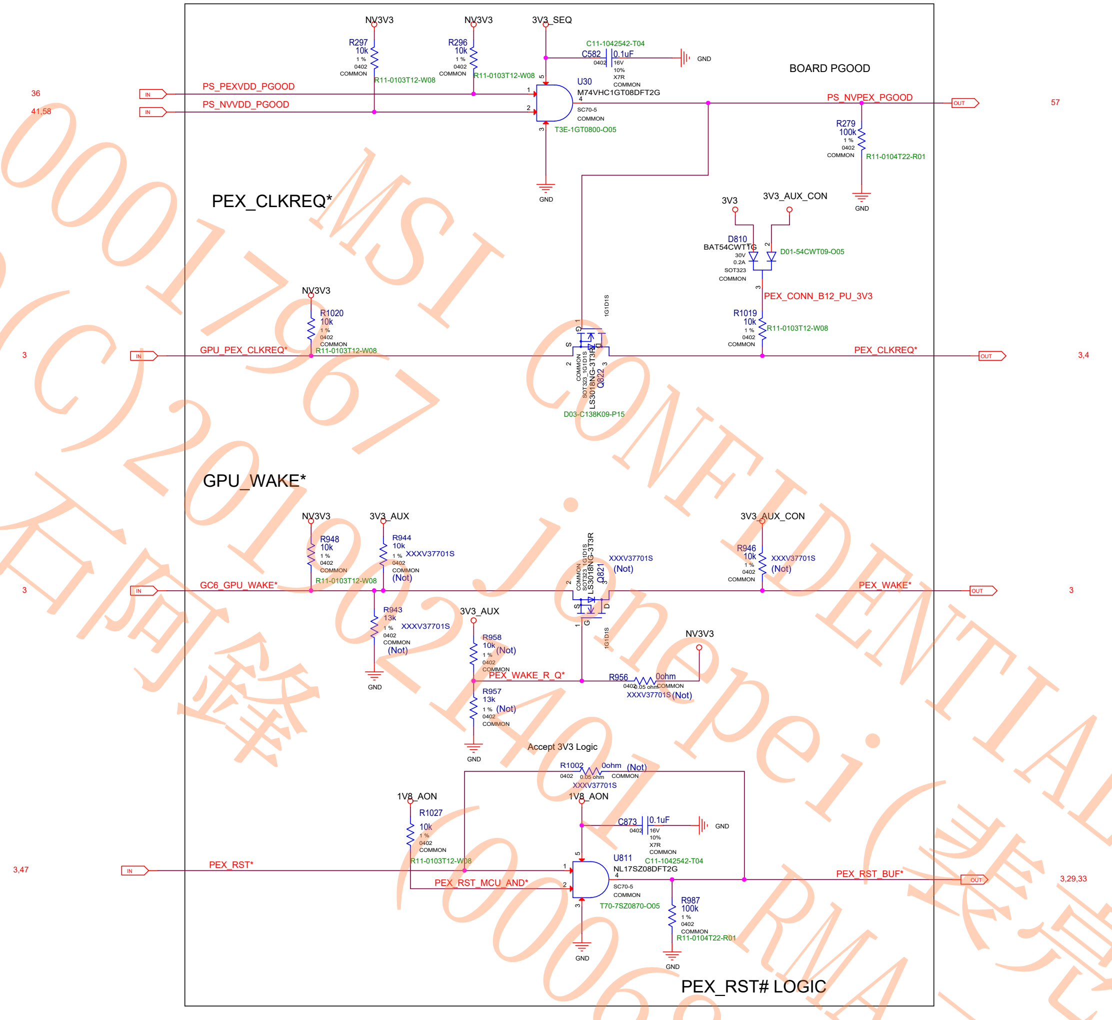
SEQUENCE:MISC



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Custom	MISC	1.0

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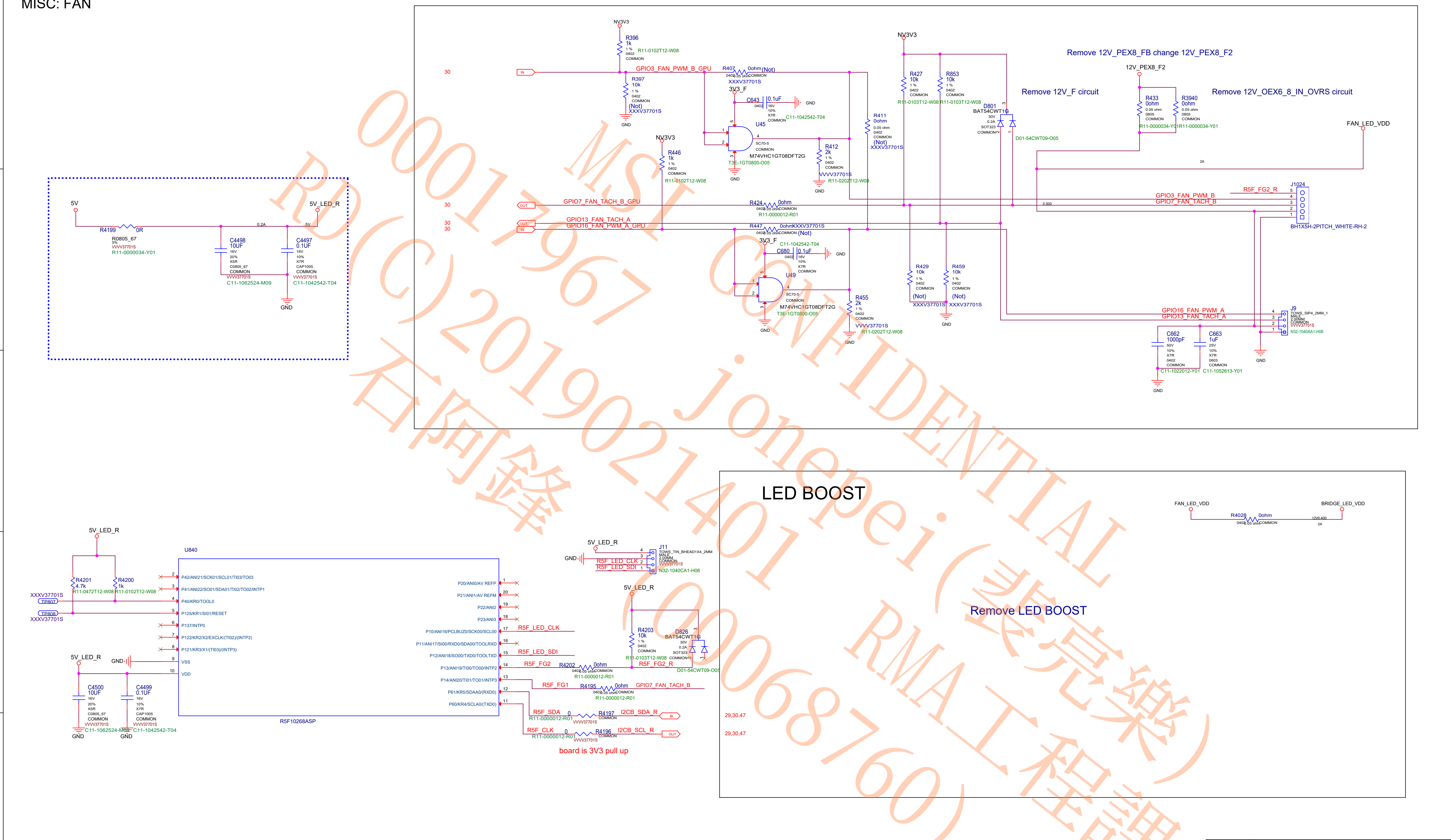
MISC: FAN



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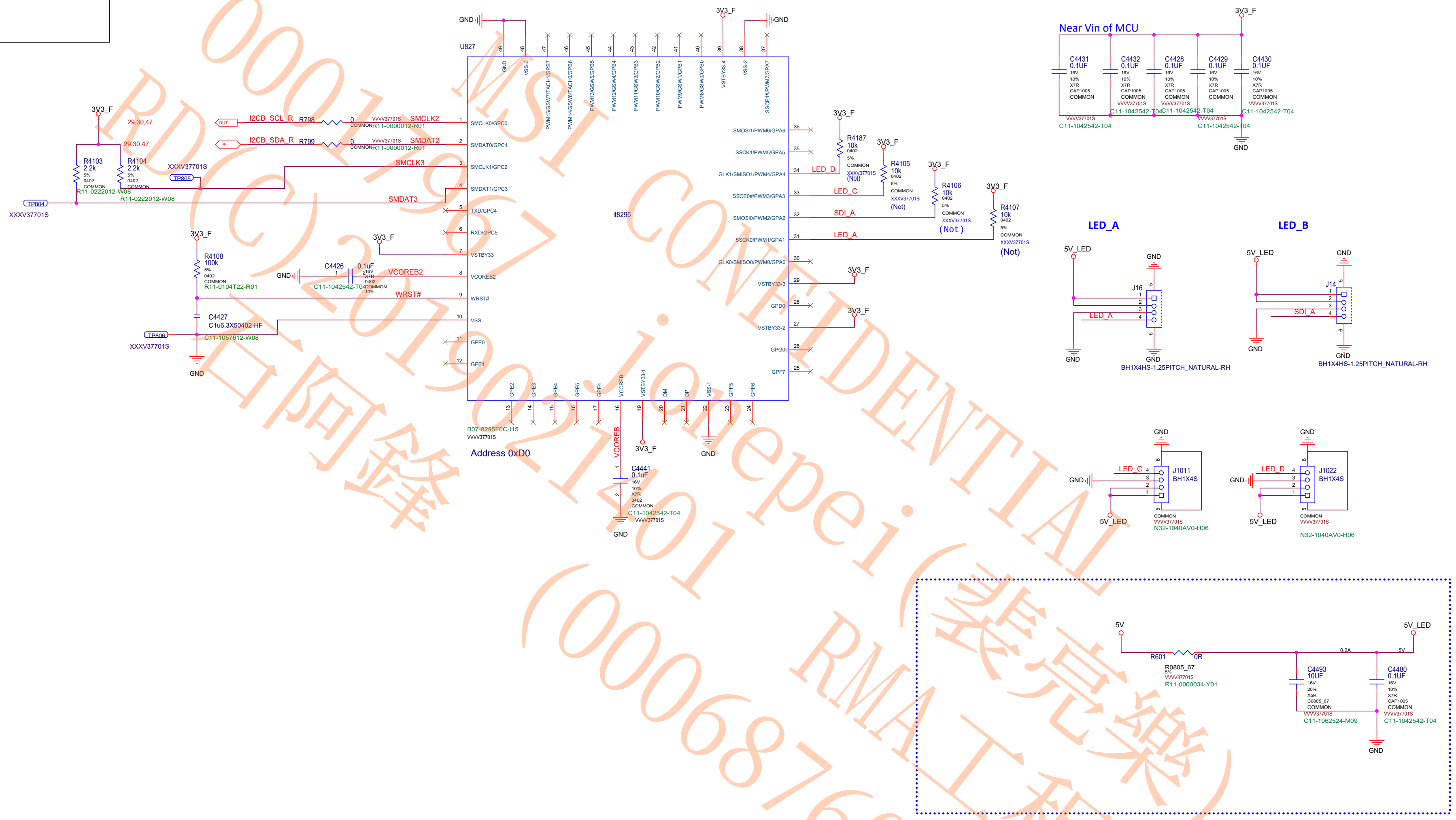
MISC: LED2

LED_CONTROLLER_IT8295

9/27 Remove J803
9/27 ADD TP804 / TP805

Firmware Programming
Debug



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ZERO IDLE POWER MCU

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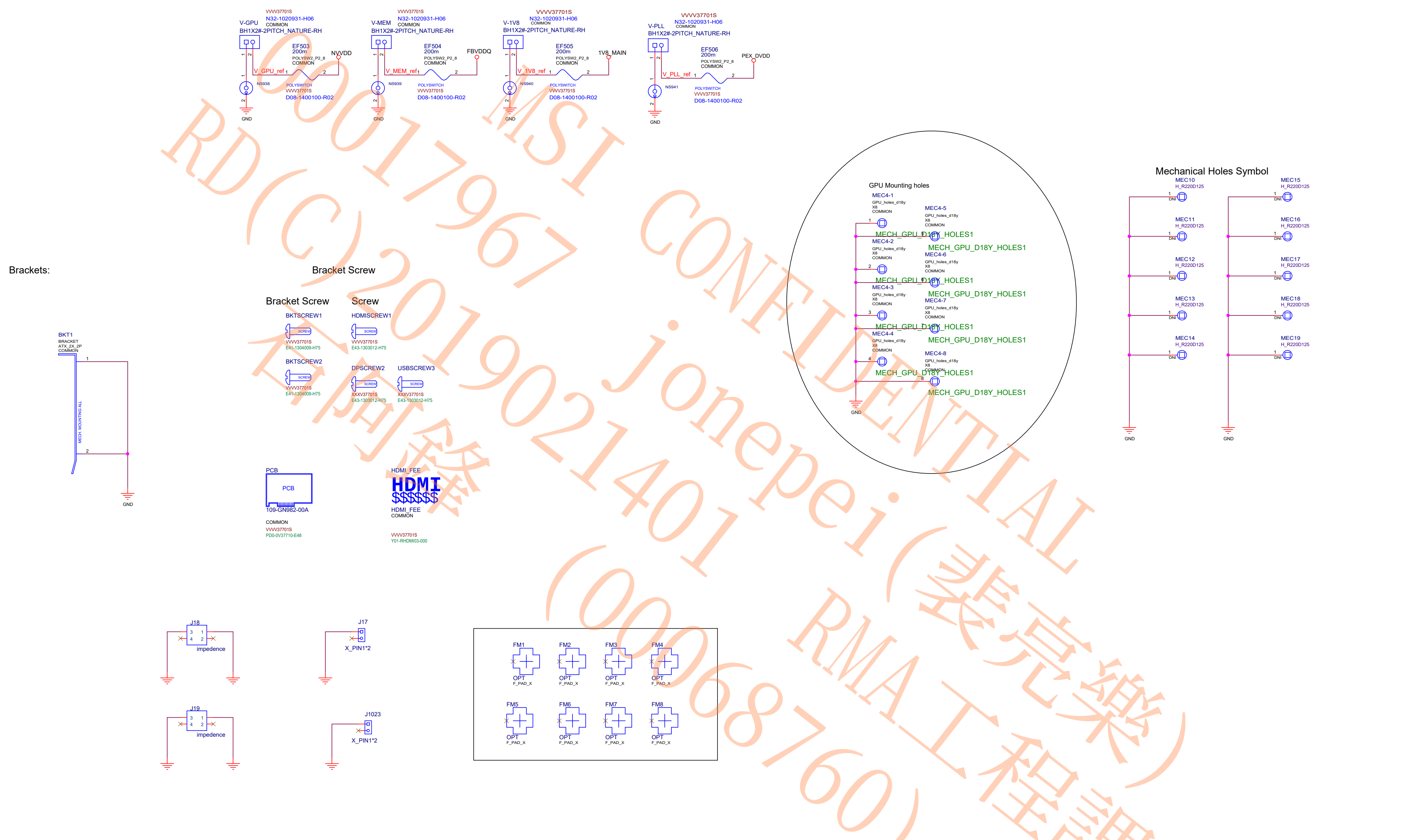
Mechanical: Bracket/Thermal Solution



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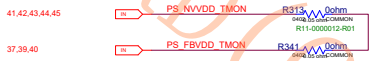
VR THERMAL PROTECTION



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