PG142-B00

DP + DP + DP + HDMI/DP

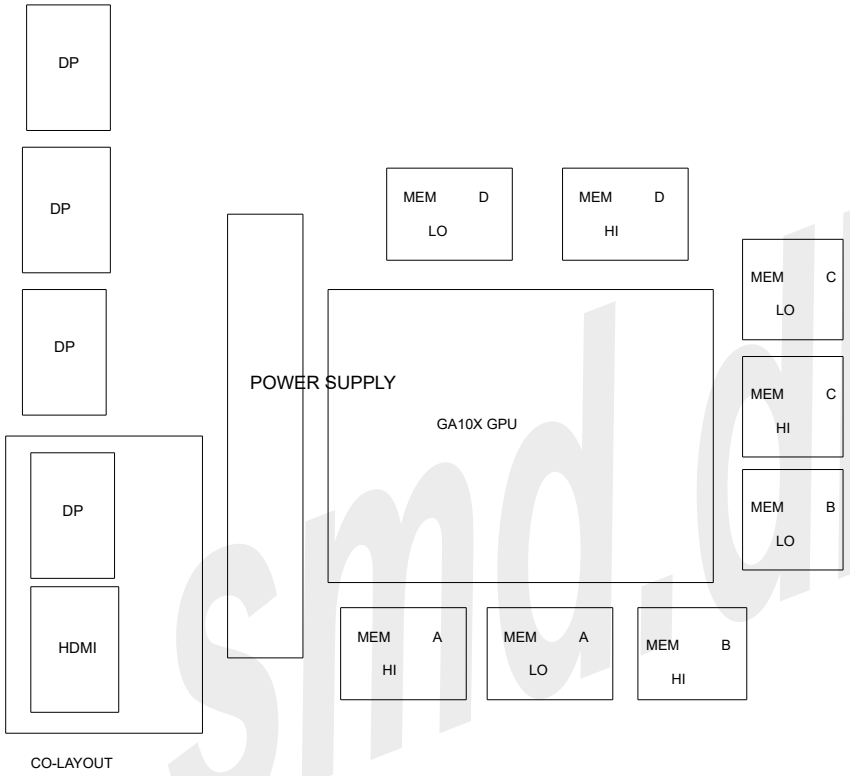
TABLE OF CONTENTS

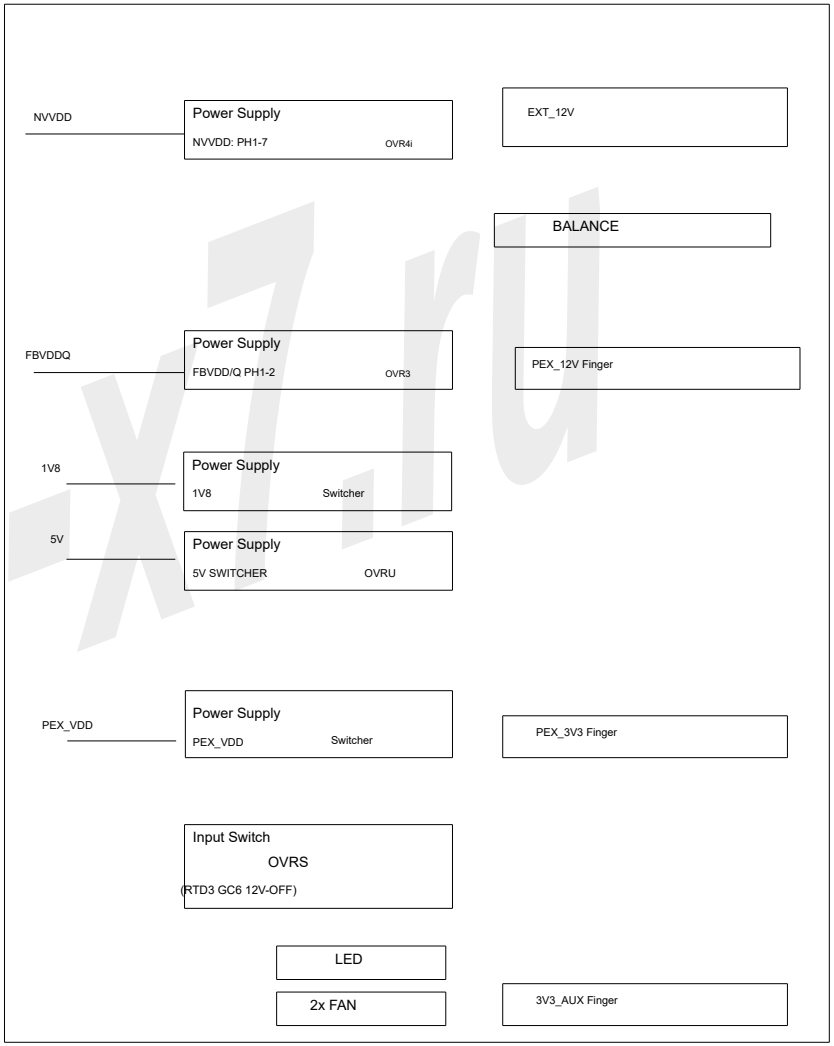
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Table of Contents

MAY
ALL
STANDARDS.

[redacted]

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	1 OF 54
BOM REV	A	DATE	27-JUN-2020





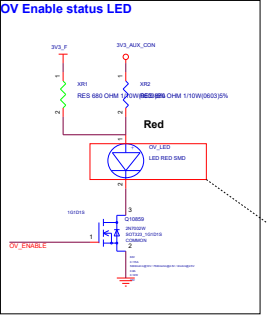
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Block Diagram

MAY
ALL
STANDARDS.

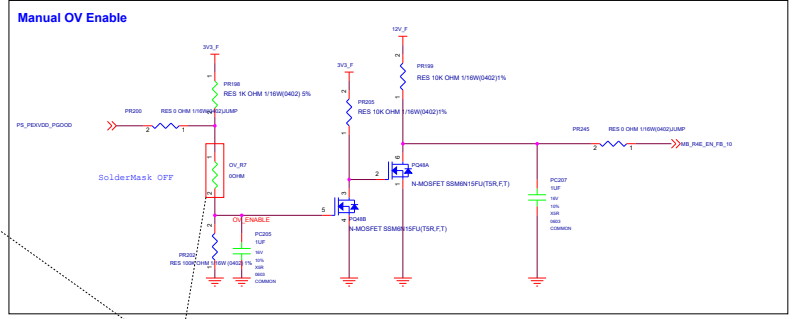
[redacted]

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	2 OF 54
BOM REV	A	DATE	27-JUN-2020

OV Enable status LED

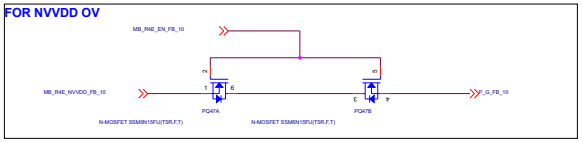


Manual OV Enable

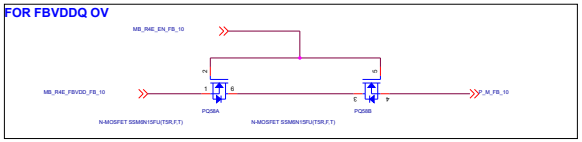


PLACE TOGETHER

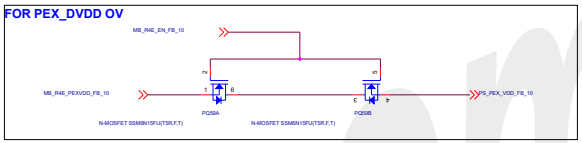
FOR NVVDD OV



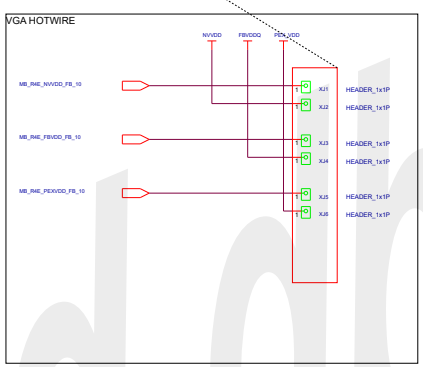
FOR FBVDDQ OV



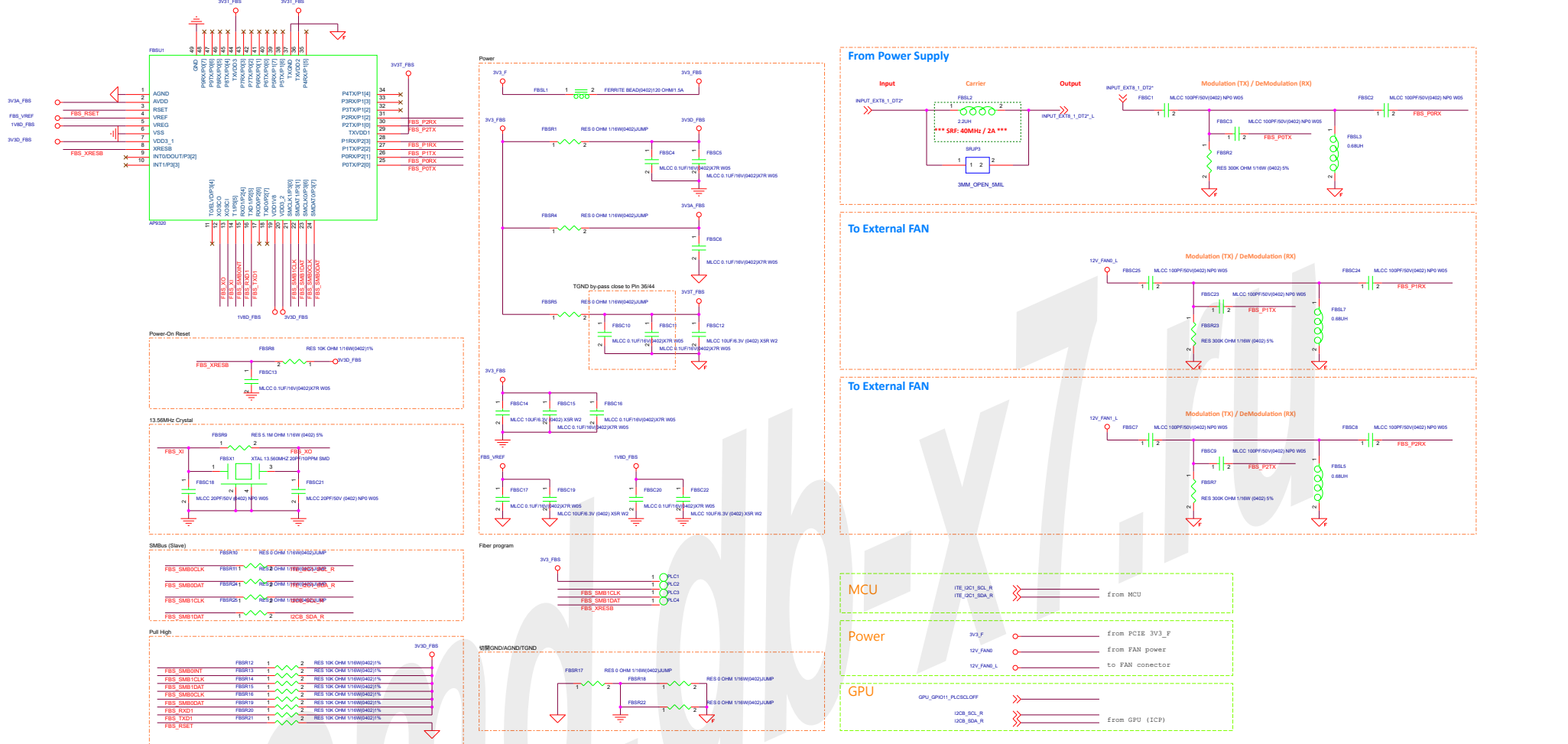
FOR PEX_DVDD OV

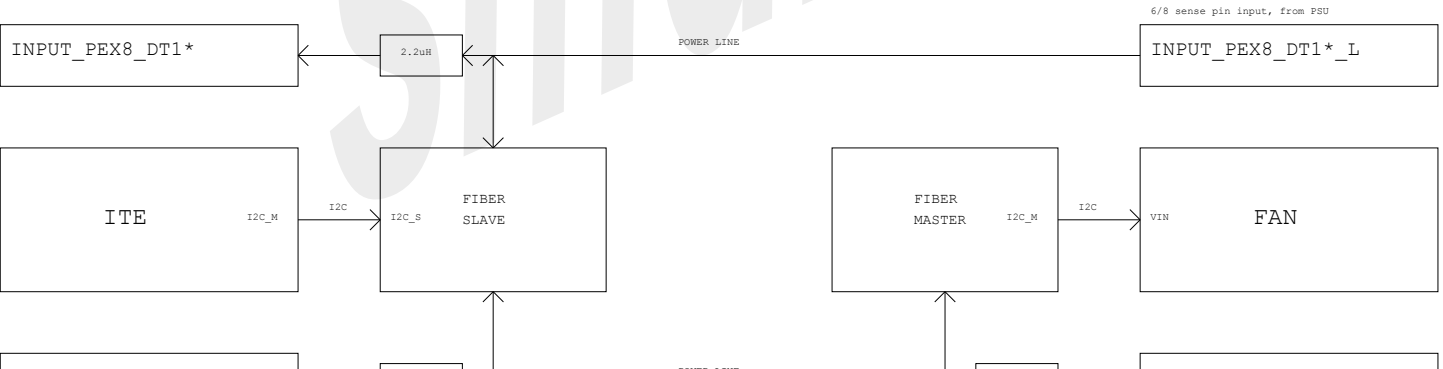


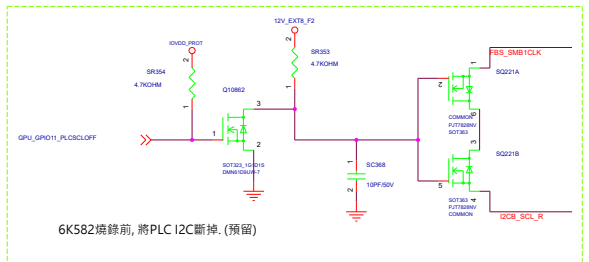
VGA HOTWIRE



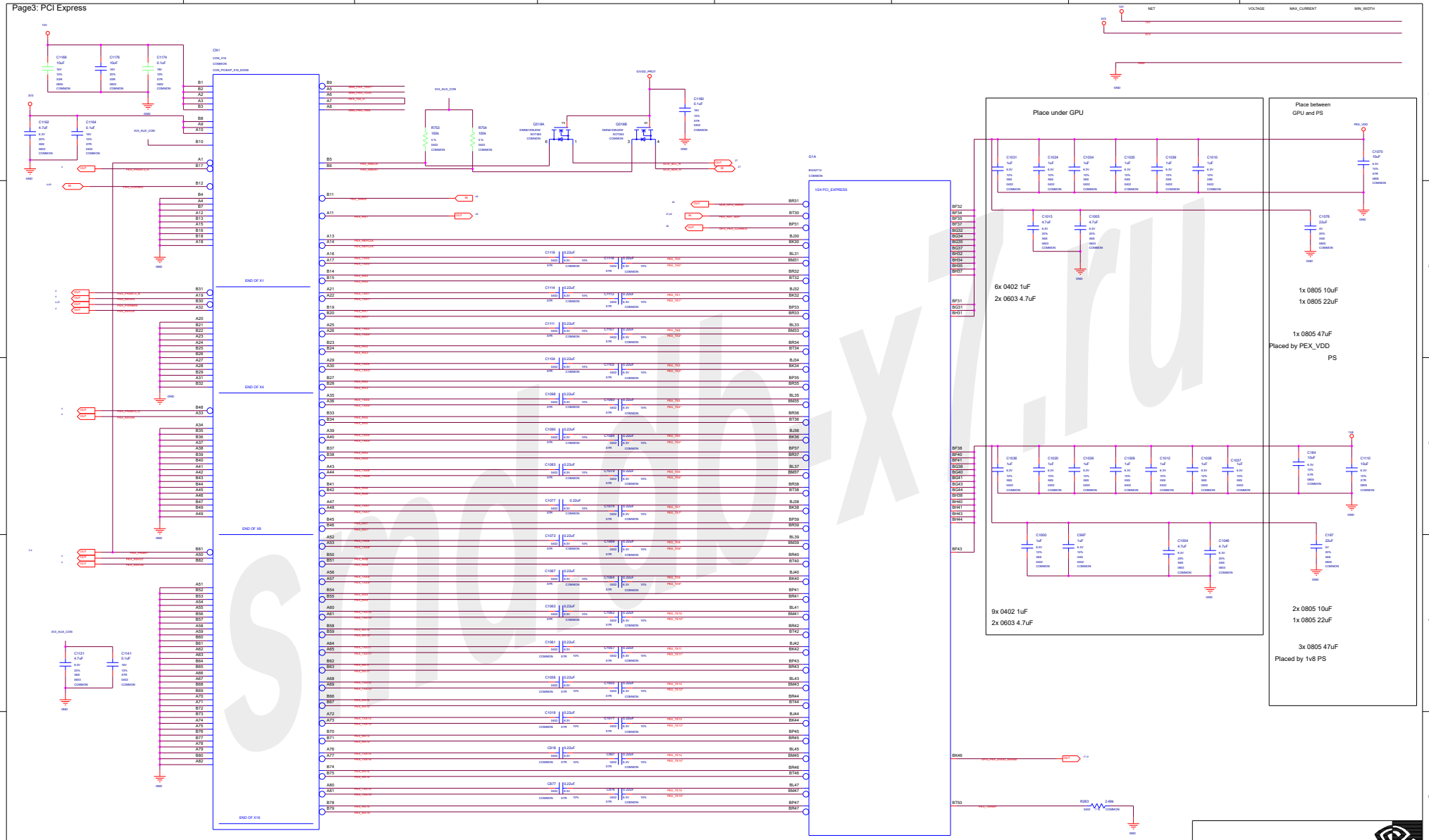
Title	<Title>	
Size: A2	Document Number <Doc>	Rev <RevCode>
Date: Monday, July 27, 2020	Sheet 6 of 7	







Title	<Title>		
Size: C	Document Number: <Doc>		Rev: <RevCode>
Date: Monday, July 27, 2020	Sheet 7 of 7		

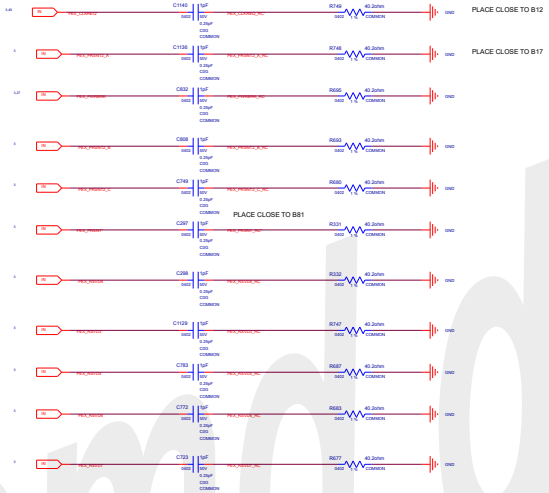


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCI Express

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	3 OF 54
DATE	27-JUN-2020

MAY
ALL
STANDARDS.

Page4: PCIE GEN4 RC TERMINATIONS

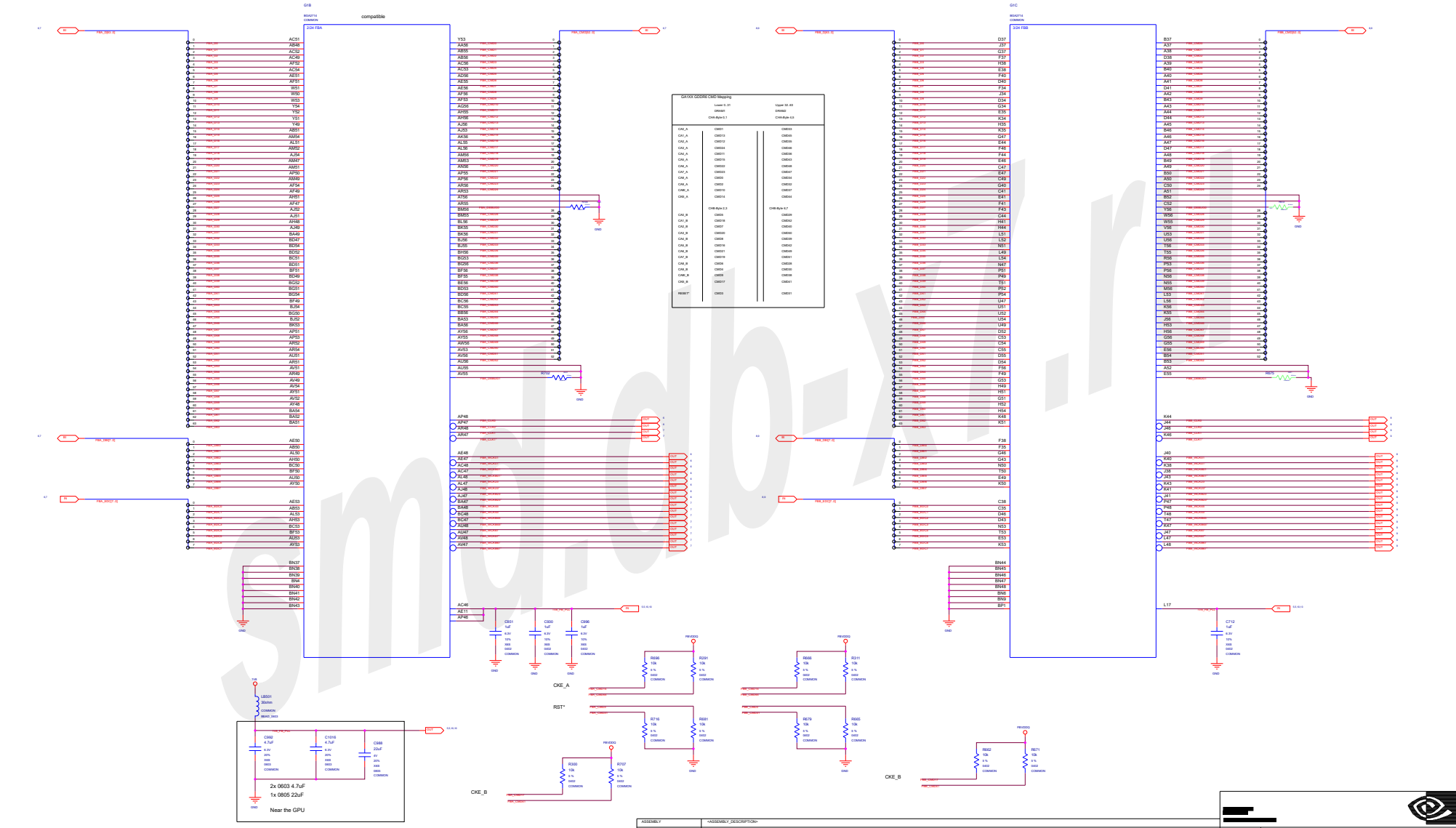


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PCIE GEN4 RC TERMINATIONS

MAY
ALL
STANDARDS.

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	4 OF 54
BOM REV	A	DATE	27-JUN-2020

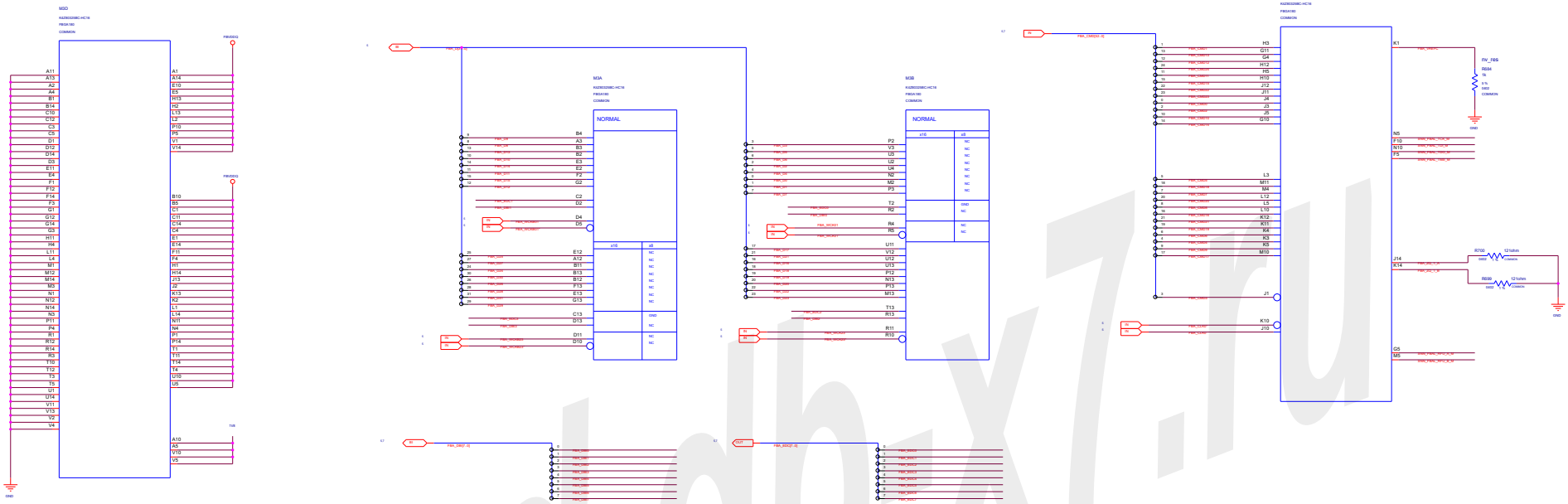
//syseng/Projects/GA1xx/GA1XX_CMD-Mapping.xlsx



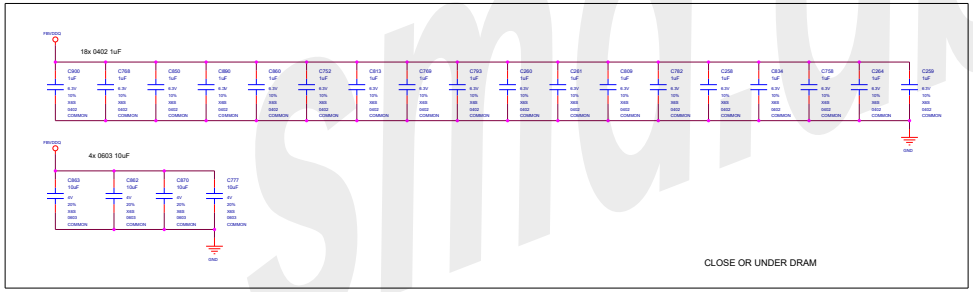
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: GPU FB_AB

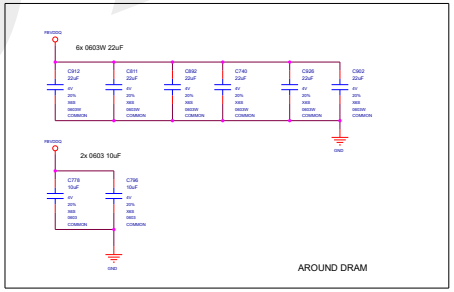
NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	5 OF 54
DATE	27-JUN-2020

MAY
ALL
STANDARDS.



decap via : at least 2 gnd vias and 2 power vias for each cap





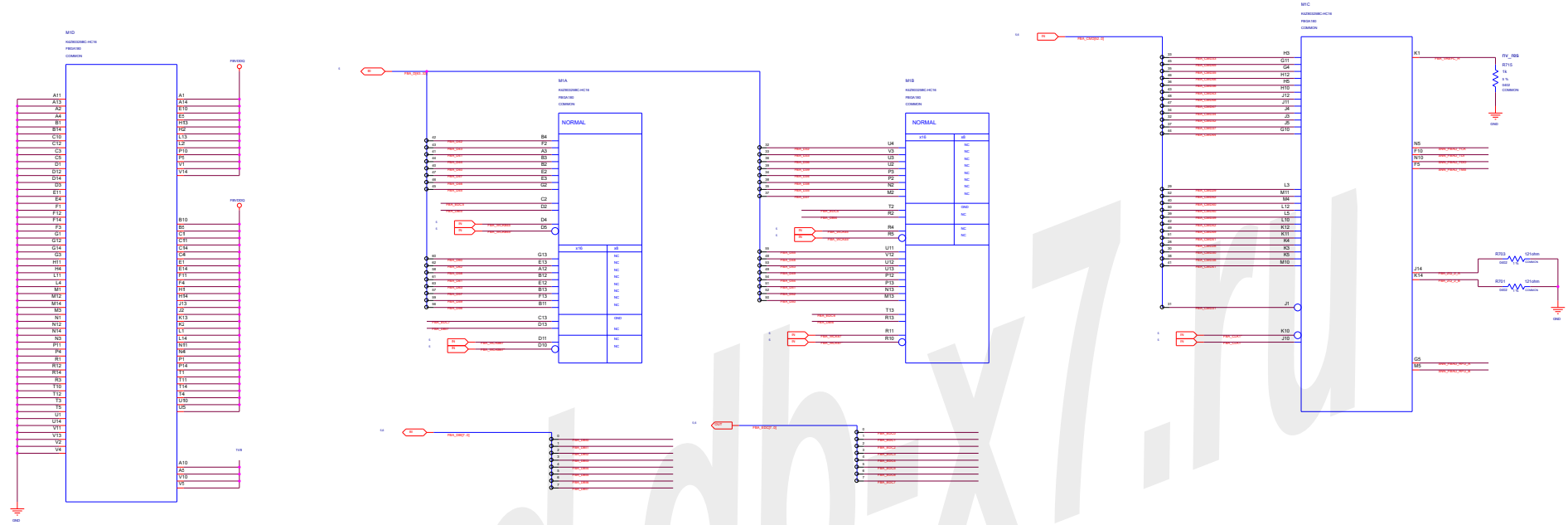
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBA[31:0]

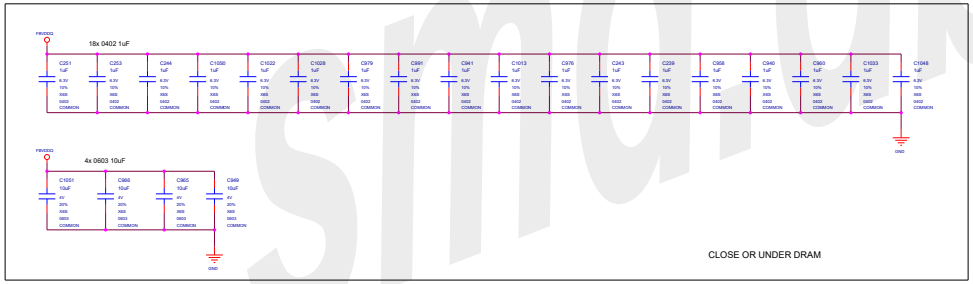
[redacted]

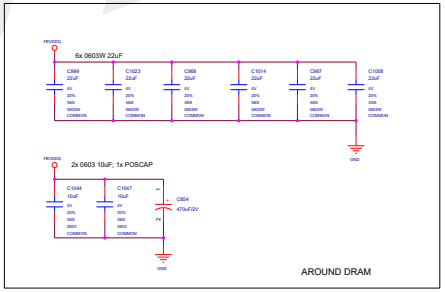
NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	6 OF 54
BOM REV	A	DATE	27-JUN-2020

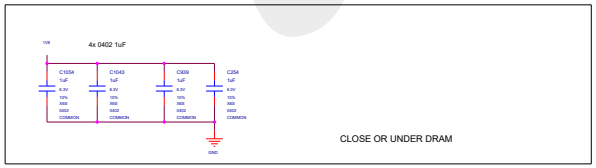
MAY
ALL
STANDARDS.

Page7: MEMORY: FBA Partition 63..32







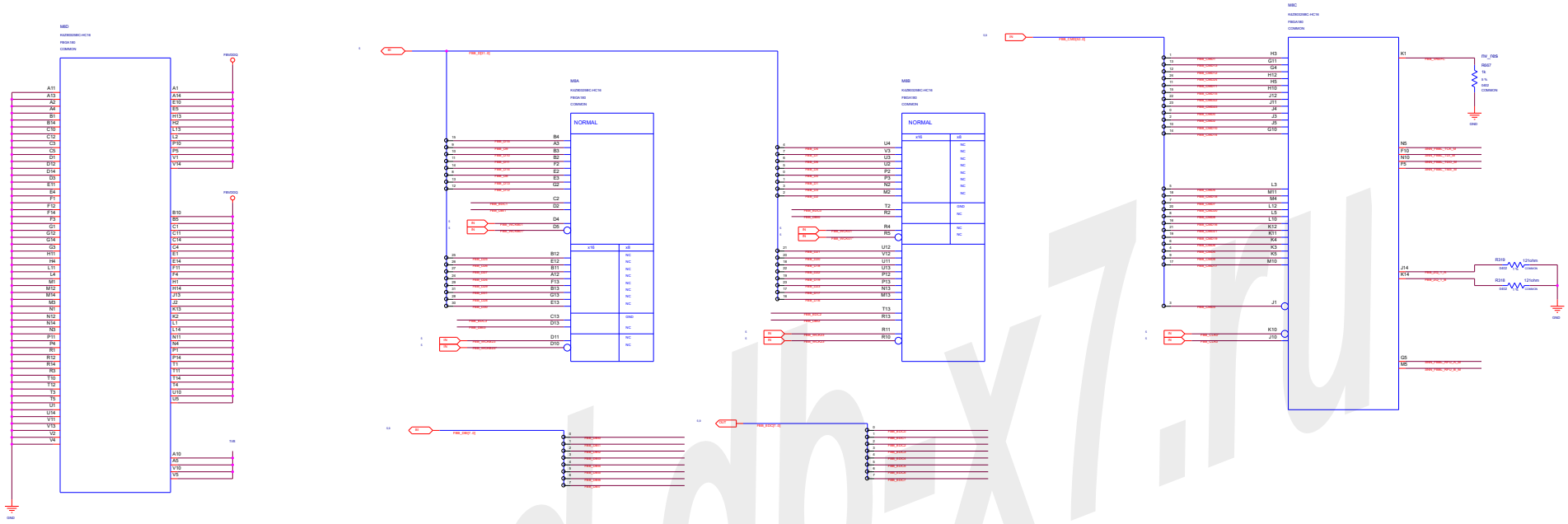


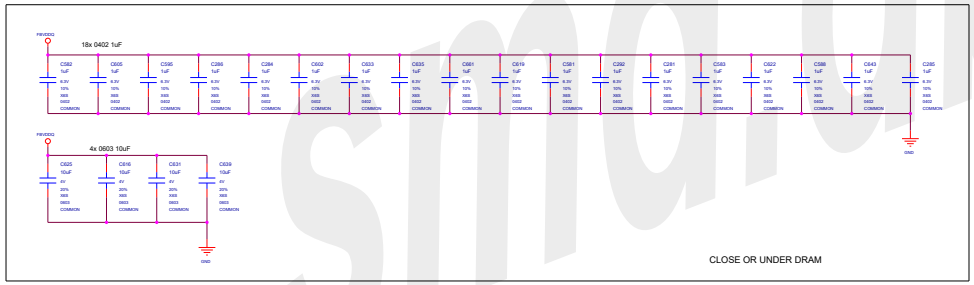
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBA[63:32]

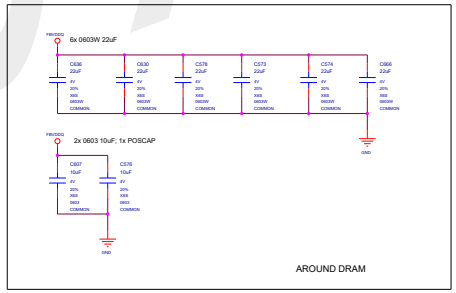
[redacted]

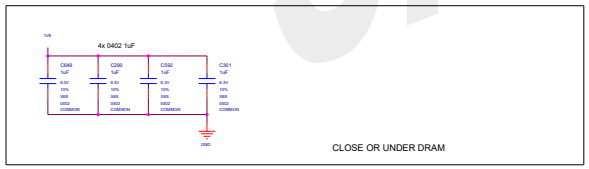
NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	7 OF 54
DATE	27-JUN-2020

MAY
ALL
STANDARDS.







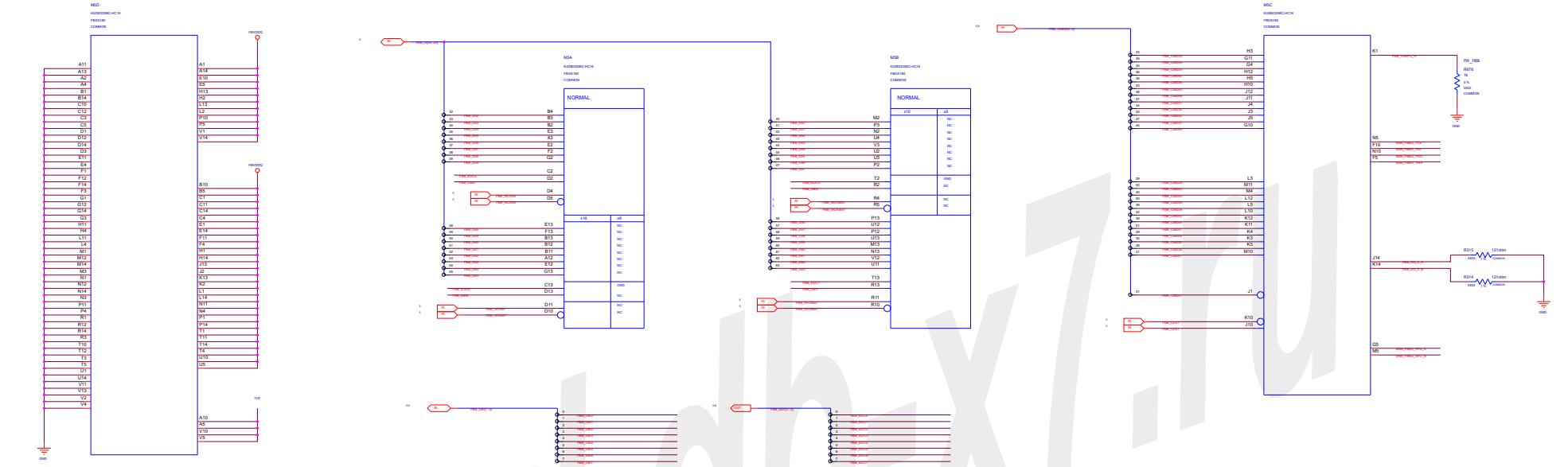


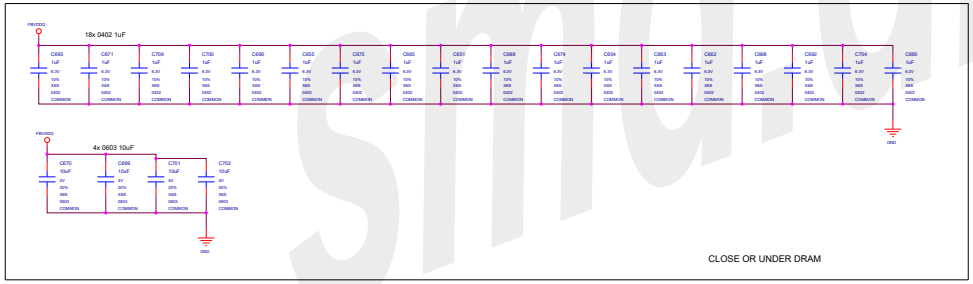
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBB[31:0]

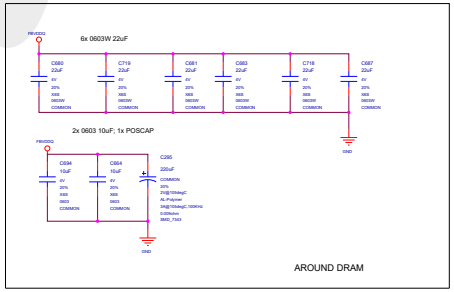
MAY
ALL
STANDARDS.

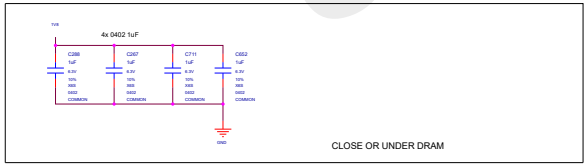
[redacted]

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	8 OF 54
DATE	27-JUN-2020



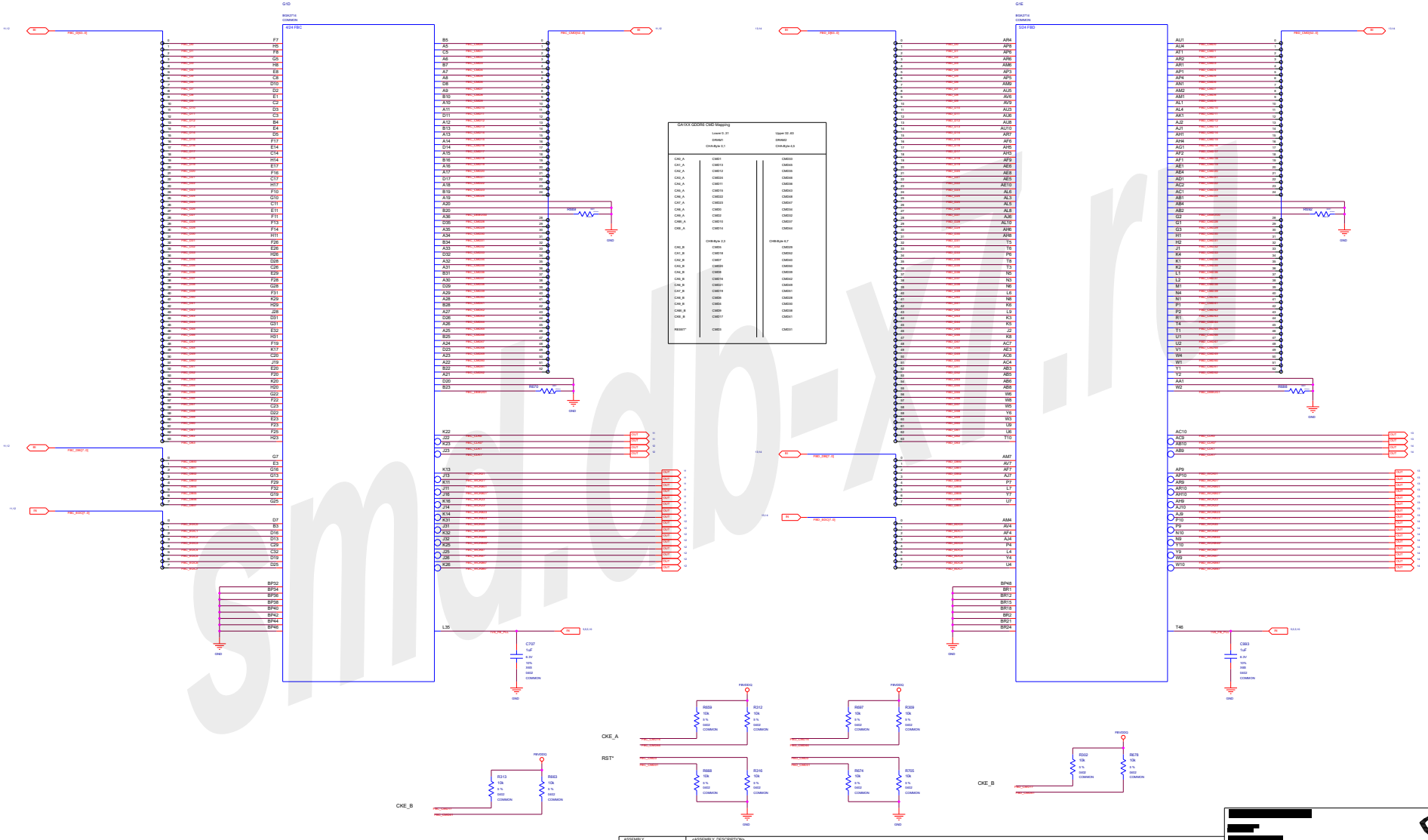






ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBB[63:32]

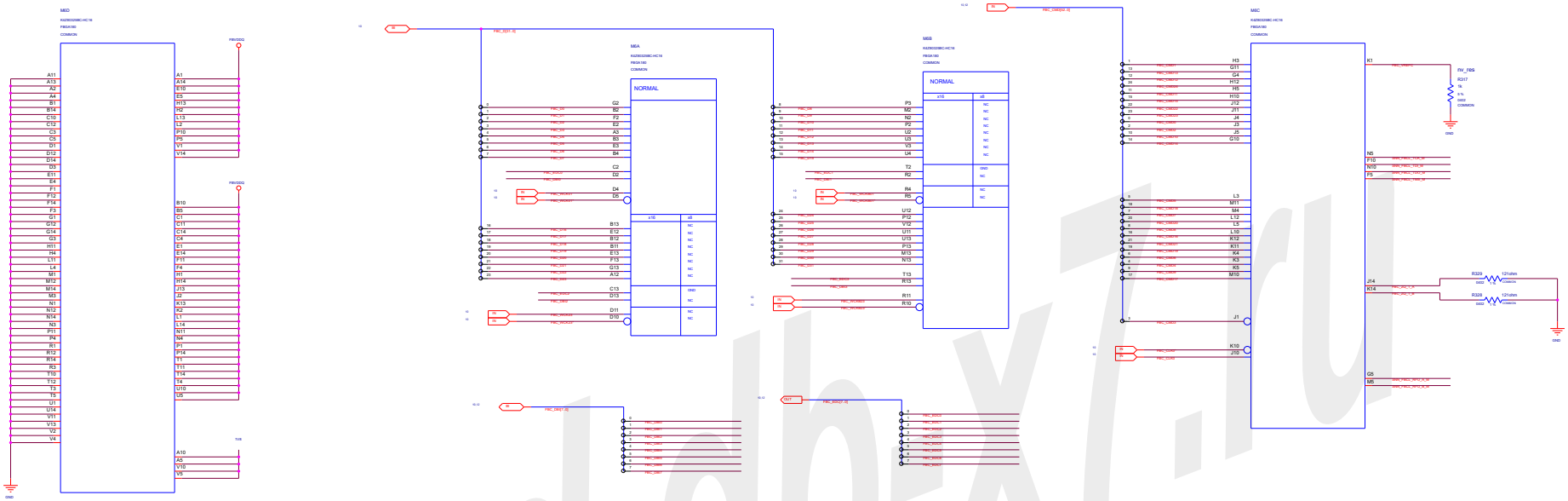
NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
PAGE	9 OF 54
BOM REV	A
DATE	27-JUN-2020

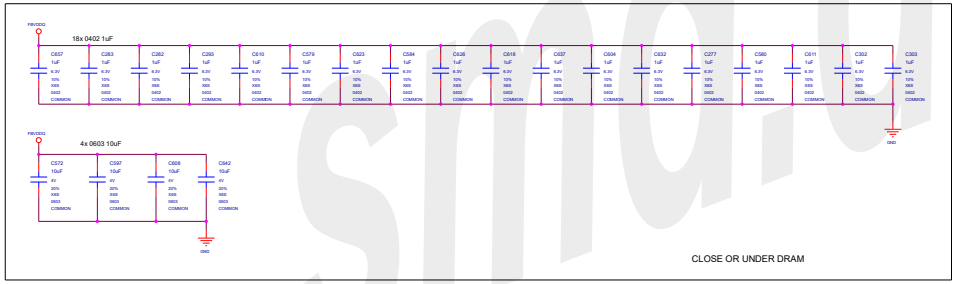


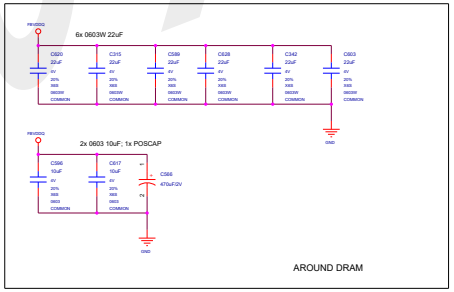
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: GPU FB_CD

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	10 OF 54
DATE	27-JUN-2020

MAY
ALL
STANDARDS.





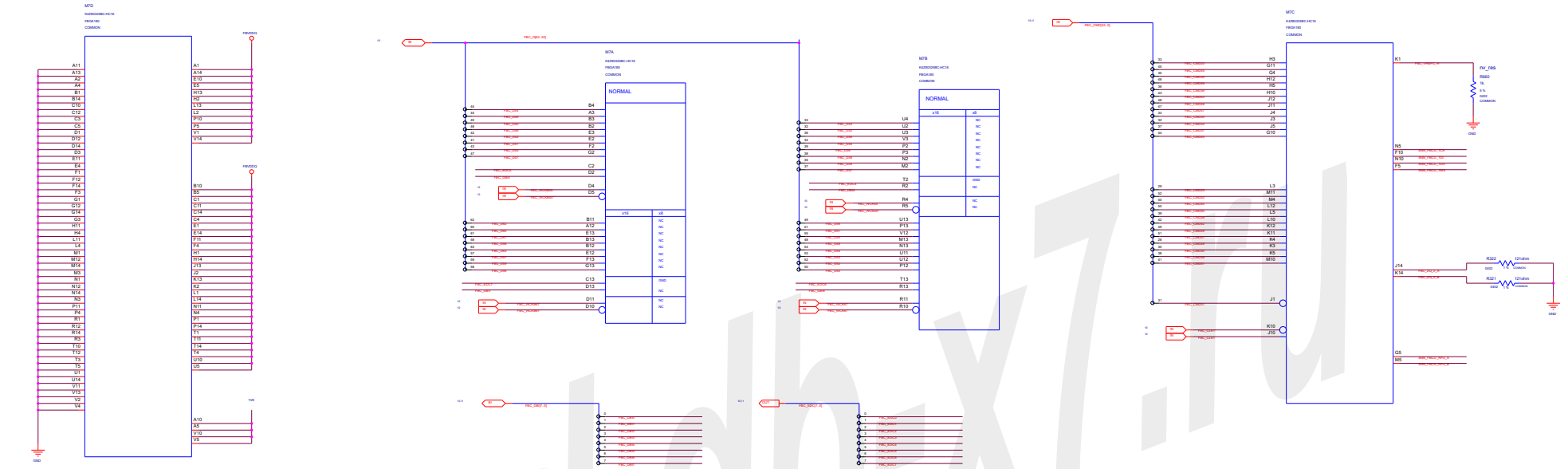


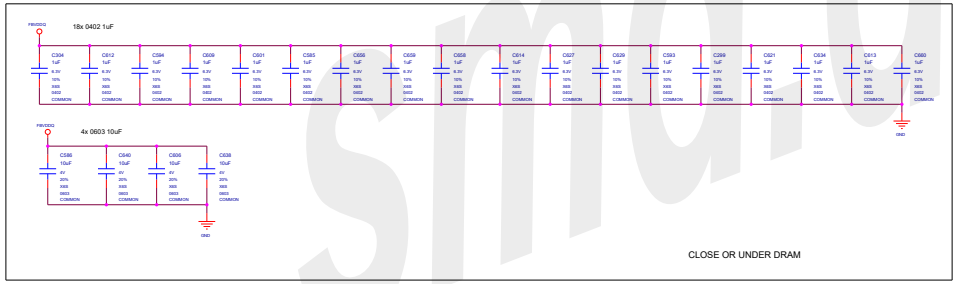
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBC[31:0]

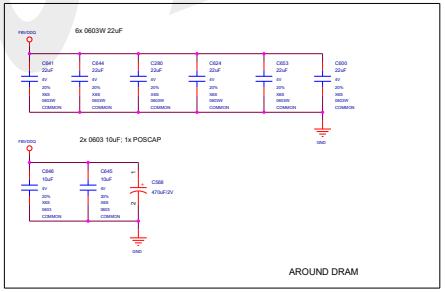
MAY
ALL
STANDARDS.

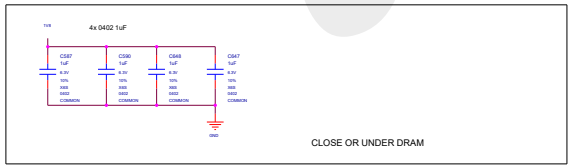
[redacted]

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	11 OF 54
DATE	27-JUN-2020





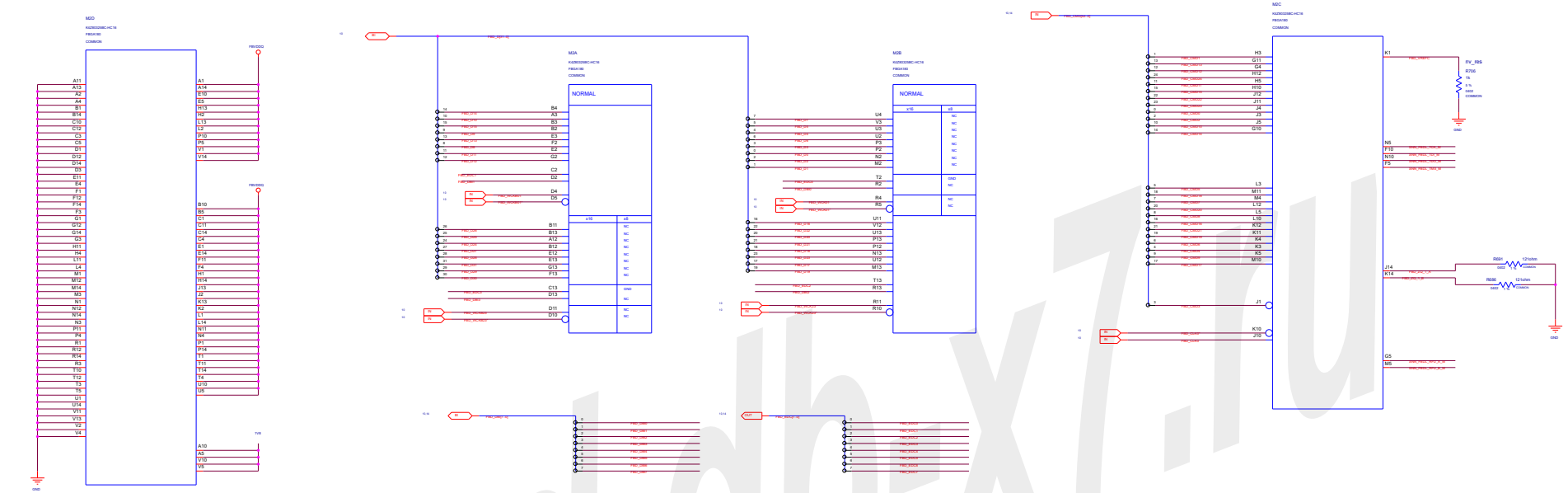


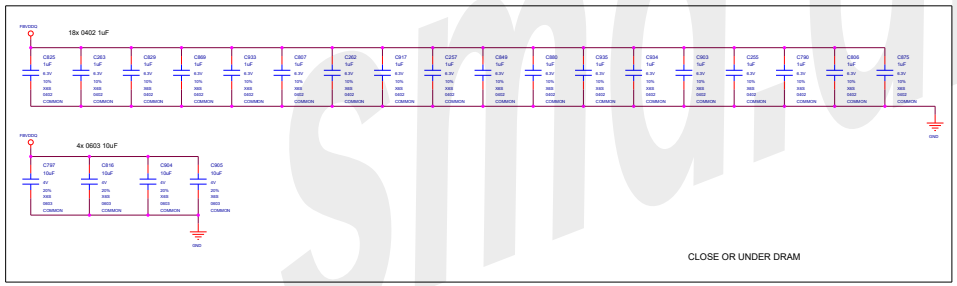


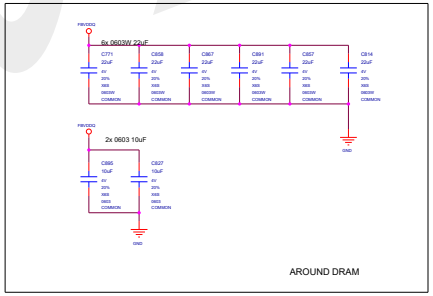
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBC[63:32]

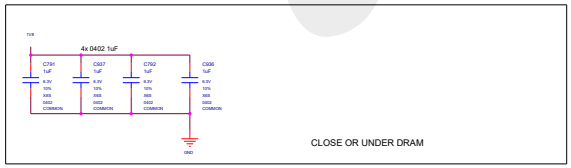
NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	12 OF 54
DATE	27-JUN-2020

MAY
ALL
STANDARDS.





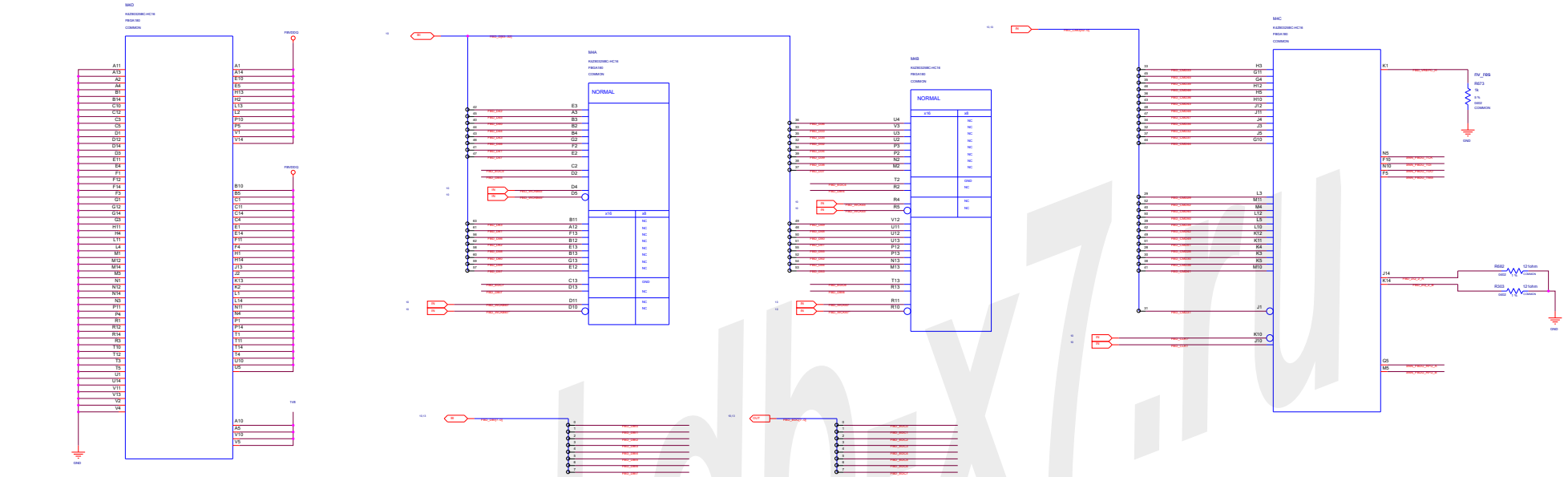


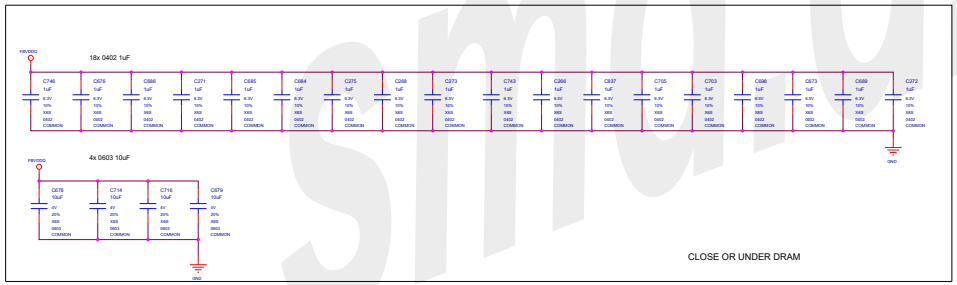


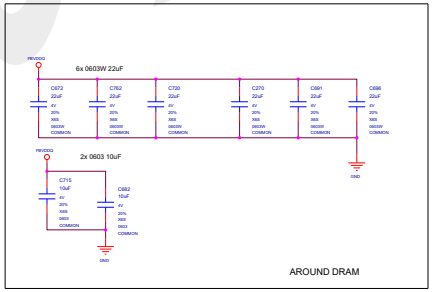
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBD[31:0]

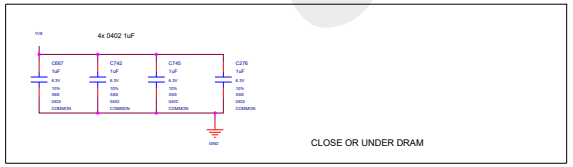
MAY
ALL
STANDARDS

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	13 OF 54
BOM REV	A	DATE	27-JUN-2020







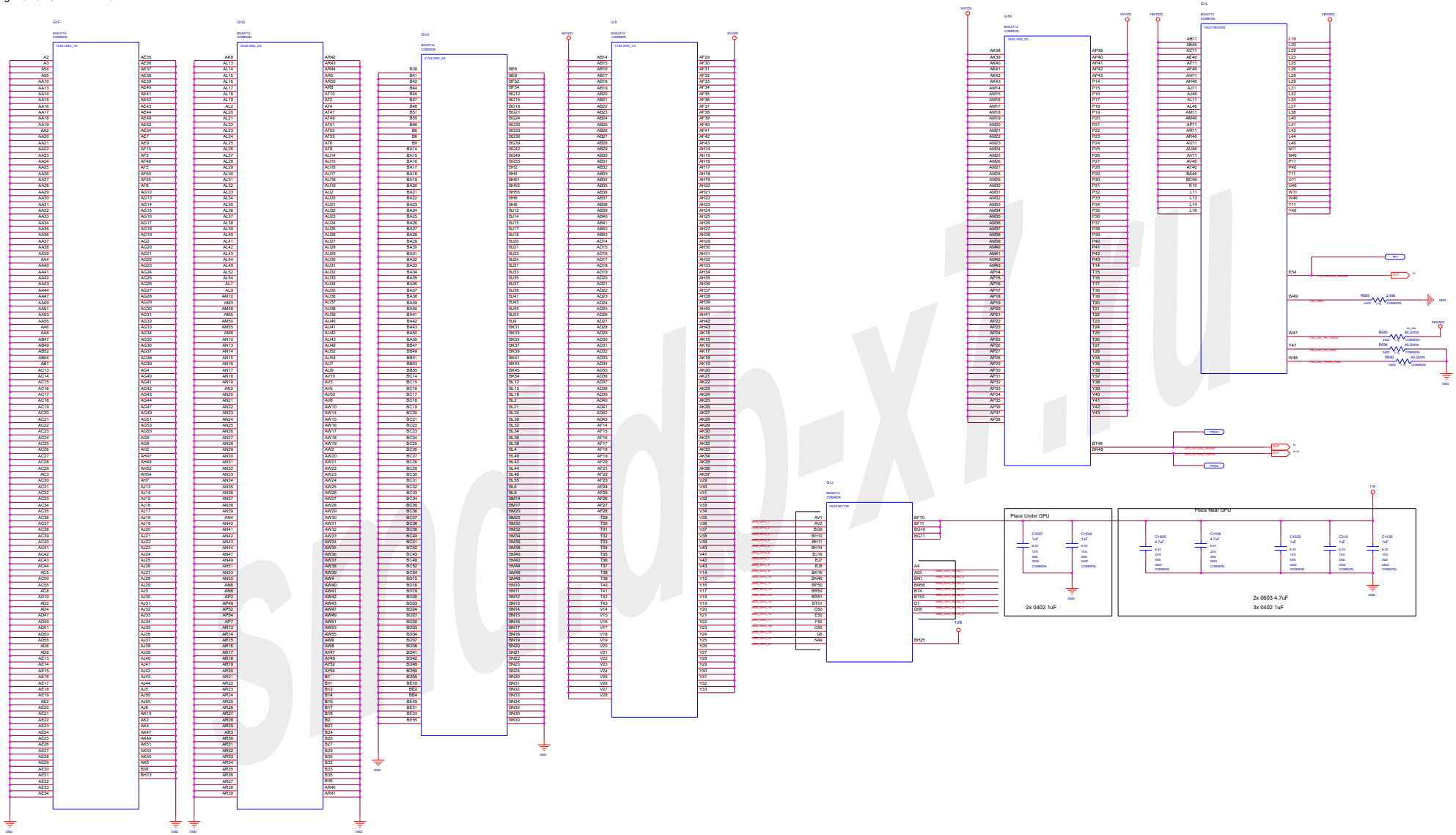


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MEMORY: FBD[63:32]

MAY ALL STANDARDS

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	14 OF 54
BOM REV	A	DATE	27-JUN-2020

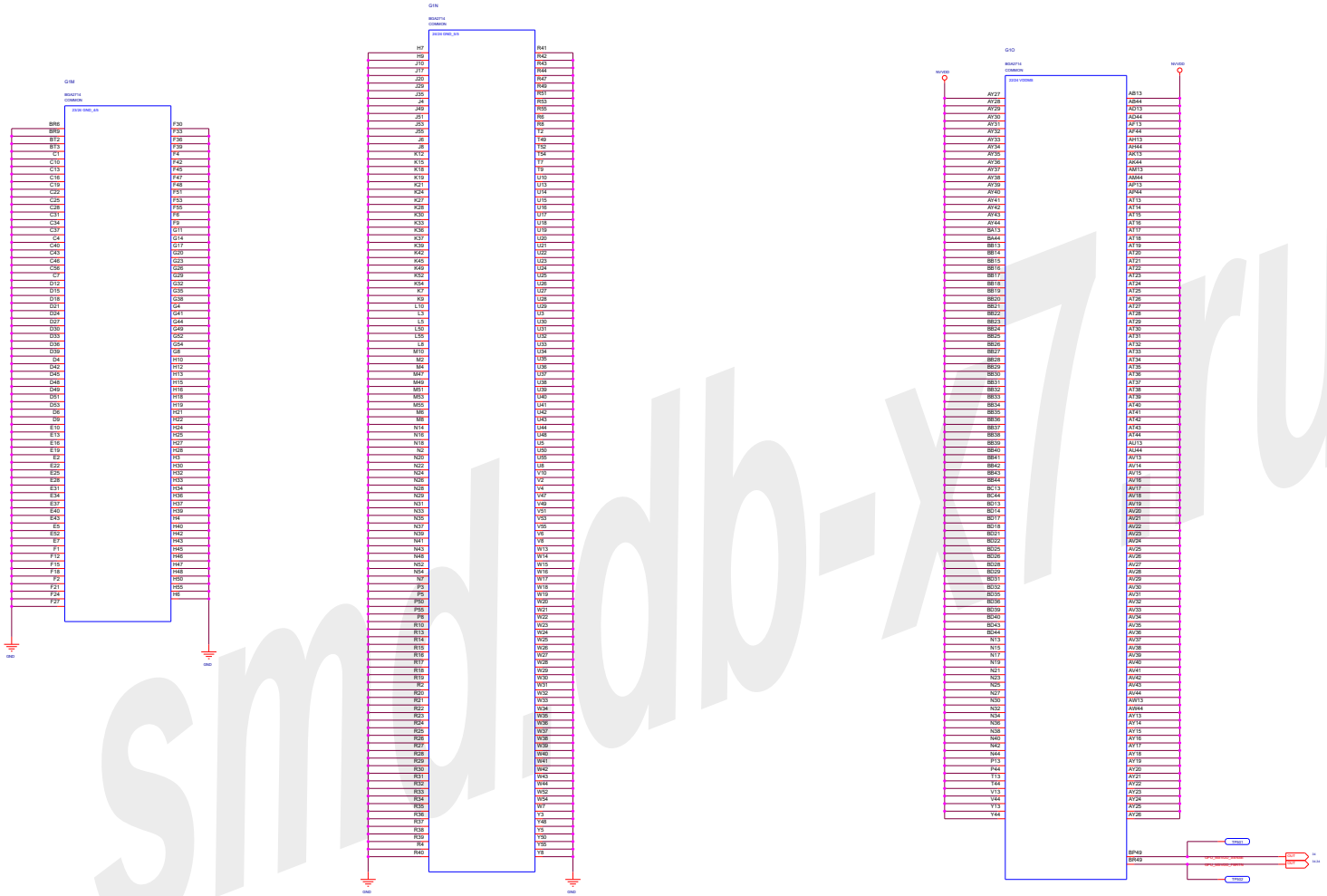
Page15: GPU PWR and GND



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR & GND

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	15 OF 54
DATE	27-JUN-2020

MAY
ALL
STANDARDS.



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR & GND 2

MAY
ALL
STANDARDS.

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	16 OF 54
BOM REV	A	DATE	27-JUN-2020

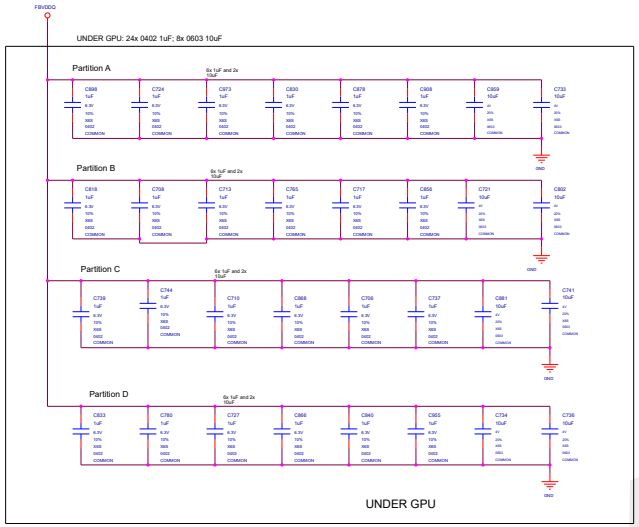
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU PWR & GND 3 (XVDD)

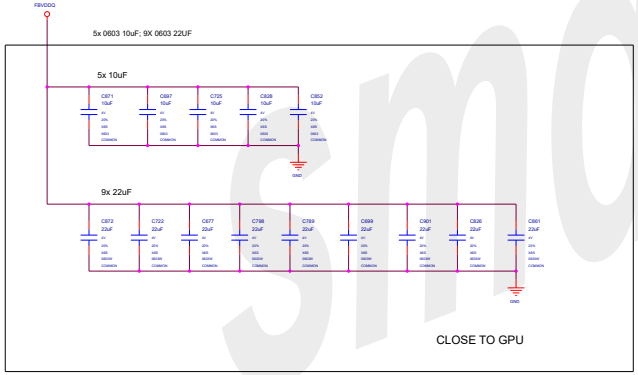
MAY
ALL
STANDARDS.

[redacted]

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	17 OF 54
BOM REV	A	DATE	27-JUN-2020

FBVDDQ



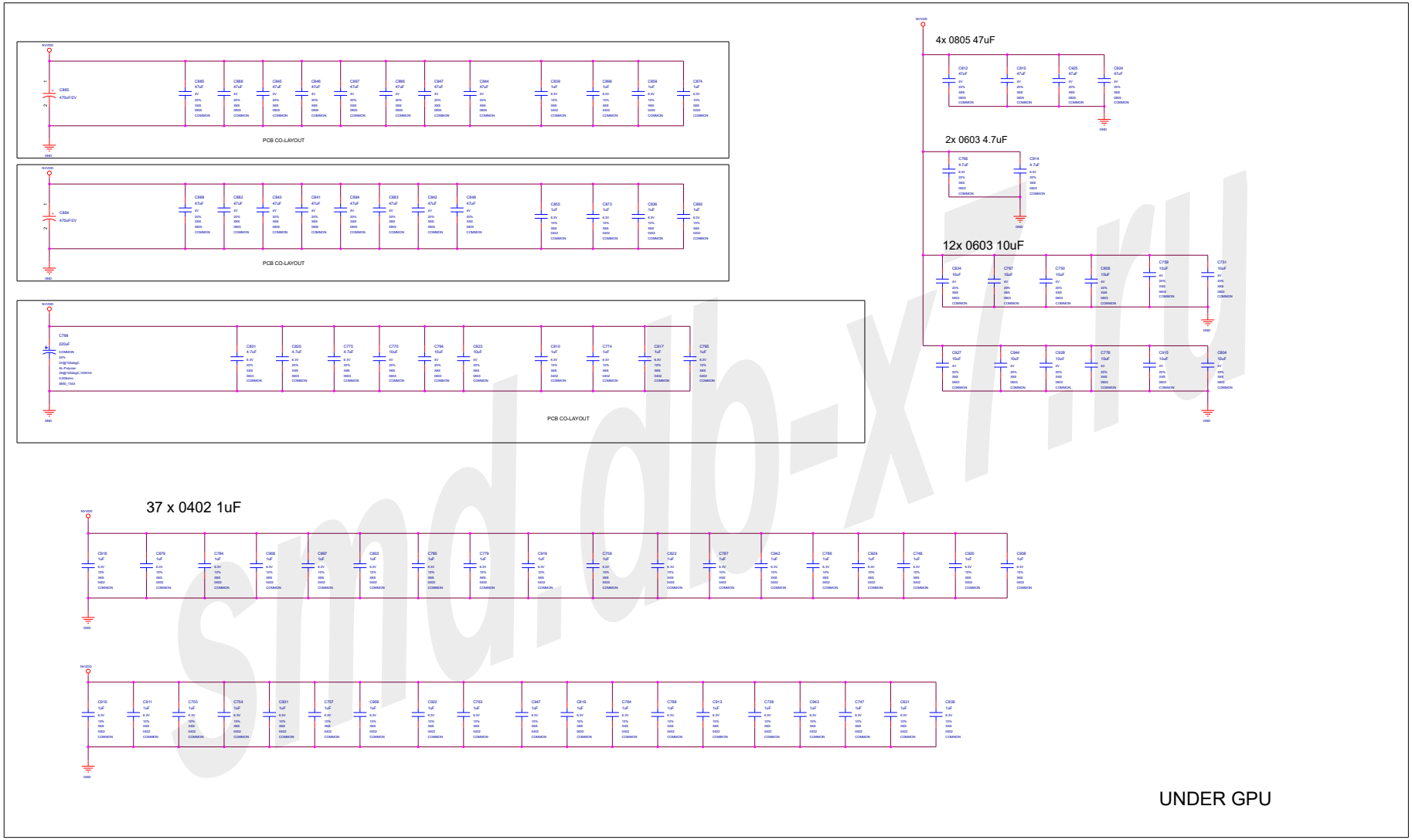


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING FBVDDQ

MAY
ALL
STANDARDS.

[redacted]

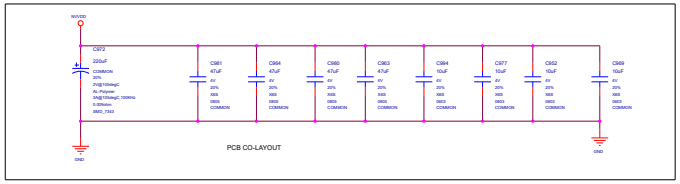
NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	18 OF 54
BOM REV	A	DATE	27-JUN-2020

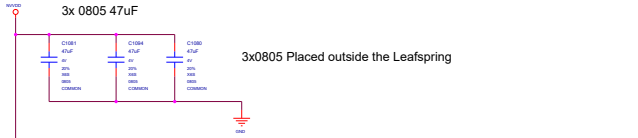


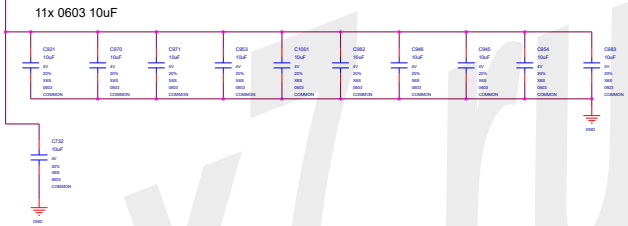
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING NVVDD

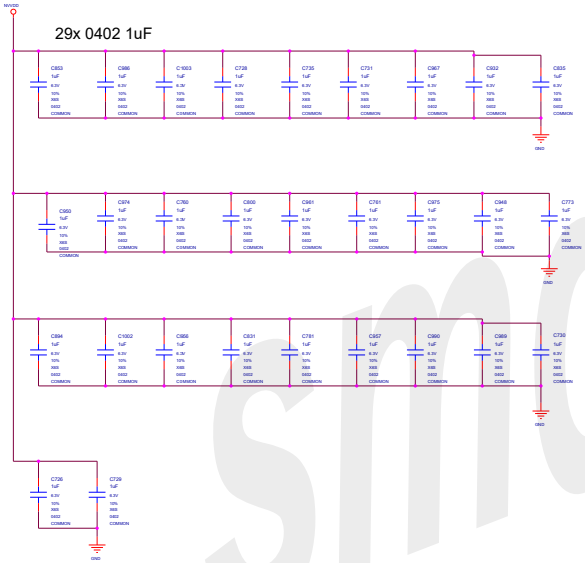
NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	19 OF 54
DATE	27-JUN-2020

MAY
ALL
STANDARDS.









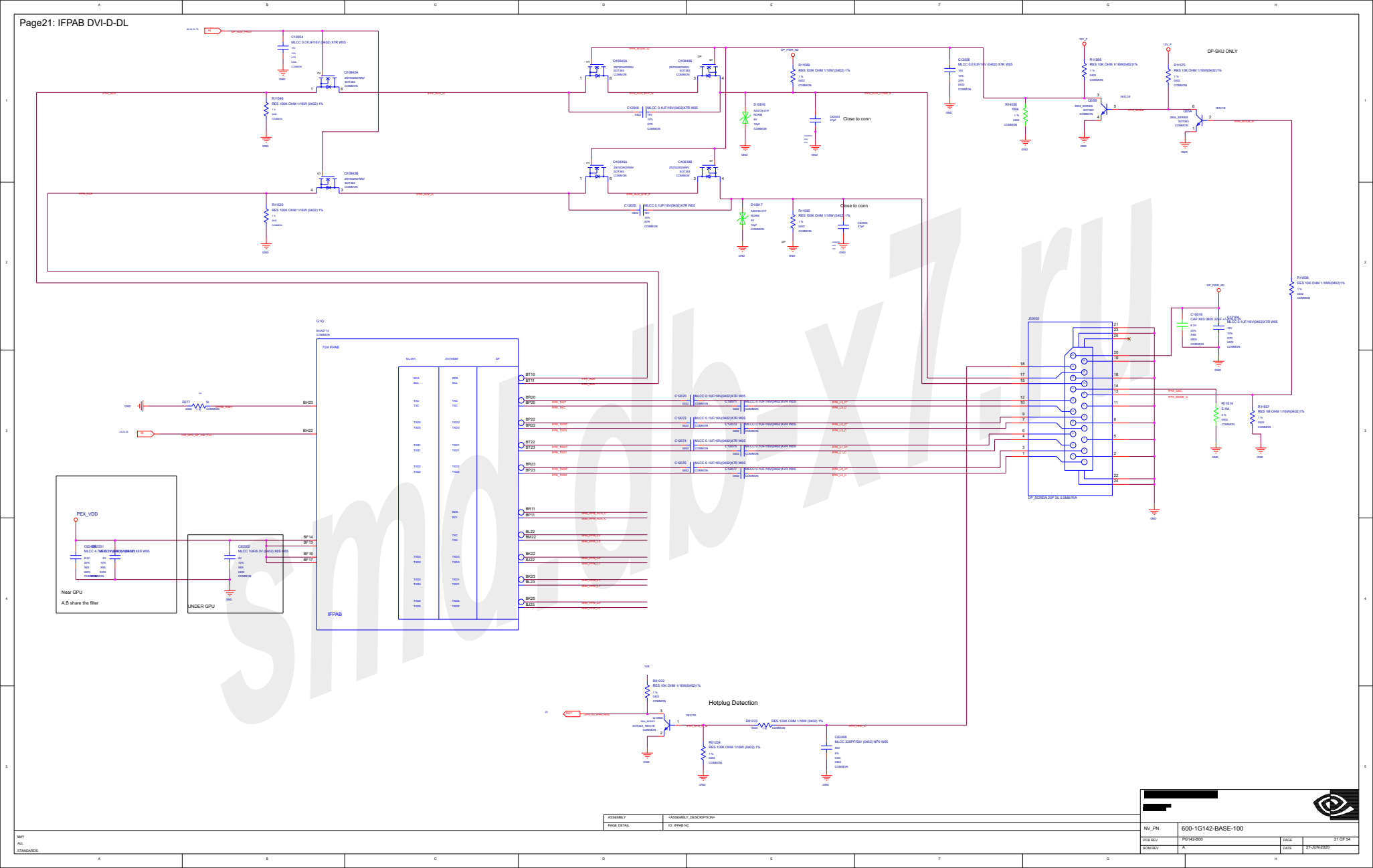
UNDER GPU

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING NVVDD

MAY
ALL
STANDARDS

[redacted]

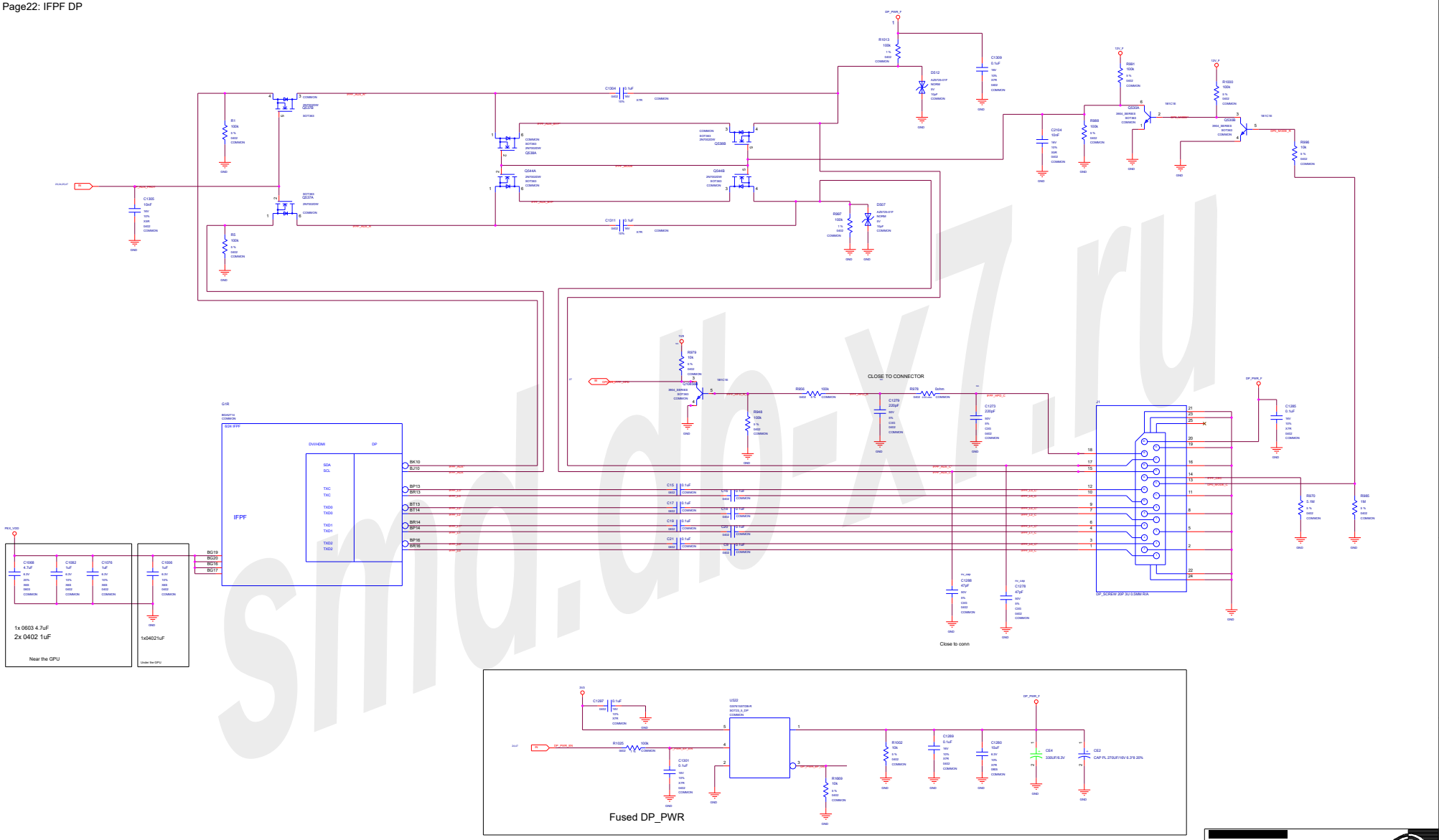
NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	20 OF 54
BOM REV	A	DATE	27-JUN-2020



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPAB NC

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
PAGE	21 OF 54
BOM REV	A
DATE	27-JUN-2020

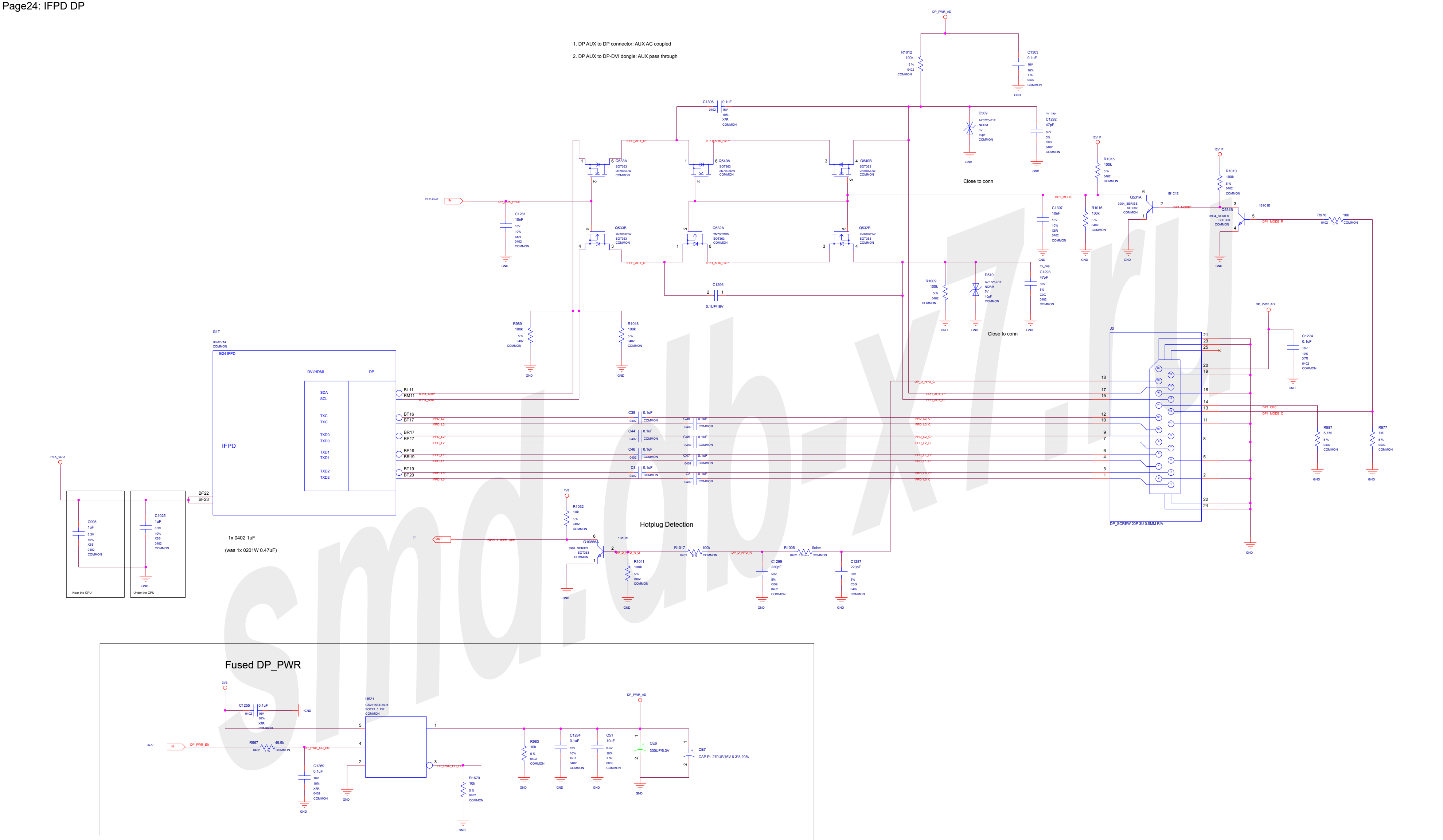
MAY
ALL
STANDARDS.



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPF DP

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	22 OF 54
DATE	27-JUN-2020

Page24: IFPD DP



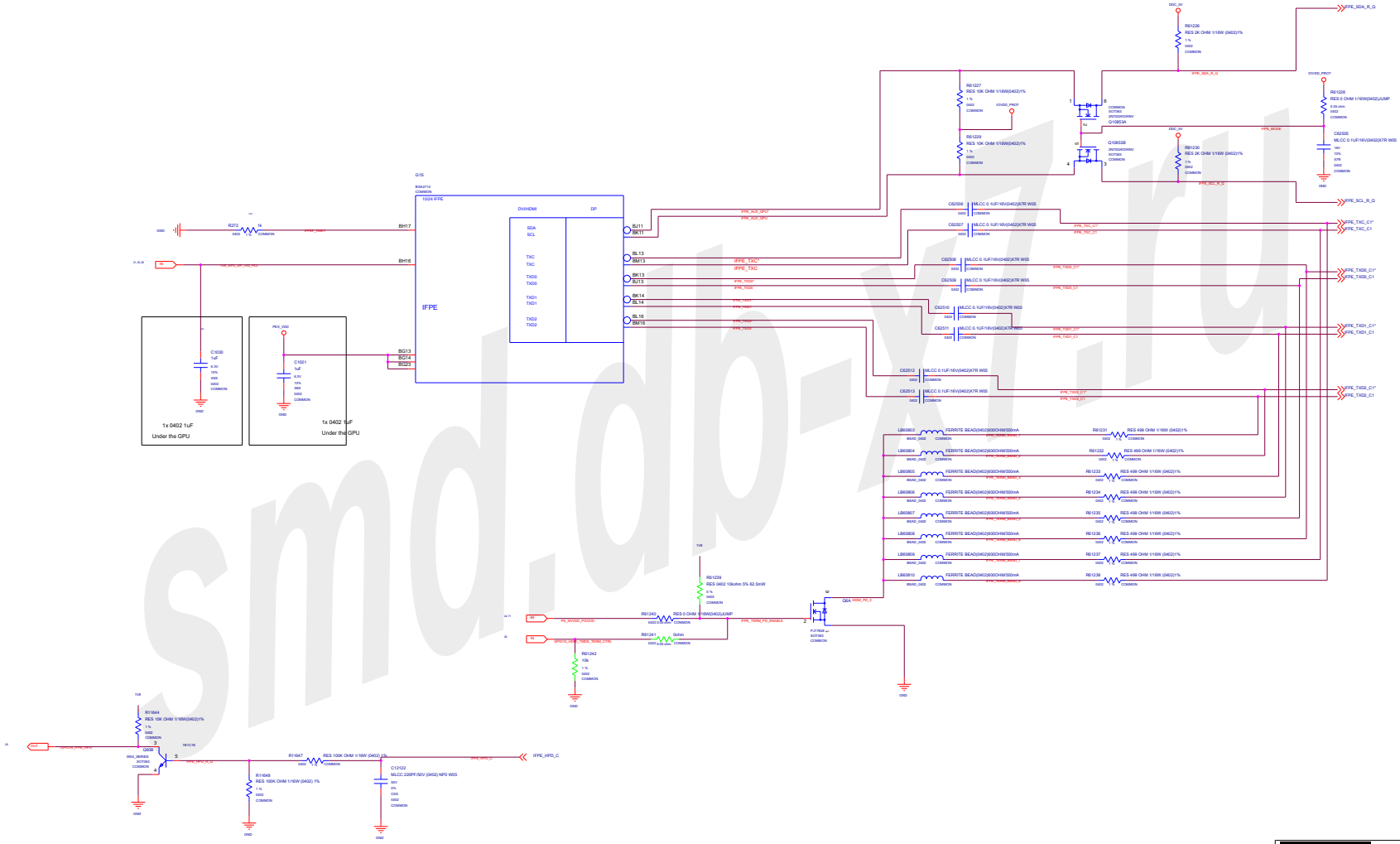
[redacted]		
ASSEMBLY	<ASSEMBLY_DESCRIPTION>	
PAGE DETAIL		
NV_PN	600-1G142-BASE-100	
PCB REV	PG142-B00	PAGE 24 OF 54
BOM REV	A	DATE

MAY
ALL
STANDARDS.

IO: IFPD DP

27-JUN-2020

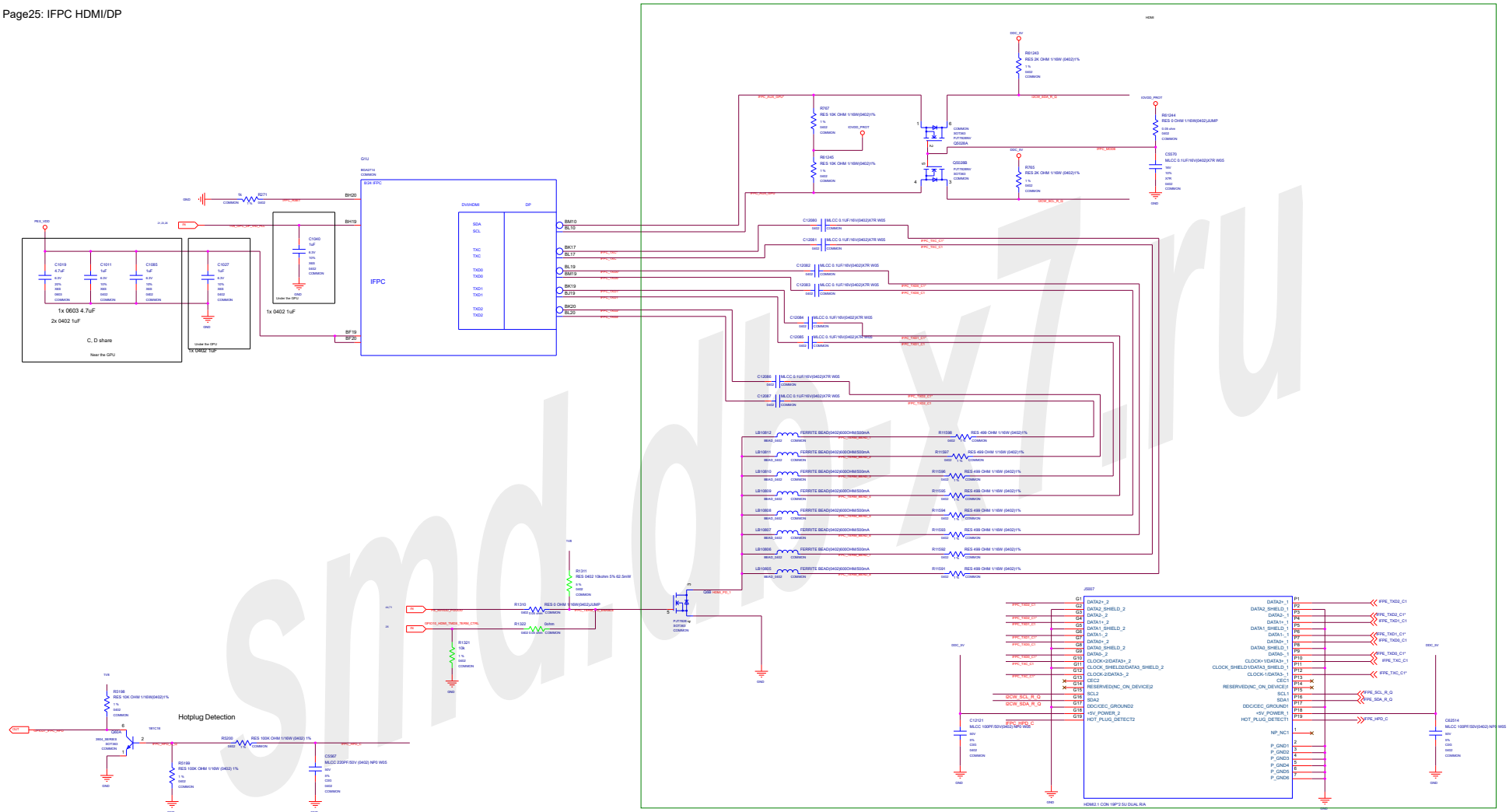
IFPE UPPER HDMI



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPE DP

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	23 OF 54
DATE	27-JUN-2020

Page25: IFPC HDMI/DP



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IO: IFPC HDMI/DP

MAY
ALL
STANDARDS.

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	25 OF 54
BOM REV	A	DATE	27-JUN-2020

Page26: MISC2: ROM, XTAL, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG SAMSUNG 8Gb 7GHz
L	L	H	00001	RAMCFG MICRON 8Gb 7GHz
L	H	L	00010	RAMCFG HYNIX 8Gb 7GHz
H	H	L	00110	RAMCFG SAMSUNG 16Gb 8GHz
		TBD		

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
H	H	M	0000	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0

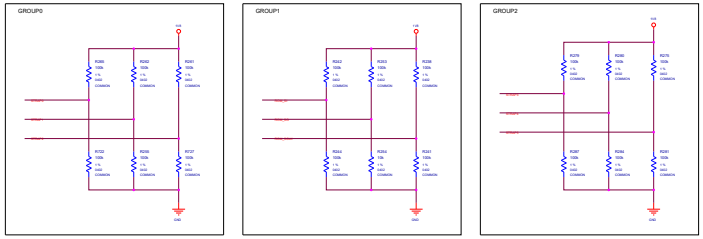
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

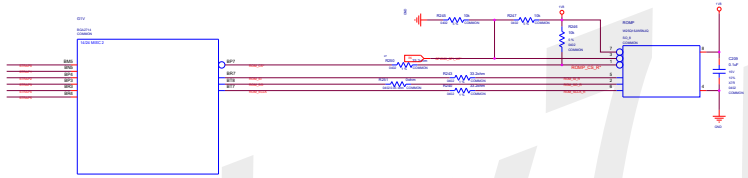
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

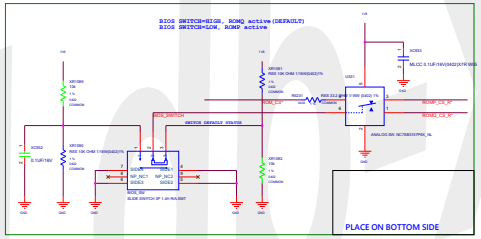
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

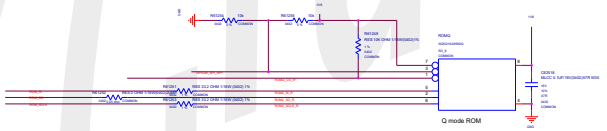
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

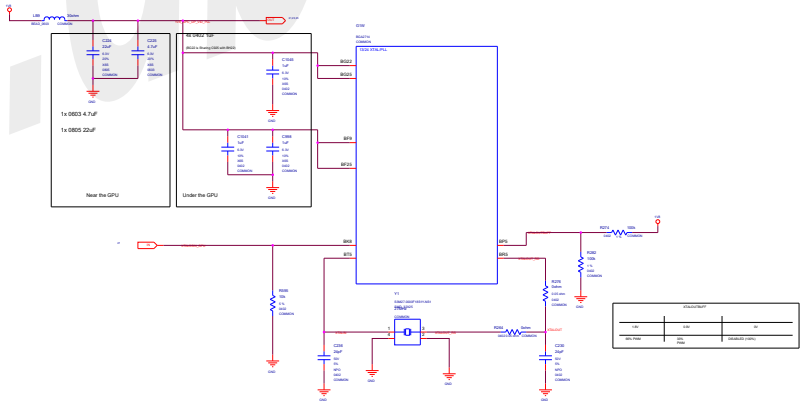
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE



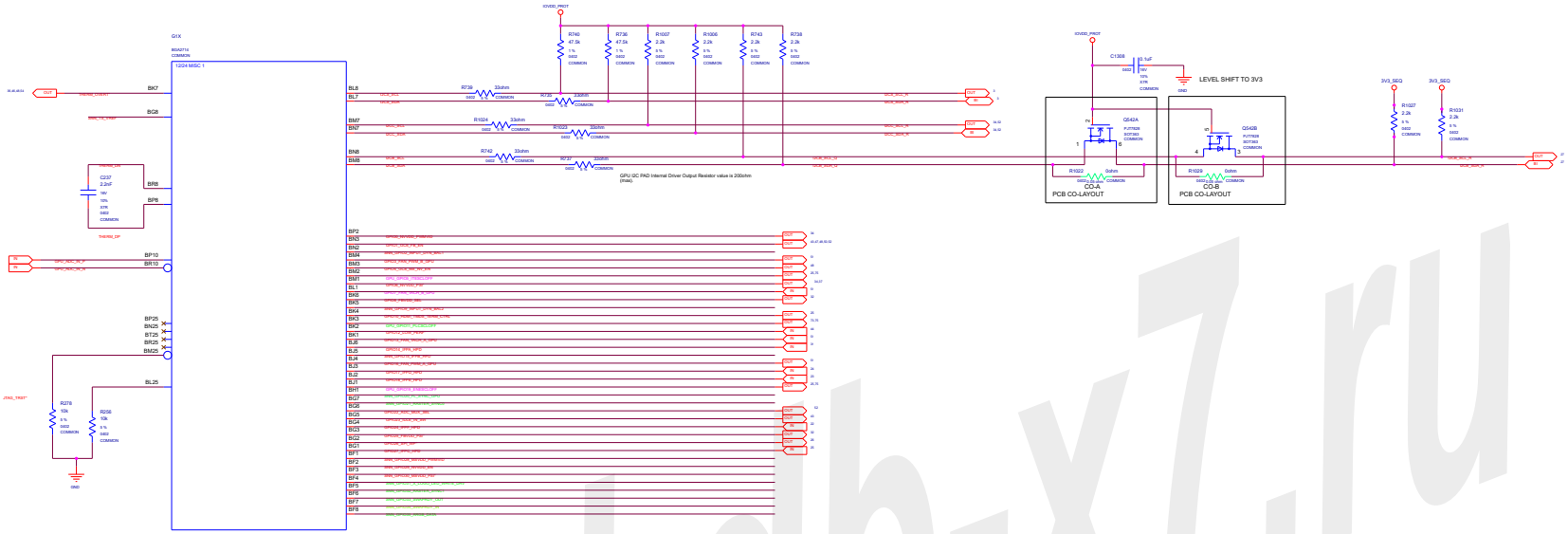








Page27: MISC1: JTAG, GPIO, ADC, I2C, OVERT



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC2: JTAG,GPIO,ADC,I2C,FL,STEERO

MAY
ALL
STANDARDS.

[redacted]

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	27 OF 54
BOM REV	A	DATE	27-JUN-2020

Page28: RGB

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MISC3: RGB

[redacted]

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	28 OF 54
BOM REV	A	DATE	27-JUN-2020

BLANK PAGE

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	BLANK PAGE

[redacted]

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	35 OF 54
BOM REV	A	DATE	27-JUN-2020

Page42: Input Power Balancing Switcher

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: OVRS_INPUT POWER BALANCE

[redacted]

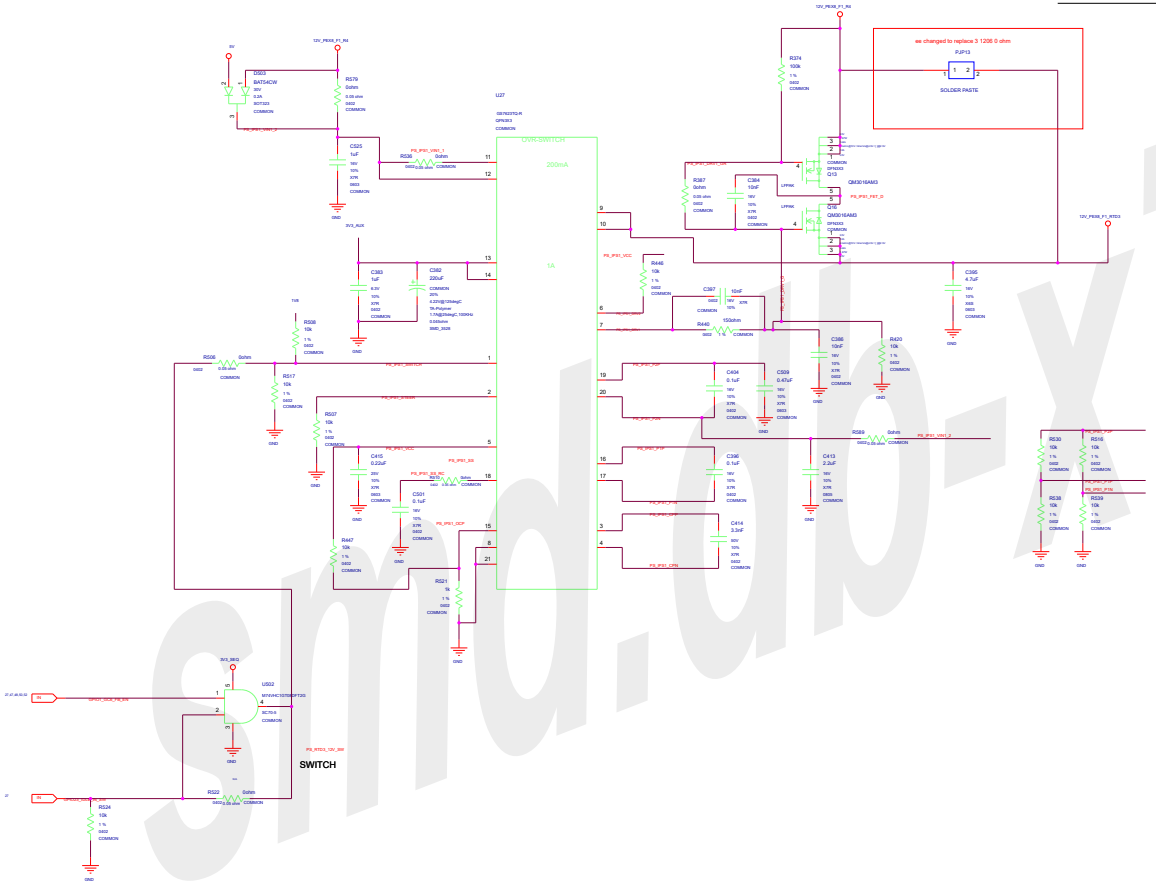
NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	42 OF 54
BOM REV	A	DATE	27-JUN-2020

Page43: INPUT SWITCH RTD3 (12V & 3V3_A SWITCHER)

AND GATE LOGIC

GPIO1	GPIO29	SWITCH	VOUT
0	0	0	12V
0	1	0	12V
1	0	0	12V
1	1	1	3V3A

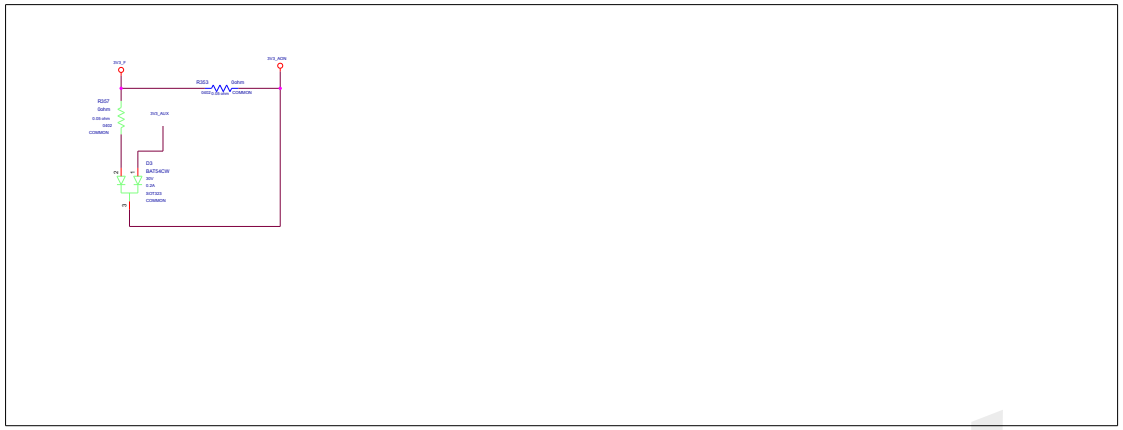
SWITCH	VOUT
0	VOUT = VIN1
1	VOUT = VIN2

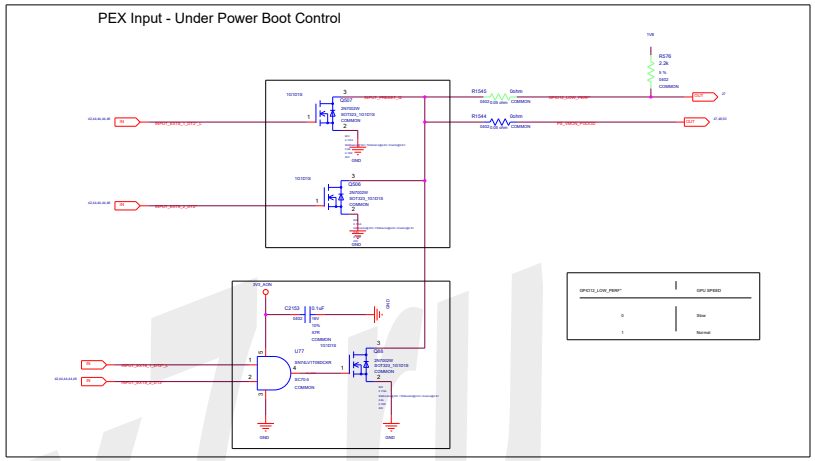


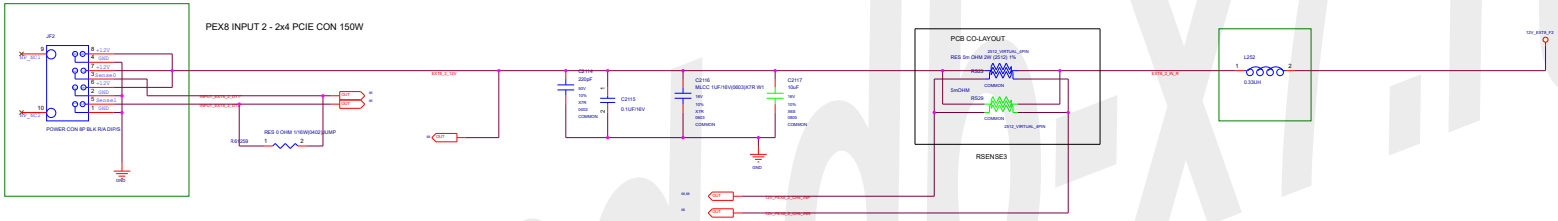
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: RDT3_12V & 3V3_A Switcher

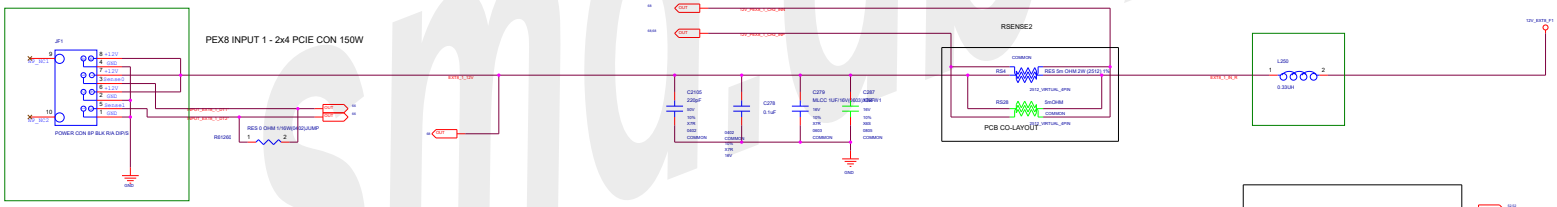
NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	43 OF 54
BOM REV	A	DATE	27-JUN-2020

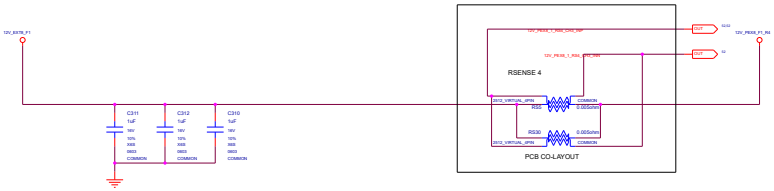
Page44: 12V_EXT_INPUT, FILTERING & UNDER POWER BOOT











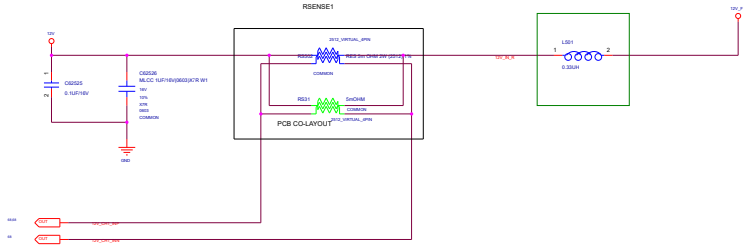
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: INPUTS, FILTERING and MONITORING

[redacted]

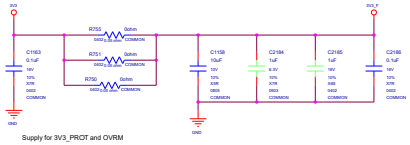
NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	44 OF 54
BOM REV	A	DATE	27-JUN-2020

Page45: PEX_INPUT & FILTERING, PEX_3V3, 3V3_AUX

PEX_12V INPUT - 66W

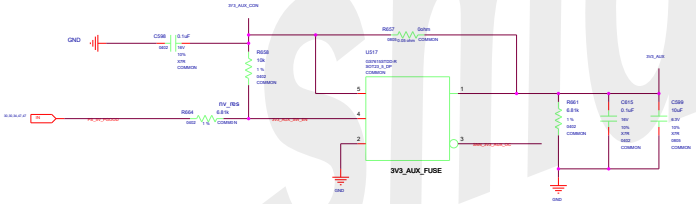


PEX 3V3 INPUT - 10W



Supply for 3V3_PROT and OVRM

3V3_AUX



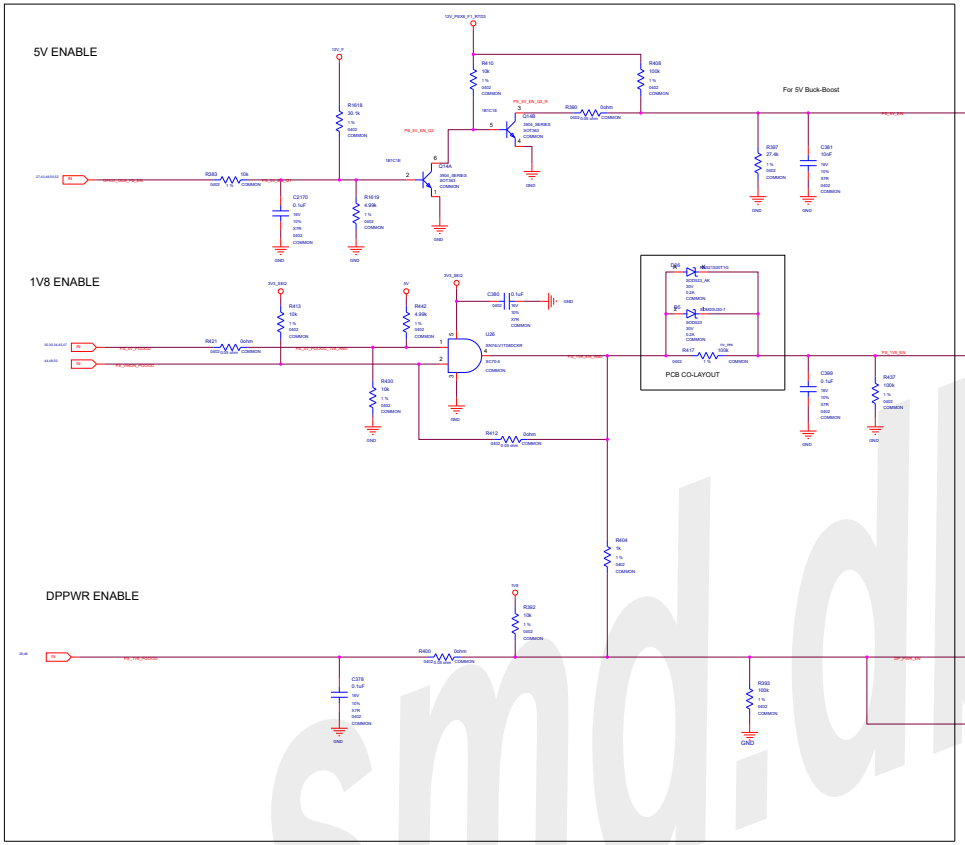
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PEX_12V, PEX_3V3 AND A3V3_AUX

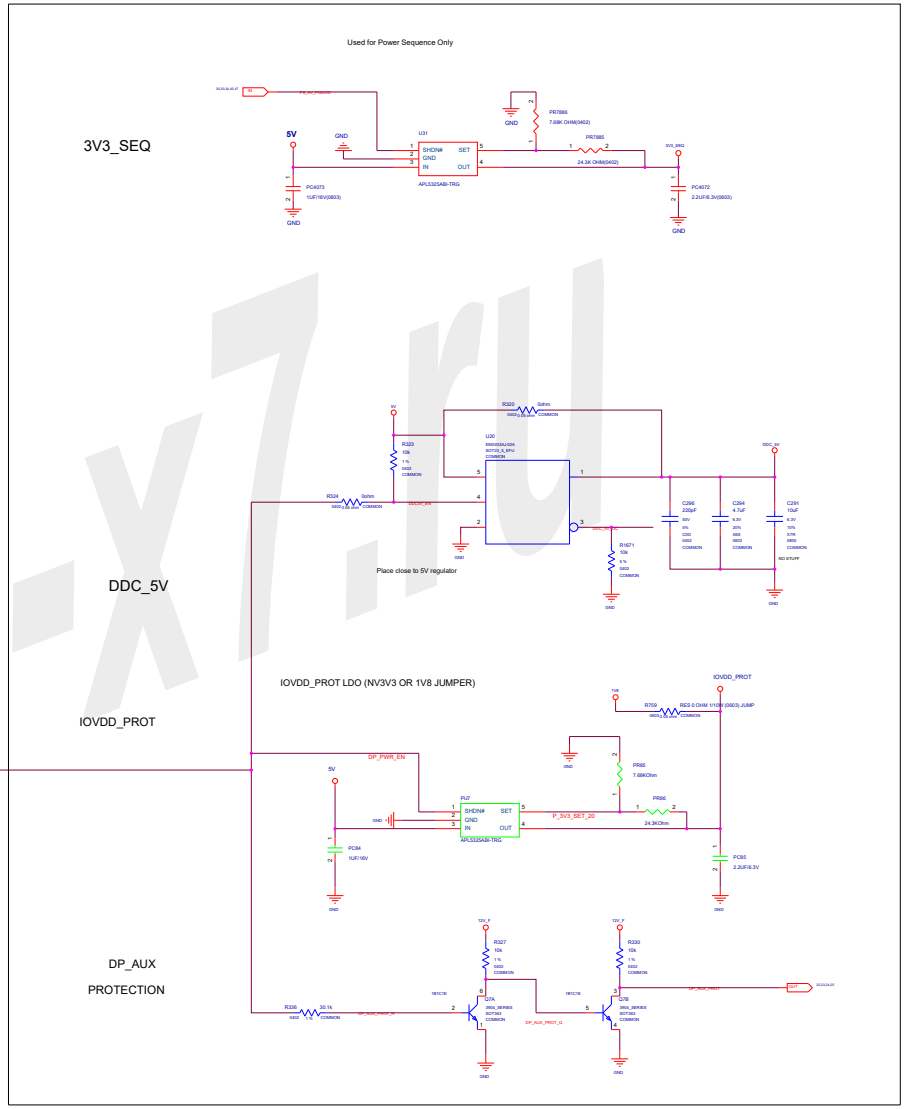
NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	45 OF 54
DATE	27-JUN-2020

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: STEERING, UPR, HOT UNPLUG

[redacted]

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	46 OF 54
BOM REV	A	DATE	27-JUN-2020



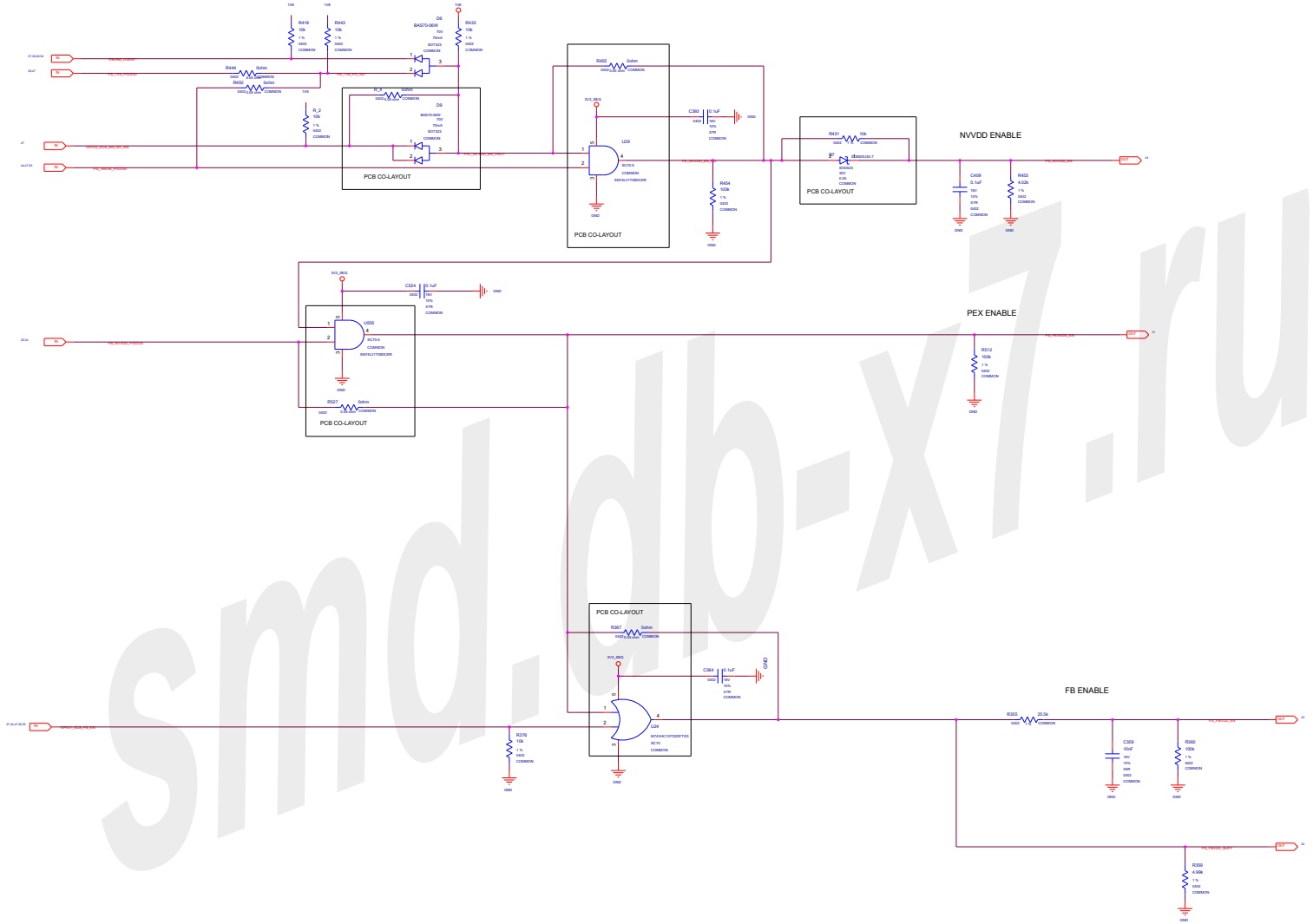


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: 5V, 1V8, 3V3_SEQ

[redacted]

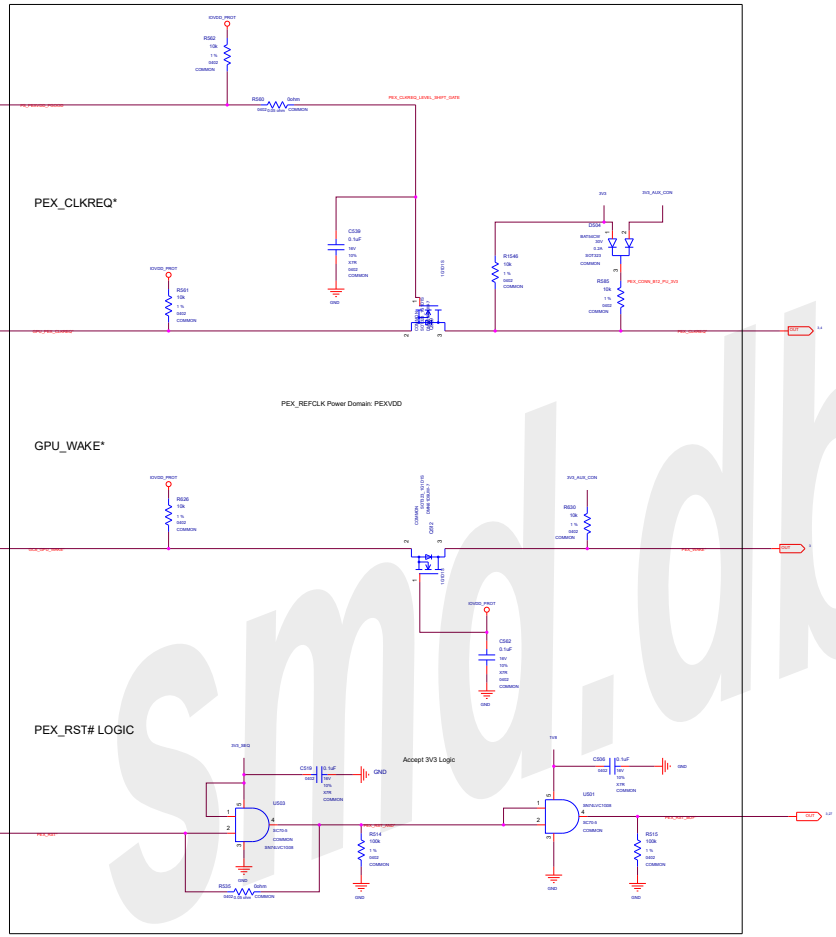
NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	47 OF 54
BOM REV	A	DATE	27-JUN-2020

Page48: SEQ:NVVDD, PEX, FBVDDQ ENABLE



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: NVVDD, PEX, FBVDDQ ENABLE

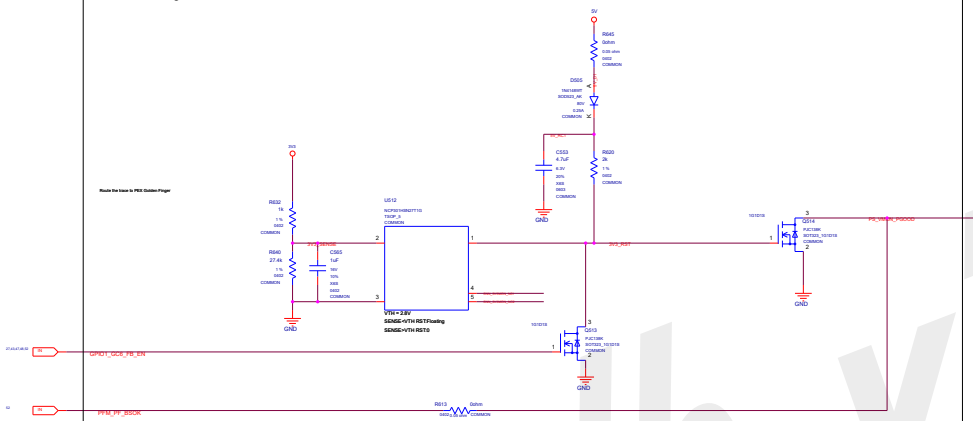
NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	48 OF 54
DATE	27-JUN-2020



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: MISC

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	49 OF 54
DATE	27-JUN-2020

3V3PEX Voltage Monitor

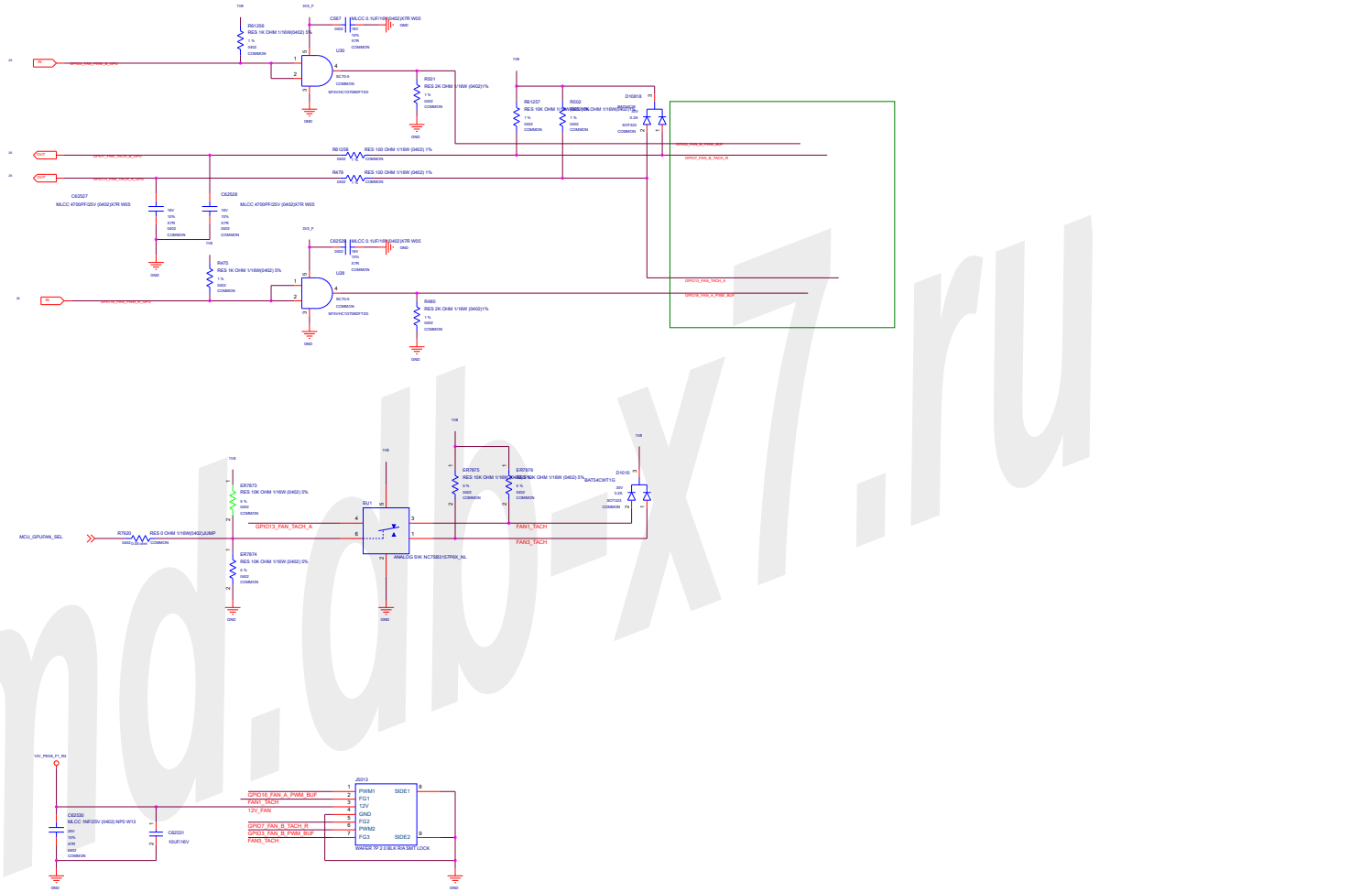


BOM Configuration

OPTIONS	PEX3V3_SENSE	PEX12V_SENSE	OTHER_12V_SENSE
Use Pre-Filter	**Pre-Filter**	**Pre-Filter**	**Pre-Filter**
NO Pre-Filter	Voltage_Monitor	Voltage_Monitor	N/A

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIE golden finger
12V	INPUT	Sense the 12V Voltage from PCIE golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach Vth
GC6_FB_EN	INPUT	Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD
PS_PF_SKIP	INPUT	From INA3221(VPU) or Pre-filter(SKIP)
PS_PF_BSOK	INPUT	From INA3221(PV) or Pre-filter(BS_OK)

Page51: FAN&LED



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	FAN & LED

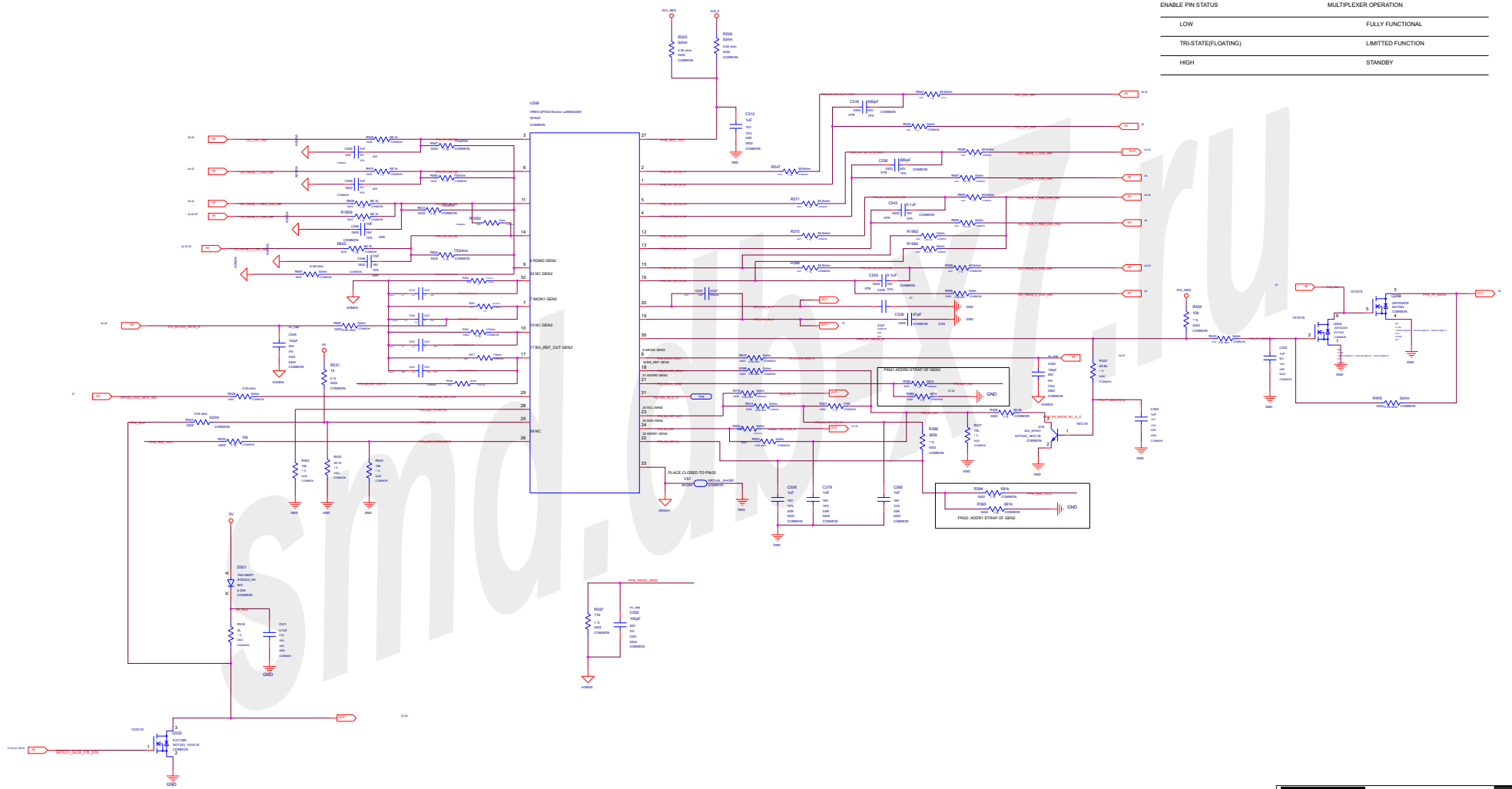
MAY
ALL
STANDARDS.

NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	51 OF 54
BOM REV	A	DATE	27-JUN-2020

Page52: OVRM_PWR SENSE

MODE PIN STATUS	MULTIPLEXER OPERATION
LOW	DEVICE A
TRI-STATE(FLOATING)	STAND-ALONE
HIGH	DEVICE B

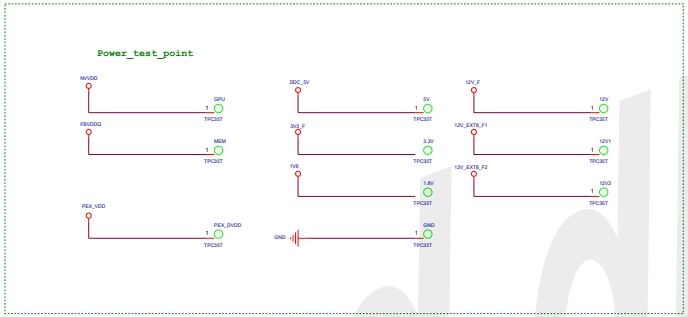
ENABLE PIN STATUS	MULTIPLEXER OPERATION
LOW	FULLY FUNCTIONAL
TRI-STATE(FLOATING)	LIMITTED FUNCTION
HIGH	STANDBY

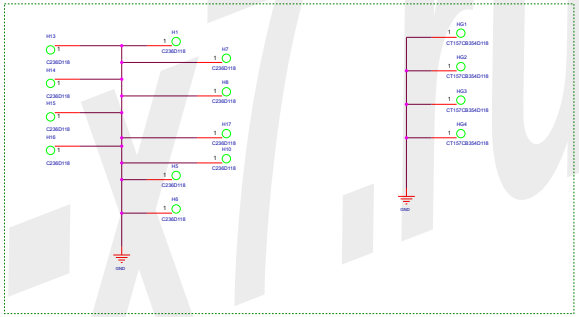


ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS:OVRM_PWR_SENSE

NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	52 OF 54
DATE	27-JUN-2020

Page53: MECH





ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MECH

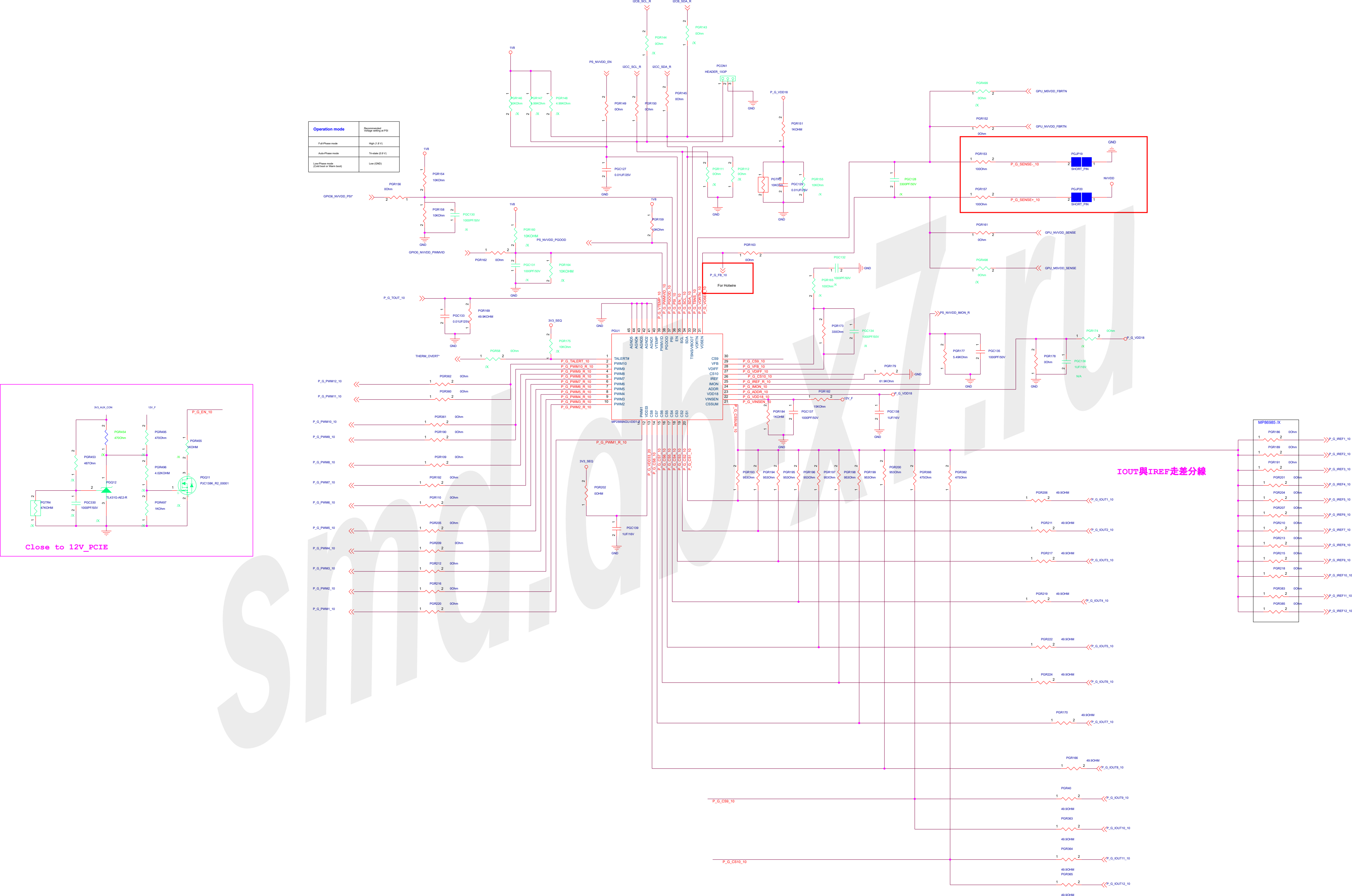
NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	53 OF 54
BOM REV	A	DATE	27-JUN-2020

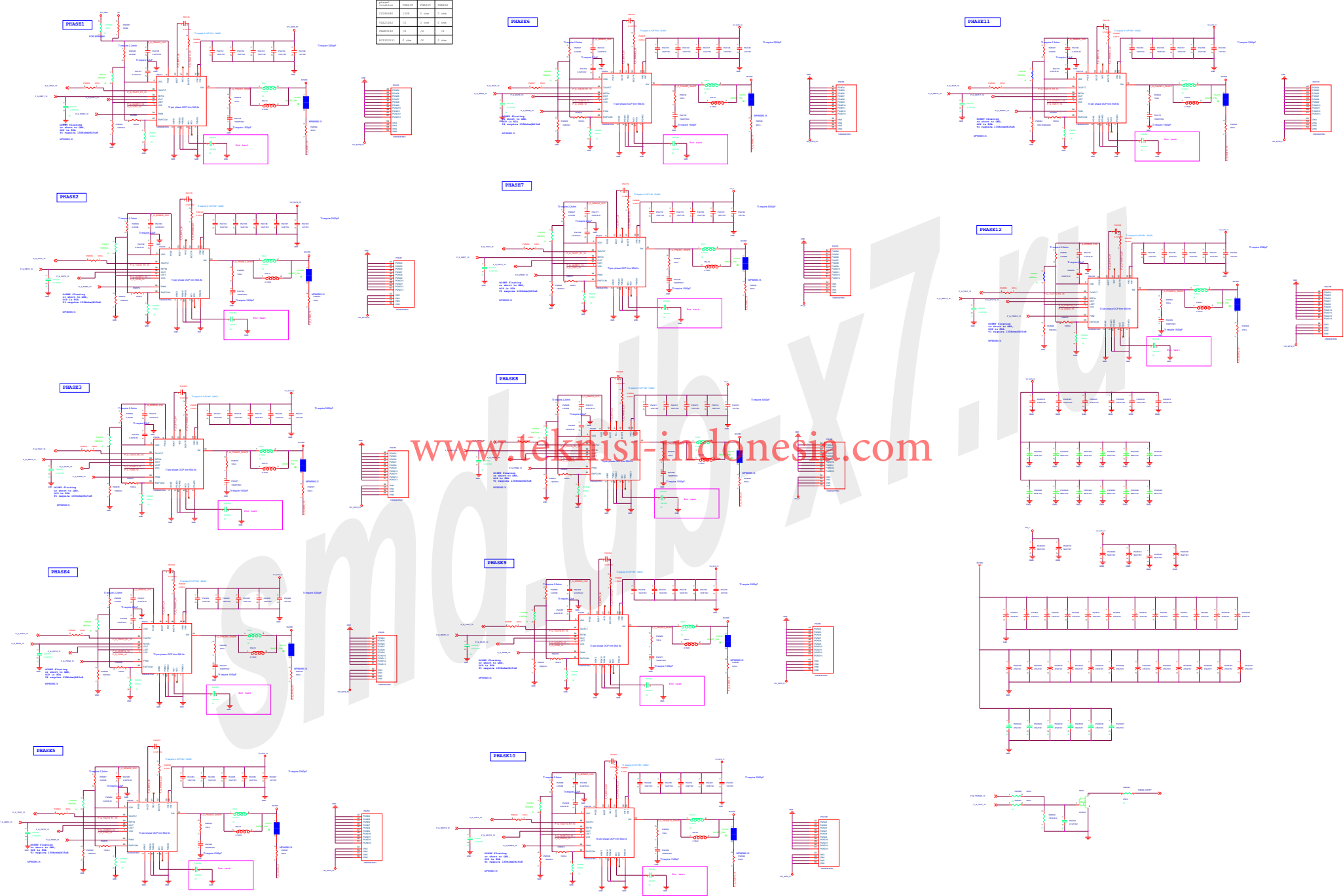
ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PTC

[redacted]

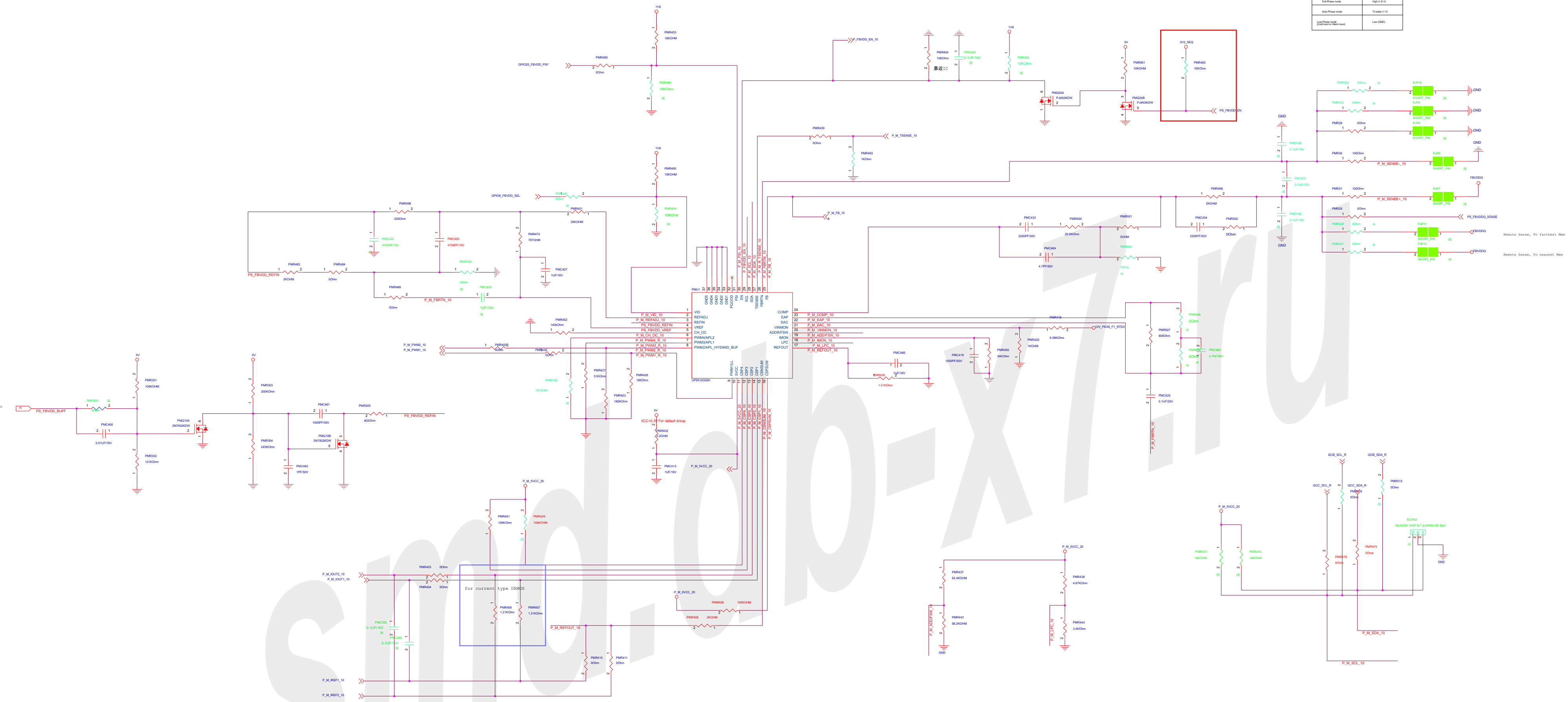
NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	54 OF 54
BOM REV	A	DATE	27-JUN-2020

Operation mode	Recommended Voltage setting at PSI
Full-Phase mode	High (1.8 V)
Auto-Phase mode	Tri-state (0.9 V)
Low-Phase mode (Cold boot or Warm boot)	Low (GND)

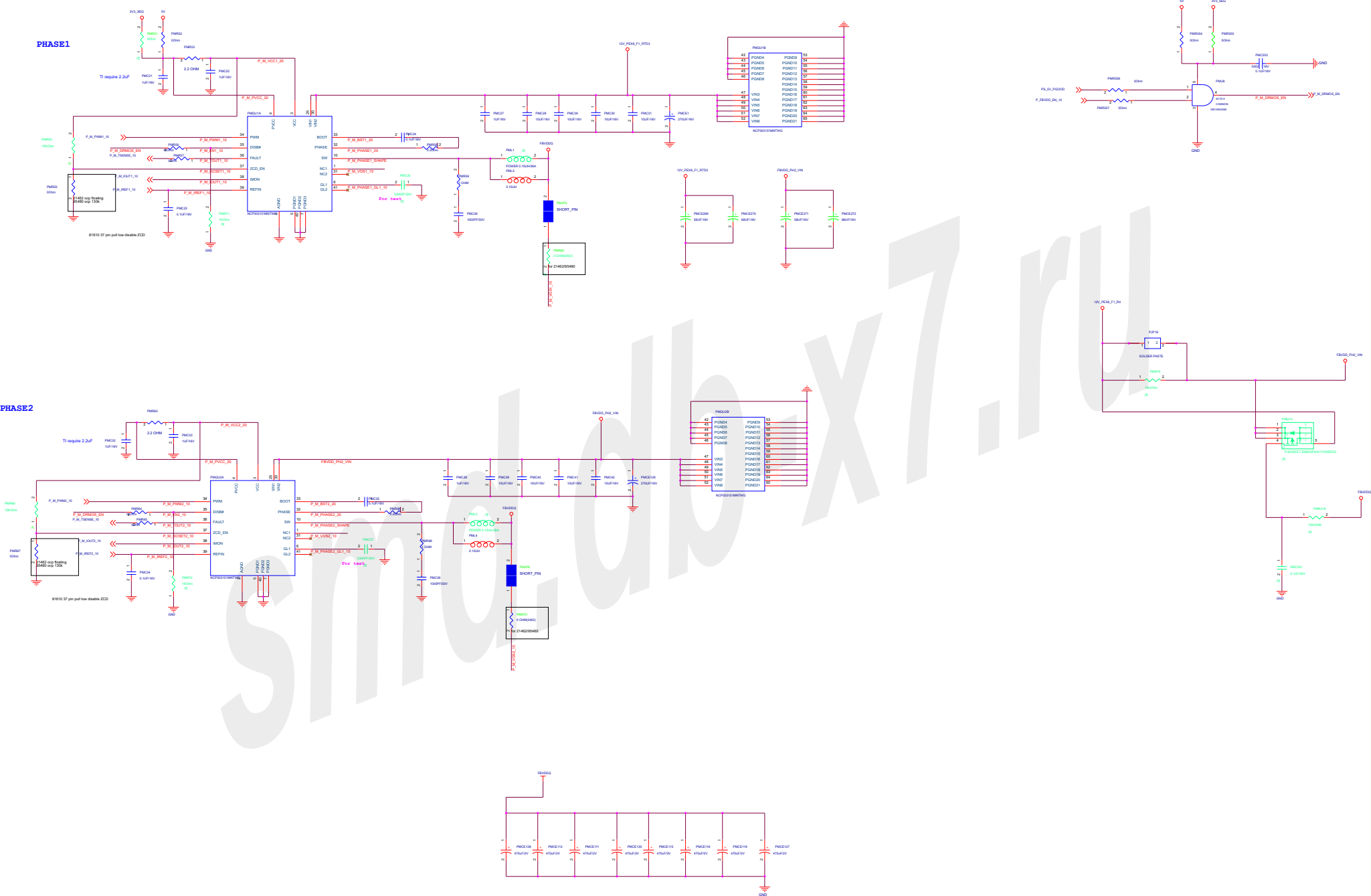


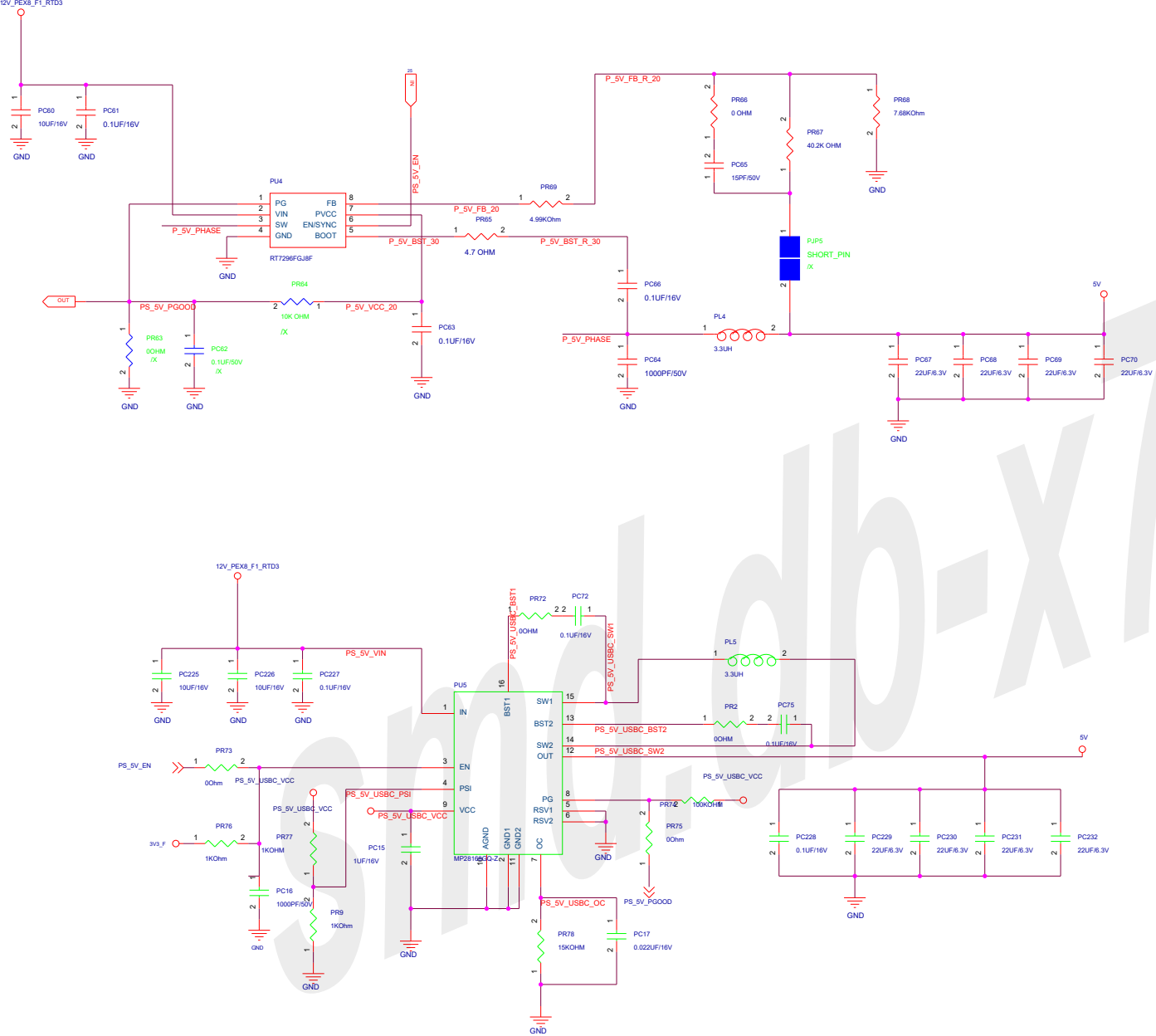


Operation mode	Recommended Voltage setting at PSI
Full-Phase mode	High (1.8 V)
Auto-Phase mode	Tri-state (1 V)
Low-Phase mode (Cold boot or Warm boot)	Low (GND)

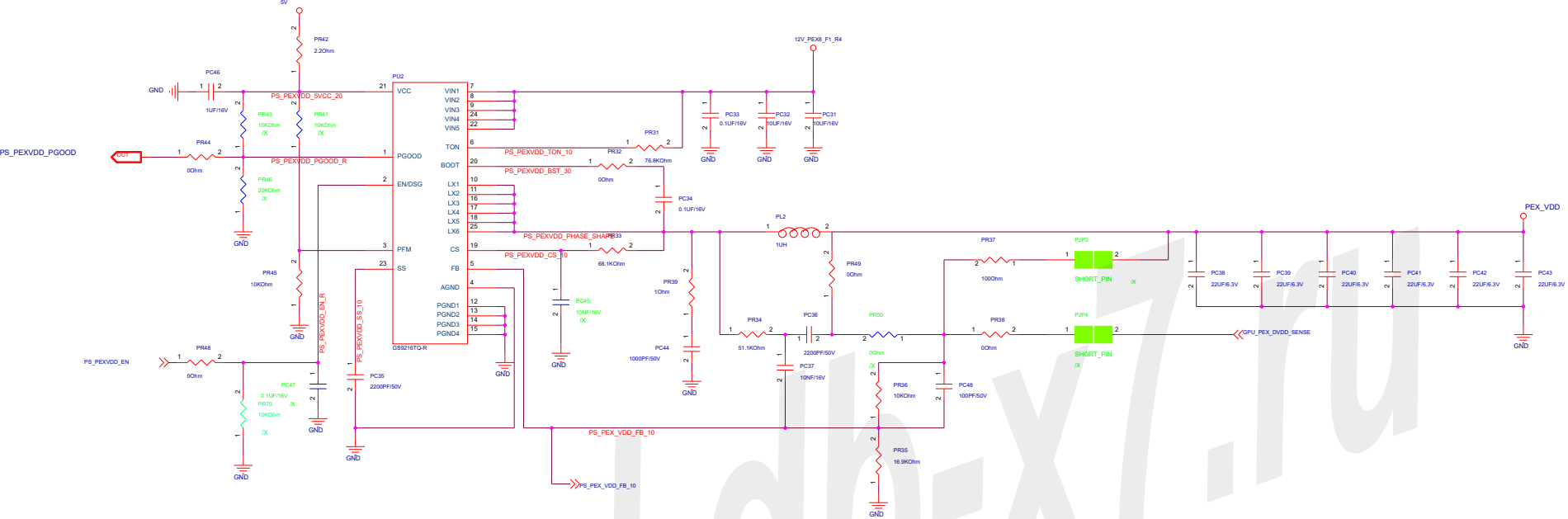


		Title :	NVVDD Controller
<OrgName>		Engineer:	James Huang
Size: D	Project Name: CG166PI		Rev: 1.00
Date: Monday, July 27, 2020		Sheet 28	of 39

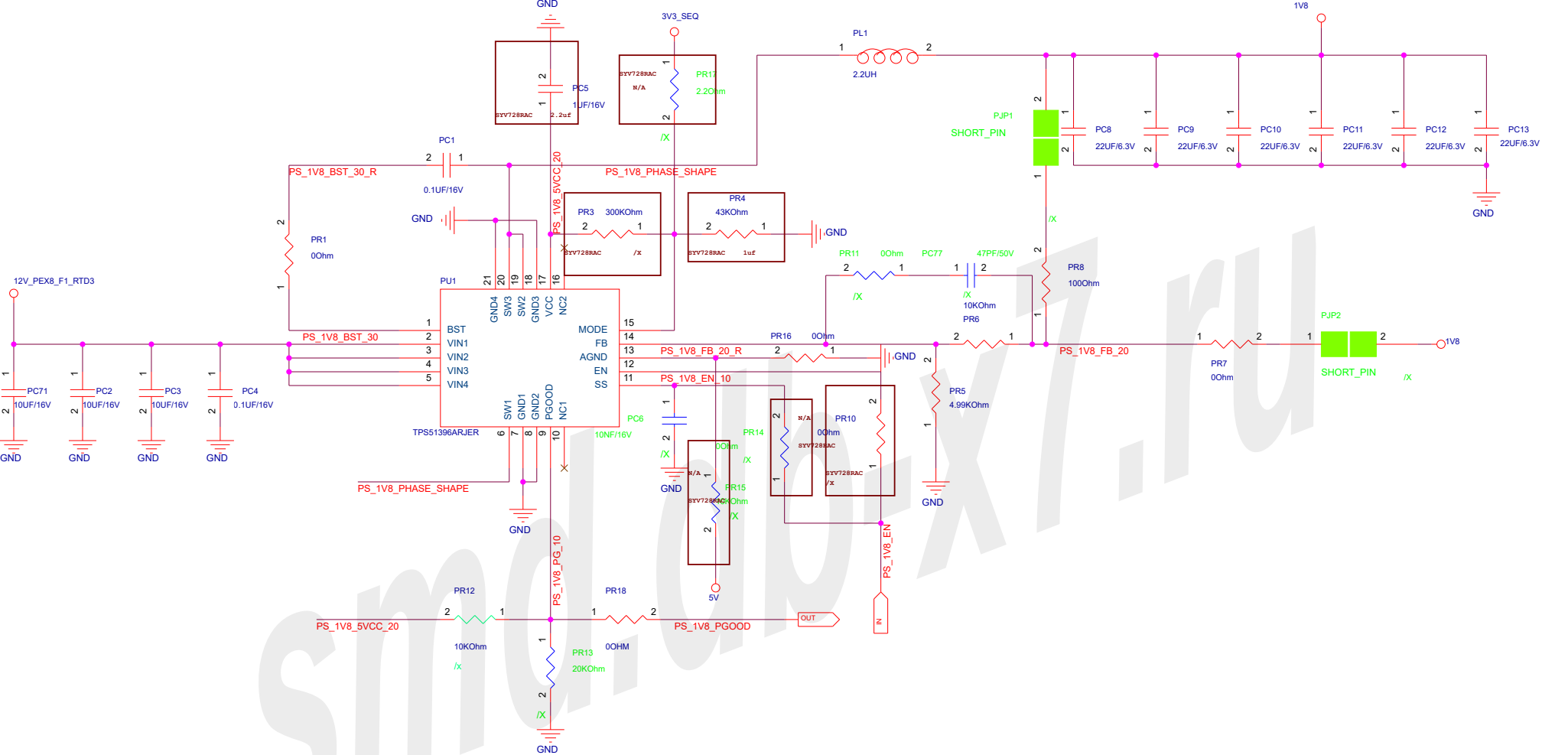

PHASE1
PHASE2
TI require 2.2uF
2.2 OHM
For test
SHORT_PIN
SOLDER PASTE
GND



Title	<Title>	
Size: A3	Document Number <Doc>	Rev <RevCode>
Date: Monday, July 27, 2020	Sheet 1 of 1	

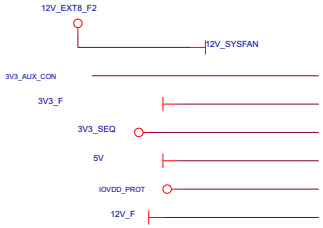


Title :		
<OrgName>	Engineer:	
Size: C	Project Name	Rev
Date:	Sheet of	



Title :		
<OrgName>	**Engineer:**	
Size: A4	Project Name	Rev
Date:	Sheet	of

Power



From 12V (for 外接式風扇使用, 任一組12V皆可)
From PCIE 3V3_AUX (for ITE)
From BUS 3V3 (for ITE logic判斷)
3v3_prot start after pex
From 5V (for 背板LED)
1V8
12V

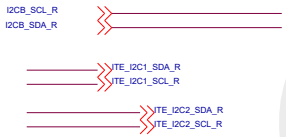
from ite for strix to swap fan1 and fan3 tach

From EXT 0 (外部電源第一組)
From EXT1 (外部電源第二組)
From EXT1 (外部電源第三組)

PSU DETECT INPUT

GPU_GPIO

I2C

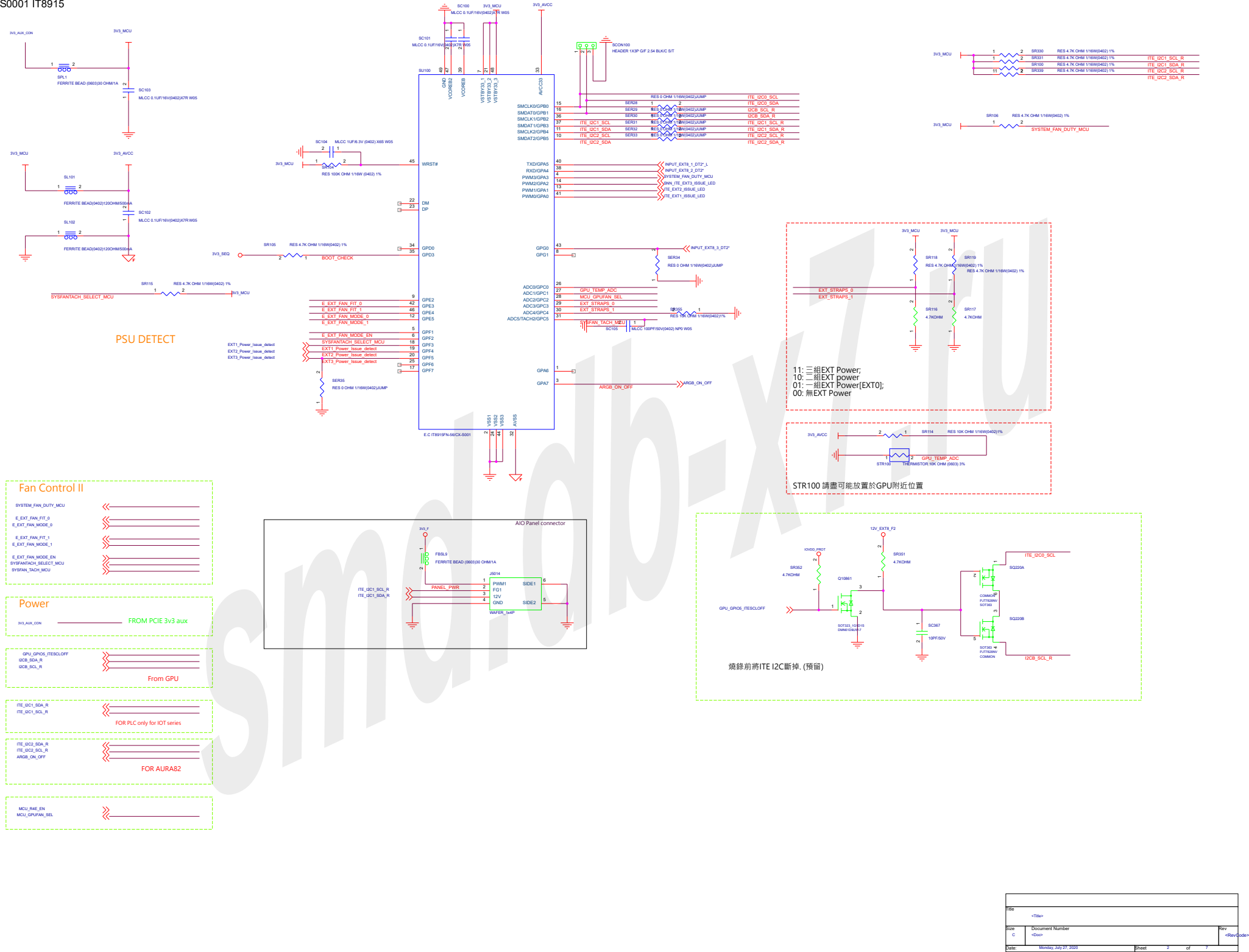


GPU I2CB Master (for ITE / ENE/NCT3933)
from ITE(FOR PLC ONLY)
ITE I2C MASTER (FOR AURA82 JUEST COLAY)

VGA HOTWIRE

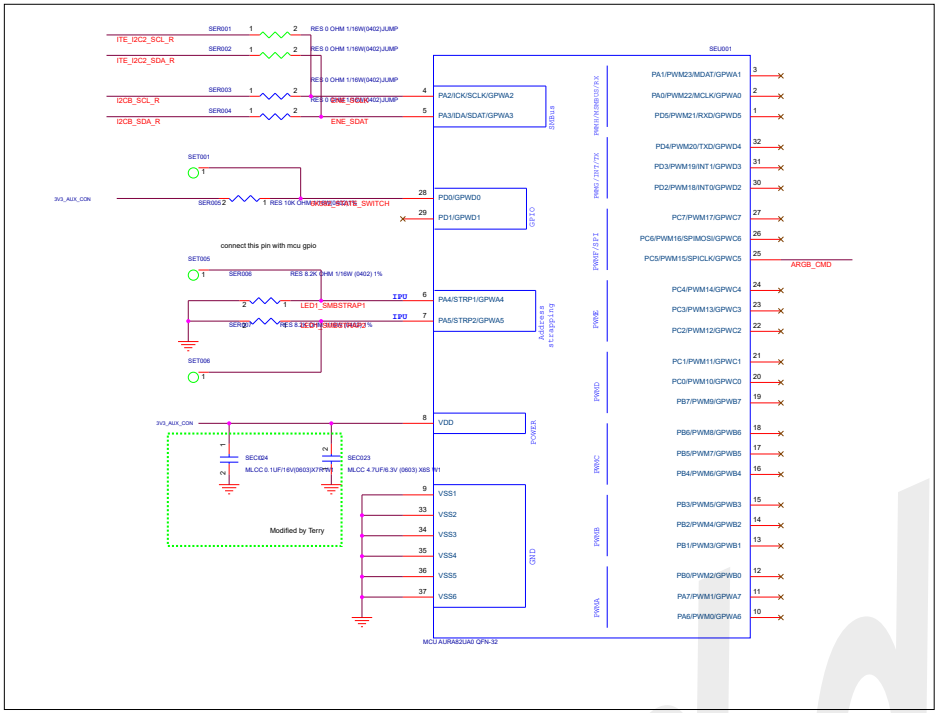
Title	<Title>	
Size: B	Document Number: <Doc>	Rev: <RevCode>
Date: Monday, July 27, 2020	Sheet 1 of 7	

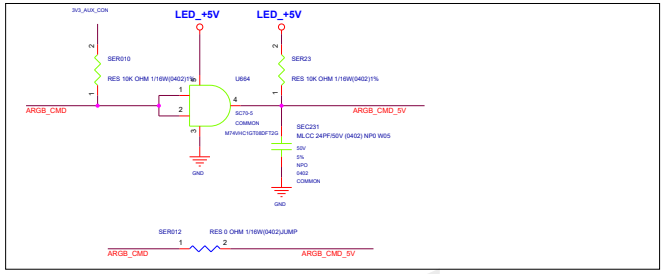
S0001 IT8915

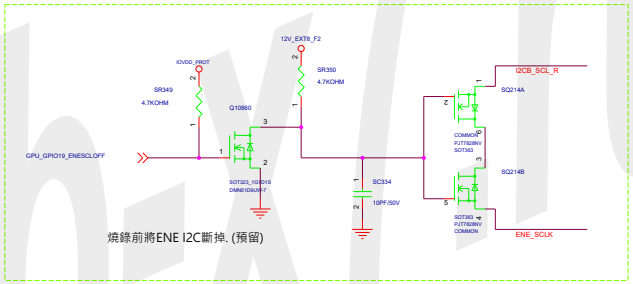


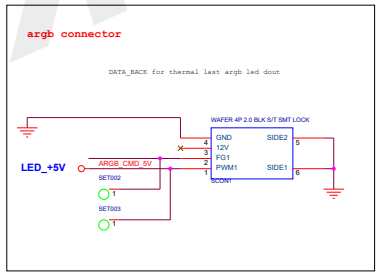
Title	<Title>		
Size: C	Document Number: <Doc>		Rev: <RevCode>
Date: Monday, July 27, 2020	Sheet 2 of 7		

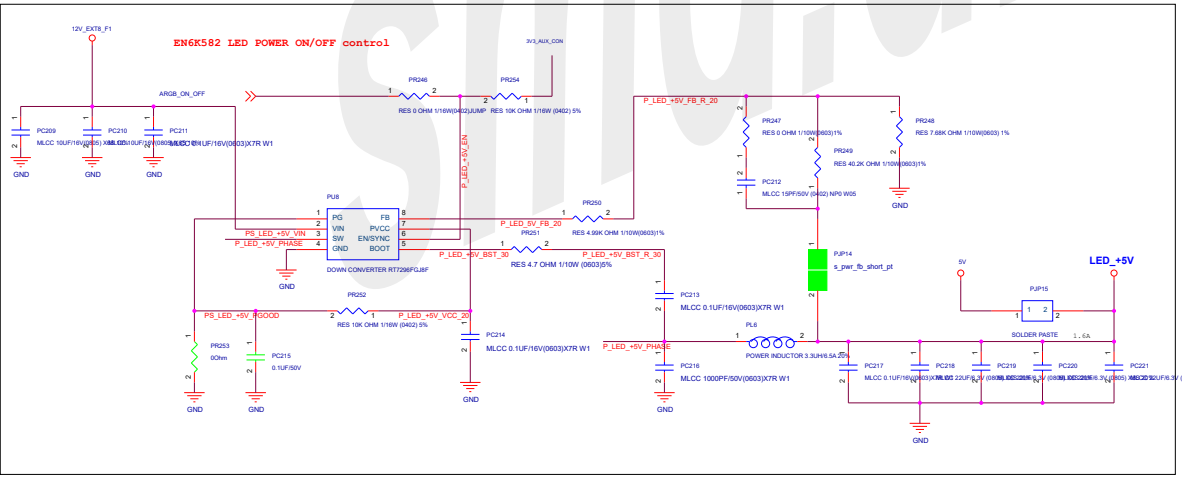
EN6K582

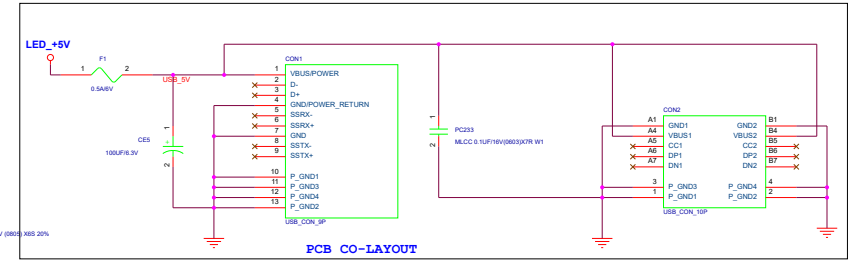






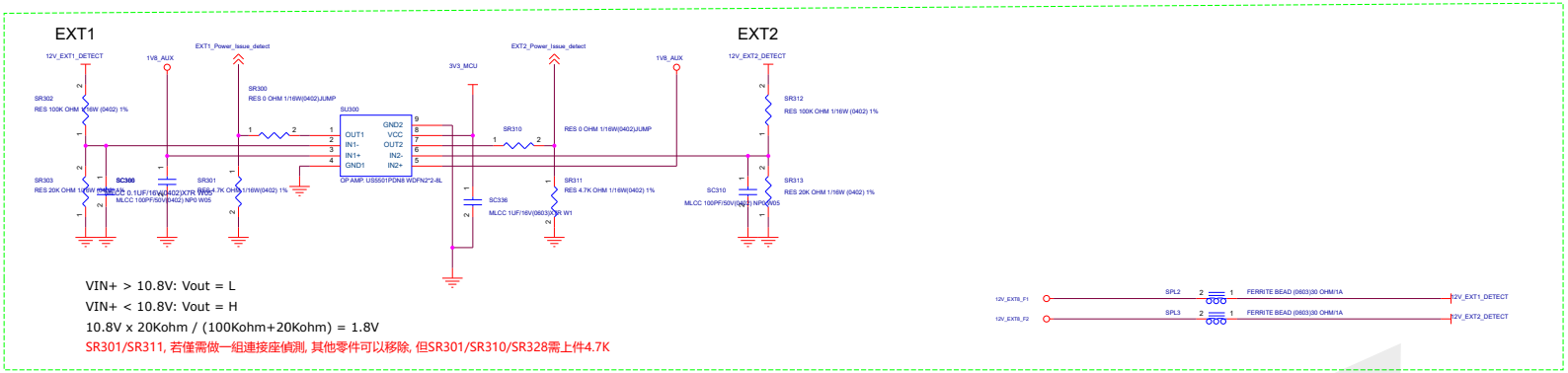






Title	<Title>		
Size: C	Document Number <Doc>		Rev <RevCode>
Date: Monday, July 27, 2020		Sheet 3 of 7	

PSU DETECT

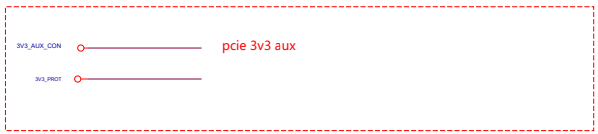


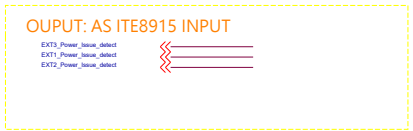
VIN+ > 10.8V: Vout = L

VIN+ < 10.8V: Vout = H

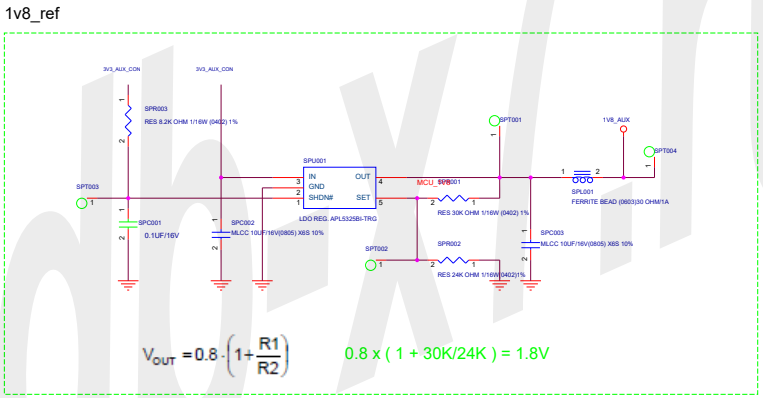
10.8V x 20Kohm / (100Kohm+20Kohm) = 1.8V

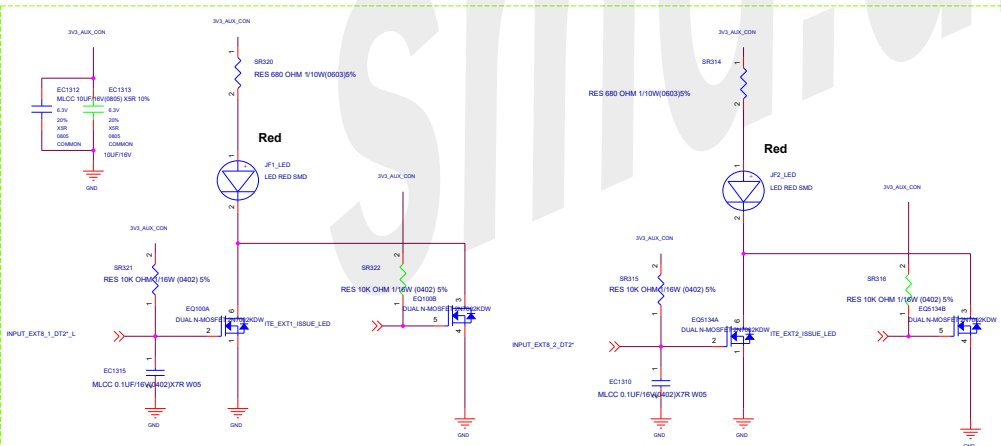
SR301/SR311, 若僅需做一組連接座偵測, 其他零件可以移除, 但SR301/SR310/SR328需上件4.7K





1v8_ref

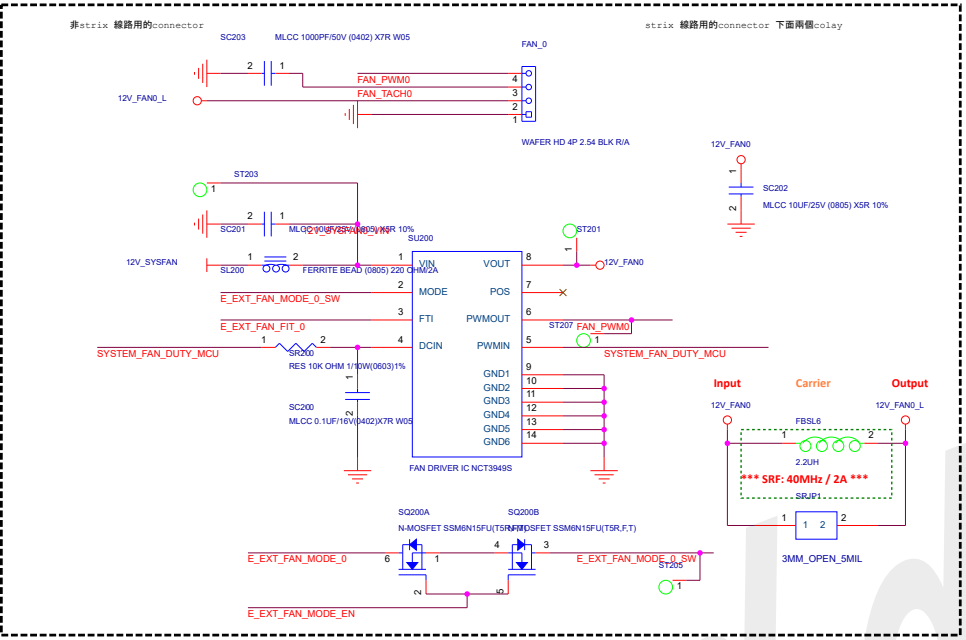


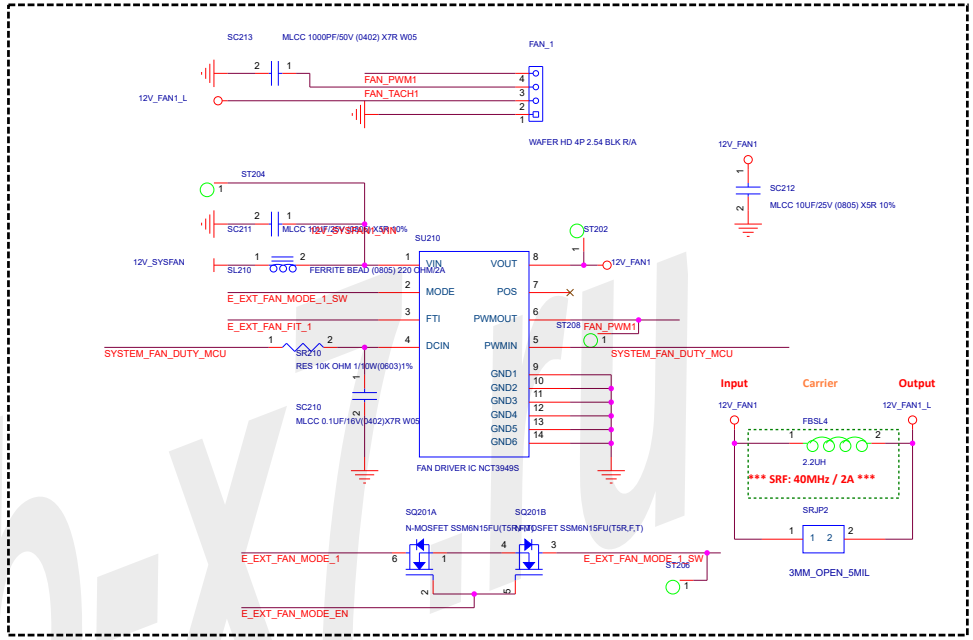


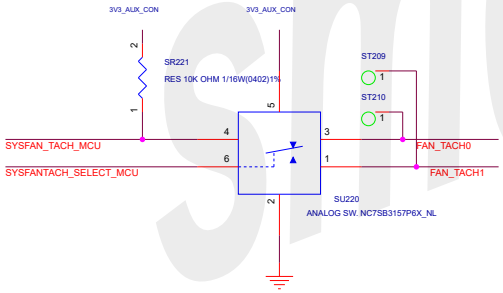
1.EXT power is not connected,
the led is always on
2.EXT power is connected
EXT 12V is over 10.8V, the led turns off
EXT 12v is below 10.8v.the led blink

Title	<Title>	
Size: C	Document Number <Doc>	Rev <RevCode>
Date: Monday, July 27, 2020	Sheet 4 of 7	

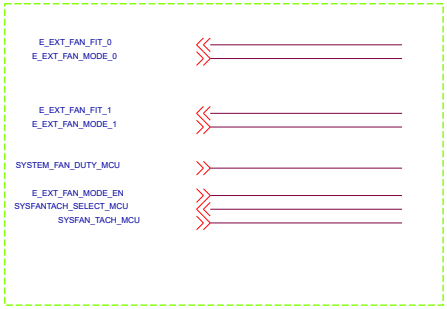
S0002 SYSTEM FAN CONTROL







Fan Control II



Title	<Title>	
Size: B	Document Number: <Doc>	Rev: <RevCode>
Date: Monday, July 27, 2020	Sheet 5 of 7	

PS: Power Flow