

PG142-B00

DP + DP + DP + HDMI/DP

TABLE OF CONTENTS

Page Description

1	Table of Contents
2	Block Diagram
3	PCI Express
4	PCIE GEN4 RC TERMINATIONS
5	MEMORY: GPU_FB_AB
6	MEMORY: FBA[31:0]
7	MEMORY: FBA[63:32]
8	MEMORY: FBB[31:0]
9	MEMORY: FBB[63:32]
10	MEMORY: GPU_FB_CD
11	MEMORY: FBC[31:0]
12	MEMORY: FBC[63:32]
13	MEMORY: FBD[31:0]
14	MEMORY: FBD[63:32]
15	GPU PWR & GND 1
16	GPU PWR & GND 2
17	GPU PWR & GND 3 (XVDD)
18	GPU DECOUPLING FBVDDQ
19	GPU DECOUPLING NVVDD
20	GPU DECOUPLING NVVDD
21	IO: IFPAB NC
22	IO: IFPF DP
23	IO: IFPE DP
24	IO: IFPD DP
25	IO: IFPC HDMI/DP

Page Description

26	MISC1: ROM, XTAL, STRAPS
27	MISC2: JTAG, GPIO, ADC, I2C, FL, STEERO
28	MISC3: RGB
29	PS: 1V8
30	PS: 5V
31	PS: PEXVDD
32	PS: FBVDDQ
33	PS: FBVDDQ PH2
34	PS: NVVDD Controller
35	BLANK PAGE
36	PS: NVVDD PH4, PH6
37	PS: NVVDD PH1, PH3
38	PS: NVVDD PH2, PH5
39	PS: NVVDD PH9
40	PS: NVVDD PH7
41	PS: NVVDD PH10, PH8
42	PS: OVRS_INPUT POWER BALANCE
43	PS: RDT3_12V & 3V3_A Switcher
44	PS: INPUTS, FILTERING and MONITORING
45	PS: PEX_12V, PEX_3V3 AND A3V3_AUX
46	PS: STEERING, UPB, HOT UNPLUG
47	SEQ: 5V, 1V8, 3V3_SEQ
48	SEQ: NVVDD, PEX, FBVDDQ ENABLE
49	SEQ: MISC
50	SEQ: VOLTAGE MONITOR

Page Description

51	FAN & LED
52	PS:OVRM_PWR_SENSE
53	MECH
54	PTC



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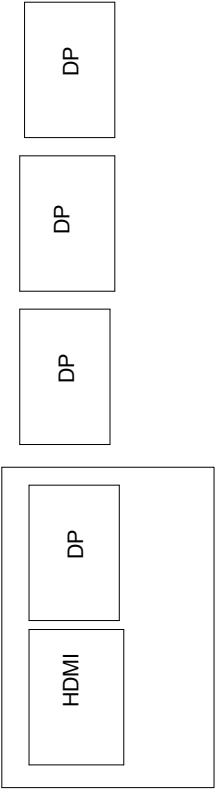
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Date: Friday, July 31, 2020		Sheet 1 of 54

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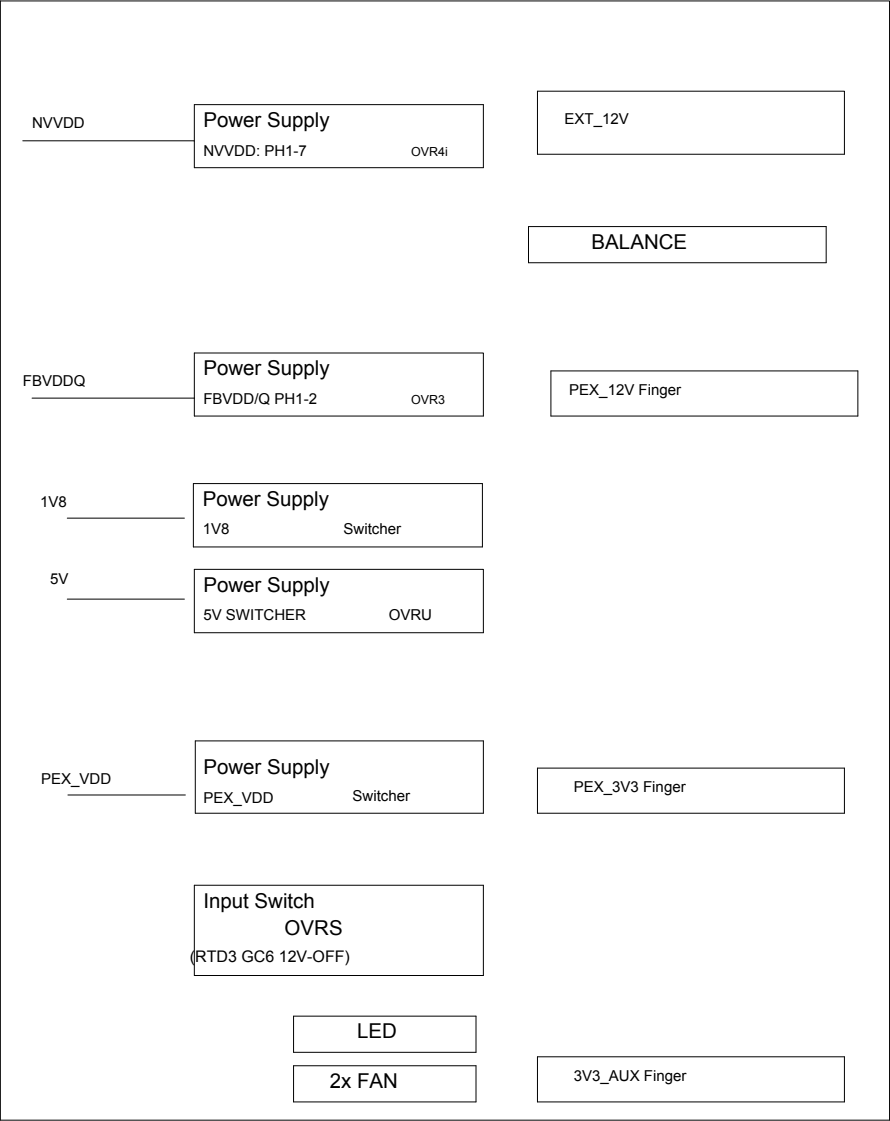
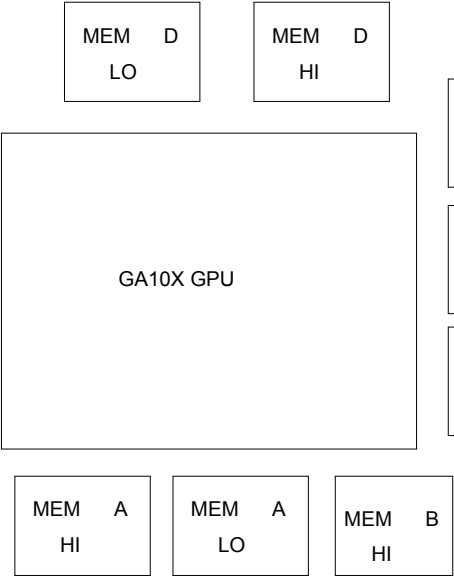


NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	1 OF 54
BCM REV	A	DATE	27-JUN-2020

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POWER SUPPLY





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Date: Friday, July 31, 2020	Sheet 2 of 56	

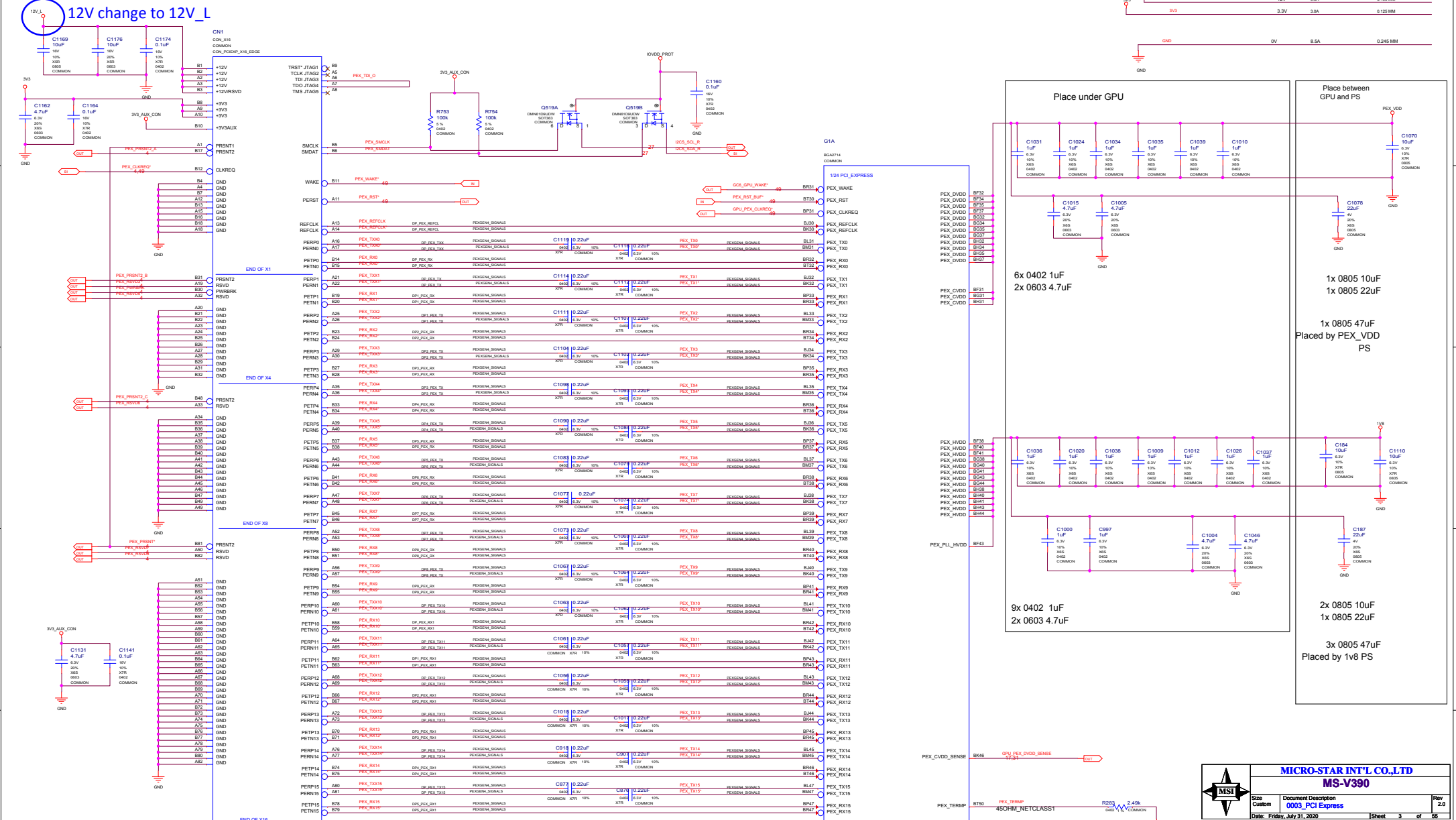
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NV_PN	600-1G142-BASE-100	PAGE	2 OF 54
PCB REV	PG142-800	DATE	27-JUN-2020
BCM REV	A		





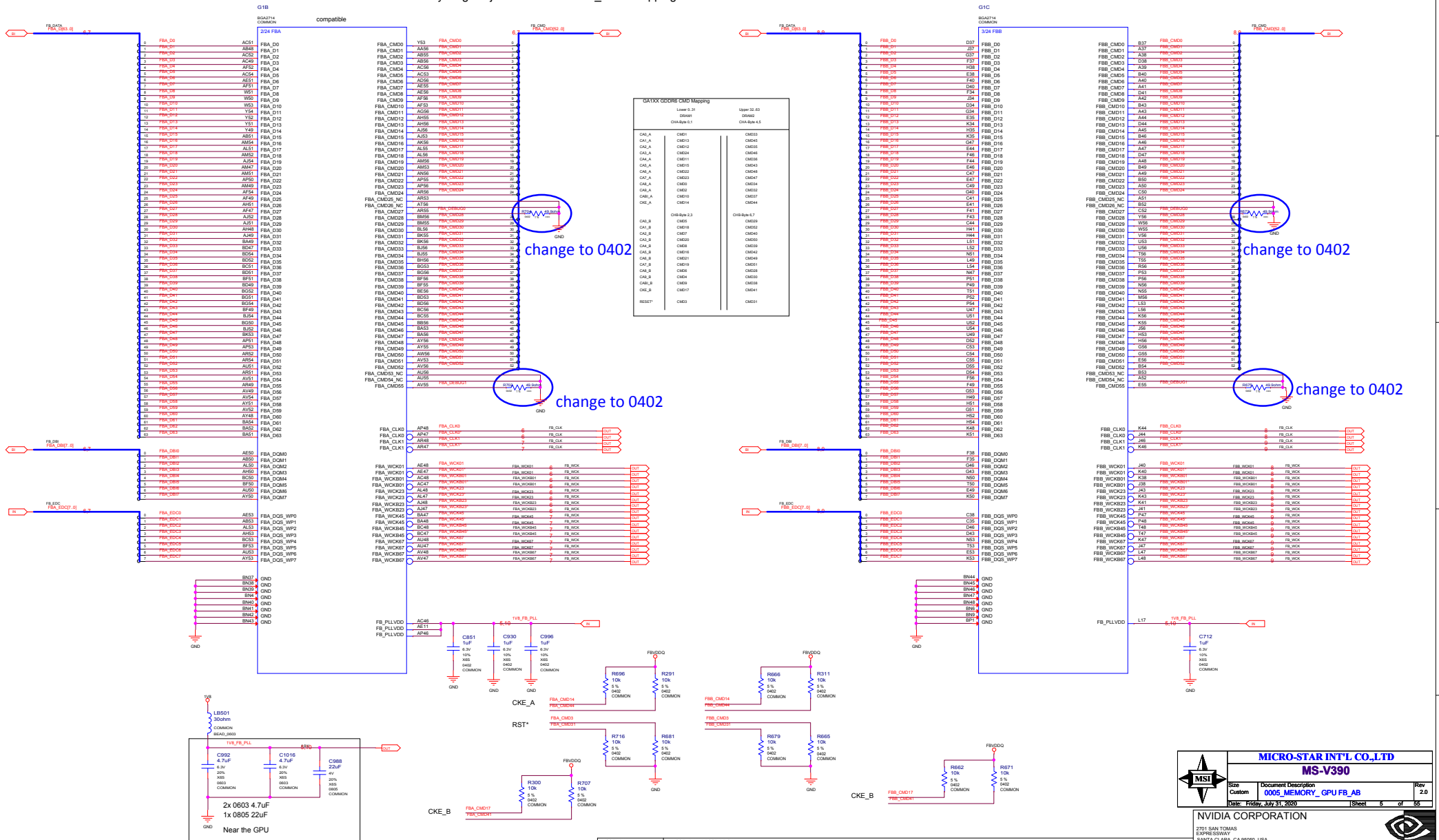


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Size	Document Description	Rev	
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Date: Friday, July 31, 2020	Sheet 4 of 56		

NVIDIA CORPORATION			
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NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	4 OF 54
BOM REV	A	DATE	27-JUN-2020

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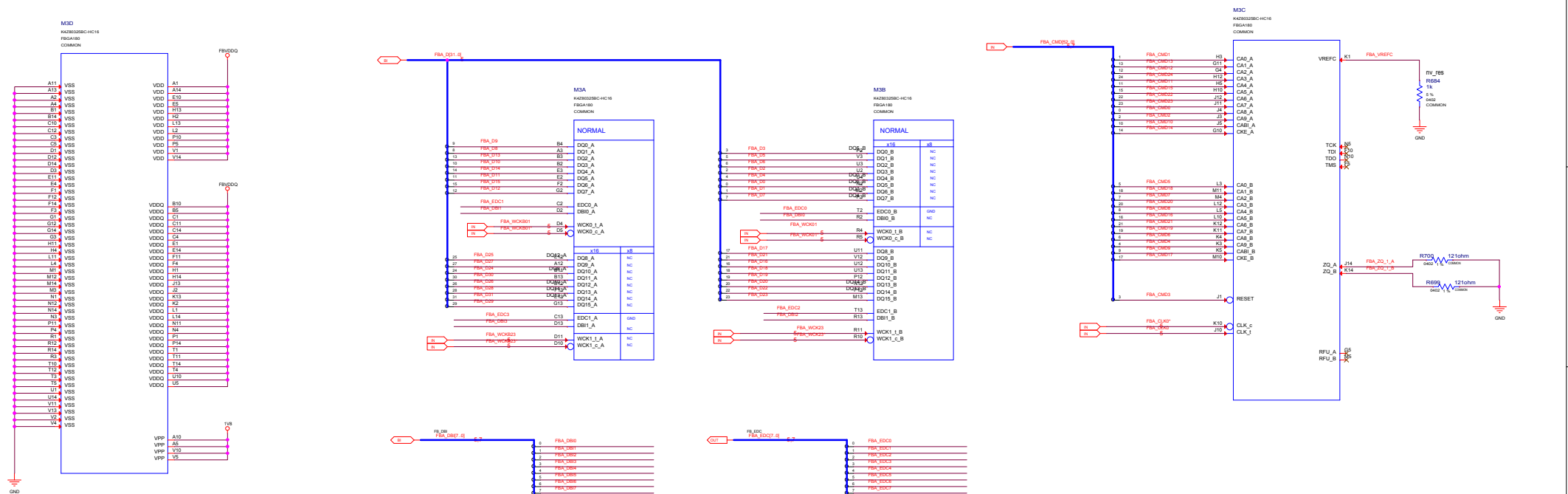
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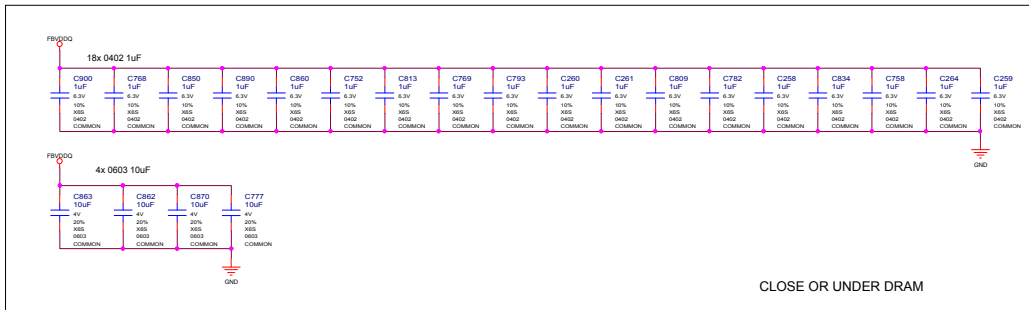
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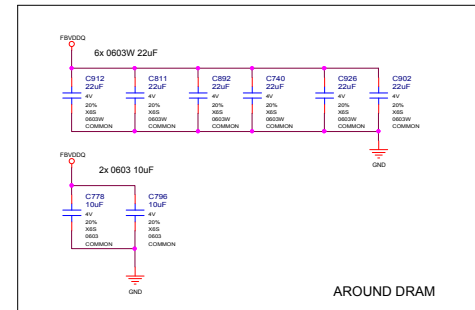
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DATE 27-JUN-2020



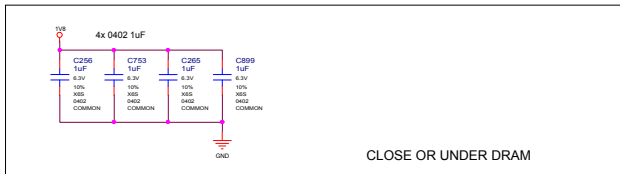
decap via : at least 2 gnd vias and 2 power vias for each cap



CLOSE OR UNDER DRAM



AROUND DRAM



CLOSE OR UNDER DRAM

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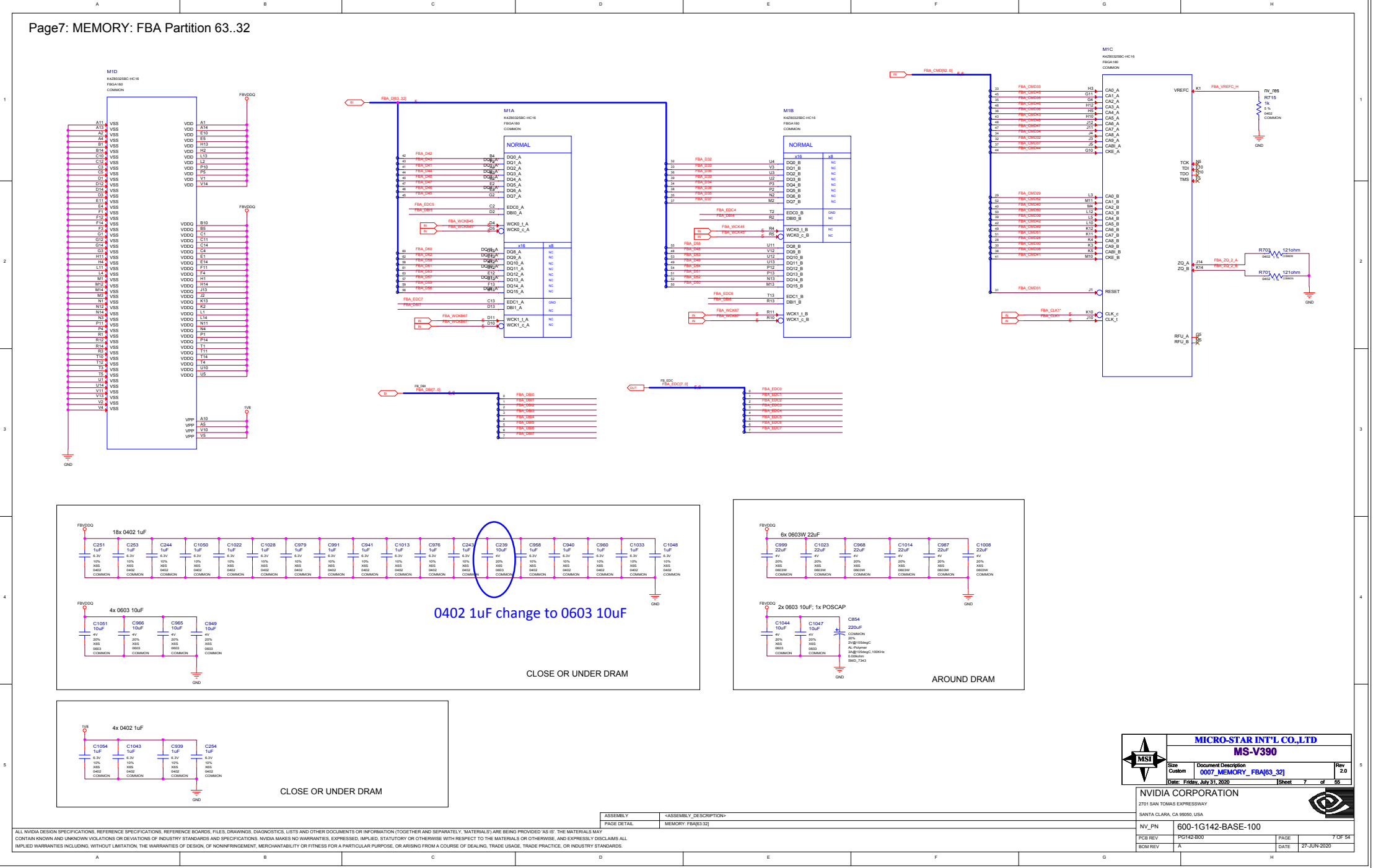
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Rev: 2.0
Sheet: 6 of 56

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NV_PN 600-1G142-BASE-100
PCB REV PG142-B00
ICM REV A

PAGE 6 OF 54
DATE 27-JUN-2020

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0007 MEMORY_FBA[63..32]

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Date:

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Sheet

7

of

55

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NV_PN

600-1G142-BASE-100

PCB REV

PG142-B00

PAGE

7

OF

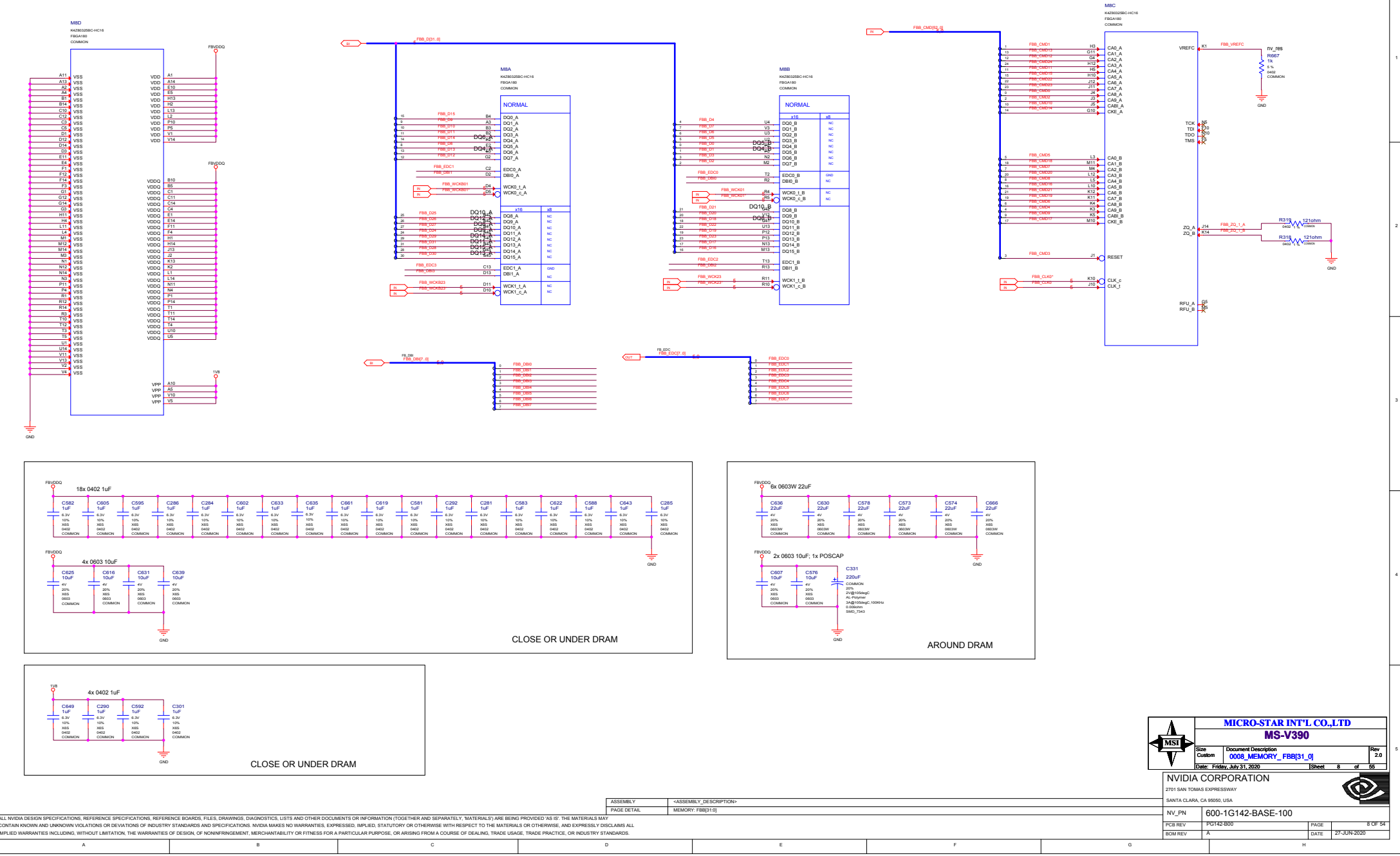
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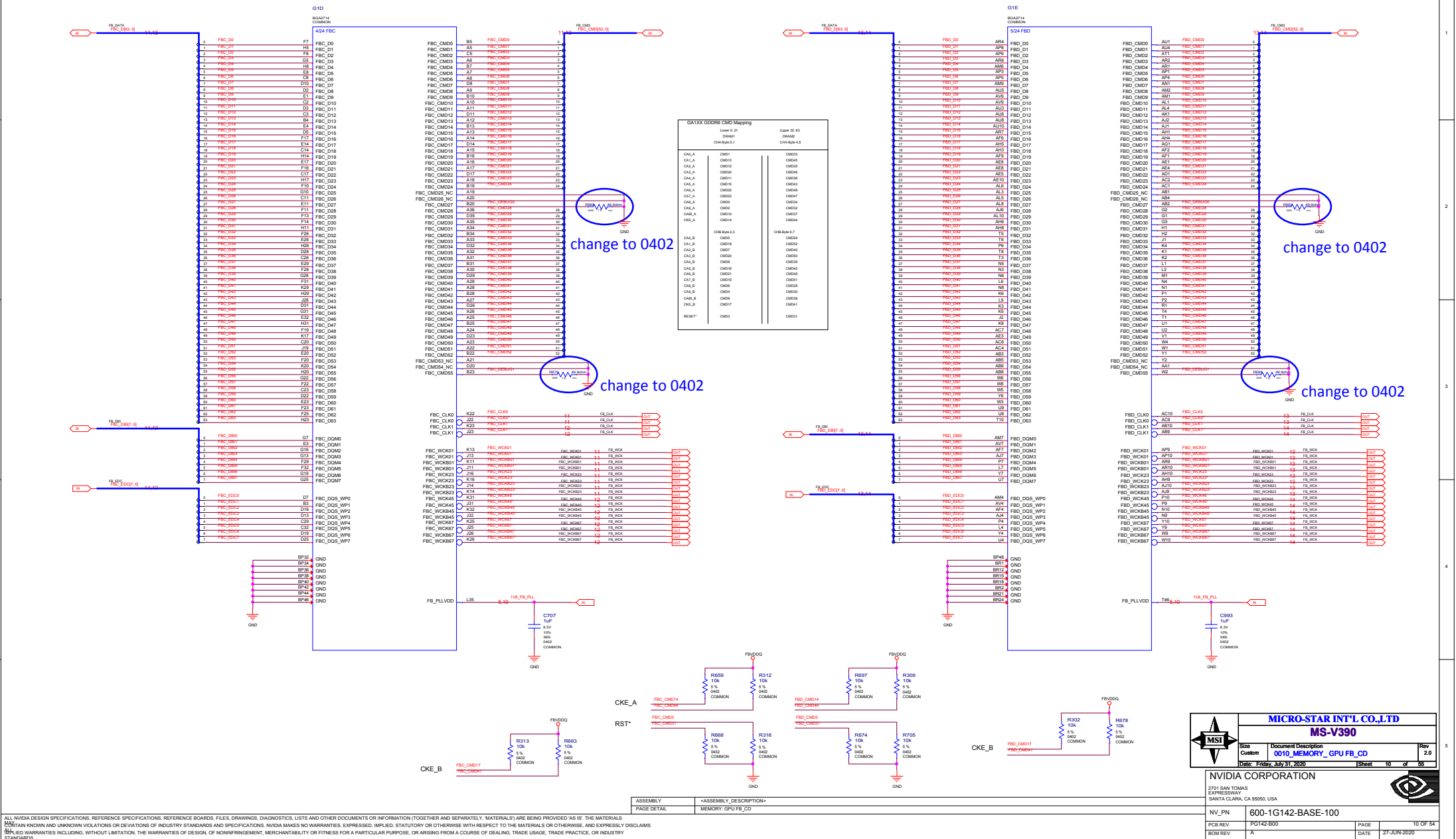
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Sheet: 10 of 55

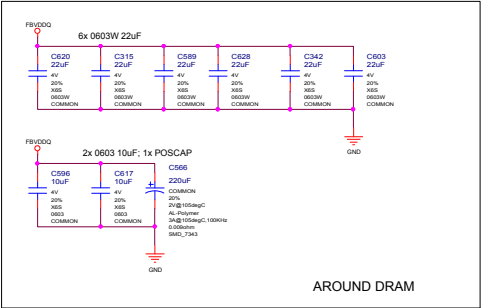
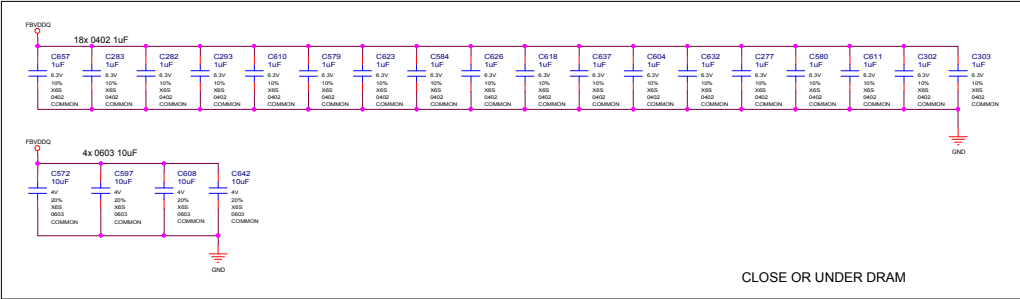
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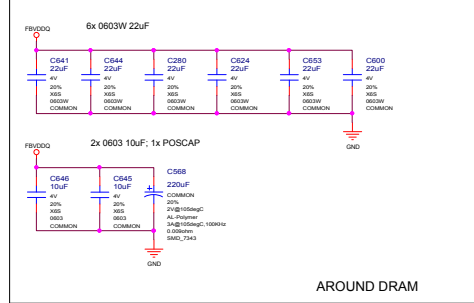
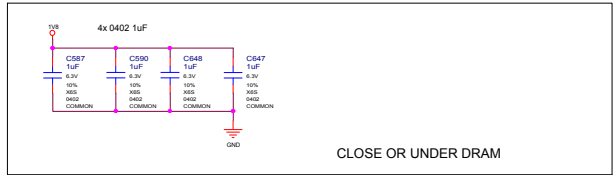
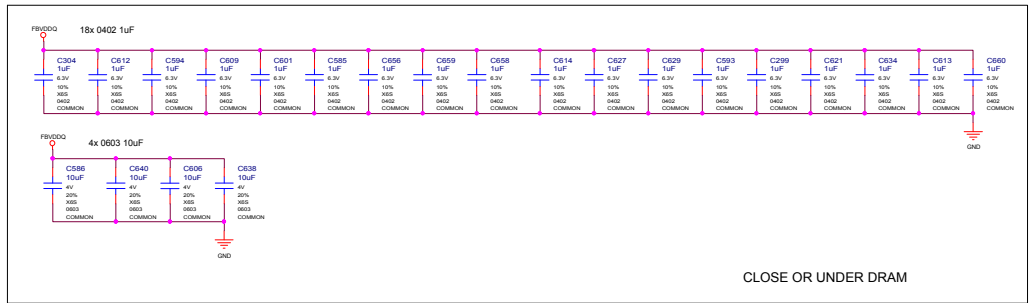
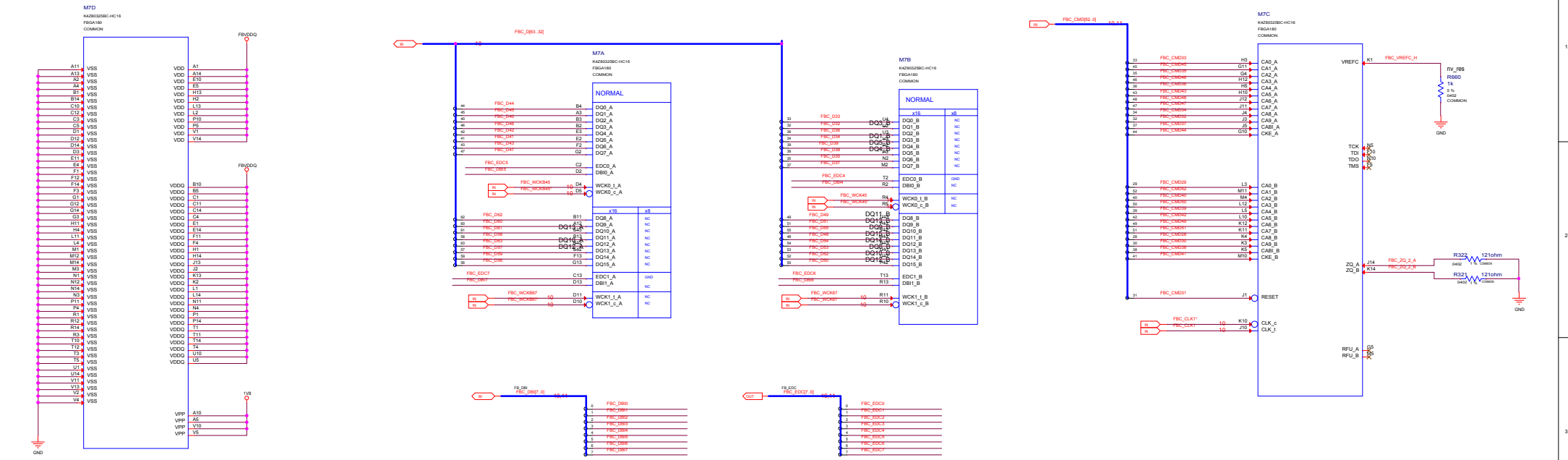
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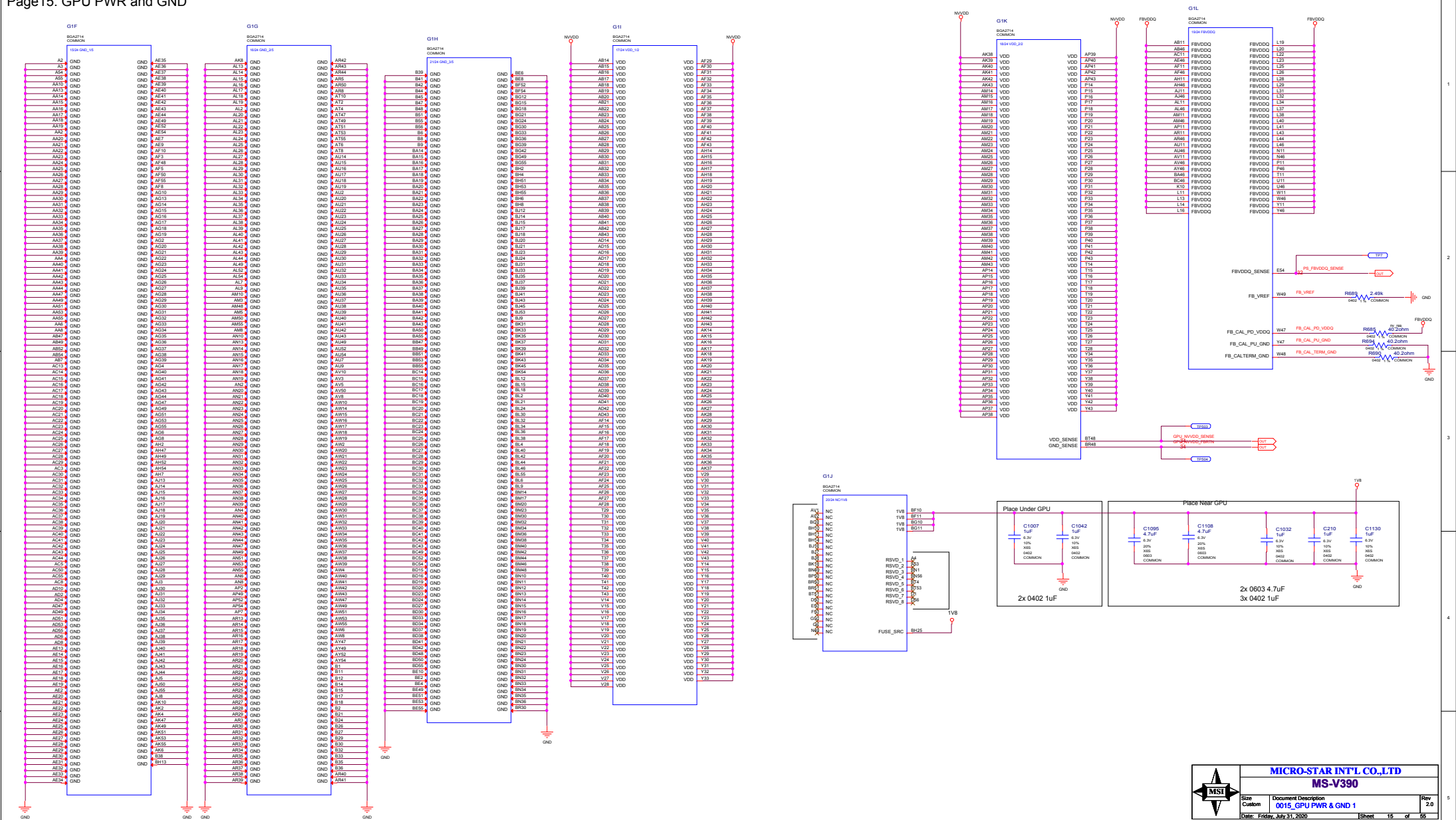
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Rev: 2.0
Sheet: 11 of 56

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NV_PN	600-1G142-BASE-100
PCB REV	PG142-800
ICOM REV	A
PAGE	11 OF 54
DATE	27-JUN-2020

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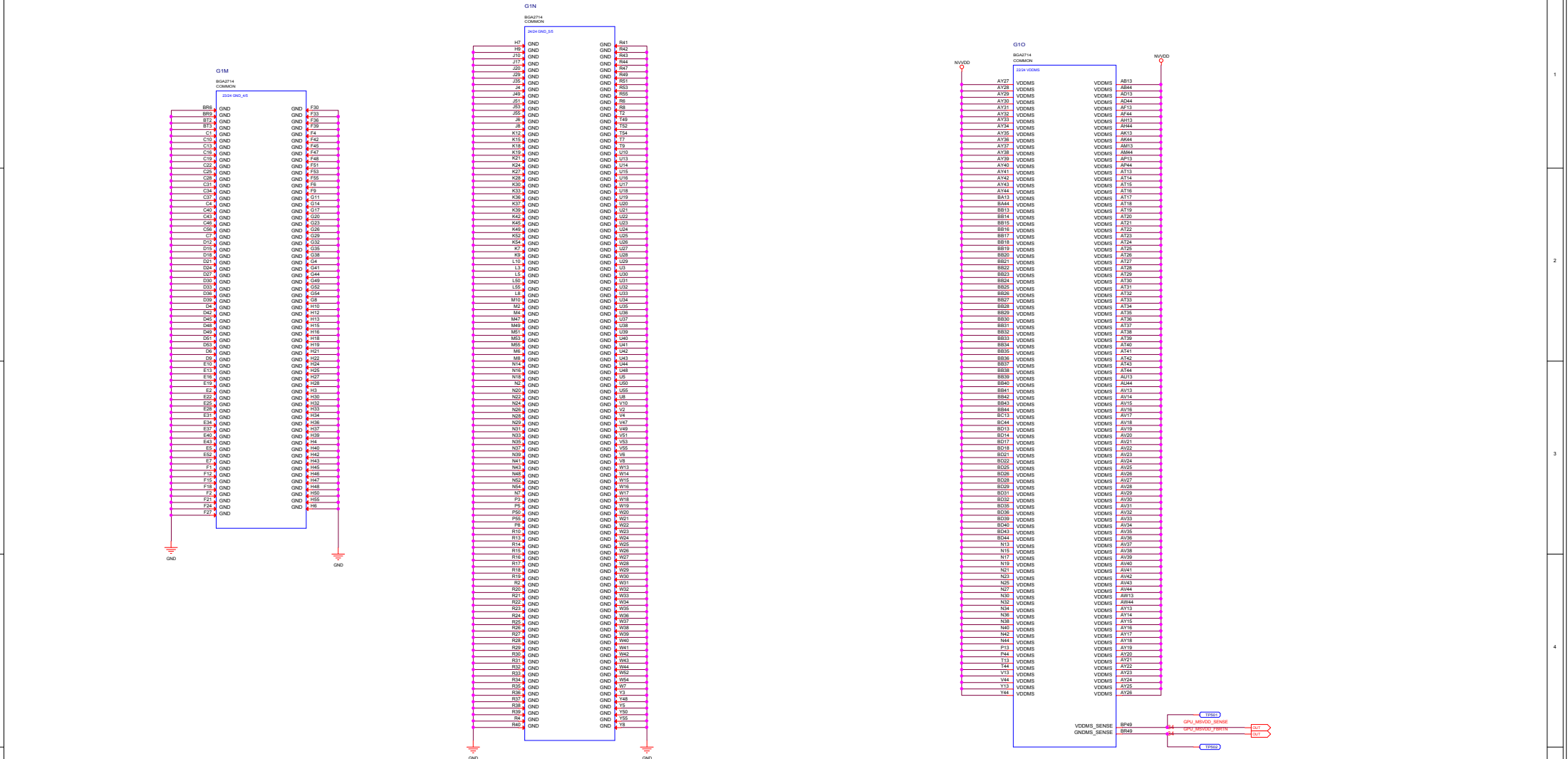




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7201 SAN TOMAS EXPRESSWAY		PAGE 15 OF 24	
SANTA CLARA, CA 95050, USA		DATE: 27-JUN-2020	





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Size: Custom

Document Description: 0016_GPU PWR & GND 2

Rev: 2.0

Date: Friday, July 31, 2020

Sheet: 18 of 55



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PCB REV PG142-800

ICM REV A

PAGE 18 OF 54

DATE 27-JUN-2020

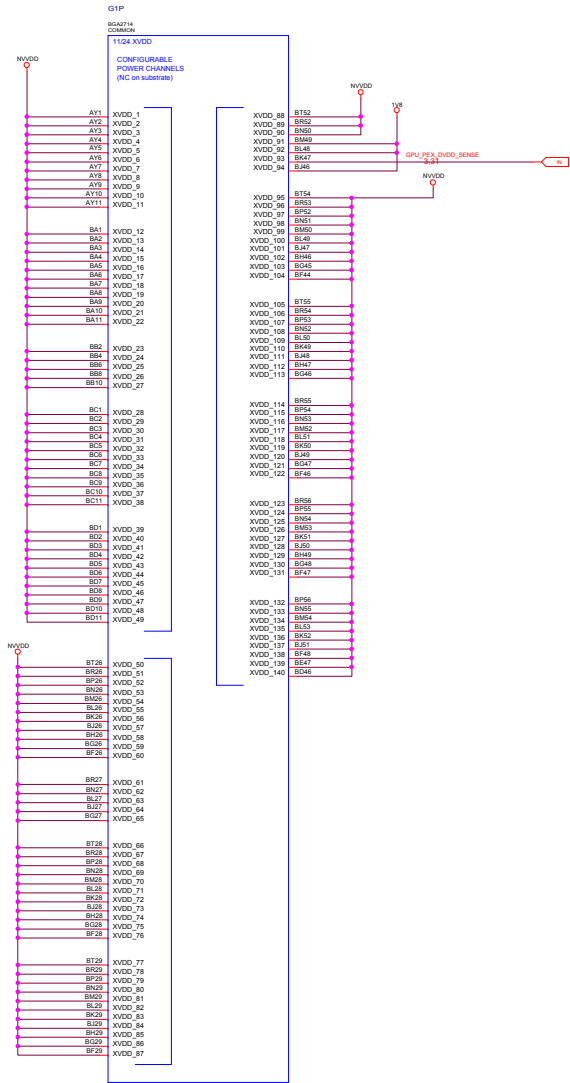
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GPU PWR & GND

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Size	Custom	Document Description	Rev
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Date:	Friday, July 31, 2020	Sheet	17 of 56

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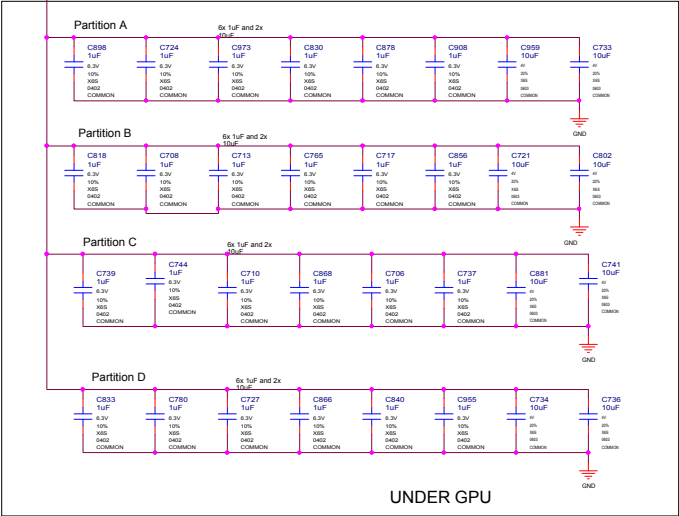


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PCB REV	PG142-B00
ICM REV	A
PAGE	17 OF 54
DATE	27-JUN-2020

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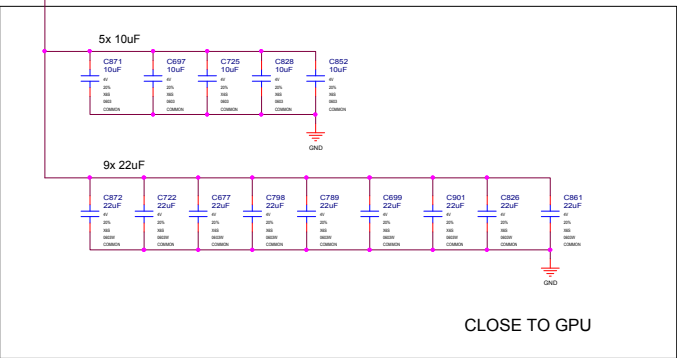
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UNDER GPU

FBVDDQ

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CLOSE TO GPU

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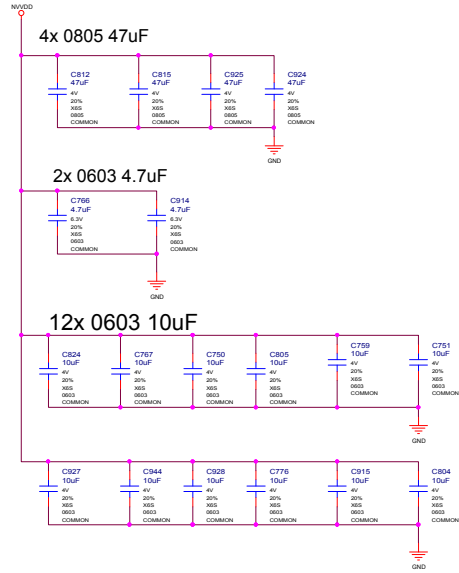
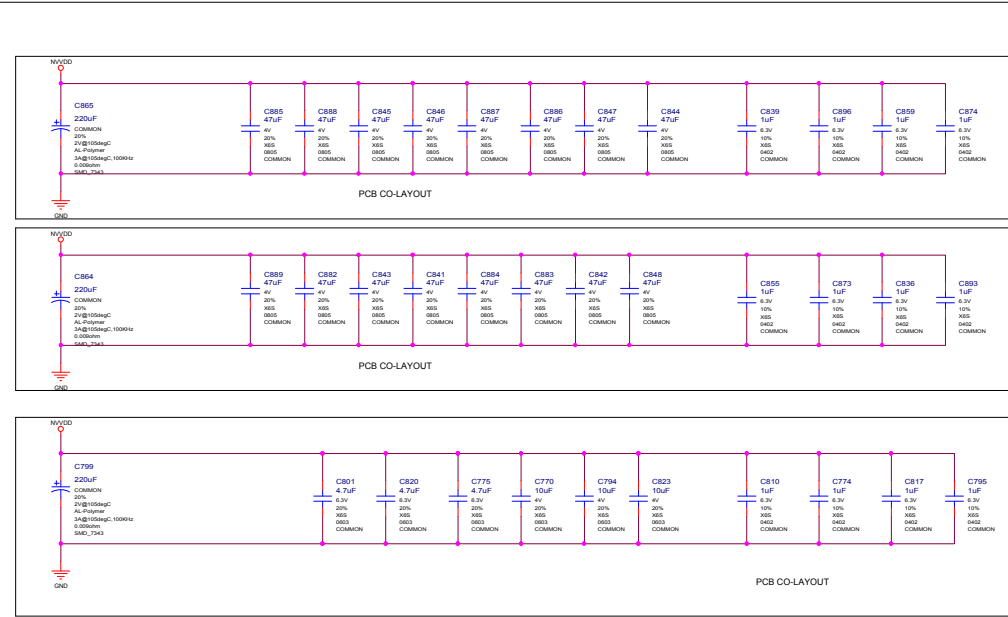
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Date:	Friday, July 31, 2020	Sheet	18	of	55

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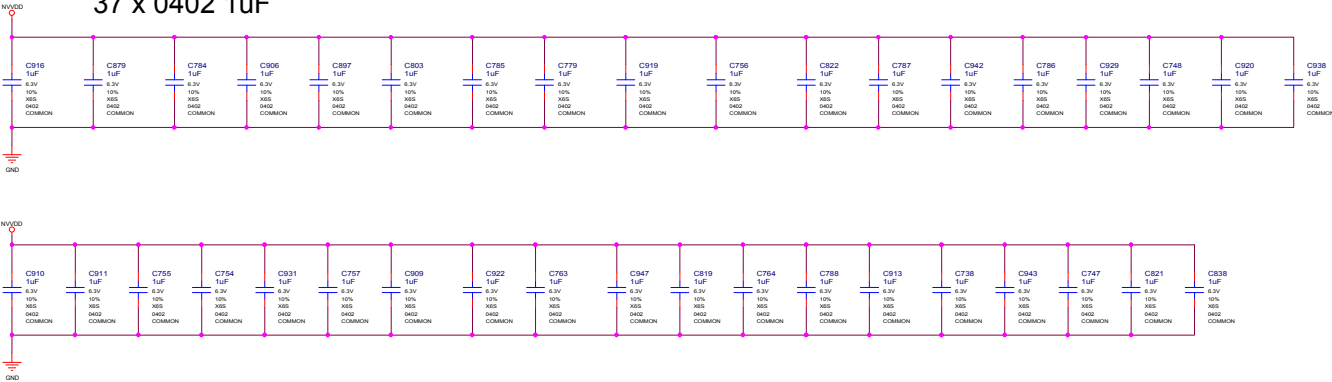


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BOM REV	A		DATE	27-JUN-2020	

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Document Description

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Date

Friday, July 31, 2020

Sheet 19 of 55

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600-1G142-BASE-100

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PG142-B00

ICOM REV

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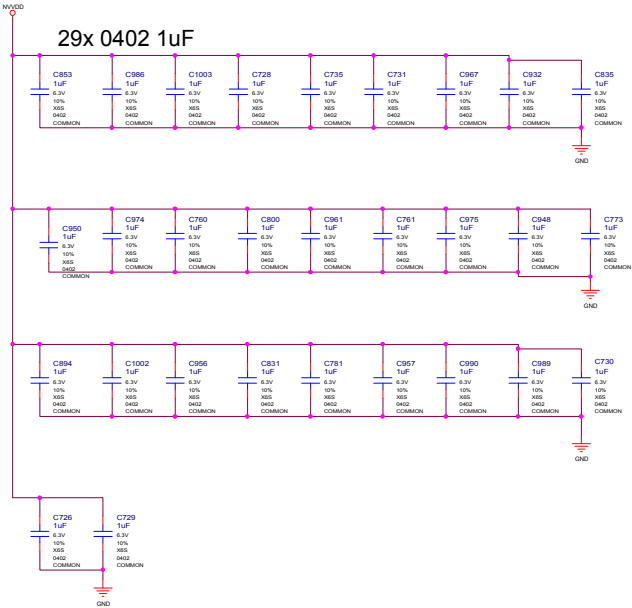
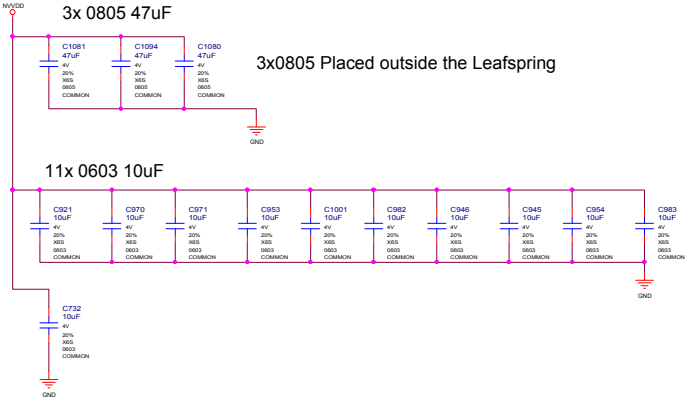
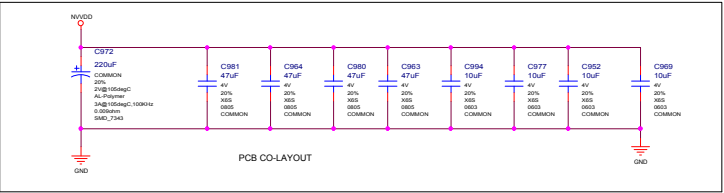
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UNDER GPU

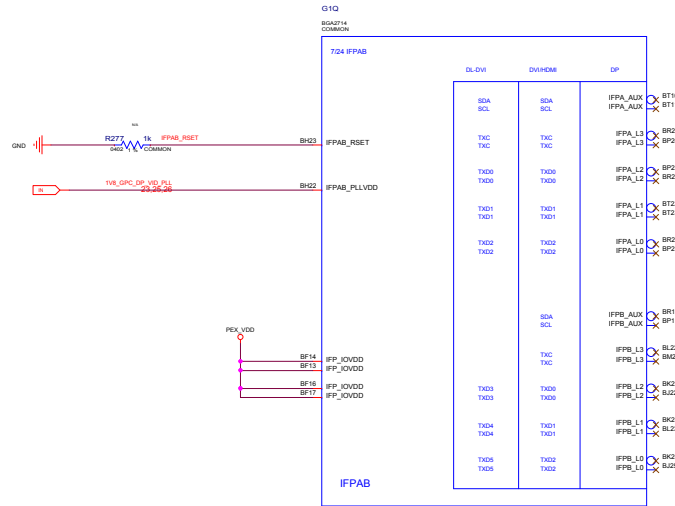


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MS-V390	
Size	Custom
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Date:	Friday, July 31, 2020
Sheet	20 of 55



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2701 SAN TOMAS EXPRESSWAY	
SANTA CLARA, CA 95050, USA	
NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	20 OF 54
DATE	27-JUN-2020

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DECLAIMS		PCB REV		PG142-B00	PAGE	21 OF 54
		BOM REV		A	DATE	27-JUN-2020



MICRO-STAR INT'L CO., LTD			
MS-V390			
Size	Document Description	Rev	
Custom	0021_IO_IFPAB NC	2.0	
Date: Friday, July 31, 2020	Sheet	21	of 55

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STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG SAMSUNG 8Gb 7GHz
L	L	H	00001	RAMCFG MICRON 8Gb 7GHz
L	H	L	00010	RAMCFG HYNIX 8Gb 7GHz
H	H	L	00110	RAMCFG SAMSUNG 16Gb 8GHz
		TBD		

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0]FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
H	H	M	0000	FS_OVERT DISABLE

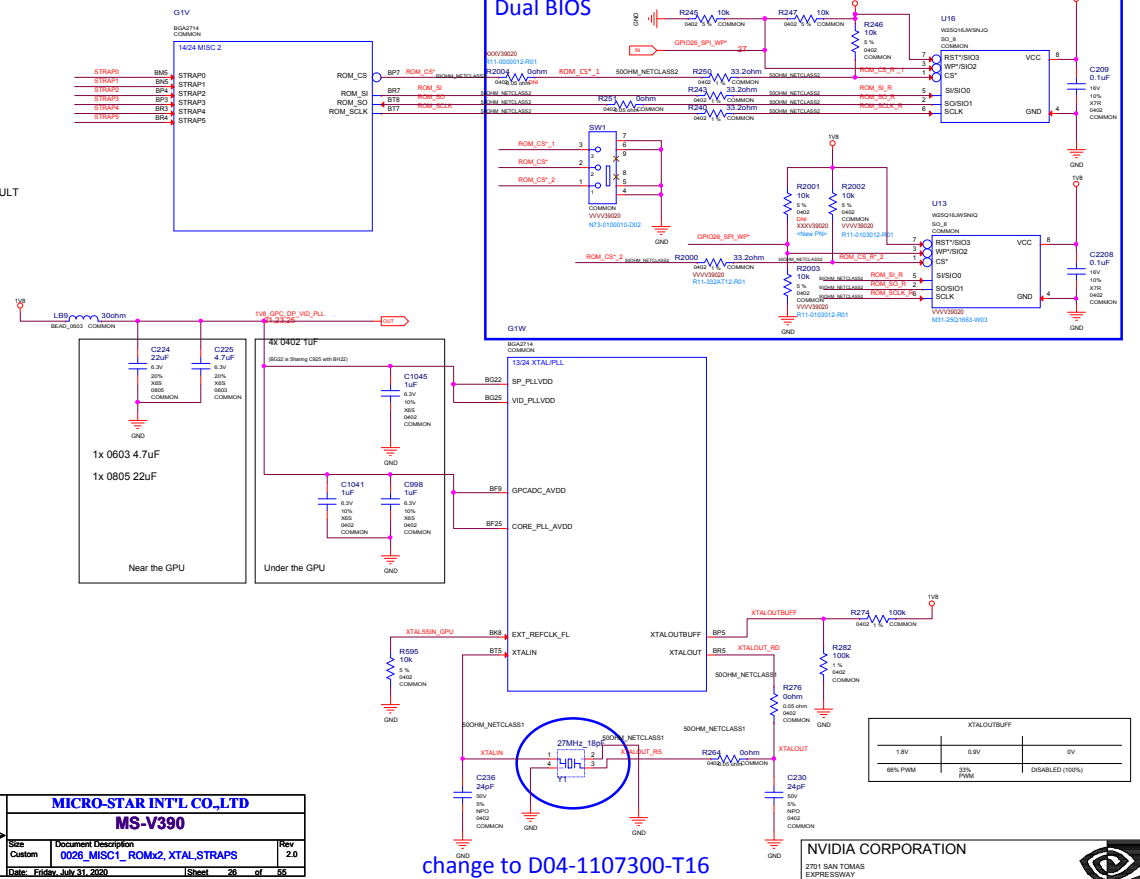
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M	L	H	1	1	0	1
M	L	L	1	0	1	1
L	H	M	1	0	1	1
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE
1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGINAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

DEFAULT



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MS-V390			
Size	Document Description	Rev	
Custom	0026_MISC1_ROMx2, XTAL_STRAPS	2.0	
Date: Friday, July 31, 2020		Sheet	26 of 55
ASSEMBLY	*ASSEMBLY DESCRIPTION*		
PAGE DETAIL	MISC1: ROM, XTAL_STRAPS		

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PCB REV PG142-800
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PAGE 26 OF 54
DATE 27-JUN-2020



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remove LED

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PAGE DETAIL	MISC3: RGB



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Size	Document Description	Rev
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Date: Friday, July 31, 2020		Sheet 28 of 56

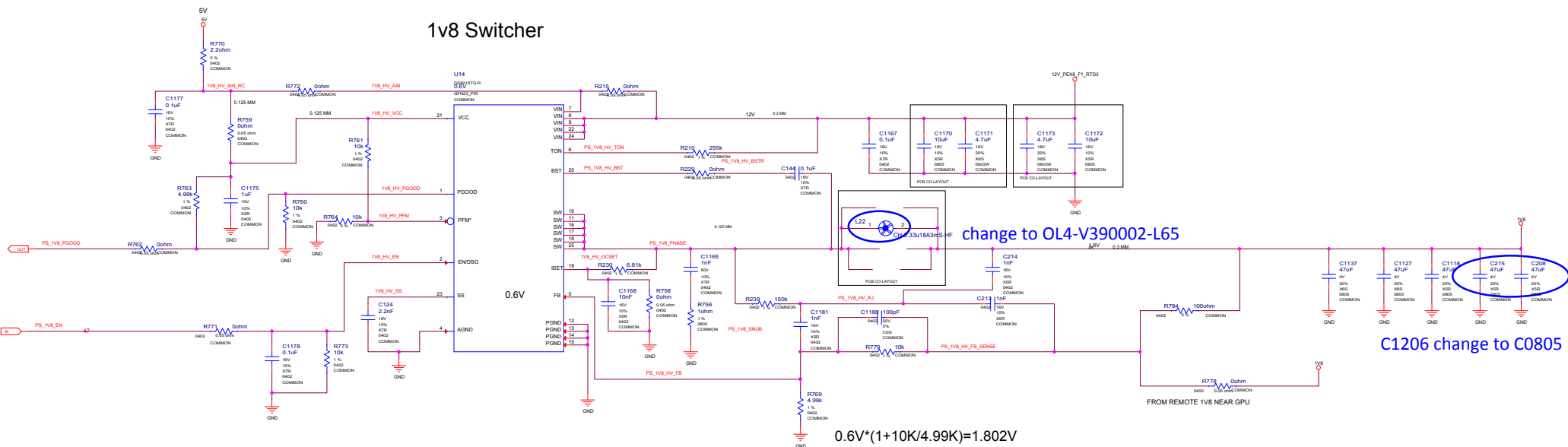
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NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	28 OF 54
BOM REV	A	DATE	27 JUN 2020

1v8 Switcher



$0.6V \times (1 + 10K / 4.99K) = 1.802V$

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Size: Custom

Document Description: 0029_PS_1V8

Rev: 2.0

Date: Friday, July 31, 2020

Sheet: 29 of 55

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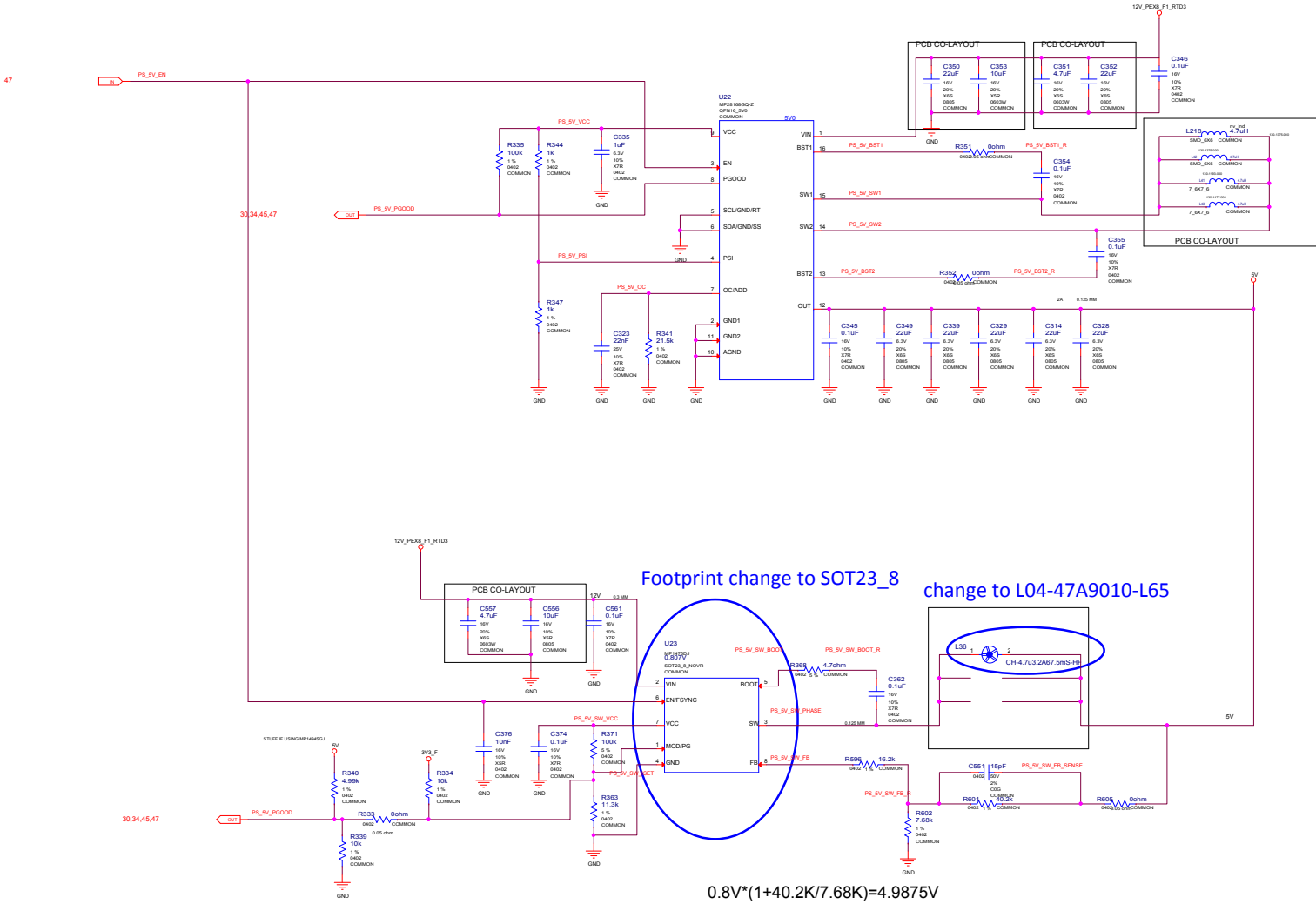
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PCB REV: PG142-800

DATE: 27-JUN-2020

PAGE: 29 OF 54

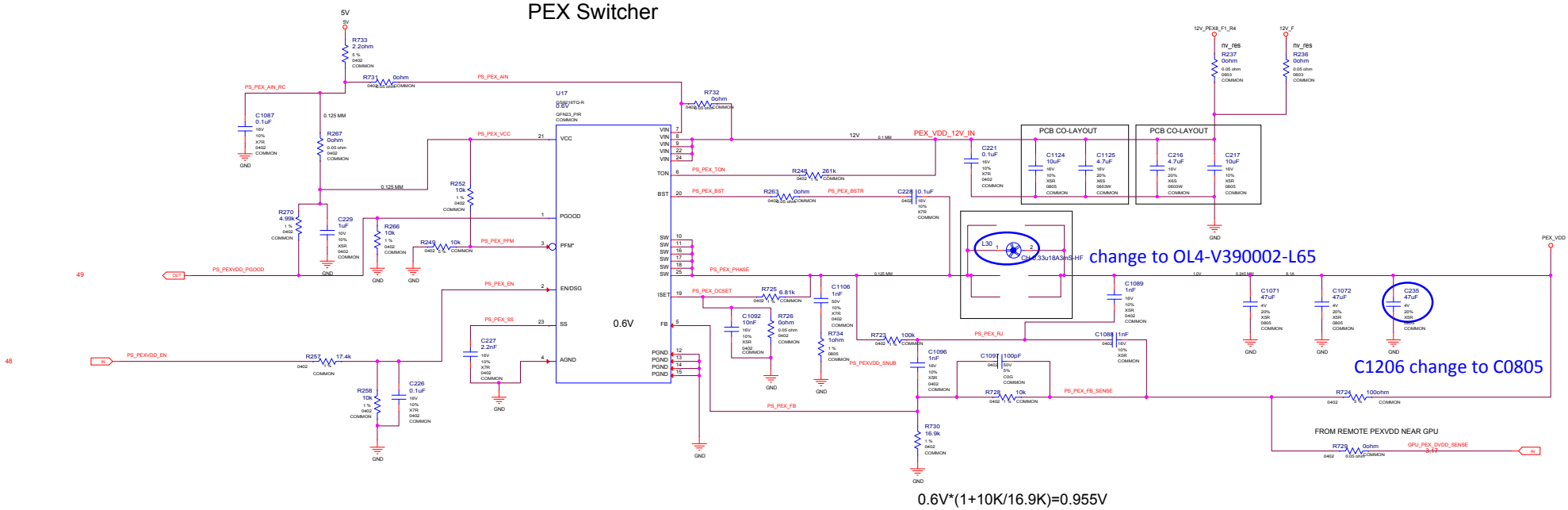
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MICRO-STAR INT'L CO.,LTD			
MS-V390			
Size	Document Description	Rev	
Custom	0030_PS_5V	2.0	
Date:	Friday, July 31, 2020	Sheet	30 of 55
NVIDIA CORPORATION			
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NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	30 OF 54
ICOM REV	A	DATE	27-JUN-2020

PEX Switcher





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MS-V390

Size	Custom	Document Description	0031_PS_PEXVDD	Rev	2.0
Date:	Friday, July 31, 2020	Sheet	31	of	55

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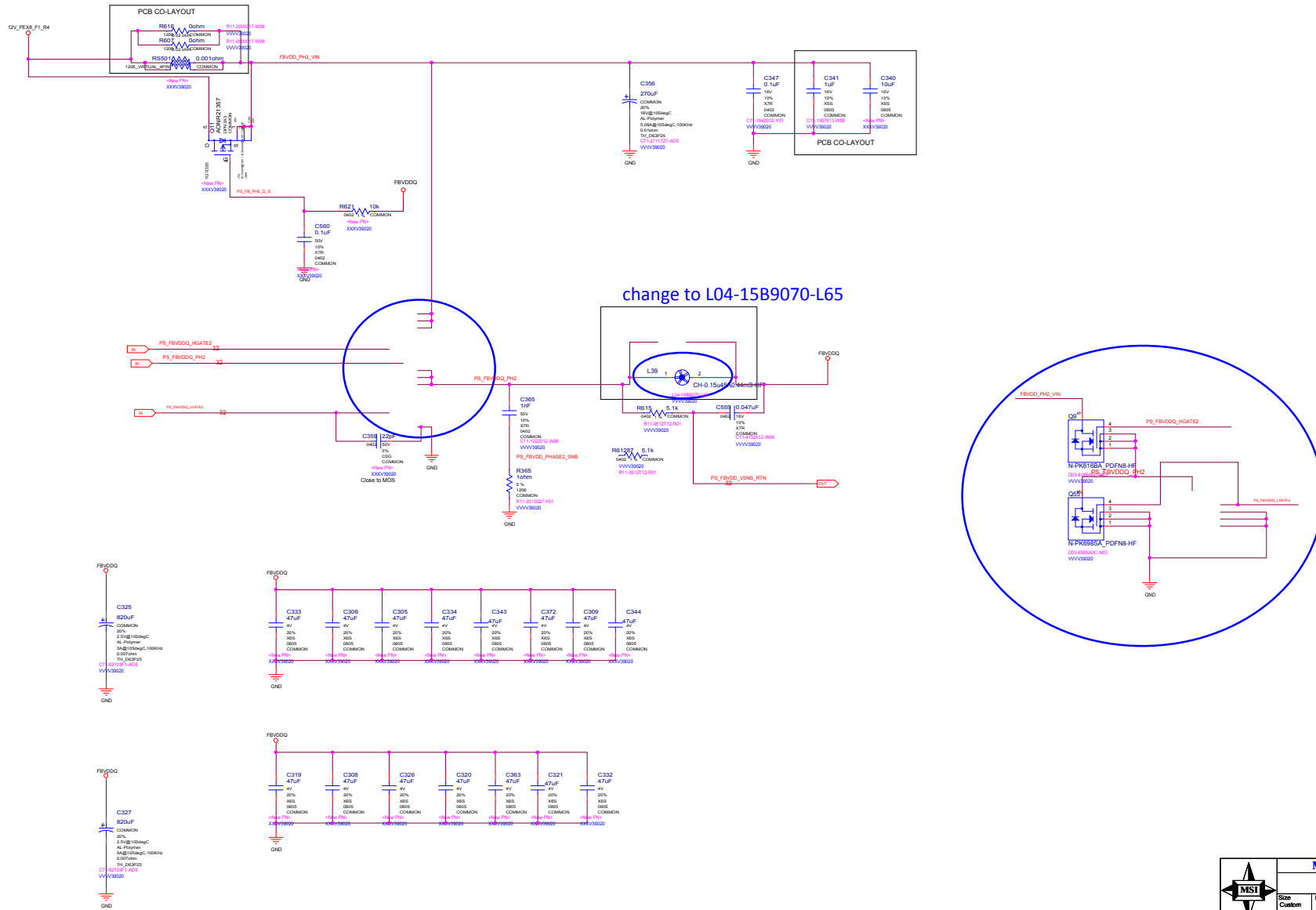


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PCB REV	PG142-B00
ICOM REV	A

PAGE	31 OF 54
DATE	27 JUN 2020

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FBVDD PH2 INPUT ANTI-BACKDRIVE



	MICRO-STAR INT'L CO.,LTD		
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	Custom	0033_PS_FBVDQ PH2	2.0
	Date: Friday, July 31, 2020		Sheet 33 of 55

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NV_PN	600-1G142-BASE-100		
PCB REV	PG142-800	PAGE	33 OF 54
ICOM REV	A	DATE	27-JUN-2020

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Size	Document Description	Rev
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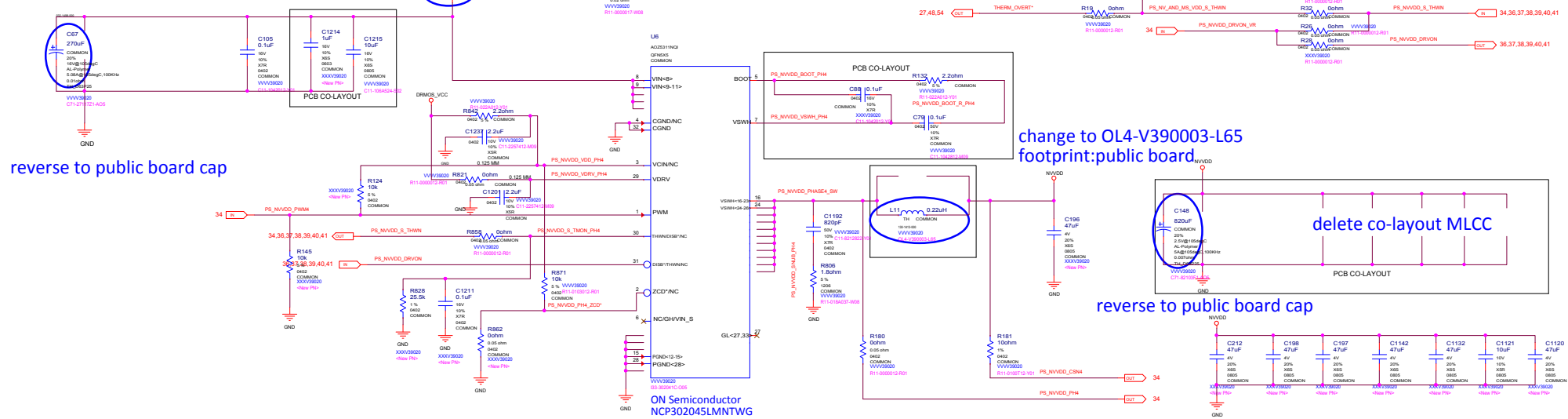


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BCM REV	A	DATE	27-JUN-2020

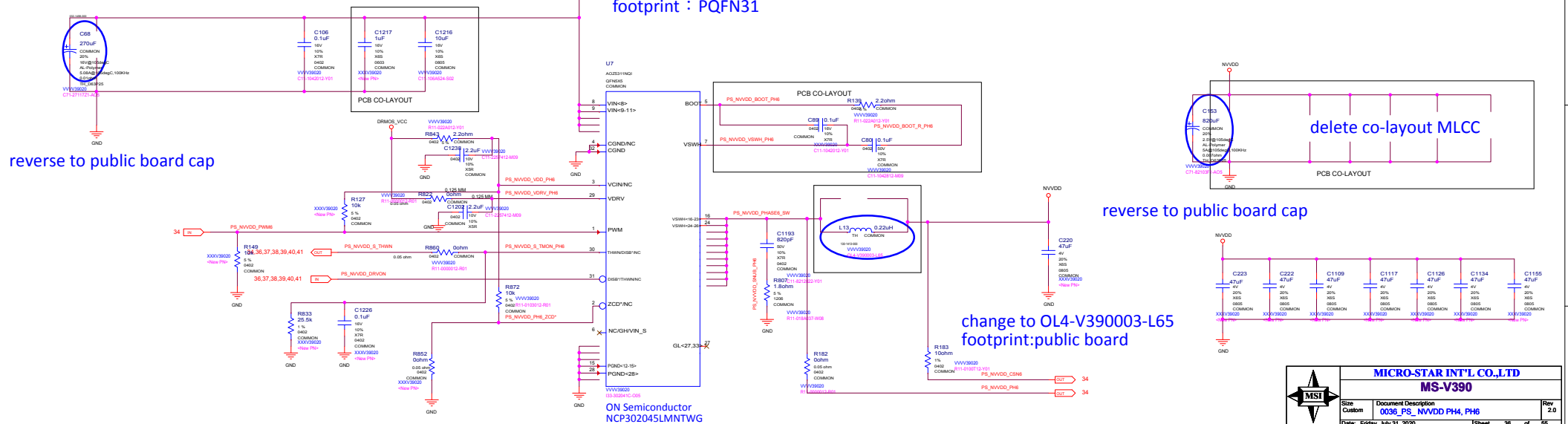
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NV_PH4_6_VIN change to 12V_PEX8_F2

NVVDD PH4(PWM4)



NVVDD PH6(PWM6)



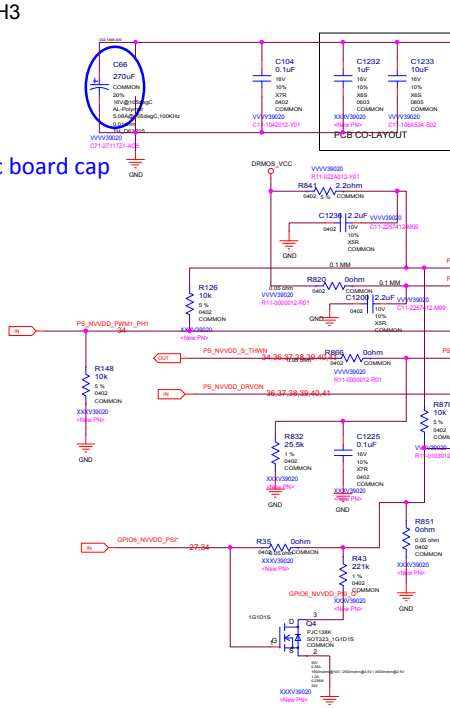
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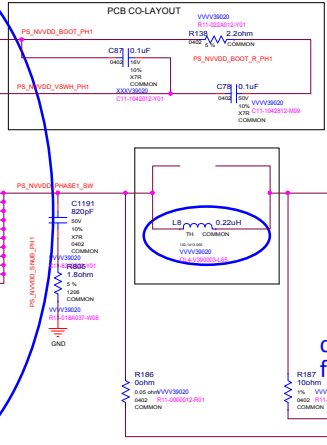
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Date:	Friday, July 31, 2020	Sheet	38 of 55
NVIDIA CORPORATION			
2701 SAN TOMAS EXPRESSWAY			
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NV_PN 600-I-G142-BASE-100			
PCB REV	PG142-B00	PAGE	38 OF 54
ICOM REV	A	DATE	27-JUN-2020

NVVDD PH1(PWM1)

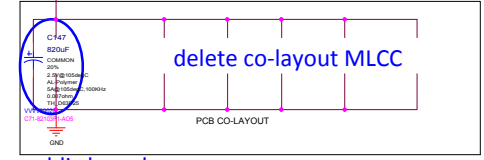
reverse to public board cap



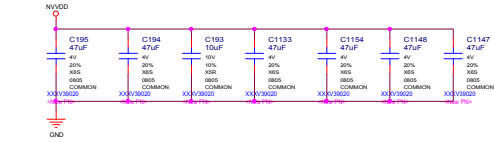
U3,U4,U5,U6,U7,U8,U9,U10,U15,U18
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footprint : PQFN31



change to OL4-V390003-L65
footprint:public board

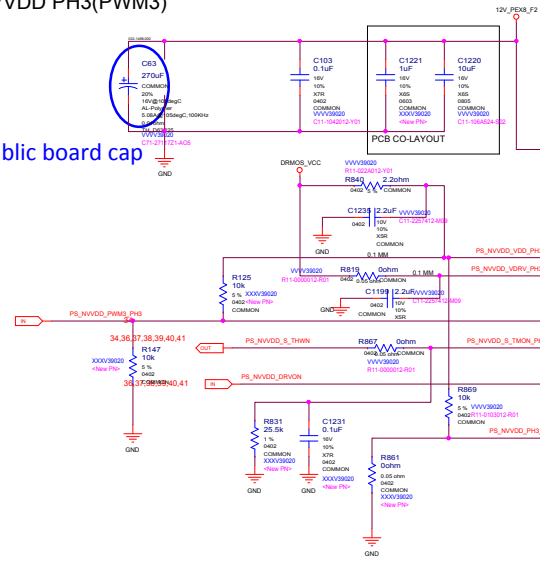


reverse to public board cap

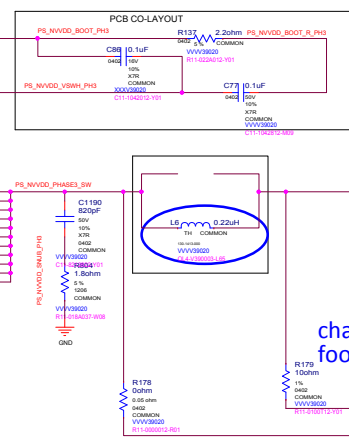


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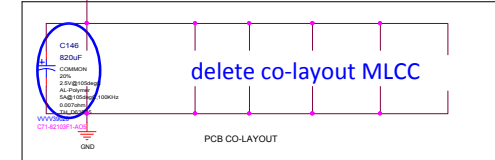
reverse to public board cap



ON Semiconductor
NCP302045LMNTWG



change to OL4-V390003-L65
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reverse to public board cap

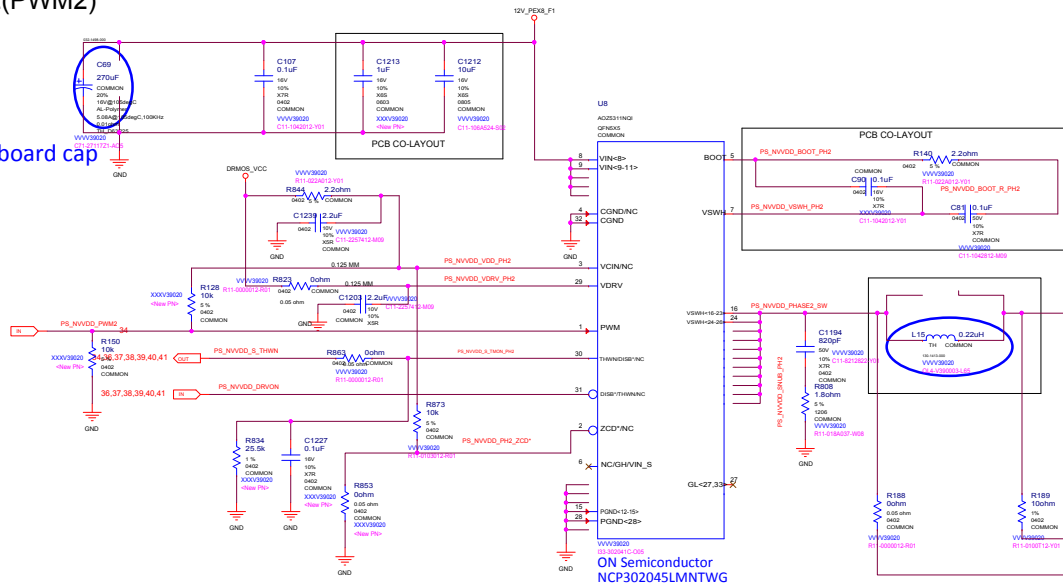
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Date:	Friday, July 31, 2020	Sheet	37 of 55
VIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
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PCB REV	PG142-800	PAGE	37 OF 54
ICOM REV	A	DATE	27-JUN-2020

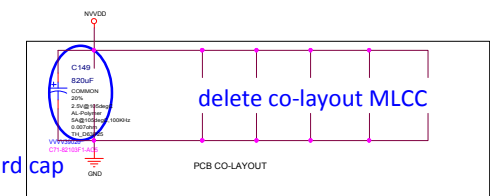
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NVVDD PH2(PWM2)

reverse to public board cap

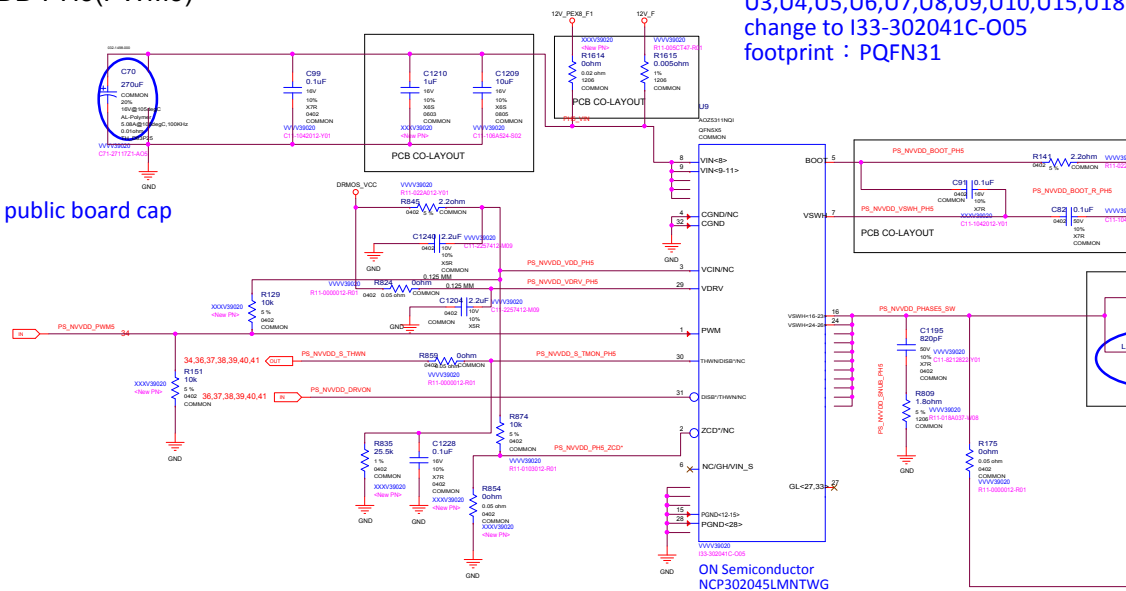


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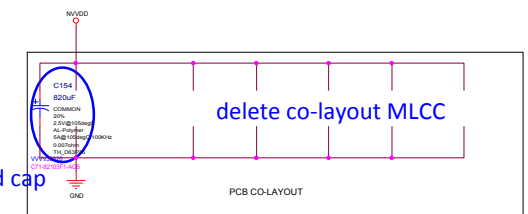
NVVDD PH5(PWM5)

reverse to public board cap



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footprint : PQFN31

reverse to public board cap

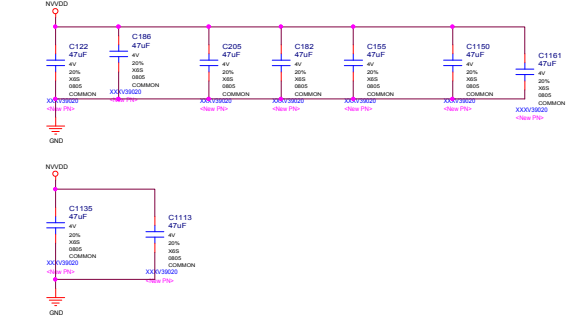
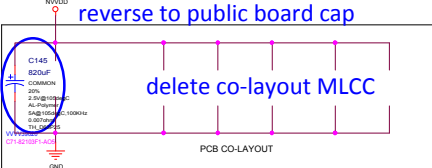
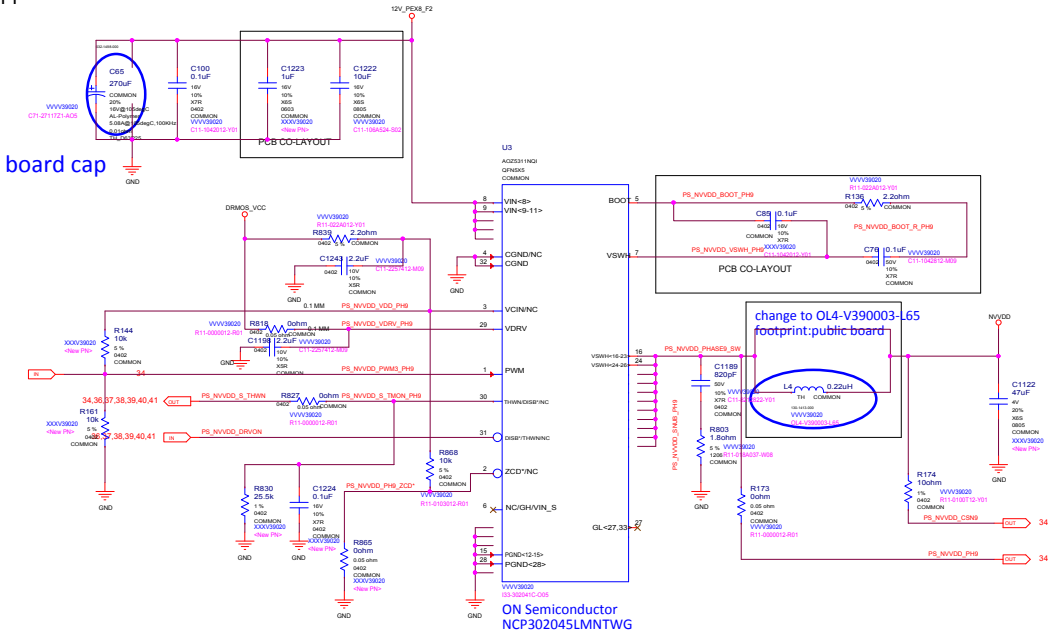


change to OL4-V390003-L65
footprint:public board

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Date:	Friday, July 31, 2020		Sheet 38 of 55
NVIDIA CORPORATION 2701 SAN TOMAS EXPRESSWAY SANTA CLARA, CA 95050, USA			
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PCB REV	PG142-800	PAGE	38 OF 54
ICOM REV	A	DATE	27-JUN-2020

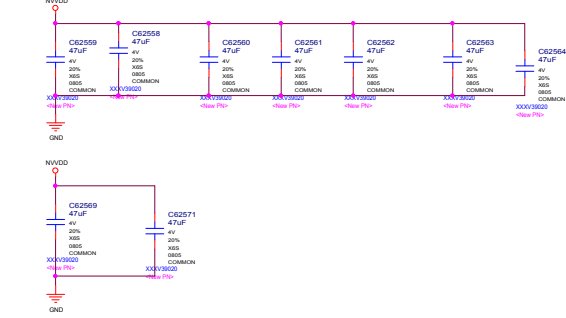
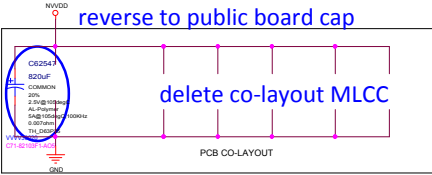
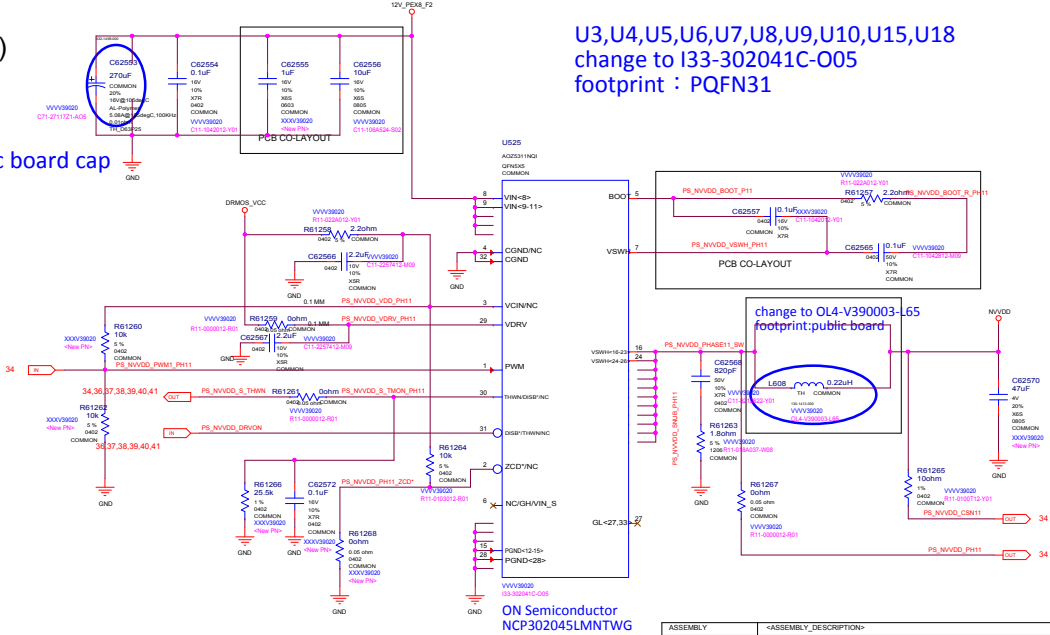
NVVDD PH9(PWM3)

reverse to public board cap



NVVDD PH11(PWM1)

reverse to public board cap



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Size	Custom	Document Description	0039 PS_NVVDD PH9, PH11	Rev	2.0
Date:	Friday, July 31, 2020			Sheet	39 of 55

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NV_PN	600-1G142-BASE-100
PCB REV	PG142-800
ICOM REV	A
PAGE	39 OF 54
DATE	27-JUN-2020

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NVVDD PH7(PWM7)

reverse to public board cap

reverse to public board cap

delete co-layout MLCC

change to OL4-V390003-L65
footprint:public board

ON Semiconductor
NCP302045LMNTWG

U3,U4,U5,U6,U7,U8,U9,U10,U15,U18
change to I33-302041C-O05
footprint : PQFN31

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Size	Custom	Document Description	0040_PS_NVVDD PH7	Rev	2.0
Date:	Friday, July 31, 2020	Sheet	40	of	55



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NV_PN 600-1G142-BASE-100
PCB REV PG142-B00
BOM REV A

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS_NVVDD PH7

PCB REV	PG142-B00	PAGE	40 OF 54
BOM REV	A	DATE	27-JUN-2020

reverse to public board cap

reverse to public board cap

delete co-layout MLCC

change to OL4-V390003-L65
footprint:public board

NVVDD PH8(PWM8)

reverse to public board cap

delete co-layout MLCC

reverse to public board cap

change to OL4-V390003-L65
footprint:public board

U3,U4,U5,U6,U7,U8,U9,U10,U15,U18
change to I33-302041C-O05
footprint : PQFN31

ON Semiconductor
NCP302045LMNTWG

ON Semiconductor
NCP302045LMNTWG



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Size: Custom

Document Description: 0041_PS_NVDD PH10, PH8

Date: Friday, July 31, 2020

Rev: 2.0

Sheet: 41 of 55



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NV_PN 600-1G142-BASE-100

PCB REV PG142-B00

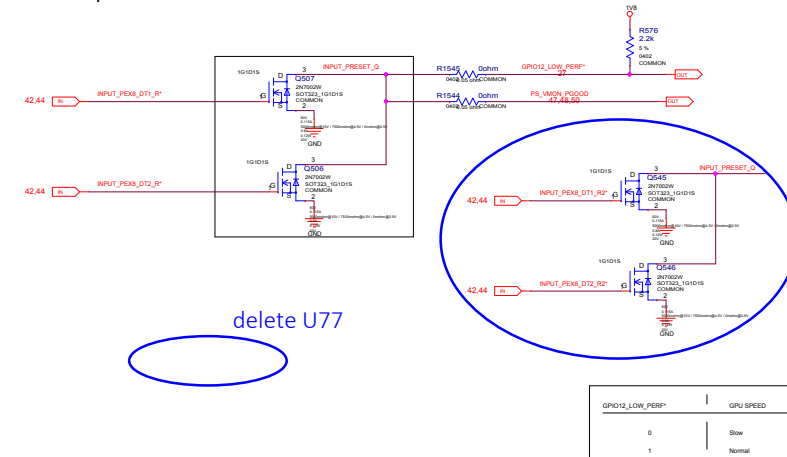
ICOM REV A

PAGE 41 OF 54

DATE 27-JUN-2020

delete 12 pin 12V EXT-POWER Current steering

PEX Input - Under Power Boot Control



delete U77

PEX8 INPUT 2/B - 2x4 PCIE CON 150W

Fuse

PCB CO-LAYOUT

F7 FUSE 2A 5610269-HF

12.5A

delete R2007

Fuse

PCB CO-LAYOUT

F9 FUSE 2A 5610269-HF

12.5A

delete R2010

PEX8 INPUT 1/A - 2x4 PCIE CON 150W

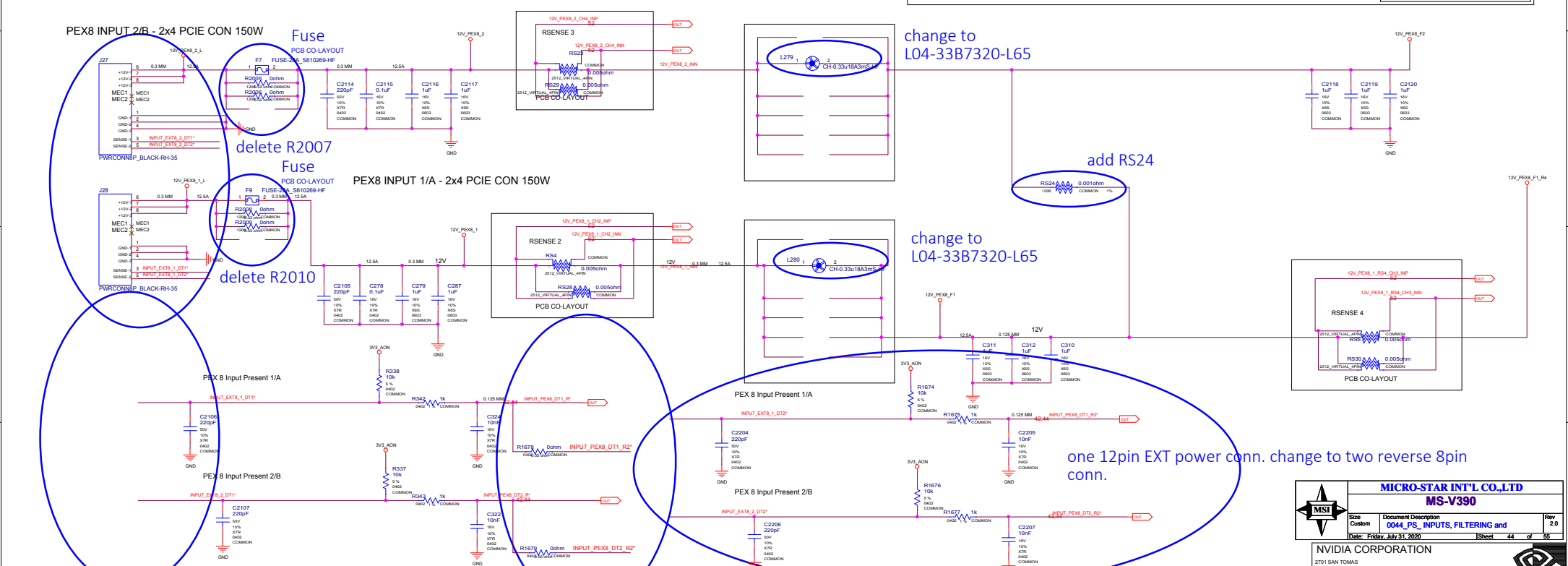
delete R2010

change to L04-33B7320-L65

add RS24

change to L04-33B7320-L65

one 12pin EXT power conn. change to two reverse 8pin conn.



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Size	Document Description	Rev	
Custom	0044_P8_INPUTS, FILTERING and	2.0	
Date:	Friday, July 31, 2020	Sheet	44 of 55
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NV_PN	600-1G142-BASE-100		
PCB REV	PG142-800	PAGE	44 OF 54
ICOM REV	A	DATE	27-JUN-2020

POWER CONNECTOR HOT-UNPLUG DETECT

delete POWER CONNECTOR HOT-UNPLUG DETECT

12V CURRENT STEERING (UNDER POWER BOOT):

GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA

delete 12V CURRENT STEERING

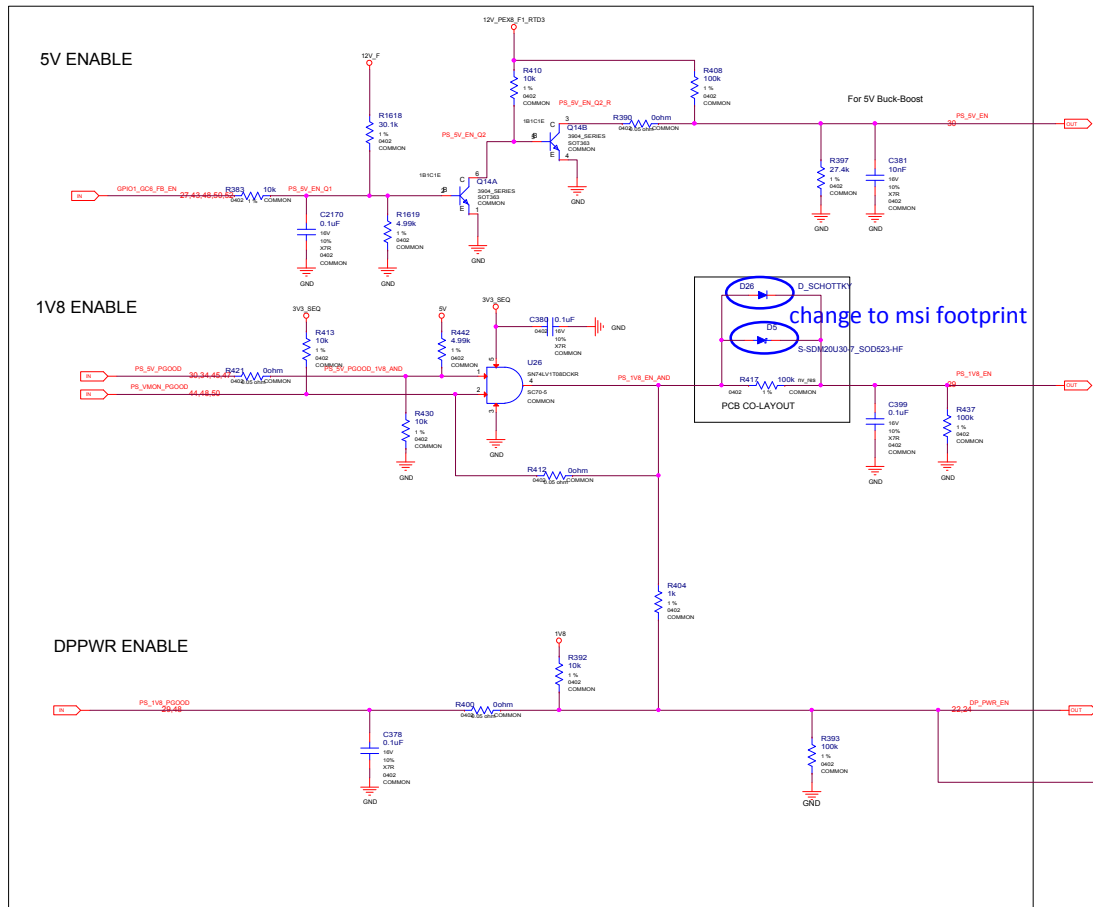
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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: STEERING, UPB, HOT UNPLUG



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Size	Document Description	Rev	
Custom	0046_PS_STEERING, UPB, HOT UNP	2.0	
Date: Friday, July 31, 2020		Sheet 46 of 56	

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NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	46 OF 54
BOM REV	A	DATE	27-JUN-2020

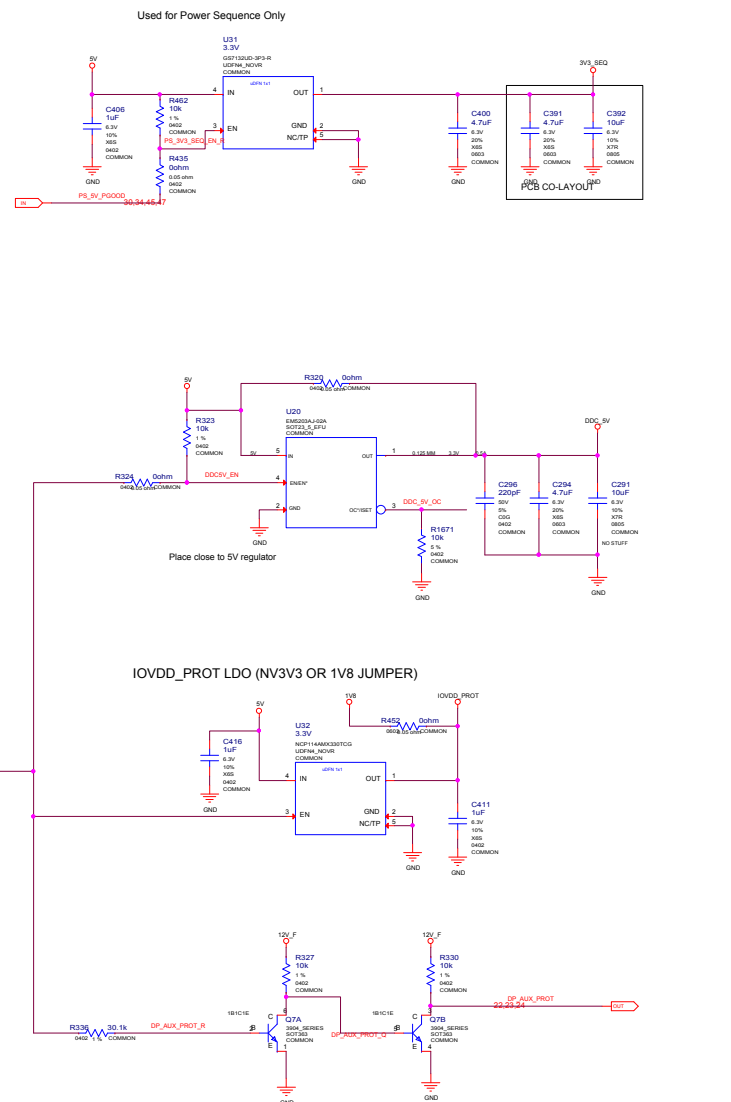


3V3_SEQ

DDC_5V

IOVDD_PROT

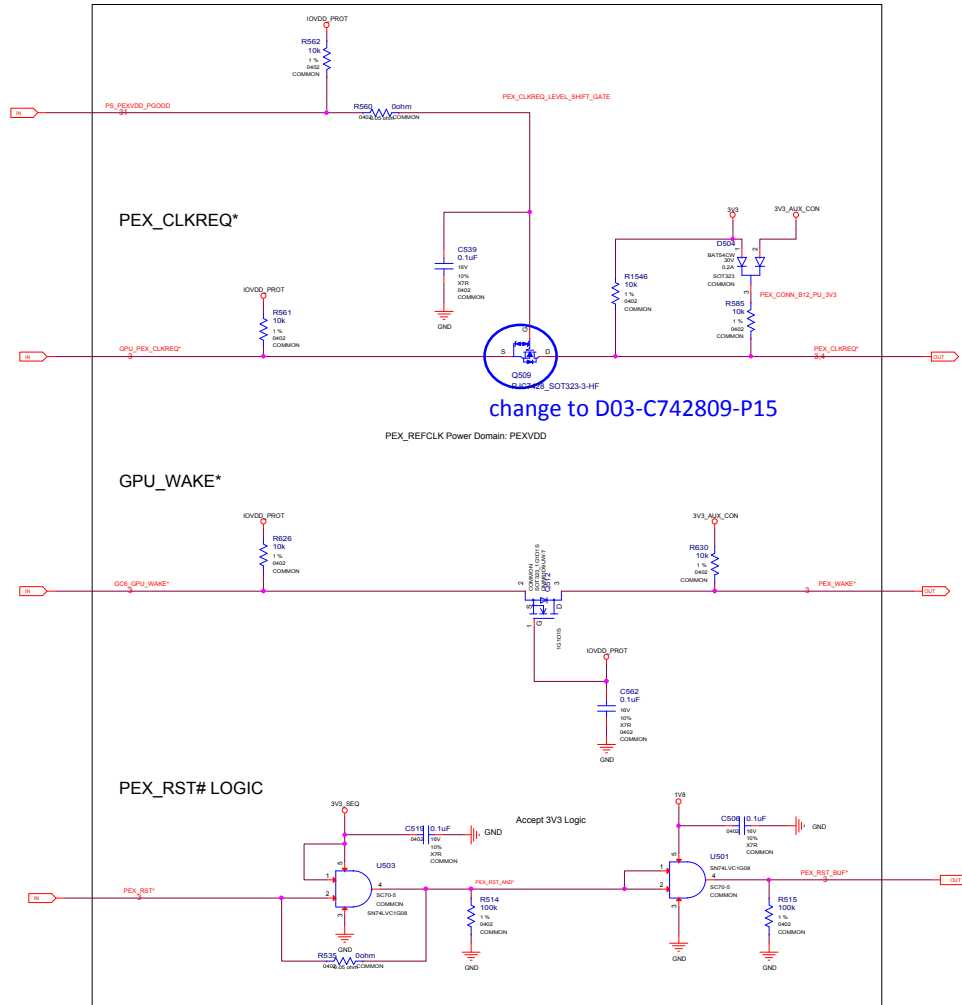
DP_AUX PROTECTION



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Size	Custom	Document Description	0047_SEQ_5V, 1V8, 3V3_SEQ
Date:	Friday, July 31, 2020	Sheet	47 of 56

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NV_PN	600-1G142-BASE-100		
PCB REV	PG142:800	PAGE	47 OF 54
ICOM REV	A	DATE	27 JUN 2020

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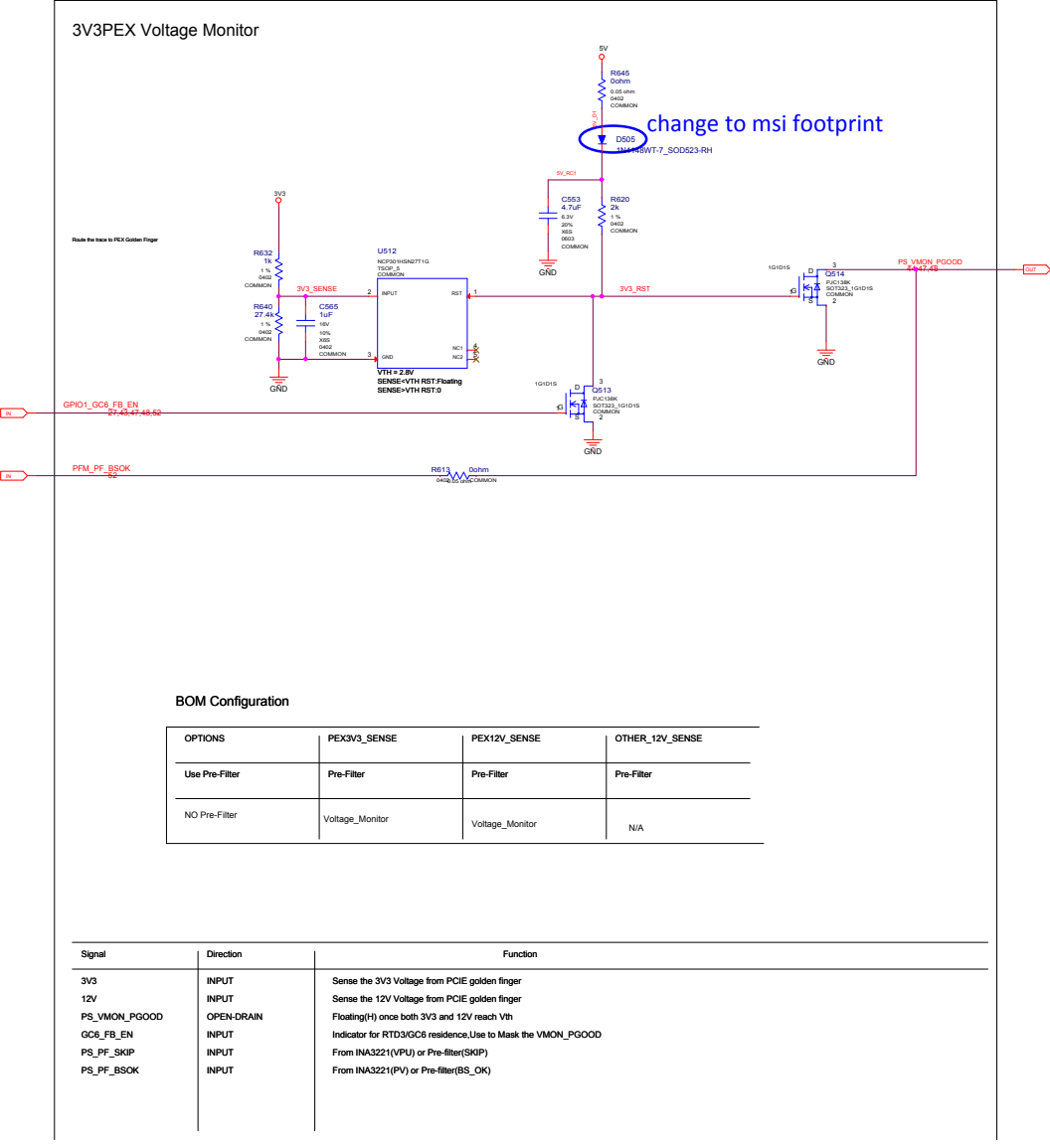
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MS-V390			
Size	Document Description	Rev	
Custom	0049_SEQ_MISC	2.0	
Date: Friday, July 31, 2020		Sheet	48 of 56

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NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	49 OF 54
BOM REV	A	DATE	27-JUN-2020

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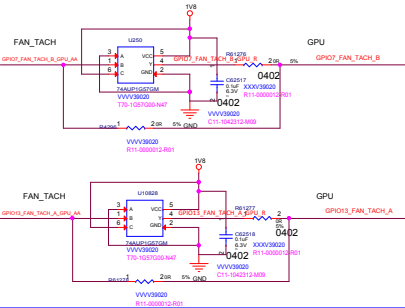
Size	Custom	Document Description	0050_SEQ_VOLTAGE MONITOR	Rev	2.0
Date:	Friday, July 31, 2020	Sheet	60	of	66

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NV_PN	600-1G142-BASE-100
PCB REV	PG142-B00
BOM REV	A
PAGE	50 OF 64
DATE	27-JUN-2020

2-PIN LED HEADER
remove 2-PIN LED HEADER

copy from V388-2.0



footprint:TOWS_SIP4_2MM_1

J15在J16的左邊,白色接口。

delete J502

footprint:TOWS_SIP4_2MM_1

J16在J15的右邊,黑色接口。

delete J501

DUAL FAN 4-PIN HEADERS

change to D01-AT54C49-LA9

R_3 change to R5101

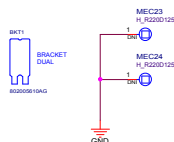
R_1 change to R5102

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MS-V390
Size: Custom
Document Description: 0051_FAN & LED
Date: Friday, July 31, 2020
Sheet: 51 of 55

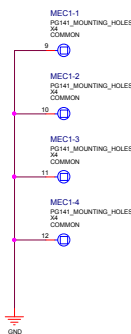
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NV_PN: 600-1G142-BASE-100
PCB REV: PG142-B00
BOM REV: A
PAGE: 51 OF 54
DATE: 27-JUN-2020

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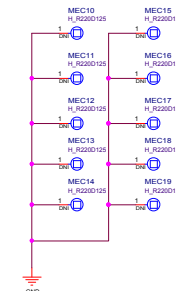
Bracket & Bracket hole: 2pcs
footprint:H_R220D125



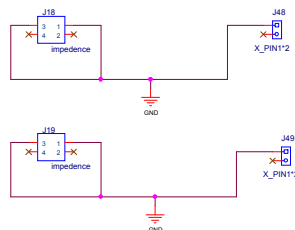
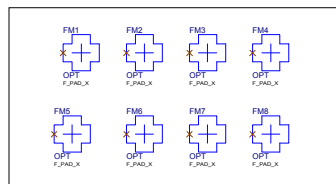
Fan module hole: 4 pcs
footprint : same as public board



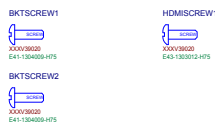
Fan module hole: 10 pcs
footprint:H_R220D125



删除CLP1~CLP3

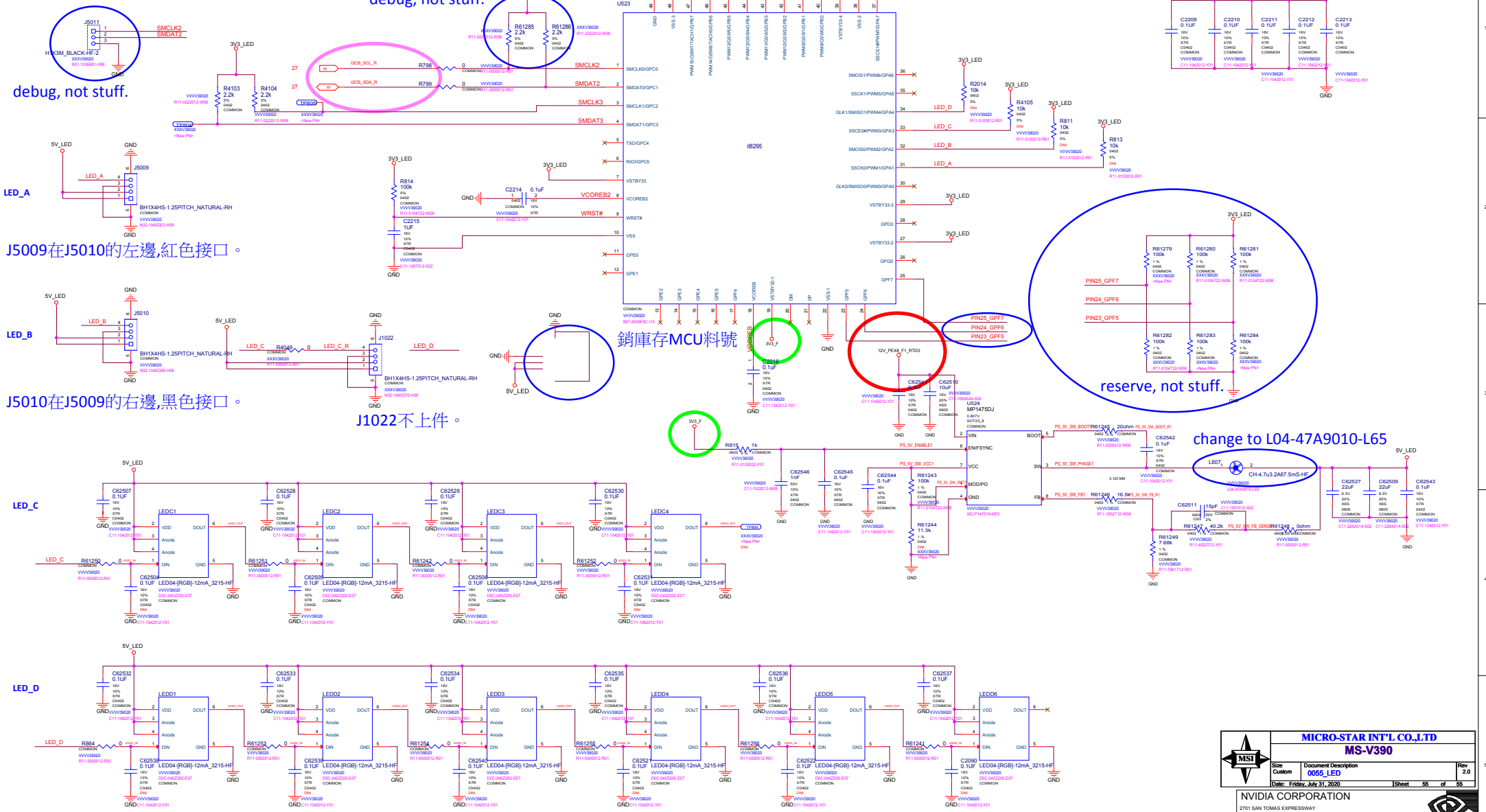


Bracket Screw



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Size	Document Description	Rev	2.0
Custom	0053_MECH		
Date: Friday, July 31, 2020	Sheet	53	of 55
NVIDIA CORPORATION			
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NV_PN	600-1G142-BASE-100		
PCB REV	PG142-B00	PAGE	53 OF 54
ROM REV	A	DATE	27-JUN-2020

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PAGE DETAIL		PS_NVVD Controller	

NV_PN		600-1G142-BASE-100	
PCB REV		PG142-800	
BOM REV		A	
PAGE		34 OF 54	
DATE		27 JUN 2020	

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