# PG142-B00

# DP + DP + DP + HDMI/DP

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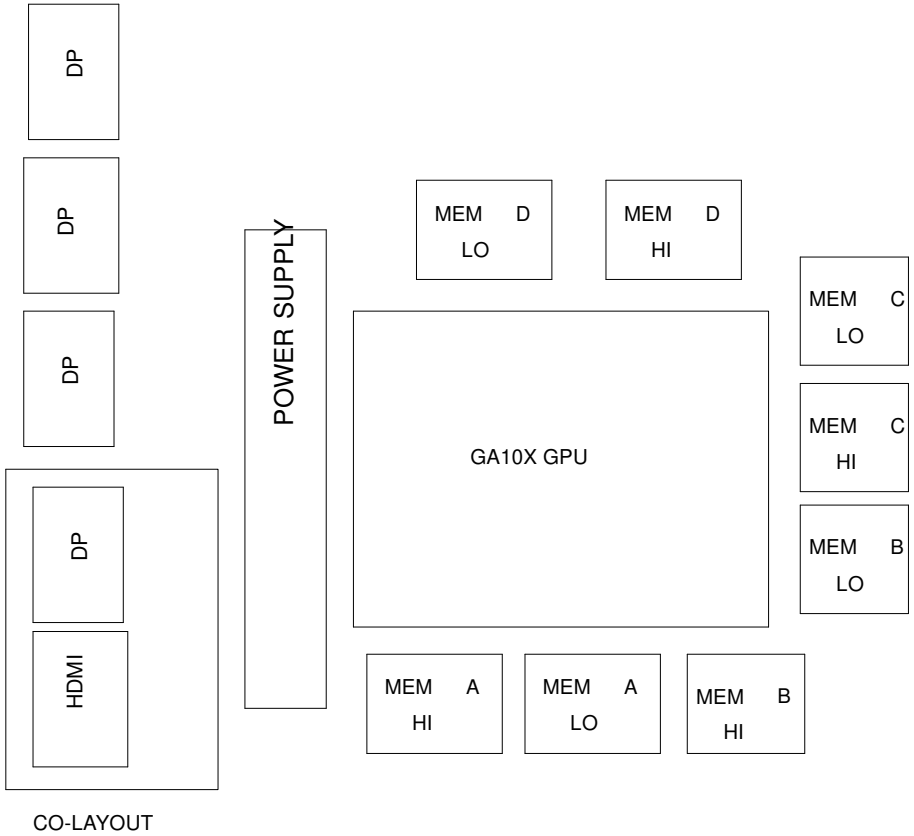
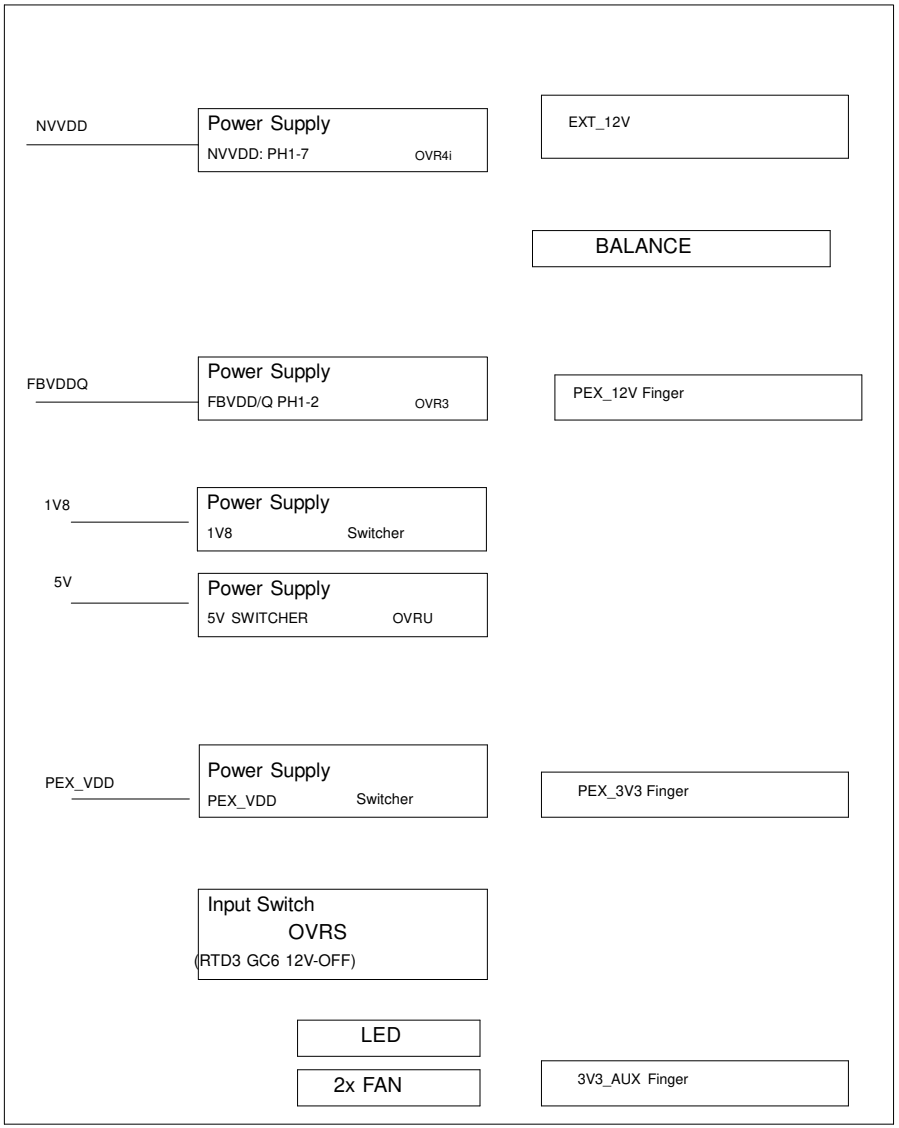
Page2: Block Diagram

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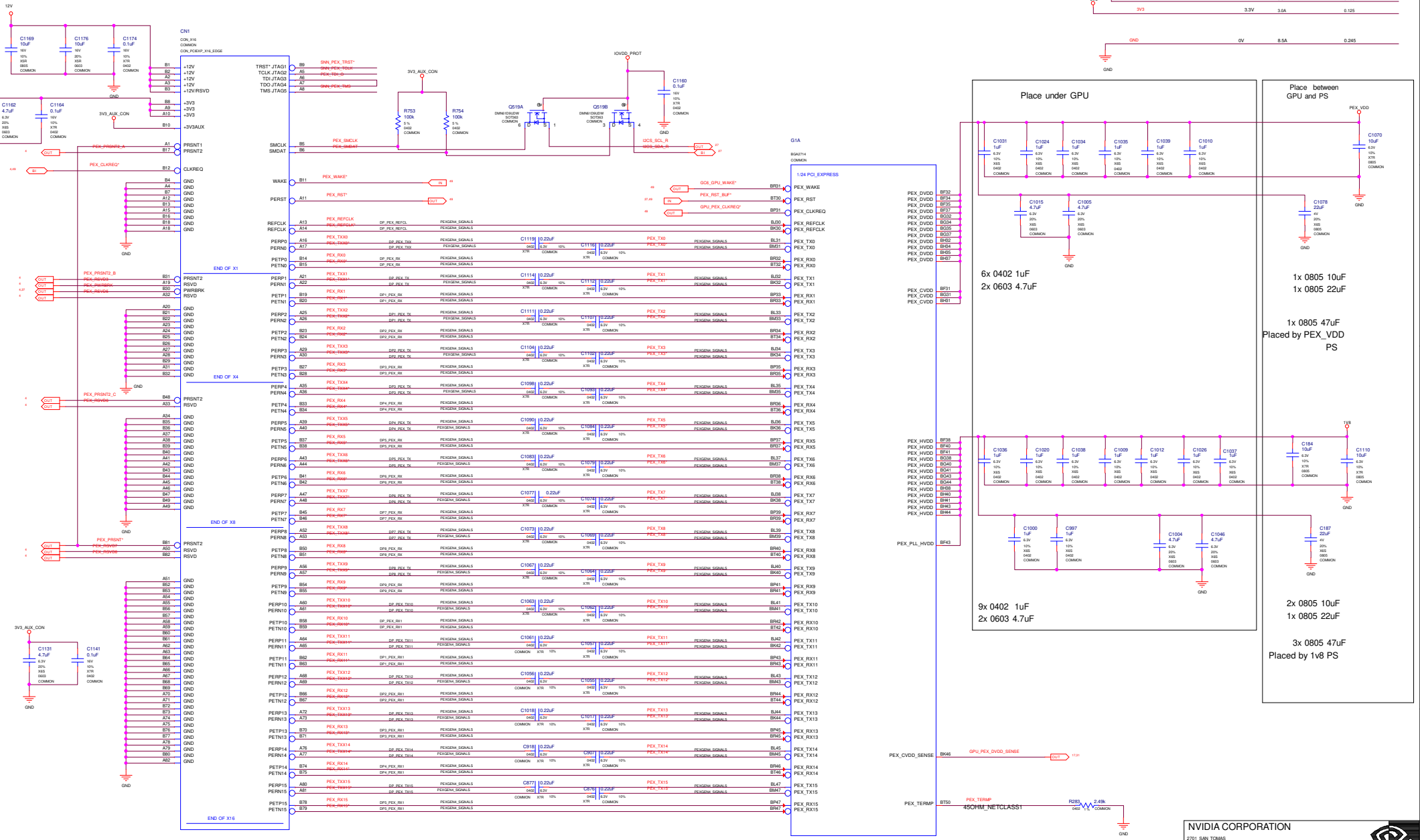
# Page3: PCI Express

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# Page4: PCIE GEN4 RC TERMINATIONS

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# Page5: MEMORY: GPU Partition A/B

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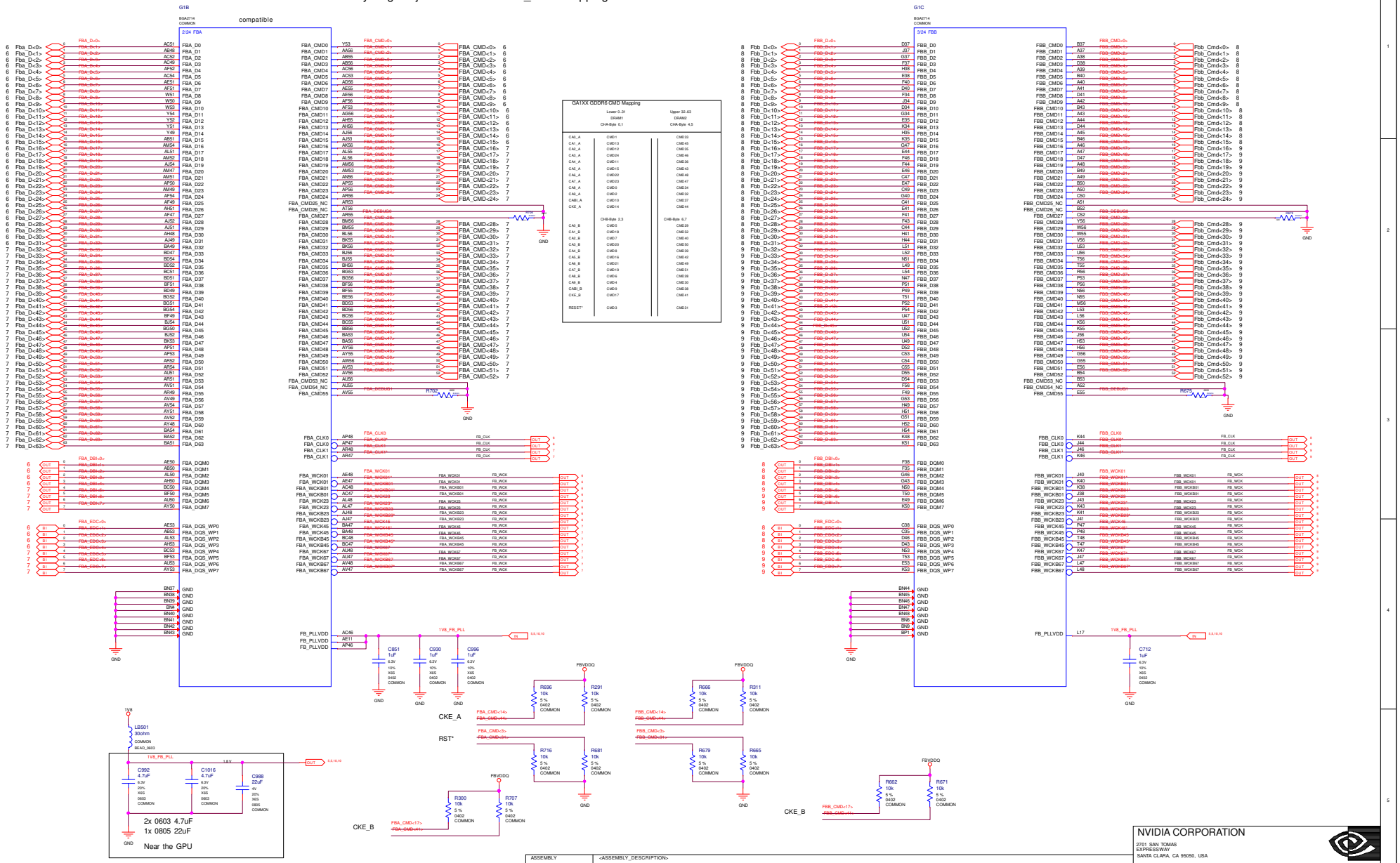


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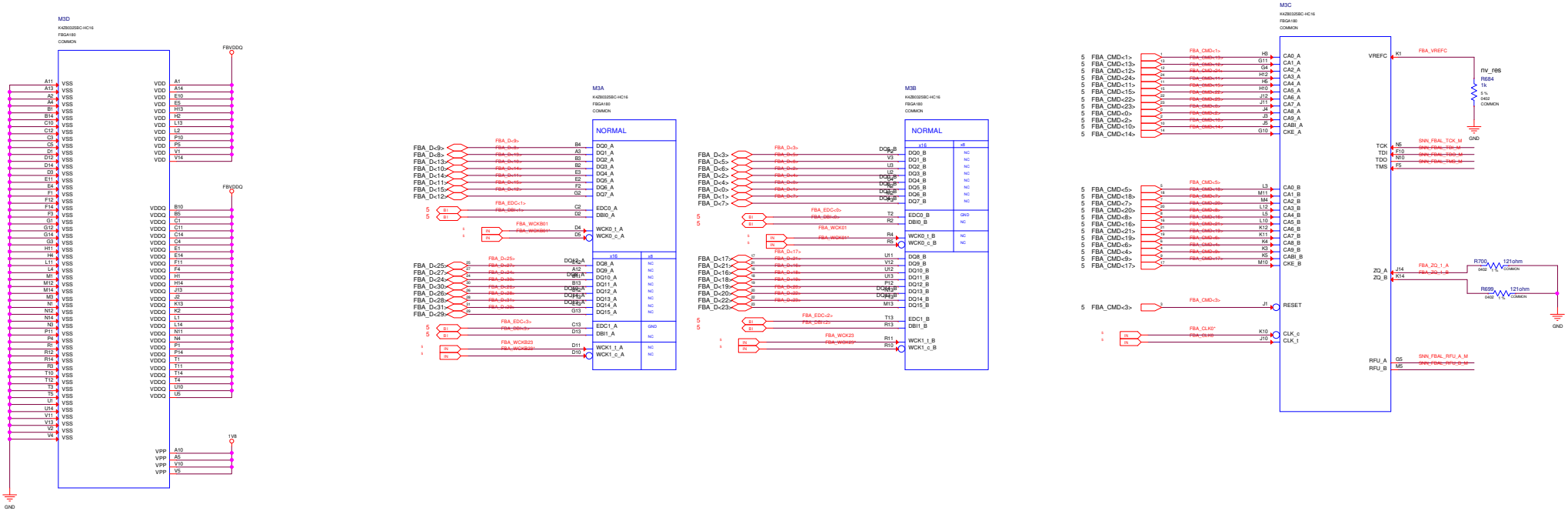
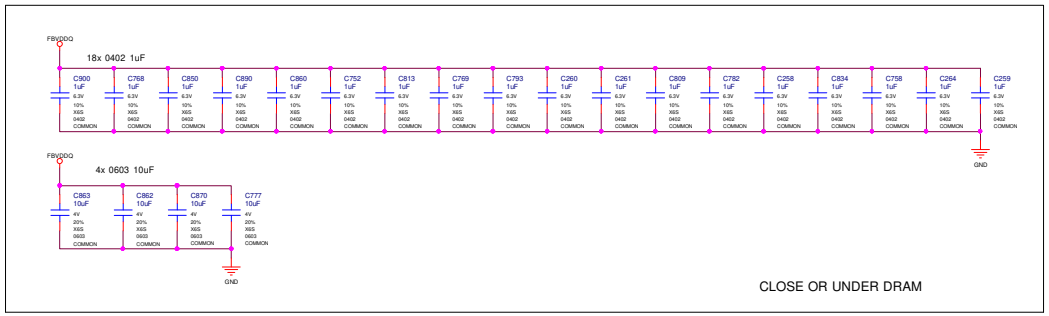
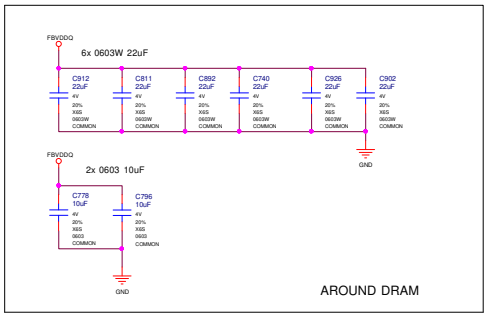
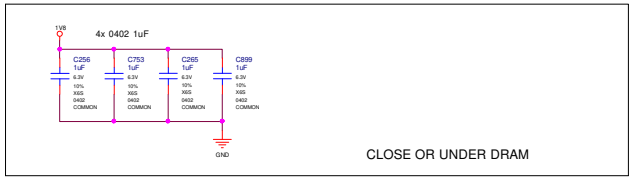
# Page6: MEMORY: FBA Partition 31..0




decap via : at least 2 gnd vias and 2 power vias for each cap

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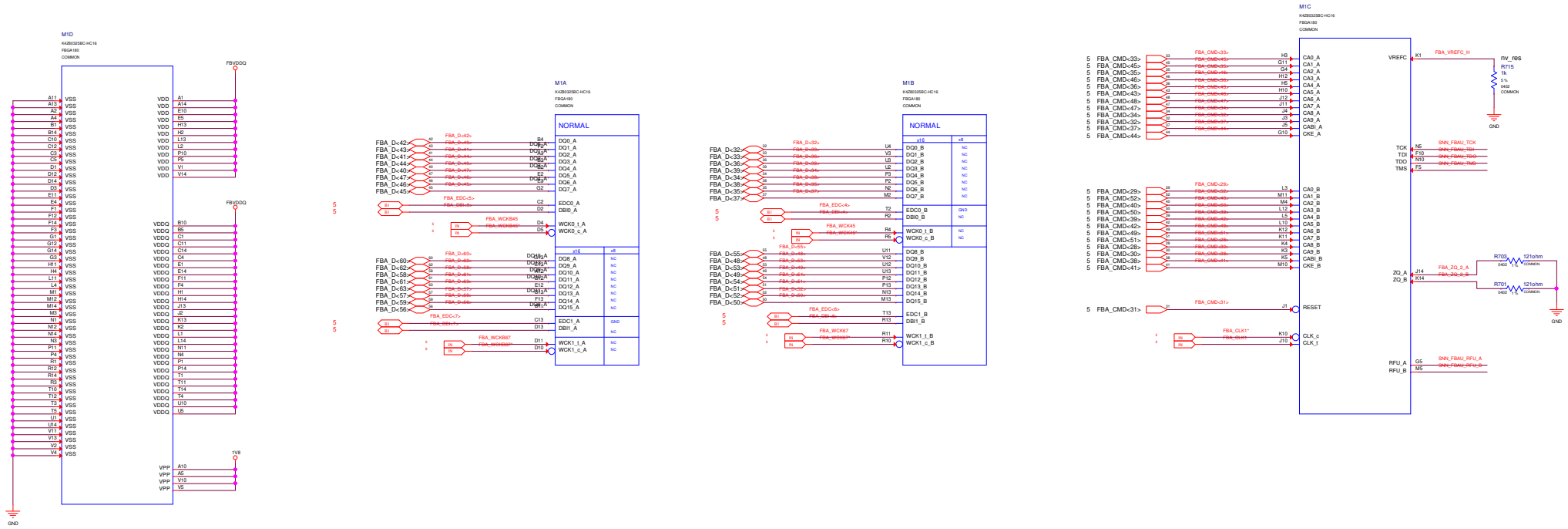
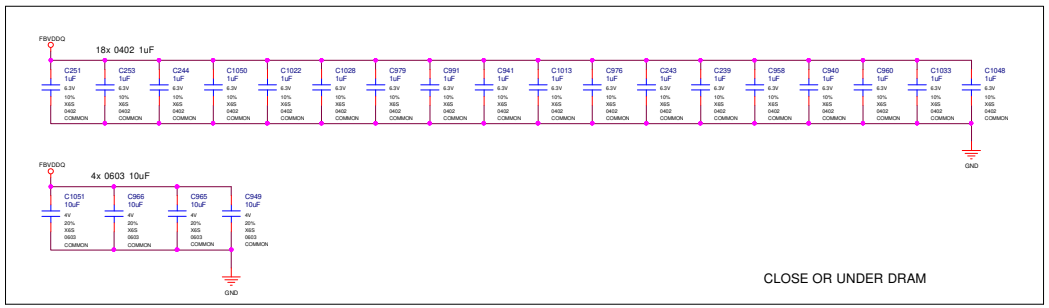
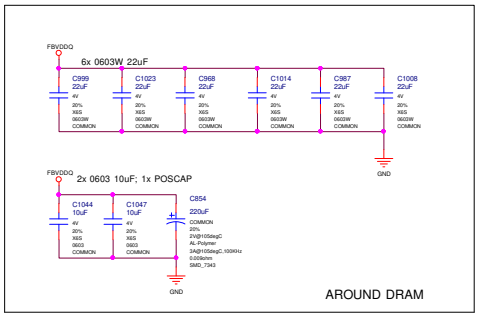
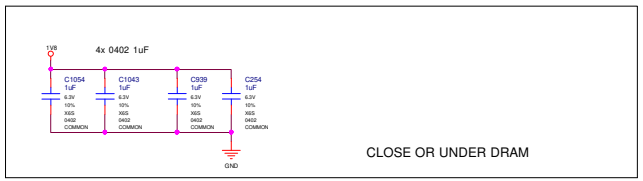
# Page7: MEMORY: FBA Partition 63..32

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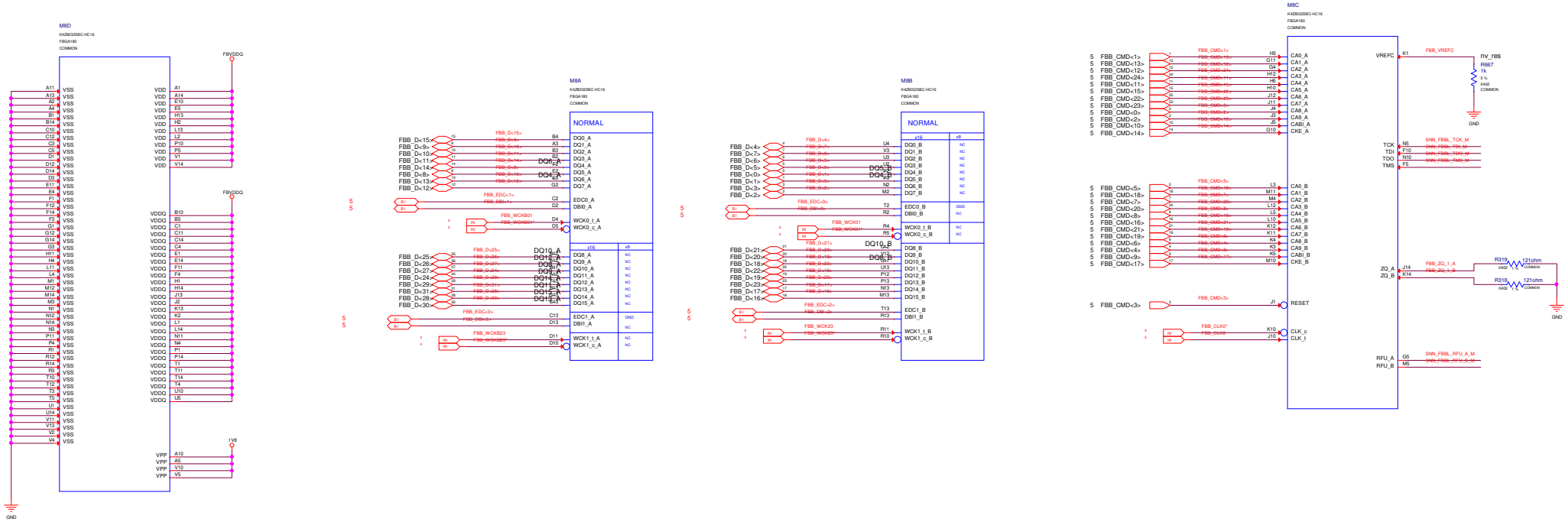
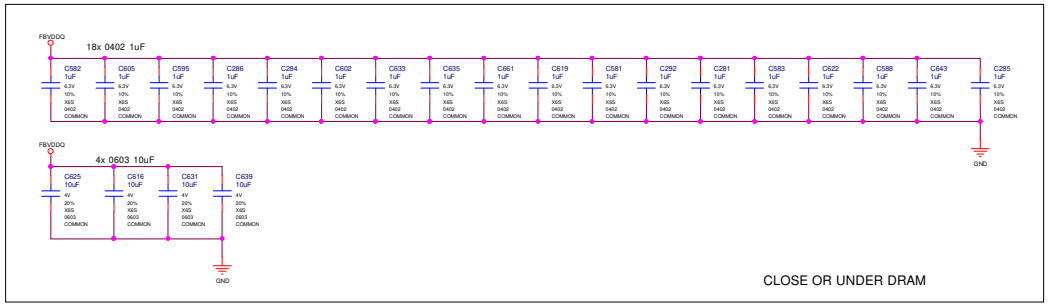
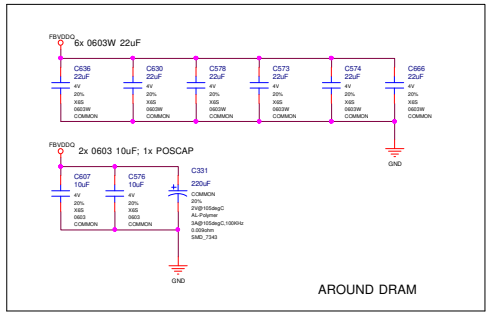
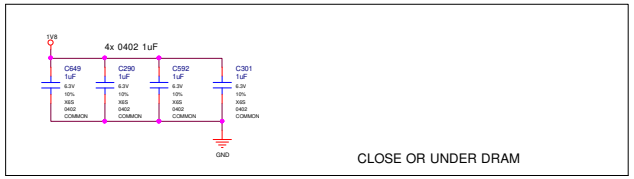
# Page8: MEMORY: FBB Partition 31..0

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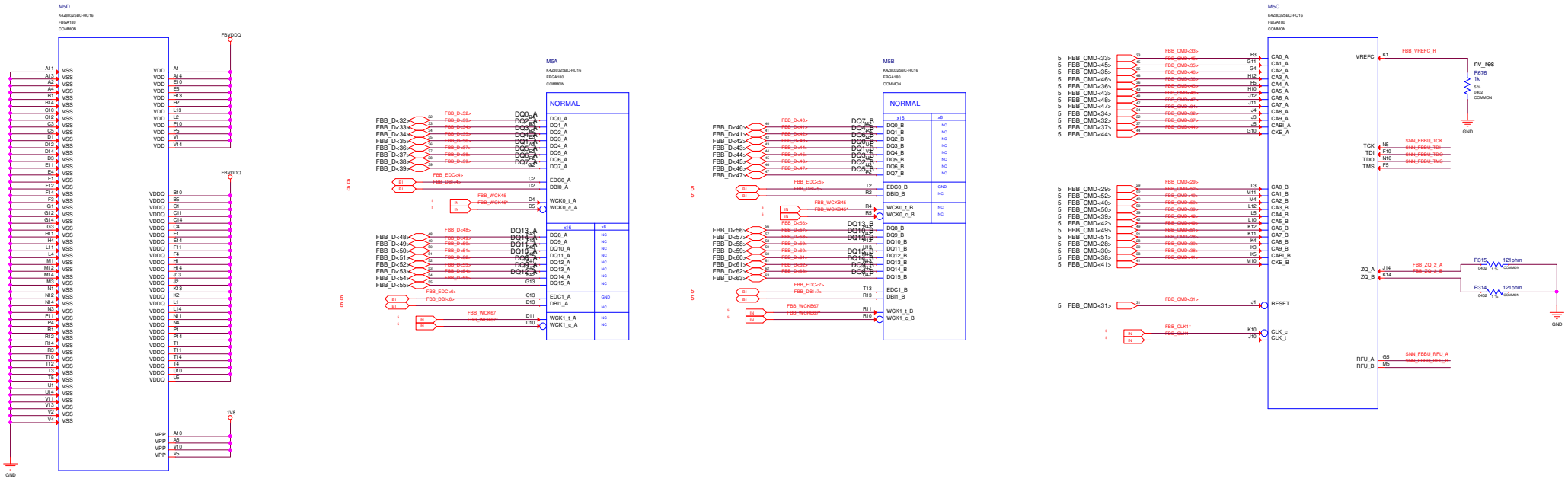
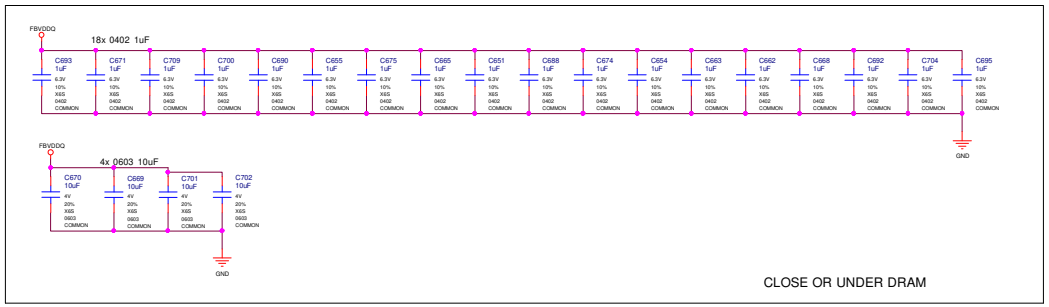
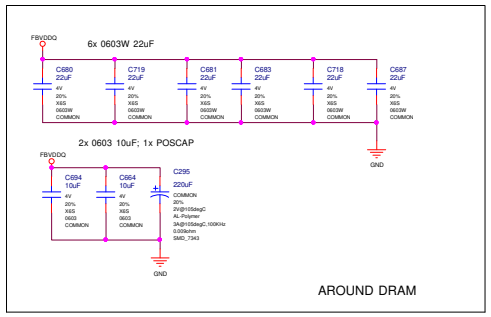
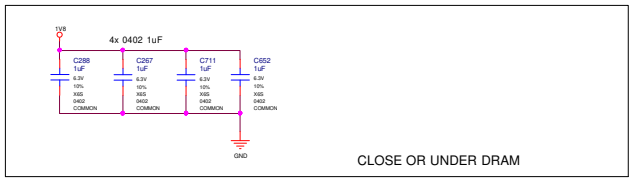
# Page9: MEMORY: FBB Partition 63..32

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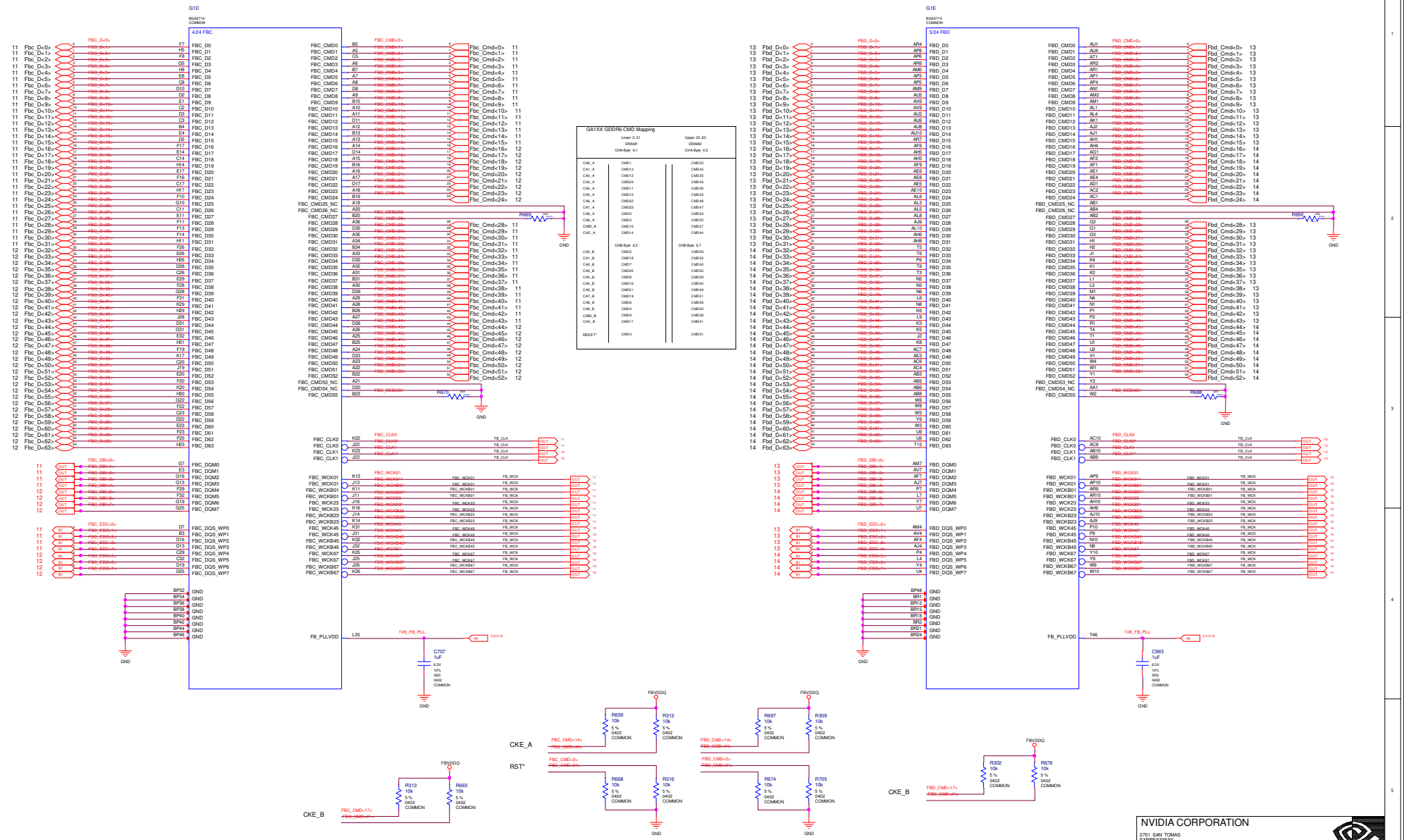
# Page10: MEMORY: GPU Partition C/D

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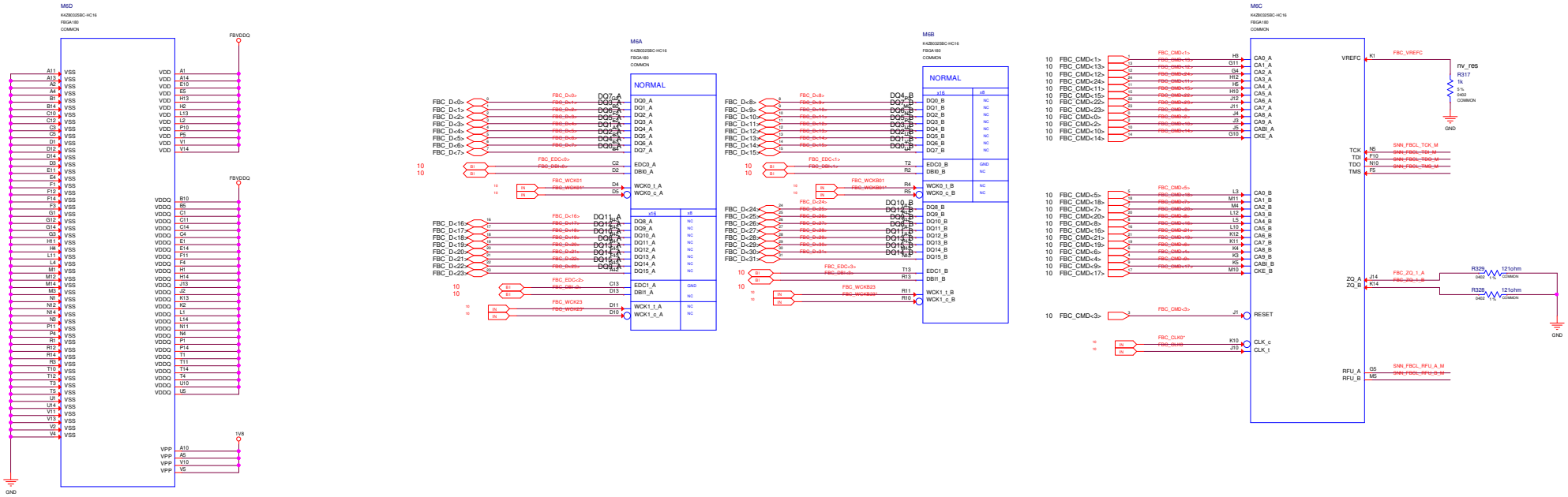
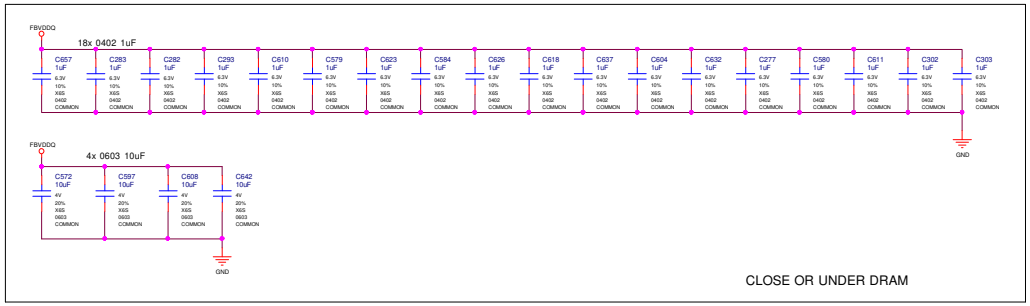
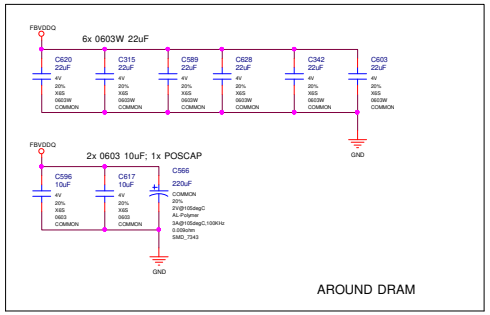
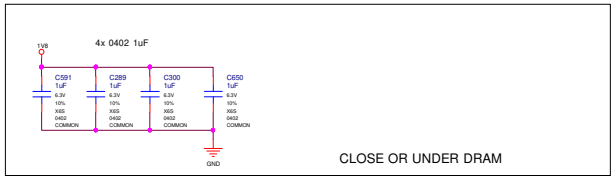
# Page11: MEMORY: FBC Partition 31..0

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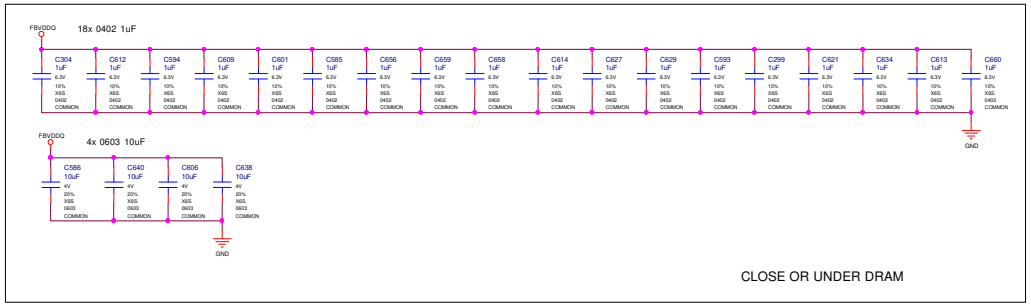
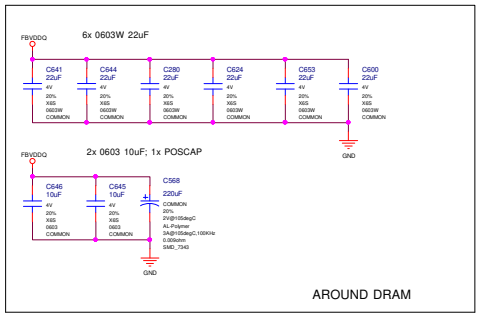
# Page12: MEMORY: FBC Partition 63..32




CLOSE OR UNDER DRAM

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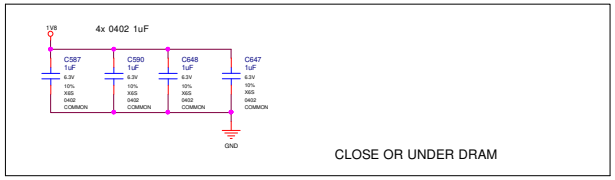


CLOSE OR UNDER DRAM

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| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | MEMORY: FBC[63:32] |

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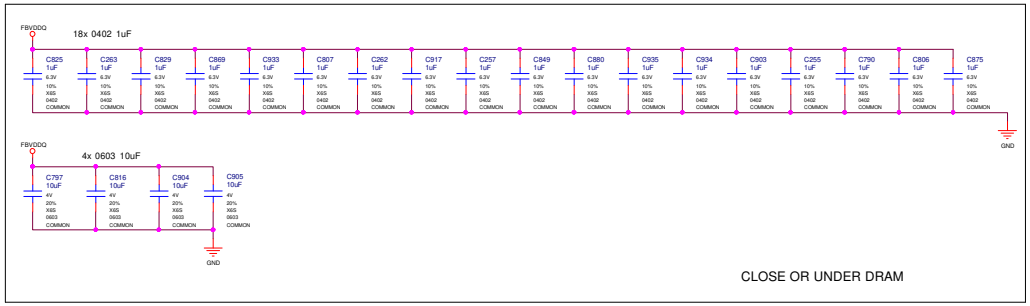
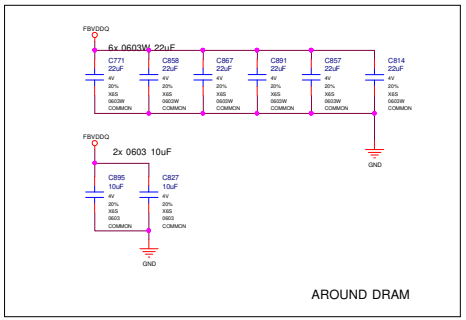
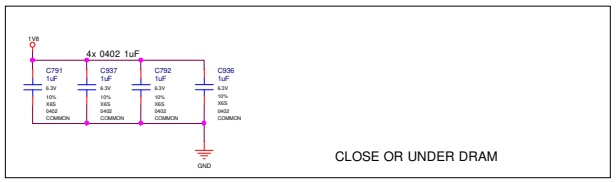
# Page13: MEMORY: FBD Partition 31..0




CLOSE OR UNDER DRAM




AROUND DRAM




CLOSE OR UNDER DRAM

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| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
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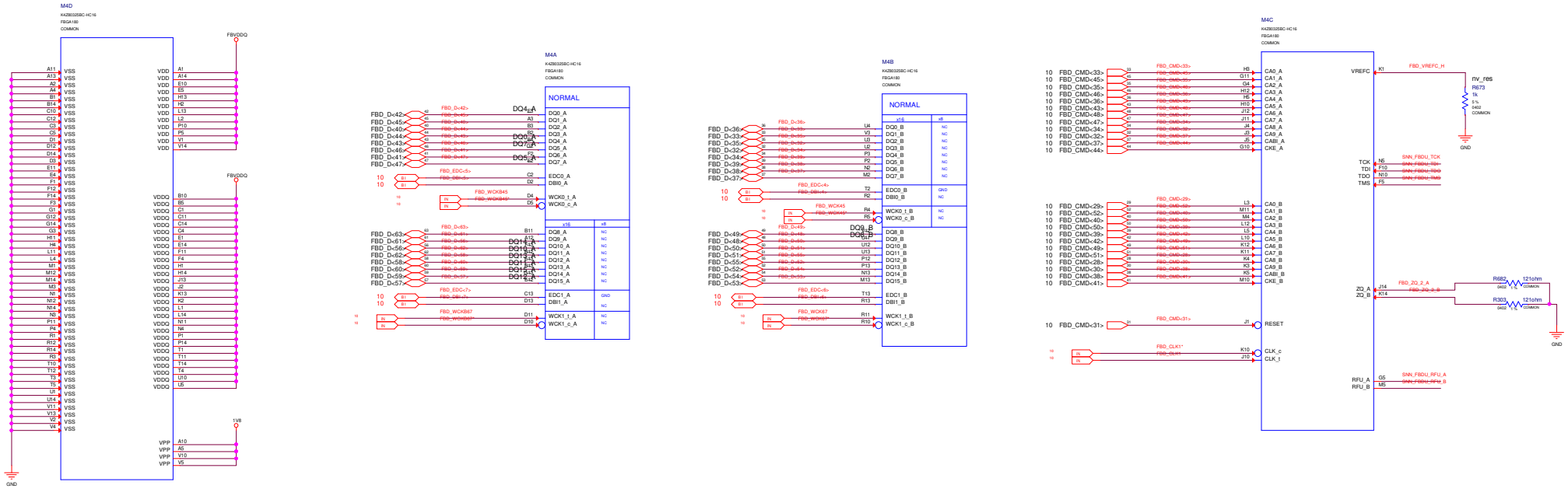
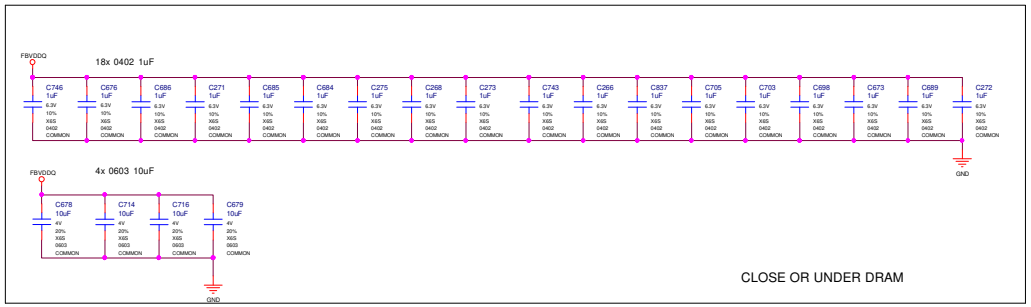
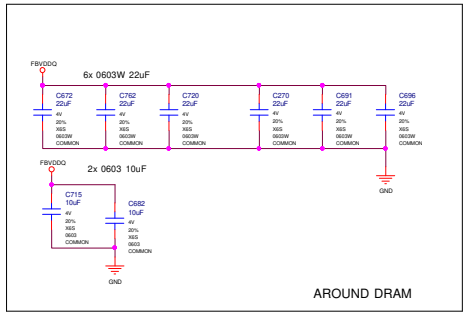
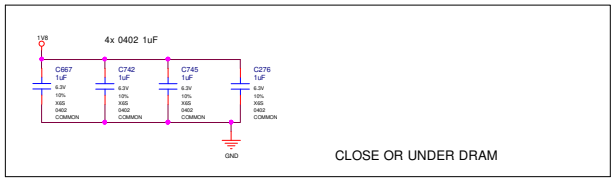
# Page14: MEMORY: FBD Partition 63..32

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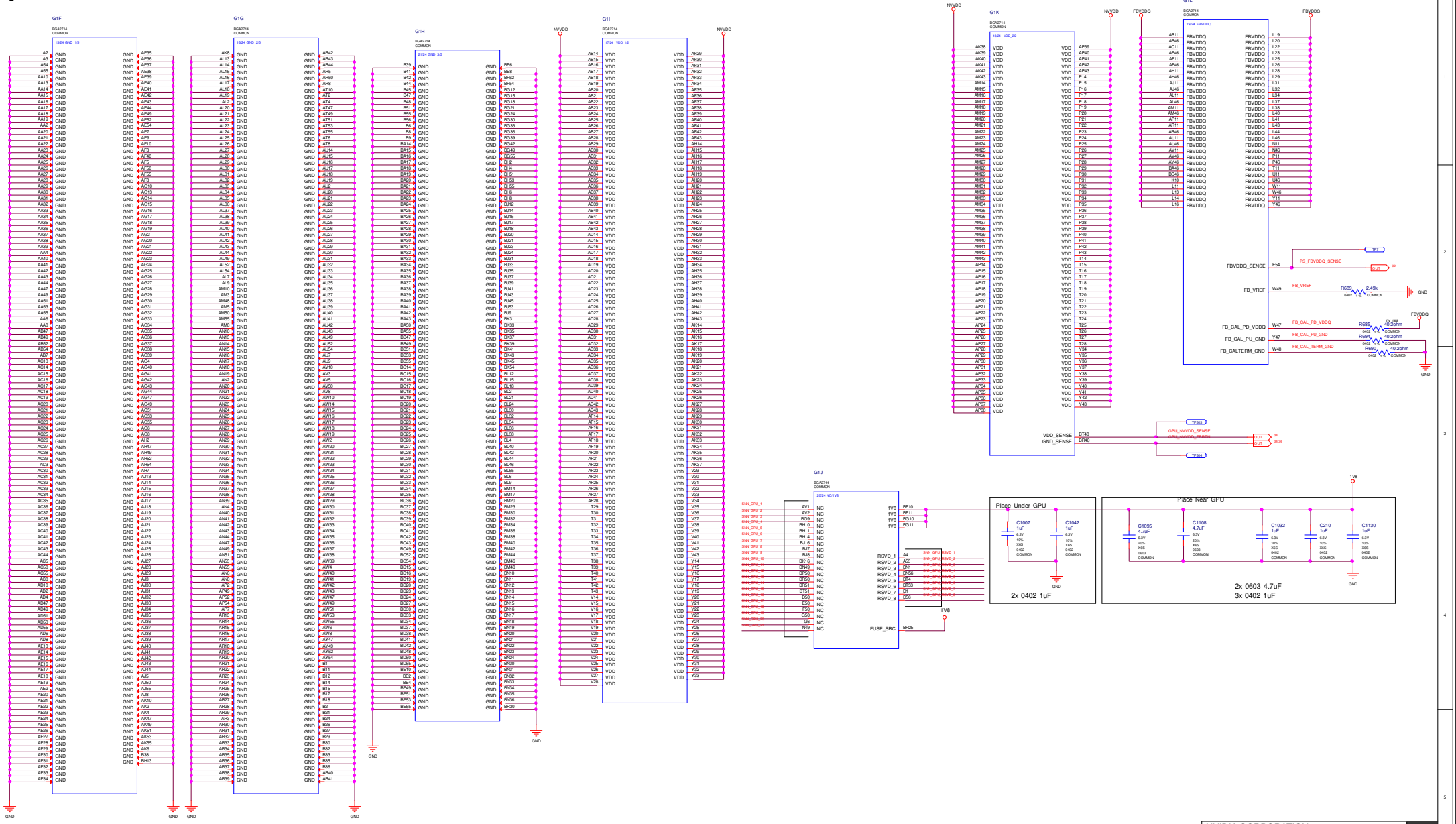
# Page15: GPU PWR and GND

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| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | GPU PWR & GND |

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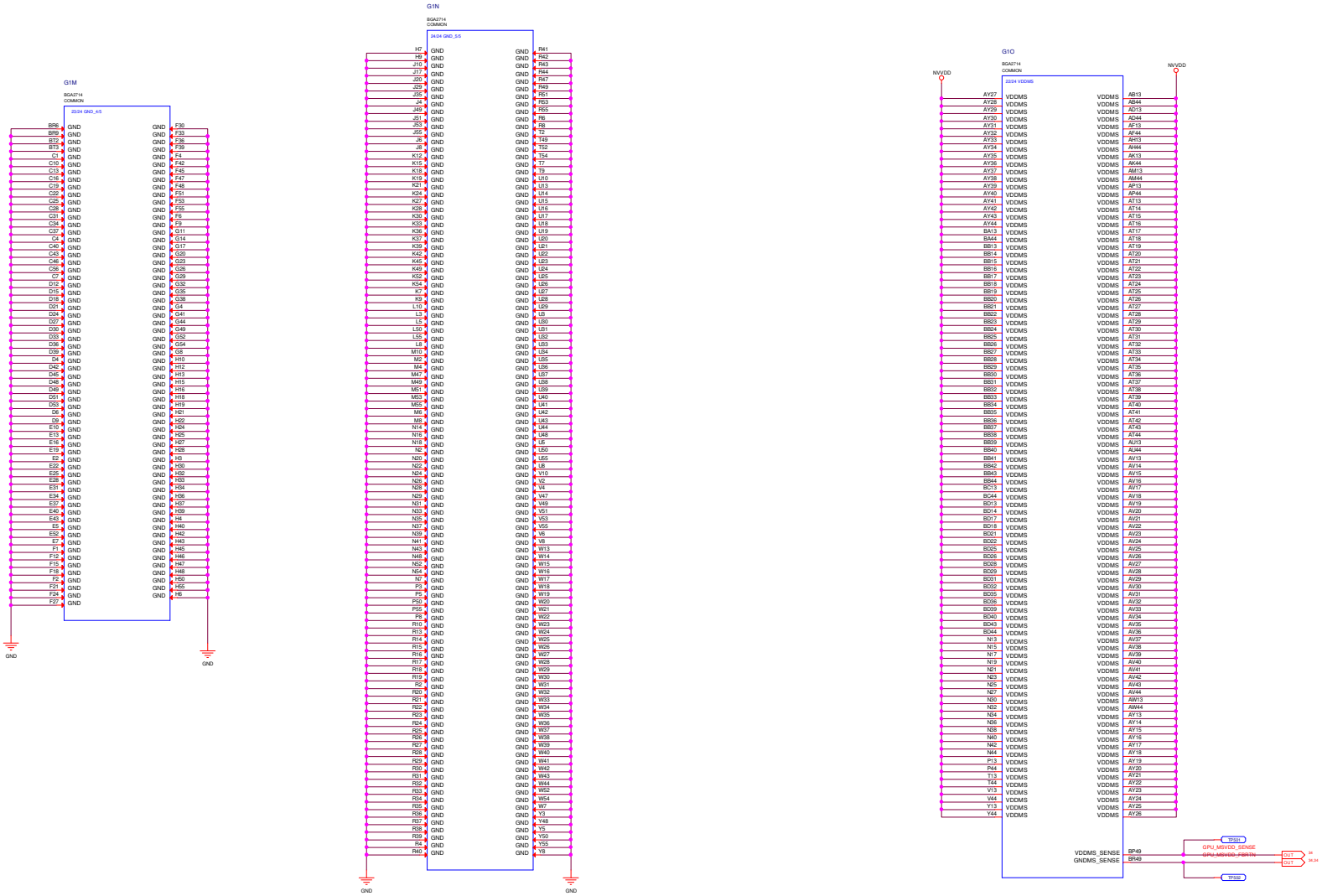
# Page16: GPU PWR and GND 2

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| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | GPU PWR & GND |

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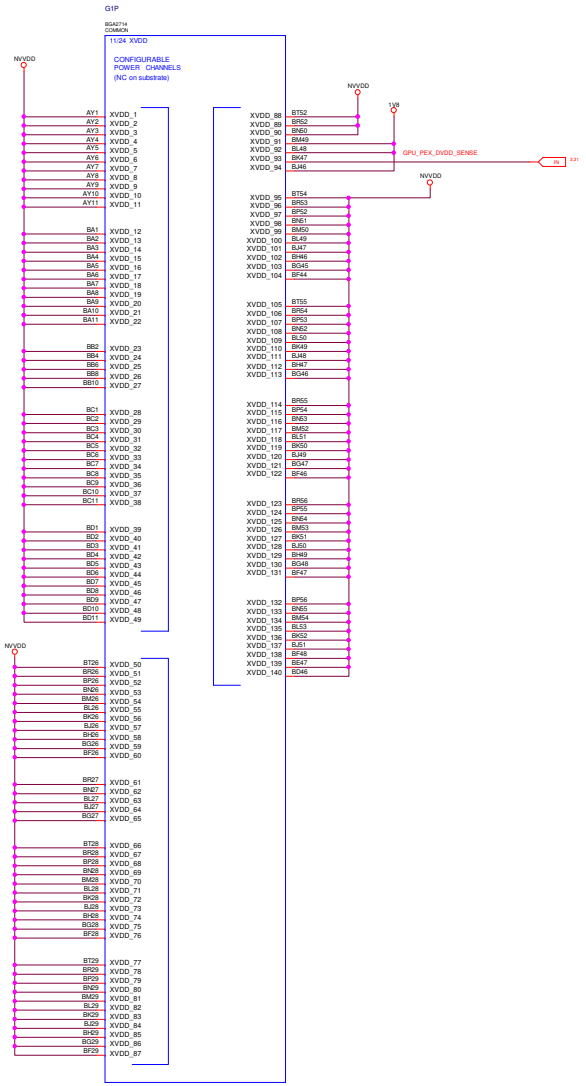
# Page17: XVDD

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| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | GPU PWR & GND 3 (NVDD) |

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| PCB REV | PG142-B00 | PAGE | 17 OF 54 |
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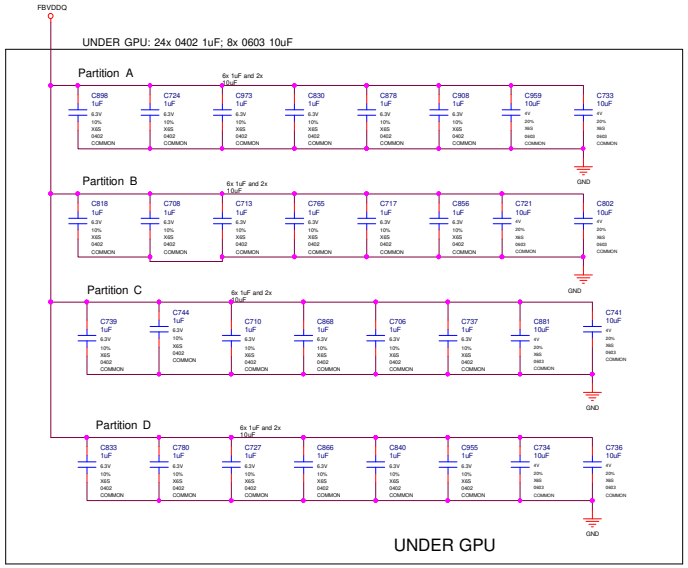
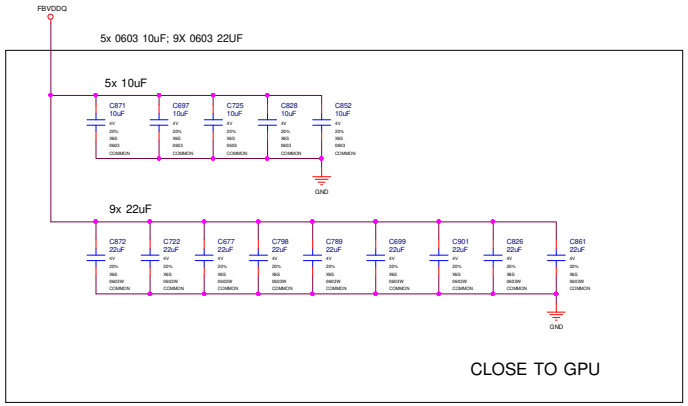
# Page18: GPU DECOUPLING FBVDDQ

## FBVDDQ

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| PAGE DETAIL | GPU DECOUPLING FBVDDQ |

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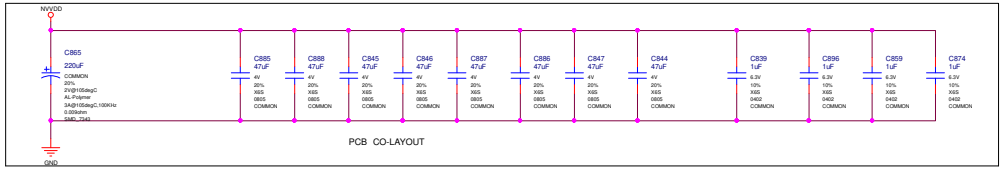
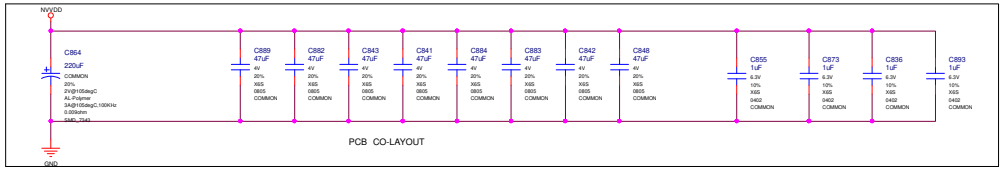
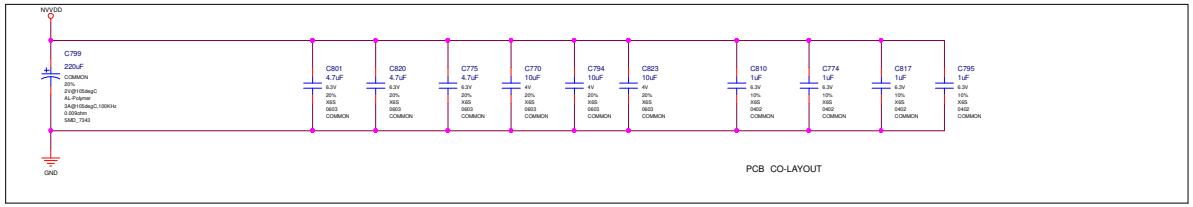
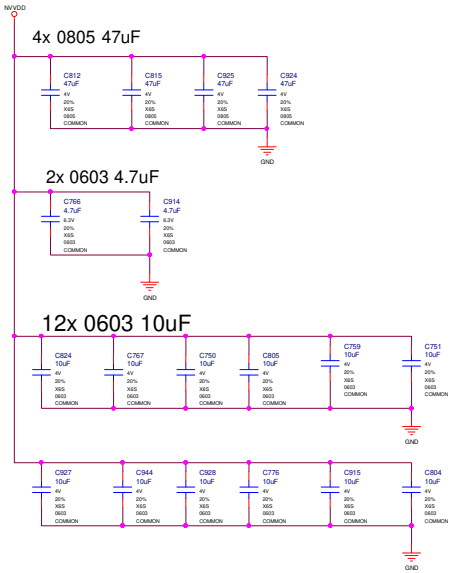
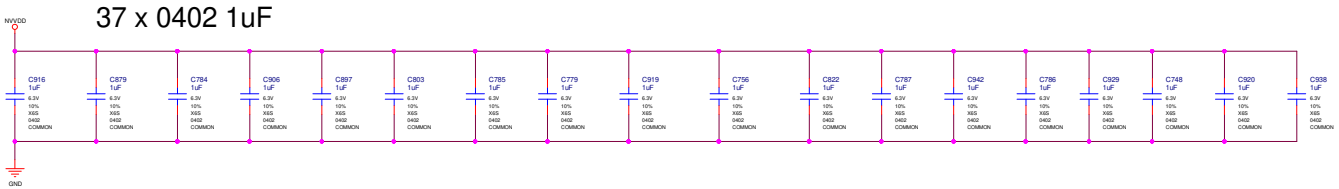
# Page19: GPU DECOUPLING NVVDD

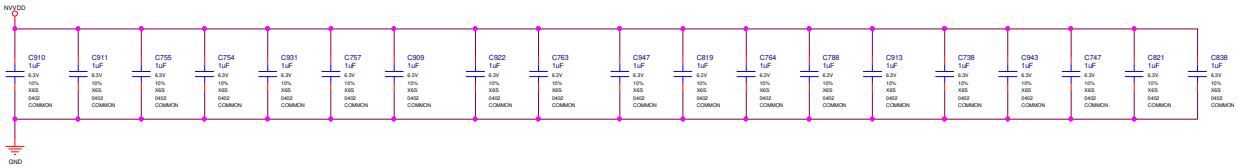



UNDER GPU

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| PAGE DETAIL | GPU DECOUPLING NVVDD |


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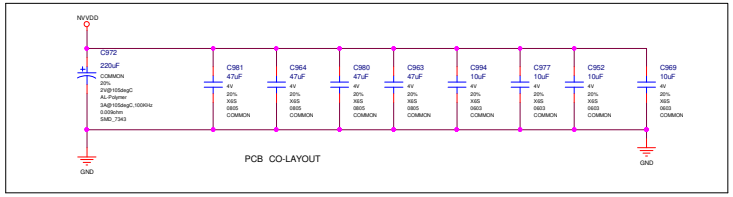
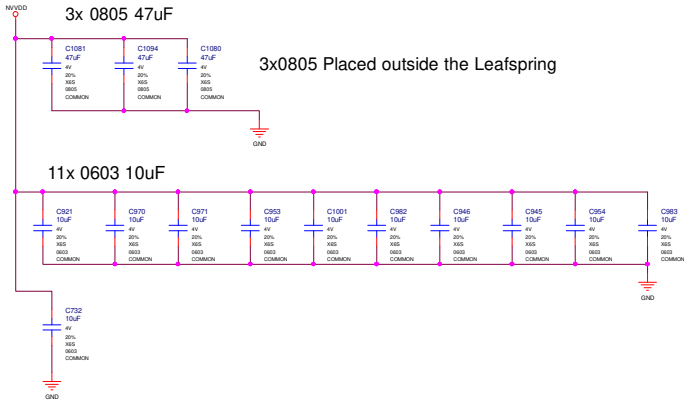
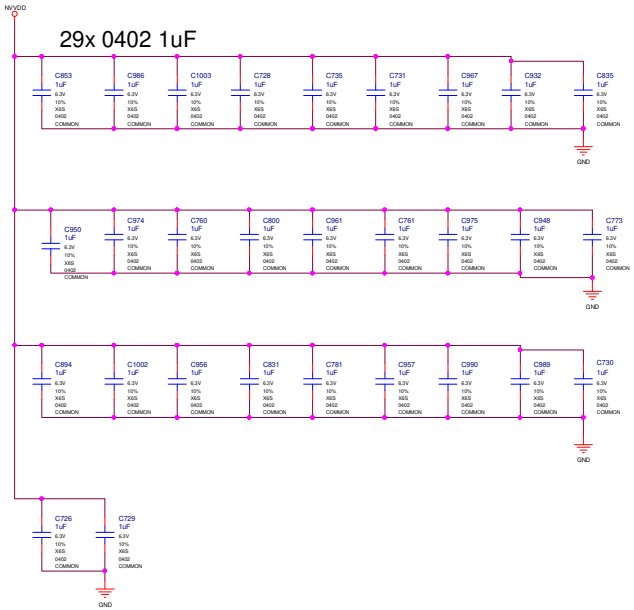
# Page20: GPU DECOUPLING NVVDD




UNDER GPU

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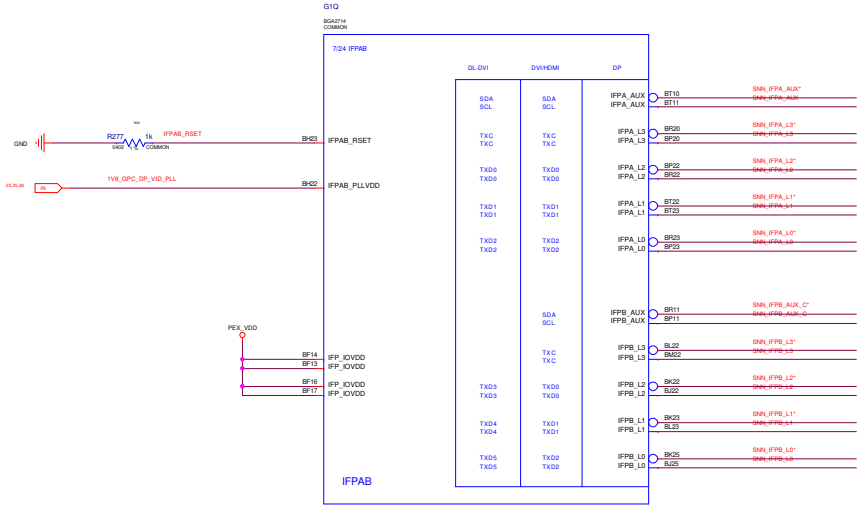
# Page21: IFPAB DVI-D-DL

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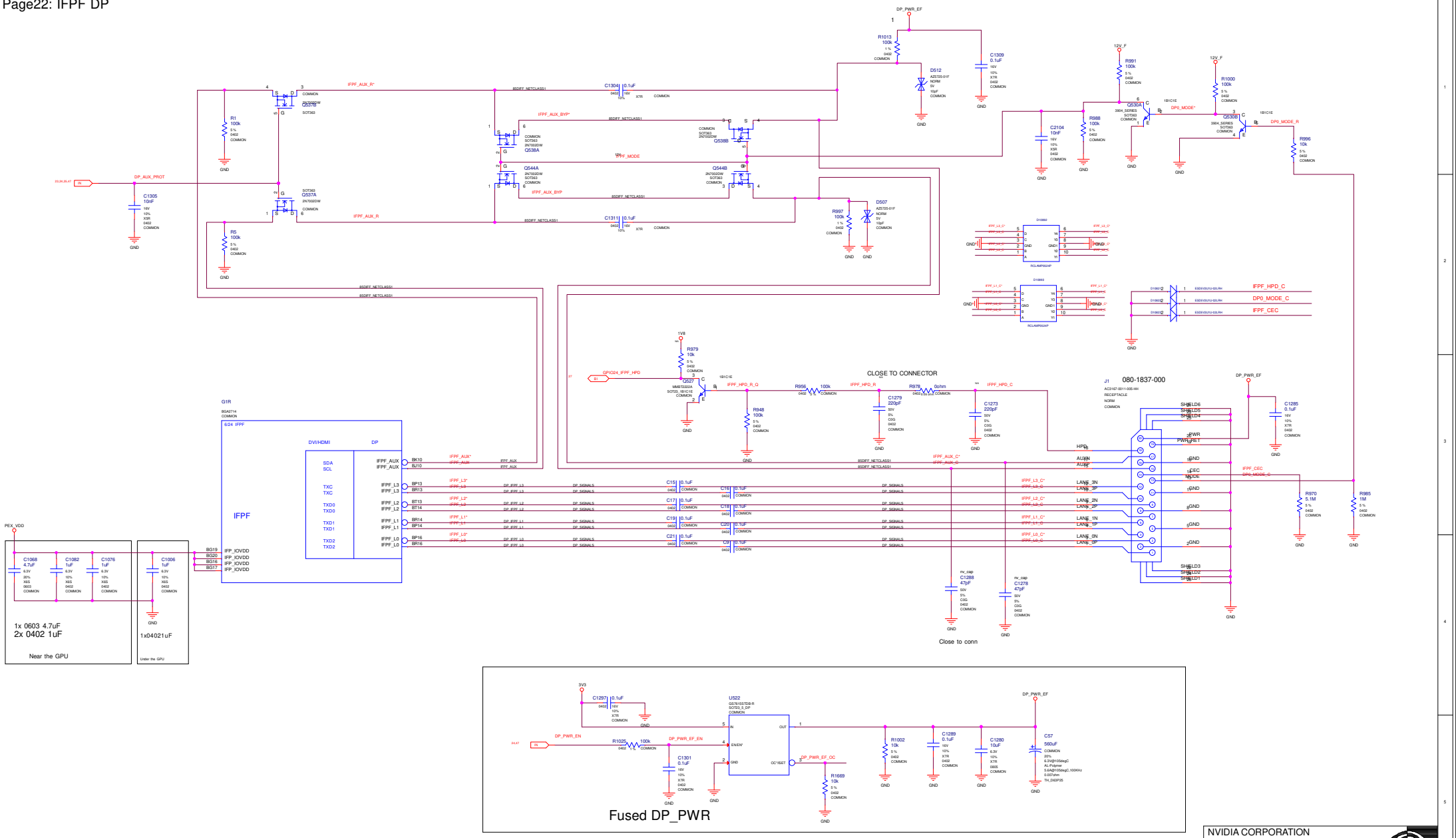
# Page22: IFPF DP

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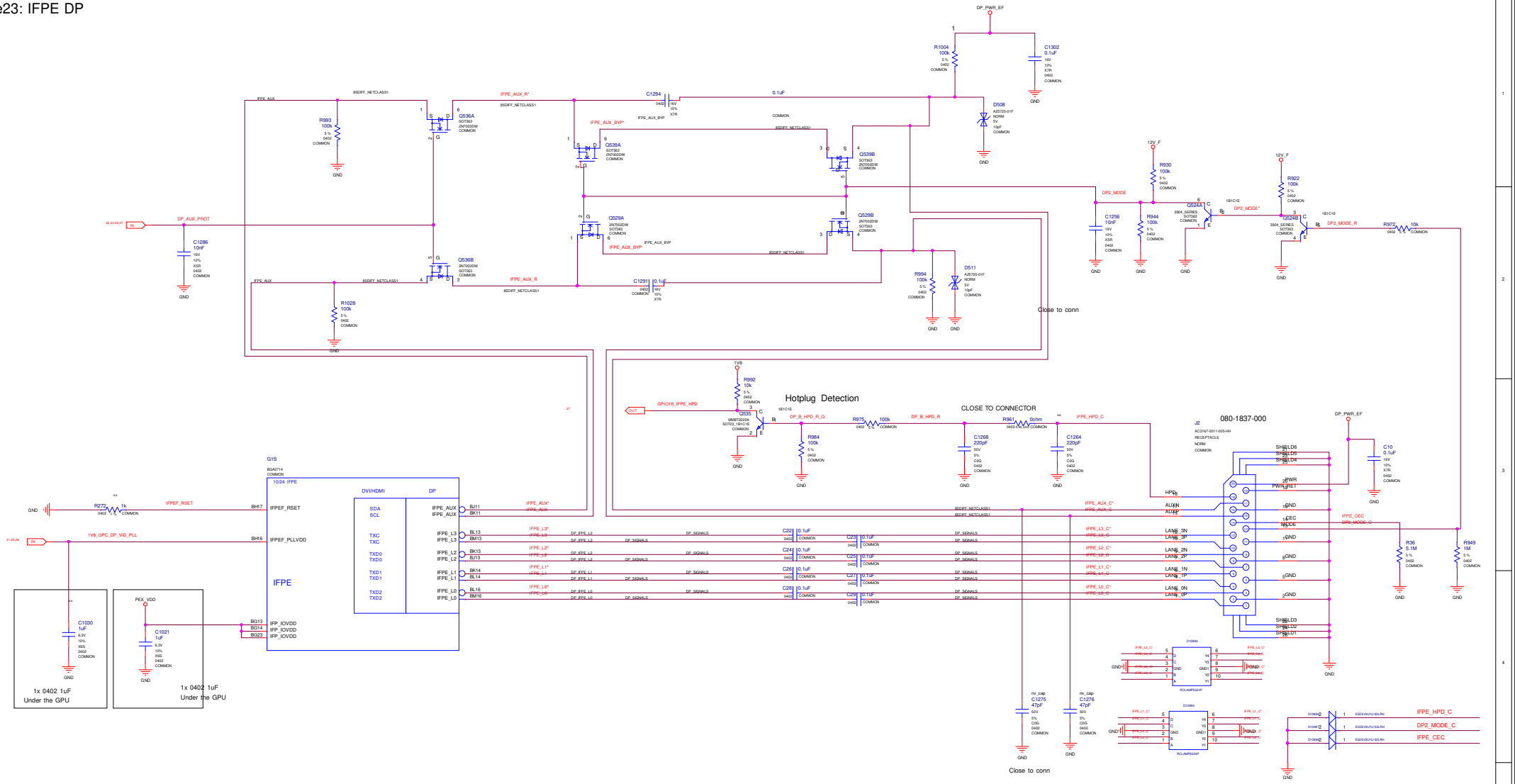
# Page23: IFPE DP

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| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | IO: IFPE DP |

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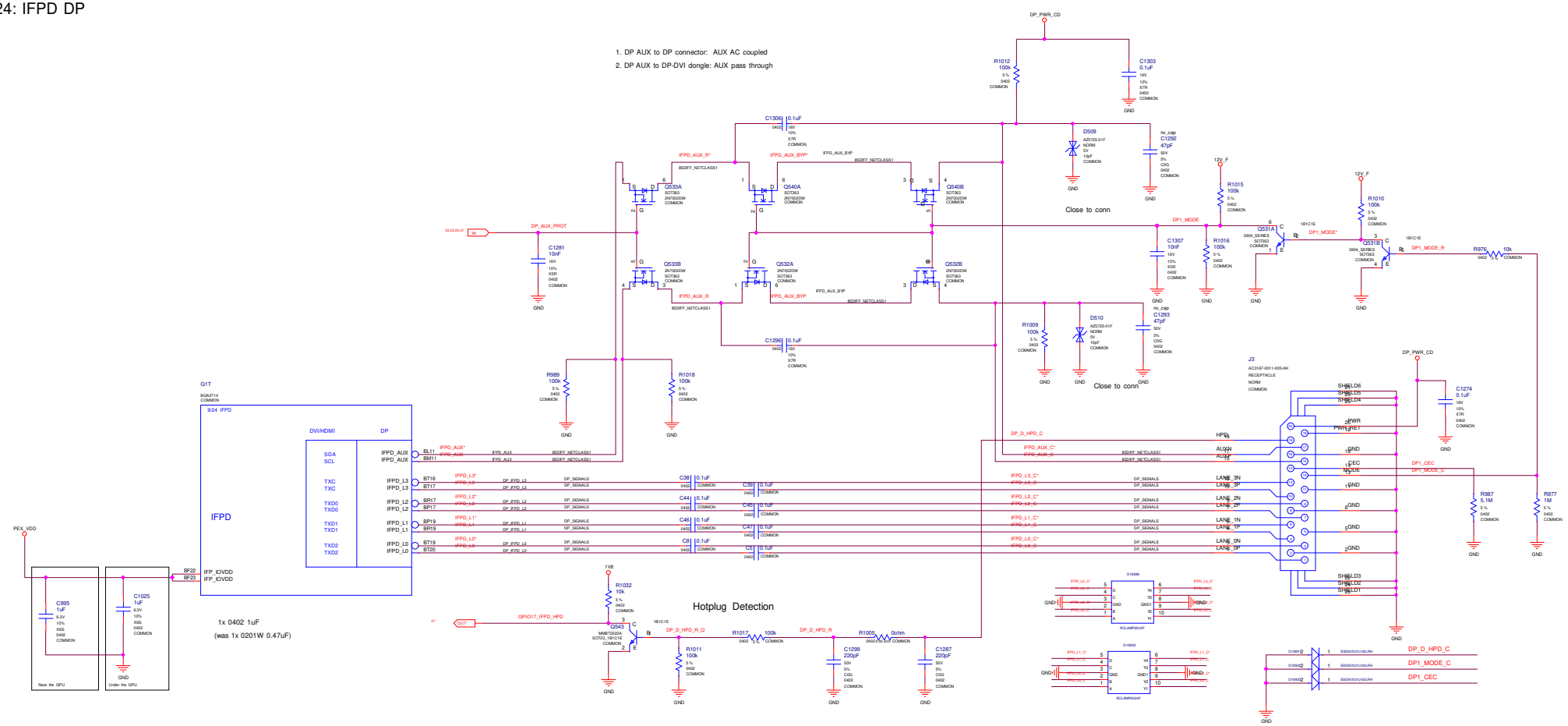
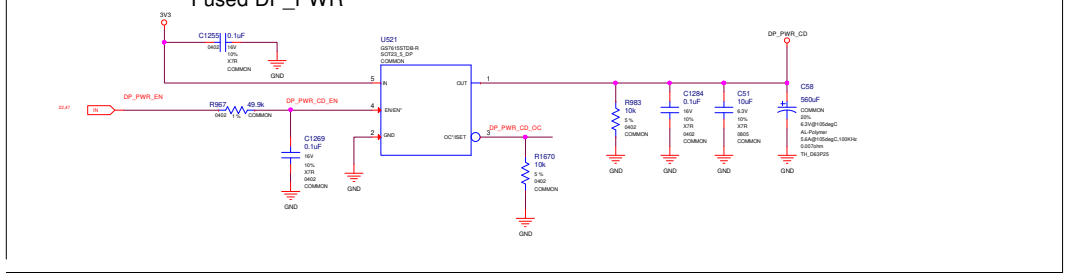
# Page24: IFPD DP

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through




## Fused DP_PWR

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| PAGE DETAIL | |

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ID: IFPD DP

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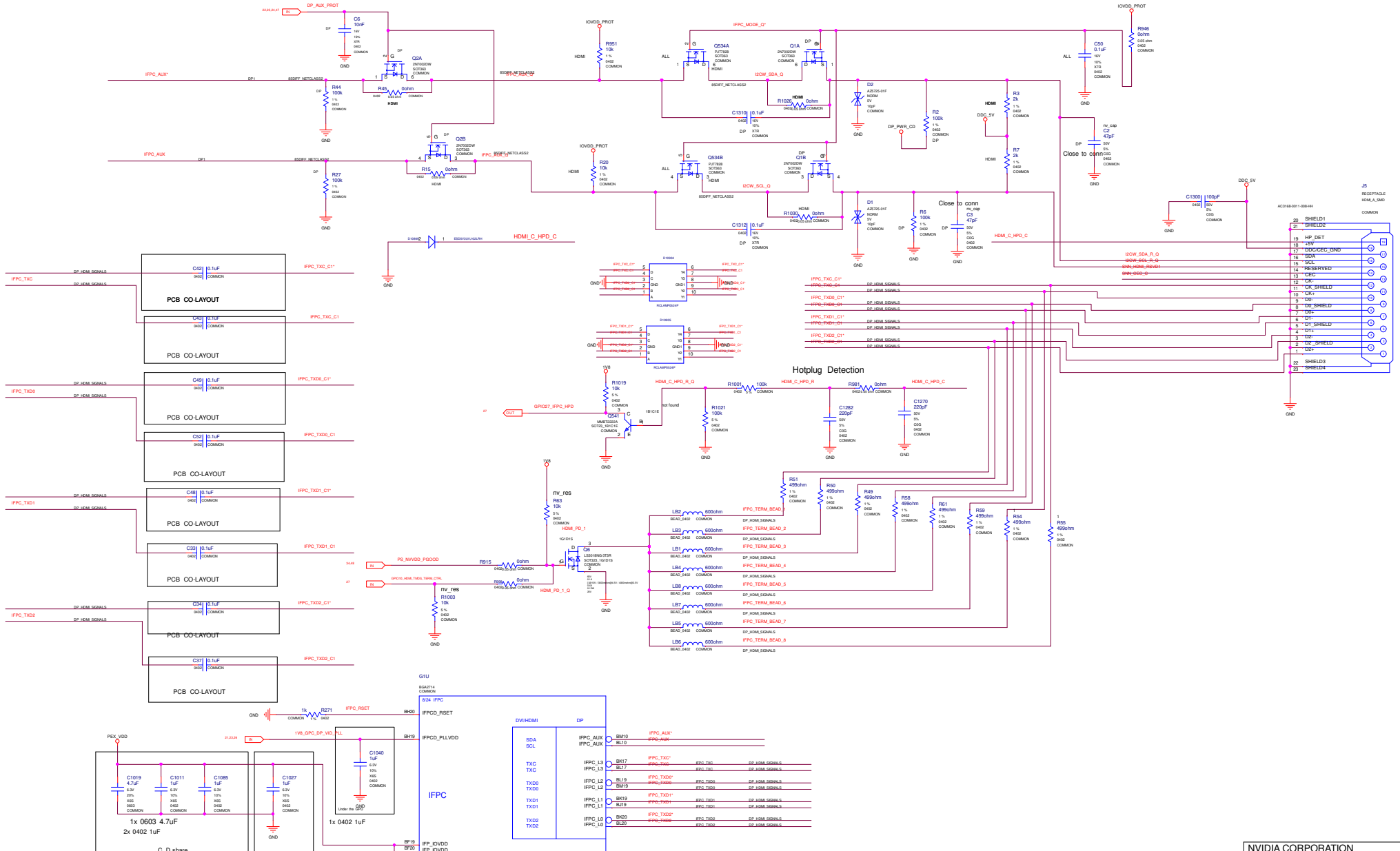
| PCB REV | PG142-B00 | PAGE | 24 OF 54 |
| BOM REV | A | DATE | 27-JUN-2020 |

# Page25: IFPC HDMI/DP

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|---|---|
| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | IO: IFPC HDMI/DP |

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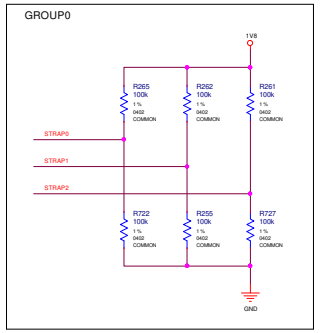
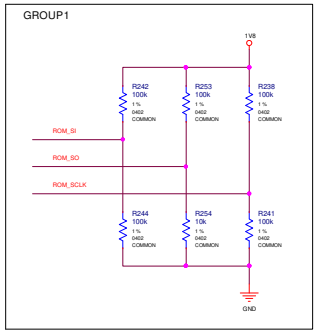
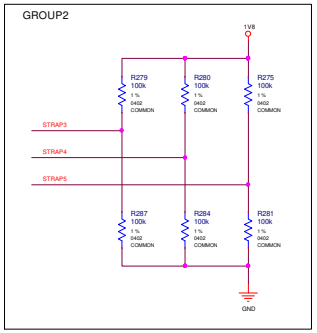
# Page26: MISC2: ROM, XTAL, Straps

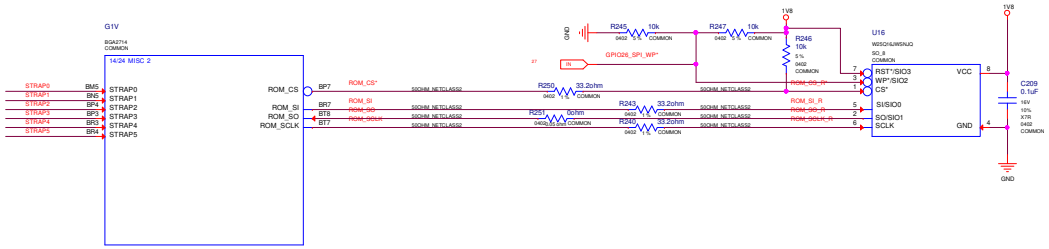
| STRAP2 | STRAP1 | STRAP0 | RAMCFG[4:0] | |
|---|---|---|---|---|
| L | L | L | 00000 | RAMCFG SAMSUNG 8Gb 7GHz |
| L | L | H | 00001 | RAMCFG MICRON 8Gb 7GHz |
| L | H | L | 00010 | RAMCFG HYNIX 8Gb 7GHz |
| H | H | L | 00110 | RAMCFG SAMSUNG 16Gb 8GHz |
| | | TBD | | |

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V




| ROM_SO | ROM_SI | ROM_SCLK | SMARTFAN[2:0],FS_OVERT | 1:ENABLE 0:DISABLE | |
|---|---|---|---|---|---|
| H | H | H | 0111 | FS_OVERT ENABLE | DEFAULT |
| H | H | M | 0000 | FS_OVERT DISABLE | |

| STRAP5 | STRAP4 | STRAP3 | SMB_ALT_ADDR | DEVID_SEL | PCIE_CFG | VGA_DEVICE |
|---|---|---|---|---|---|---|
| M | H | H | 1 | 1 | 1 | 1 |
| M | H | L | 1 | 1 | 1 | 0 |
| M | L | H | 1 | 1 | 0 | 1 |
| M | L | L | 1 | 1 | 0 | 0 |
| L | H | M | 1 | 0 | 1 | 1 |
| L | M | H | 1 | 0 | 1 | 0 |
| L | M | L | 1 | 0 | 0 | 1 |
| L | L | M | 1 | 0 | 0 | 0 |
| H | H | H | 0 | 1 | 1 | 1 |
| H | H | L | 0 | 1 | 1 | 0 |
| H | L | H | 0 | 1 | 0 | 1 |
| H | L | L | 0 | 1 | 0 | 0 |
| L | H | H | 0 | 0 | 1 | 1 |
| L | H | L | 0 | 0 | 1 | 0 |
| L | L | H | 0 | 0 | 0 | 1 DEFAULT |
| L | L | L | 0 | 0 | 0 | 0 |

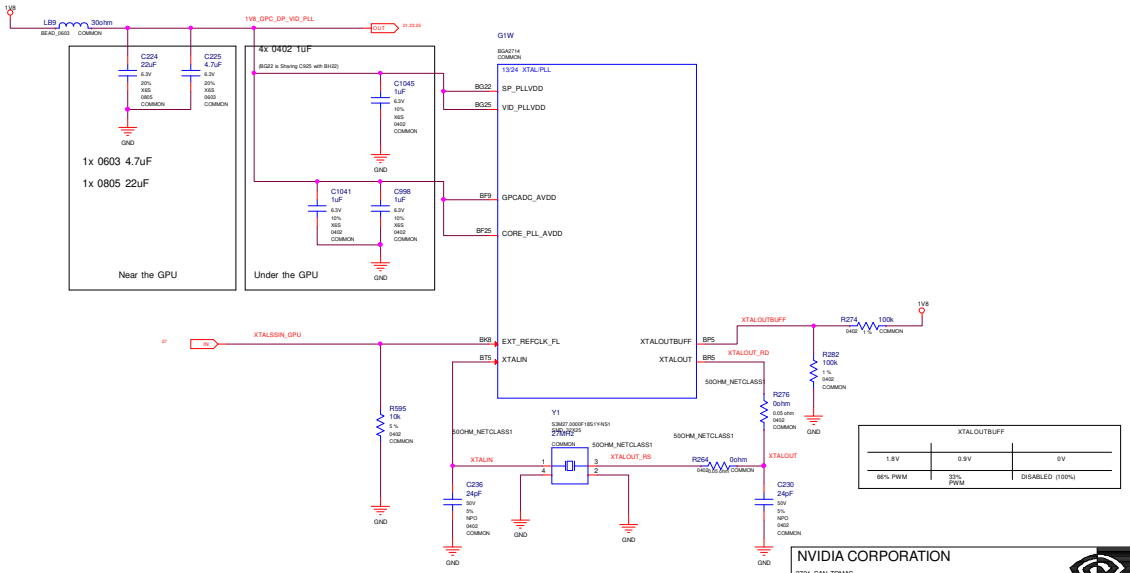
H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE




| XTALOUTBUFF | | |
|---|---|---|
| 1.8V | 0.9V | 0V |
| 66% PWM | 33% PWM | DISABLED (100%) |

| | |
|---|---|
| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | MISC1: ROM, XTAL,STRAPS |

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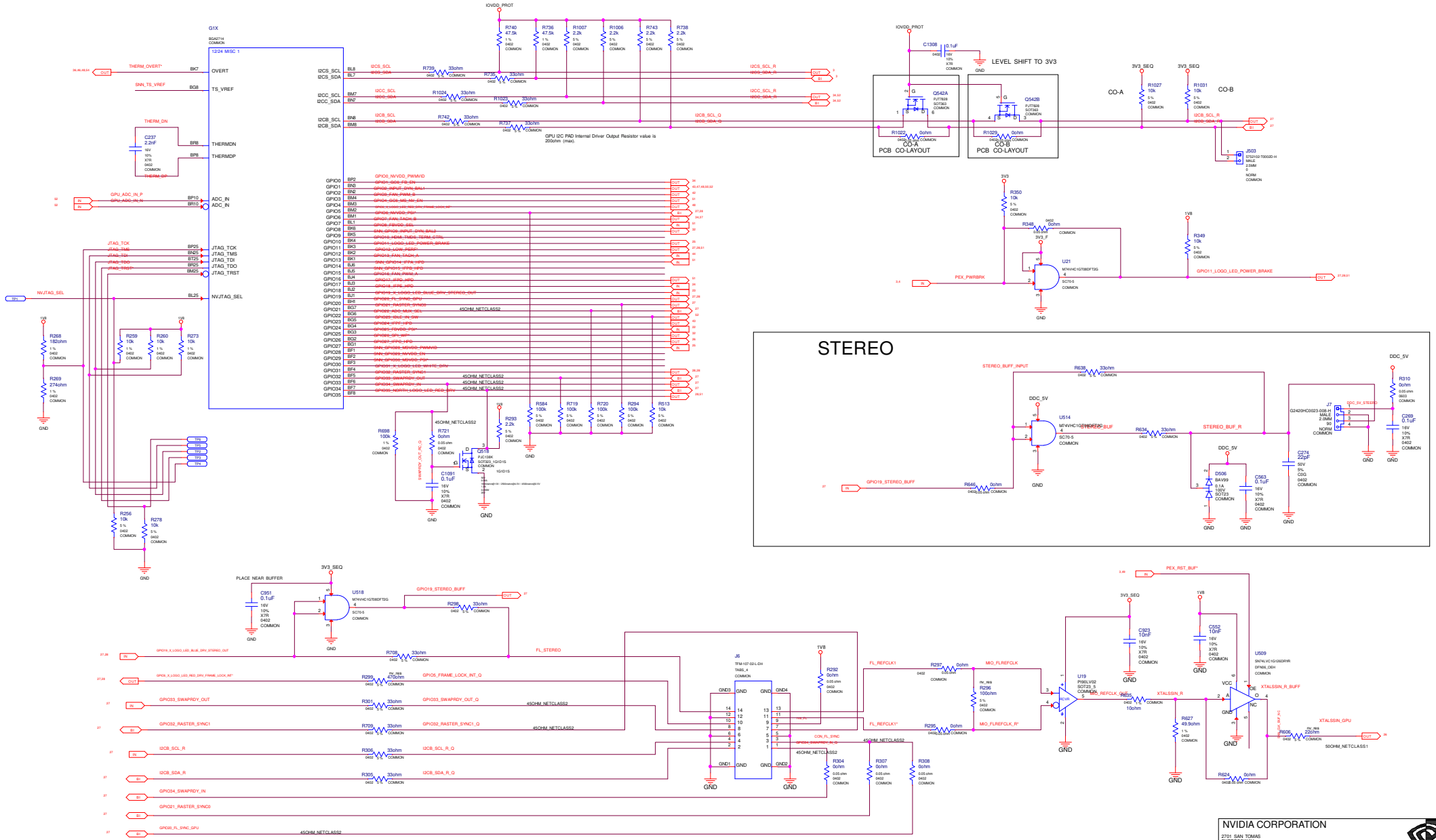
# Page27: MISC1: JTAG, GPIO, ADC, I2C, OVERT

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| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | MISC2: JTAG,GPIO,ADC,I2C,FL,STEERO |

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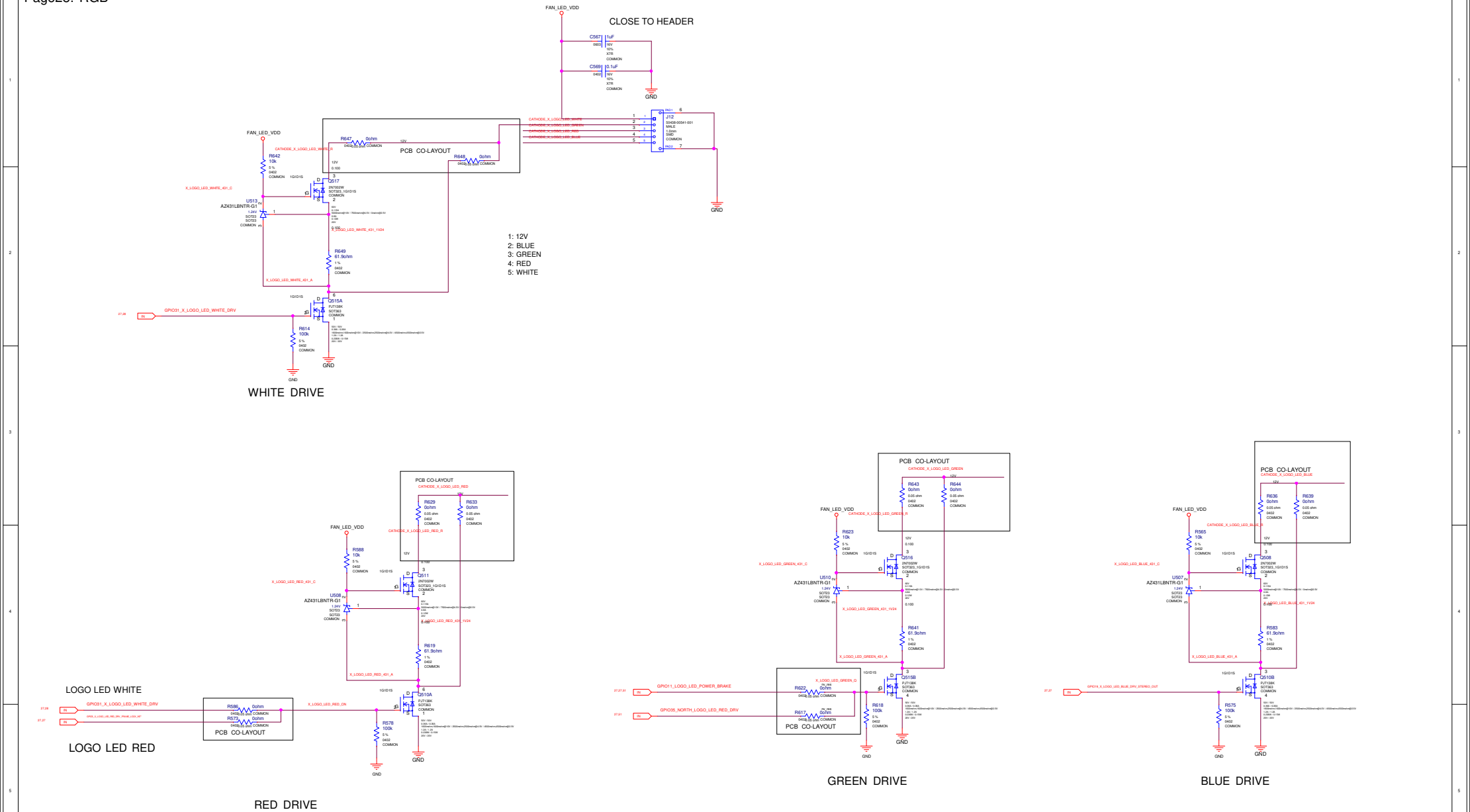
# Page28: RGB

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| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | MISC3: RGB |

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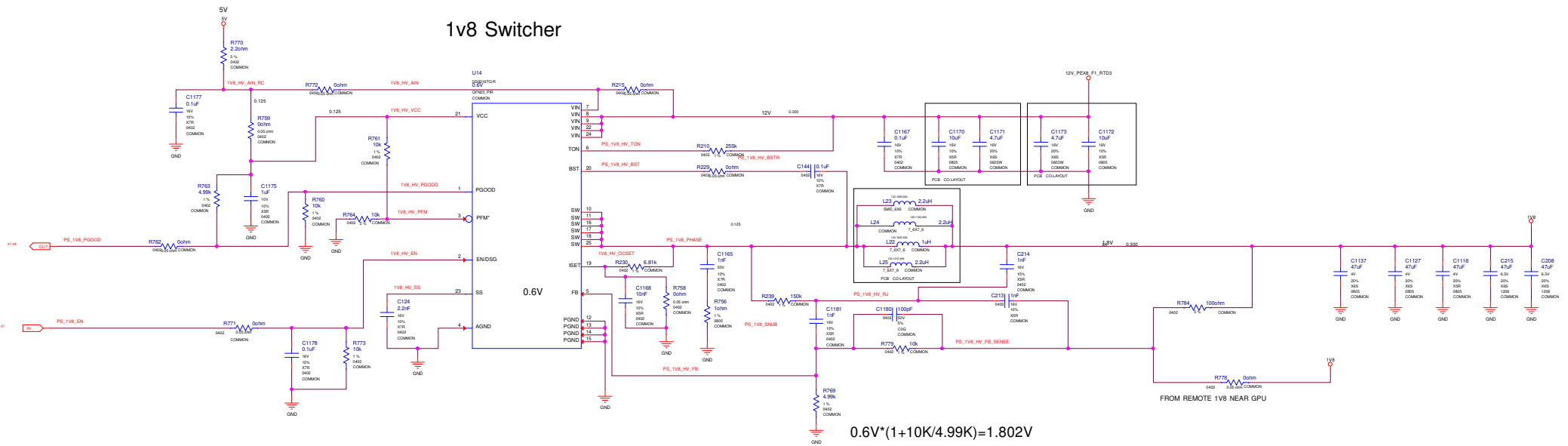
| PCB REV | PG142-B00 | PAGE | 28 OF 54 |
| BOM REV | A | DATE | 27-JUN-2020 |

# 1v8 Switcher

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| PAGE DETAIL | PS: 1V8 |

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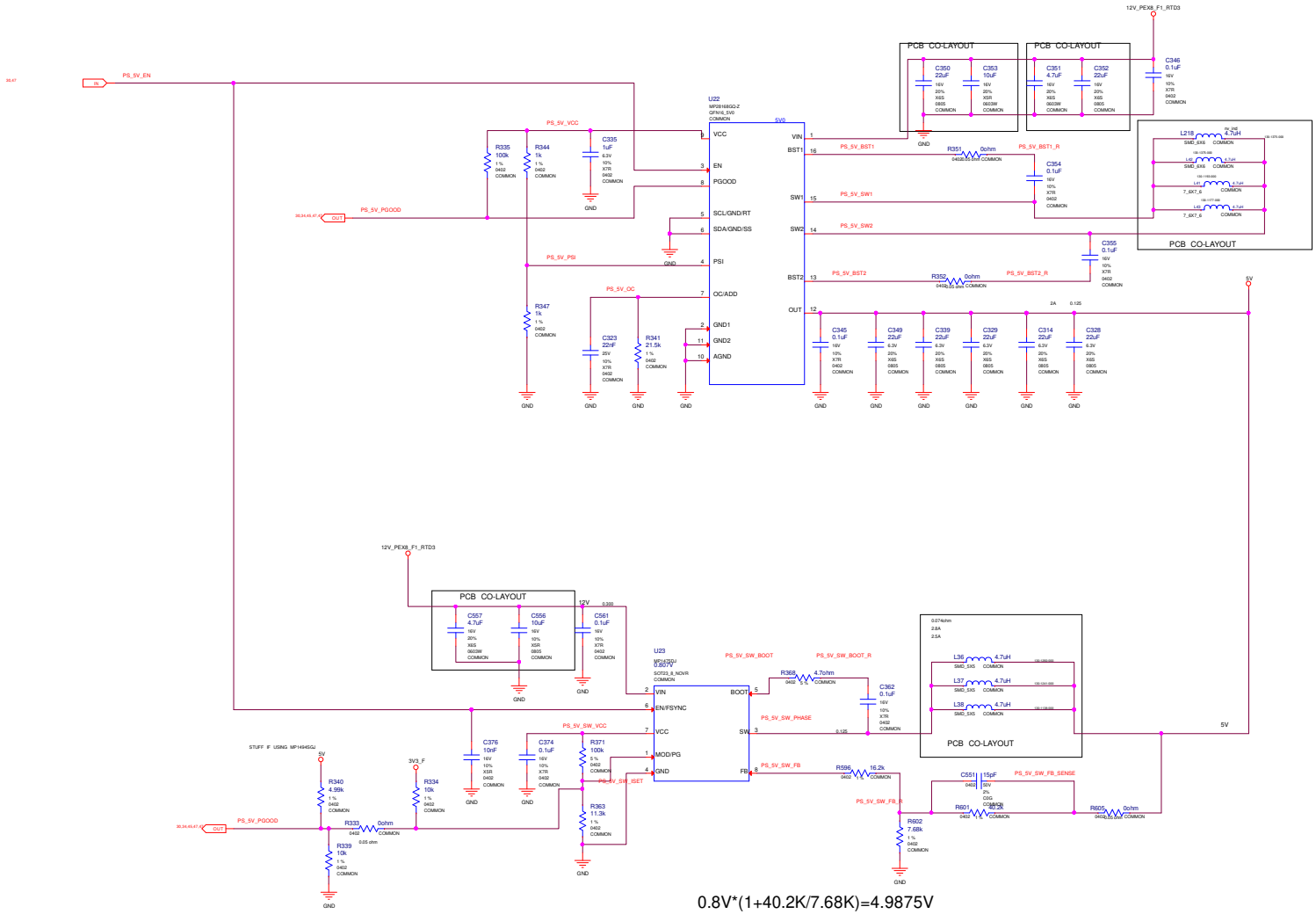
# Page30: PS: 5V

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| PAGE DETAIL | PS: 5V |

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| PCB REV | PG142-B00 | PAGE | 30 OF 54 |
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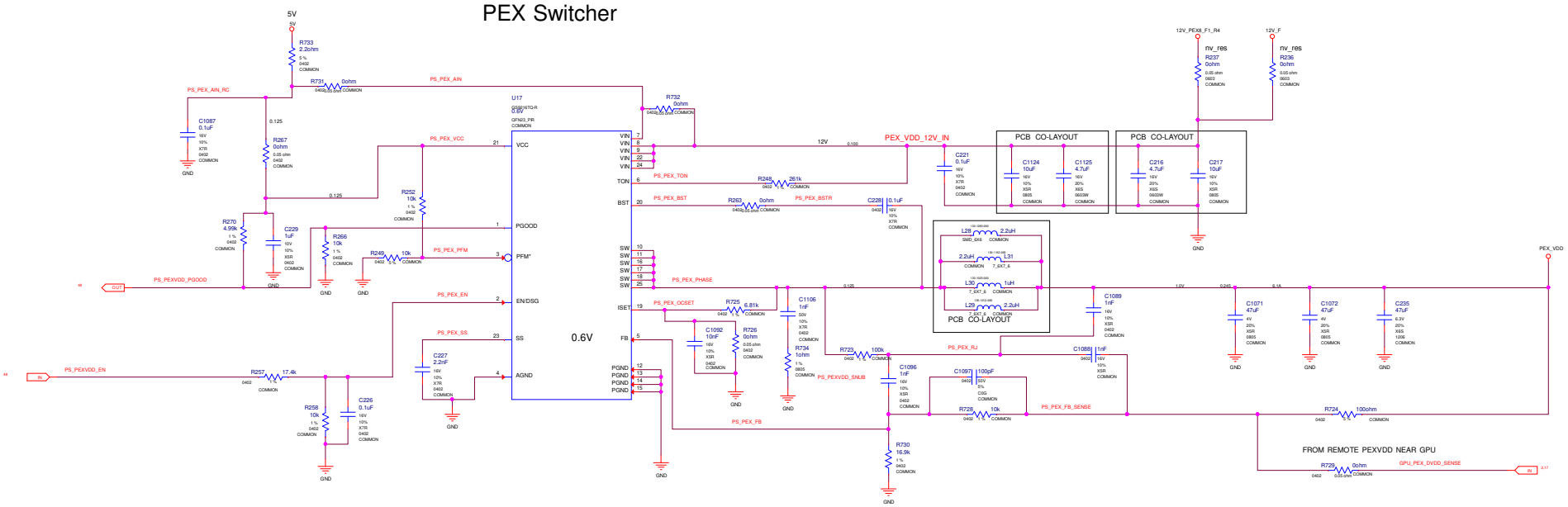
# Page31: PS: PEXVDD

## PEX Switcher




0.6V*(1+10K/16.9K)=0.955V

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| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | PS: PEXVDD |

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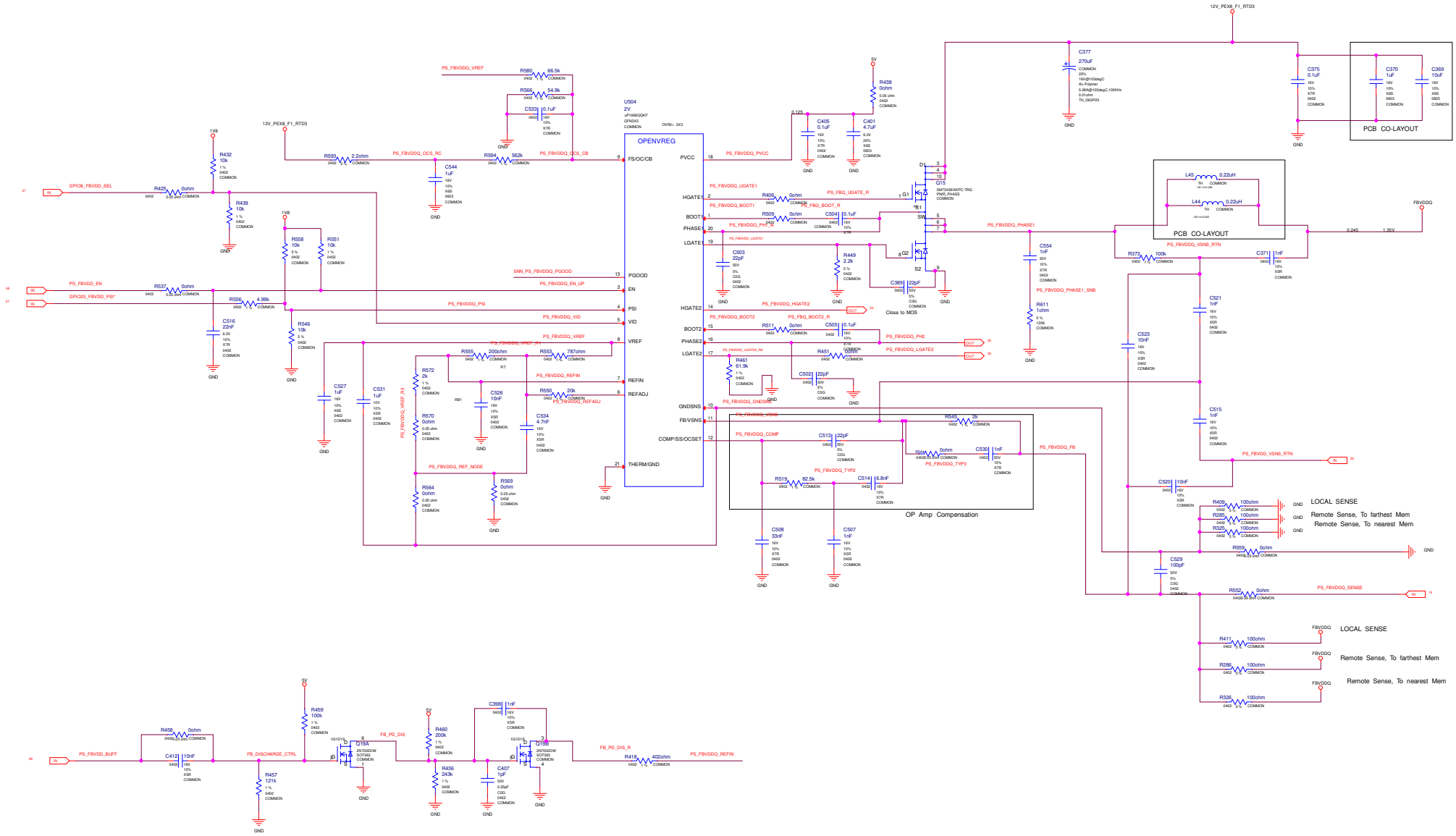
| NV_PN | 600-1G142-BASE-100 | | |
| PCB REV | PG142-B00 | PAGE | 31 OF 54 |
| BOM REV | A | DATE | 27-JUN-2020 |

# Page32: PS: FBVDDQ

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| PAGE DETAIL | PS: FBVDDQ |

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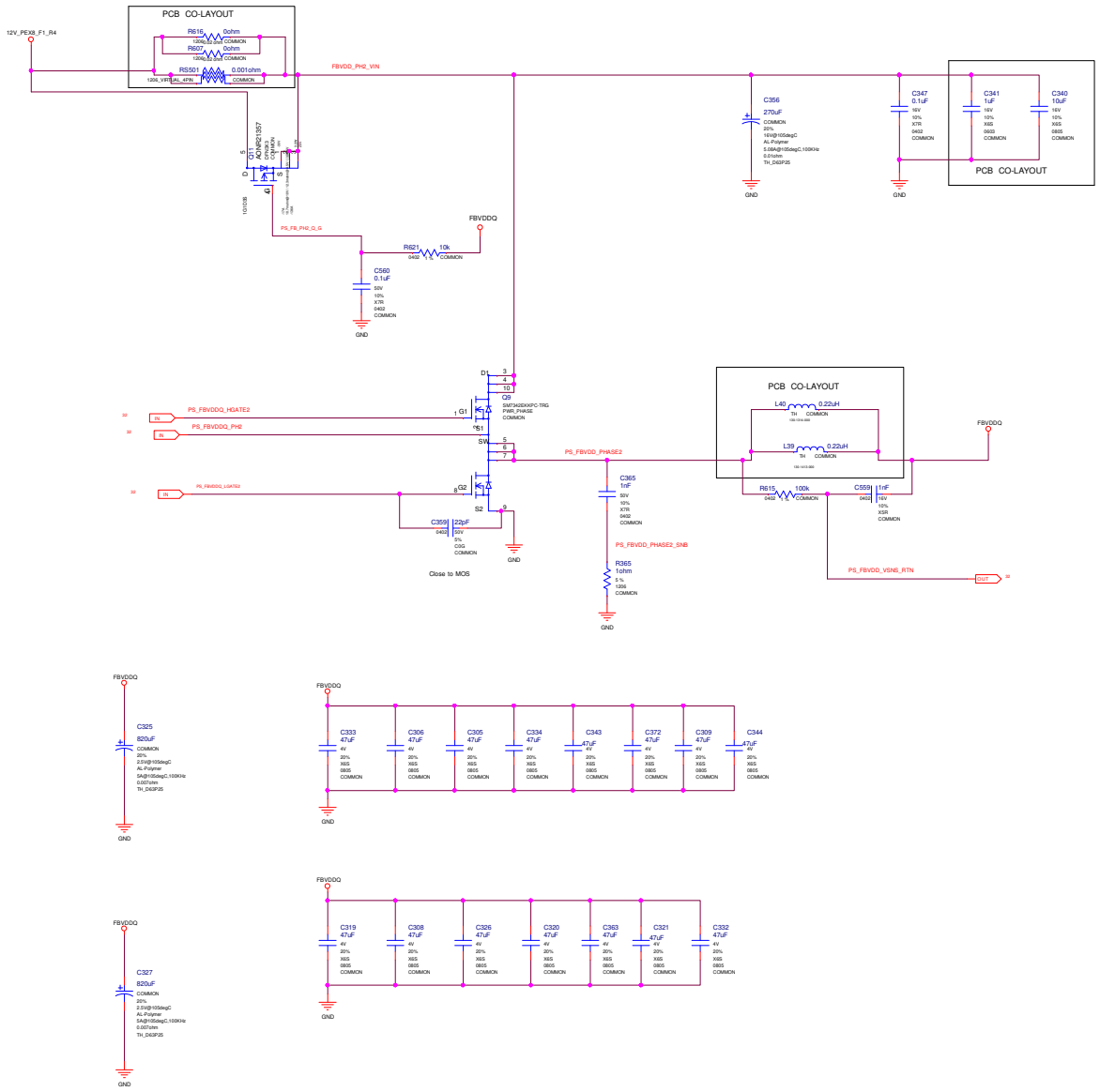
| BOM REV | A | DATE | 27-JUN-2020 |

# Page33: PS: FBVDDQ PH2

## FBVDD PH2 INPUT ANTI-BACKDRIVE

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| PAGE DETAIL | PS: FBVDDQ PH2 |

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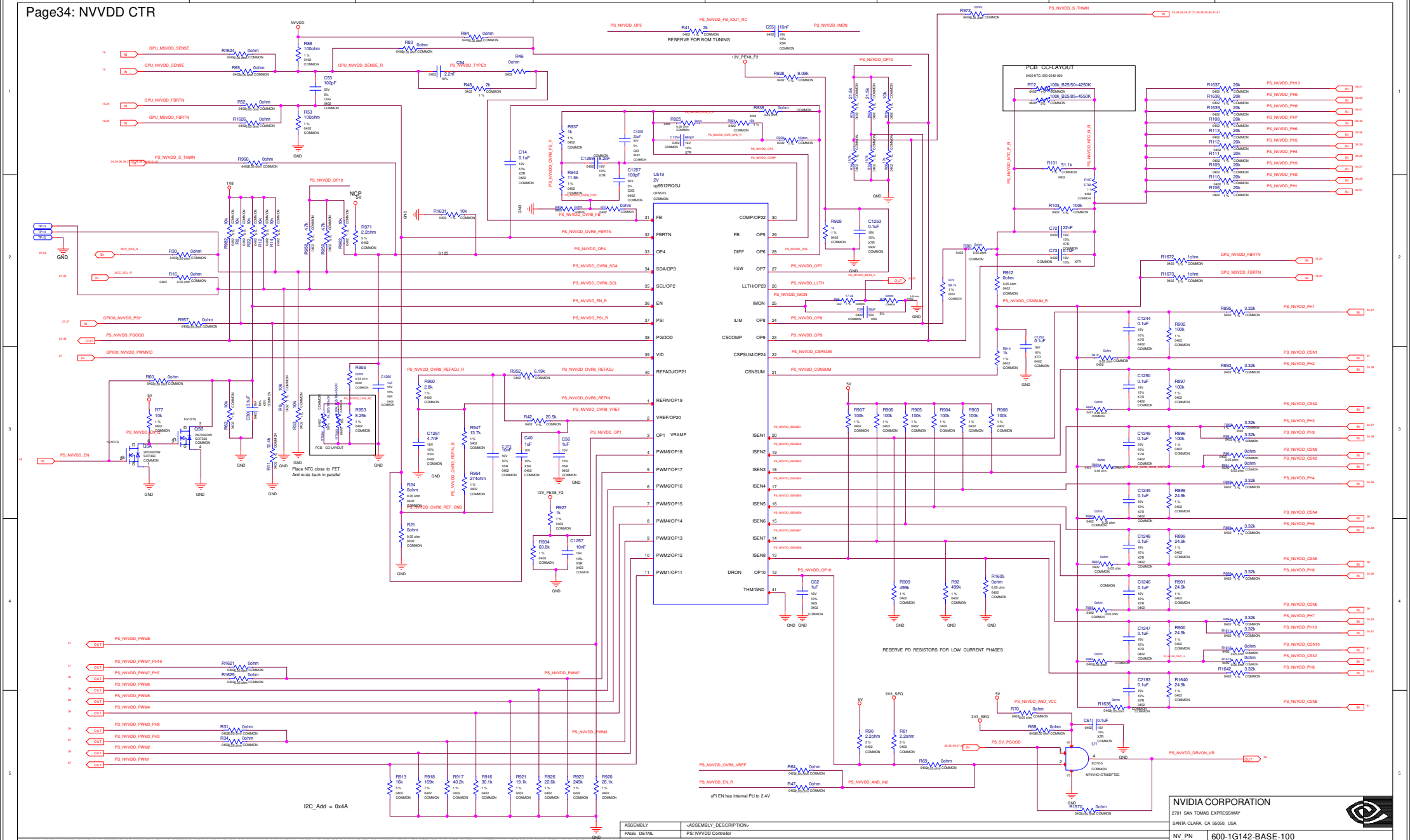
| PCB REV | PG142-B00 | PAGE | 33 OF 54 |
| BOM REV | A | DATE | 27-JUN-2020 |

# Page34: NVVDD CTR

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| PAGE DETAIL | BLANK PAGE |

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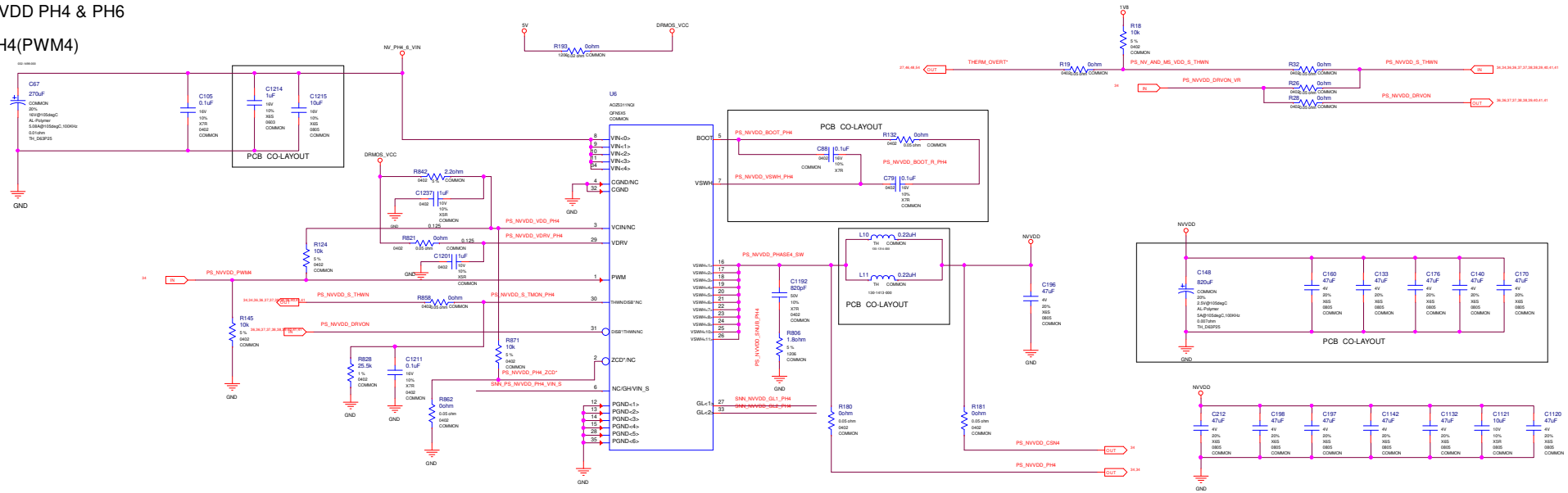
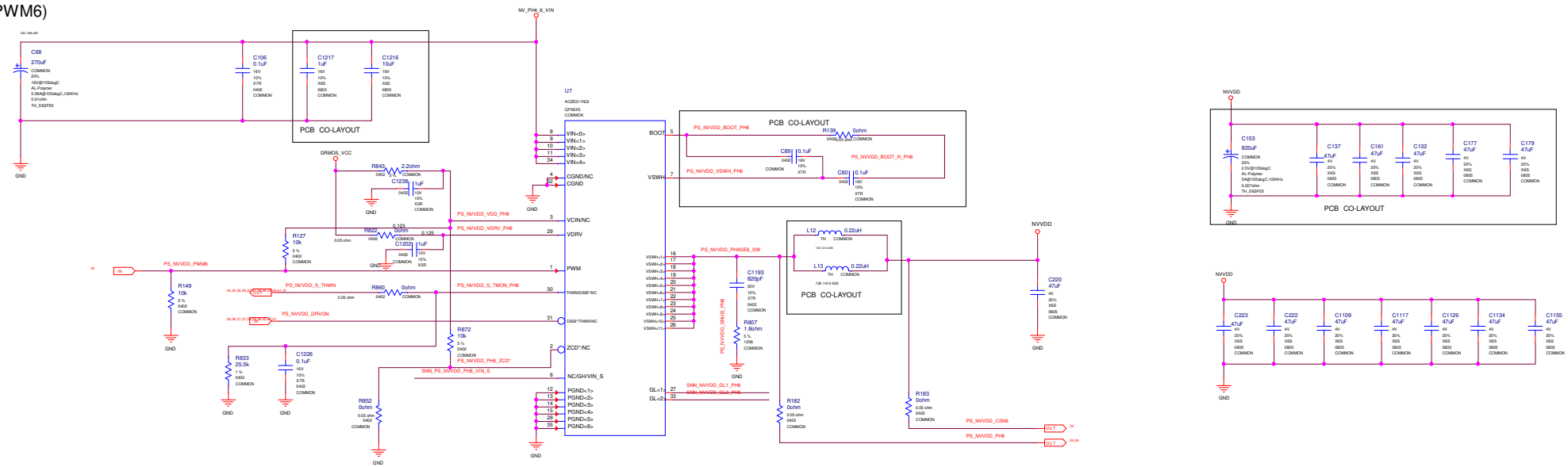
| BOM REV | A | DATE | 27-JUN-2020 |

# Page36: NVVDD PH4 & PH6

## NVVDD PH4(PWM4)




## NVVDD PH6(PWM6)

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| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | PS: NVVDD PH4, PH6 |

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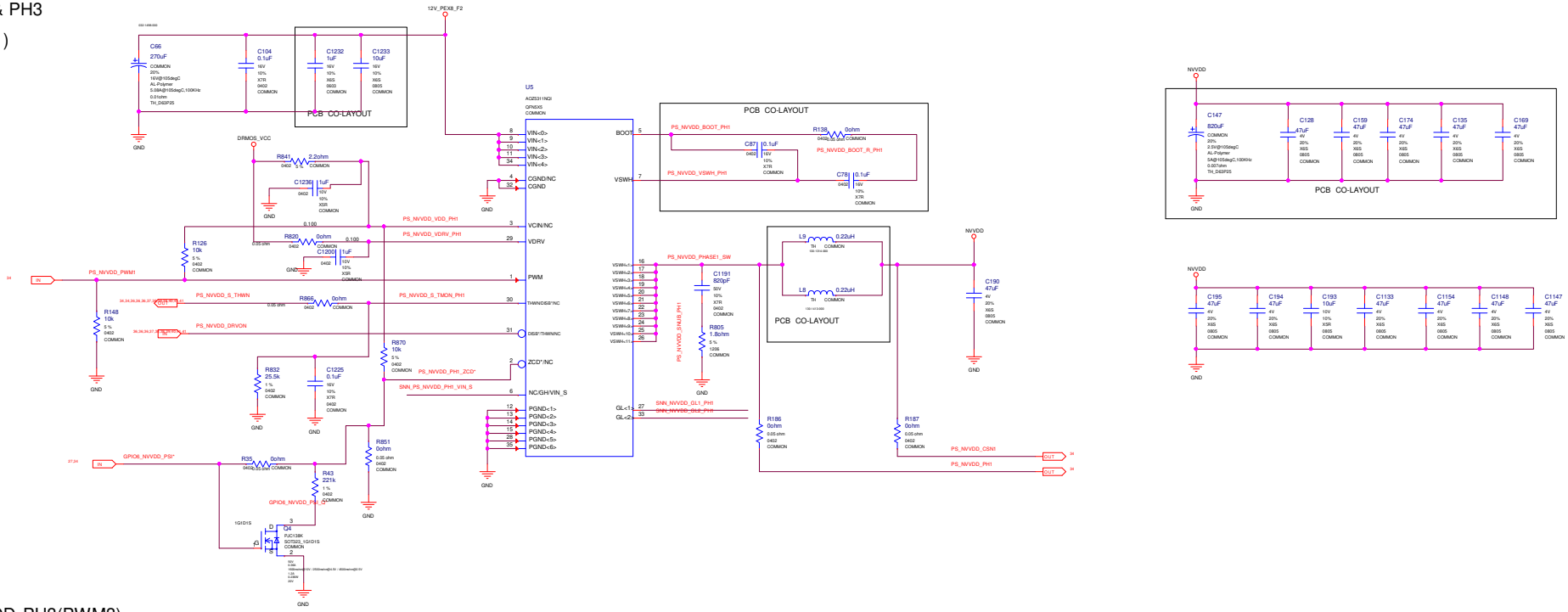
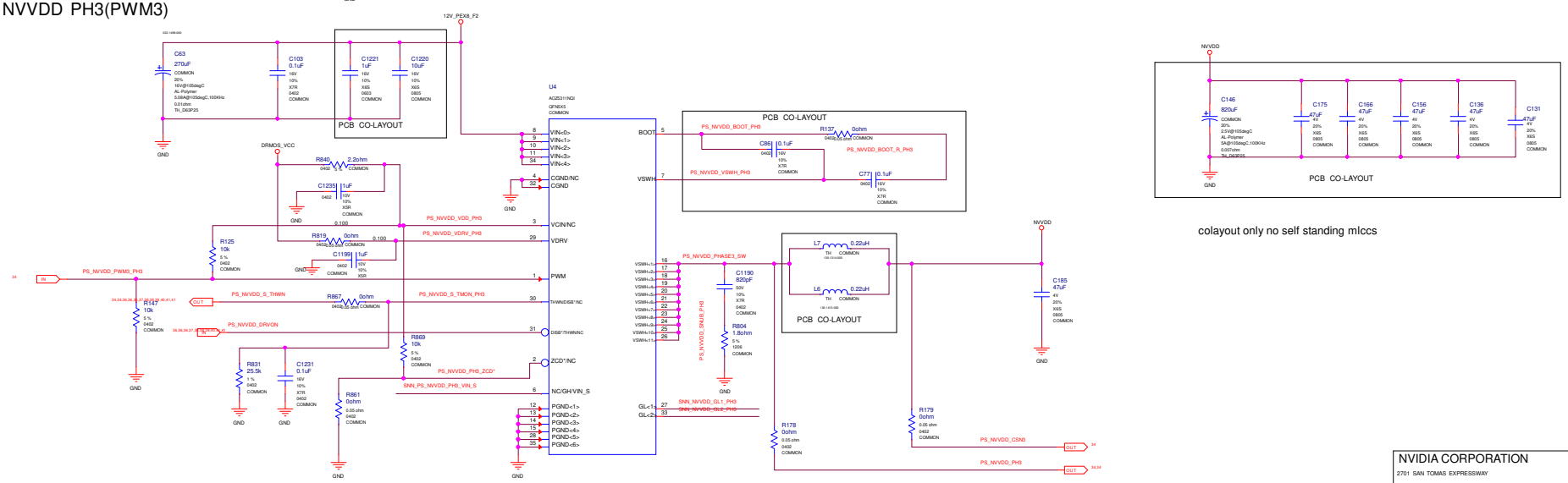
| NV_PN | 600-1G142-BASE-100 | | |
| PCB REV | PG142-B00 | PAGE | 36 OF 54 |
| BOM REV | A | DATE | 27-JUN-2020 |

# Page37: NVVDD PH1 & PH3

## NVVDD PH1(PWM1)




## NVVDD PH3(PWM3)




colayout only no self standing mlccs

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|---|---|
| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | PS: NVVDD PH1 , PH3 |

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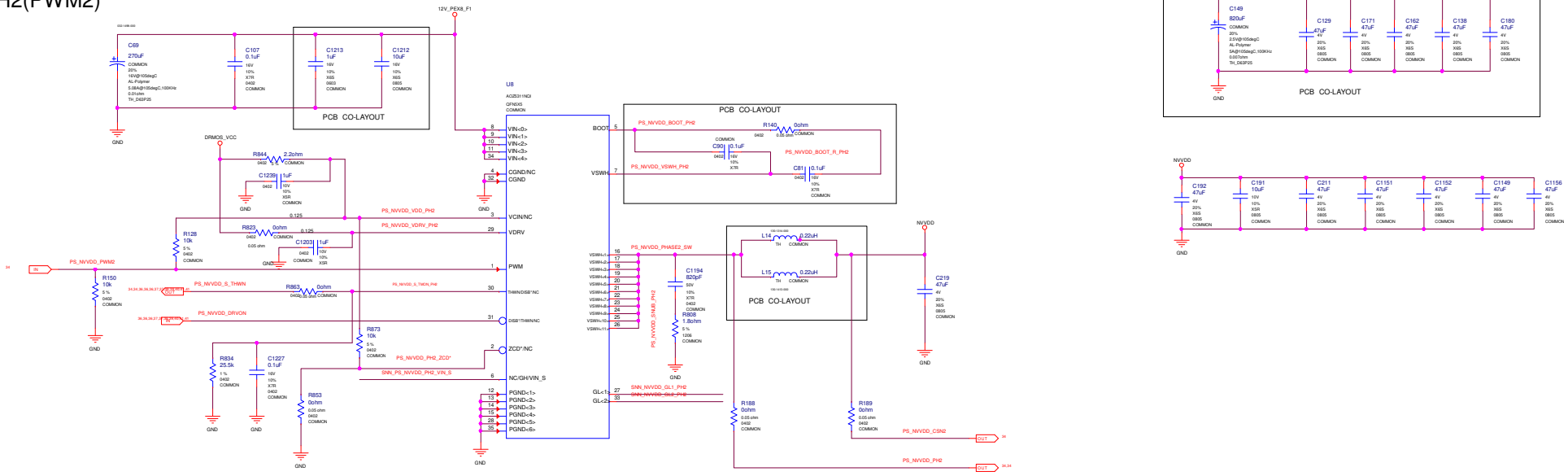
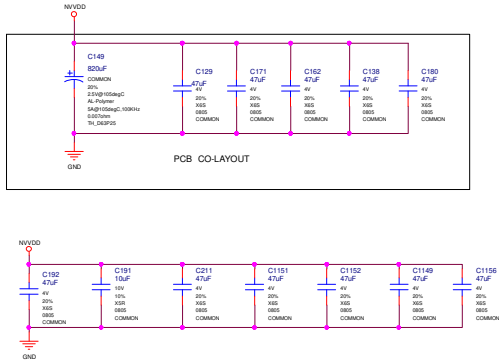
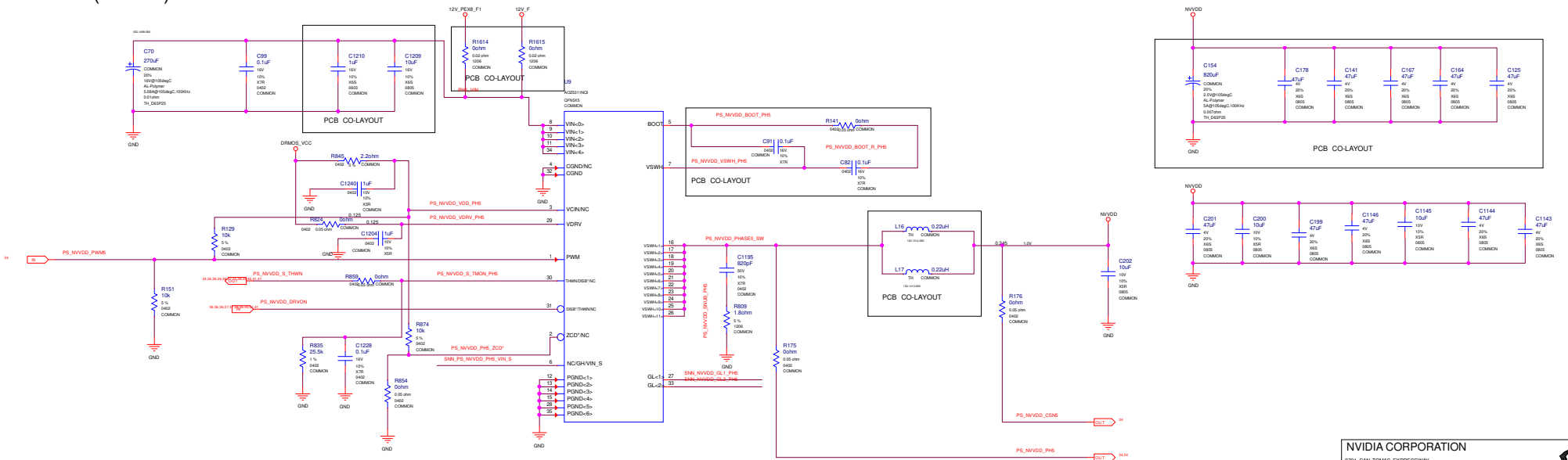
| PCB REV | PG142-B00 | PAGE | 37 OF 54 |
| BOM REV | A | DATE | 27-JUN-2020 |

## NVVDD PH2(PWM2)




## NVVDD PH5(PWM5)







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| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | PS: NVVDD PH2, PH5 |

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| PCB REV | PG142-B00 | PAGE | 38 OF 54 |
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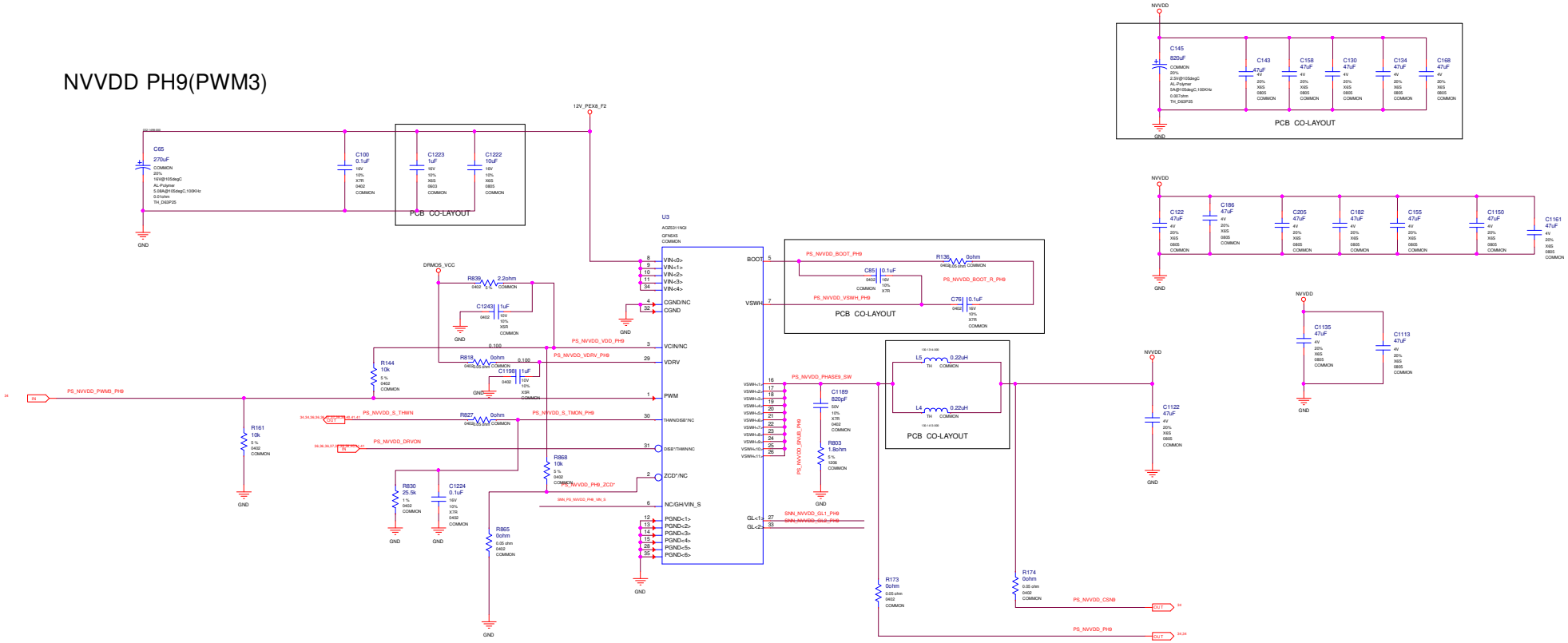
# NVVDD PH9(PWM3)

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| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | PS: NVVDD PH9 |

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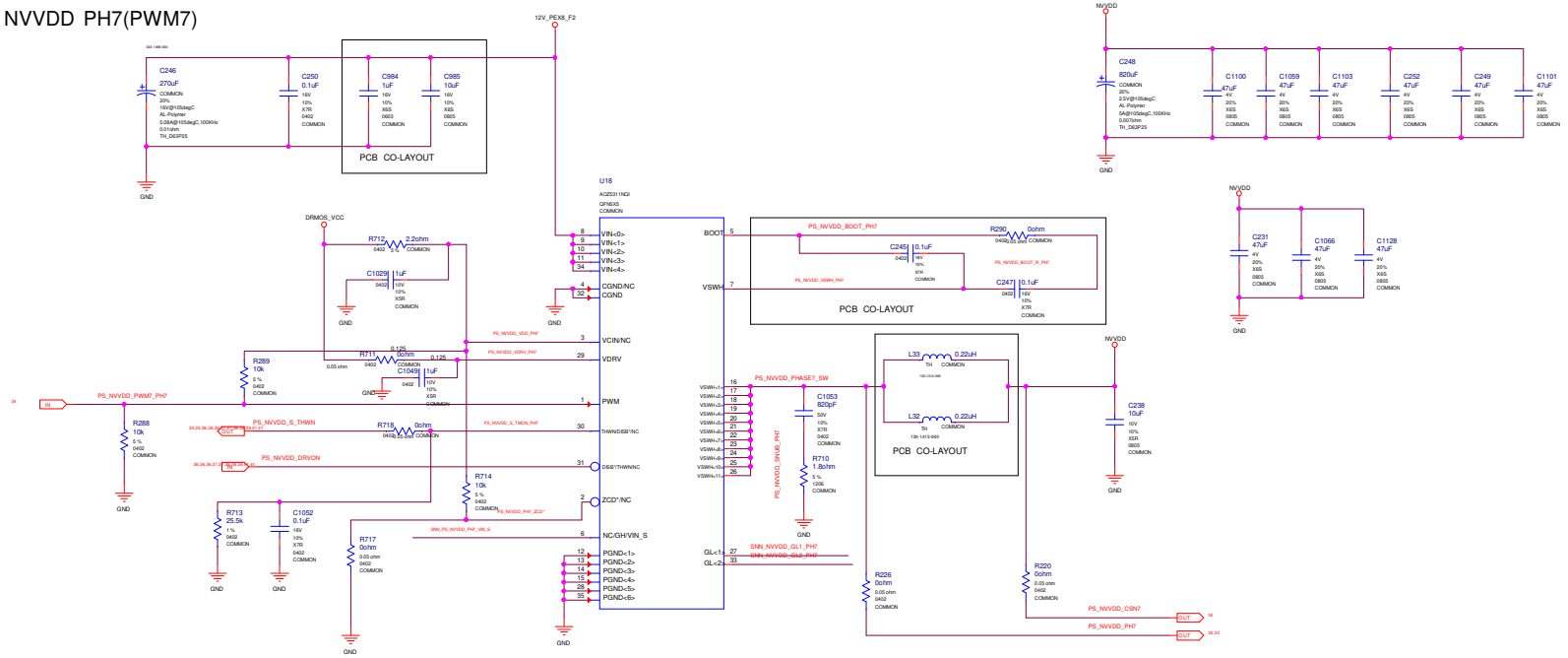
| PCB REV | PG142-B00 | PAGE | 39 OF 54 |
| BOM REV | A | DATE | 27-JUN-2020 |

# Page40: NVVDD PH7

## NVVDD PH7(PWM7)

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| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | PS: NVVDD PH7 |

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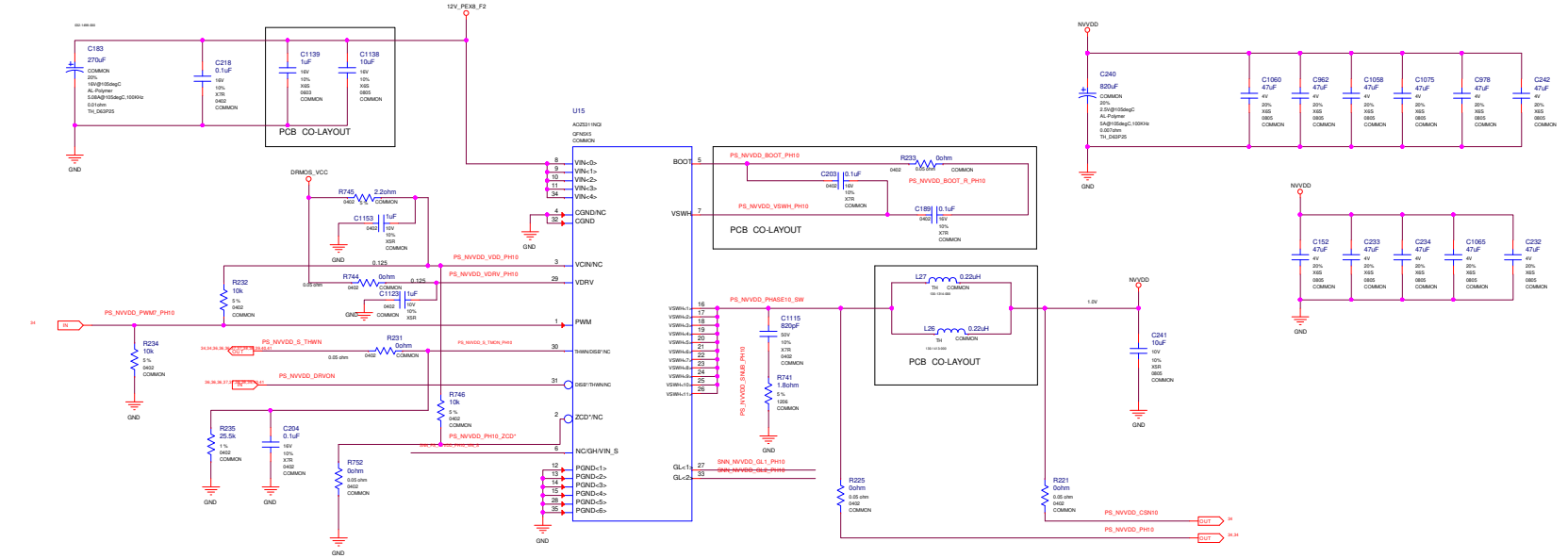
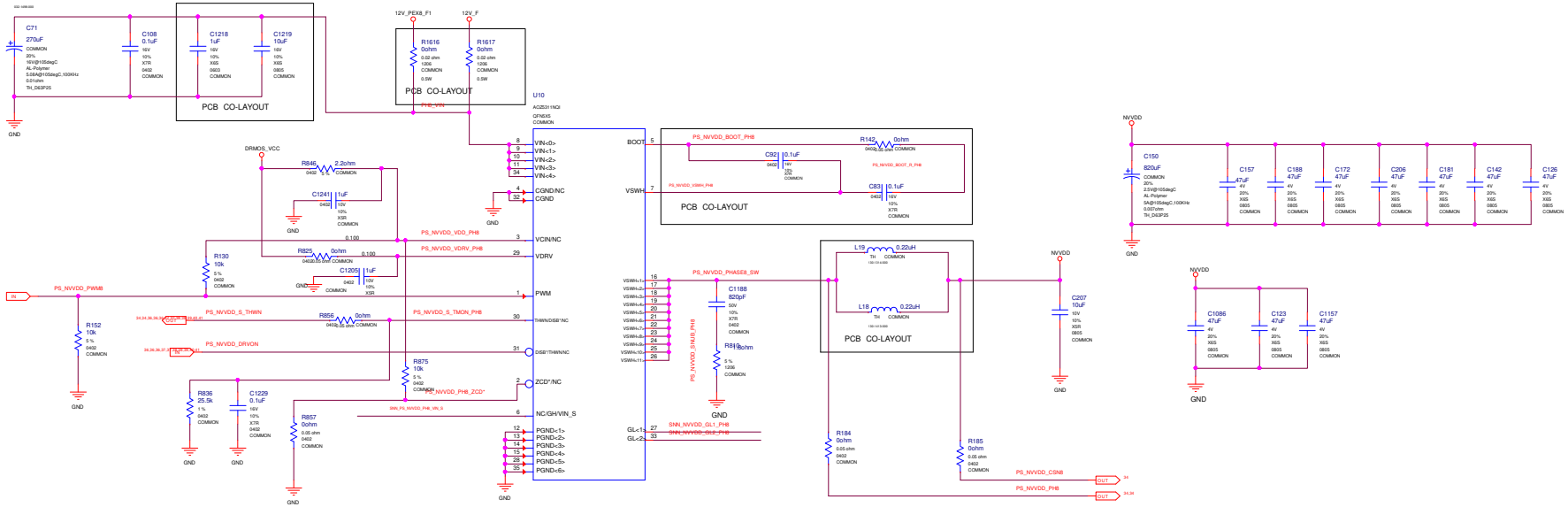
| BOM REV | A | DATE | 27-JUN-2020 |

# Page41: NVVDD PH10 & 8

## NVVDD PH10(PWM7)




## NVVDD PH8(PWM8)

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|---|---|
| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | PS: NVVDD PH10, PH8 |

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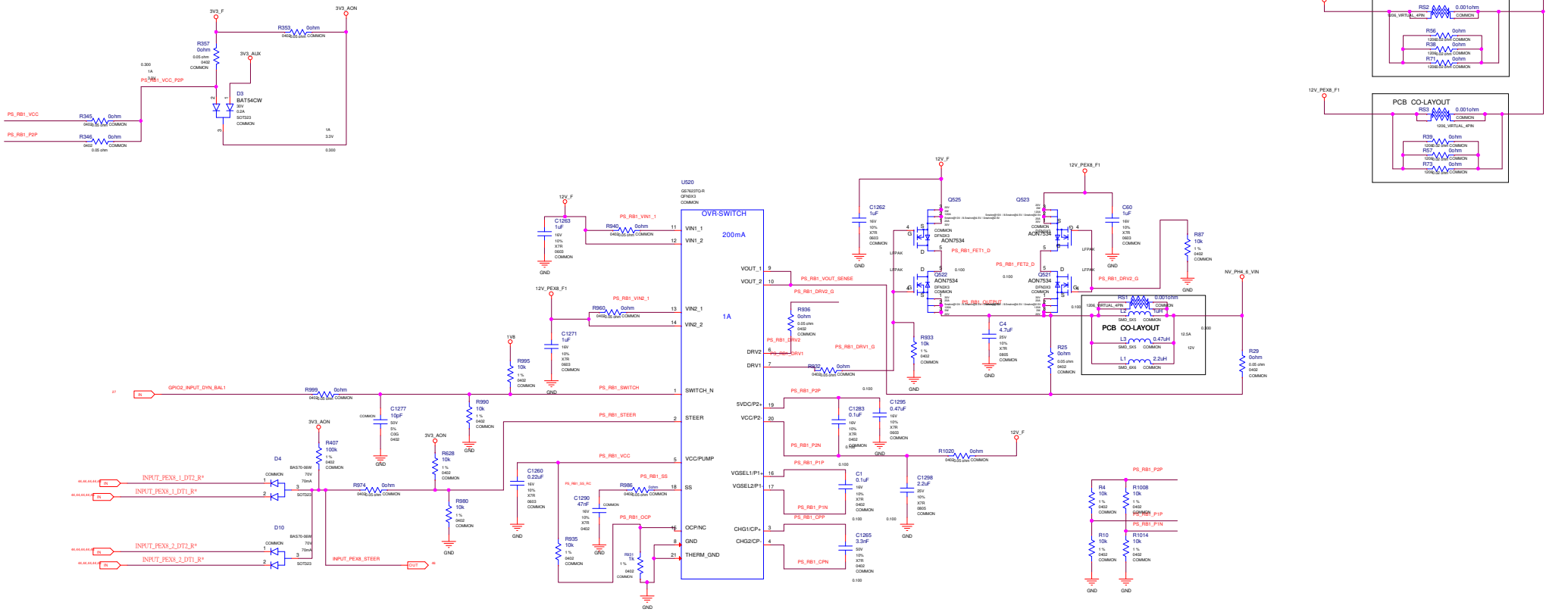
| PCB REV | PG142-B00 | PAGE | 41 OF 54 |
| BOM REV | A | DATE | 27-JUN-2020 |

# Page42: Input Power Balancing Switcher

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|---|---|
| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | PS: OVRS_INPUT POWER BALANCE |

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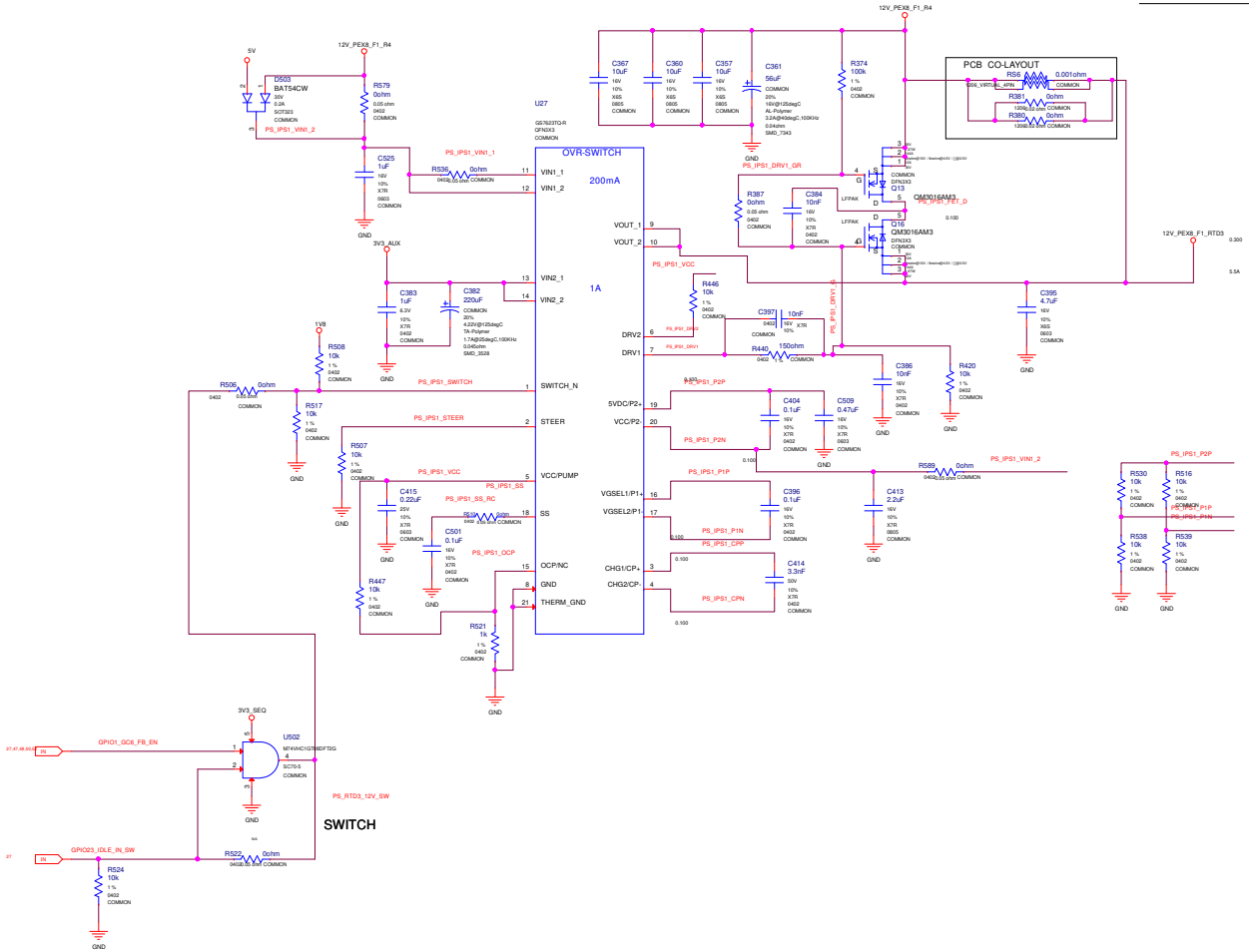
| PCB REV | PG142-B00 | PAGE | 42 OF 54 |
| BOM REV | A | DATE | 27-JUN-2020 |

# Page43: INPUT SWITCH RTD3 (12V & 3V3_A SWITCHER)

AND GATE LOGIC

| GPIO1 | GPIO29 | SWITCH | VOUT |
|---|---|---|---|
| 0 | 0 | 0 | 12V |
| 0 | 1 | 0 | 12V |
| 1 | 0 | 0 | 12V |
| 1 | 1 | 1 | 3V3A |

| SWITCH | VOUT |
|---|---|
| 0 | VOUT = VIN1 |
| 1 | VOUT = VIN2 |

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|---|---|
| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | PS: RDT3_12V & 3V3_A Switcher |

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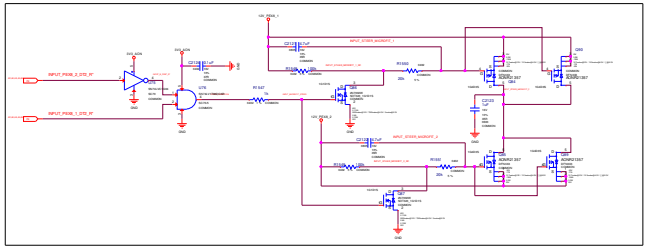
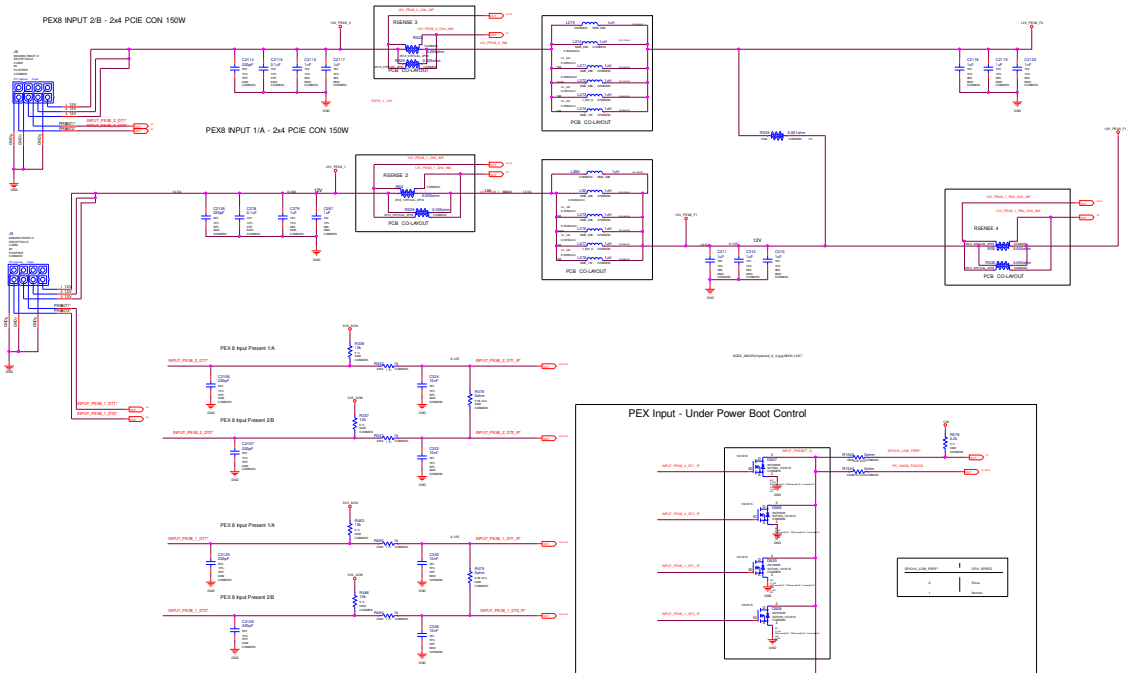
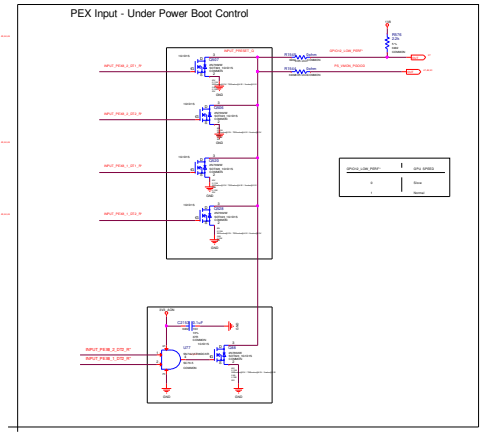
| BOM REV | A | DATE | 27-JUN-2020 |

# Page44: 12V_EXT_INPUT, FILTERING & UNDER POWER BOOT



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| PRODUCT DATEMA | PN: 5M5TE, PCI/PMU and SENSORMD |

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| | | | |
|---|---|---|---|
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| TOP SIZE | PCI-E X16 | PAGE | 44 OF 64 |
| SCHREV | A | DATE | 07-JUN-2018 |


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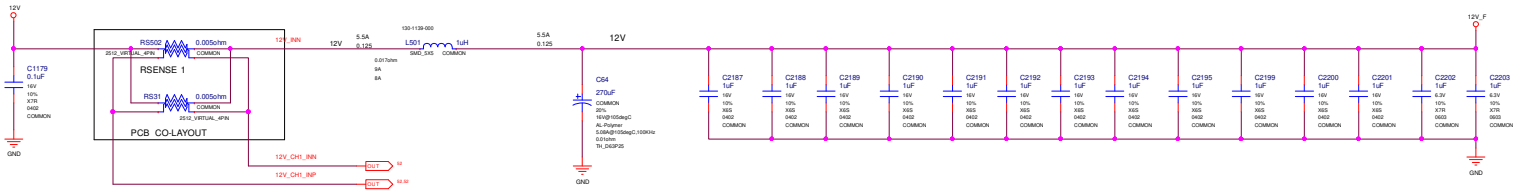
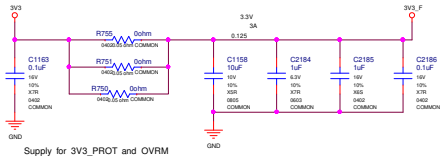
# Page45: PEX_INPUT & FILTERING, PEX_3V3, 3V3_AUX

## PEX_12V INPUT - 66W

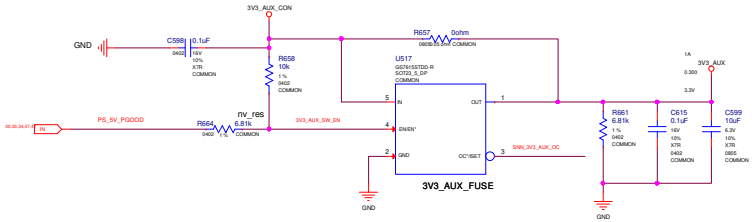



## PEX 3V3 INPUT - 10W




Supply for 3V3_PROT and OVRM

## 3V3_AUX

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|---|---|
| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | PS: PEX_12V, PEX_3V3 AND A3V3_AUX |

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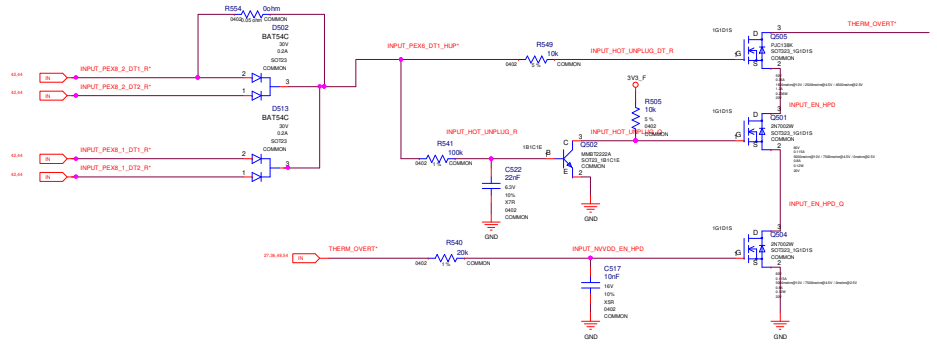
| BOM REV | A | DATE | 27-JUN-2020 |

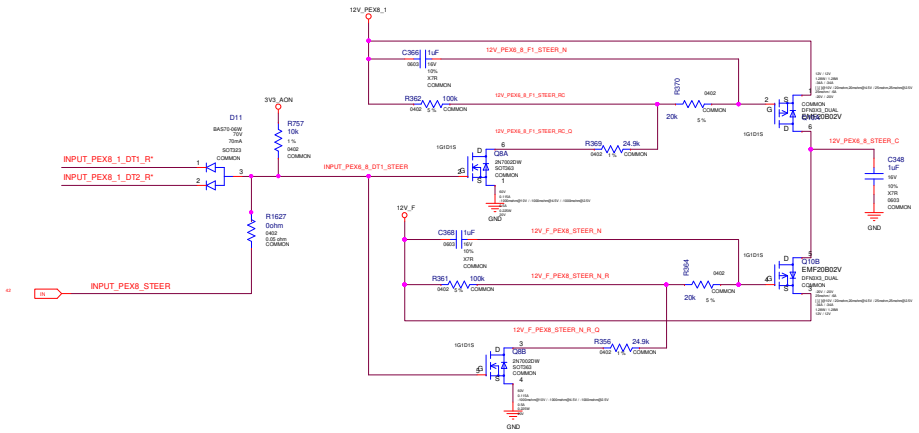
# Page46: STEERING, UPB, HOT UNPLUG

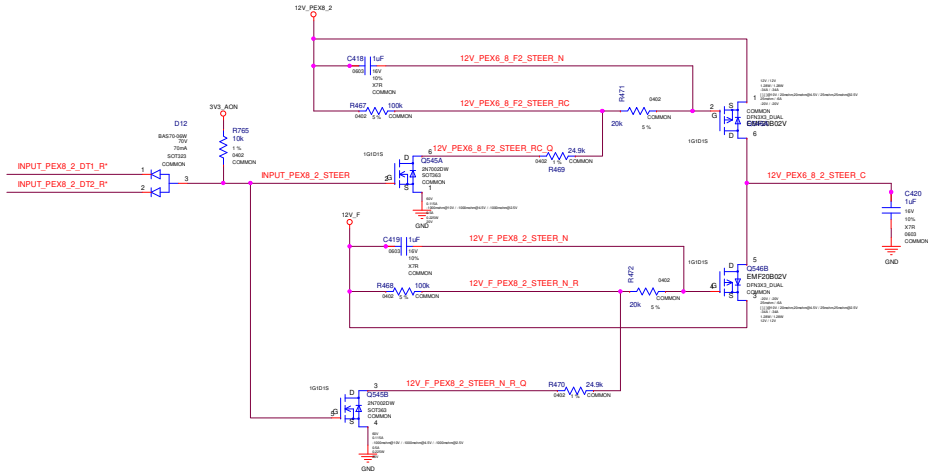
## POWER CONNECTOR HOT-UNPLUG DETECT




## 12V CURRENT STEERING (UNDER POWER BOOT):

**GUIDES CURRENT FROM PEX EDGE TO PEX 8 PIN INPUT AREA**

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|---|---|
| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | PS: STEERING, UPB, HOT UNPLUG |

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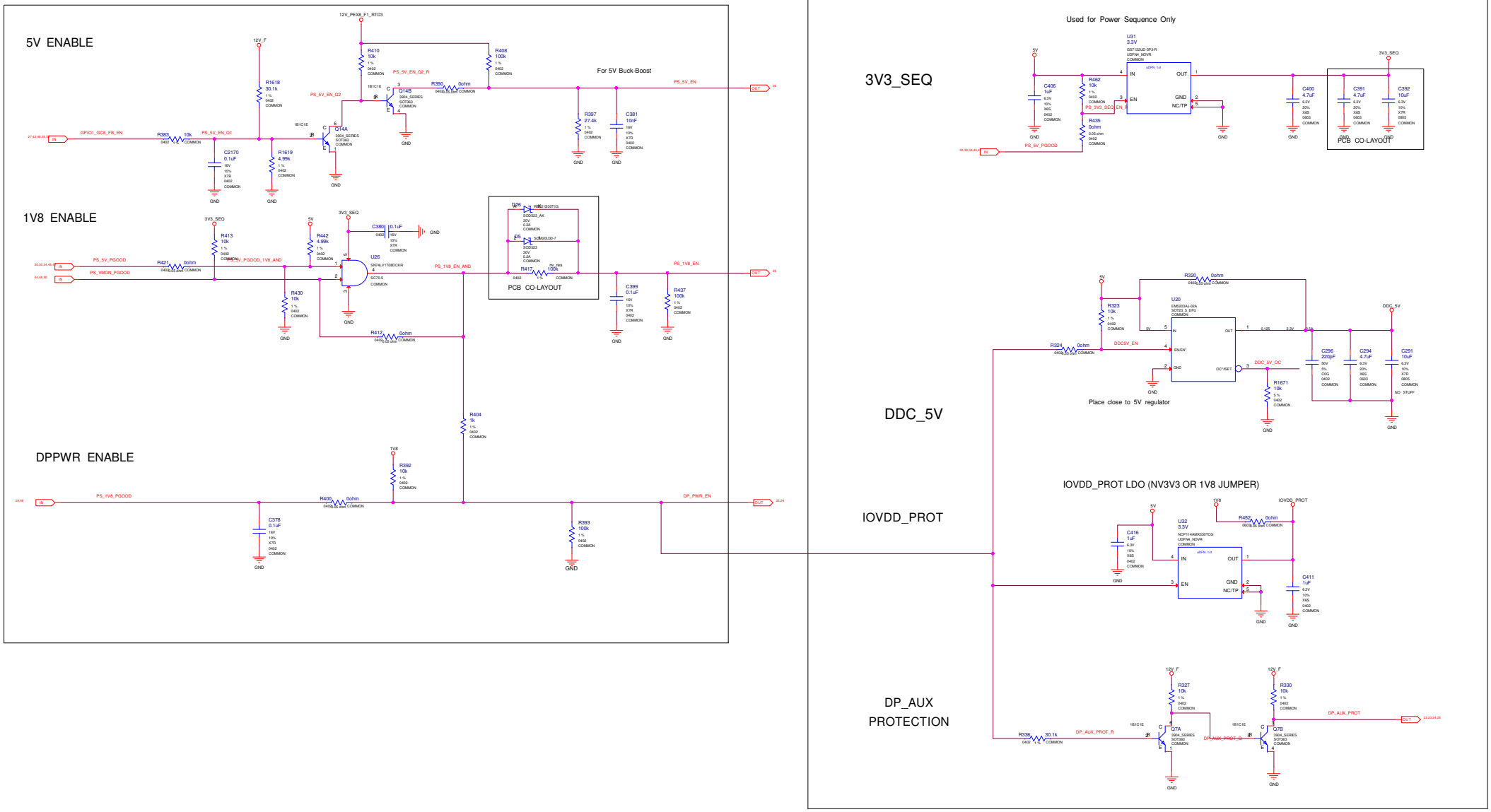
| BOM REV | A | DATE | 27-JUN-2020 |

# Page47: SEQ: 5V, 1V8, 3V3_SEQ, DDC_5V, DP_AUX_PROT




| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
|---|---|
| PAGE DETAIL | SEQ: 5V 1V8, 3V3_SEQ |

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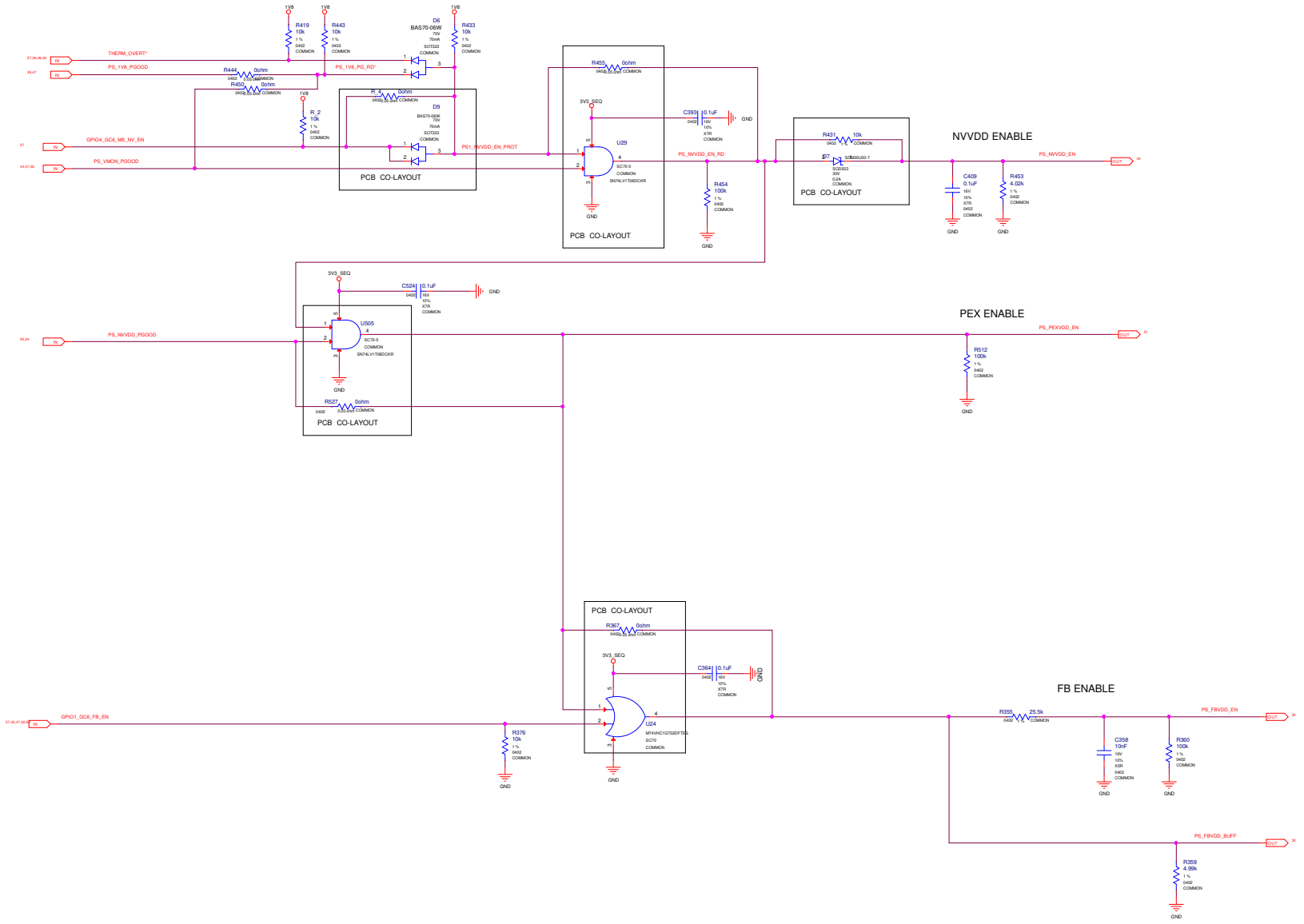
| BOM REV | A | DATE | 27-JUN-2020 |

# Page48: SEQ:NVVDD, PEX, FBVDDQ ENABLE

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| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | SEQ: NVVDD, PEX, FBVDDQ ENABLE |

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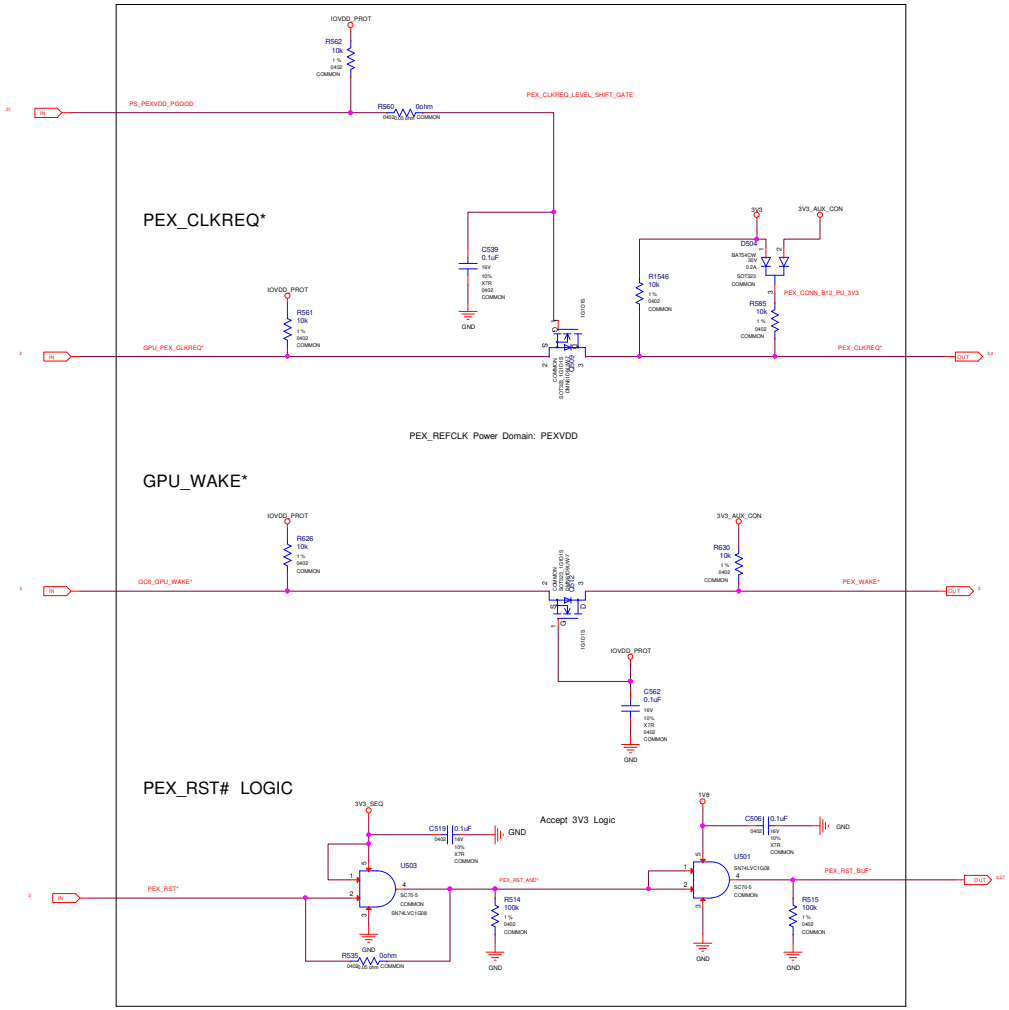
# Page49: SEQ:MISC

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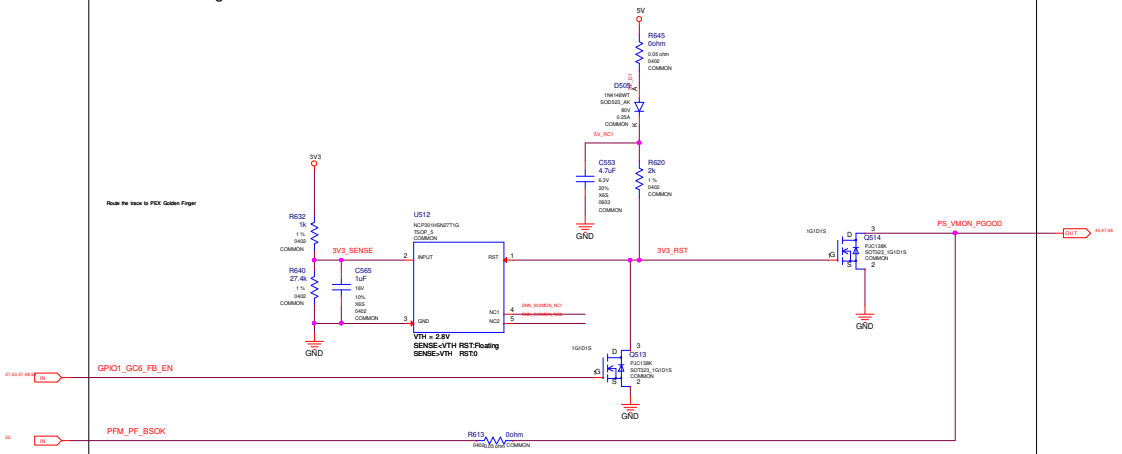
## 3V3PEX Voltage Monitor




### BOM Configuration

| OPTIONS | PEX3V3_SENSE | PEX12V_SENSE | OTHER_12V_SENSE |
|---|---|---|---|
| Use Pre-Filter | Pre-Filter | Pre-Filter | Pre-Filter |
| NO Pre-Filter | Voltage_Monitor | Voltage_Monitor | N/A |

| Signal | Direction | Function |
|---|---|---|
| 3V3 | INPUT | Sense the 3V3 Voltage from PCIE golden finger |
| 12V | INPUT | Sense the 12V Voltage from PCIE golden finger |
| PS_VMON_PGOOD | OPEN-DRAIN | Floating(H) once both 3V3 and 12V reach Vth |
| GC6_FB_EN | INPUT | Indicator for RTD3/GC6 residence,Use to Mask the VMON_PGOOD |
| PS_PF_SKIP | INPUT | From INA3221(VPU) or Pre-filter(SKIP) |
| PS_PF_BSOK | INPUT | From INA3221(PV) or Pre-filter(BS_OK) |

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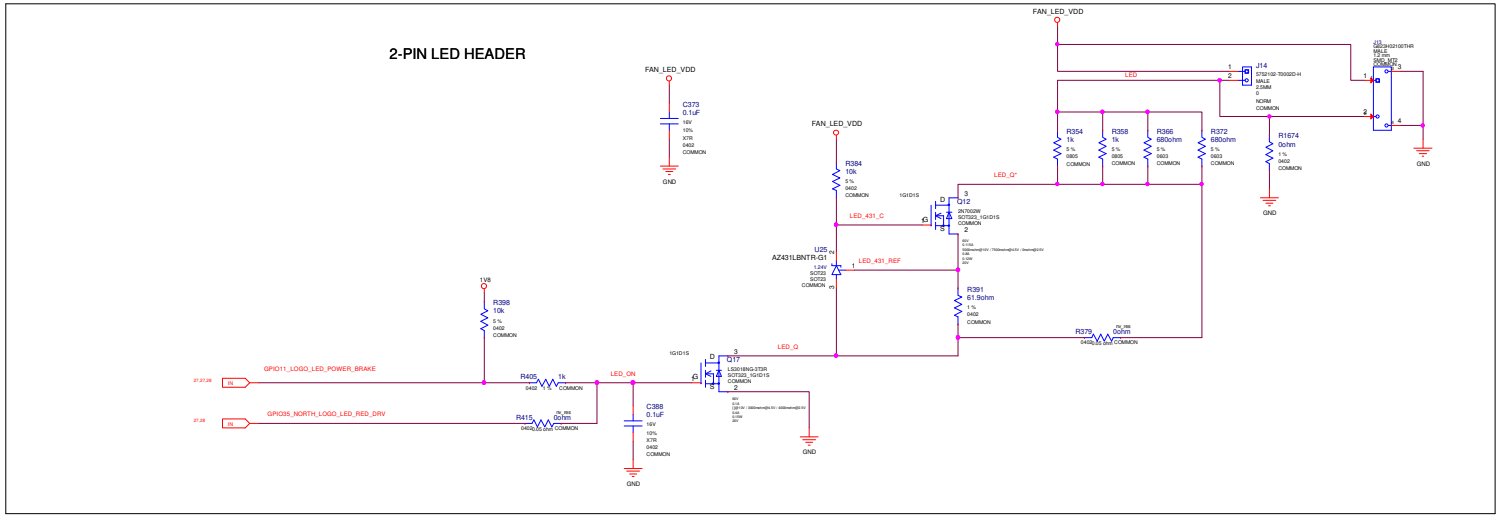
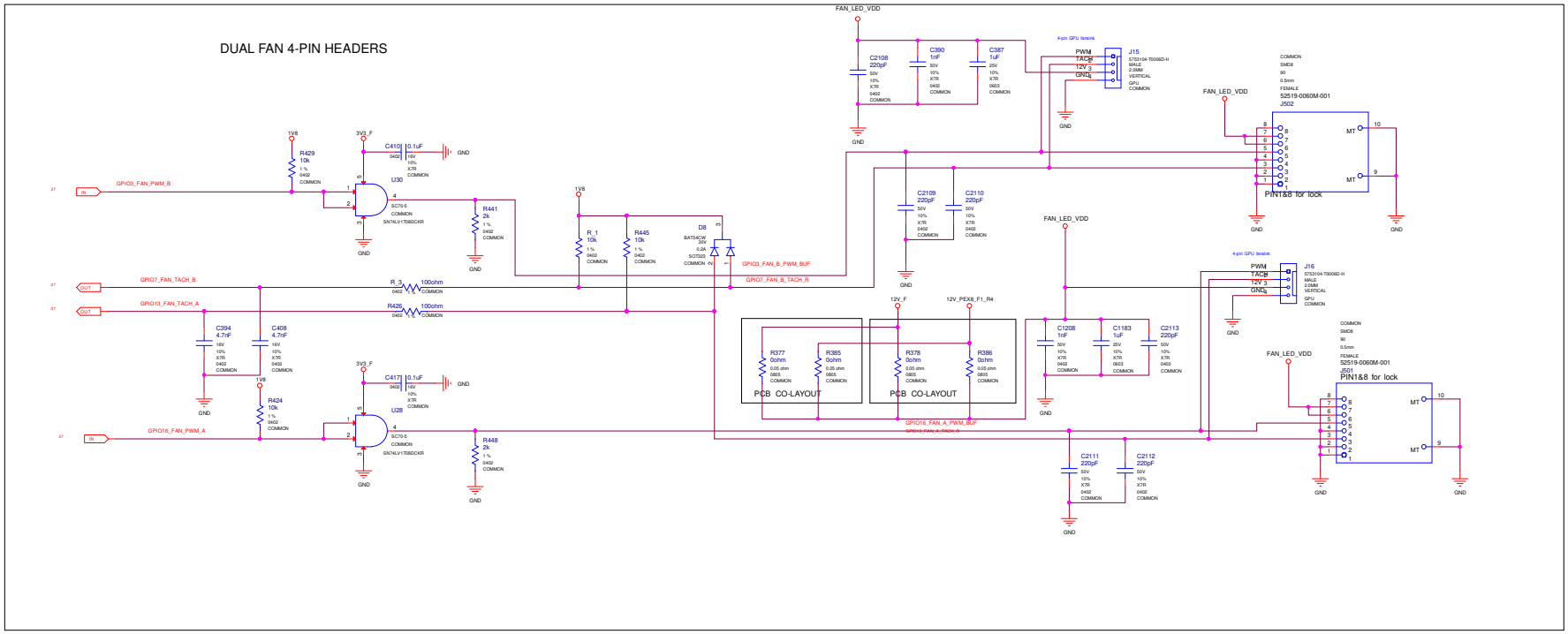
# Page51: FAN&LED

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| PAGE DETAIL | FAN & LED |

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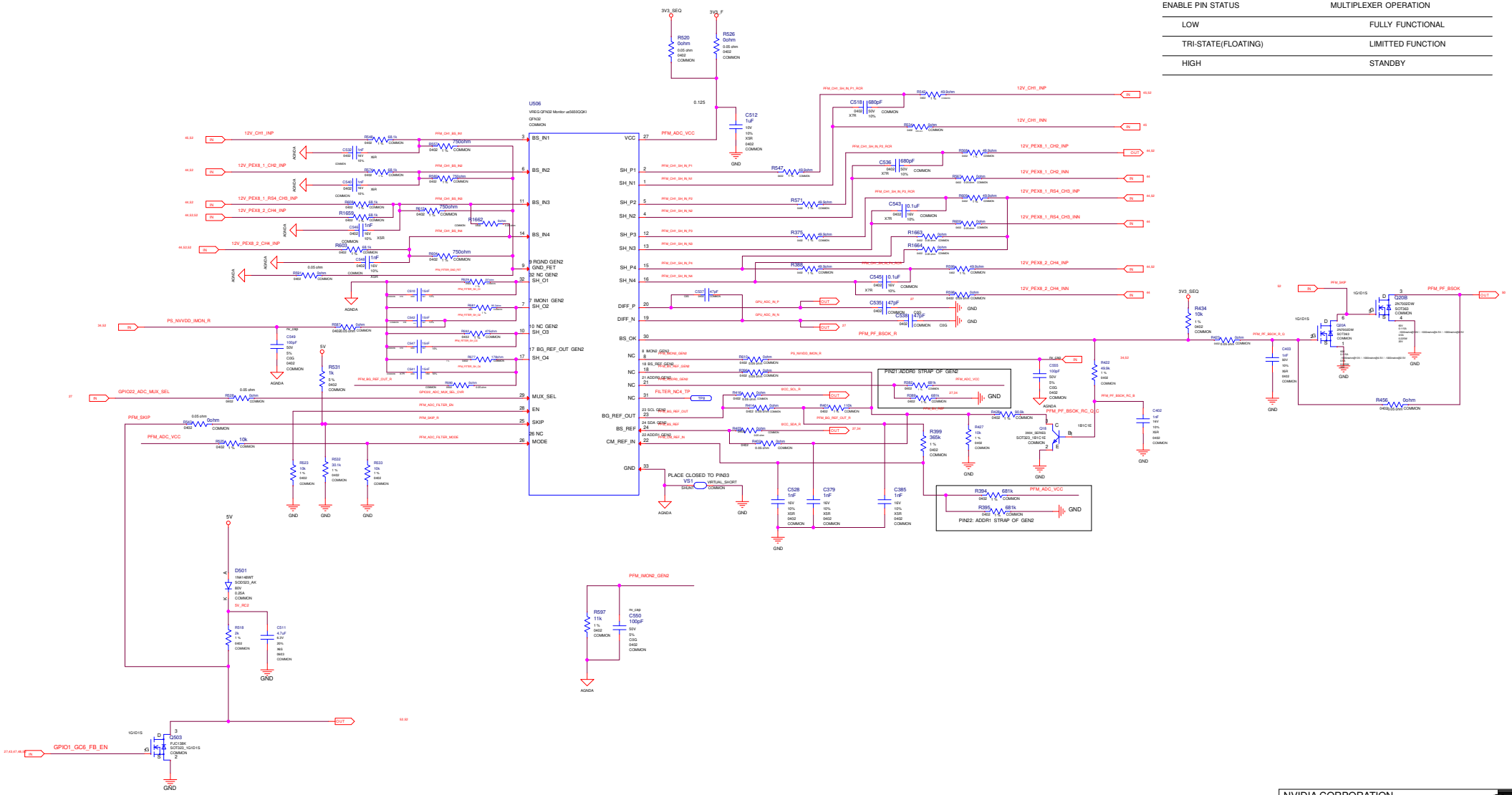
# Page52: OVRM_PWR SENSE

| MODE PIN STATUS | MULTIPLEXER OPERATION |
|---|---|
| LOW | DEVICE A |
| TRI-STATE(FLOATING) | STAND-ALONE |
| HIGH | DEVICE B |

| ENABLE PIN STATUS | MULTIPLEXER OPERATION |
|---|---|
| LOW | FULLY FUNCTIONAL |
| TRI-STATE(FLOATING) | LIMITTED FUNCTION |
| HIGH | STANDBY |




| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
|---|---|
| PAGE DETAIL | PS:OVRM_PWR_SENSE |

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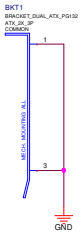
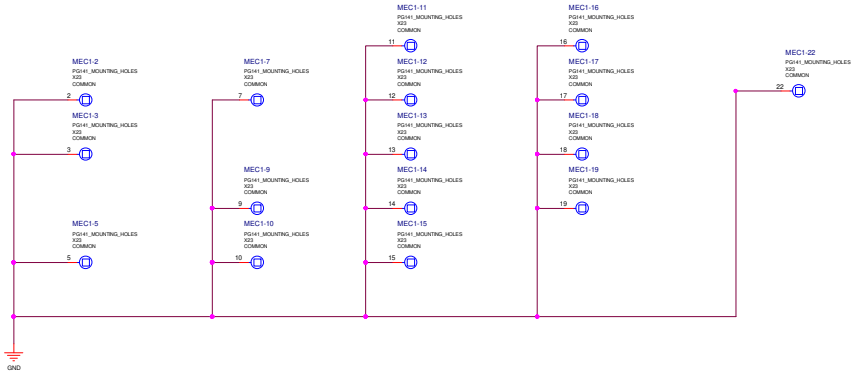
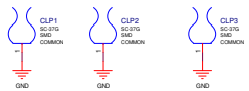
# Page53: MECH

Bracket:

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| ASSEMBLY | <ASSEMBLY_DESCRIPTION> |
| PAGE DETAIL | MECH |

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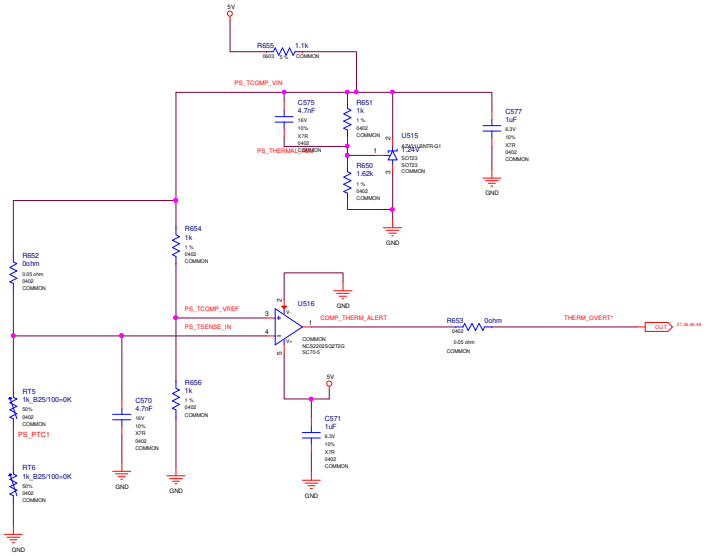
Close to FBVDD MOS

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