GA102 DT SKU P-BOARD

350W, FH Std PCB, 384b, GDDR6X x8
DP + DP + DP + HDMI/DP

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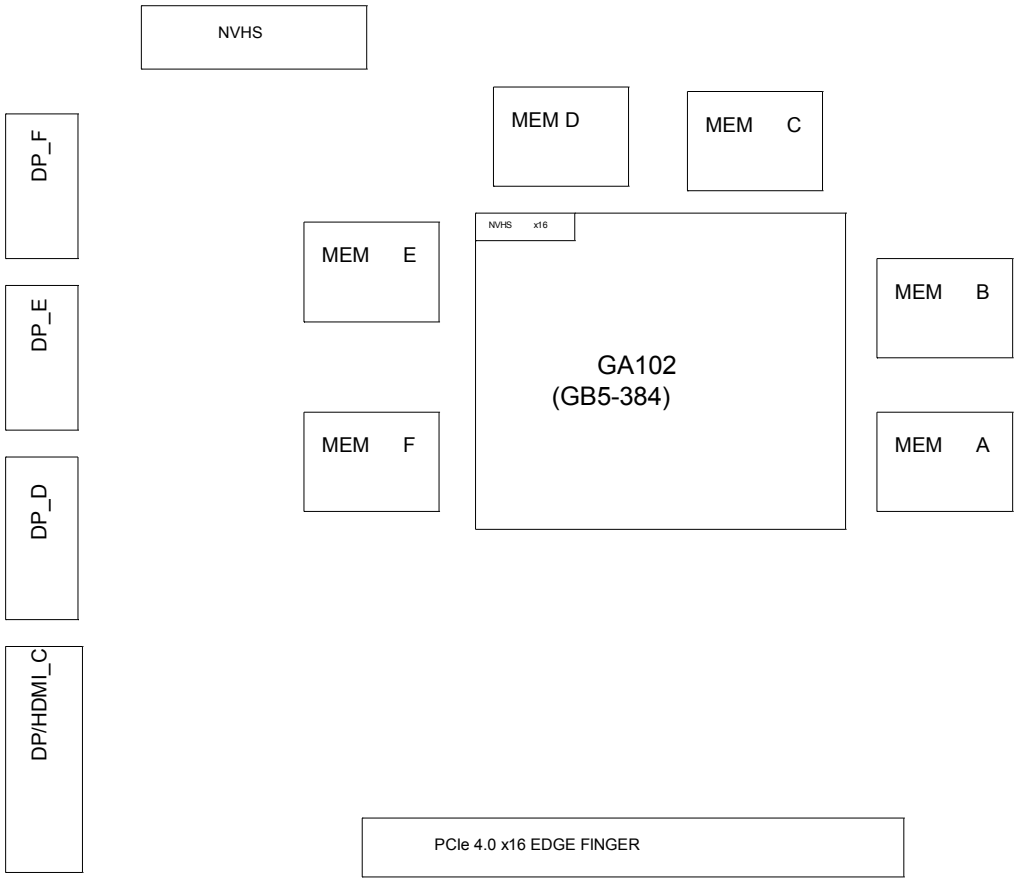
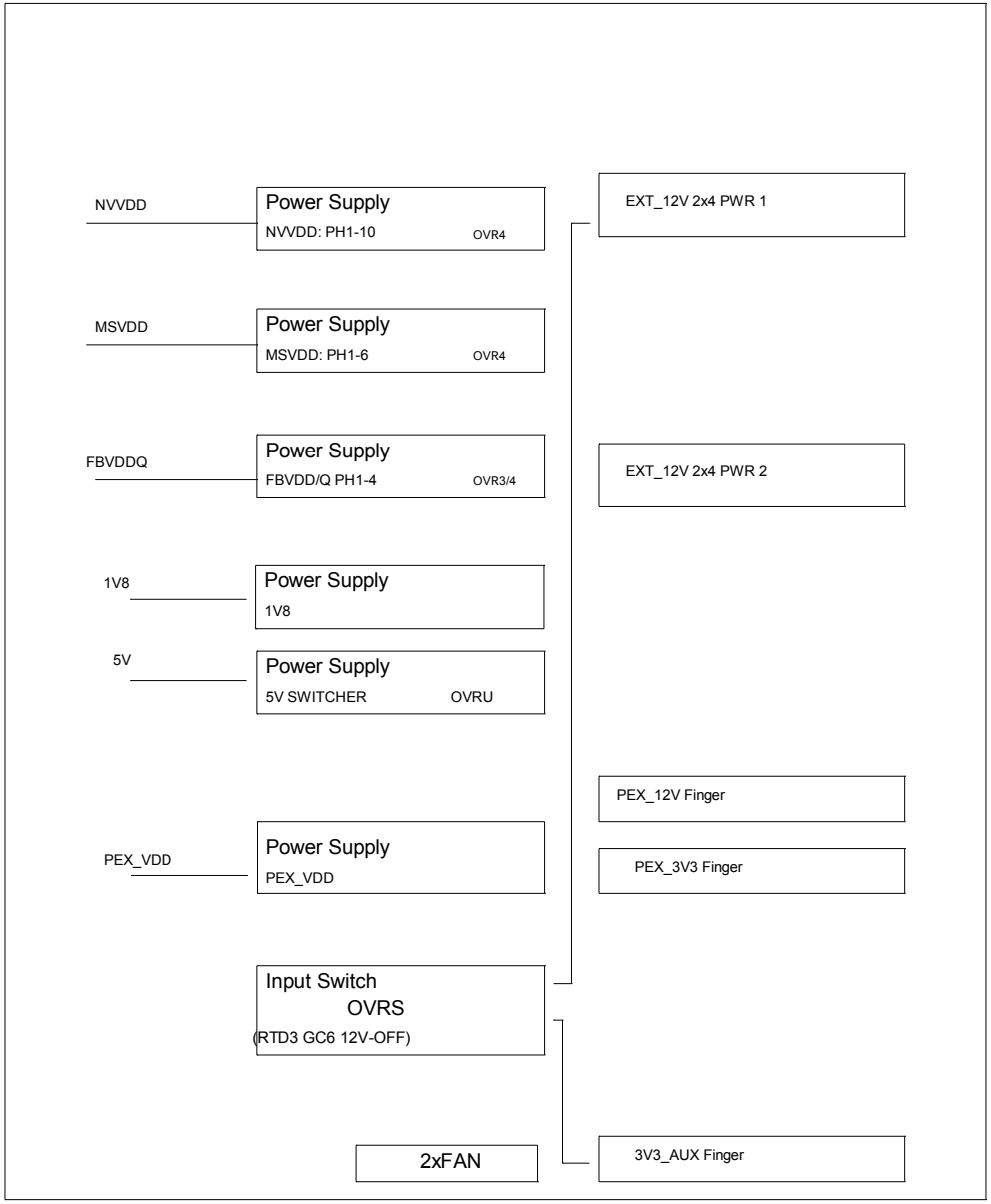
Block Diagram





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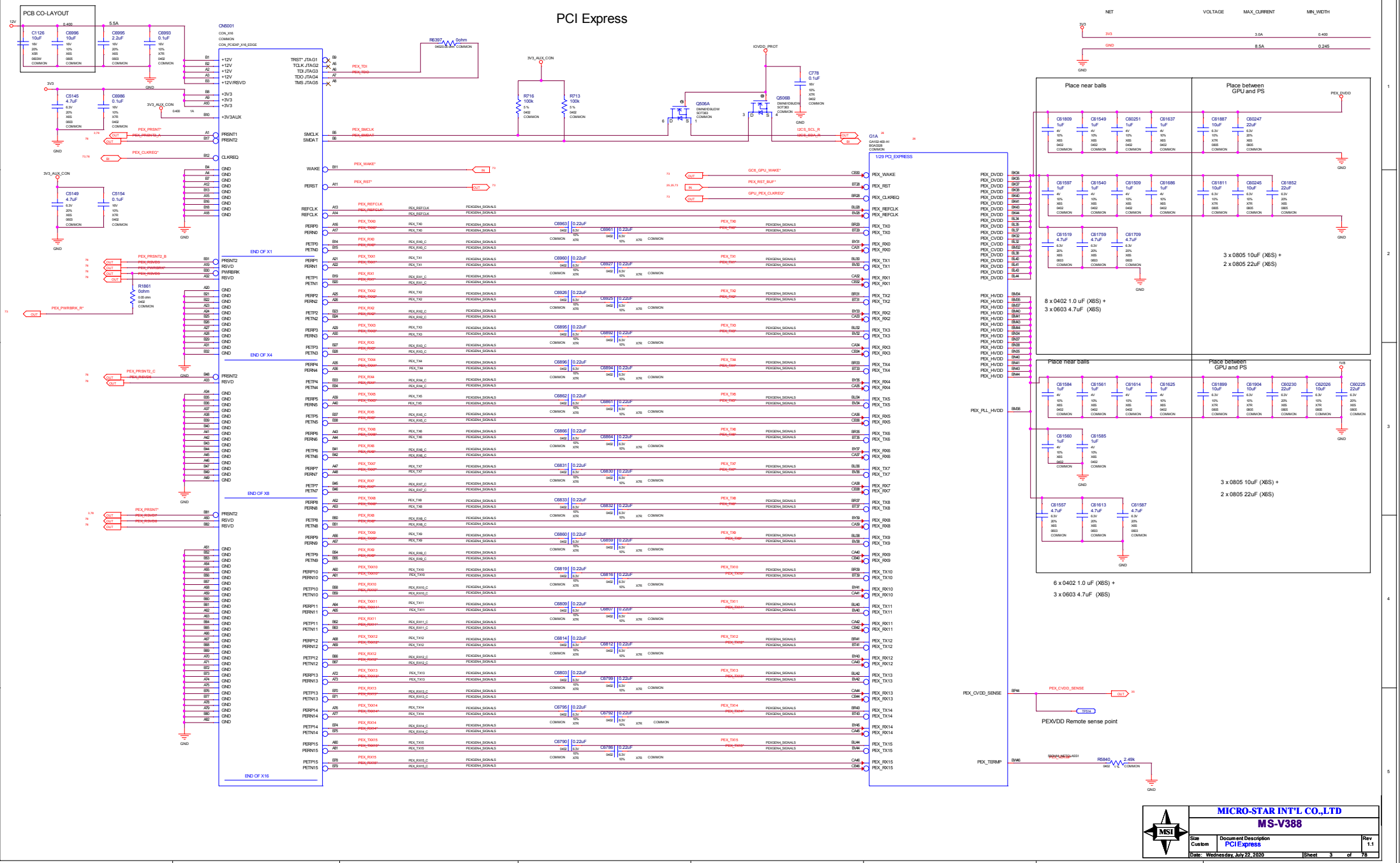
PCI Express



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
3V3	3V3	3.0A	0.400
GND		8.5A	0.245

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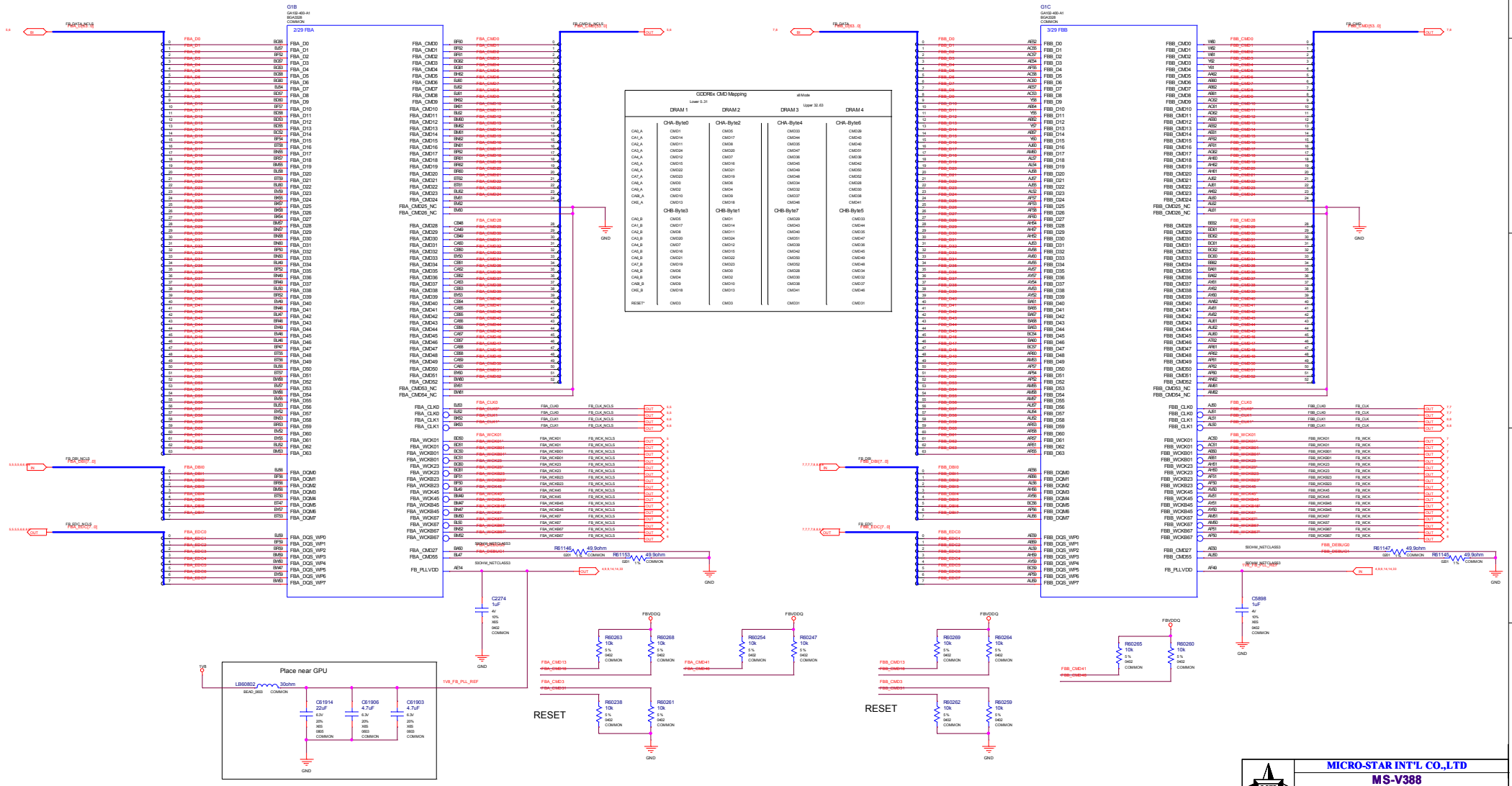
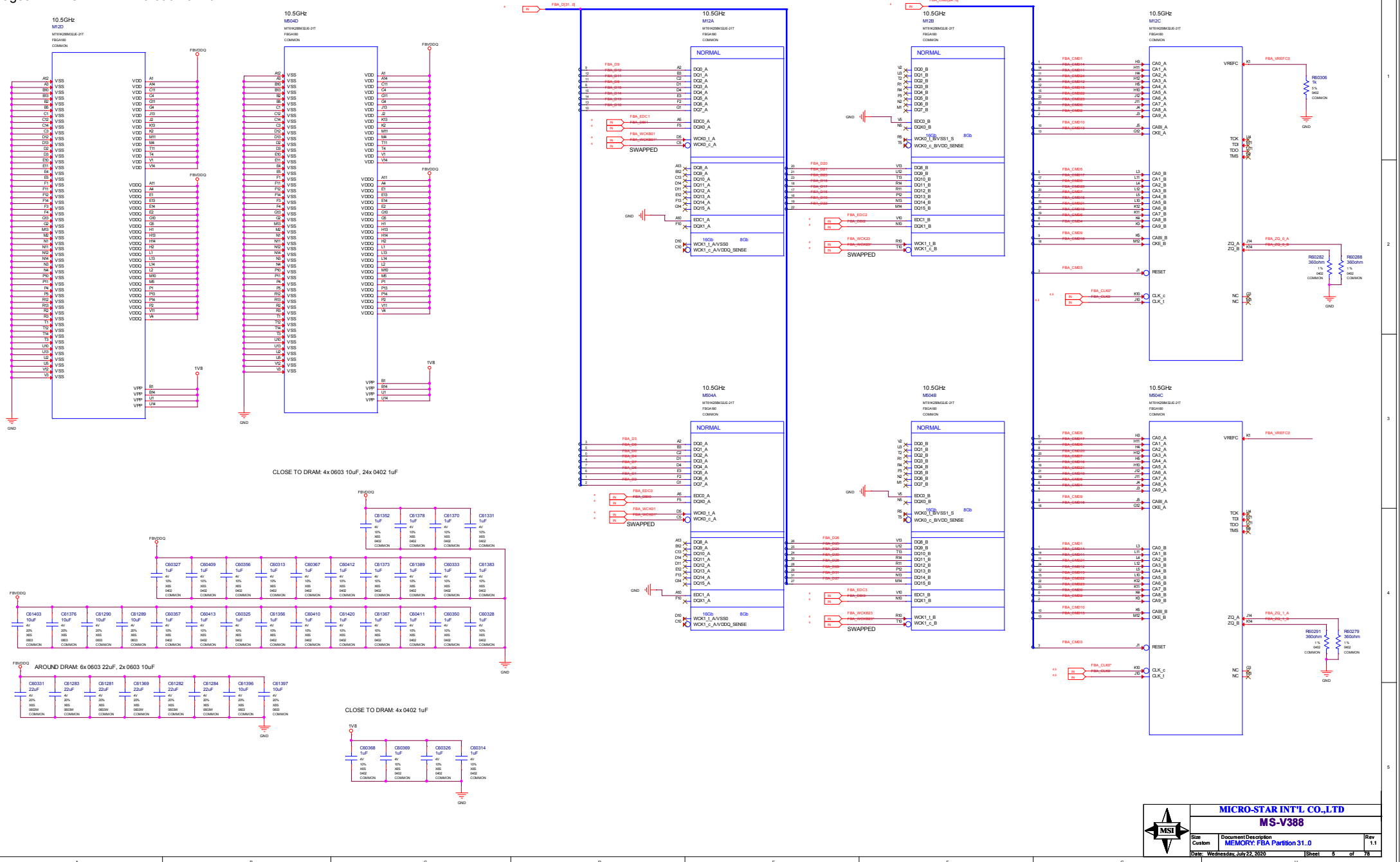
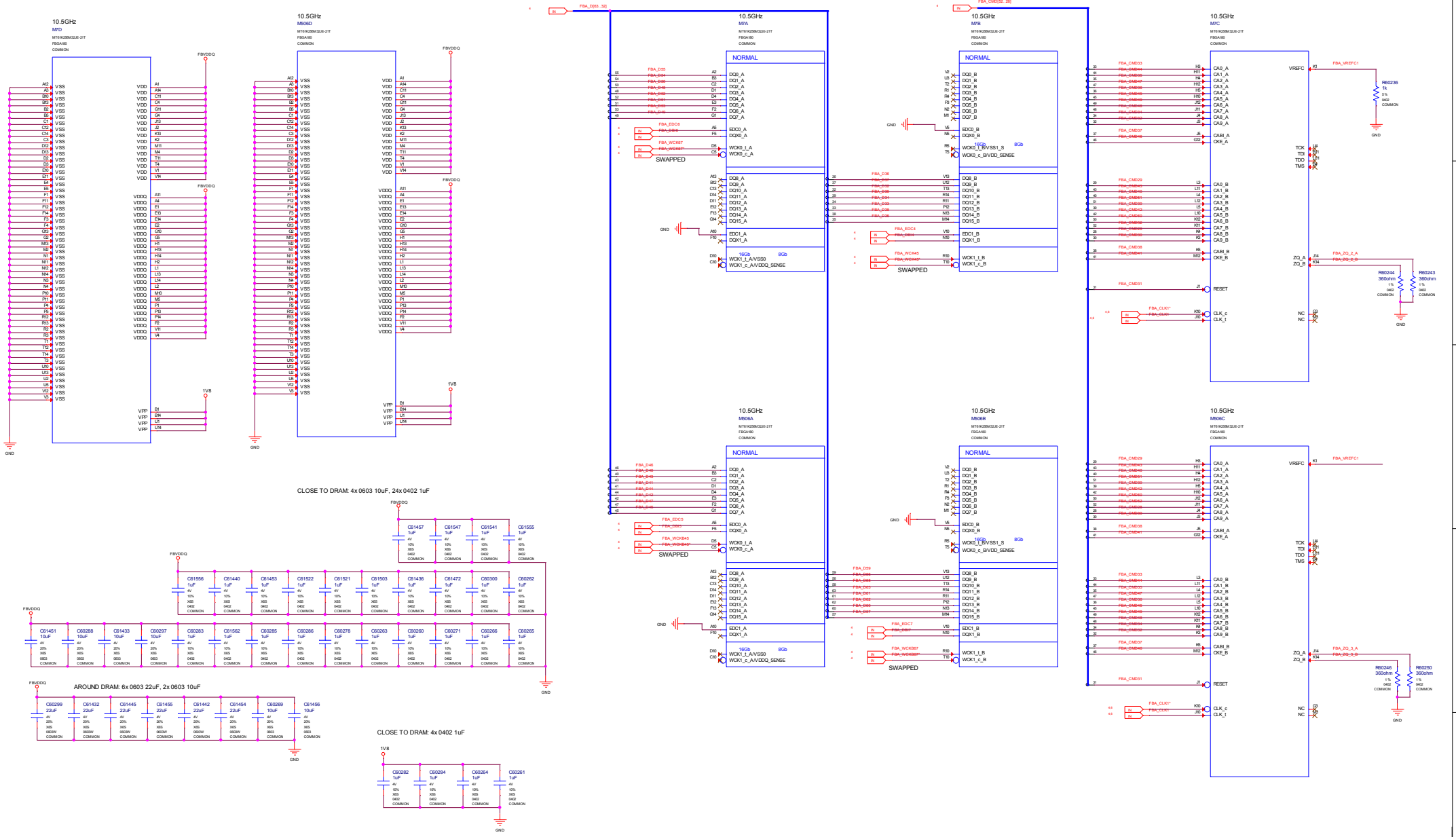
MEMORY: GPU Partition A/B



Page5: MEMORY: FBA Partition 31..0



Page6: MEMORY: FBA Partition 63..32



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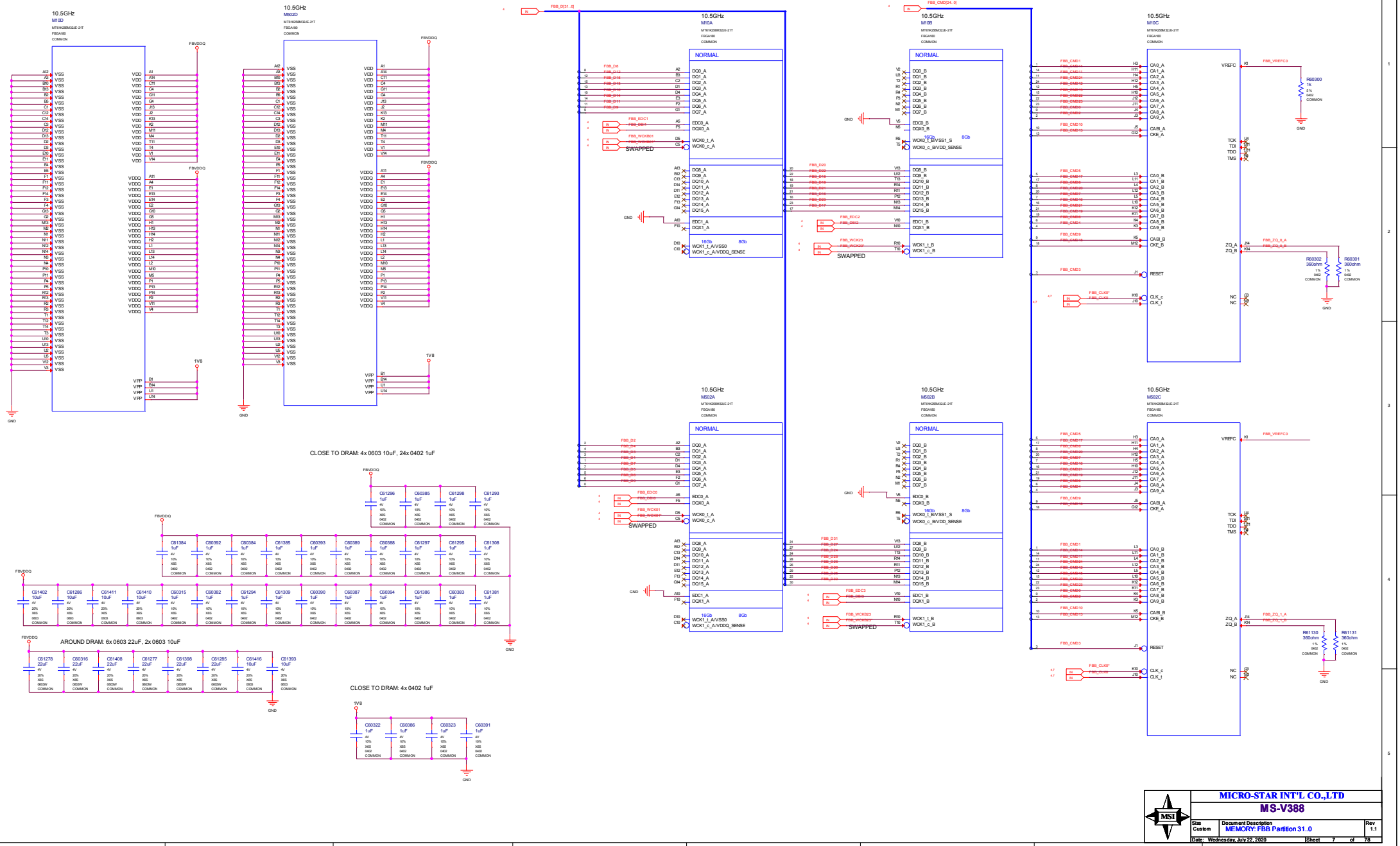
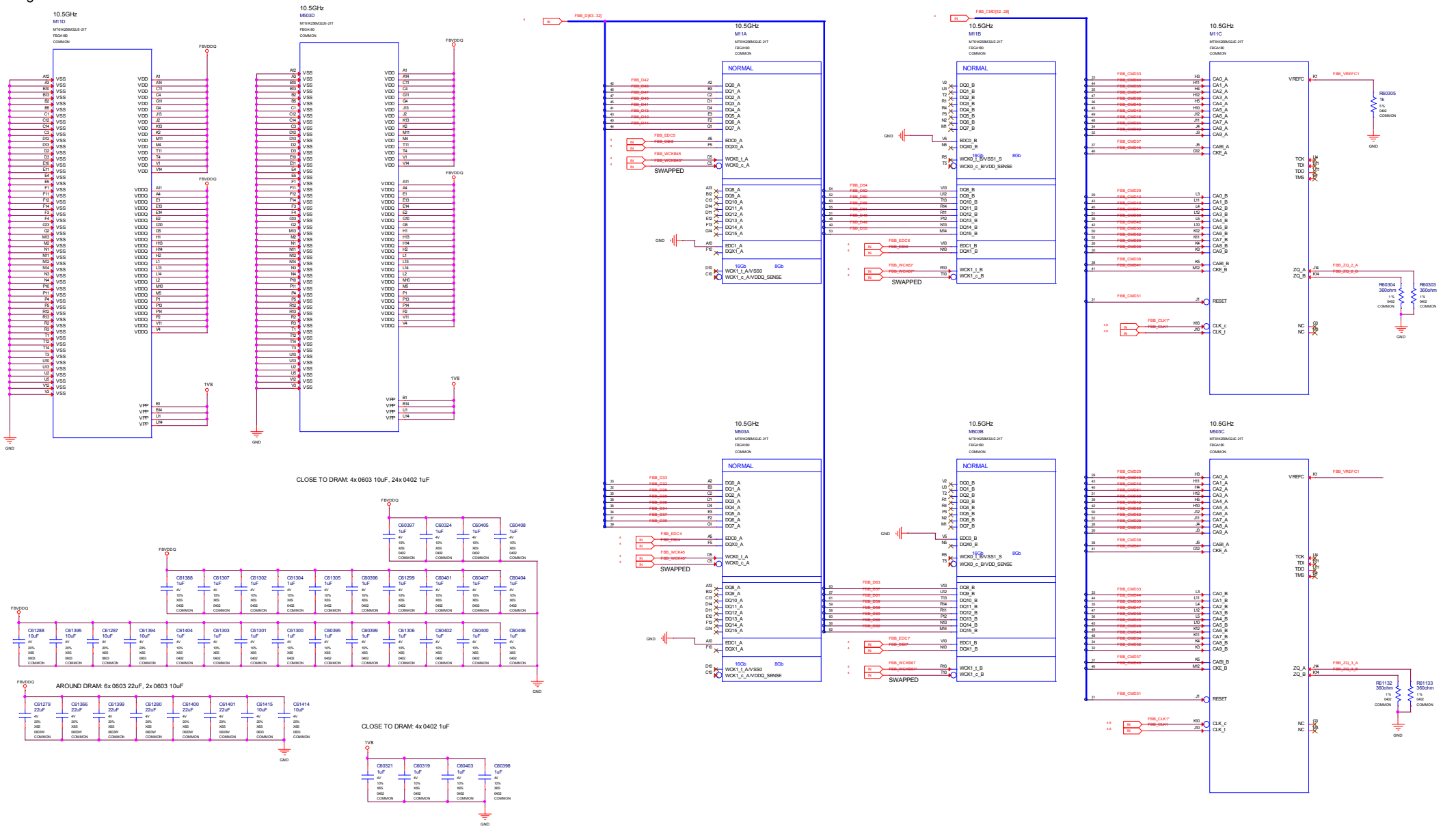
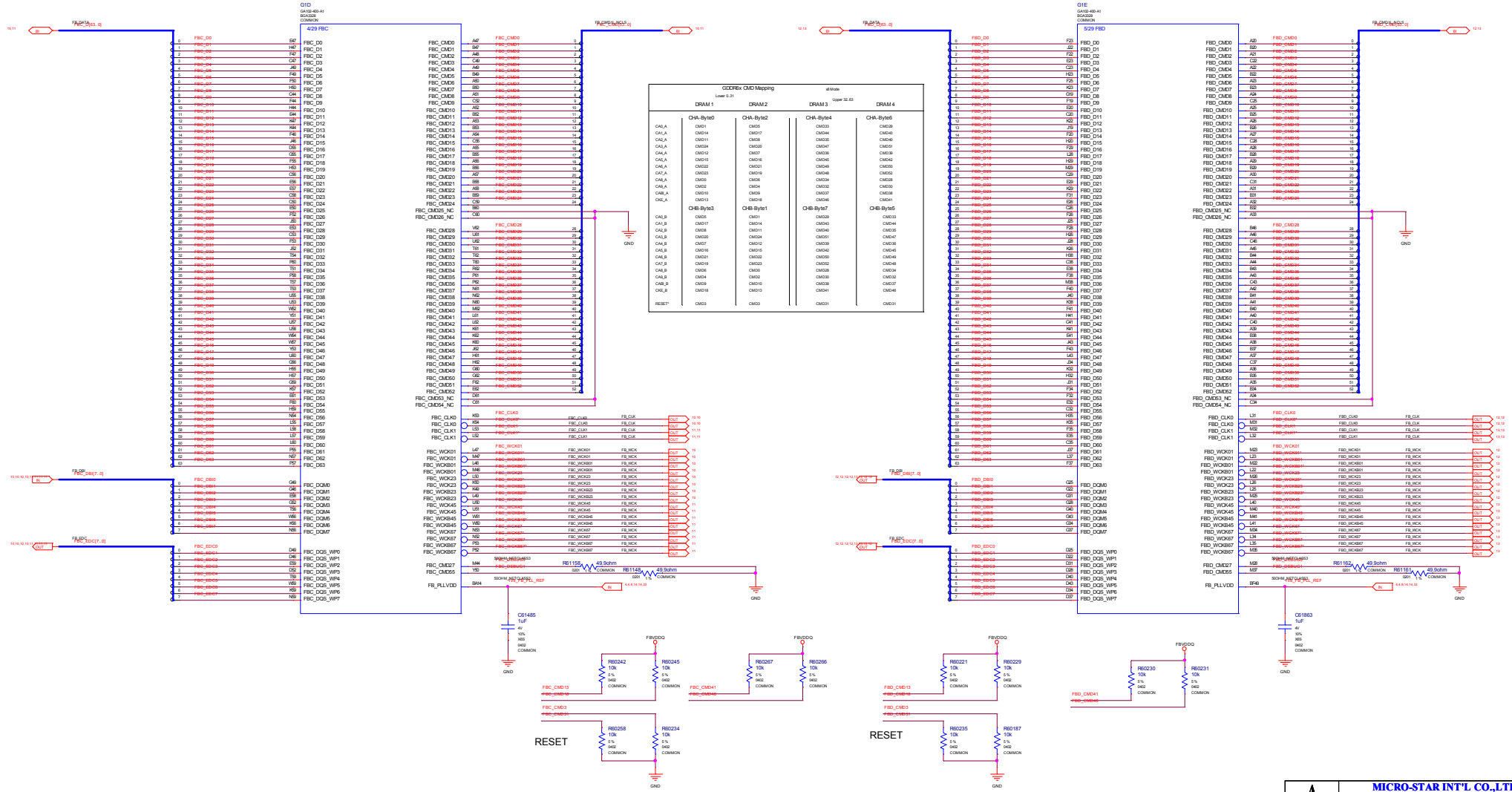
Page7: MEMORY: FBB Partition 31..0



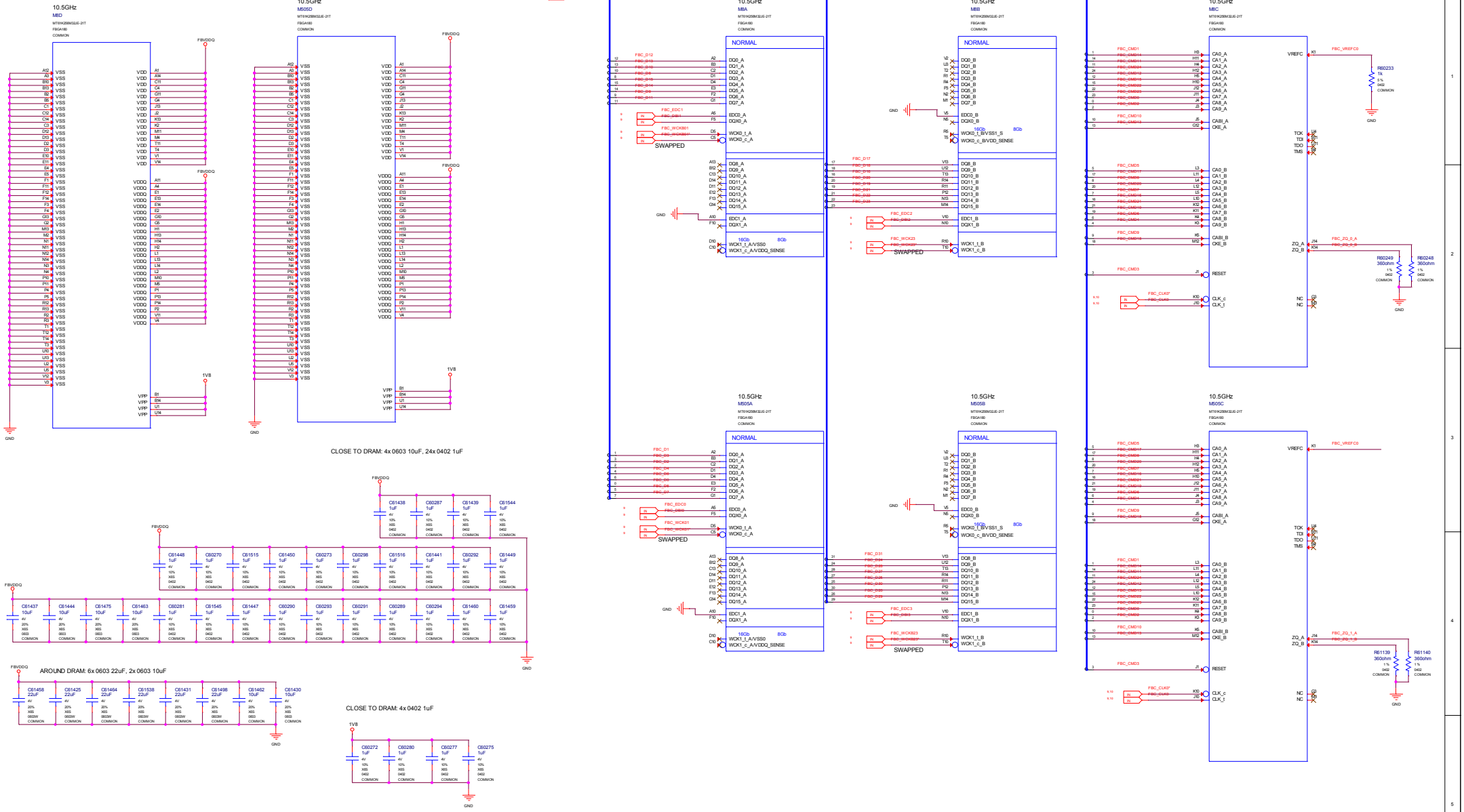
Page8: MEMORY: FBB Partition 63..32



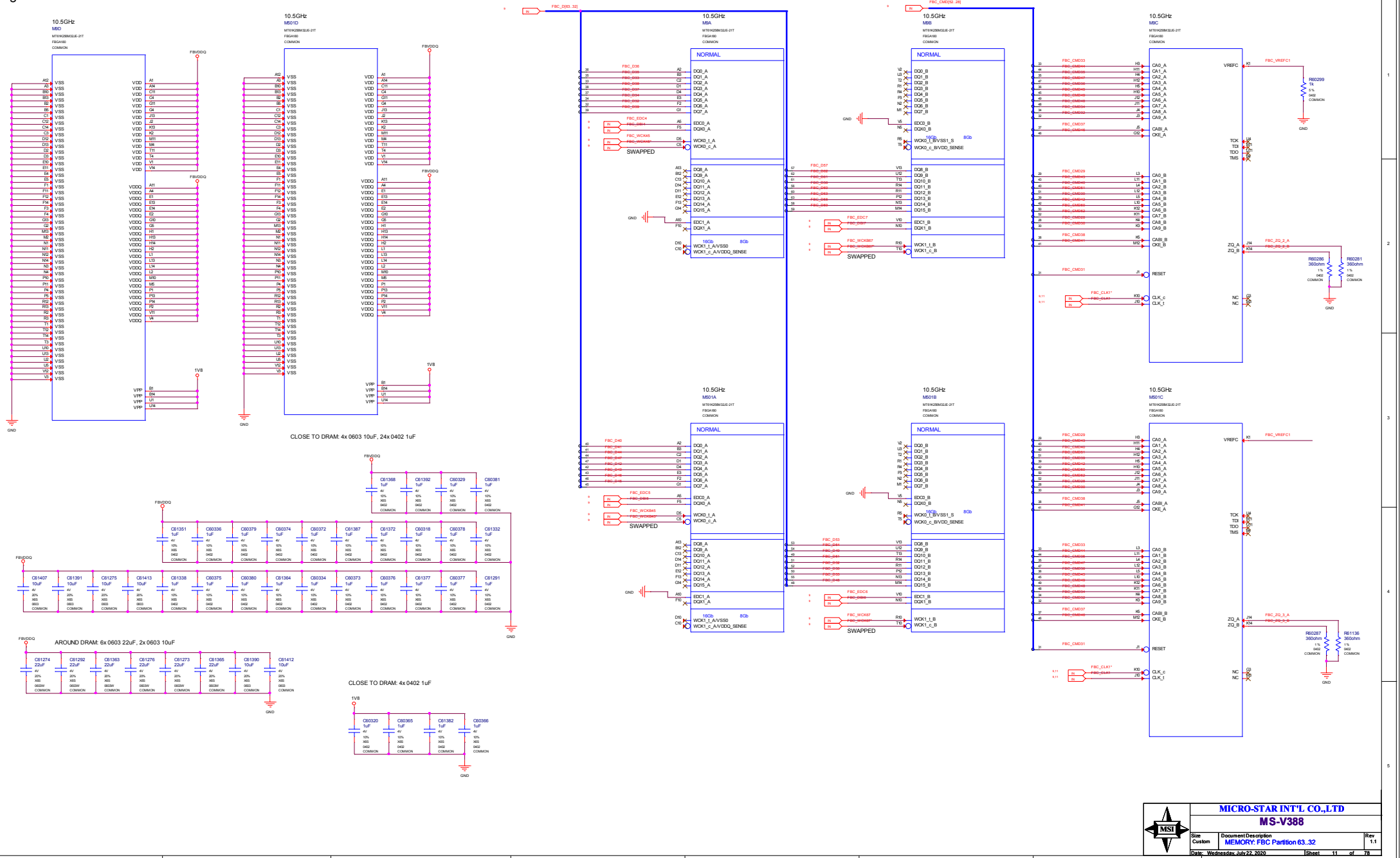
MEMORY: GPU Partition C/D



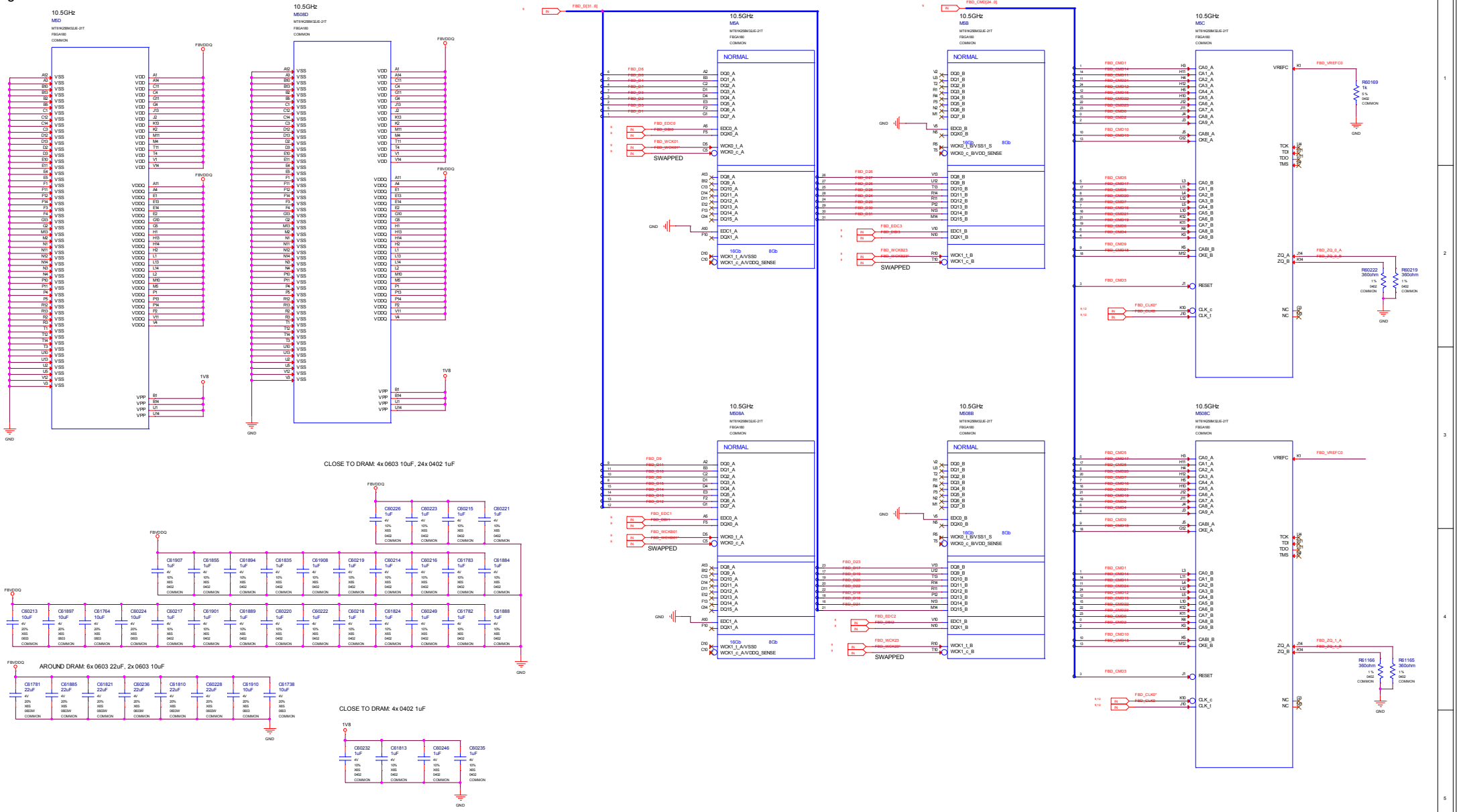
Page 10: MEMORY: FBC Partition 31..0



Page 11: MEMORY: FBC Partition 63..32



Page 12: MEMORY: FBD Partition 31..0



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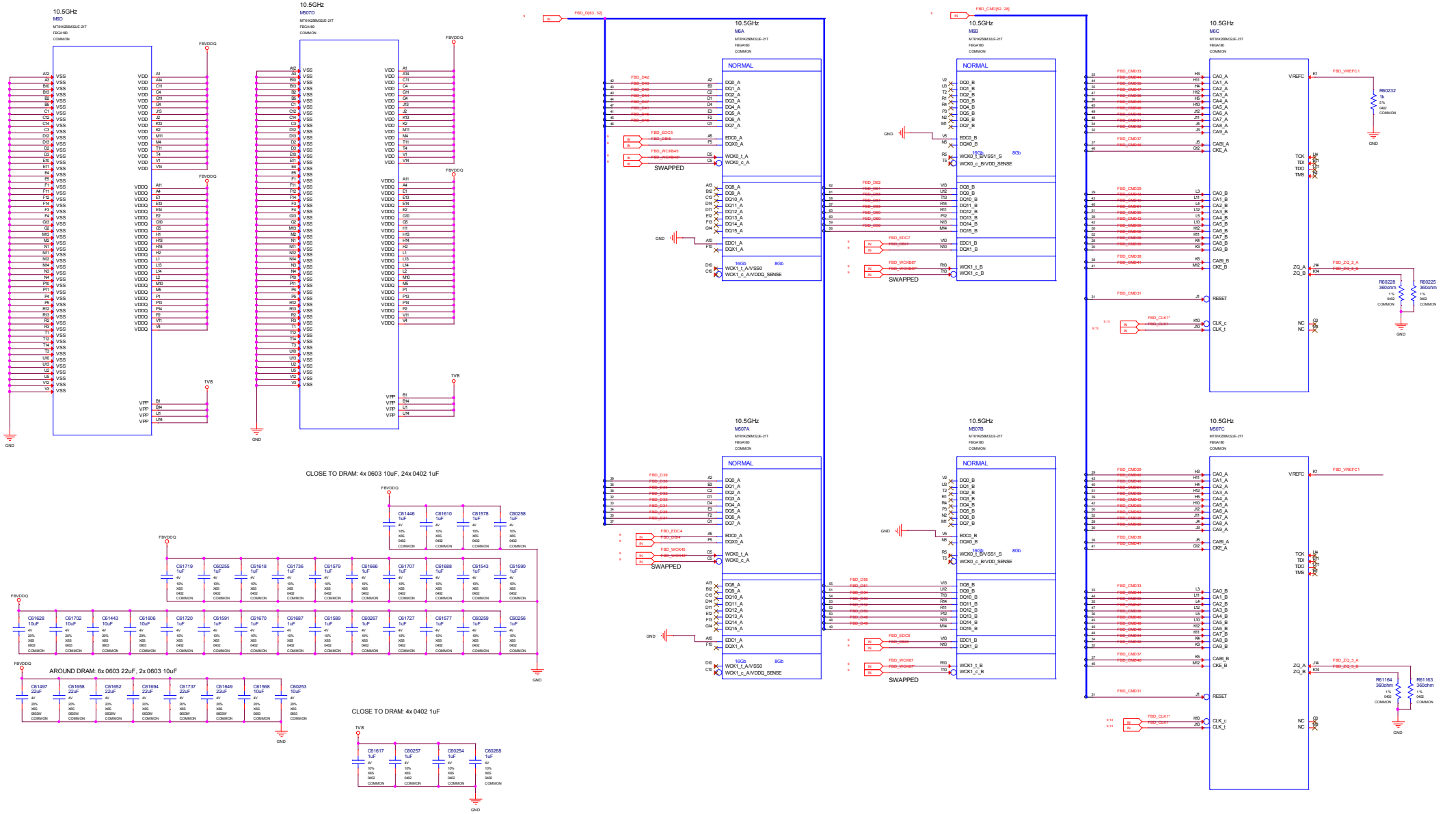
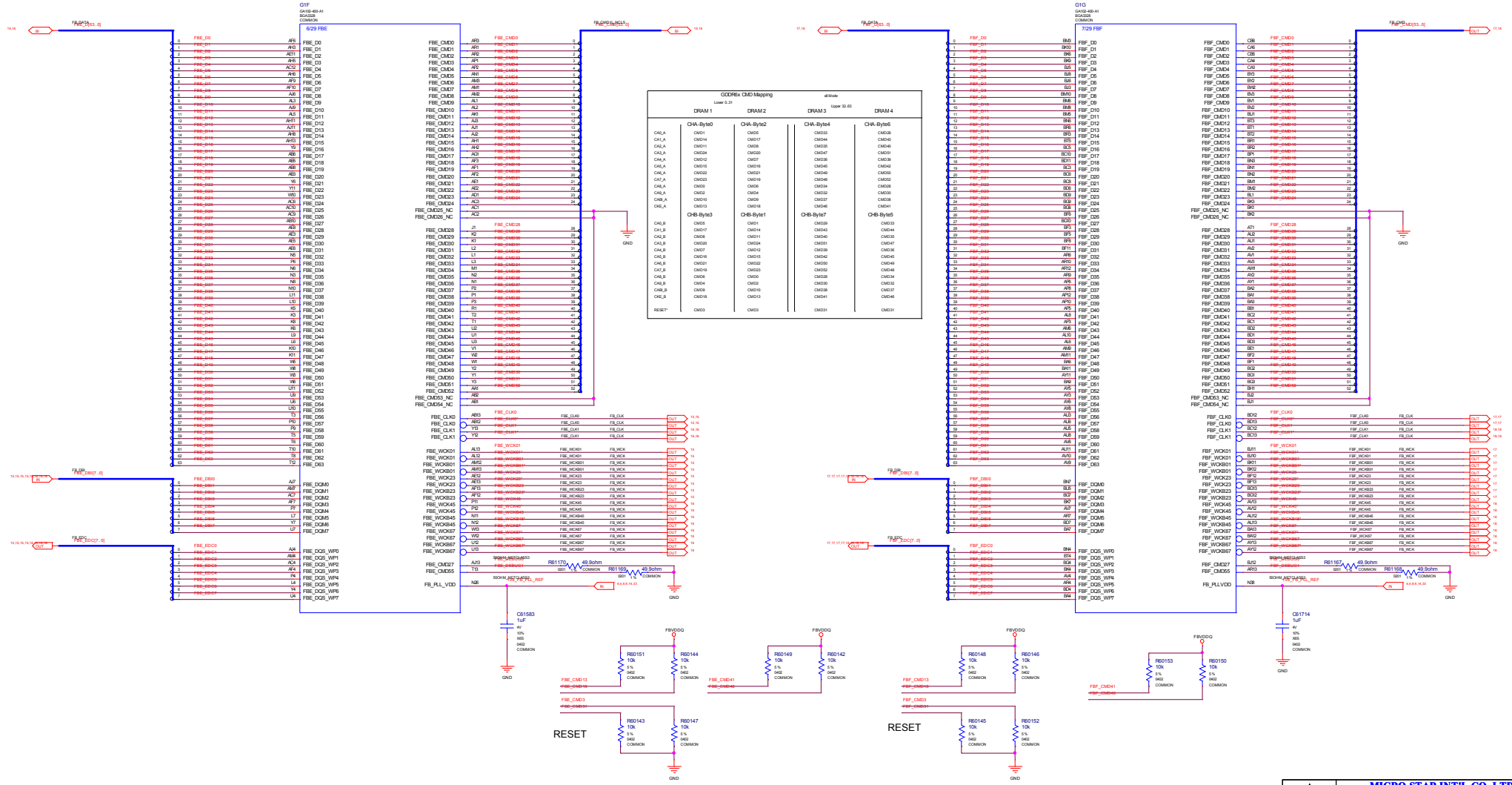
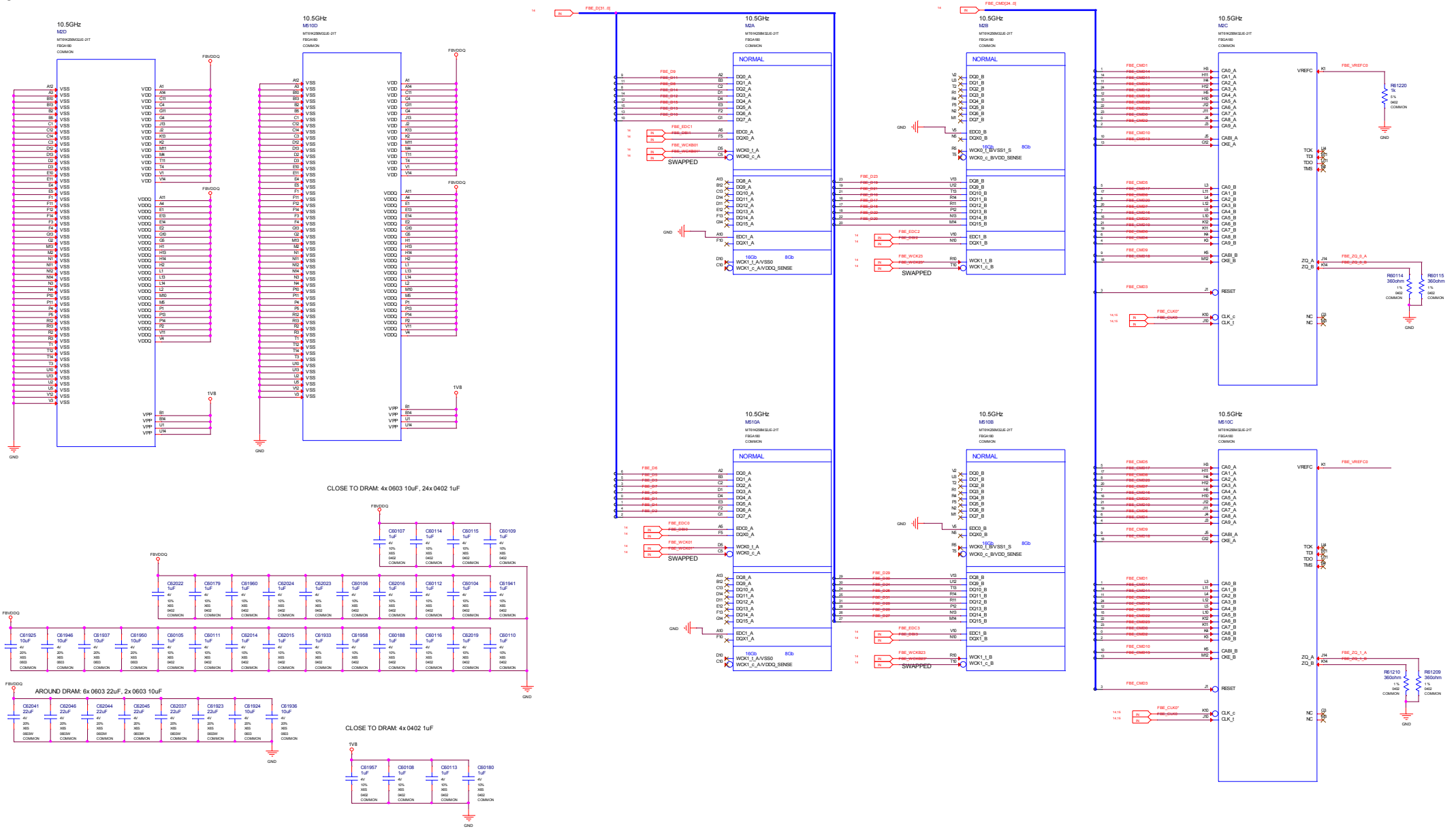


MEMORY: GPU Partition E/F




10.5Ghz
M2D
10.5Ghz
M510D
10.5Ghz
M2A
NORMAL
10.5Ghz
M2B
NORMAL
10.5Ghz
M2C
10.5Ghz
M510A
NORMAL
10.5Ghz
M510B
NORMAL
10.5Ghz
M510C
SWAPPED
SWAPPED
SWAPPED
CLOSE TO DRAM: 4x 0603 10uF, 24x 0402 1uF
AROUND DRAM: 6x 0603 22uF, 2x 0603 10uF
CLOSE TO DRAM: 4x 0402 1uF
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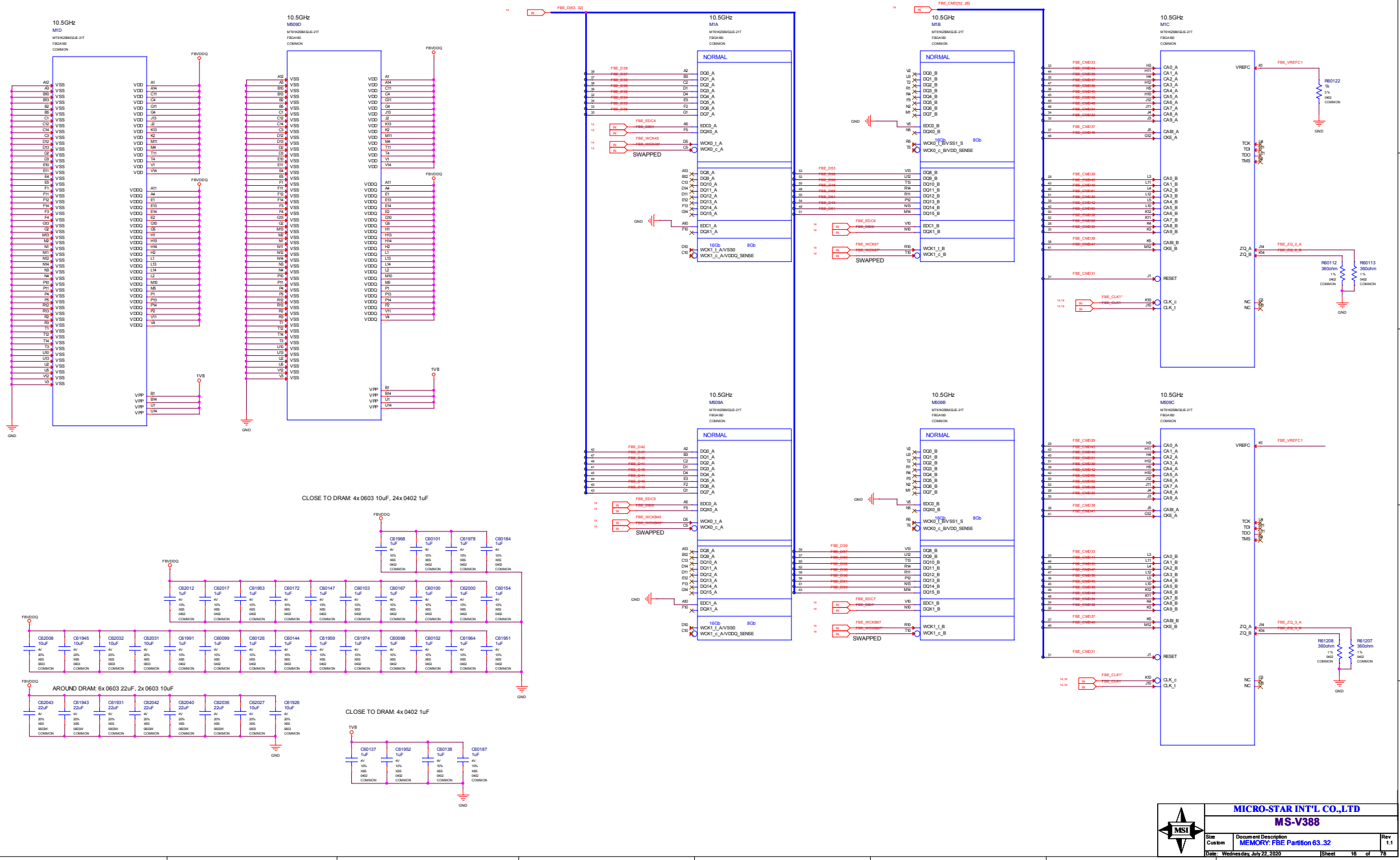

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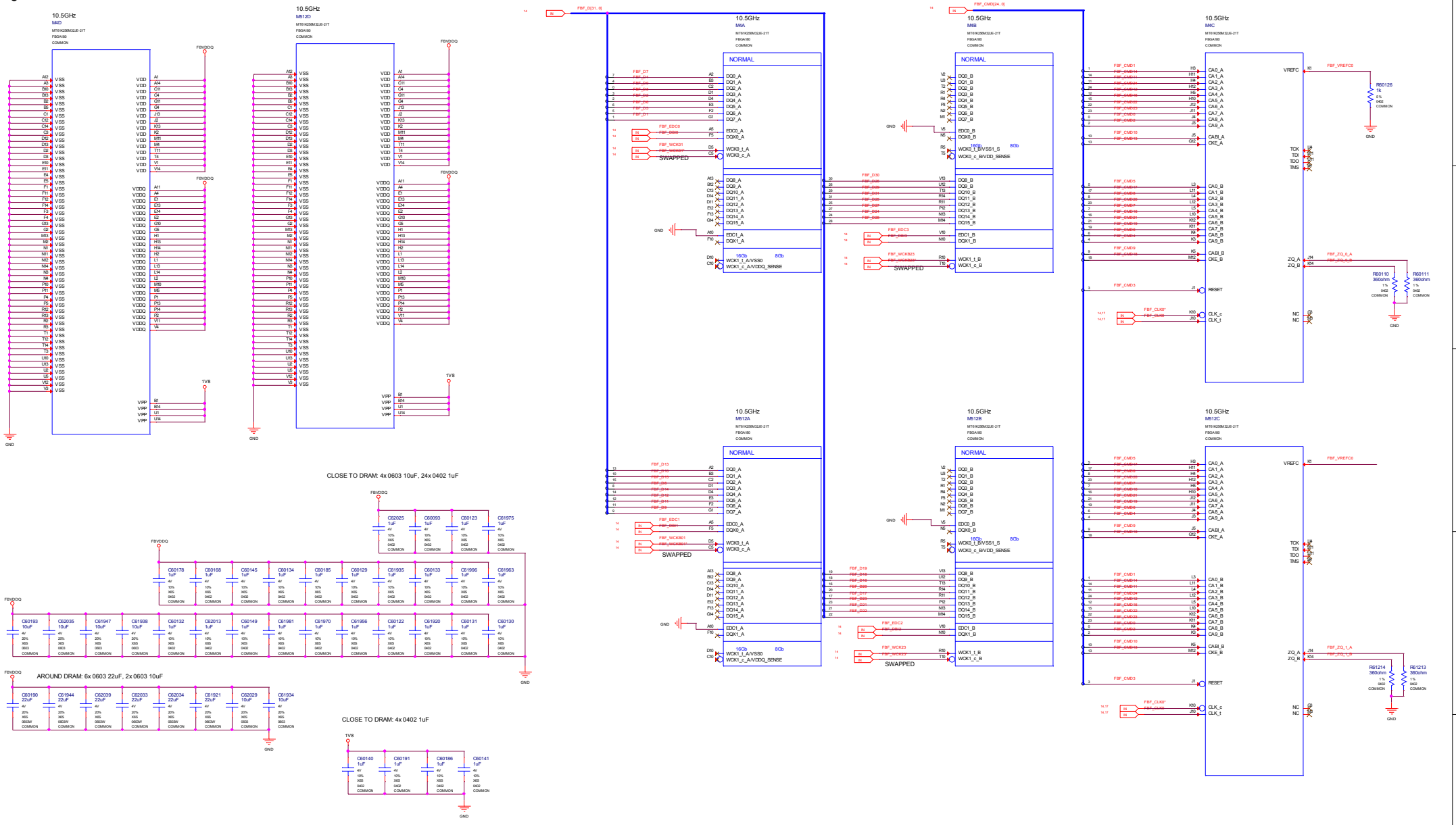

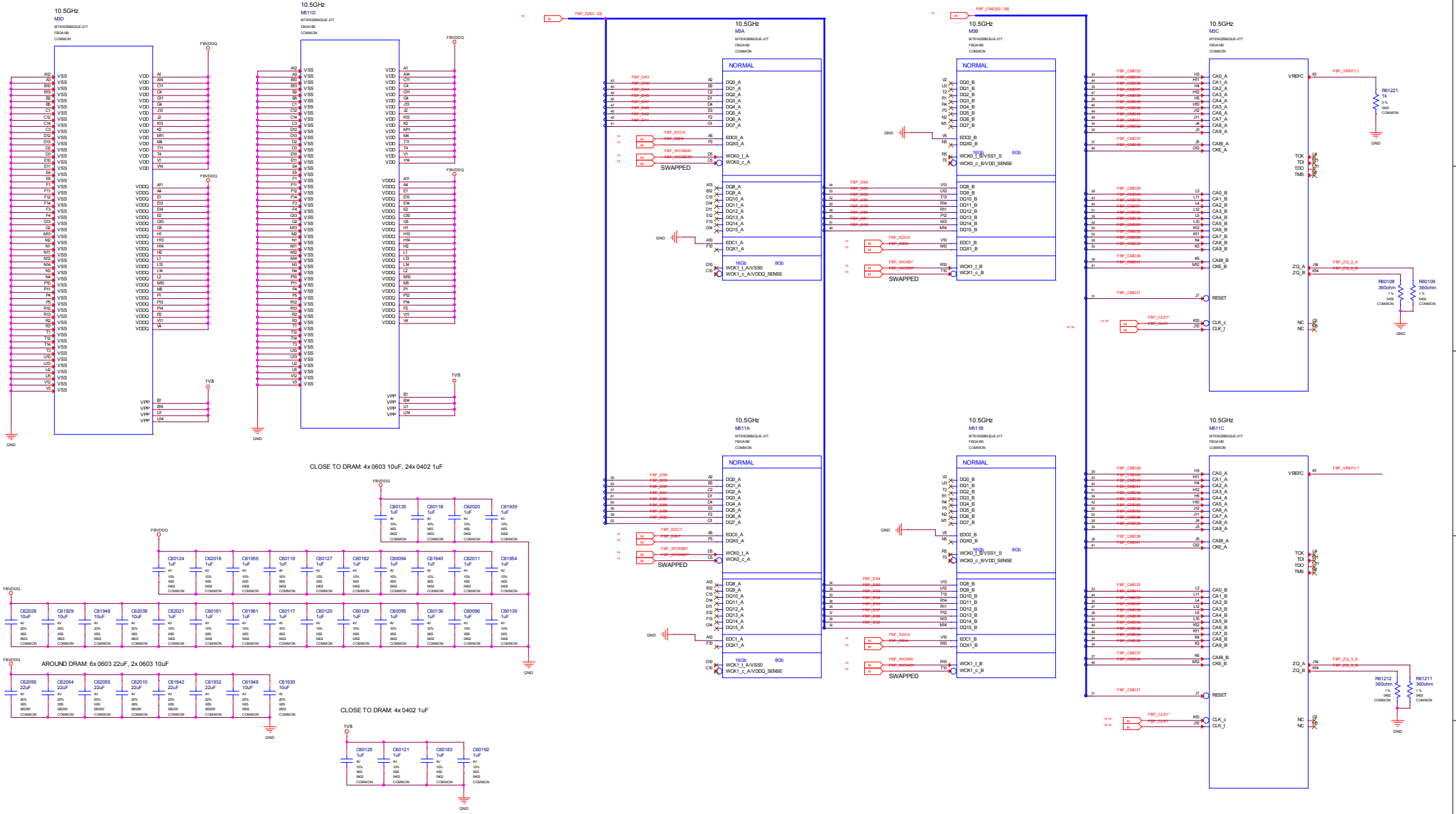

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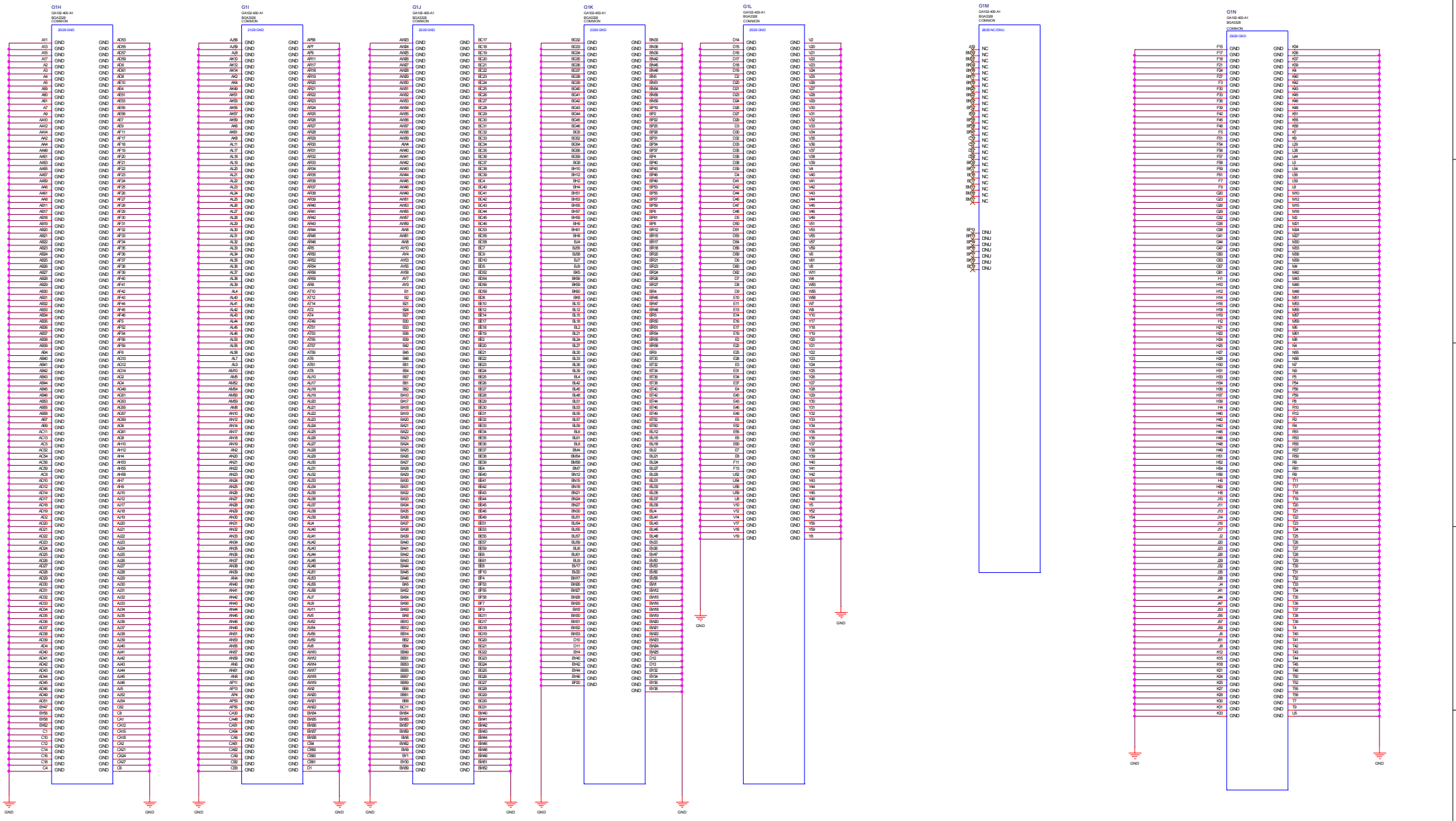
GPU GND, RFUs & RSVD



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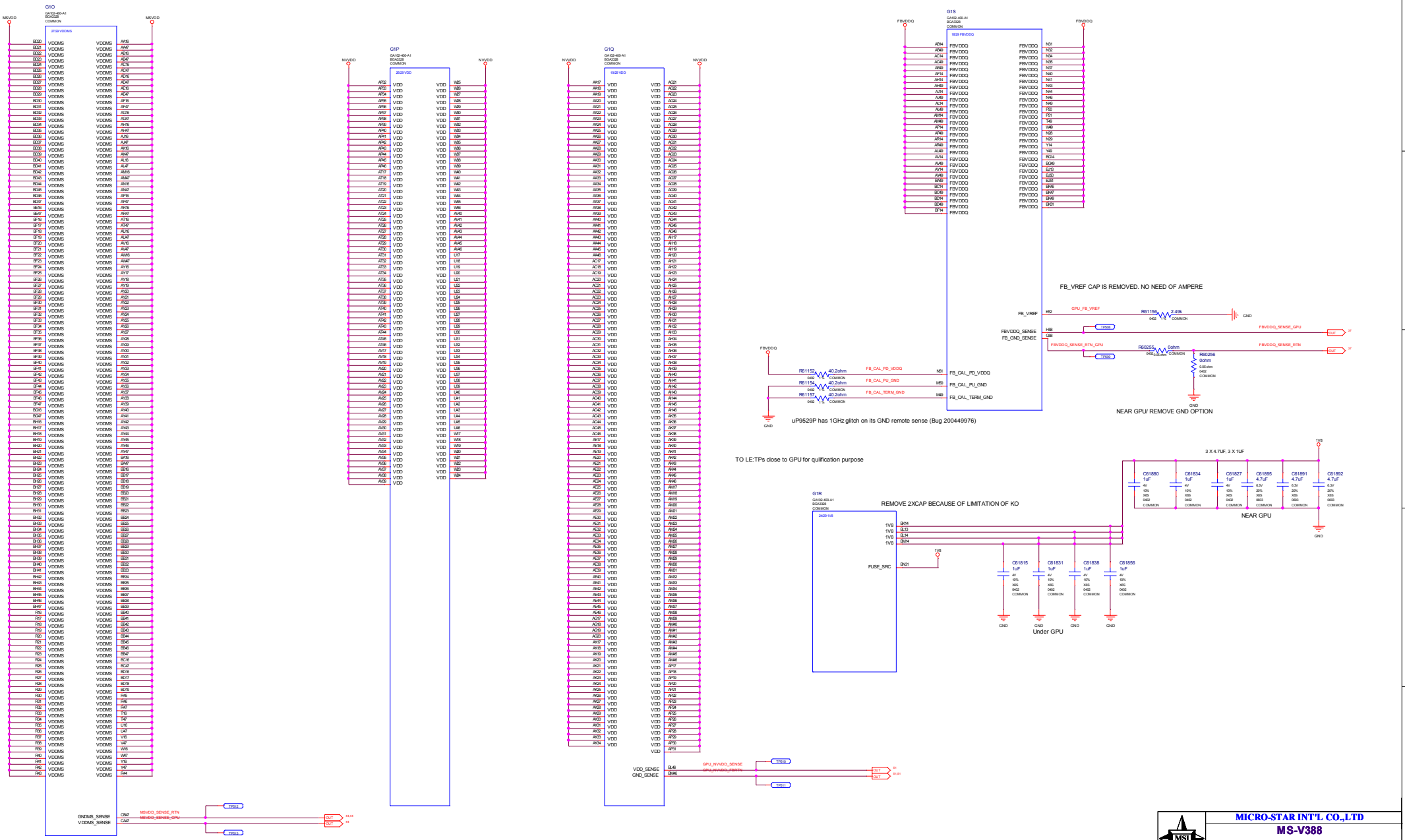
GPU PWR and GND



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NVVDD

UNDER GPU

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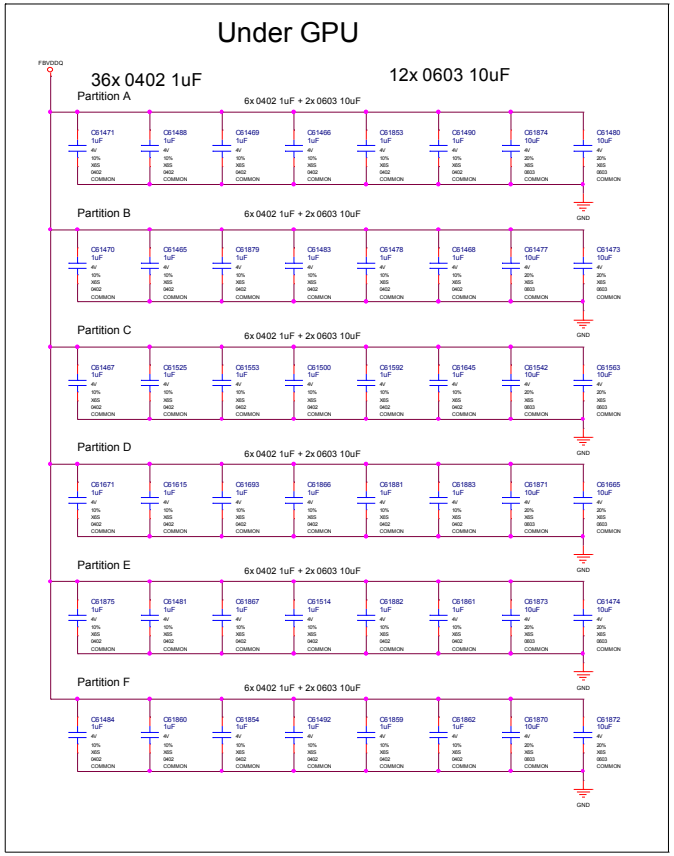
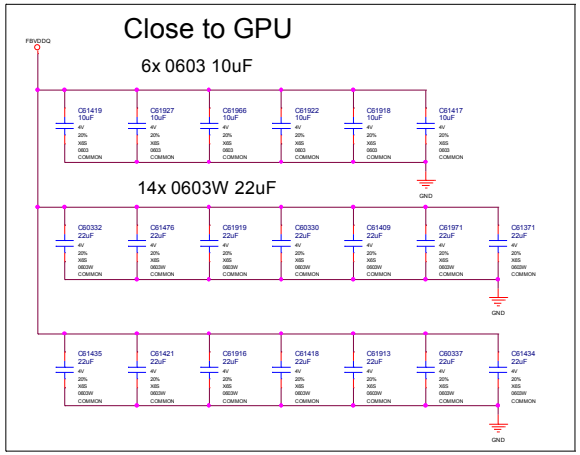
FBVDDQ





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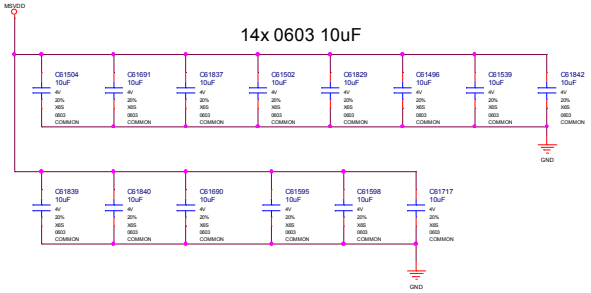
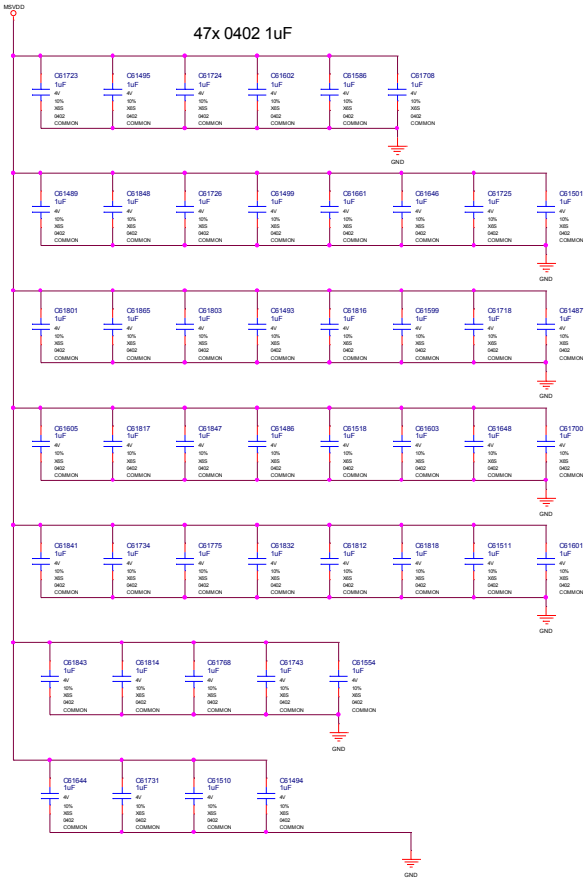
UNDER GPU

MSVDD

14x 0603 10uF

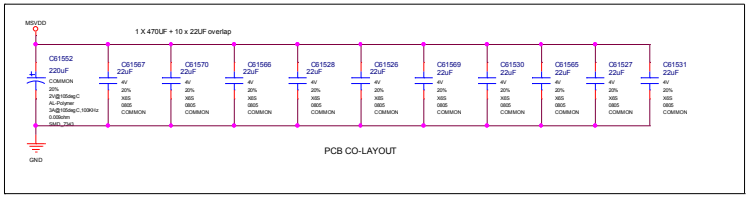


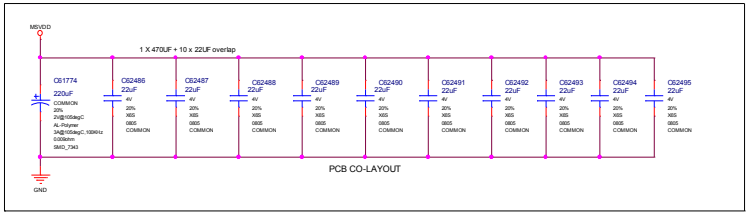
47x 0402 1uF



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)





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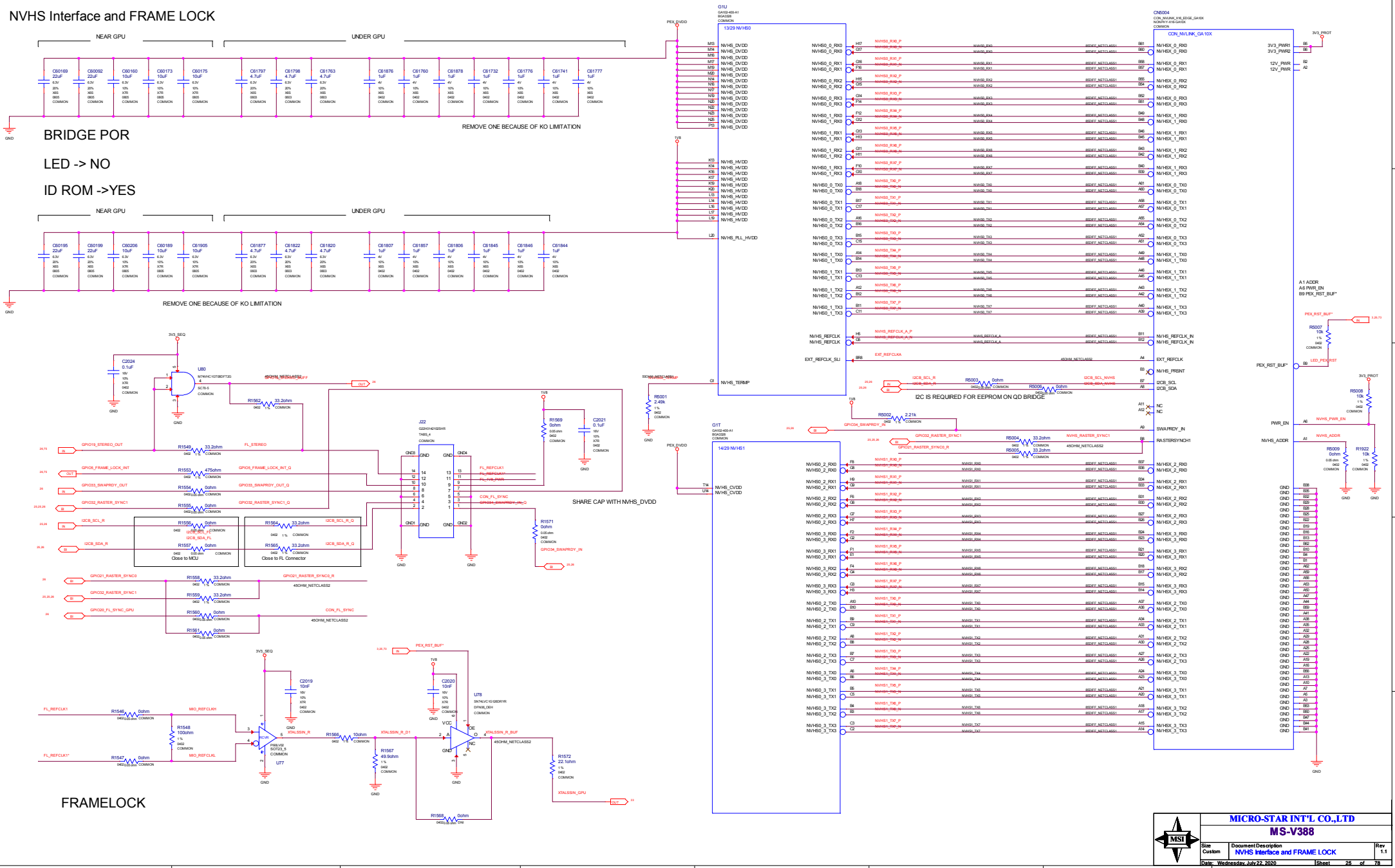
NVHS Interface and FRAME LOCK



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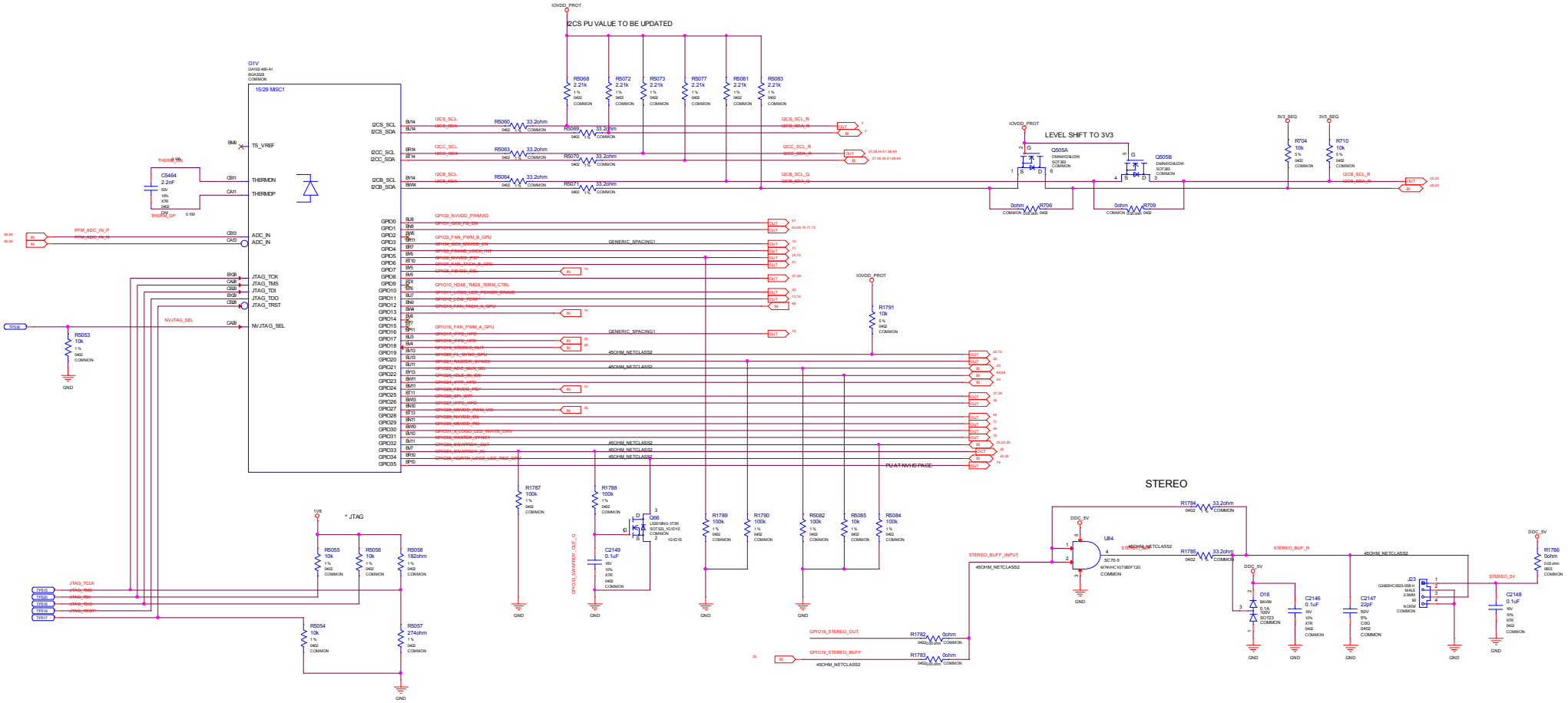
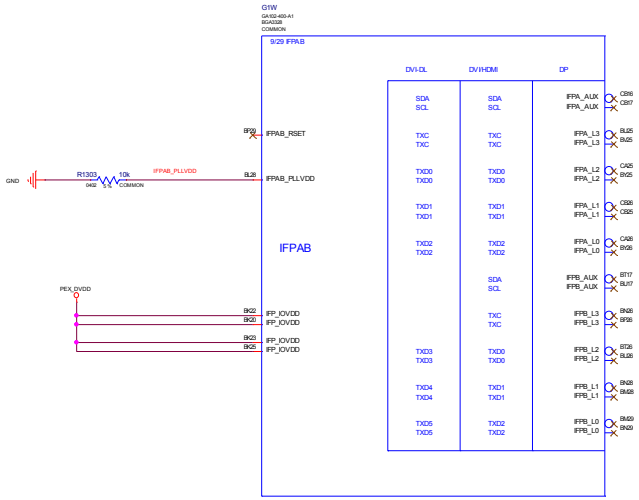
MISC1: Fan, Thermal, JTAG, GPIO, STEREO



IFPA UNUSED, IFPB UNUSED



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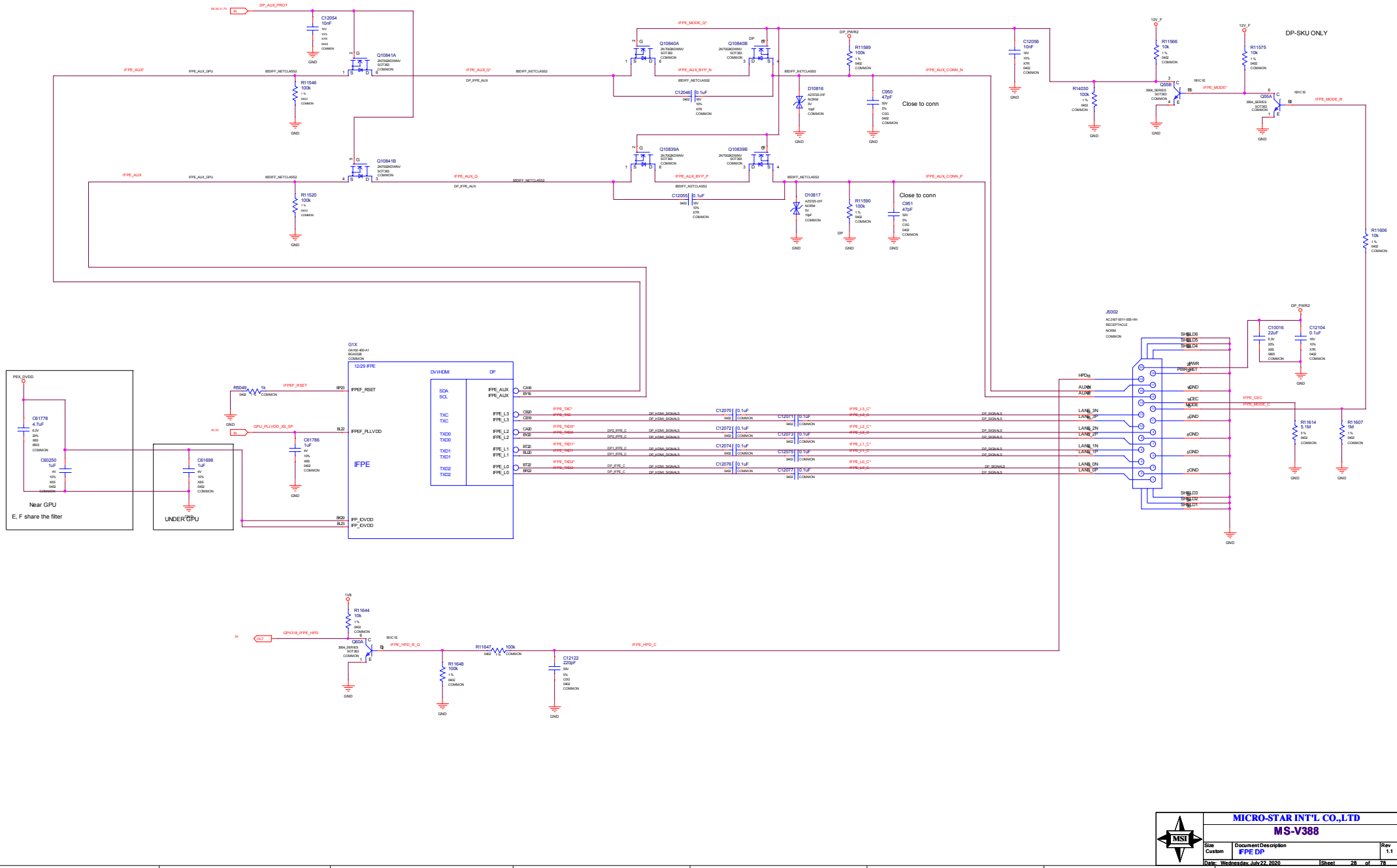
IFPE DP



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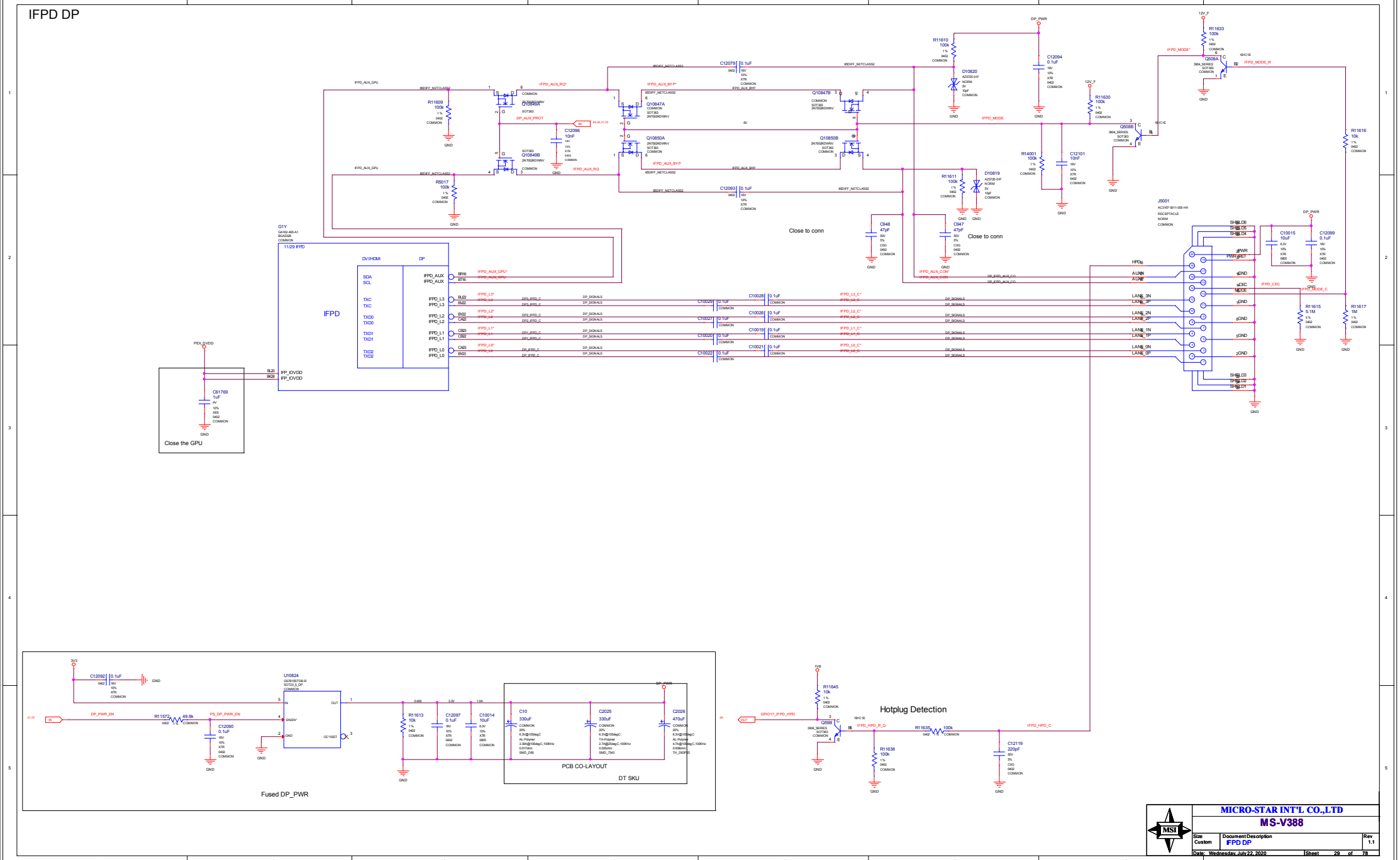
IFPD DP



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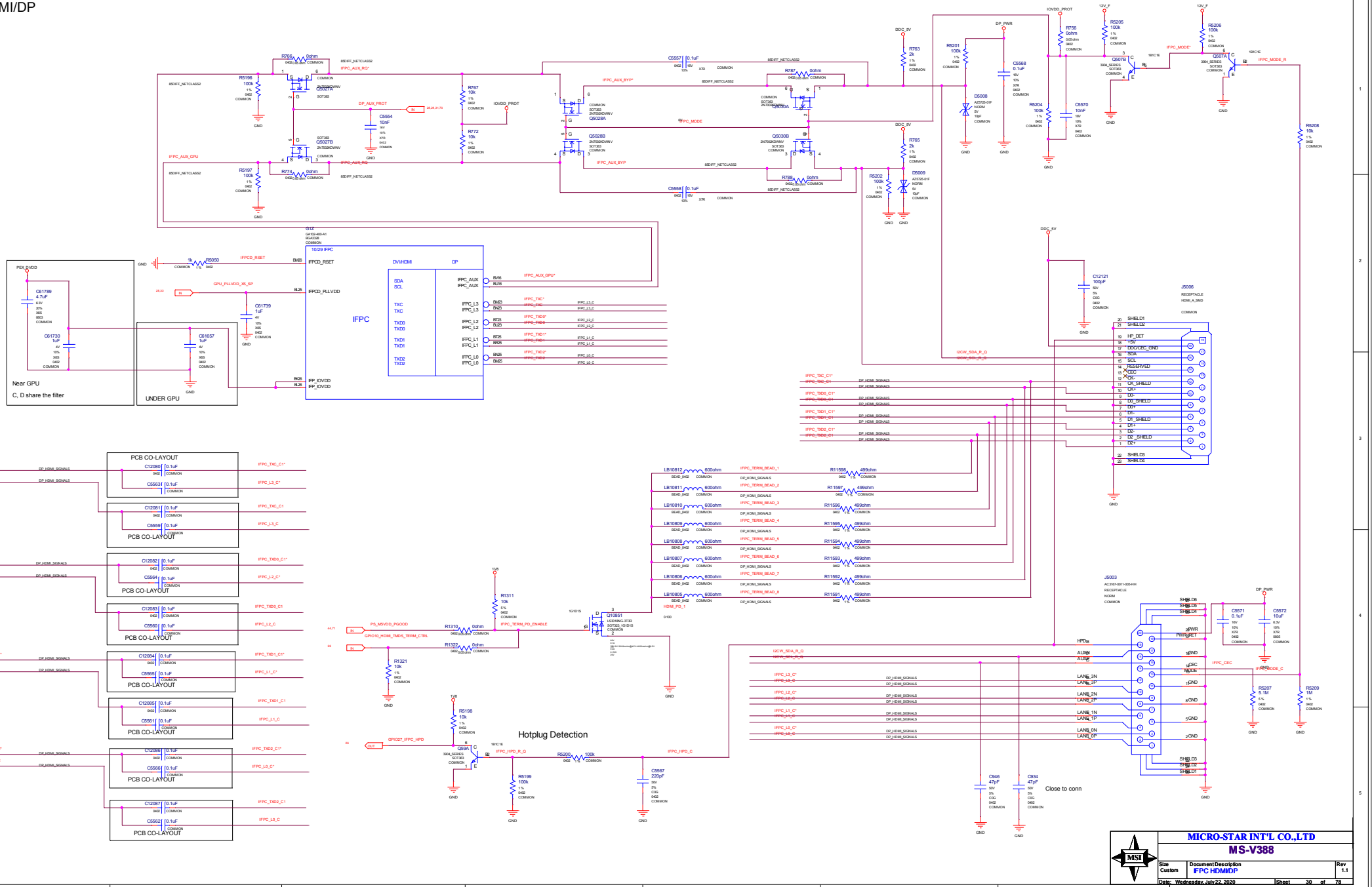
IFPC HDMI/DP


IFPC
DP/HDMI
DP
Near GPU
C, D share the filter
UNDER GPU
PCB CO-LAYOUT
Hotplug Detection
Close to conn
J5006
J5003
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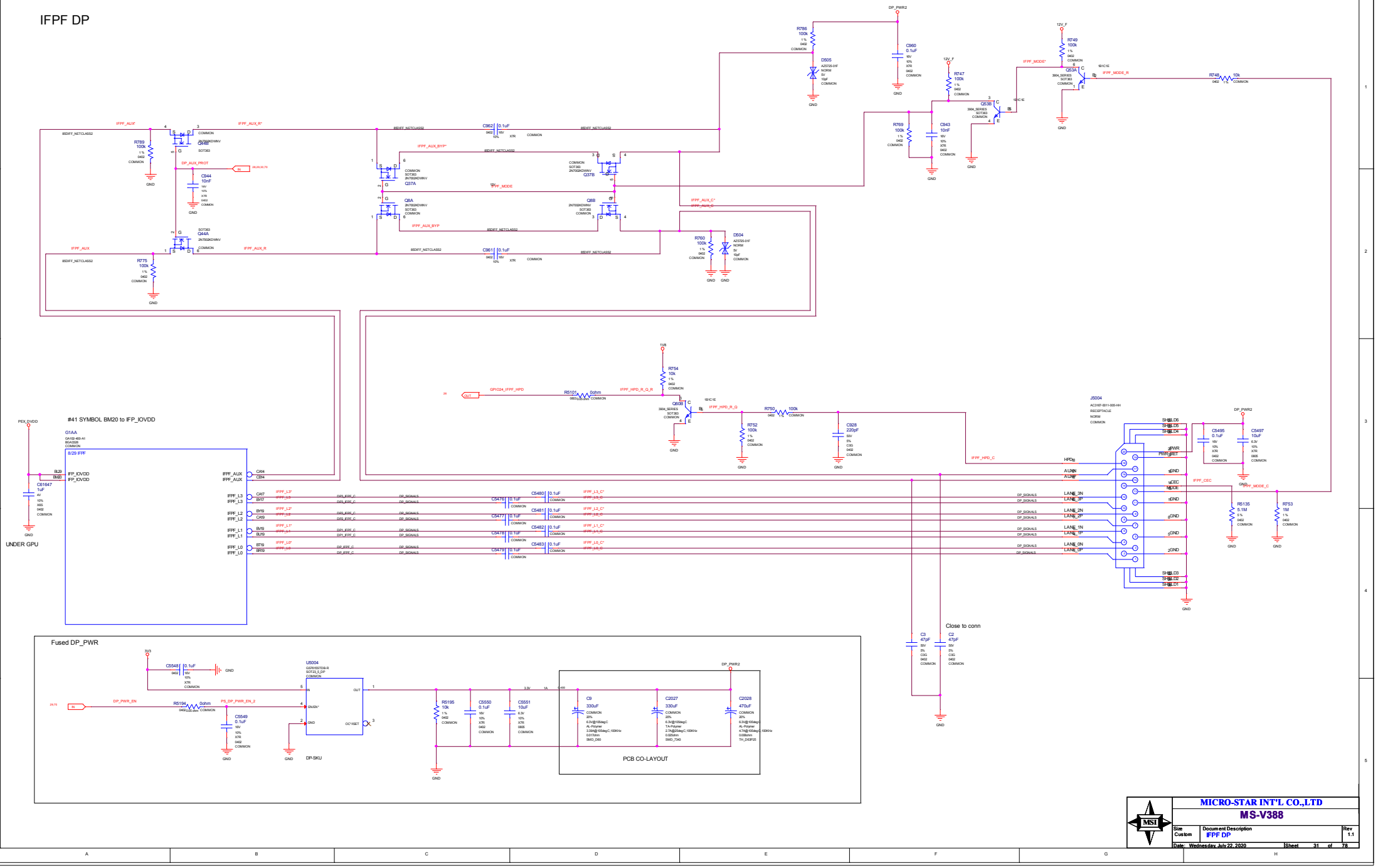
IFPF DP



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MISC: ROM, Straps

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 8Gb 19Gbps
L	H	L	00010	RAMCFG TBD
H	L	L	00100	RAMCFG TBD
H	L	H	00101	RAMCFG TBD
H	L	H	00101	RAMCFG MICRON 8Gb 21Gbps

DEFAULT

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE
H	H	H	0111	FS_OVERT ENABLE
L	L	L	0000	FS_OVERT DISABLE

DEFAULT

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	H 1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0

Default

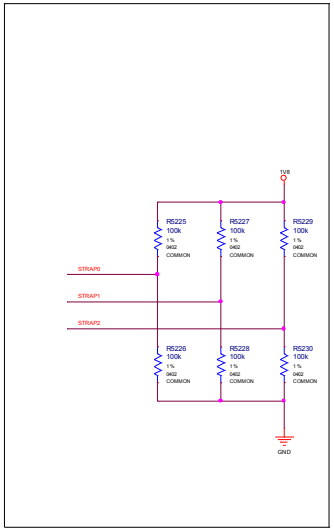
1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

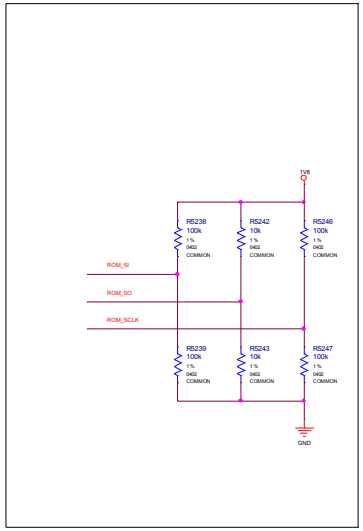
1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

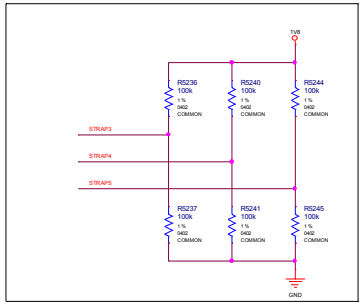
1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

GROUP0

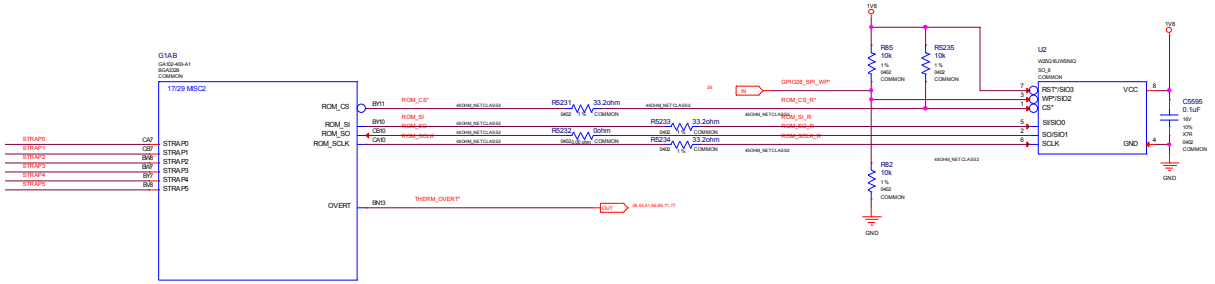


GROUP1





GROUP2



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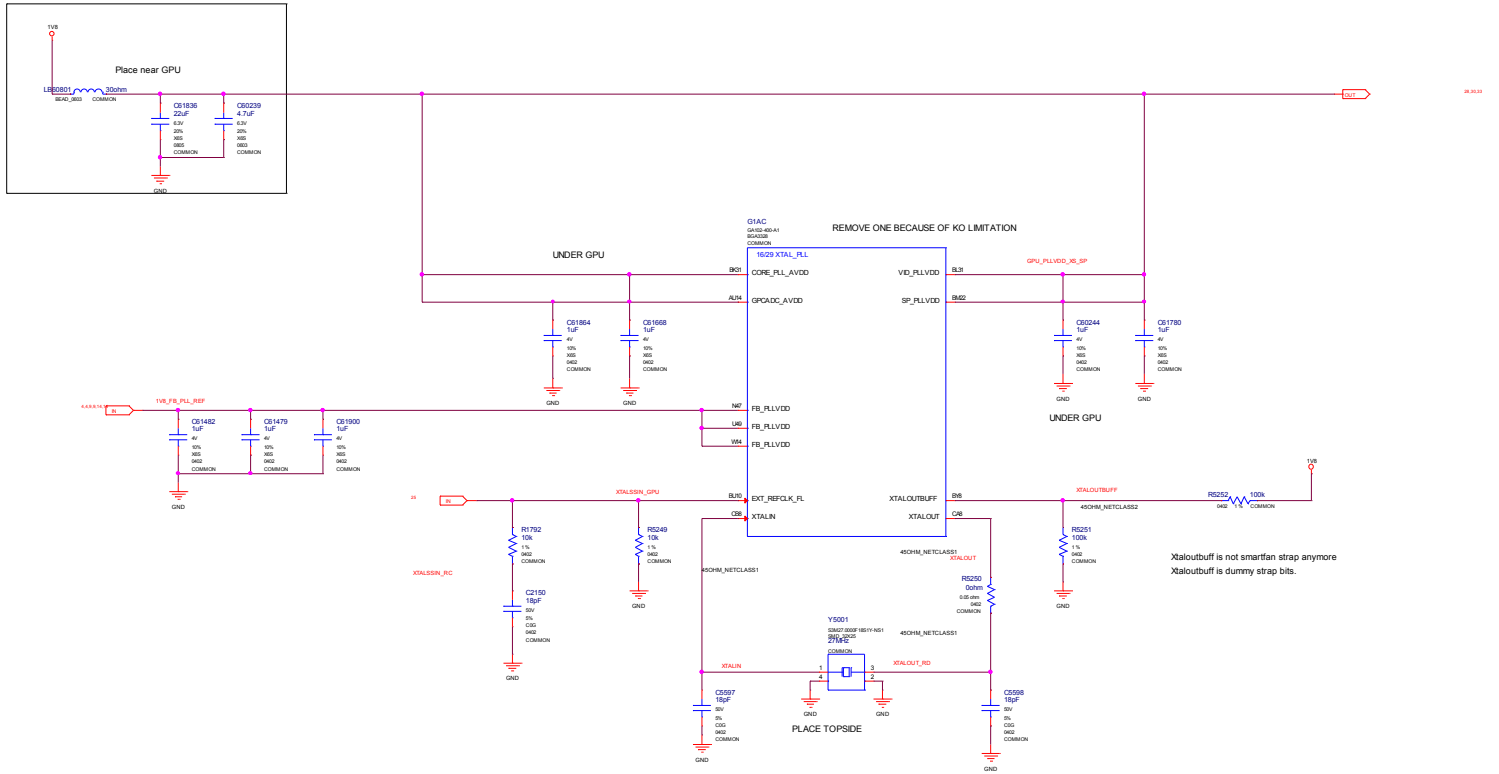
MISC: XTAL. PLL



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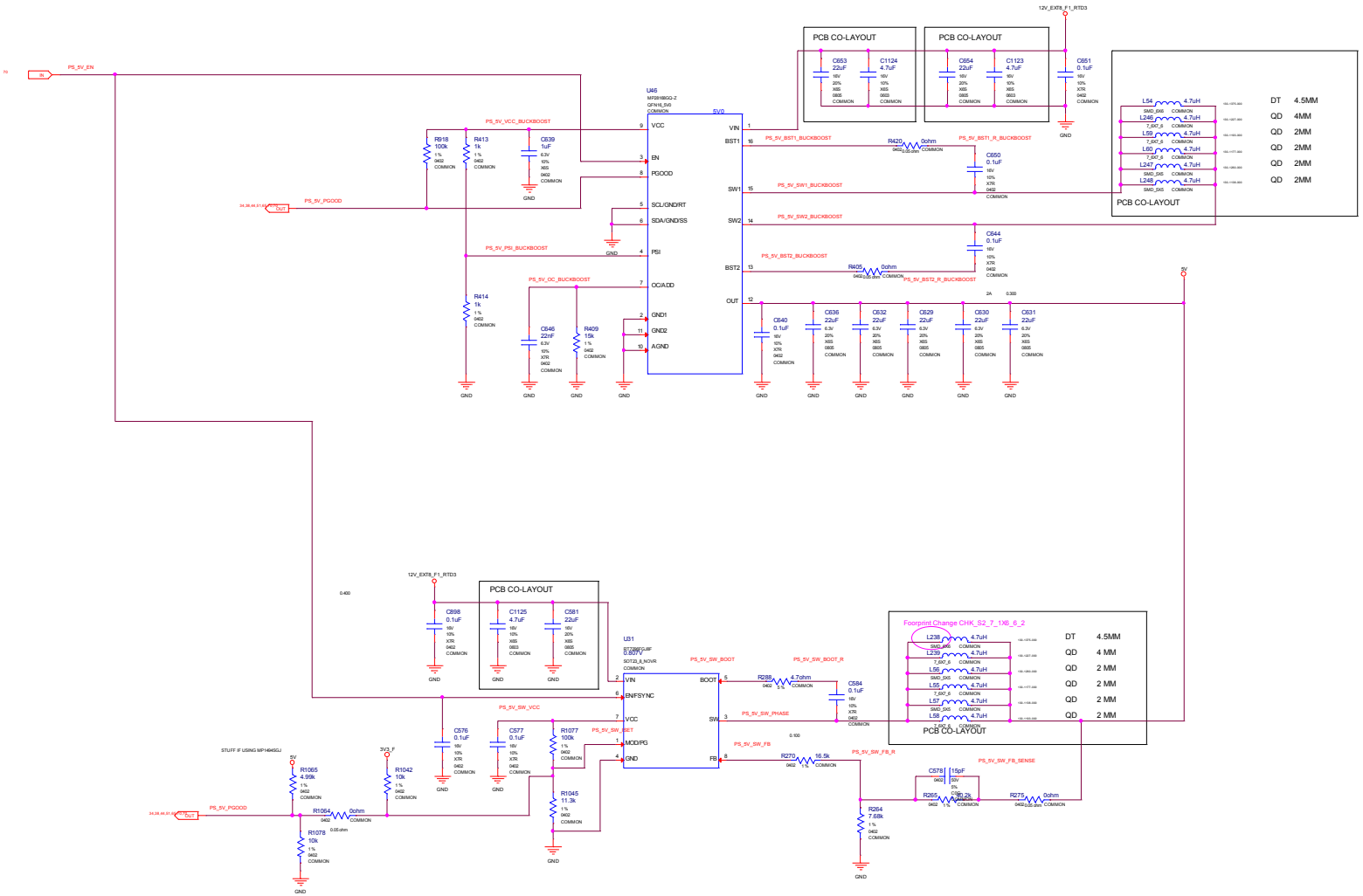
PS: 5V, 5V_BACKUP



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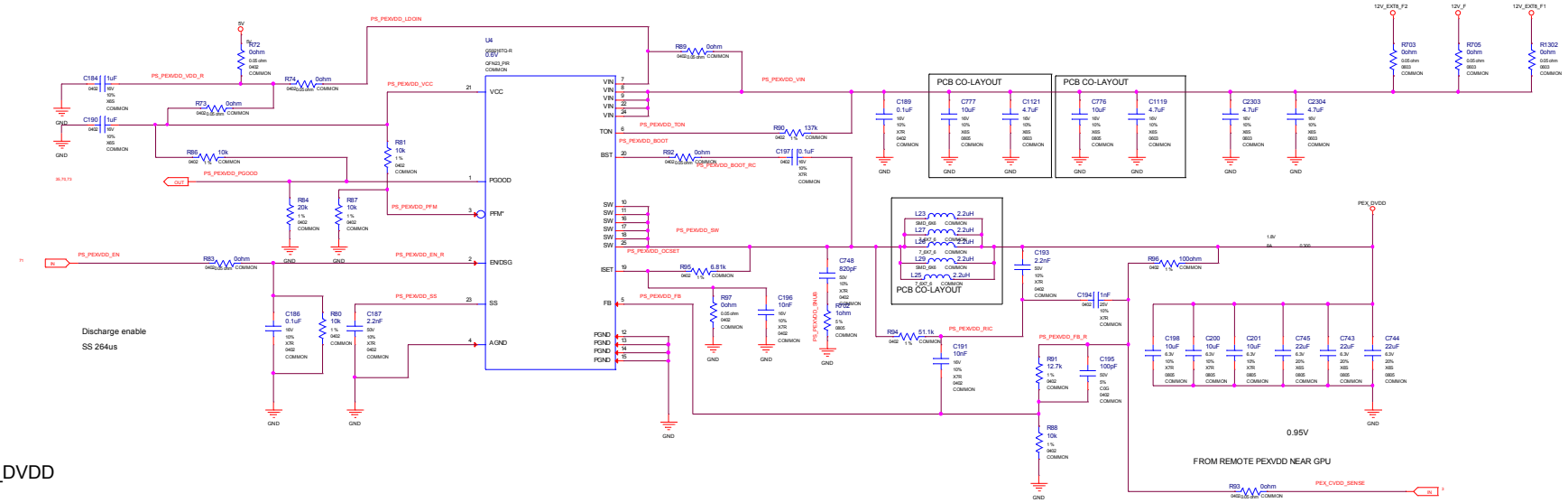
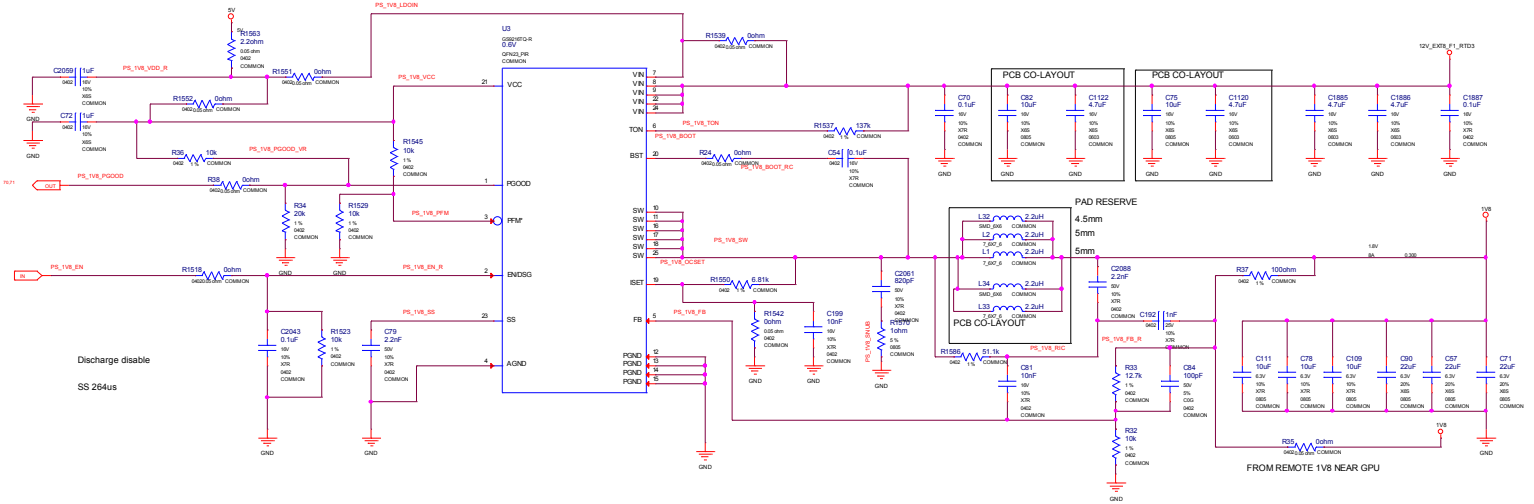
PS: PEX_DVDD 1V8 Rail



PEX_DVDD



1V8

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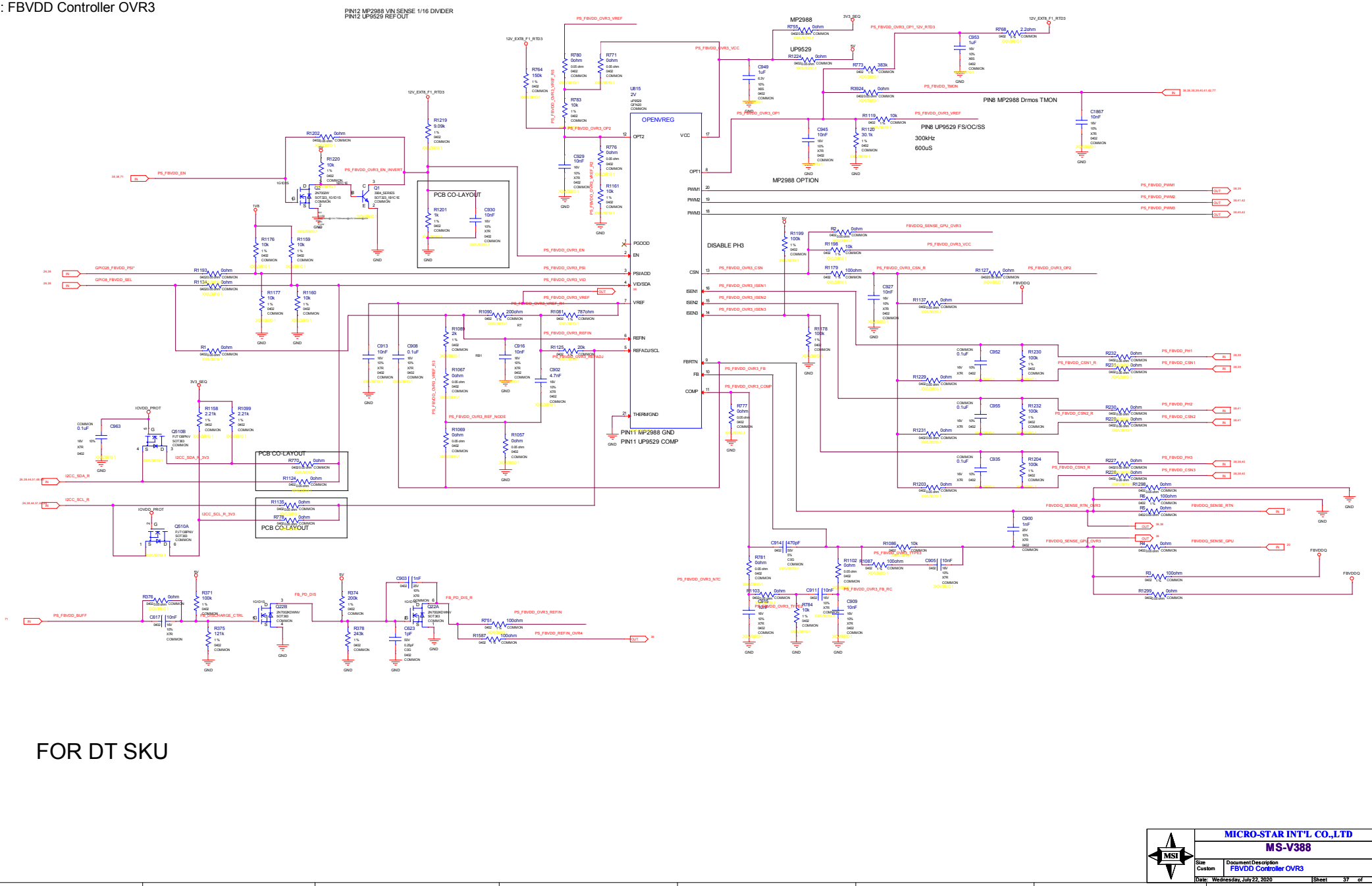
PS: FBVDD Controller OVR3



FOR DT SKU

MICRO-STAR INT'L CO.,LTD		
MS-V388		
Size: Custom	Document Description: FBVDD Controller OVR3	Rev: 1.1
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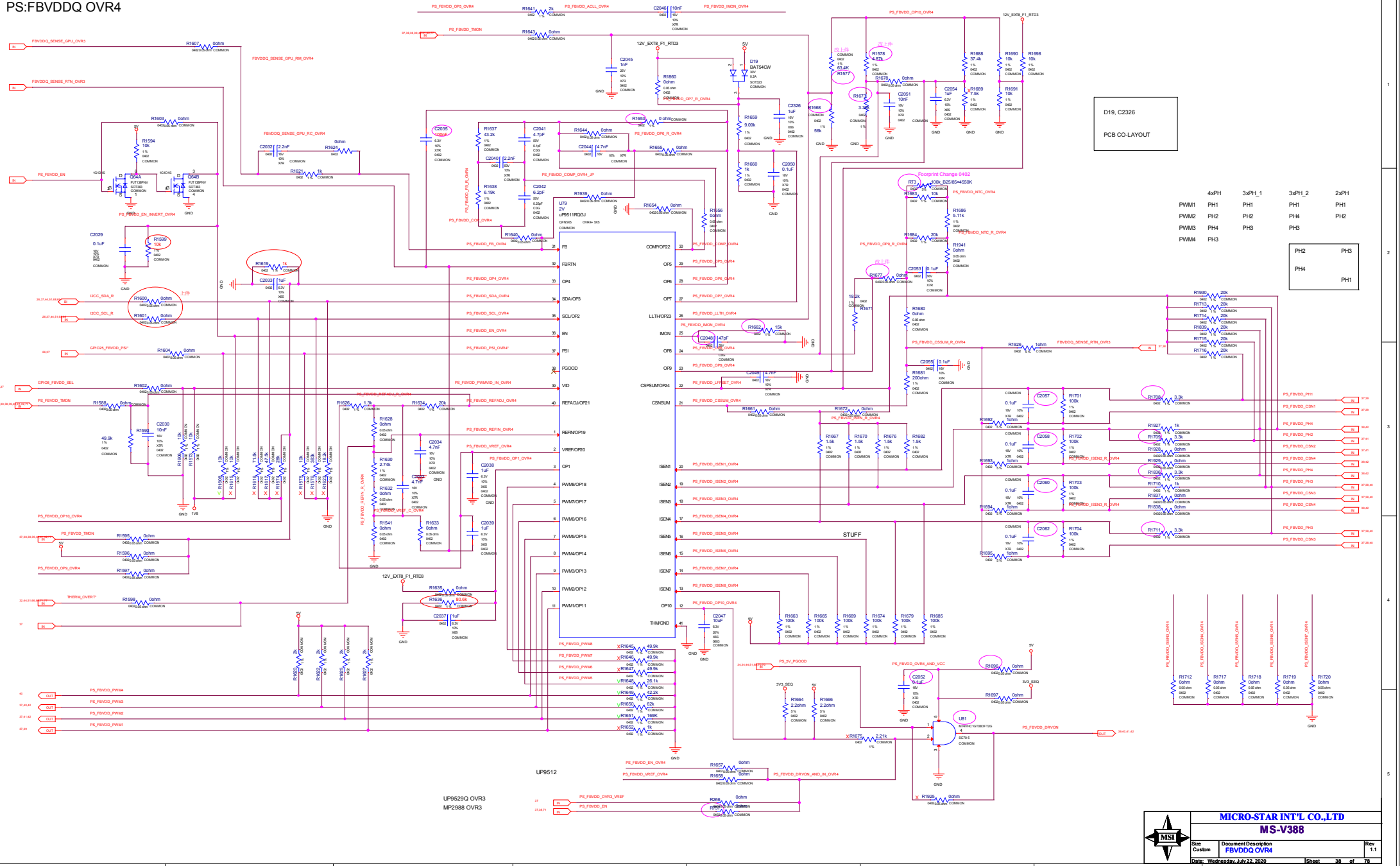
PS:FBVDDQ OVR4



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MS-V388	
Size: Custom	Document Description: FBVDDQ OVR4
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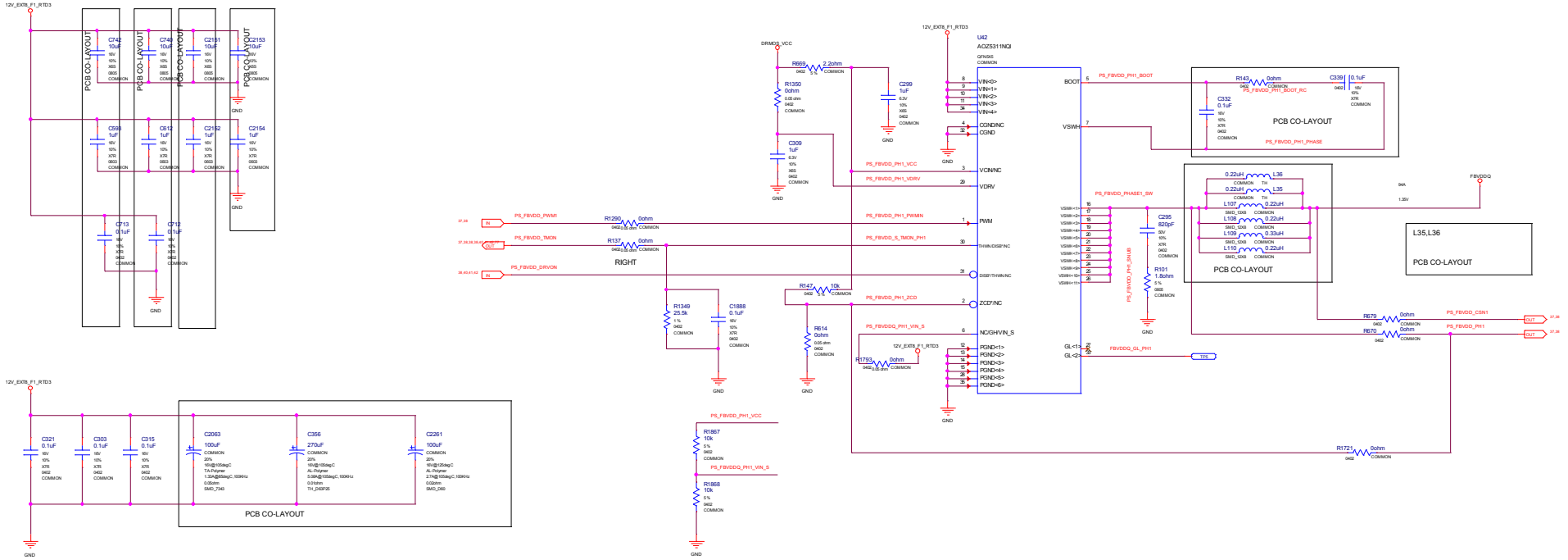
PS: FBVDD PH1



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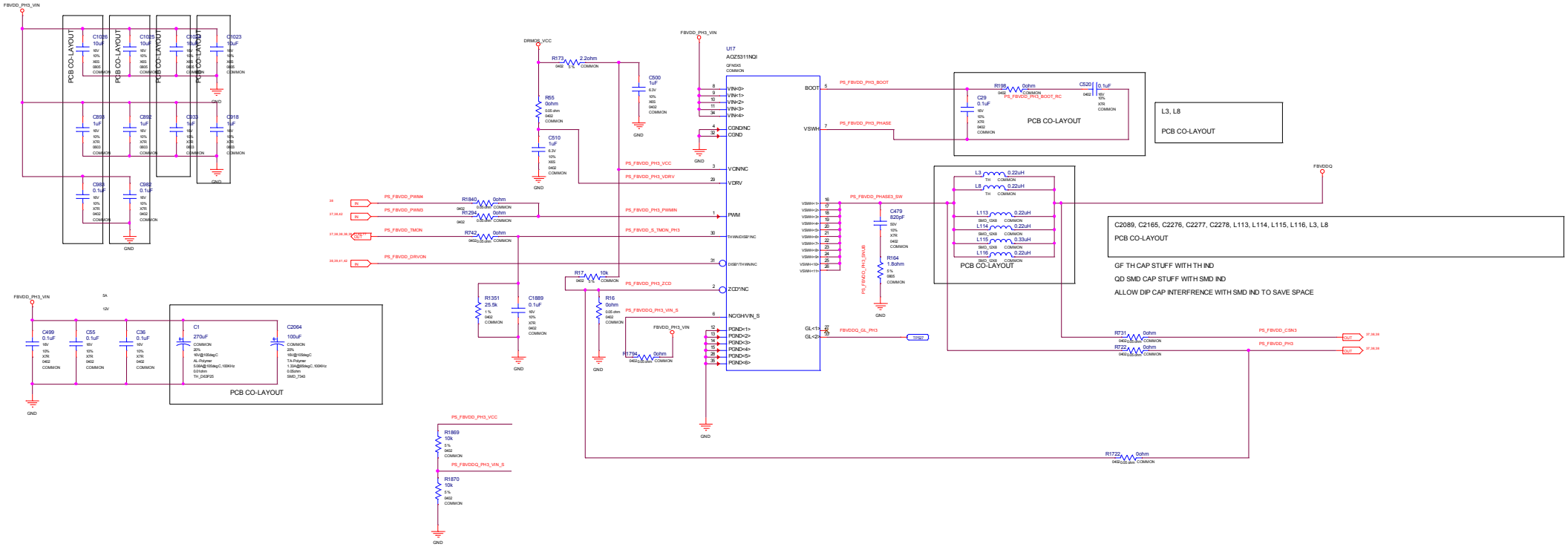
PS: FBVDD PH3



FBVDD PH3 INPUT ANTI-BACKDRIVE

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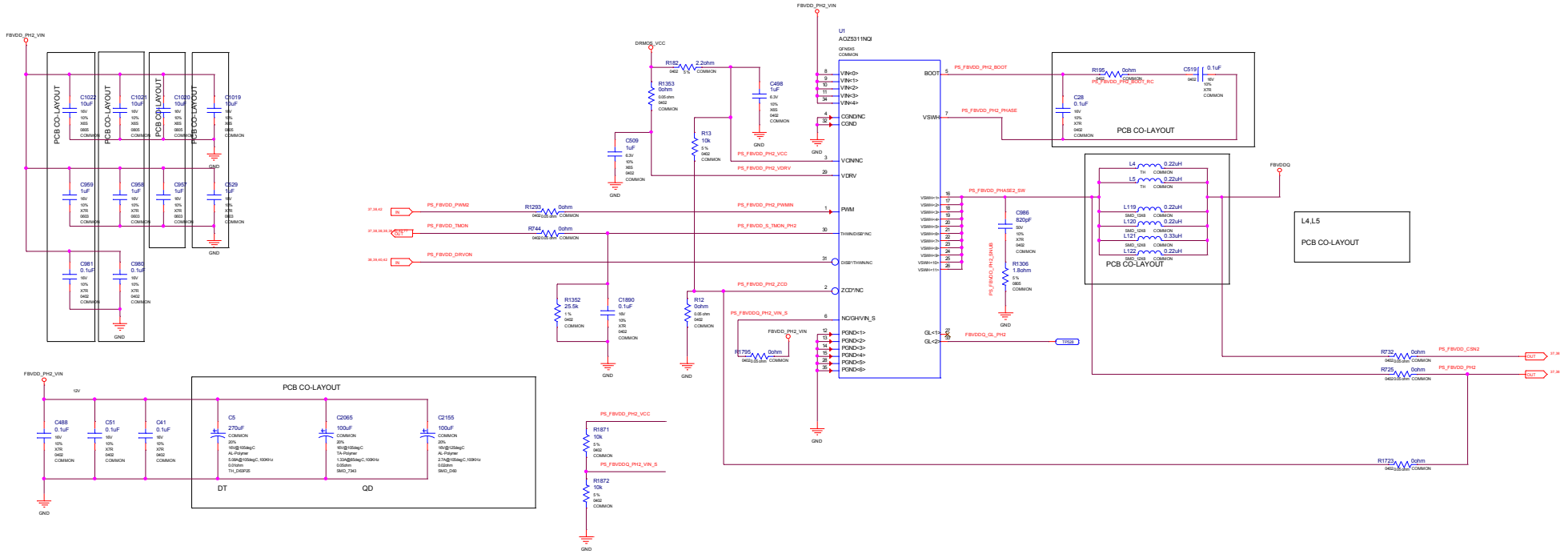
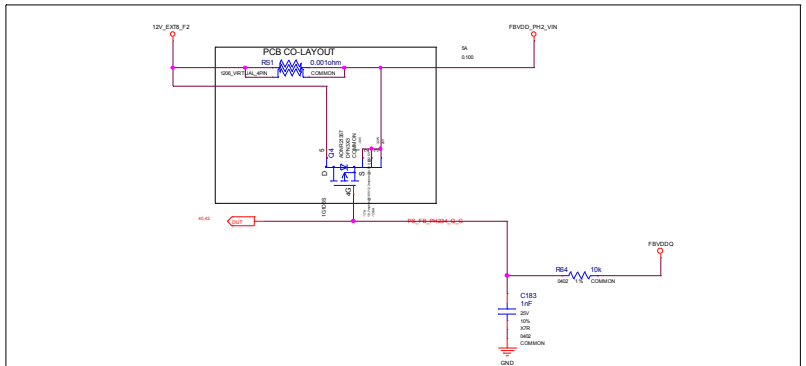
PS: FBVDD PH2





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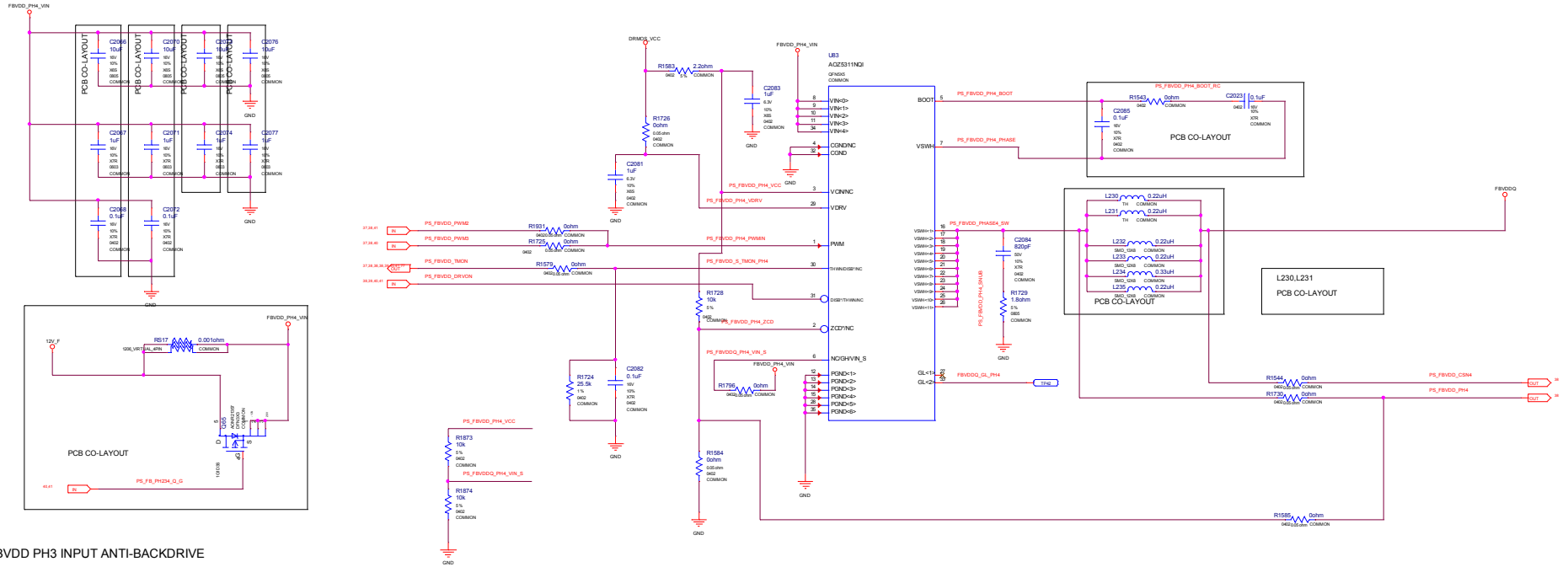
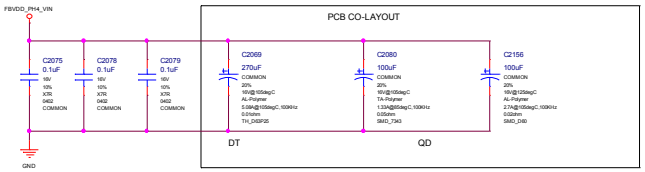
PS: FBVDD PH4



FBVDD PH3 INPUT ANTI-BACKDRIVE



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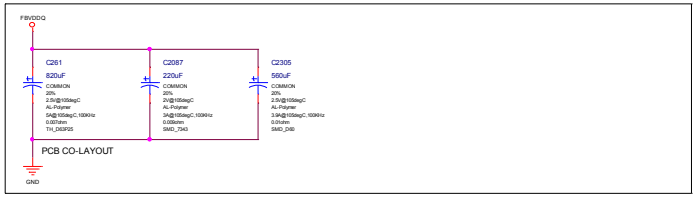
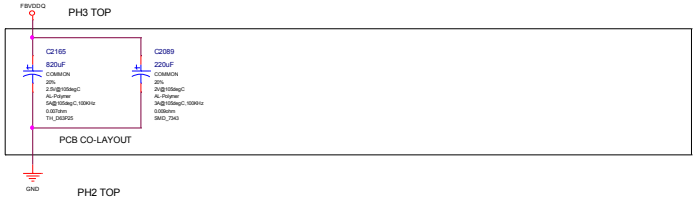
PS: FBVDD OUTPUT CAP

REFER TO PCB FOR BOM STUFFING

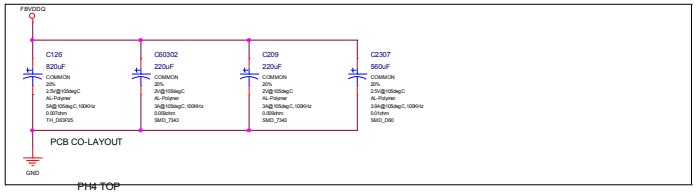
PH1 TOP



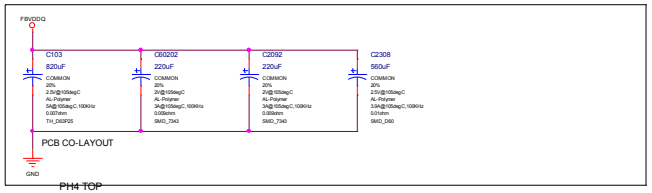
PH3 TOP

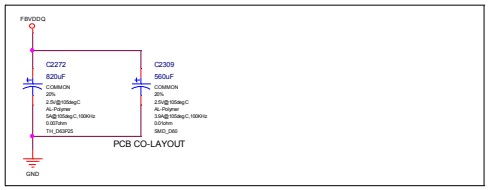


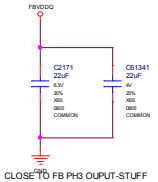
PH2 TOP



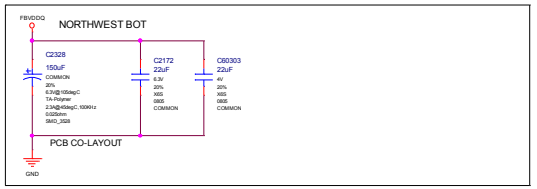
PH4 TOP

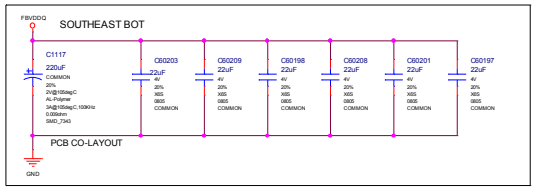


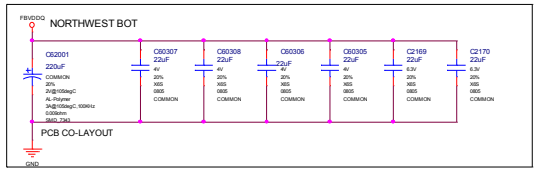


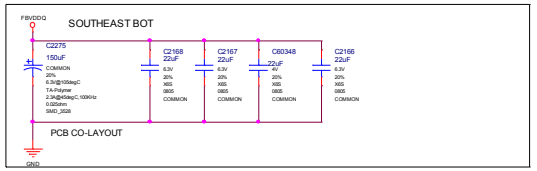


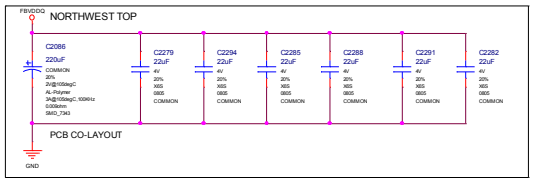
CLOSE TO FB PH3 OUPUT-STUFF

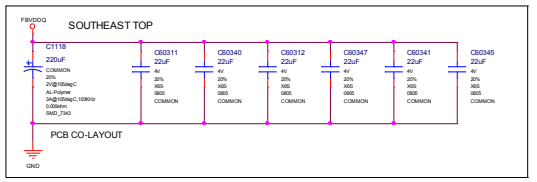


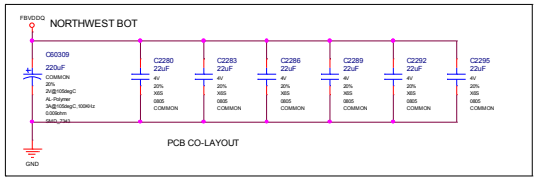


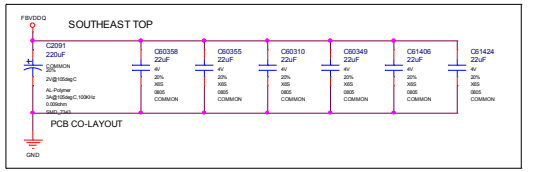


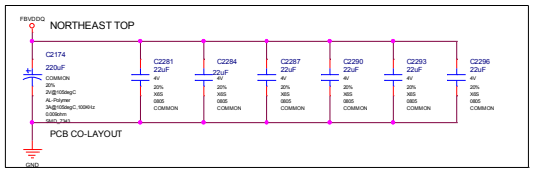


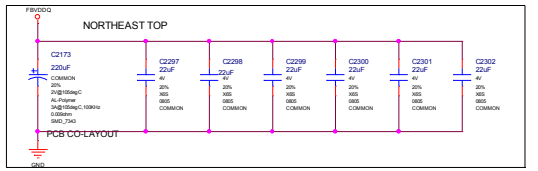


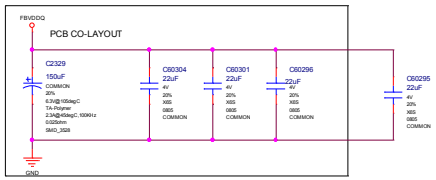












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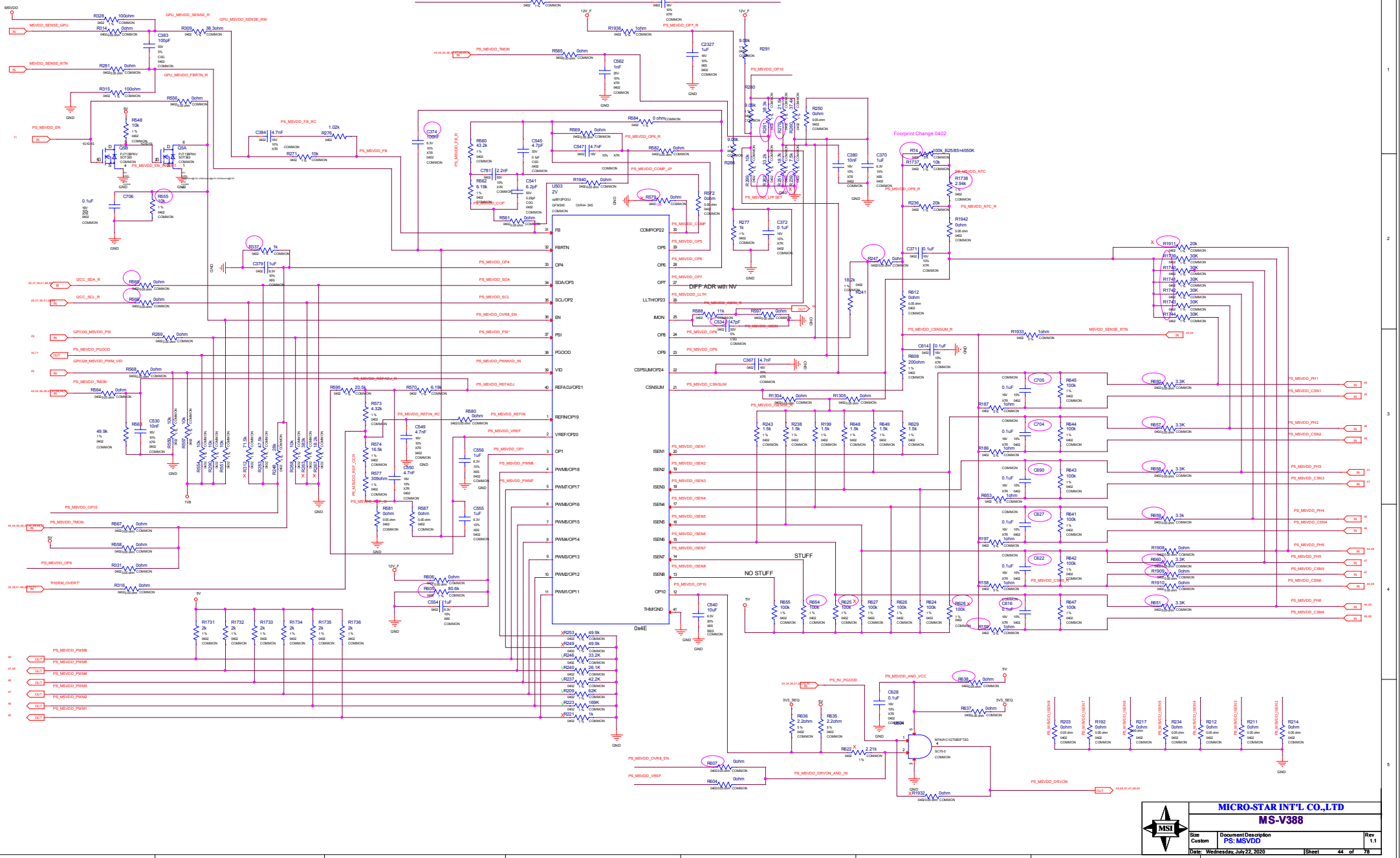
PS: MSVDD


DIFF ADR with NV
Footprint Change 0402
STUFF
NO STUFF
0x4E
MICRO-STAR INT'L CO.,LTD
MS-V388
Size: Custom
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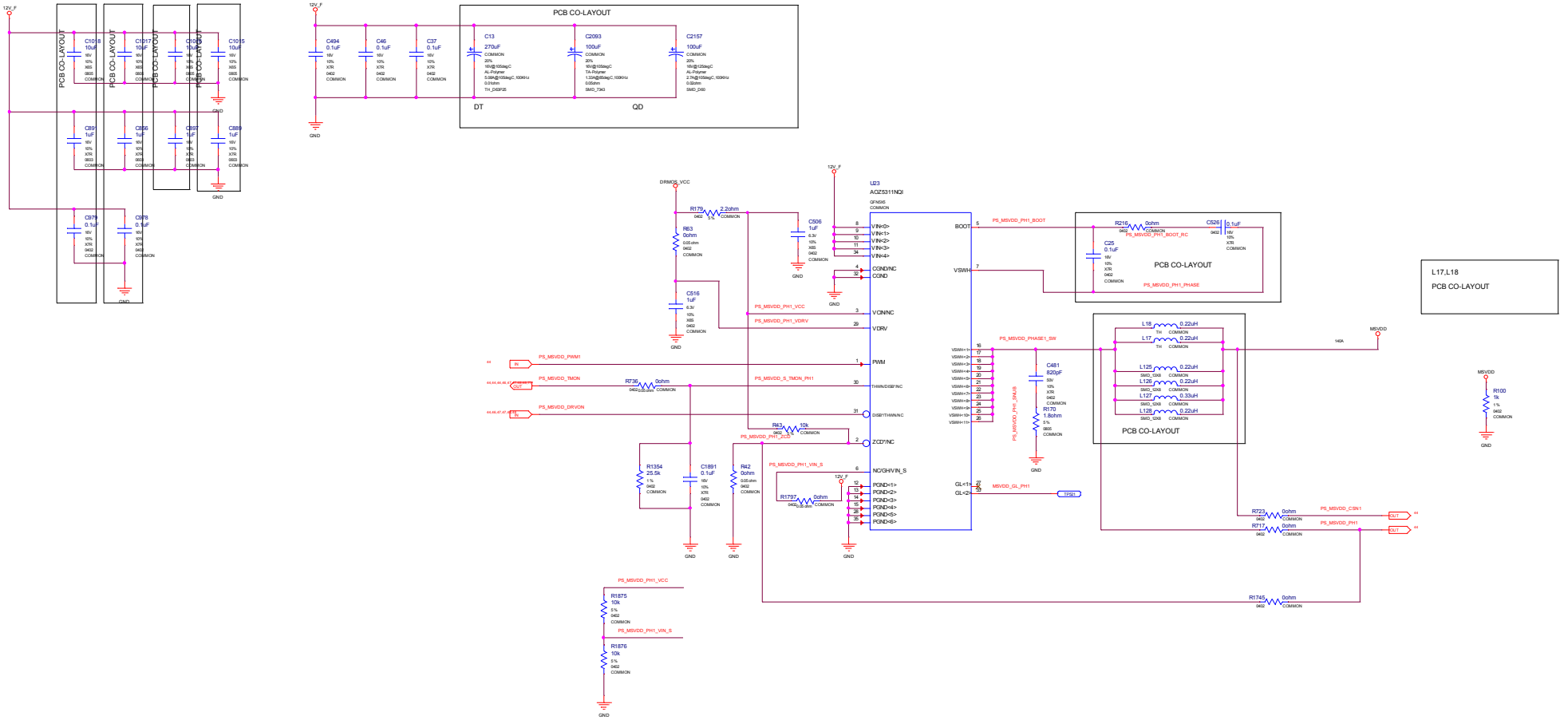
PS: MSVDD Phase 1



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	MS-V388	
Size: Custom	Document Description: PS: MSVDD Phase 1	Rev: 1.1
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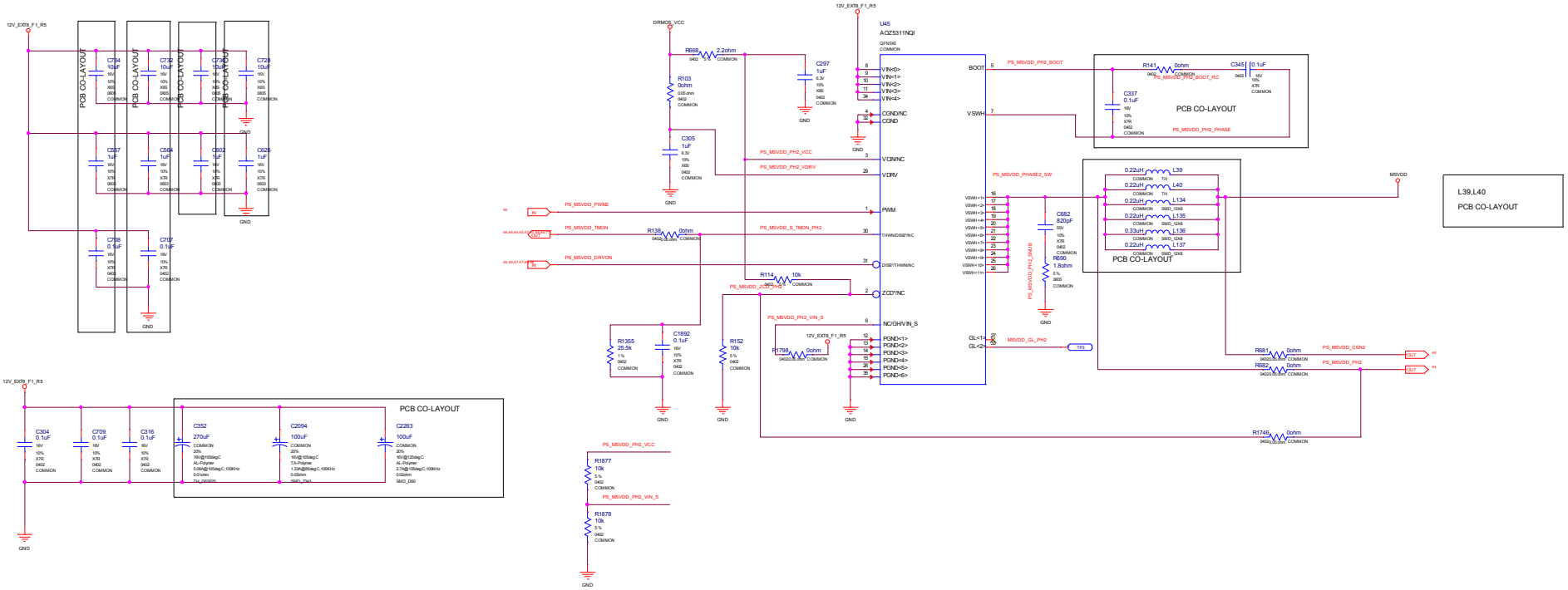
PS: MSVDD PH 2



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Size: Custom	Document Description: PS: MSVDD PH 2
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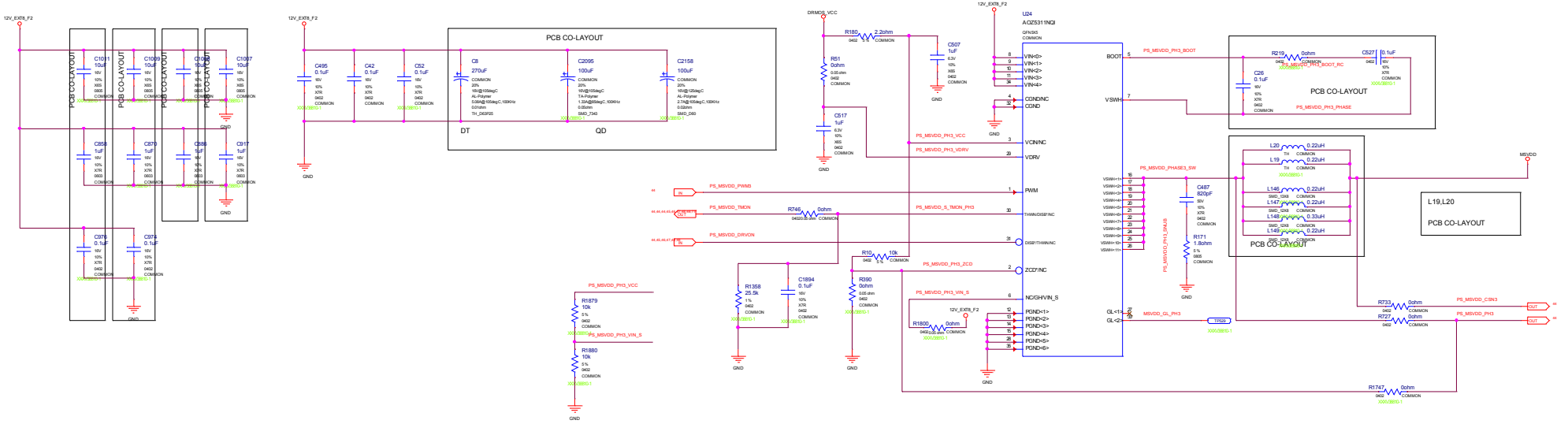
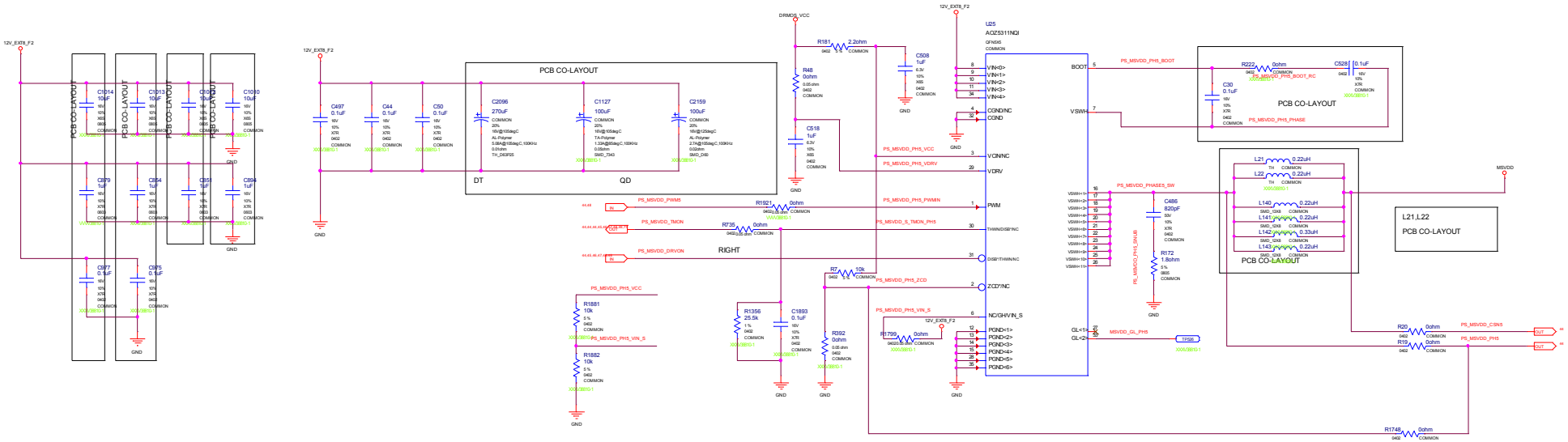
PS:MSVDD Phase 3, 5





MSI	MICRO-STAR INT'L CO.,LTD	
	MS-V388	
Size: Custom	Document Description: PS:MSVDD Phase 3, 5	Rev: 1.1
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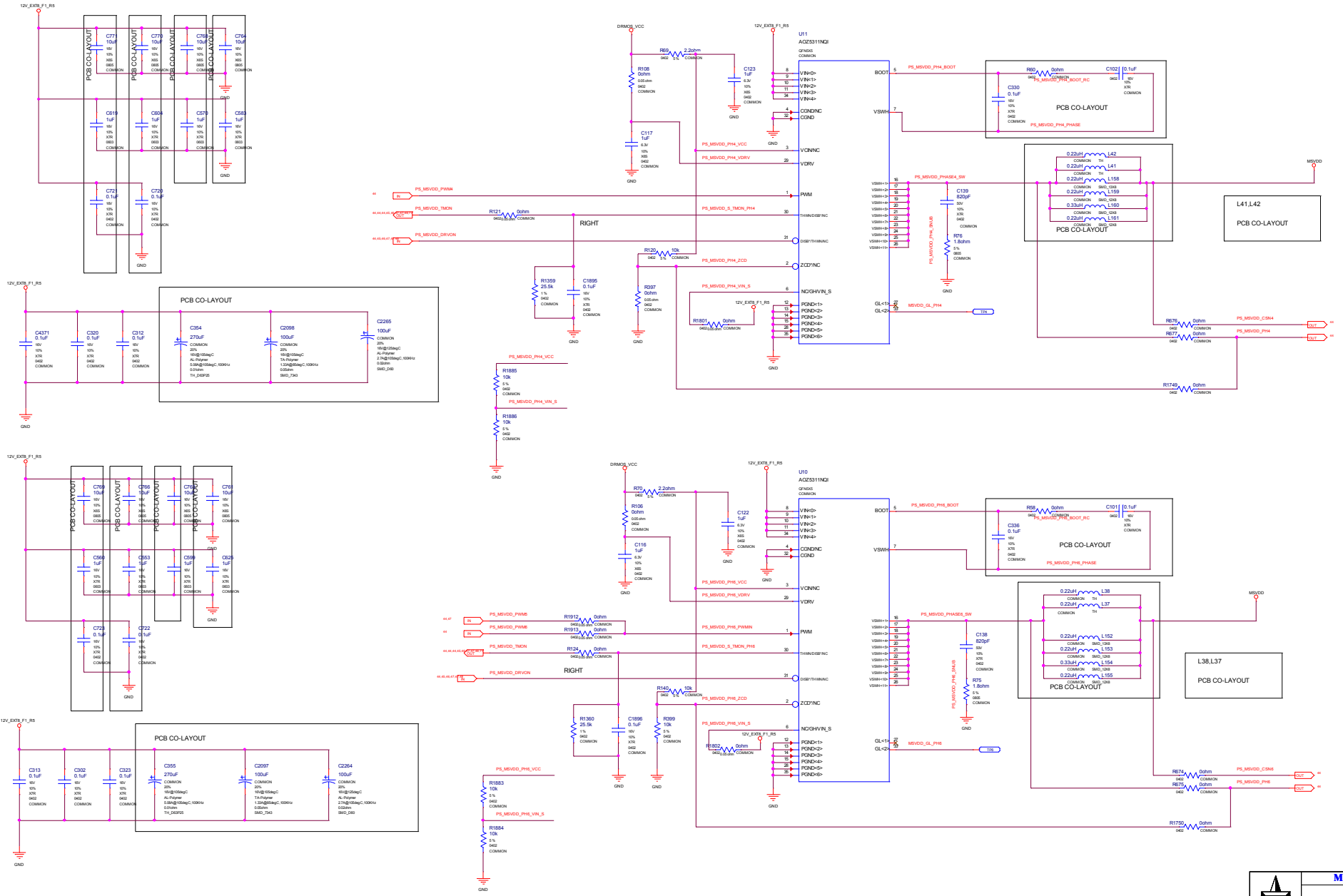
PS: MSVDD PH 4,6



MICRO-STAR INT'L CO.,LTD		
MS-V388		
Size: Custom	Document Description: PS: MSVDD PH 4,6	Rev: 1.1
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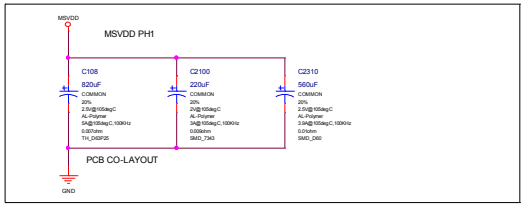
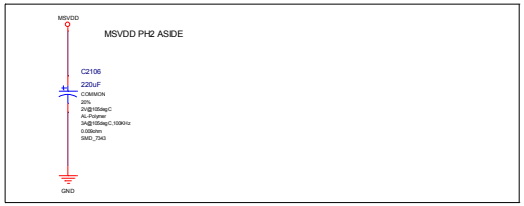
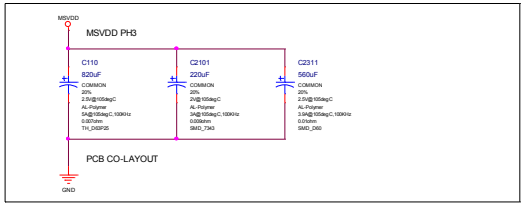
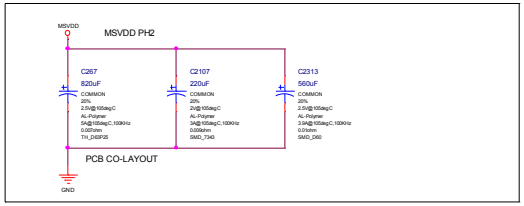
PS:MSVDD OUTPUT CAP (TOP)

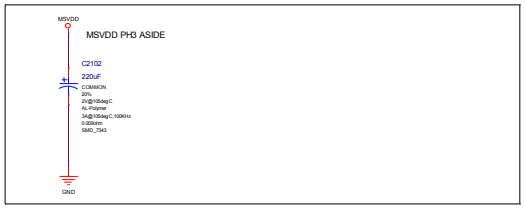
REFER TO PCB FOR BOM STUFFING

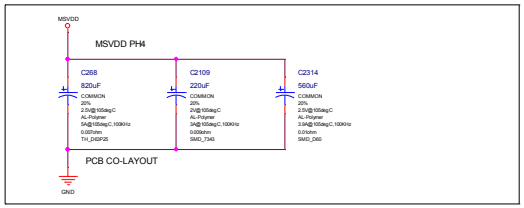


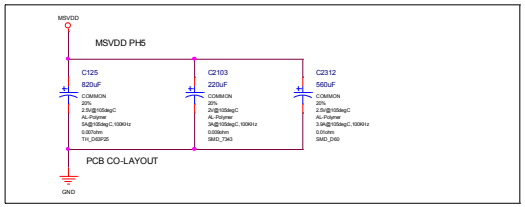


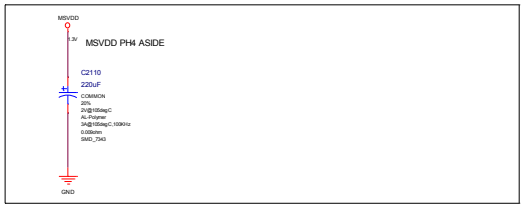


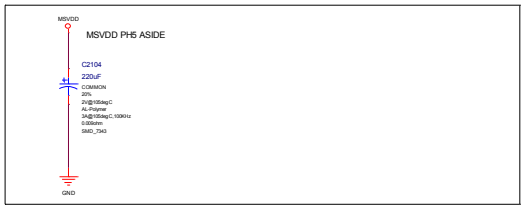


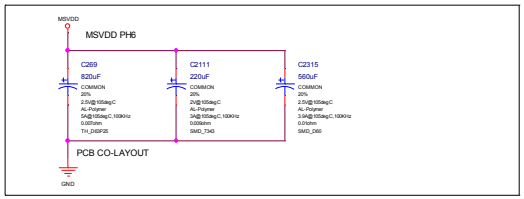


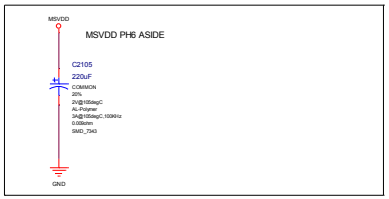












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MS-V388		
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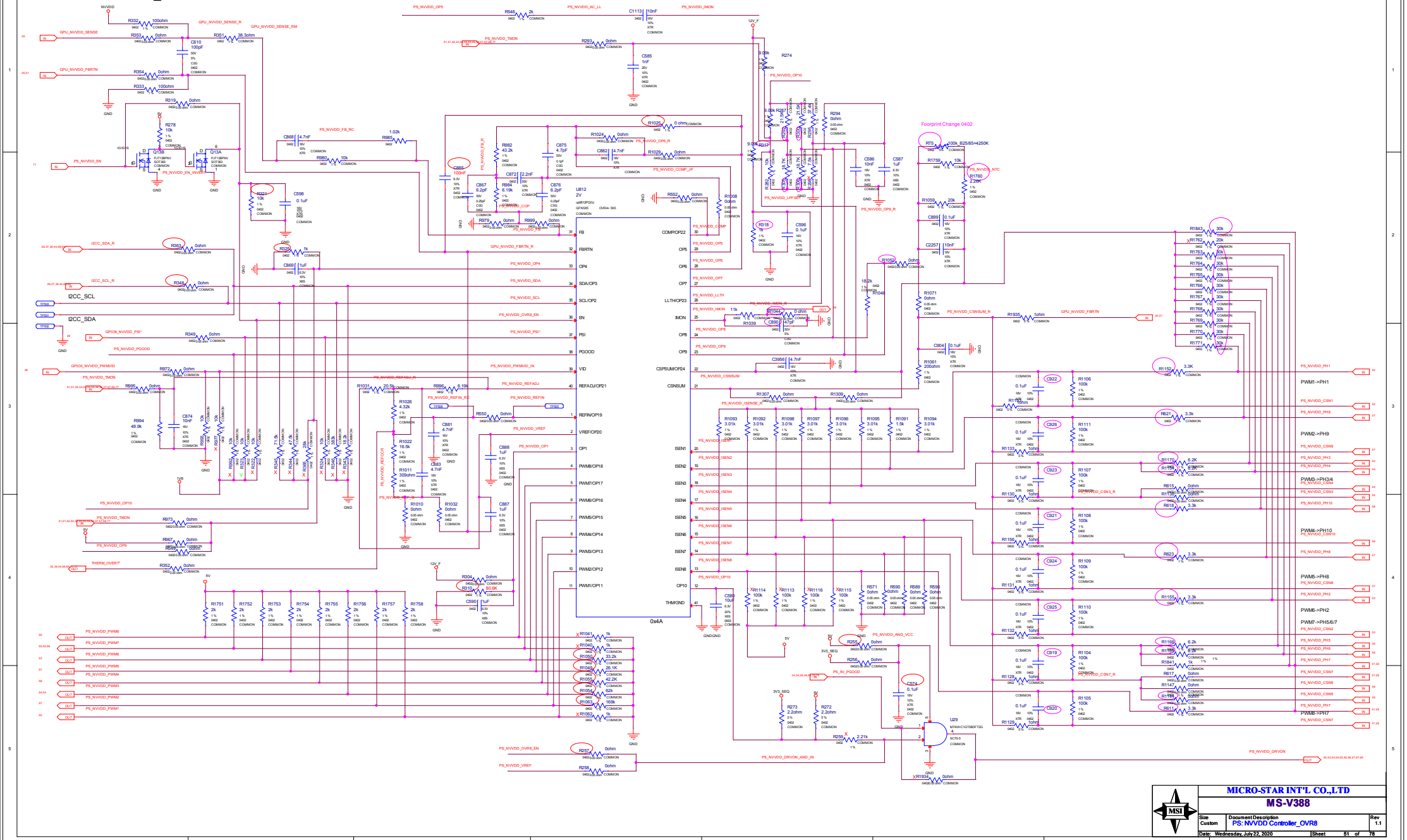
PS: NVVDD Controller_OVR8



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MS-V388		
Size: Custom	Document Description: PS: NVVDD Controller_OVR8	Rev: 1.1
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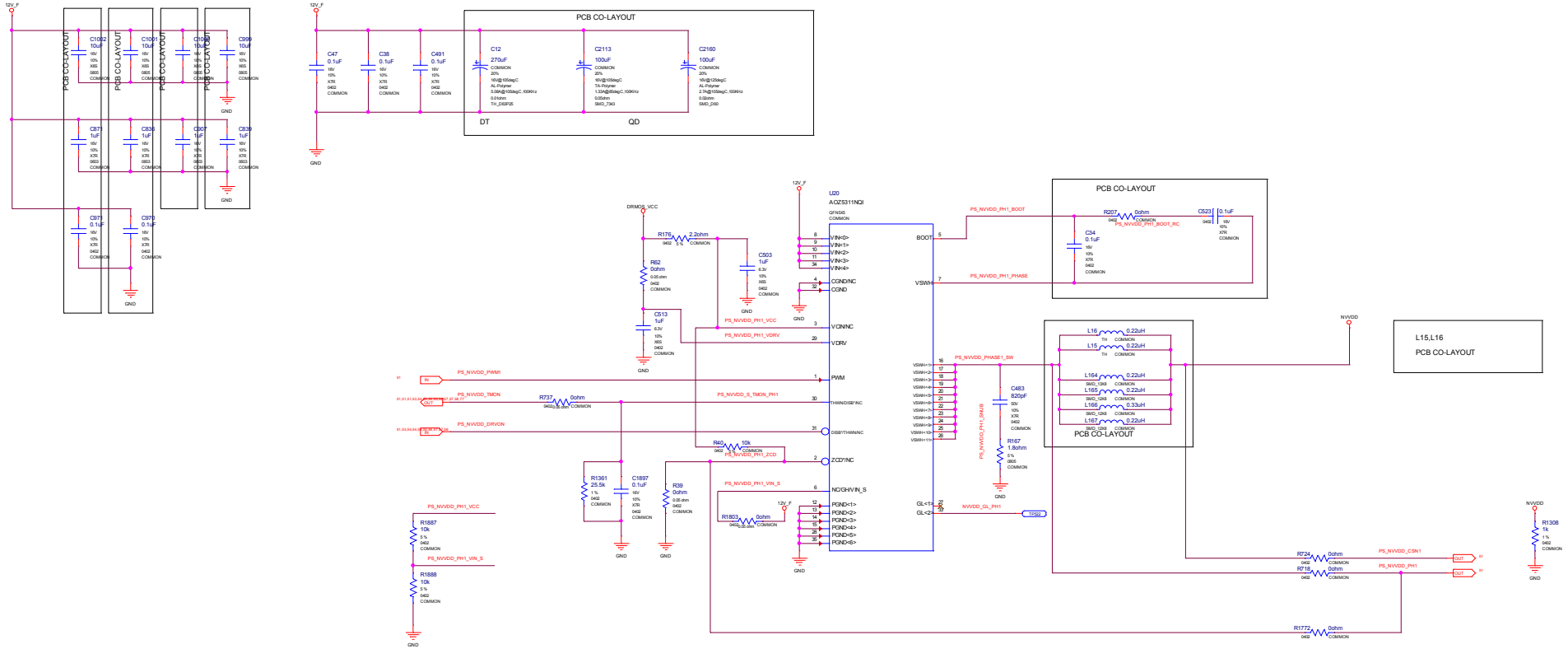
PS: NVVDD Phase 1



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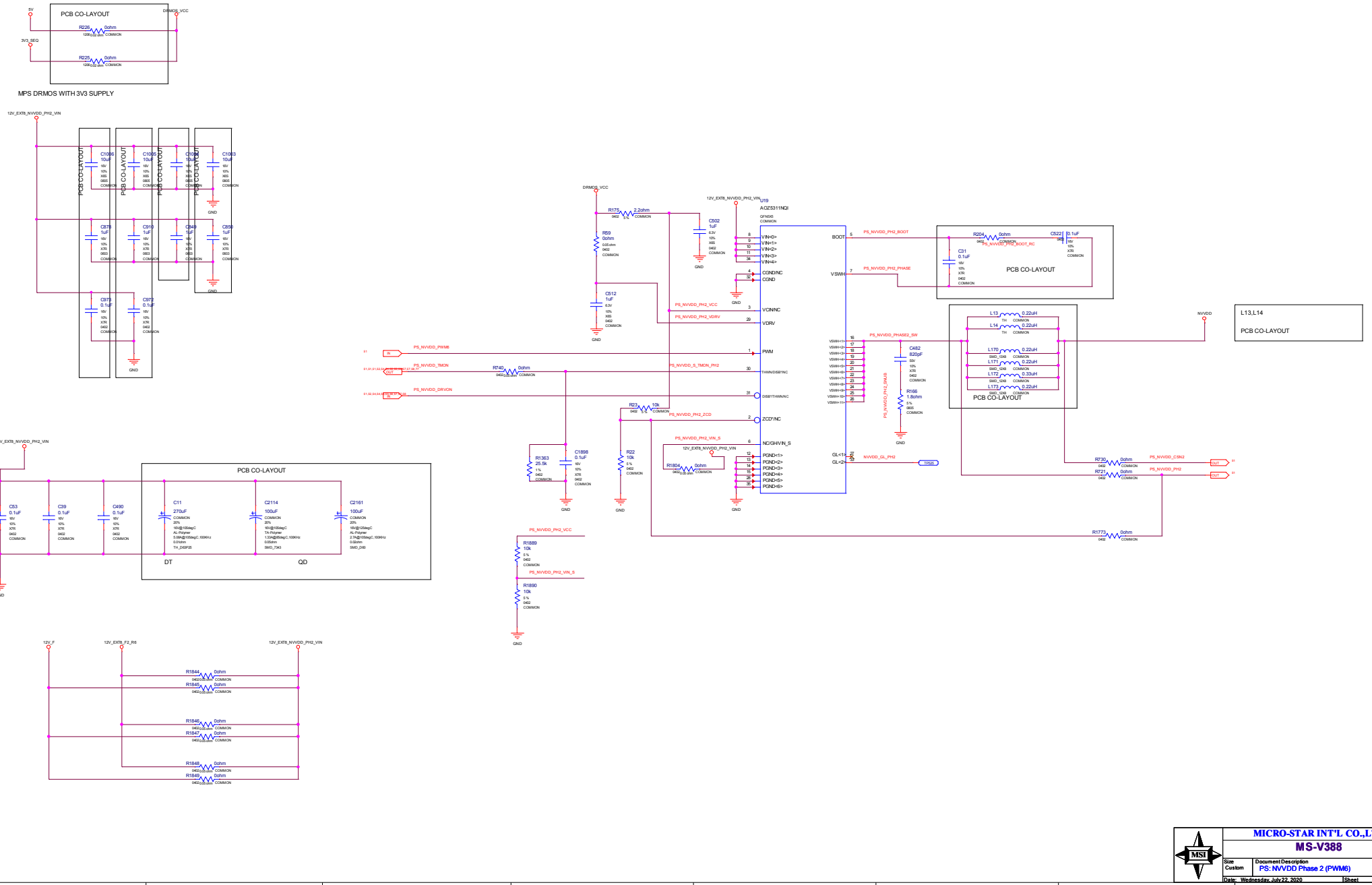
PS: NVVDD Phase 2 (PWM6)



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Size: Custom
Document Description: PS: NVVDD Phase 2 (PWM6)
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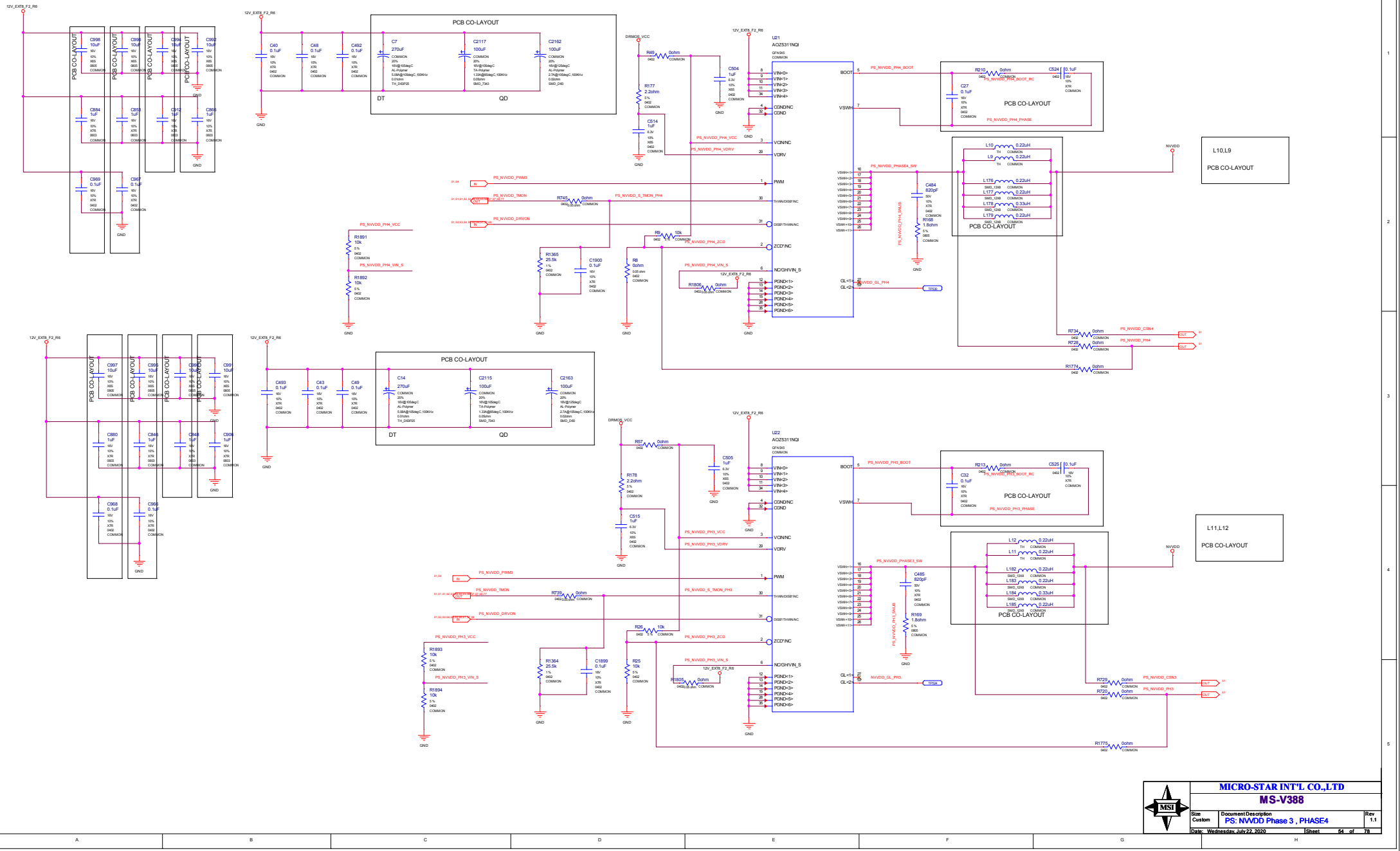
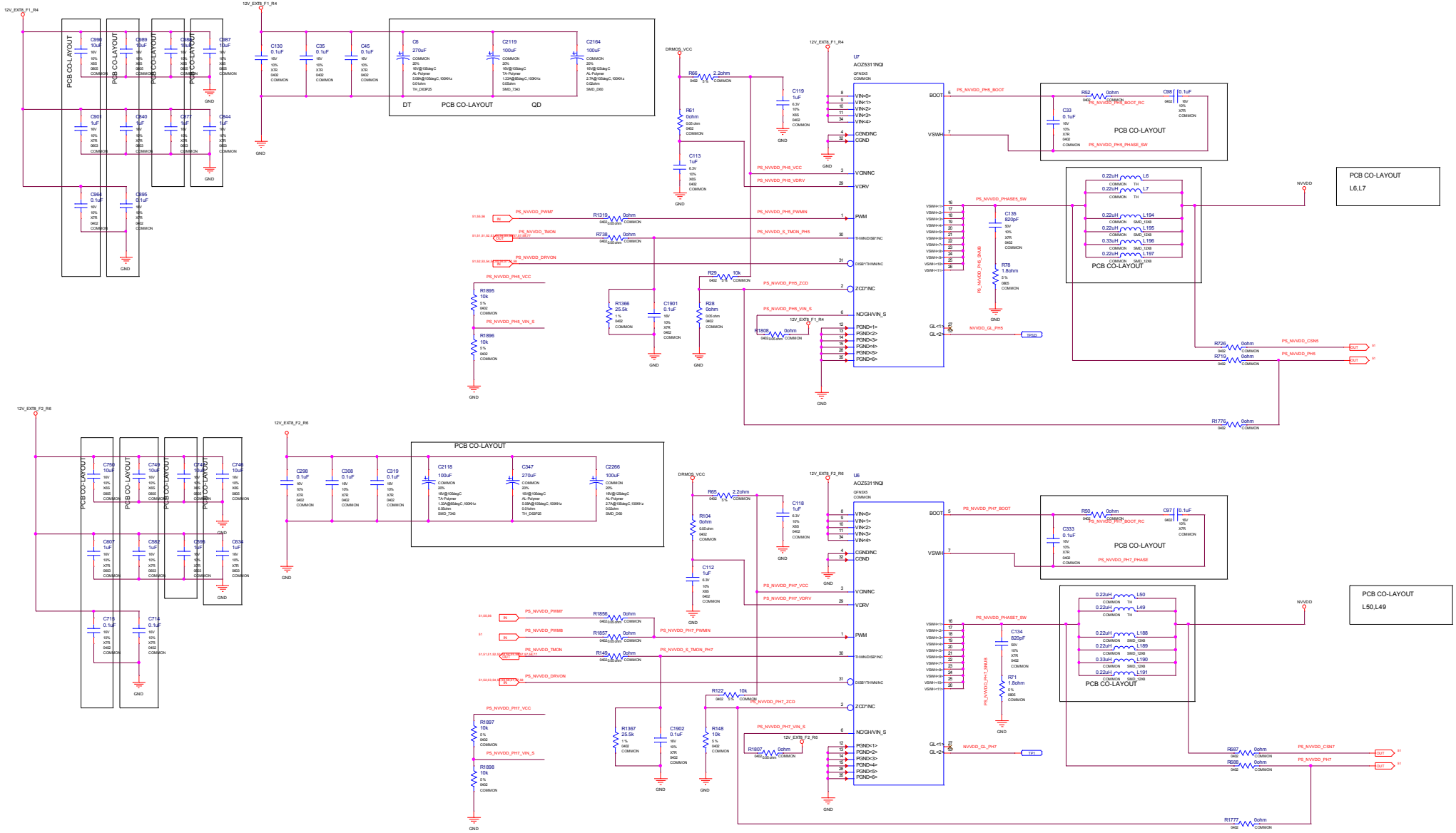
PS: NVVDD Phase 3 (PWM3), PHASE4 (PWM3)



PS: NVVDD PH 5(PWM4), PH7(PWM8/4)



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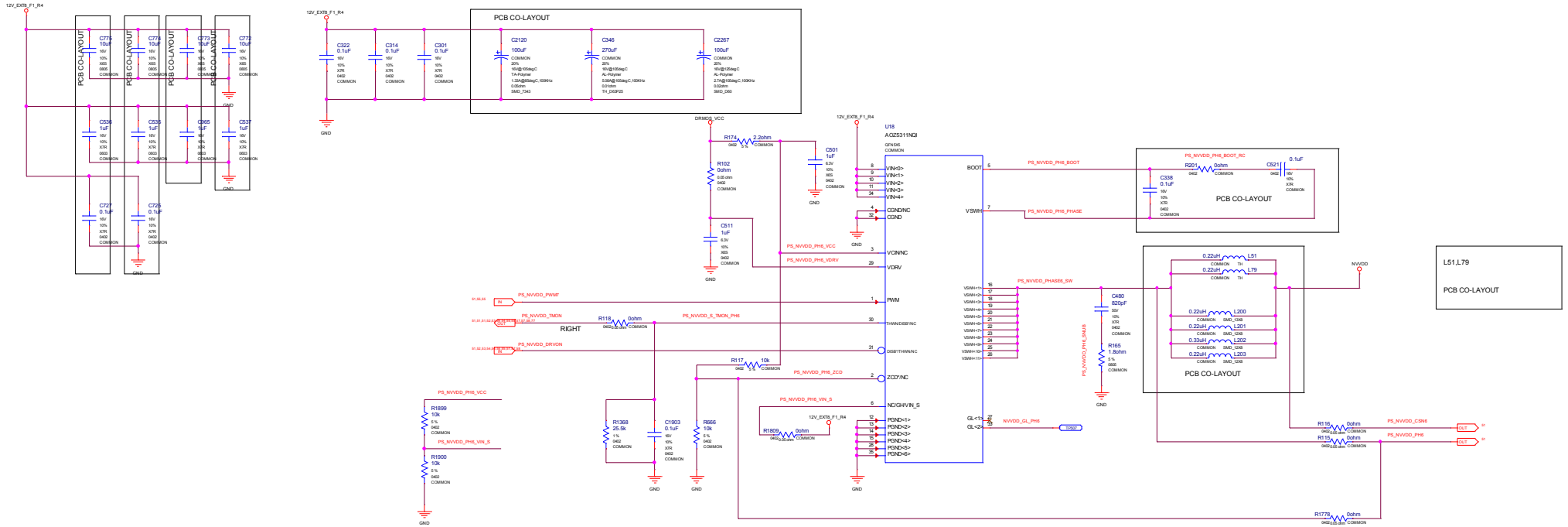
PS: NVVDD Phase 6(PWM4)



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Size: Custom	Document Description: PS: NVVDD Phase 6(PWM4)
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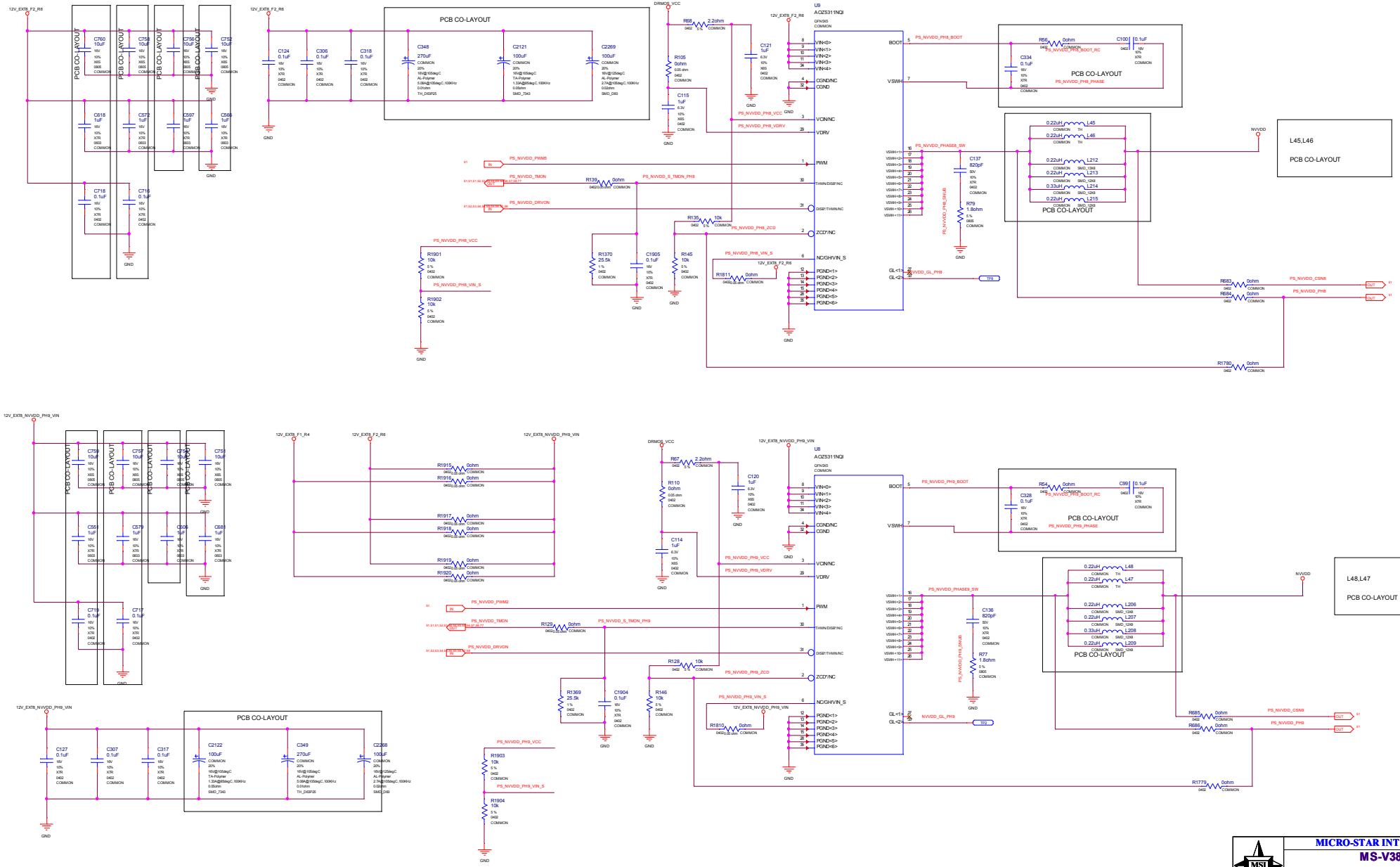
PS: NVVDD PH 8 (PWM5), PH 9(PWM2)



MICRO-STAR INT'L CO.,LTD	
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Size: Custom	Document Description: PS: NVVDD PH 8 (PWM5), PH 9(PWM2)
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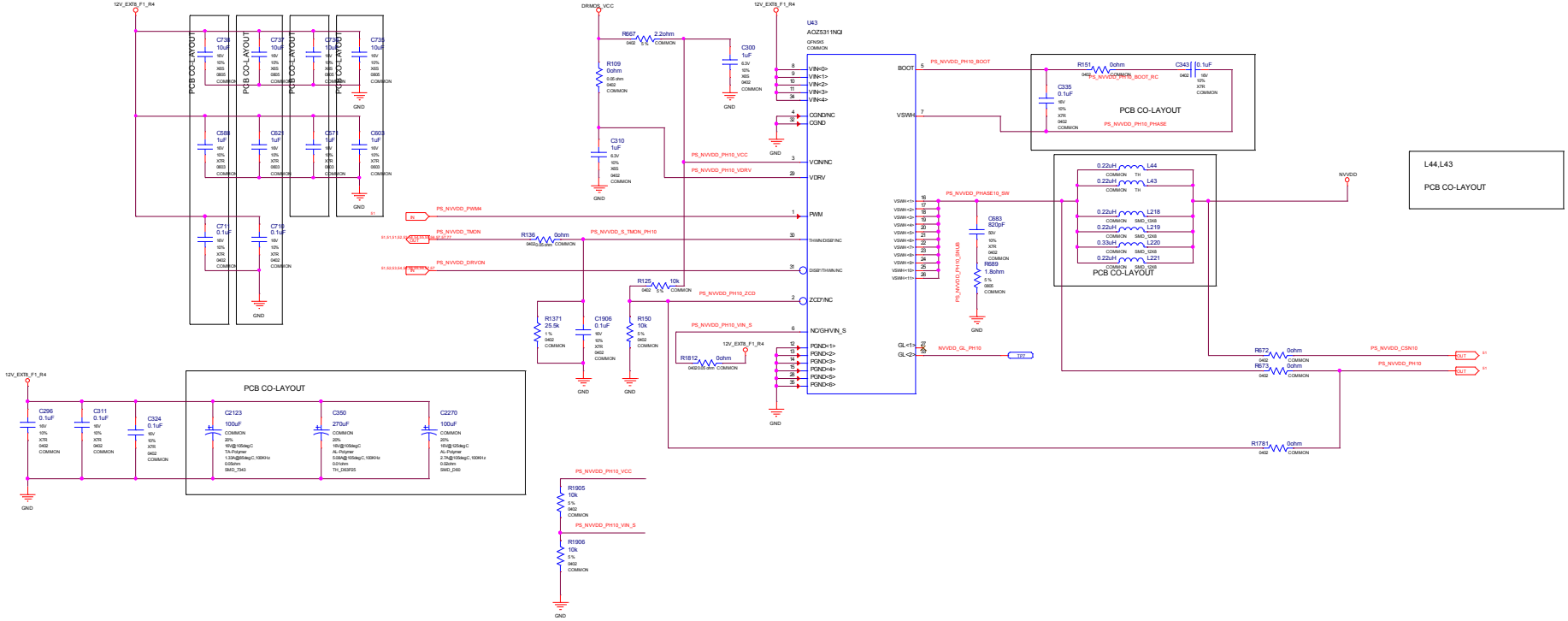
PS: NVVDD Phase 10 (PWM7)



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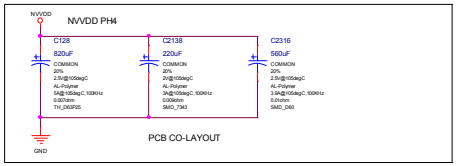
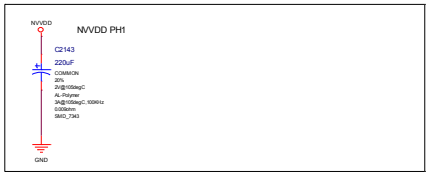
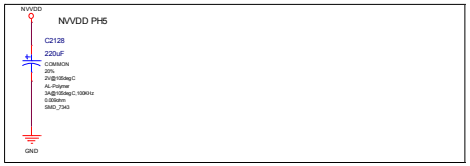
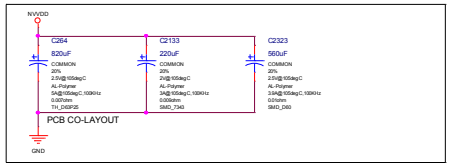
PS: NVVDD OUTPUT CAP(TOP)

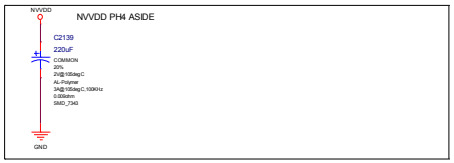
REFER TO PCB FOR BOM STUFFING

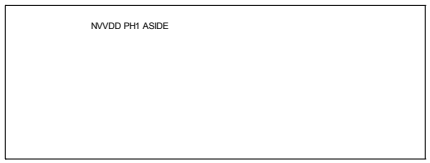


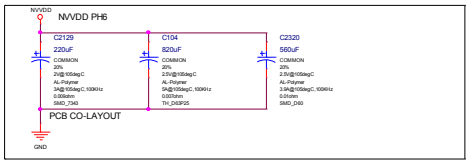


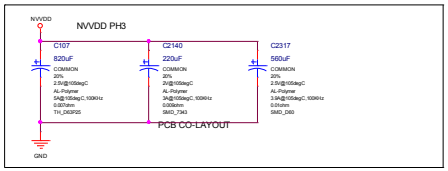


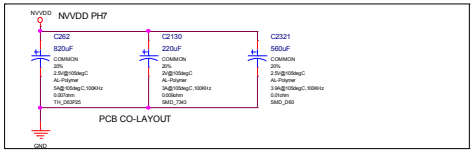


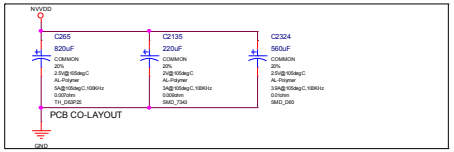


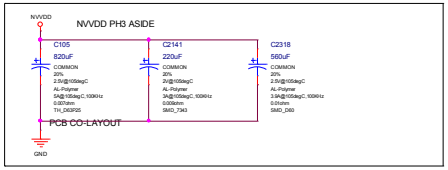


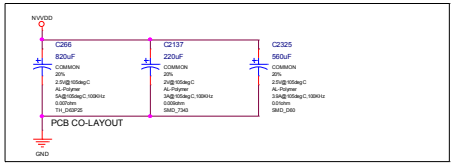


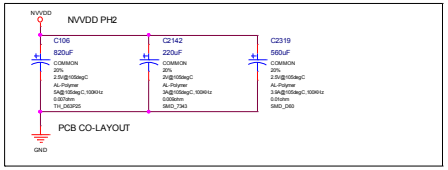


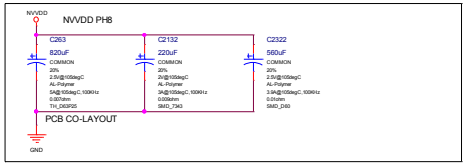












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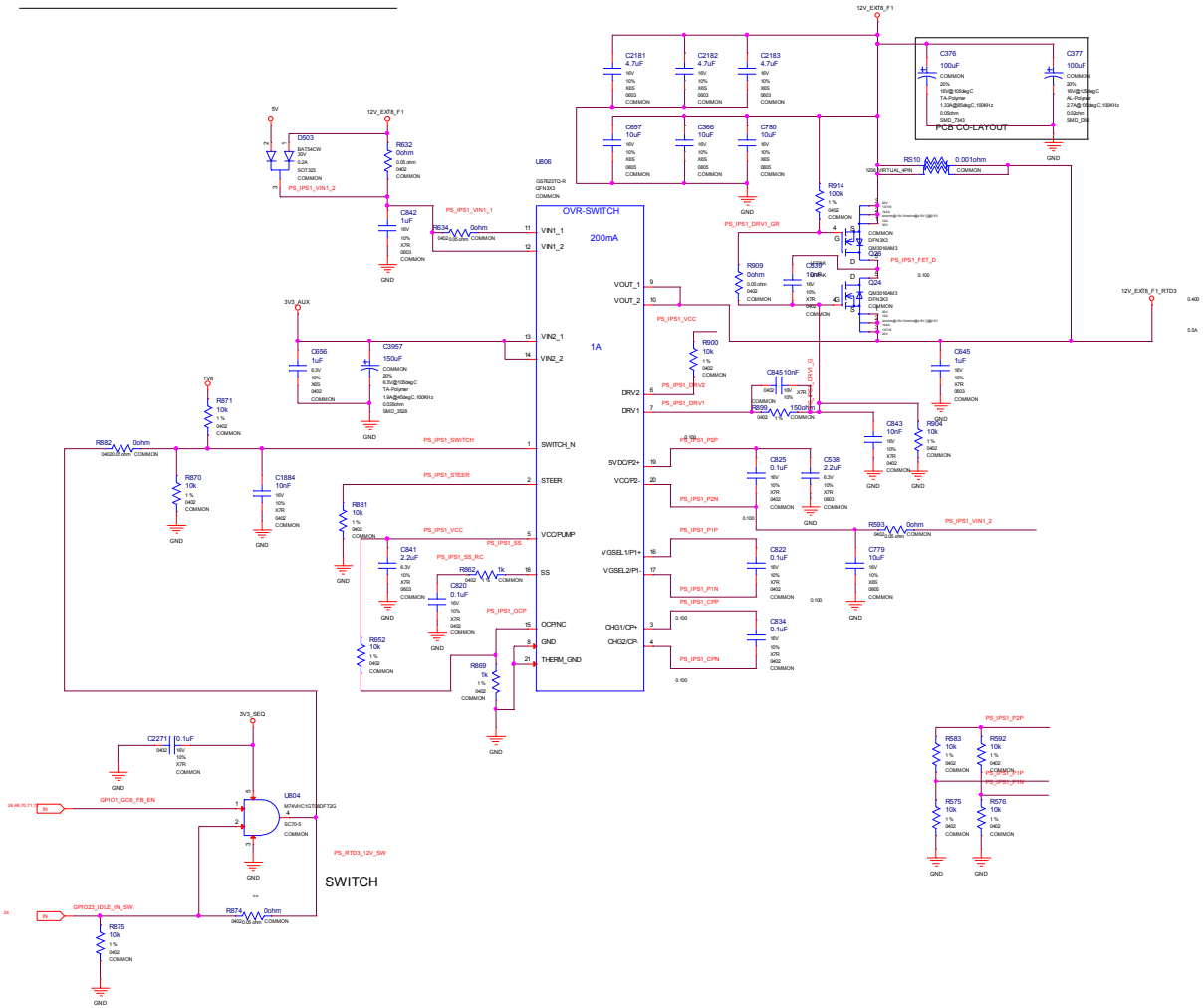
PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO23	SWITCH	VOUT
0	0	0	12V_F
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



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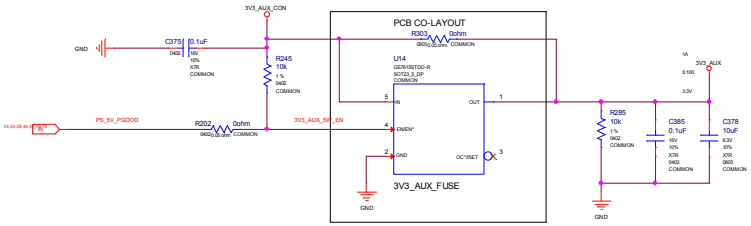
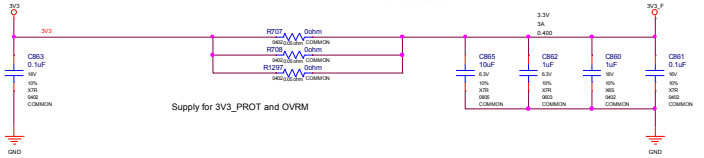
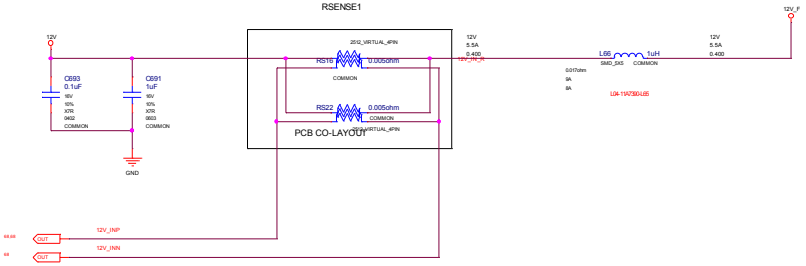
PS: Inputs, Filtering, and Monitoring



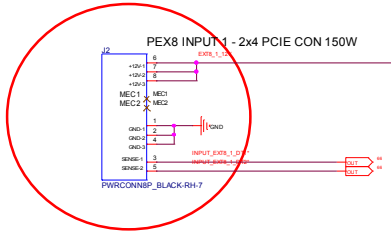
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W

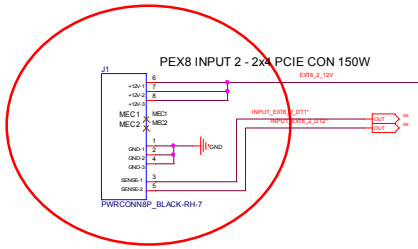


PEX8 INPUT 1 - 2x4 PCIE CON 150W



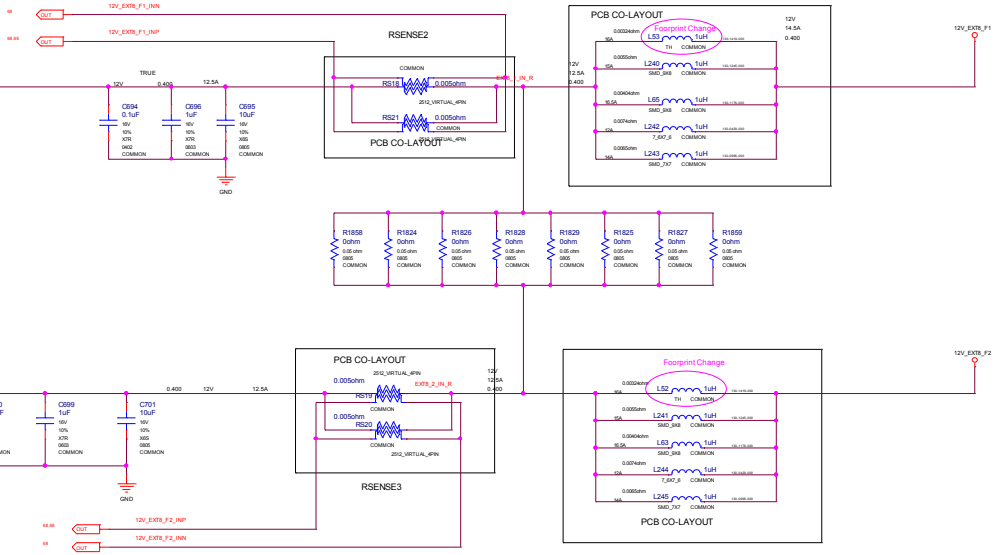
改反向8pin

PEX8 INPUT 2 - 2x4 PCIE CON 150W



J24,J25,J26,J27 Remove

QD SKU CABLE



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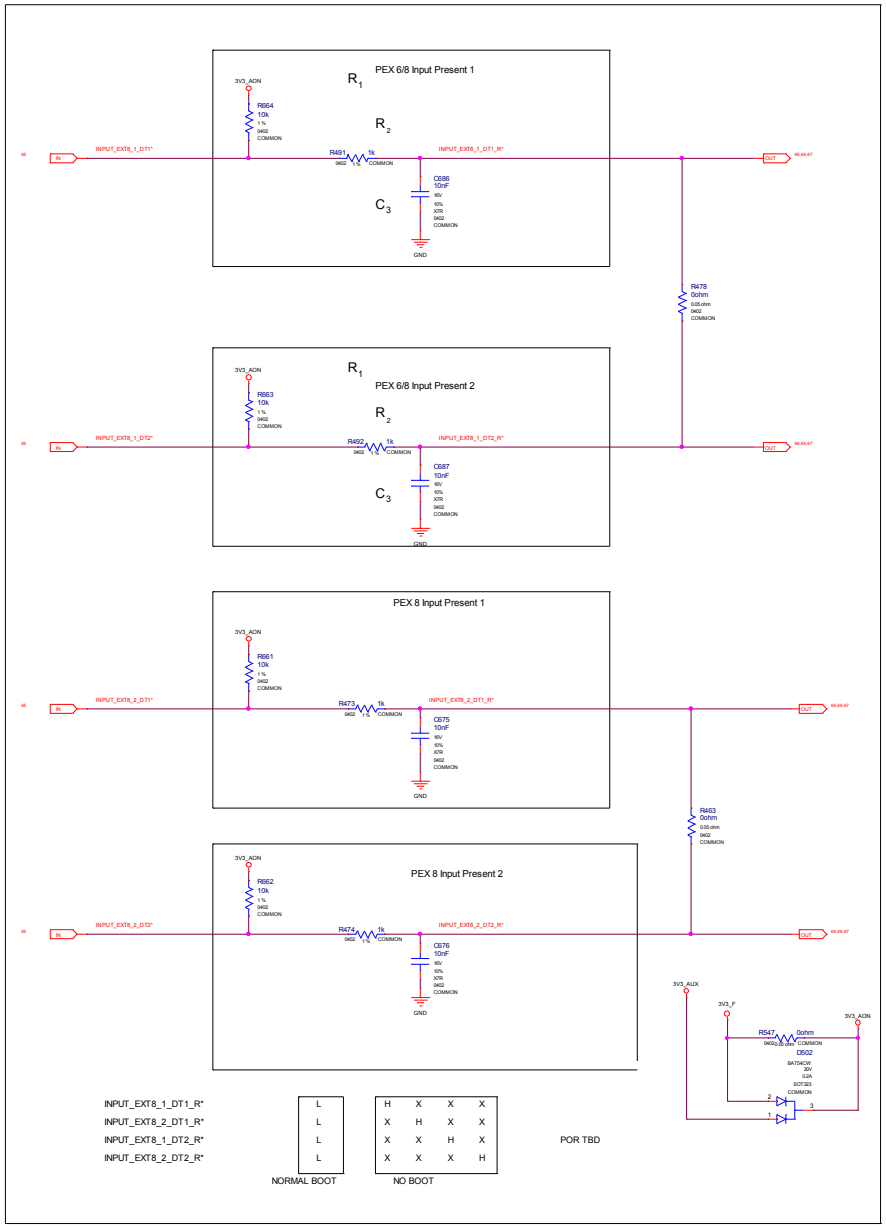
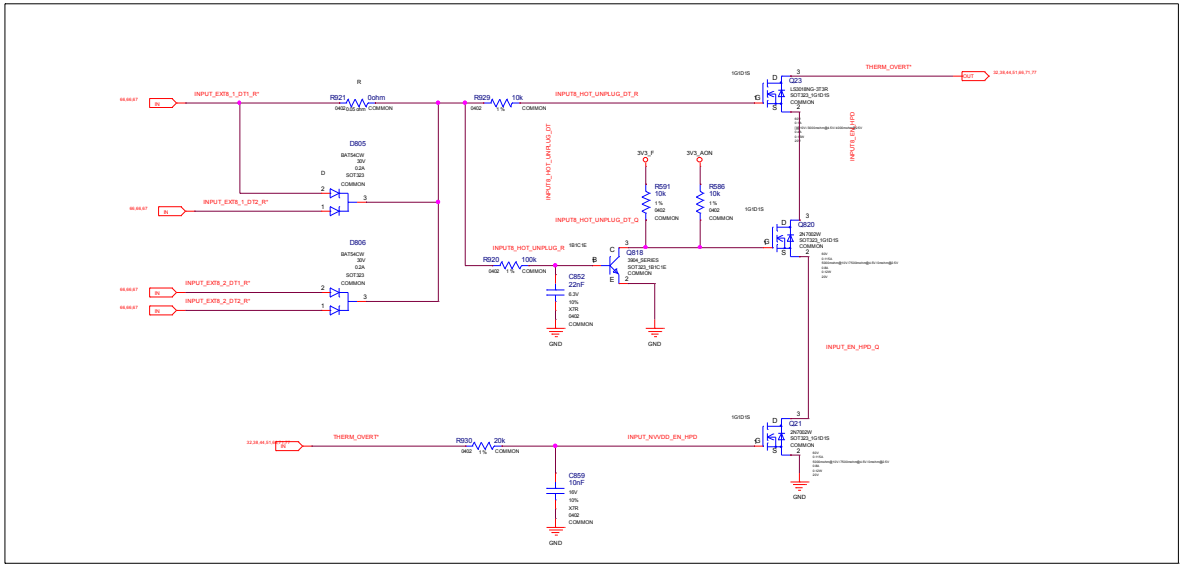
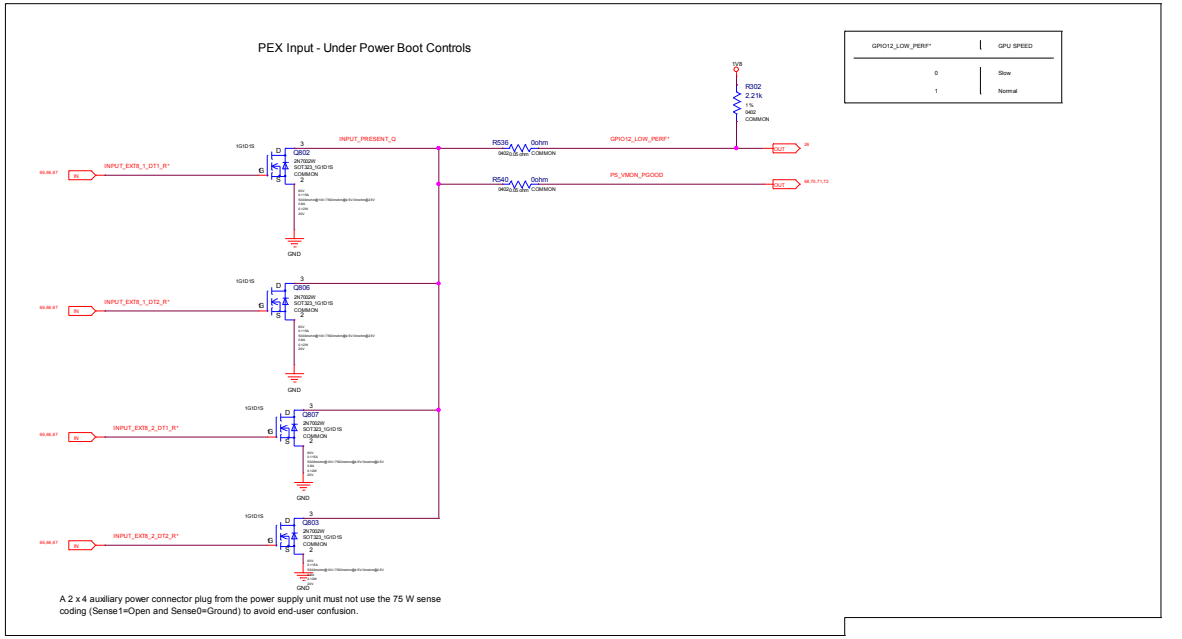
PS: 12V Current Steering & Hot Unplug Detect







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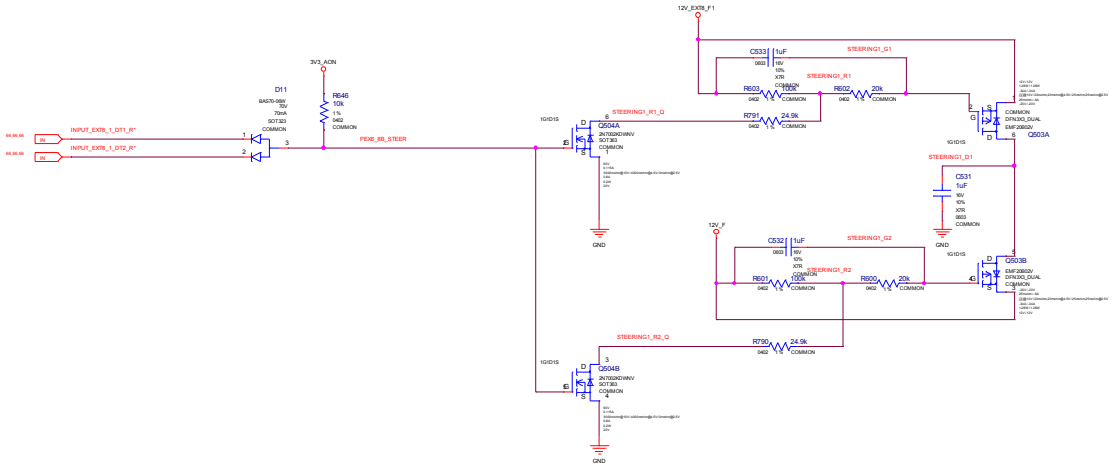
PS: Discrete Steering

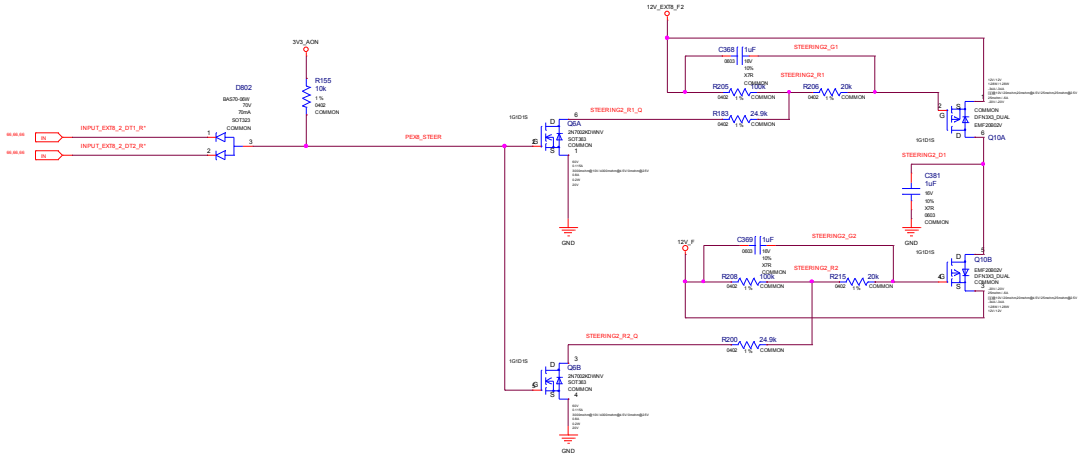
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V_EXT8_F1



NO STUFF BY DEFAULT REF ONLY

PEX12V AND 12V_EXT8_F2



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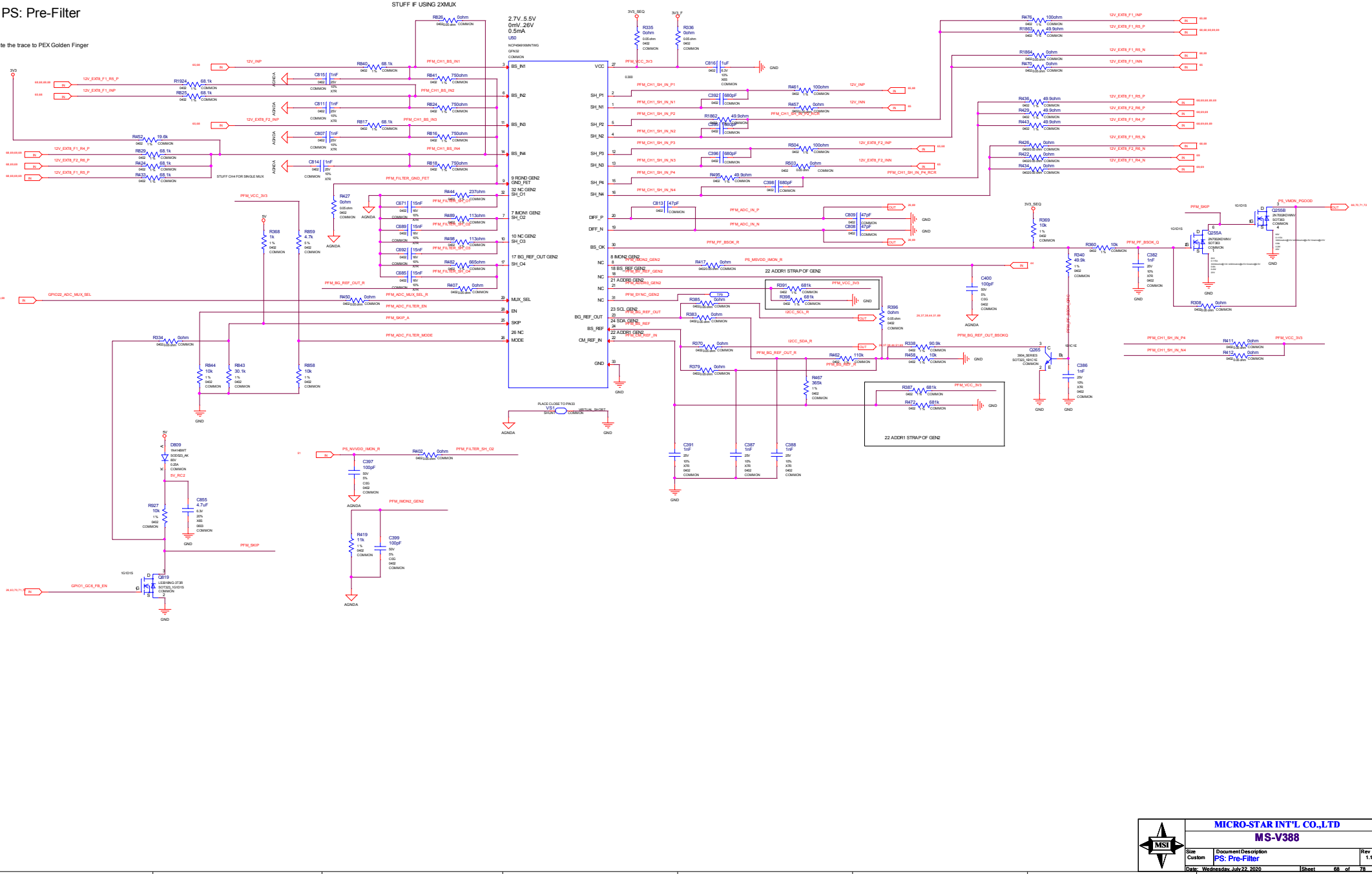
PS: Pre-Filter

Route the trace to PEX Golden Finger



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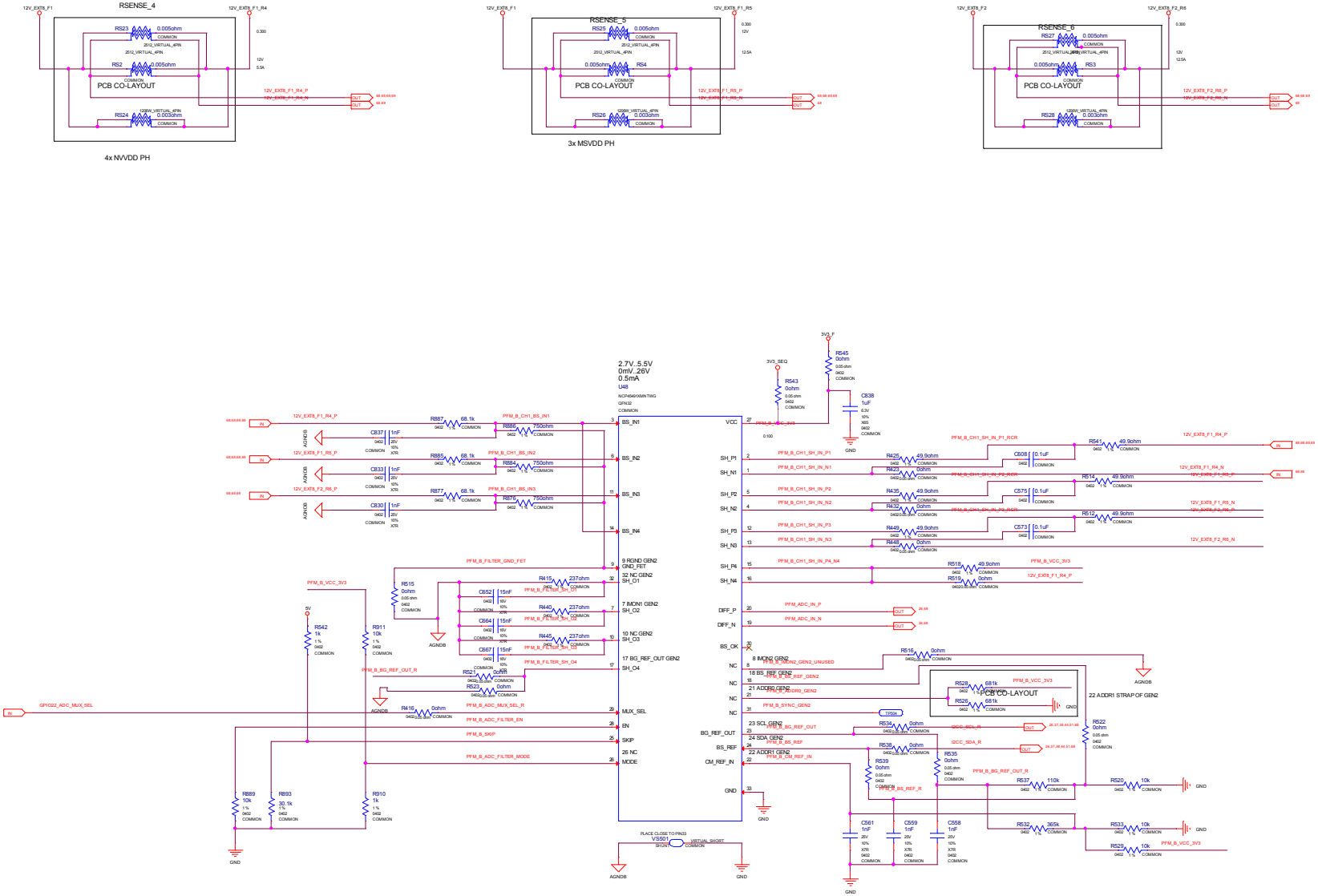
PS: Pre-Filter B



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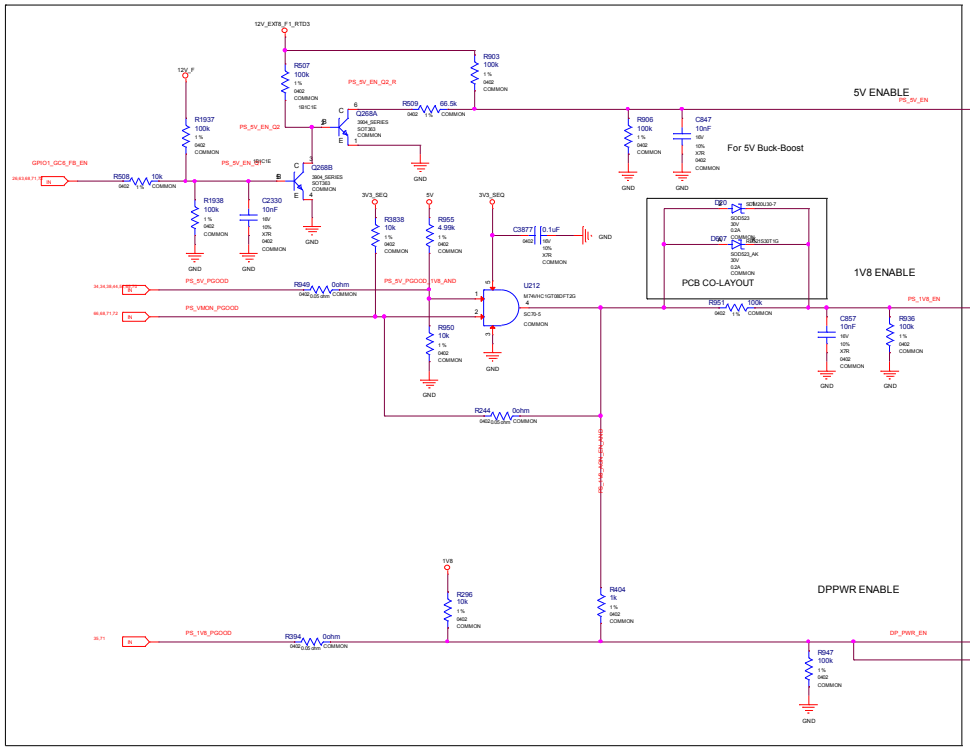
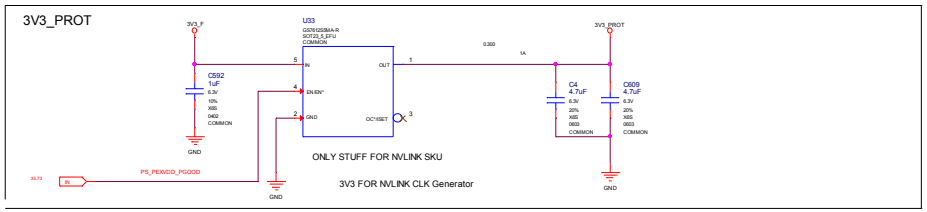
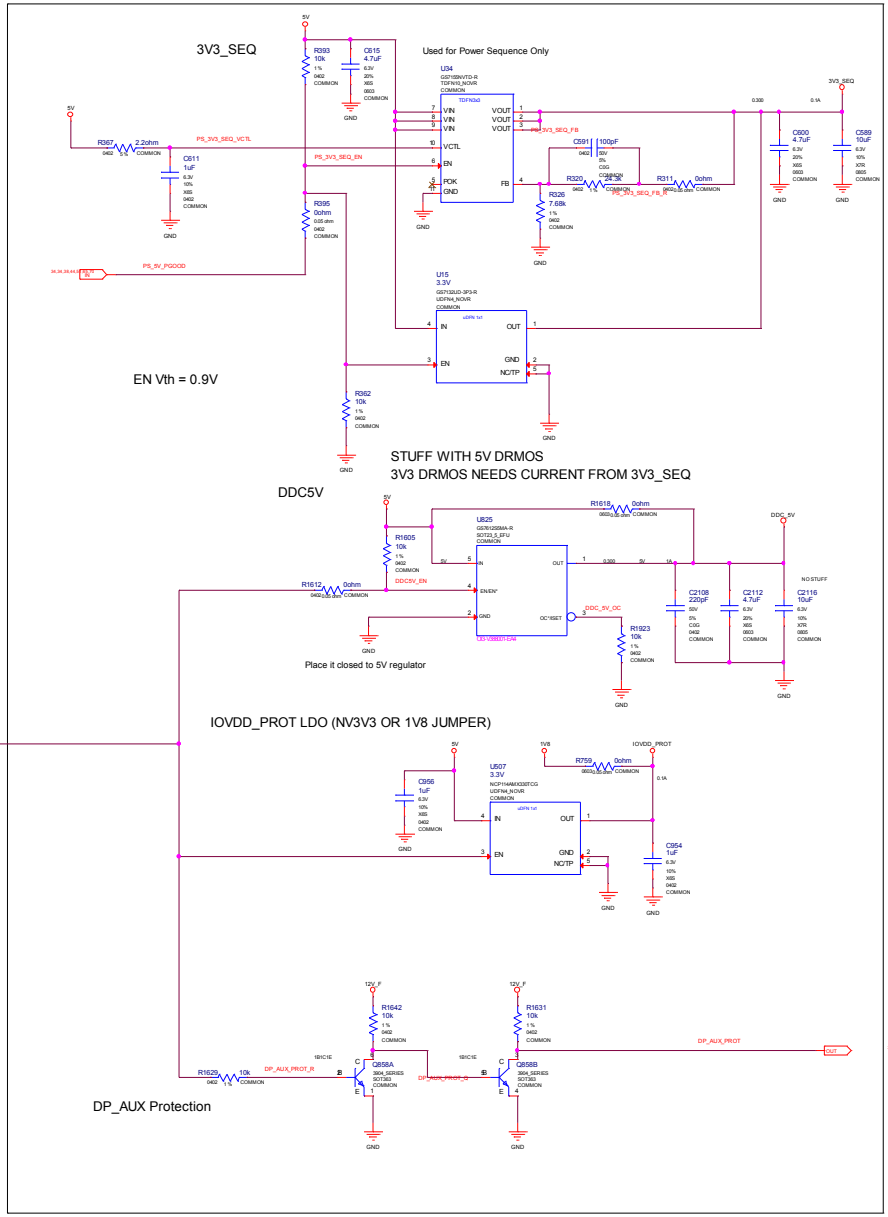
SEQUENCE:5V,1V8,3V3_SEQ ENABLE







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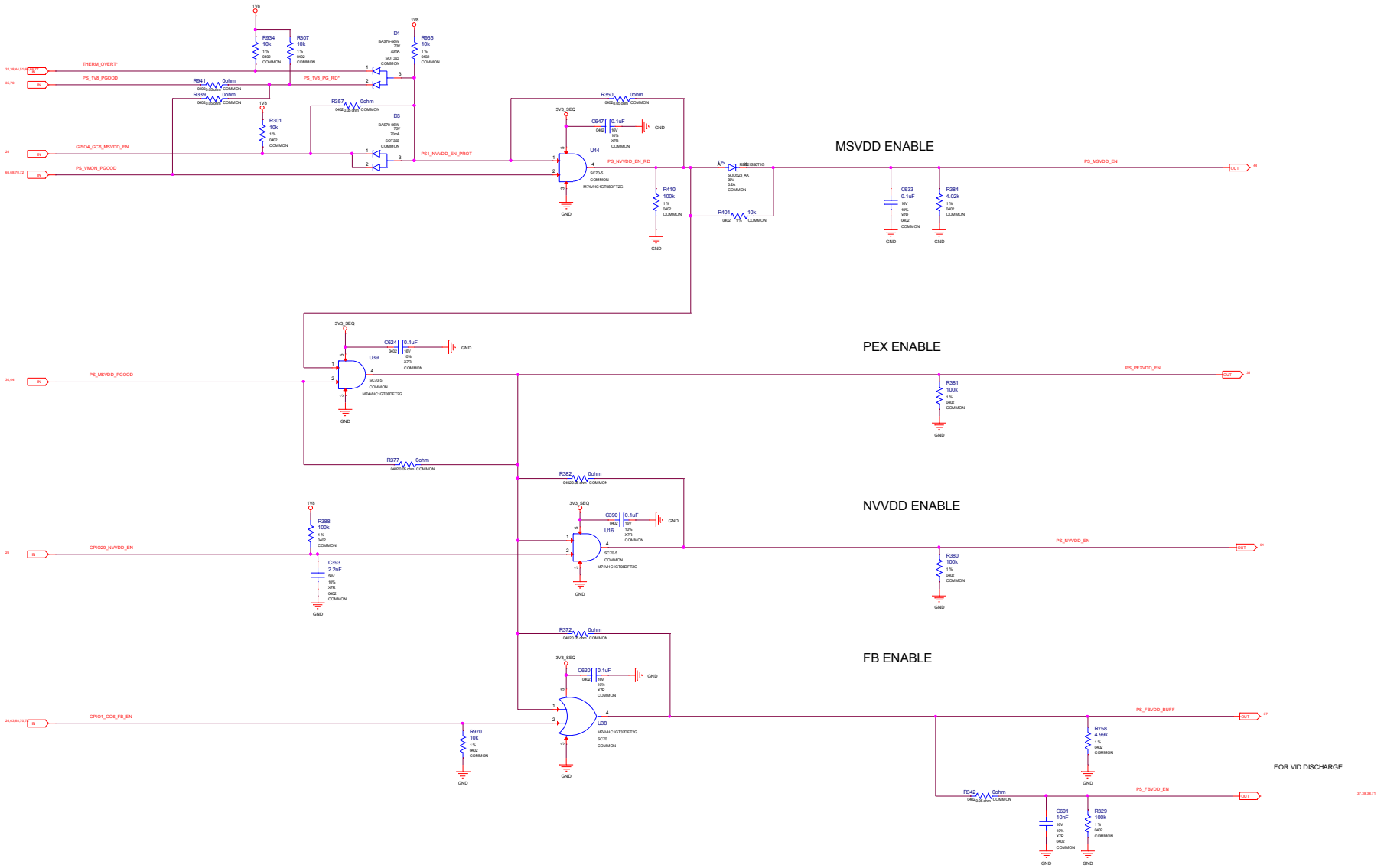
SEQUENCE:NV,PEX,FB ENABLE



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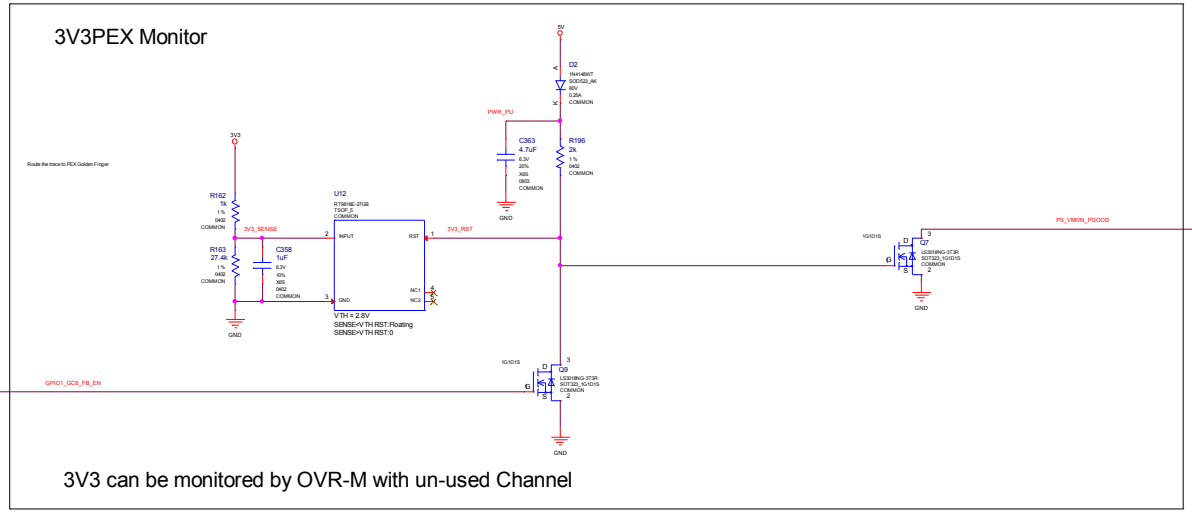

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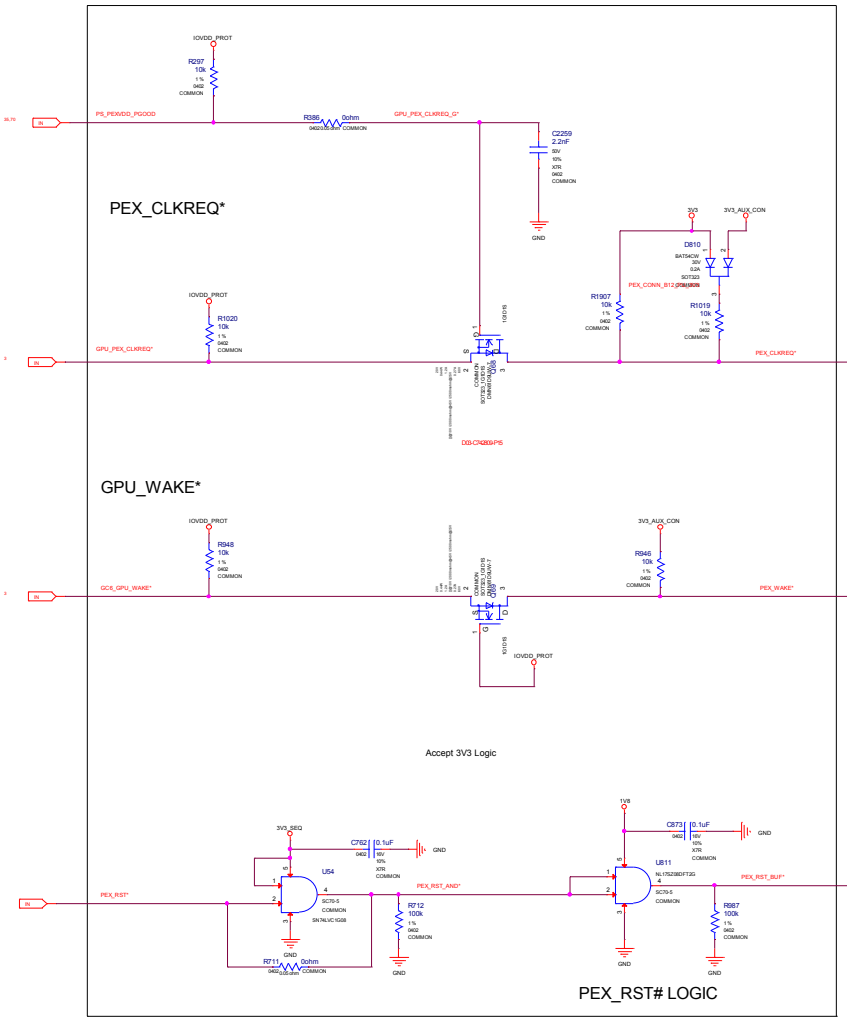
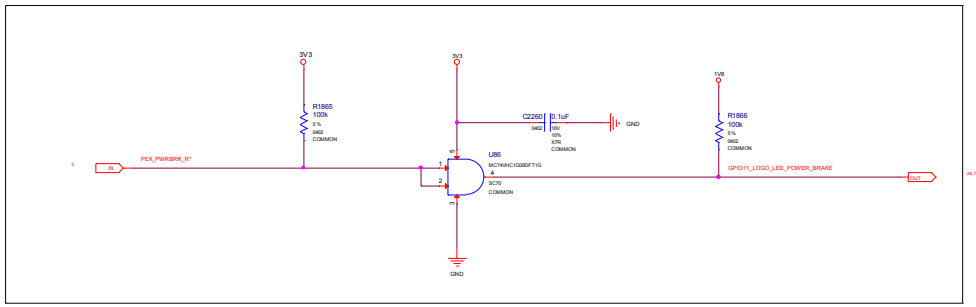
SEQUENCE:MISC





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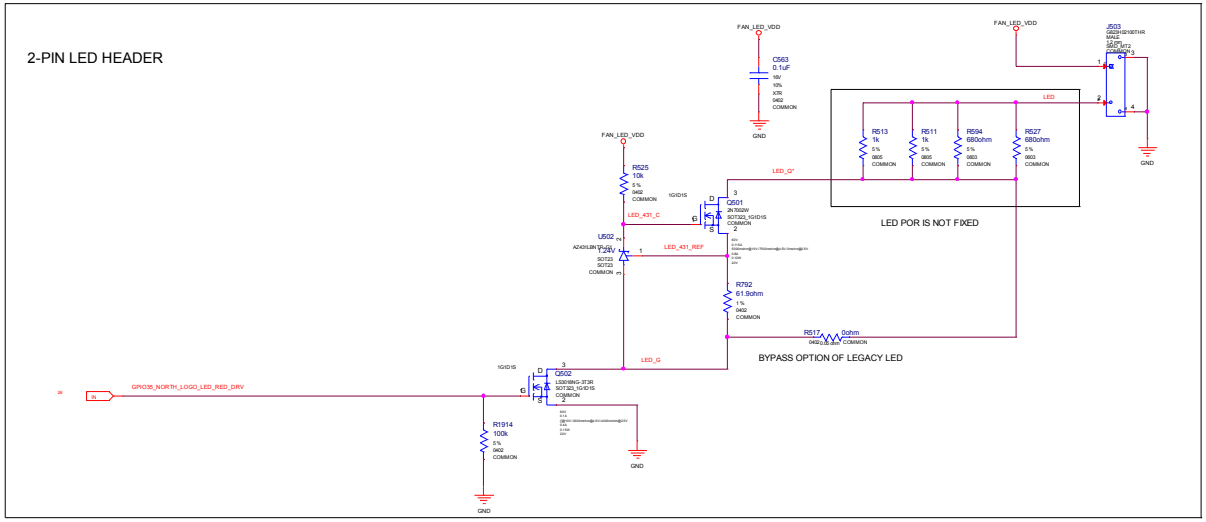
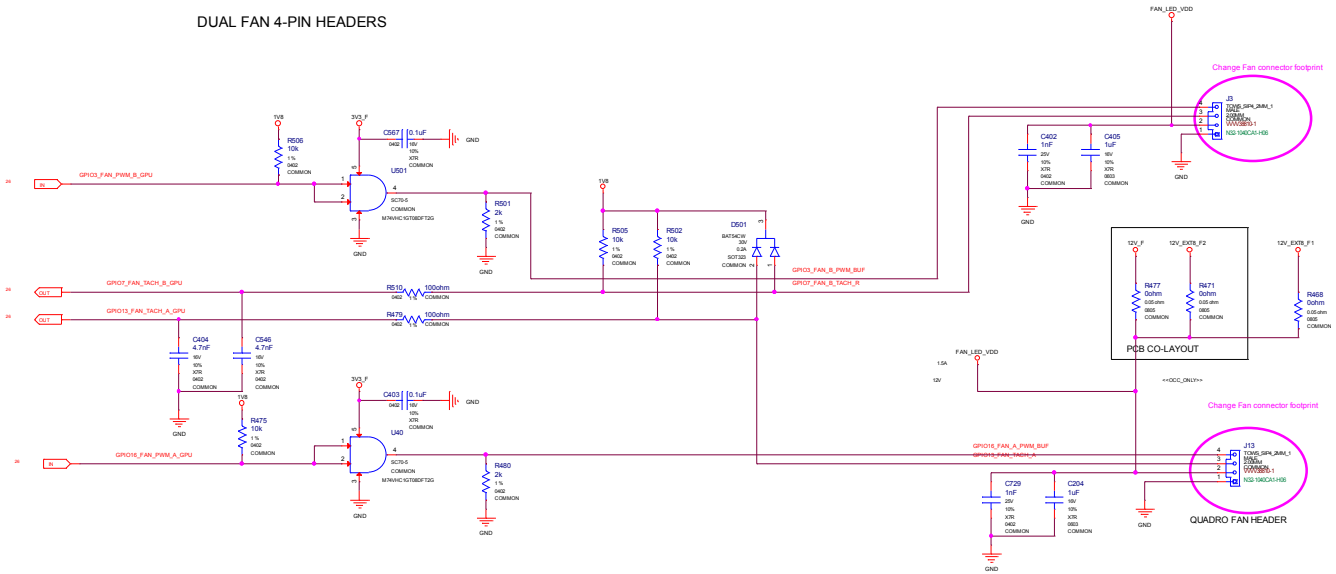
MISC: LED & FAN

2-PIN LED HEADER



DUAL FAN 4-PIN HEADERS



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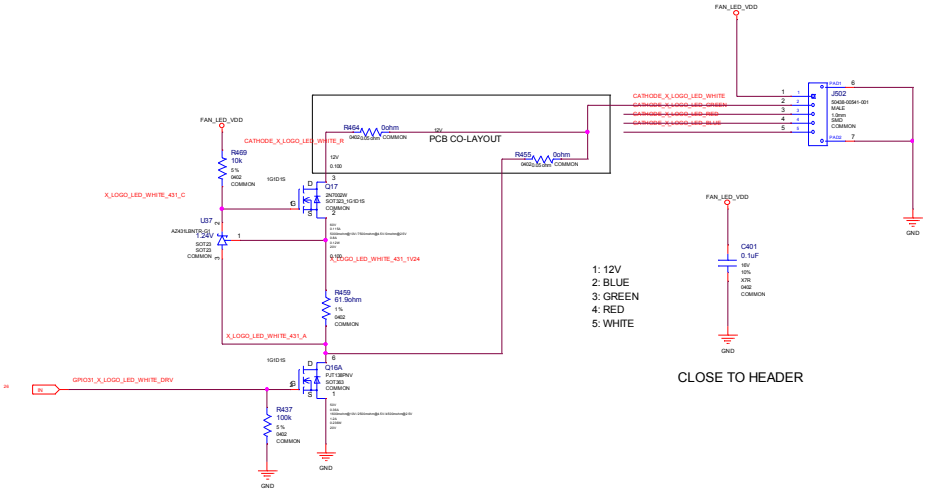
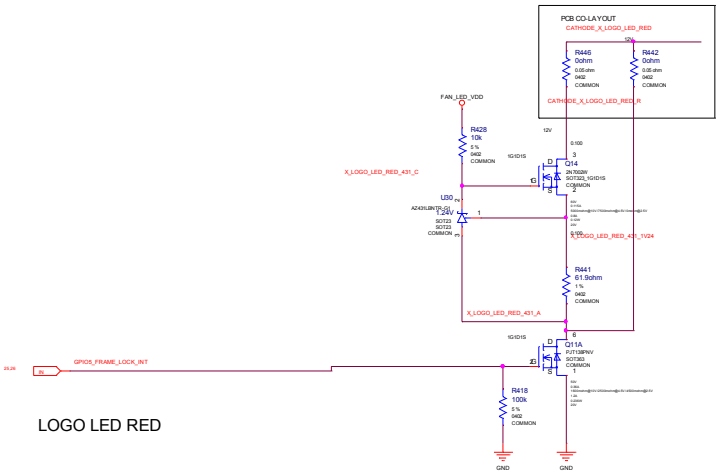
MISC: RGBW LED REF



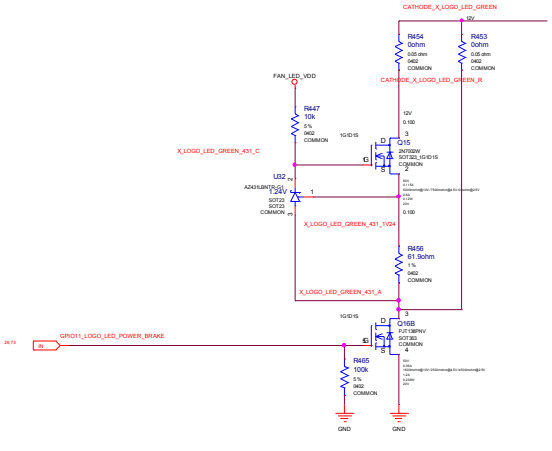
WHITE DRIVE

CONNECTOR SIZE TO FIT LAYOUT
ALL CIRCUIT NO STUFF BY DEFAULT
ALIGN WITH PASH
IF ADDTIONAL POWER CONSUPTION R NEEDED, IT SHOULD BE ON LED MOD.

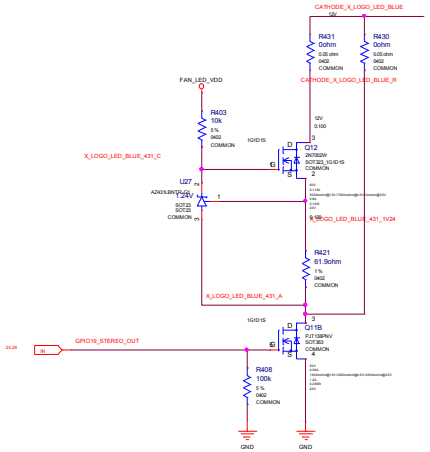


LOGO LED RED

RED DRIVE



GREEN DRIVE



BLUE DRIVE

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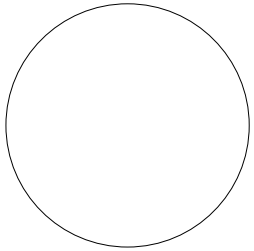
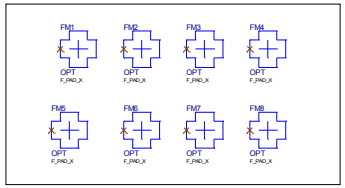
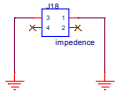
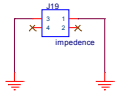
Mechanical: Mounting holes

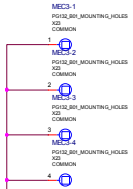
Remove CLP2 CLP3



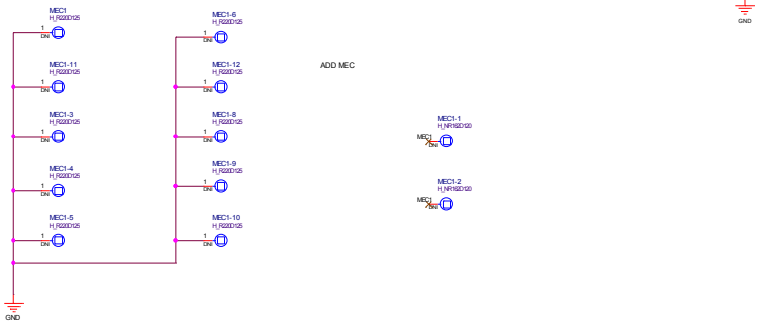








Remove MEC



ADD MEC

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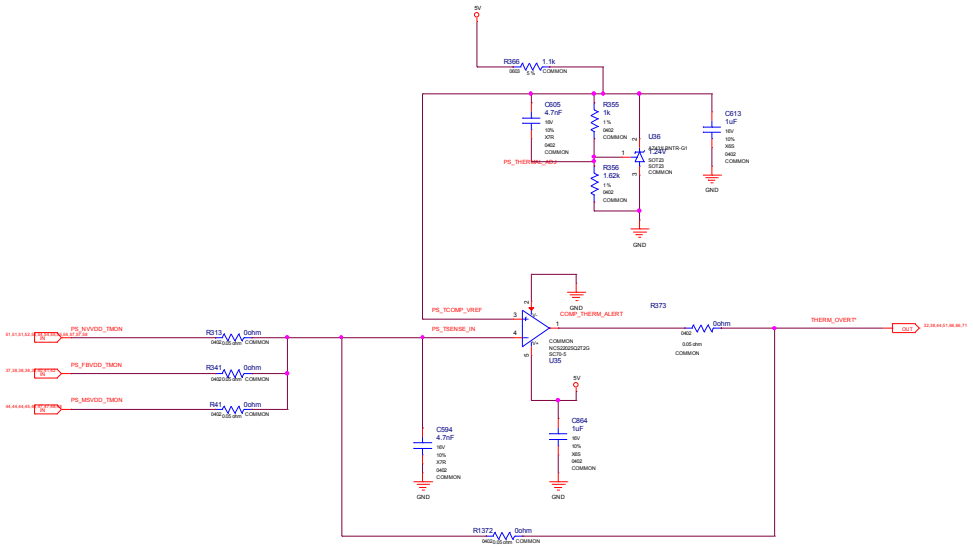
VR THERMAL PROTECTION



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PCI TERM

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