PG132-A02

370W, FH Std PCB, 384b, GDDR6x 2CH X16
DP + DP + DP + HDMI/DP

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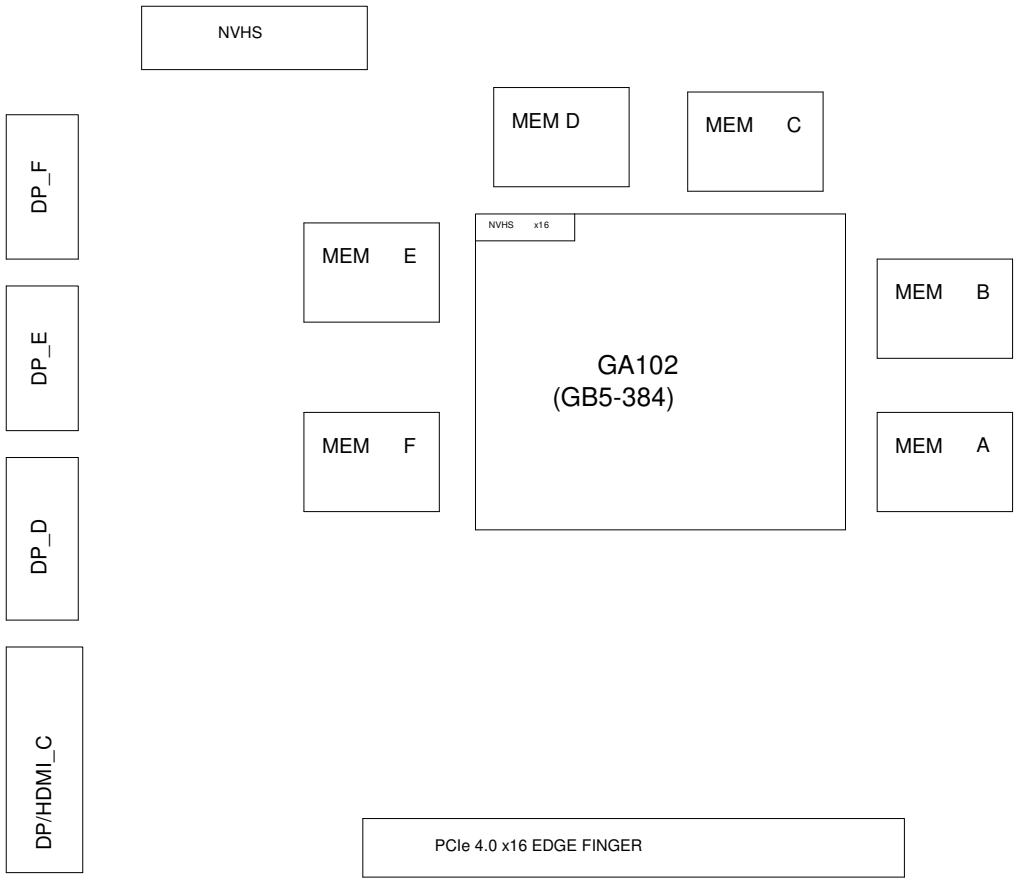
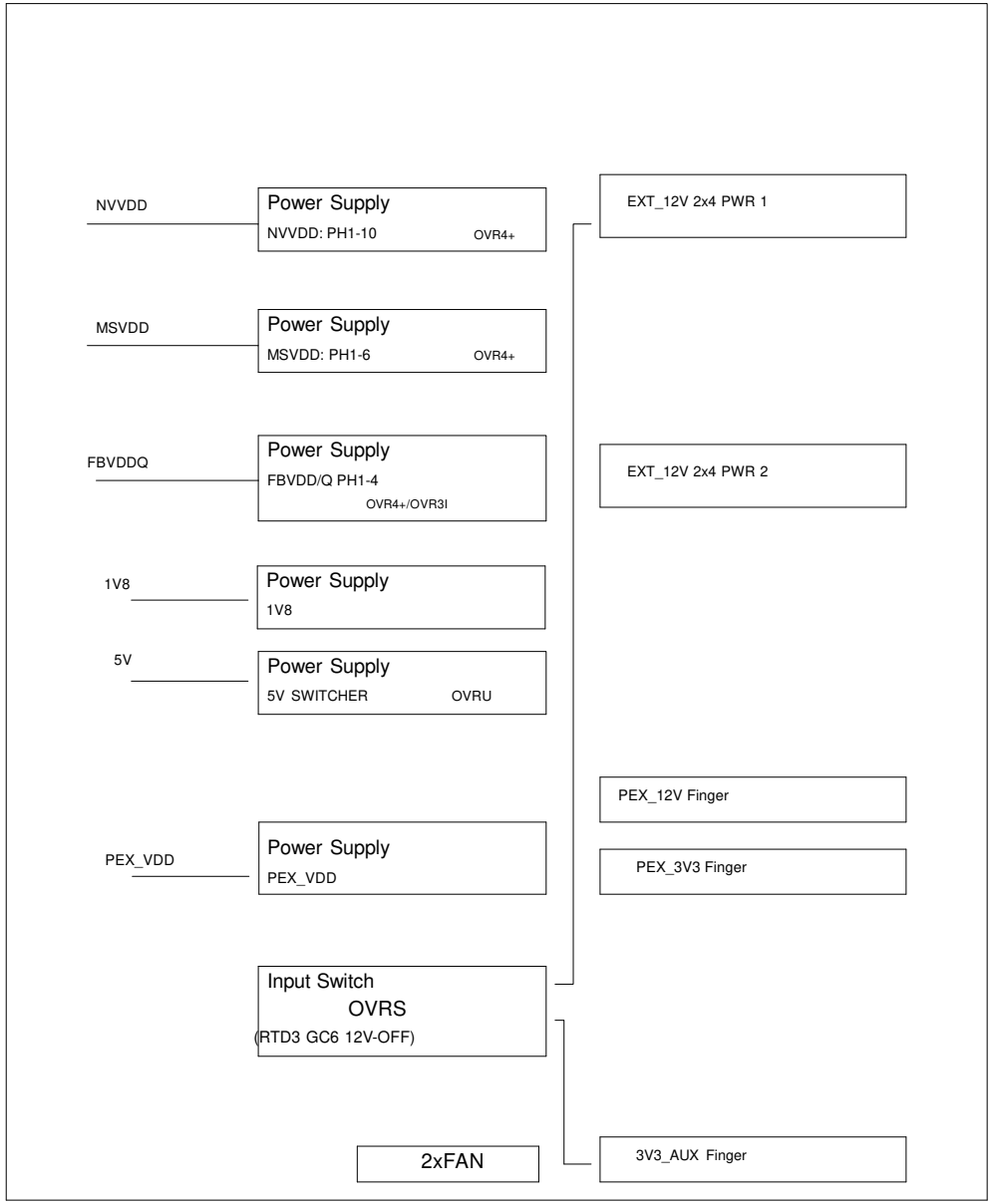
Block Diagram





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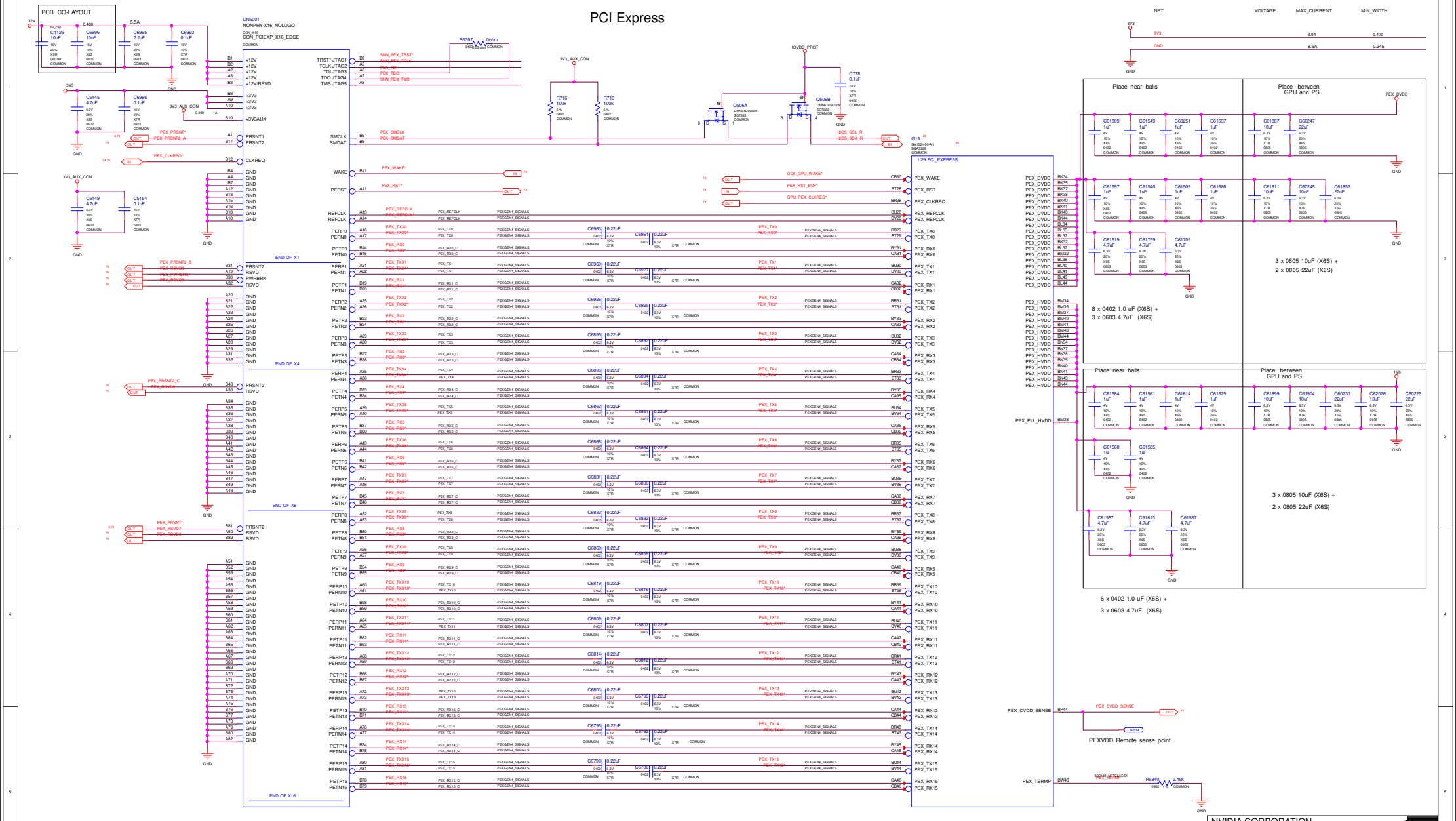

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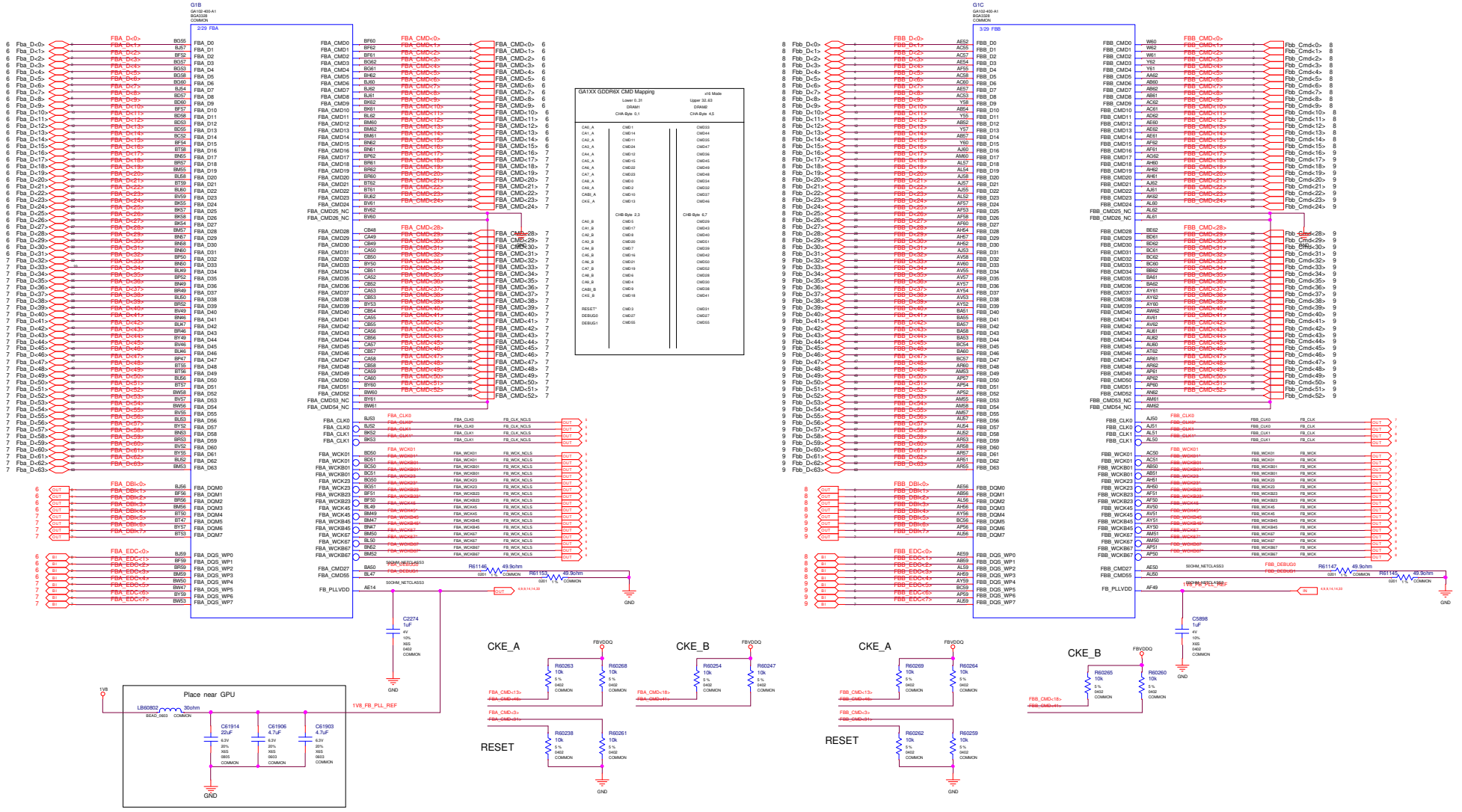
MEMORY: GPU Partition A/B



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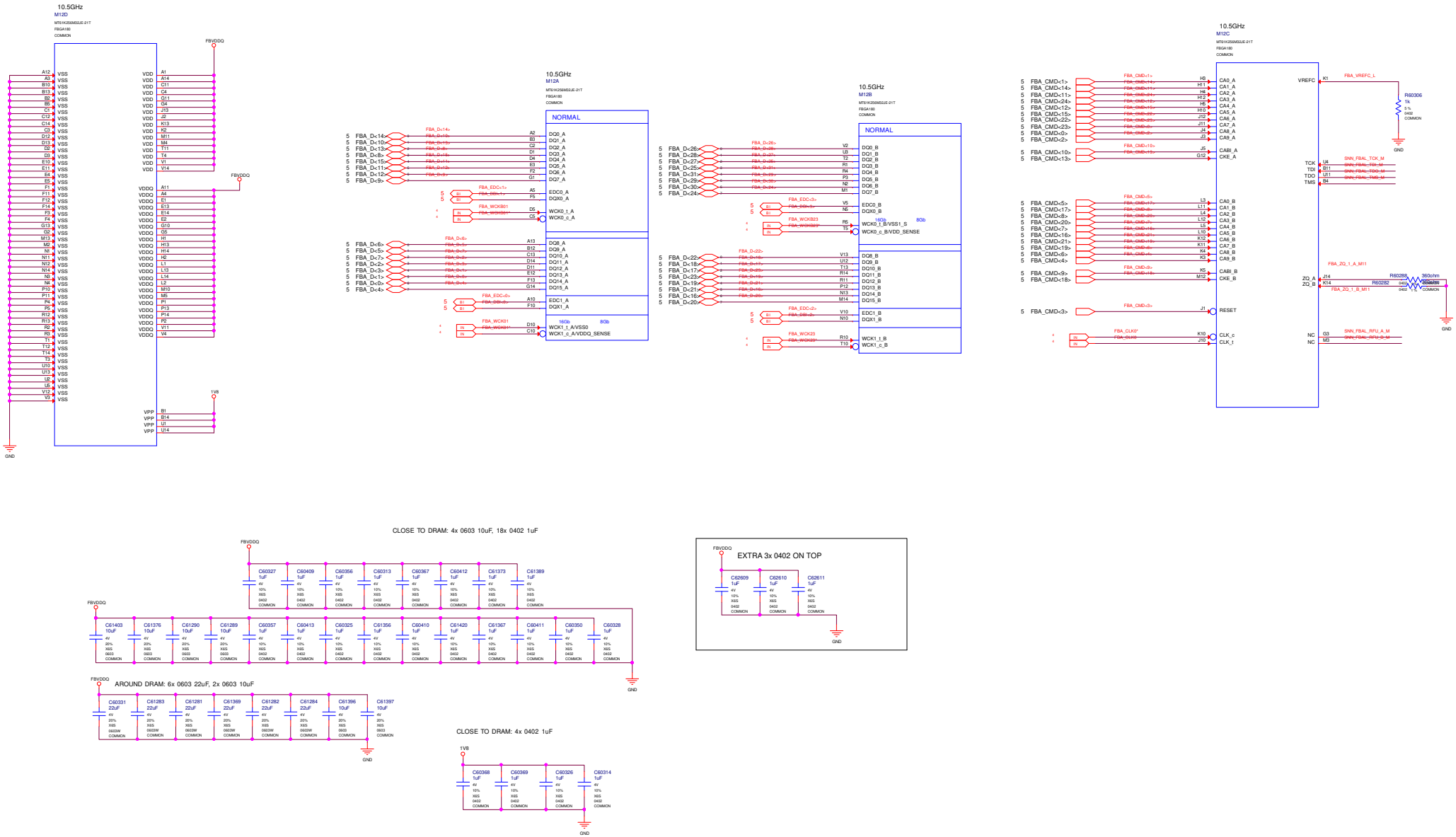

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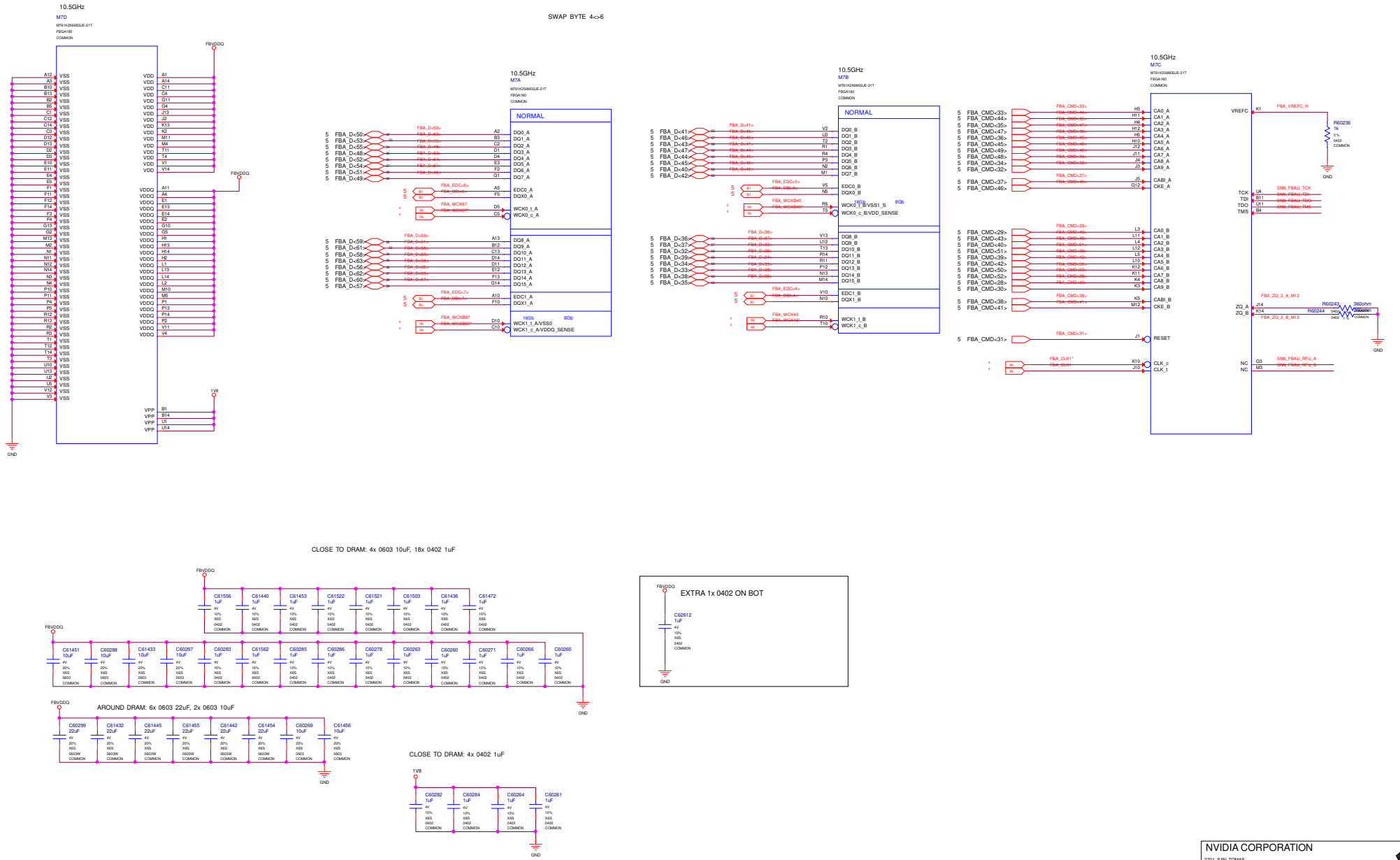
MEMORY: FBA Partition 63..32



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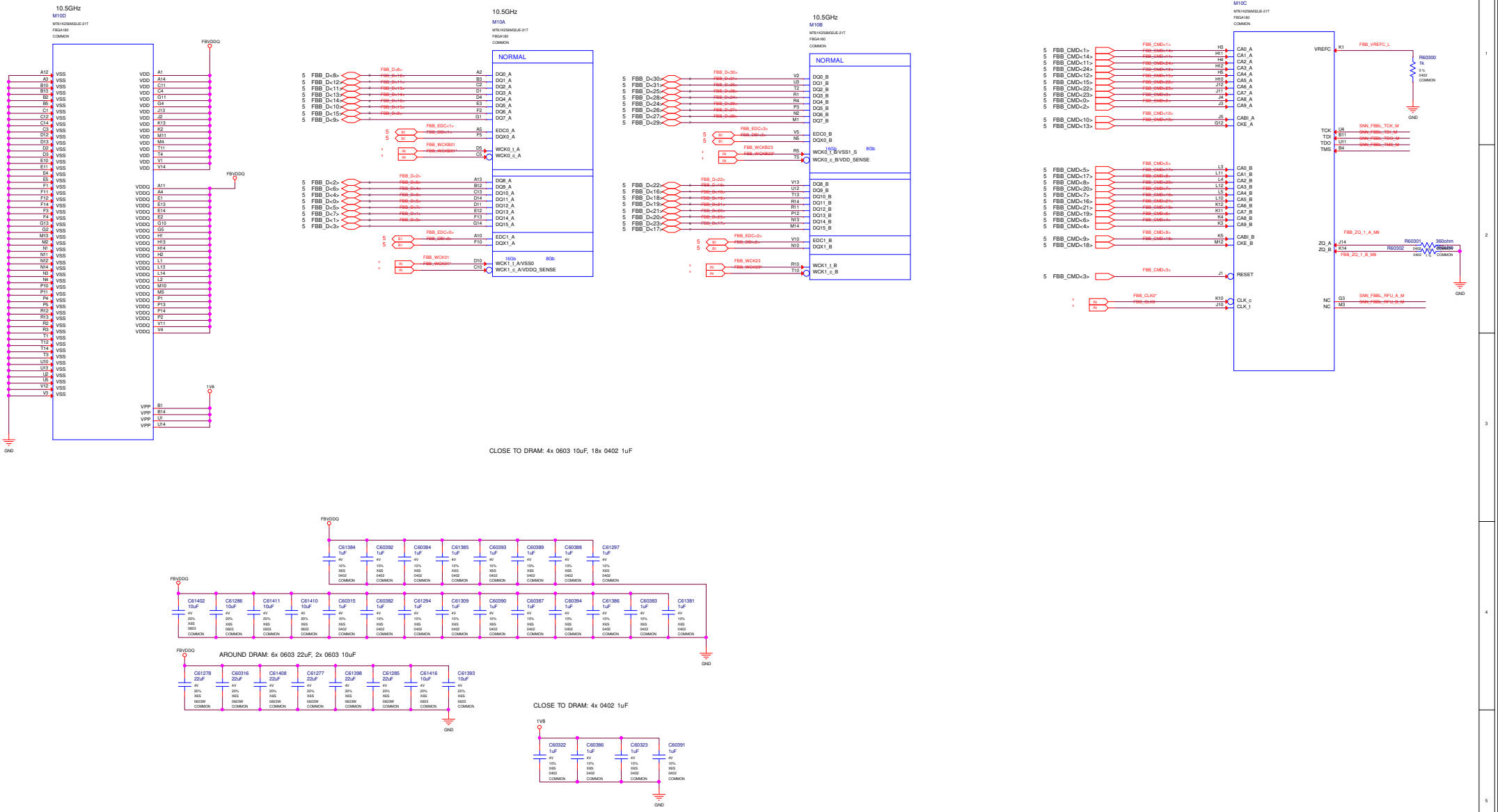
MEMORY: FBB Partition 31..0



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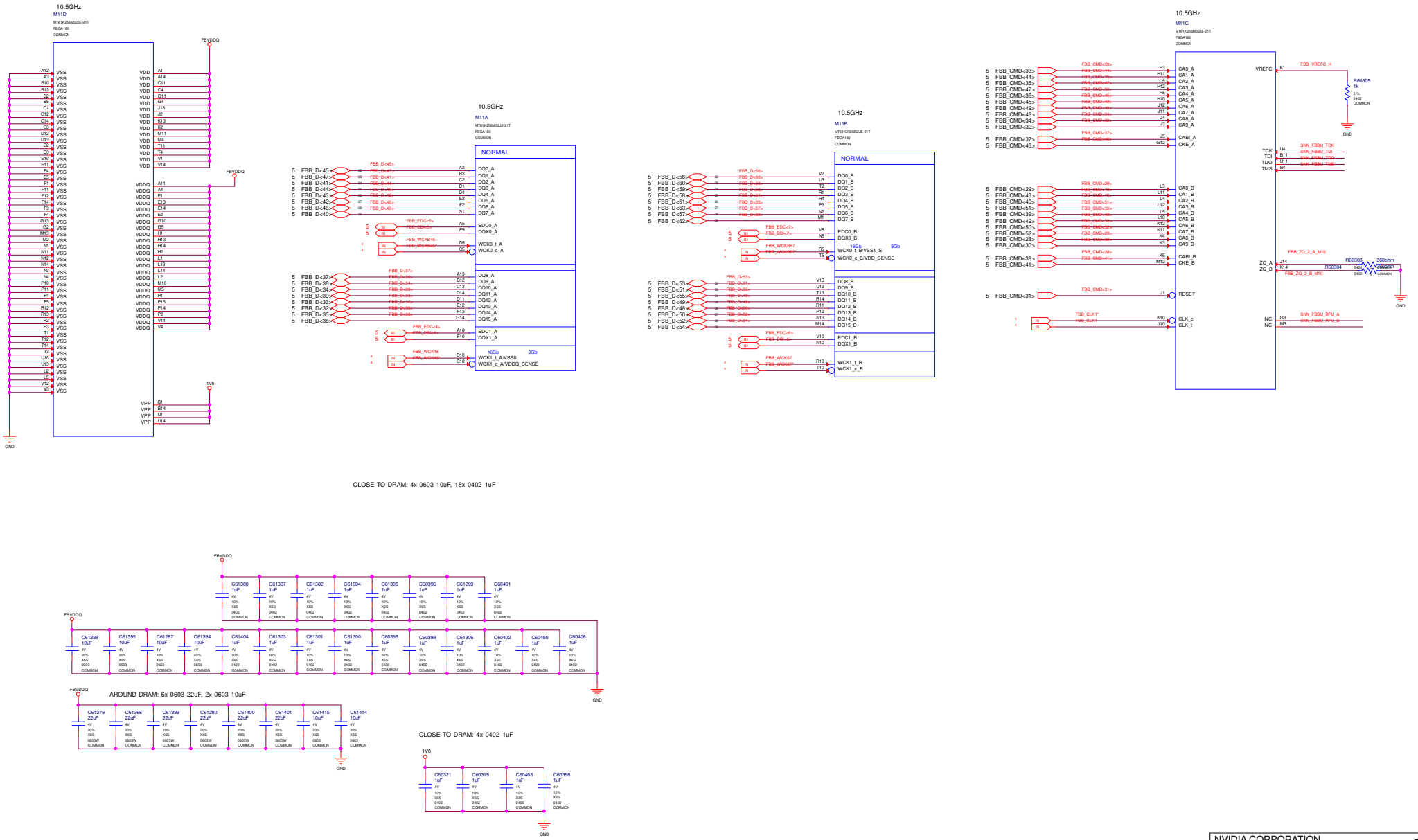
MEMORY: FBB Partition 63..32



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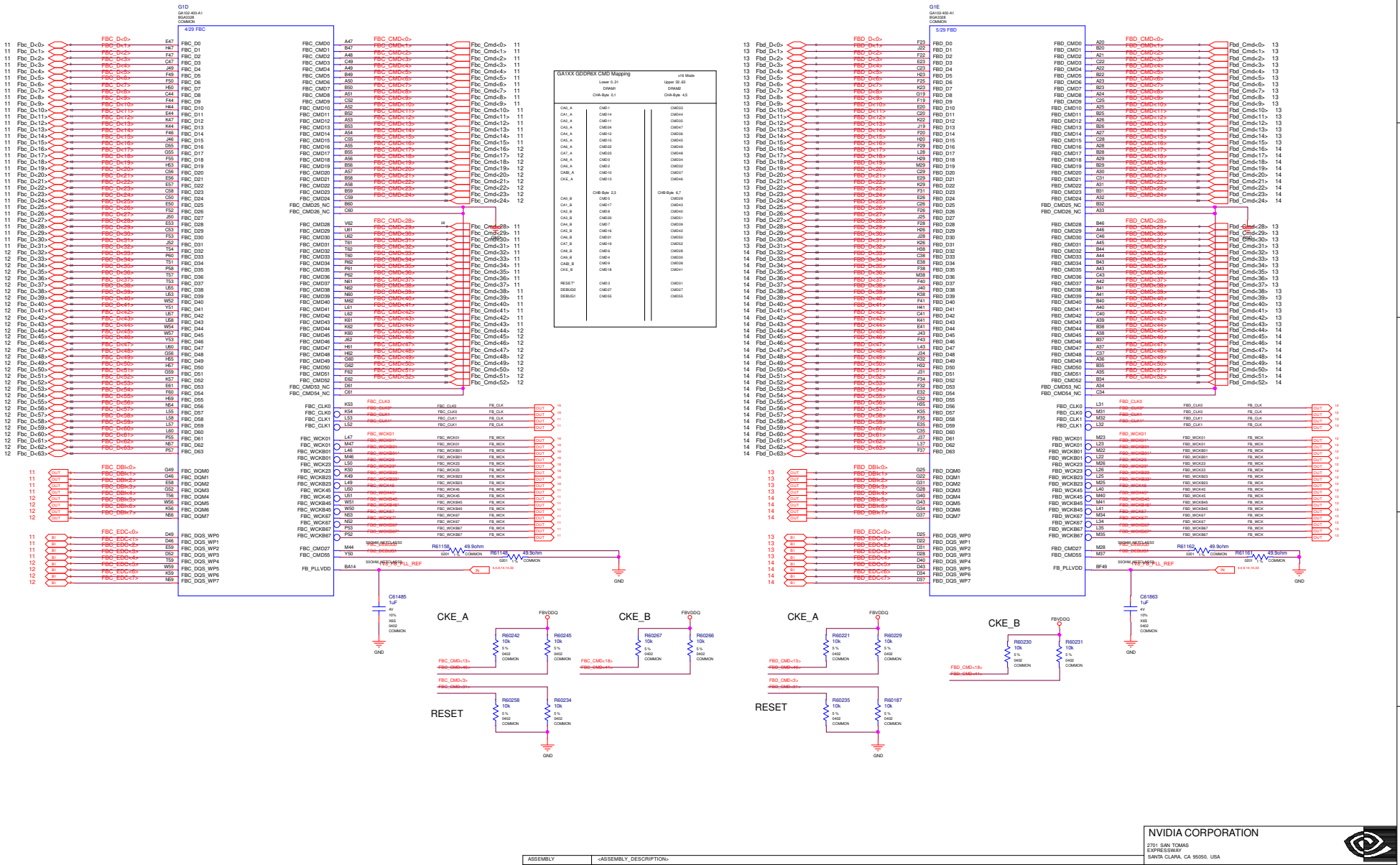
MEMORY: GPU Partition C/D



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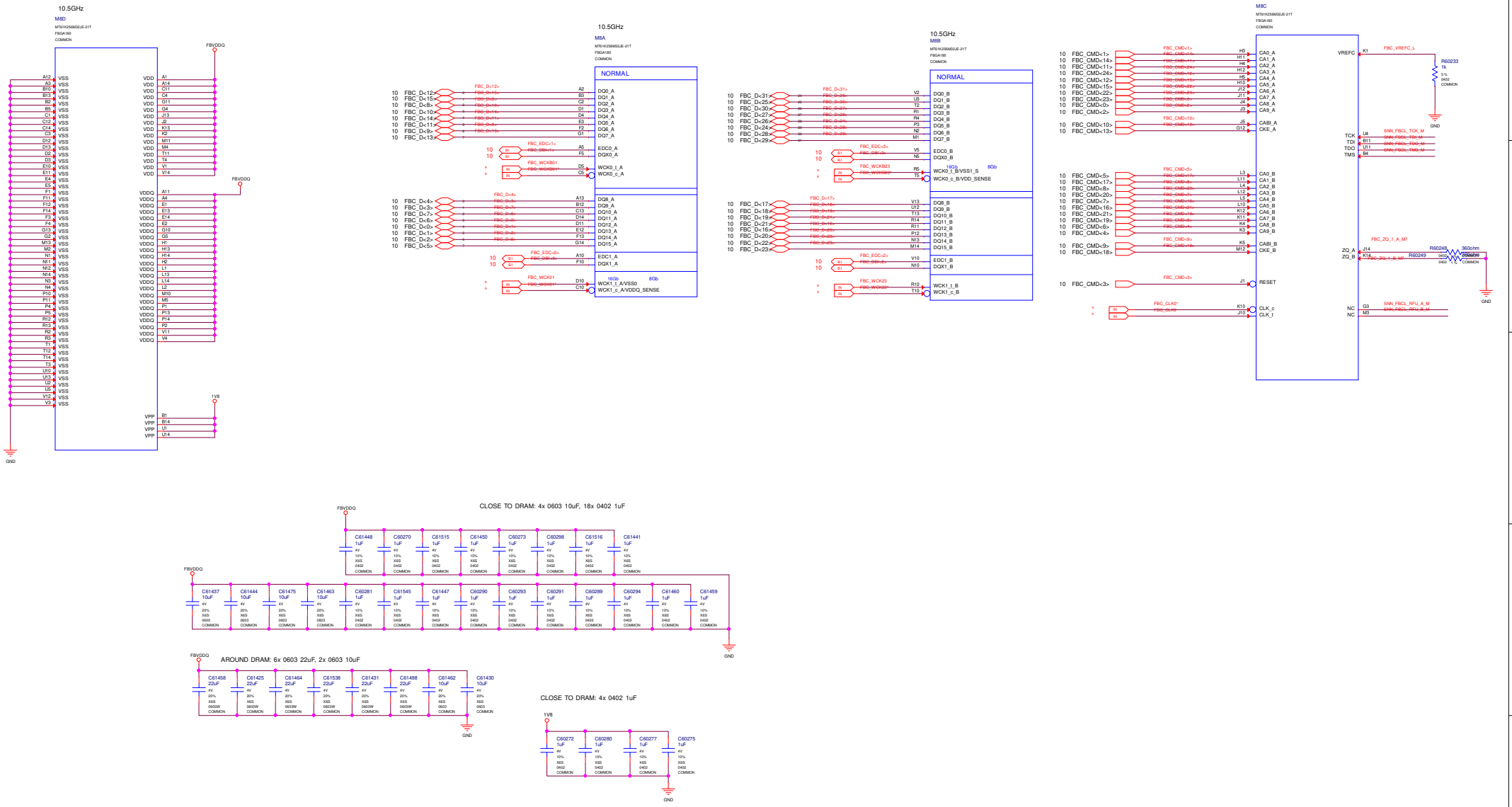

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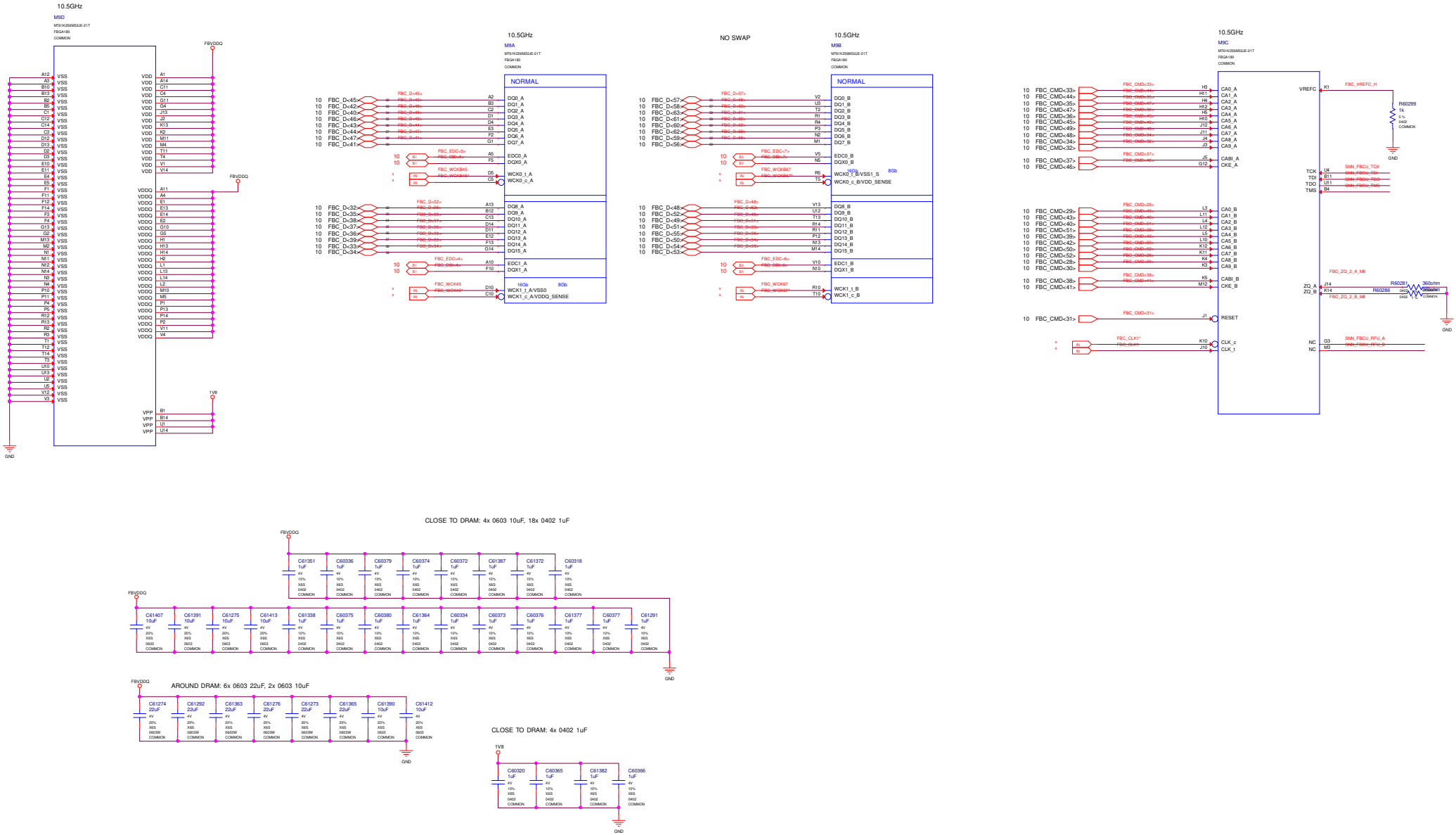
MEMORY: FBC Partition 63..32



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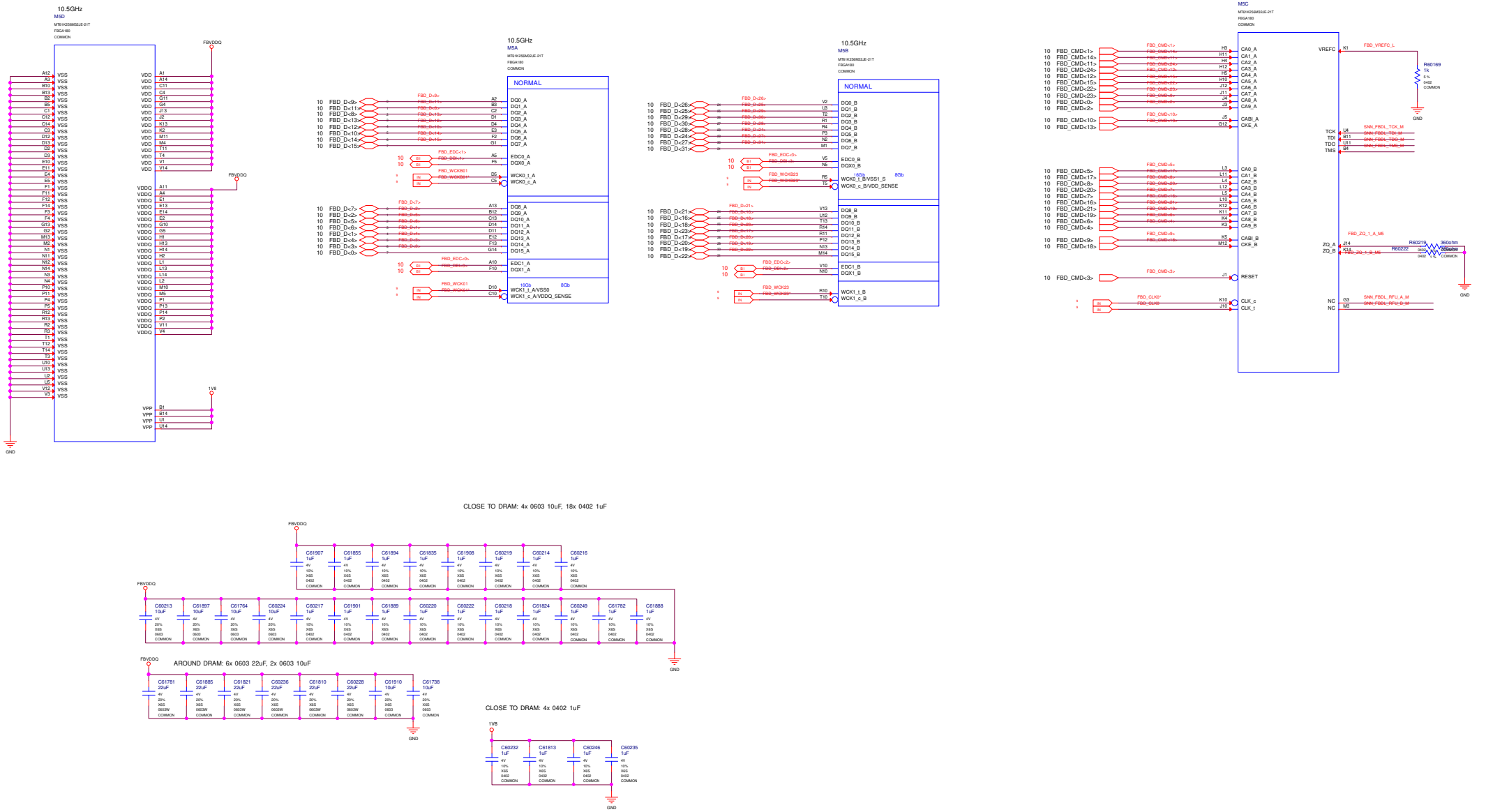
MEMORY: FBD Partition 31..0



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AROUND DRAM: 6x 0603 22uF, 2x 0603 10uF

CLOSE TO DRAM: 4x 0402 1uF

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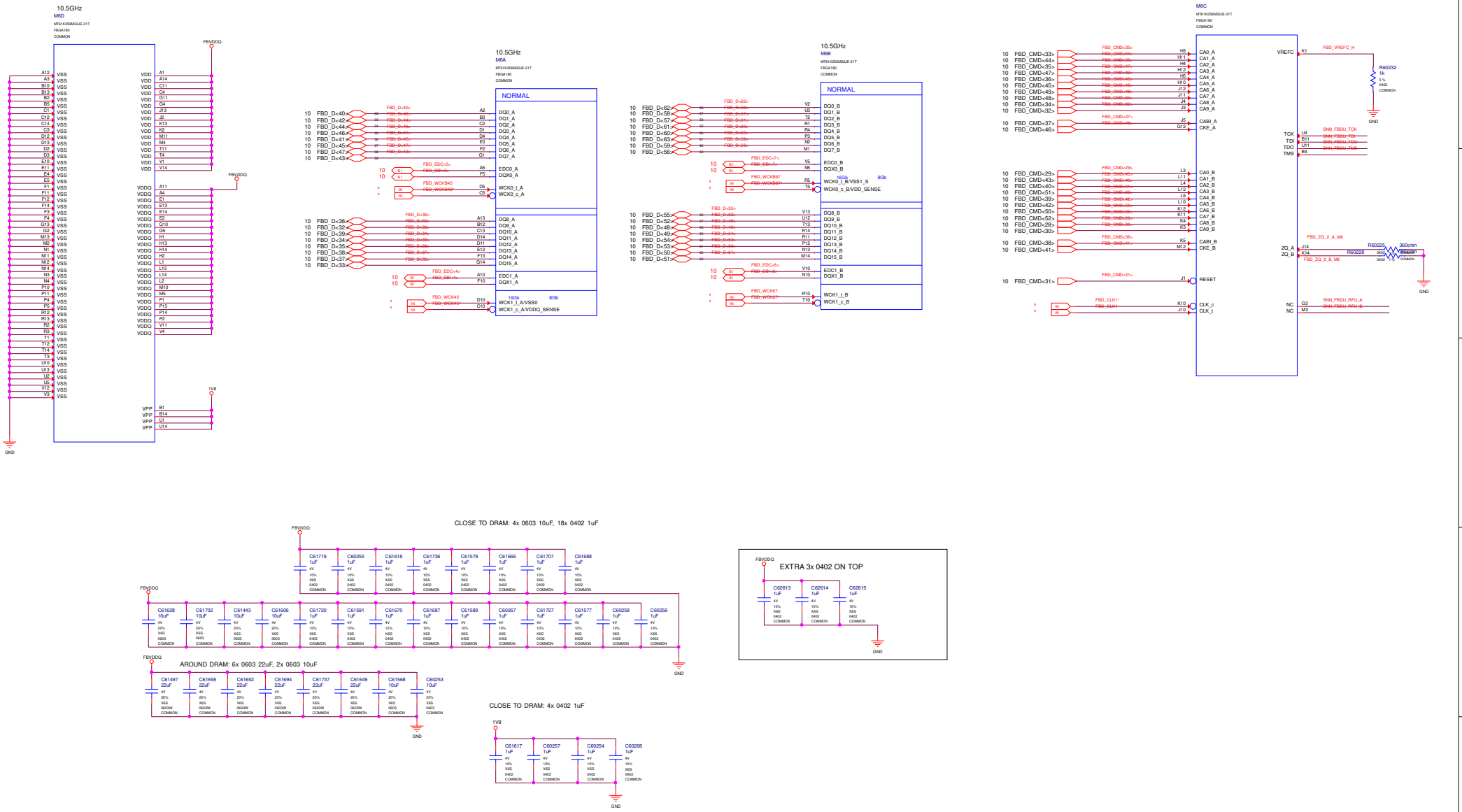

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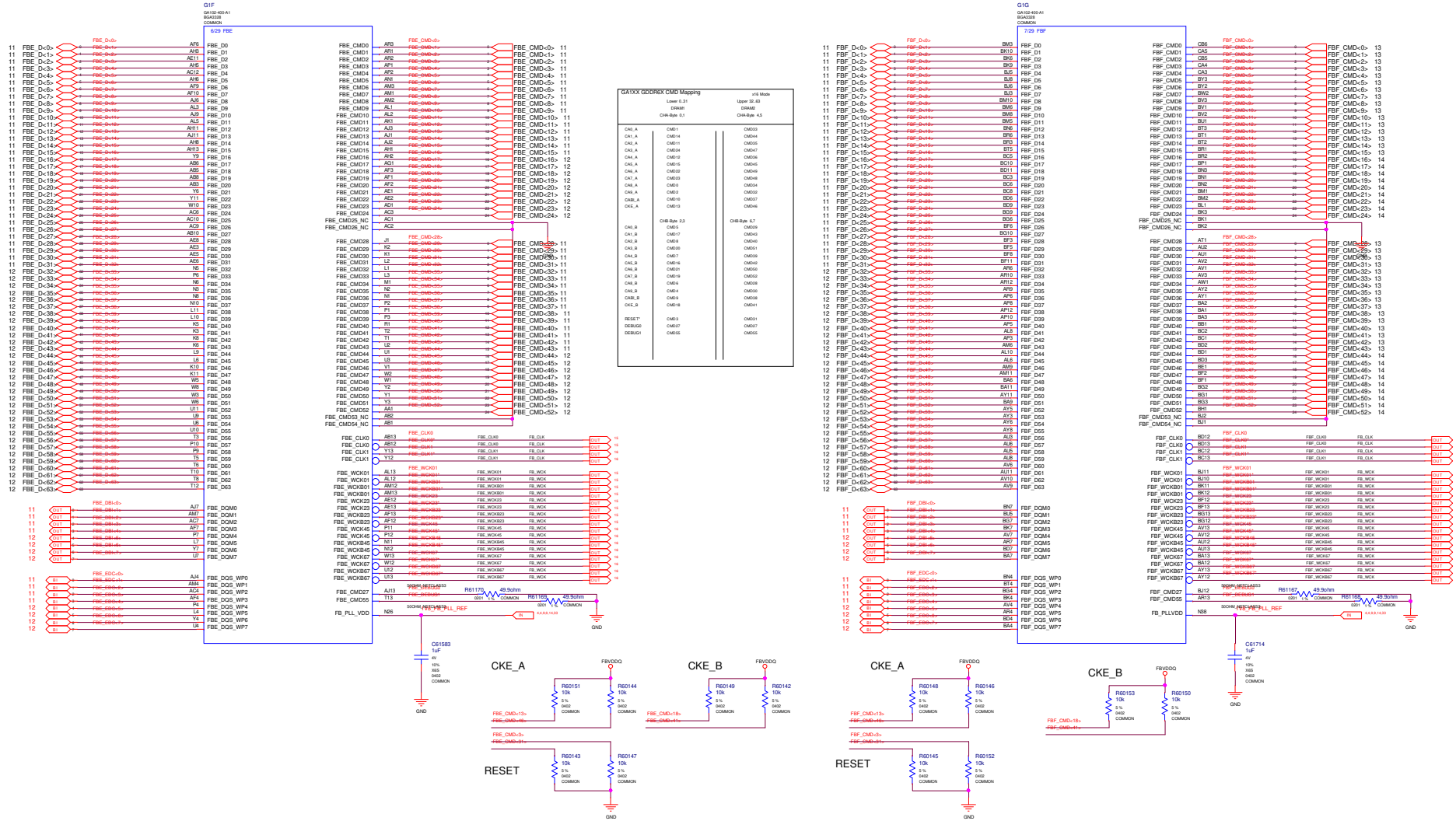
MEMORY: GPU Partition E/F



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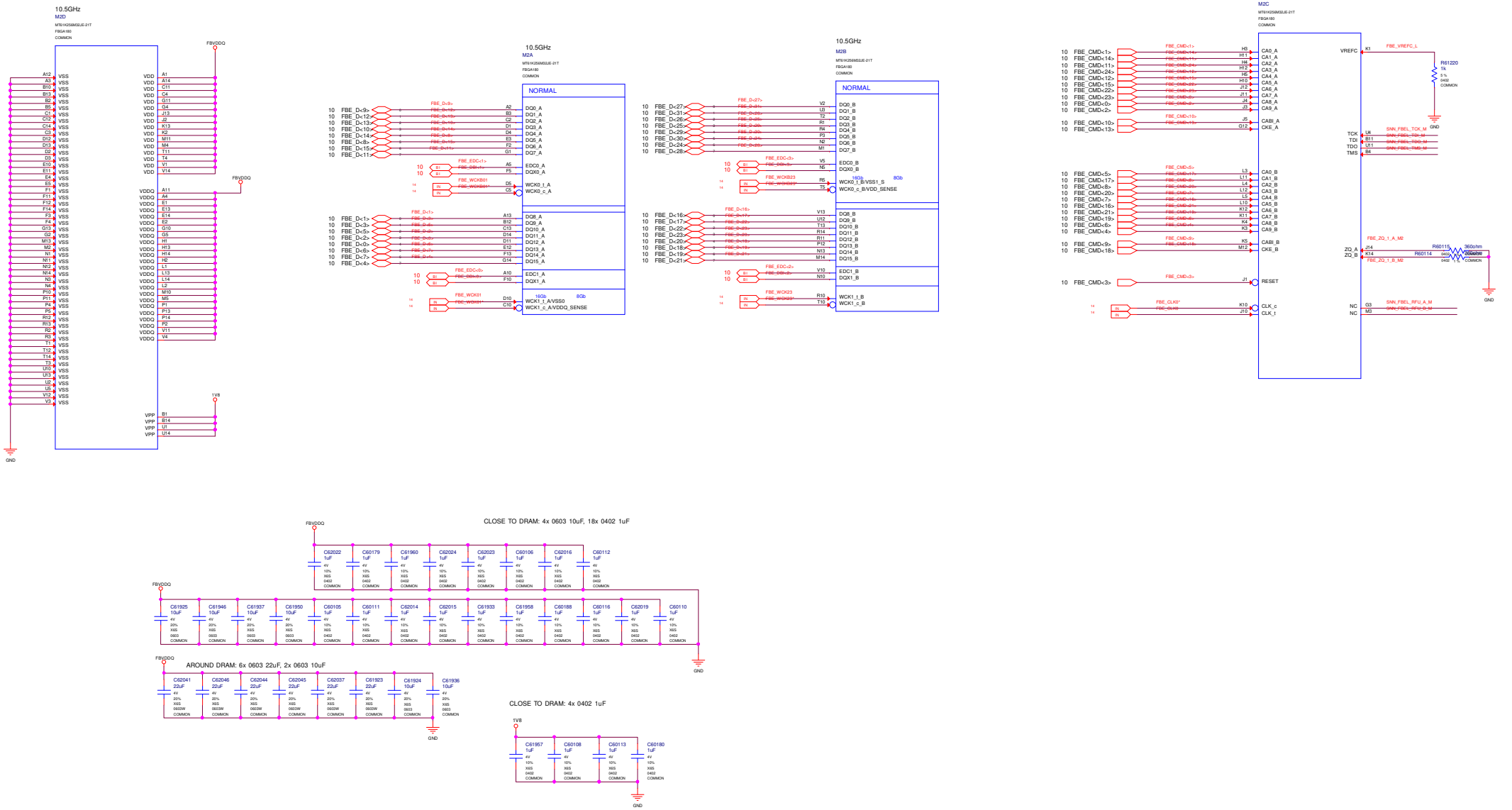
MEMORY: FBE Partition 31..0



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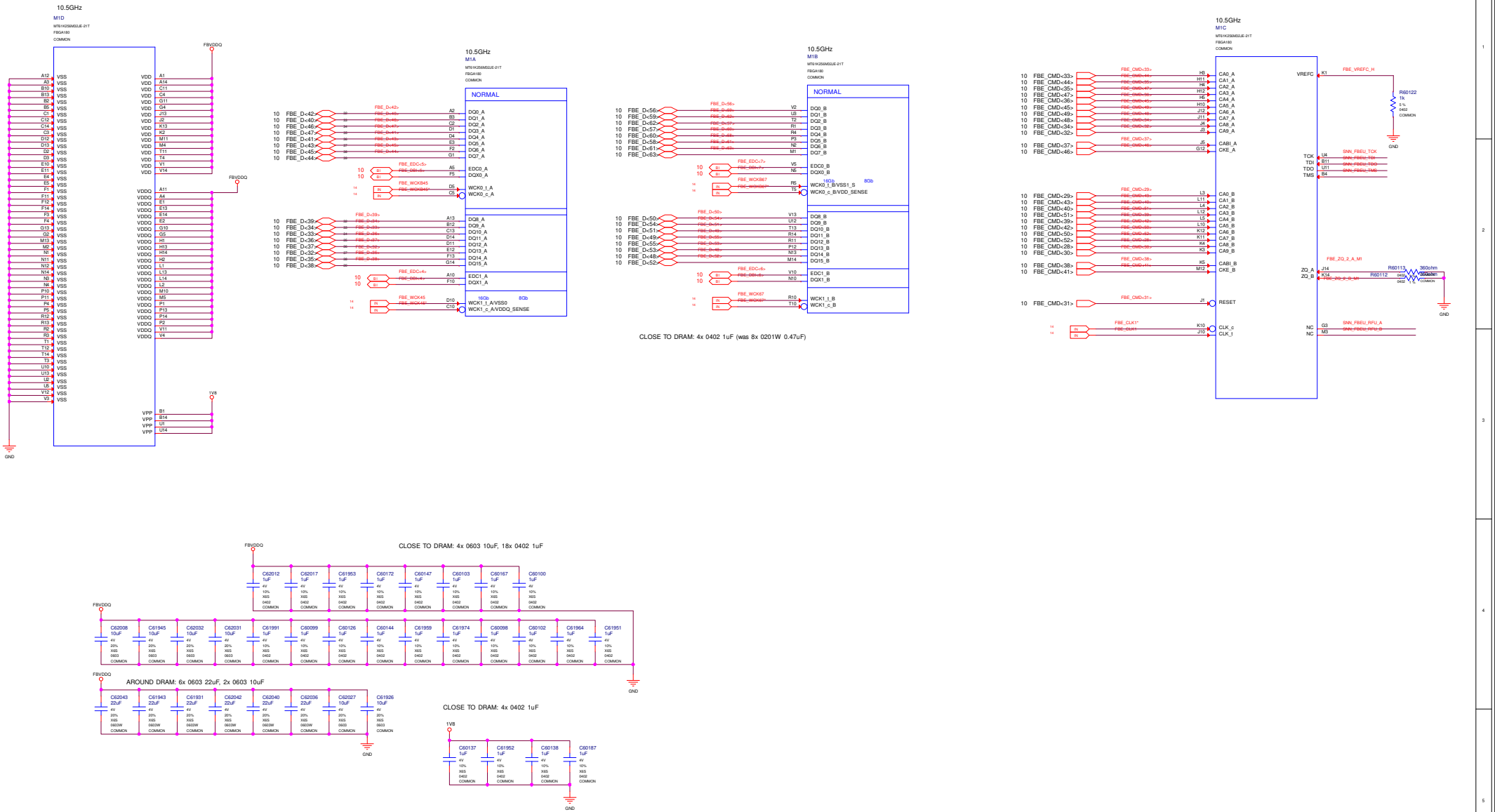
MEMORY: FBE Partition 63..32



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE_DETAIL	MEMORY: FBE PARTITION[63:32]

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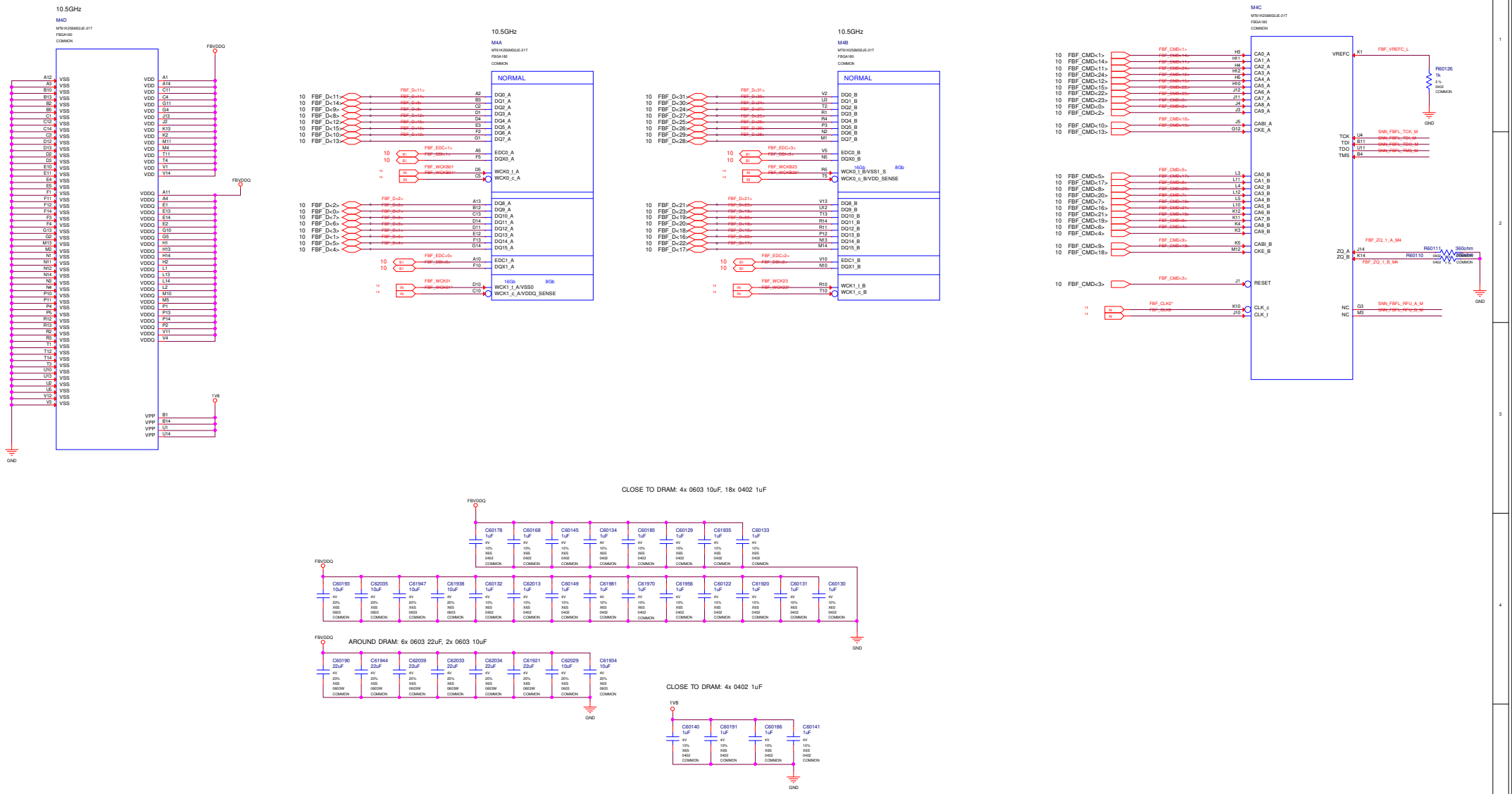
BOM REV	A	DATE	10-JUN-2020

MEMORY: FBF Partition 31..0



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PAGE_DETAIL	MEMORY: FBF PARTITION[31:0]

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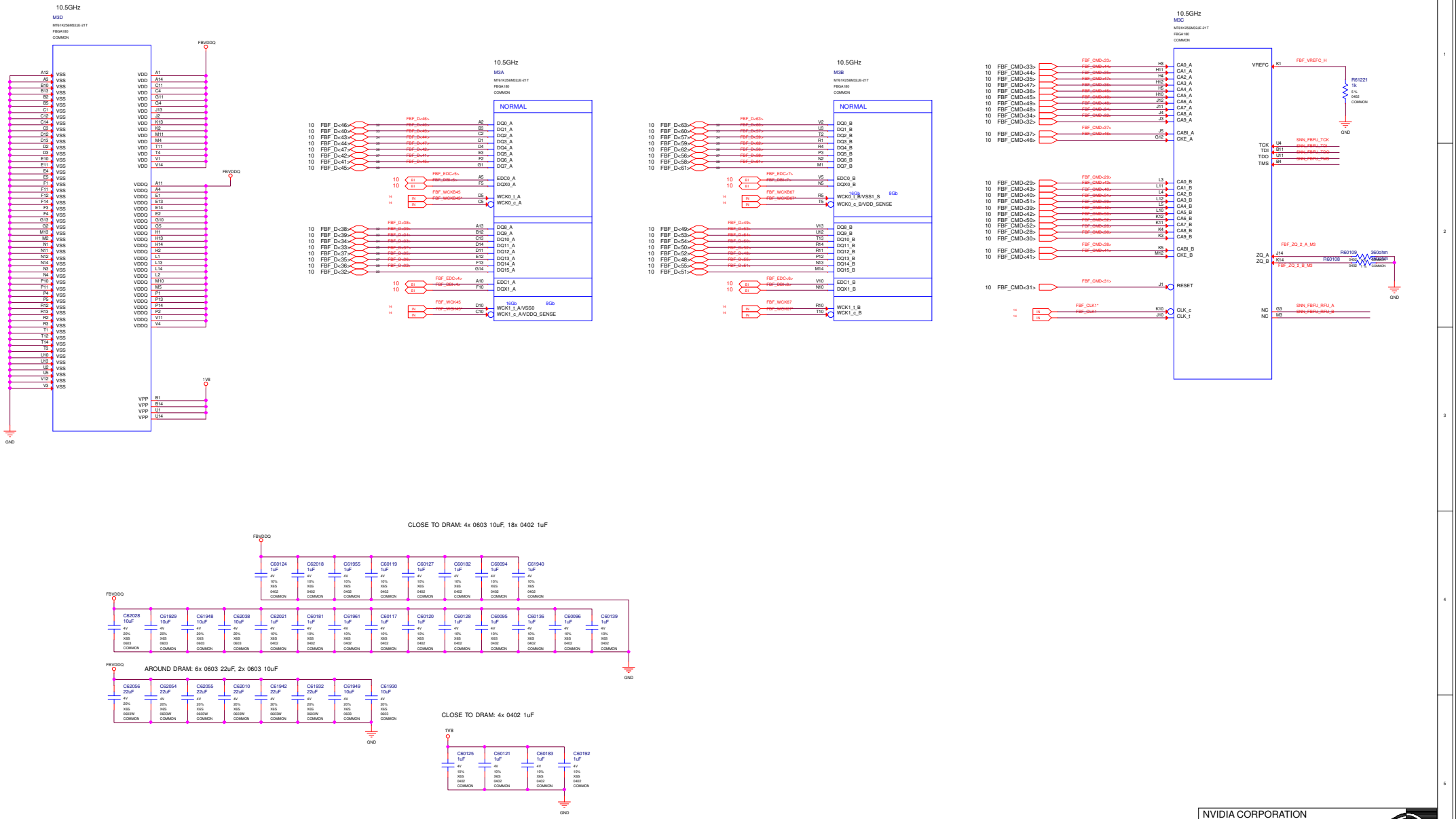
MEMORY: FBF Partition 63..32



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PAGE_DETAIL	MEMORY: FBF PARTITION[63:32]

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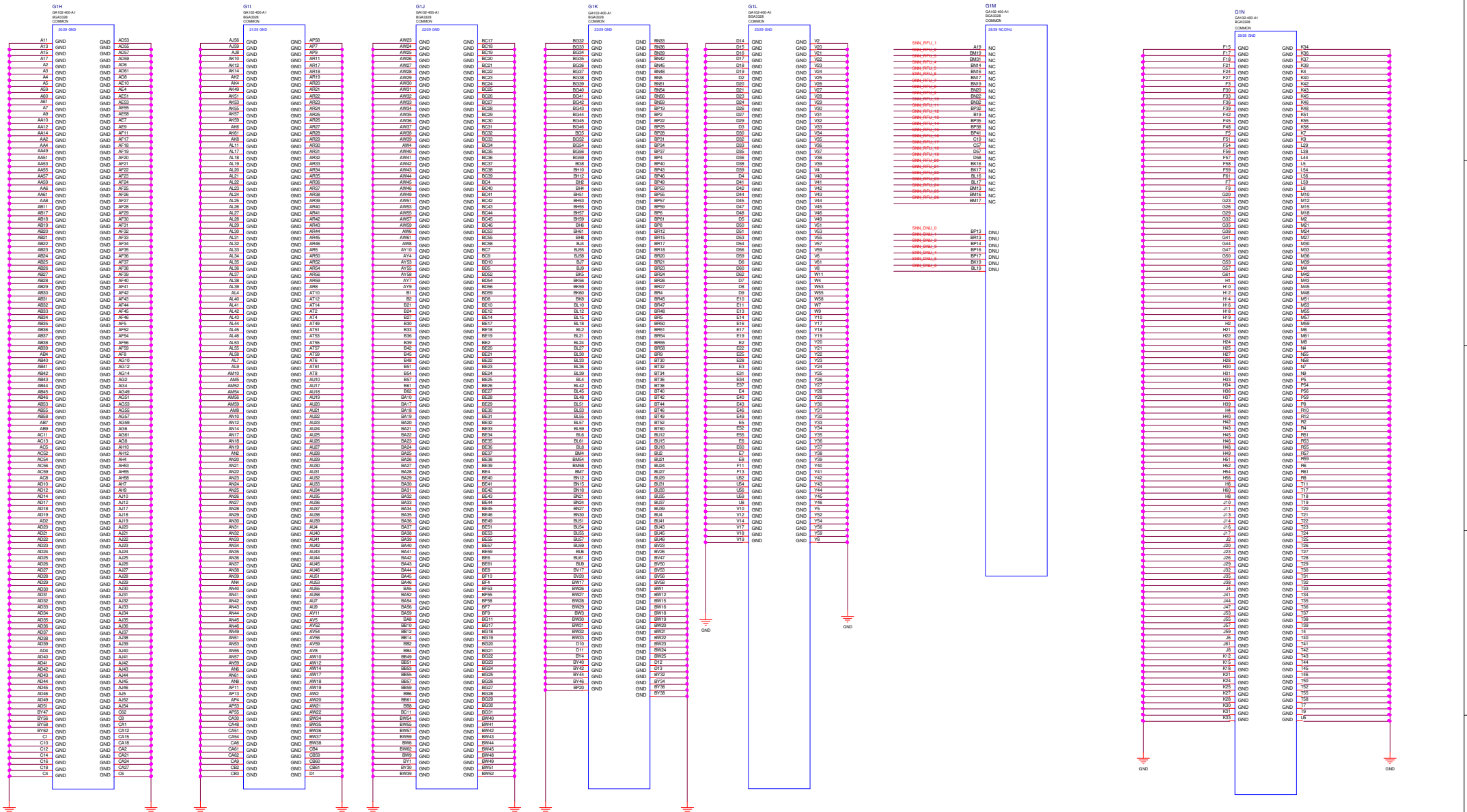
GPU GND, RFUs & RSVD



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU GND, RFUs & RSVD

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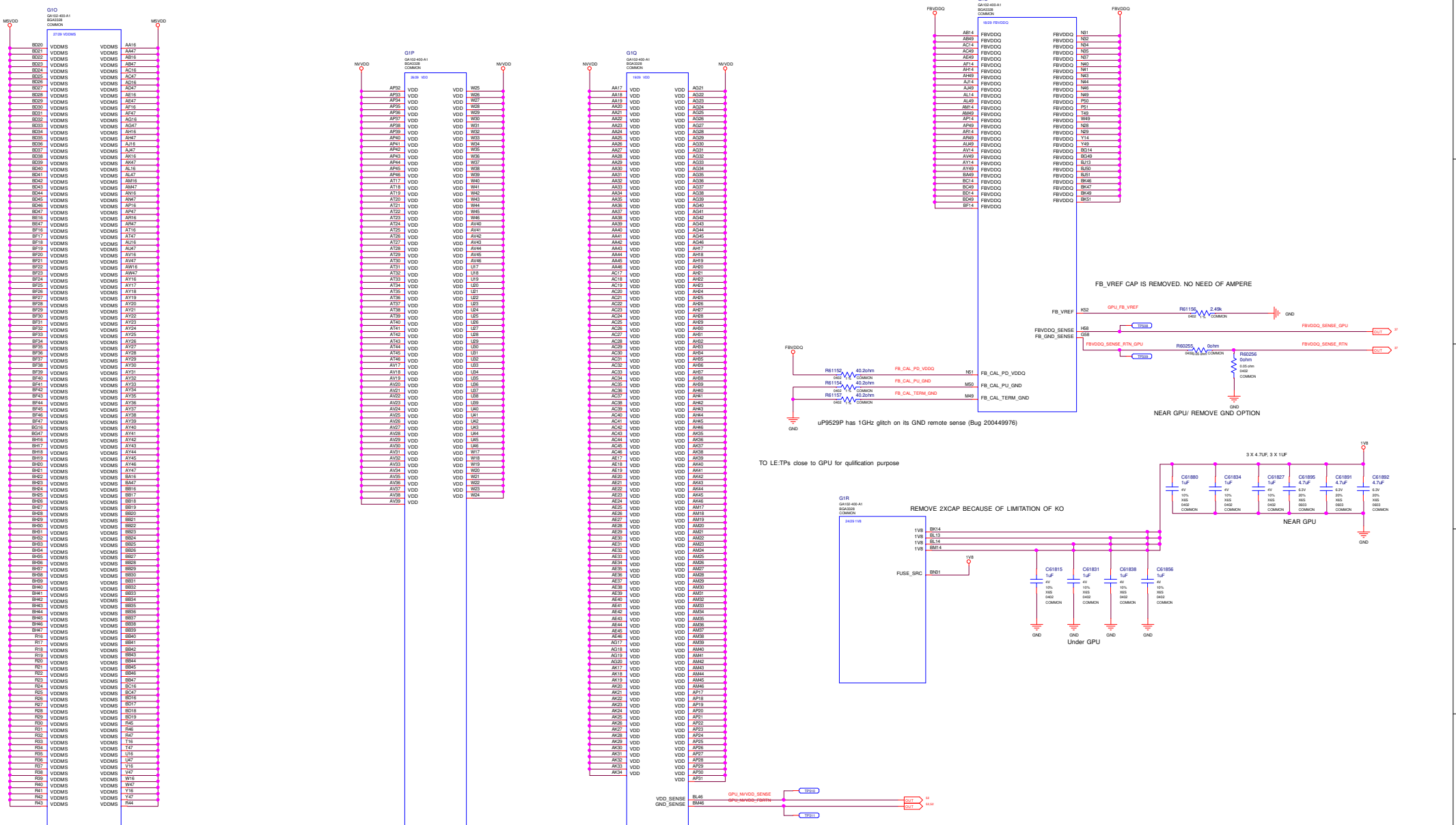
GPU PWR and GND



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE_DETAIL	GPU POWERS

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NVVDD

UNDER GPU

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING NVVDD

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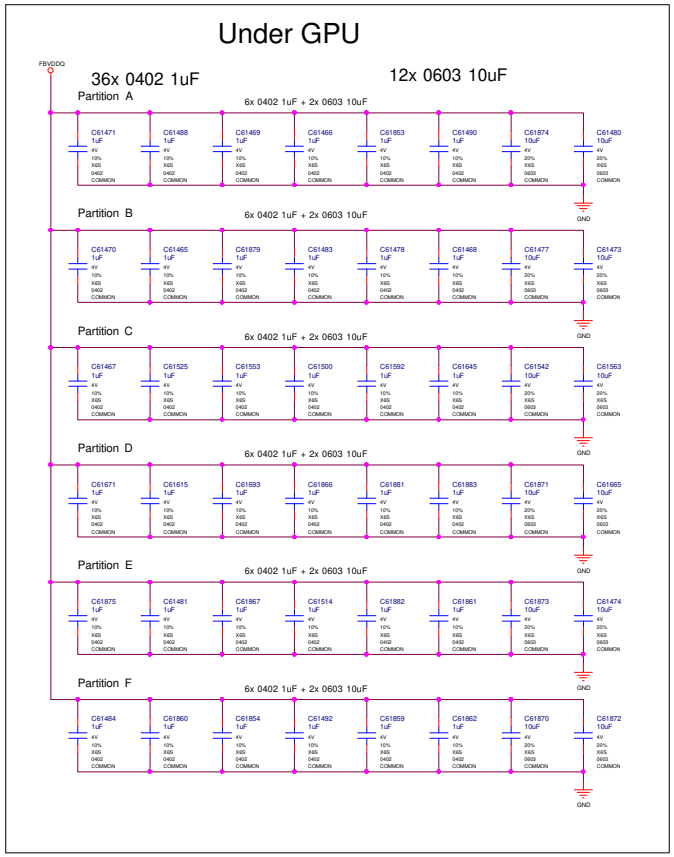
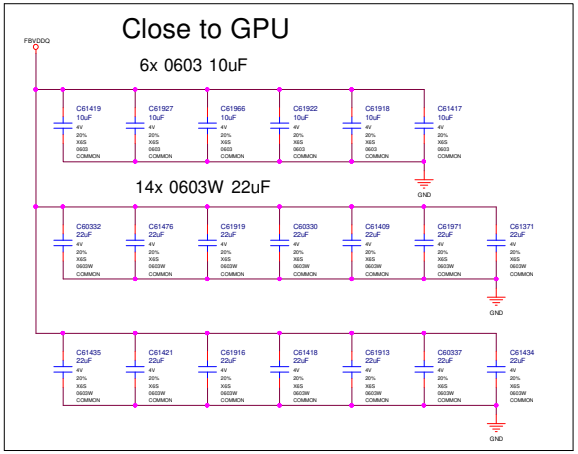
FBVDDQ





ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE_DETAIL	GPU DECOUPLING FBVDDQ

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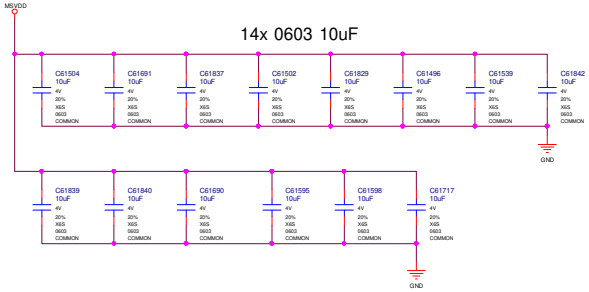
Page 23: GPU: MSVDD DECOUPLING

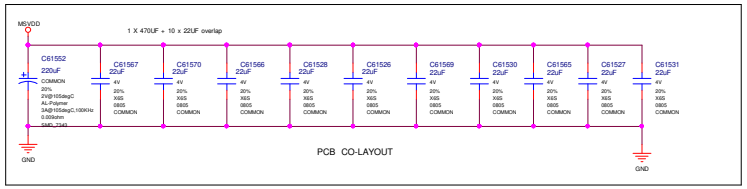
UNDER GPU

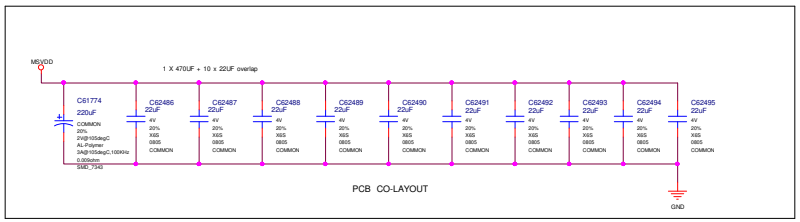
MSVDD

14x 0603 10uF

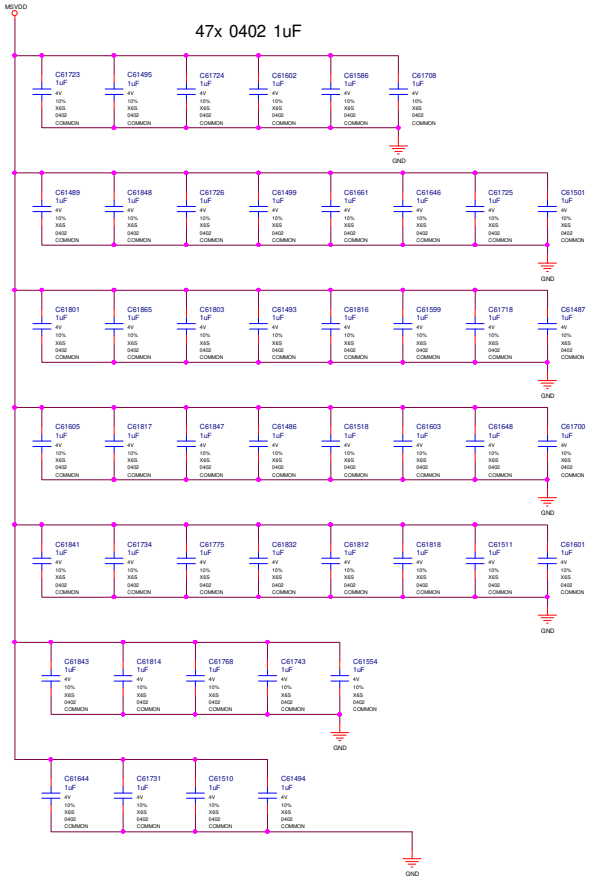


2x SMD7343 220uF (EACH CO-LAYOUT WITH 10x 22uF 0805)





47x 0402 1uF



REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	GPU DECOUPLING MSVDD

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE_DETAIL	BLANK

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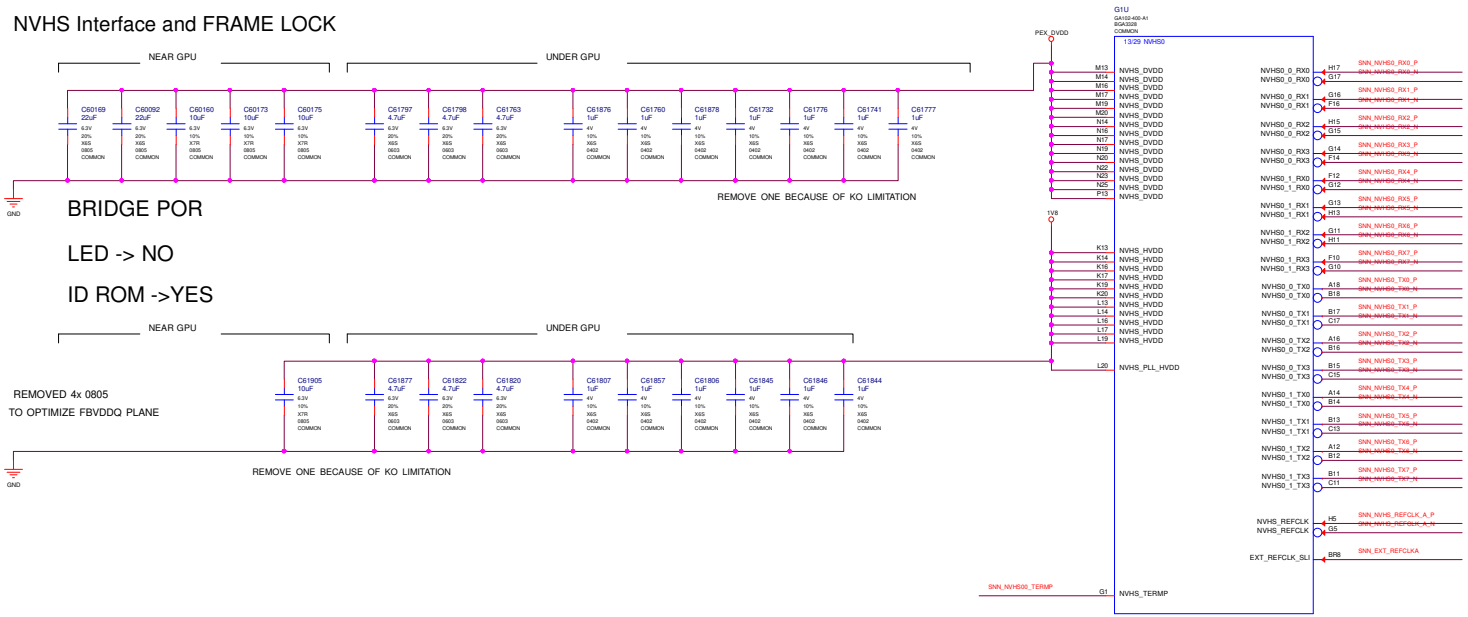
NVHS Interface and FRAME LOCK



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PAGE DETAIL	NVHS x16

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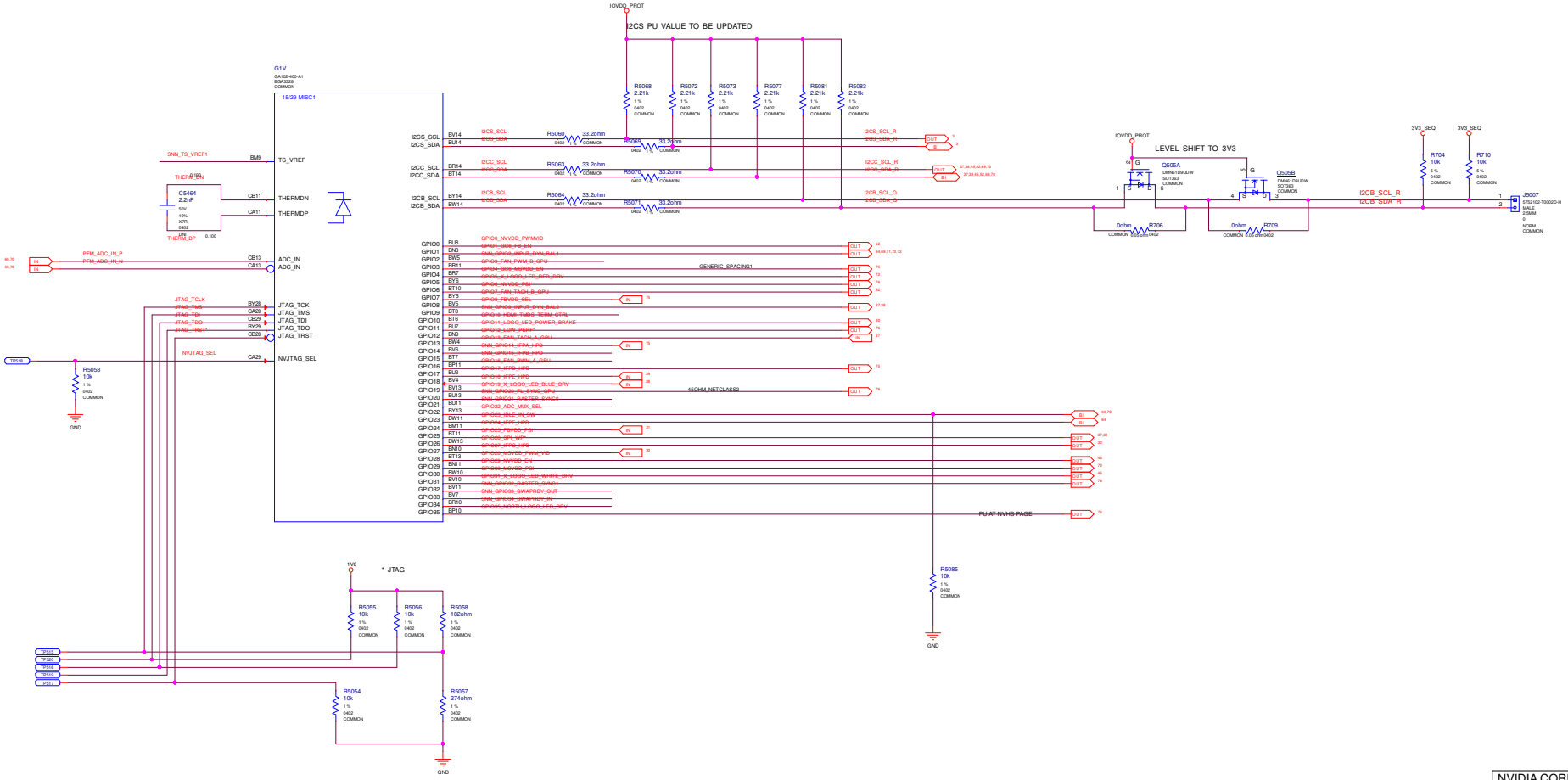
MISC1: Fan, Thermal, JTAG, GPIO, STEREO



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE_DETAIL	MISC: THERMAL, JTAG, GPIO

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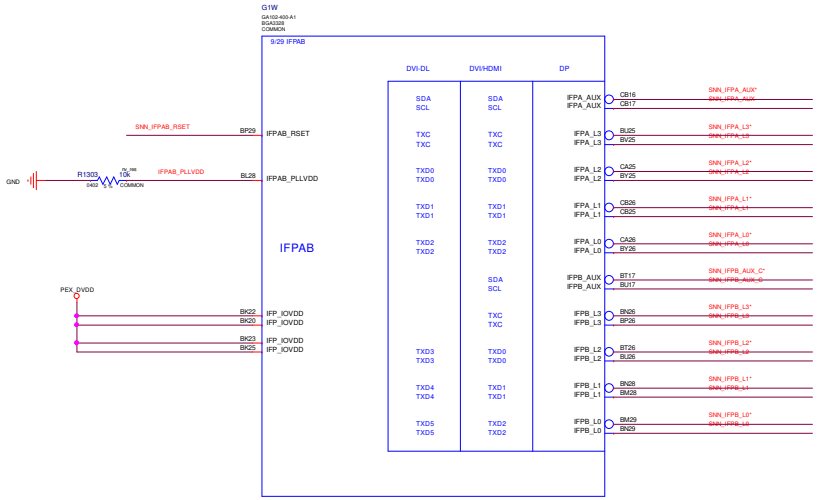
IFPA UNUSED, IFPB UNUSED



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE_DETAIL	IFPA UNUSED, IFPB UNUSED

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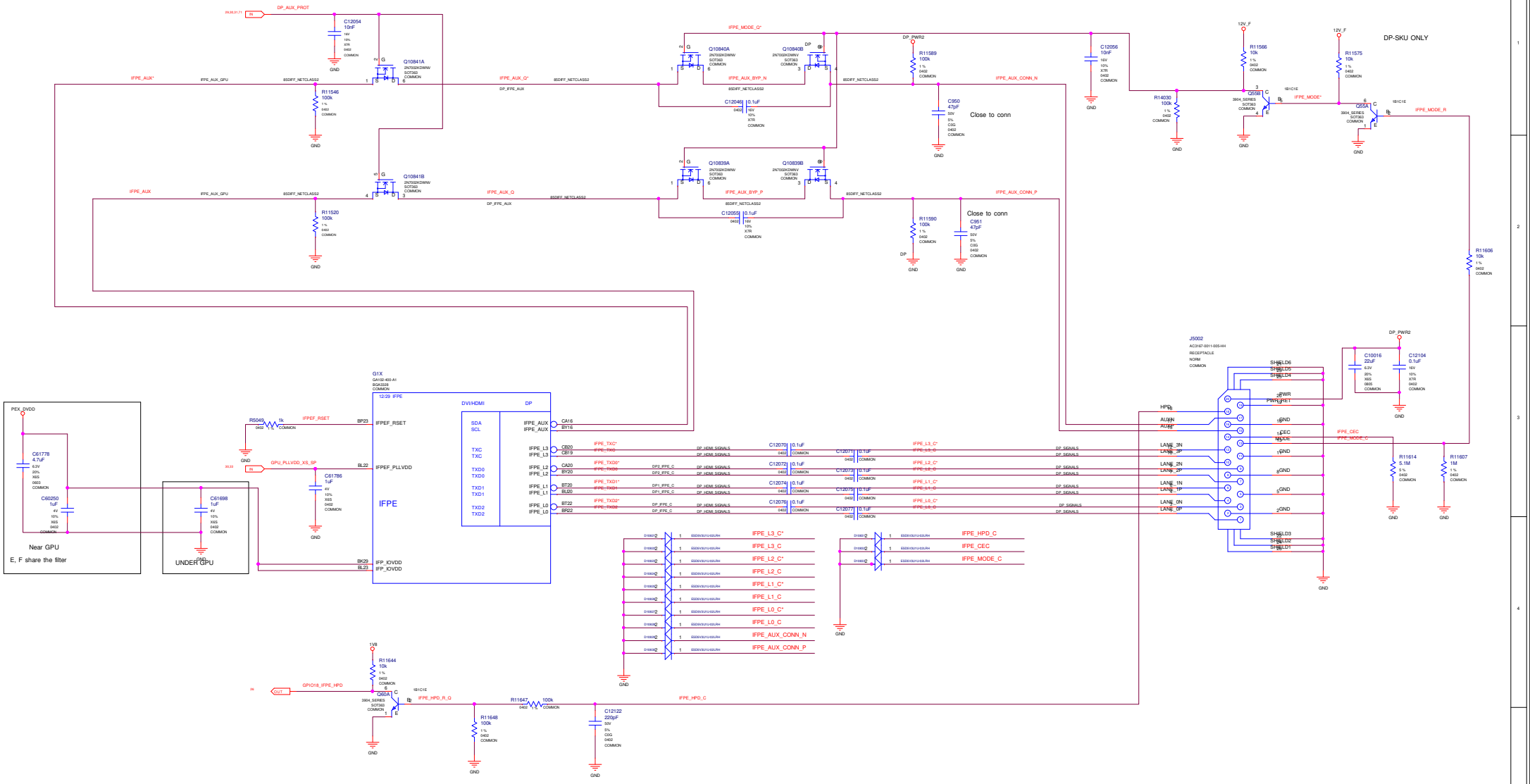
IFPE DP



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	IFPE DP

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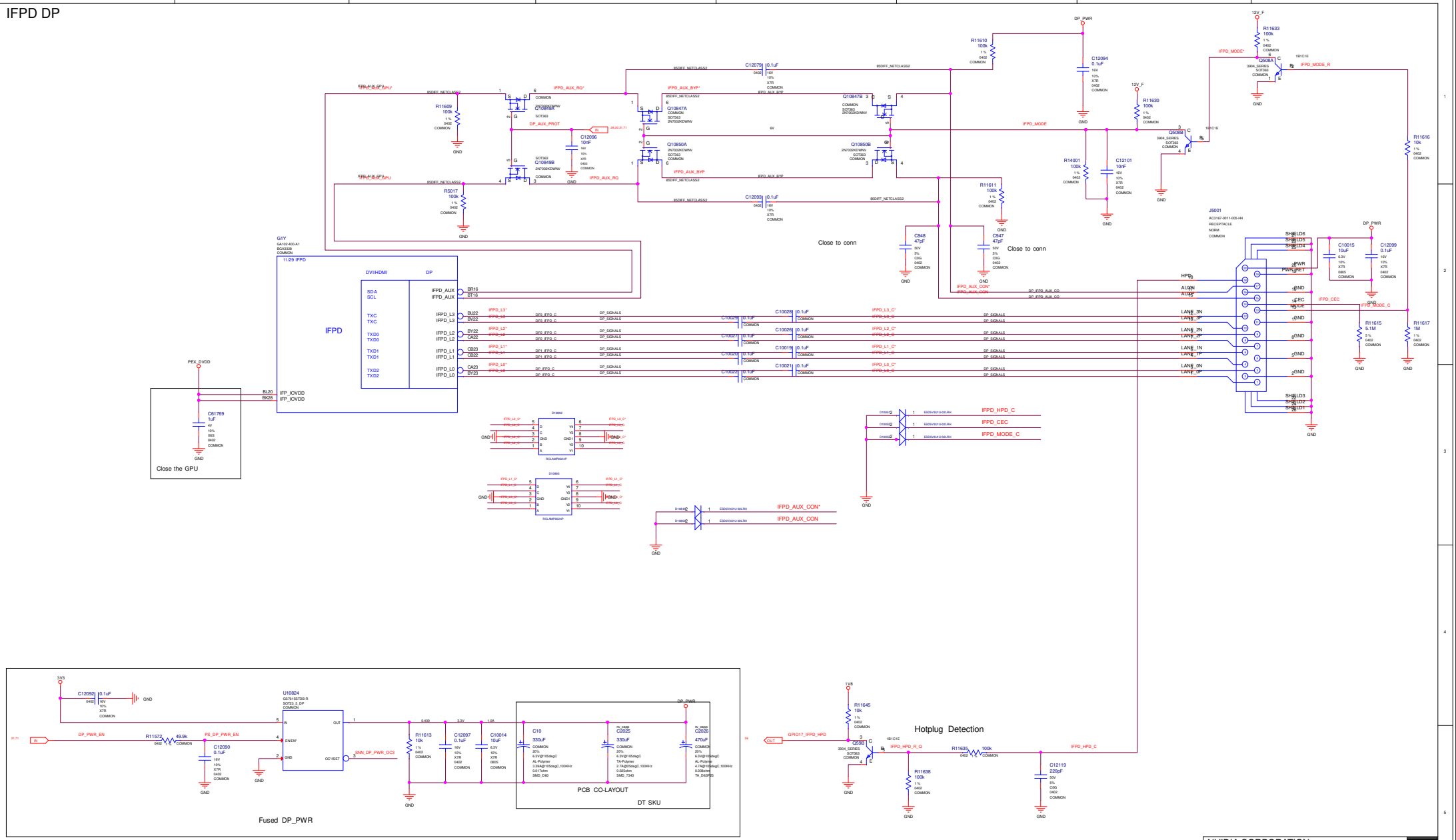
IFPD DP



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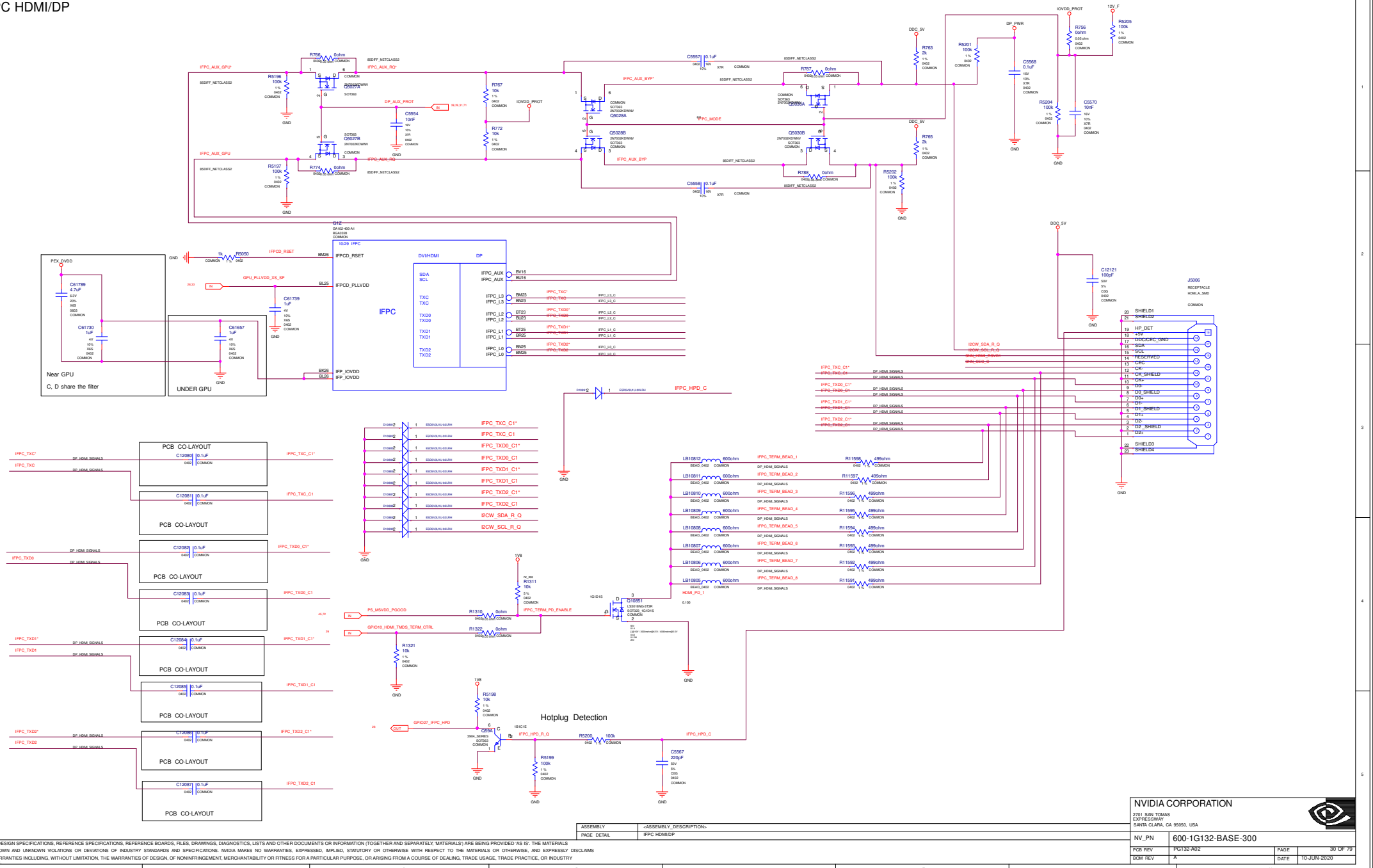
IFPC HDMI/DP



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE_DETAIL	IFPC HDMI/DP

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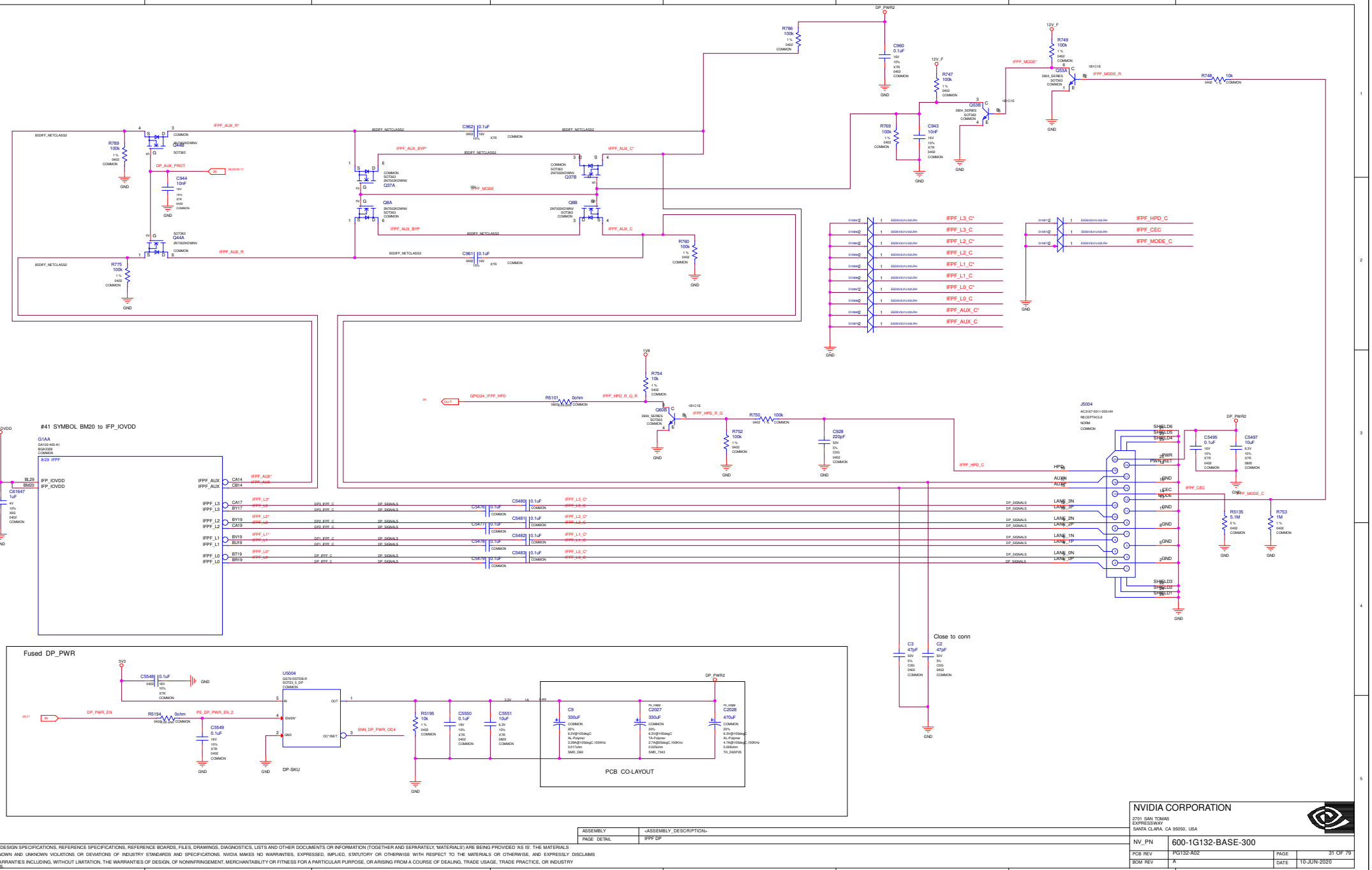

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MISC: ROM, Straps

H=High :Tied to 1.8V
M=Middle:Tied to 0.9V
L=Low :Tied to 0V

GROUP0

STRAP2	STRAP1	STRAP0	RAMCFG[4:0]		
L	L	L	00000	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)	<-A01 PCB
H	L	L	00100	RAMCFG MICRON 8Gb G6X 19Gbps x8 (161-0430-900)	
H	L	H	00101	RAMCFG MICRON 8Gb G6X 21Gbps x8 (161-0431-900)	
L	L	M	01000	RAMCFG MICRON 8Gb G6X 20Gbps x16 (161-0424-900)	
L	L	H	00001	RAMCFG MICRON 8Gb G6X 21Gbps x16 (161-0431-900)	<-OLD
L	M	H	01010	RAMCFG MICRON 8Gb G6X 19Gbps x16 (161-0430-900)	<-LATEST A02 PCB

ROM_SO	ROM_SI	ROM_SCLK	SMARTFAN[2:0],FS_OVERT	1:ENABLE 0:DISABLE	
H	H	H	0111	FS_OVERT ENABLE	DEFAULT
L	L	L	0000	FS_OVERT DISABLE	

1:SMB_ALT_ADDR ENABLE
0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND
0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER
0:PCIE_CFG HIGH POWER

1:VGA_DEVICE ENABLE
0:VGA_DEVICE DISABLE

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE	
M	H	H	1	1	1	1	
M	H	L	1	1	1	0	
M	L	H	1	1	0	1	
M	L	L	1	1	0	0	
L	H	M	1	0	1	1	
L	M	H	1	0	1	0	
L	M	L	1	0	0	1	
L	L	M	1	0	0	0	
H	H	H	0	1	1	1	
H	H	L	0	1	1	0	
H	L	H	0	1	0	1	
H	L	L	0	1	0	0	
L	H	H	0	0	1	1	
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L	L	H	0	0	0	1	Default
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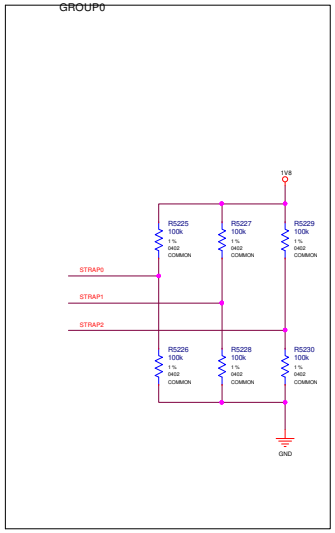

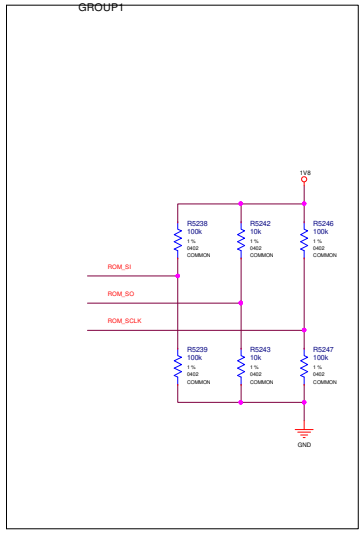

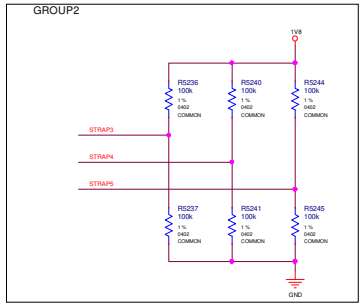

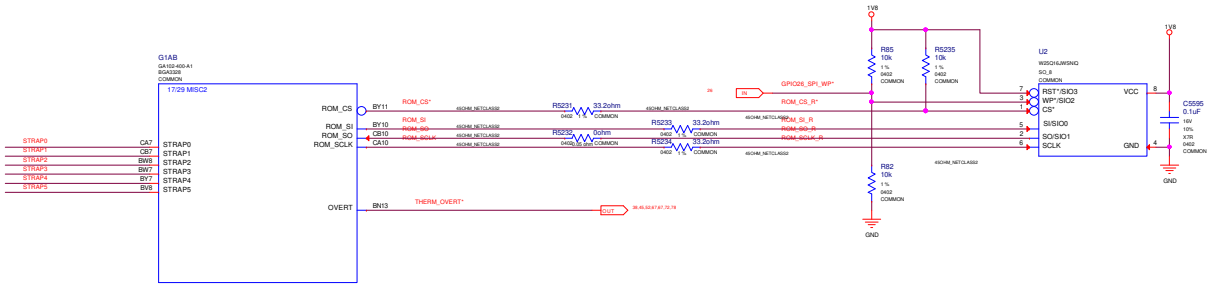

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PAGE DETAIL	'MISC: ROM, STRAPS'

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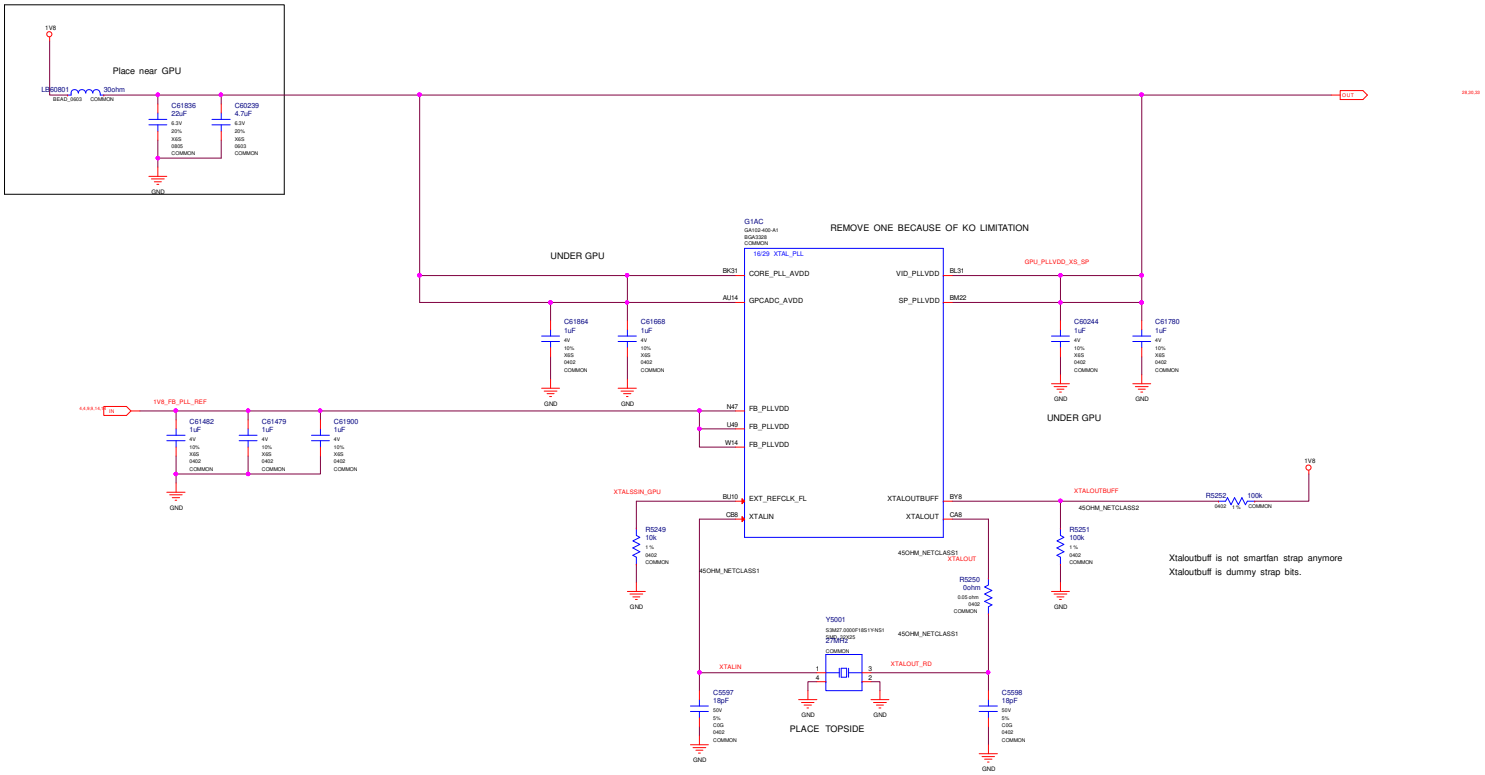
MISC: XTAL. PLL



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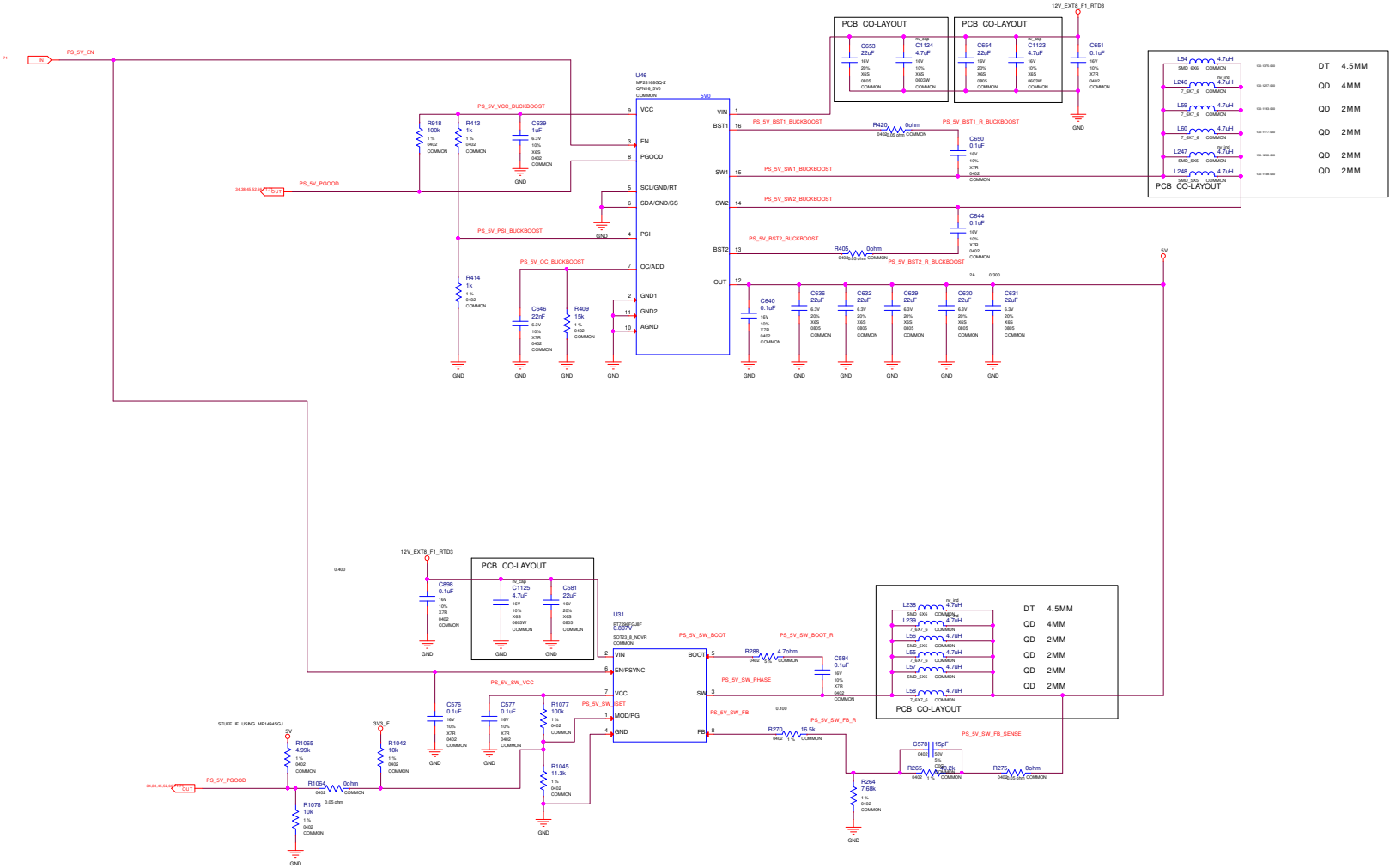

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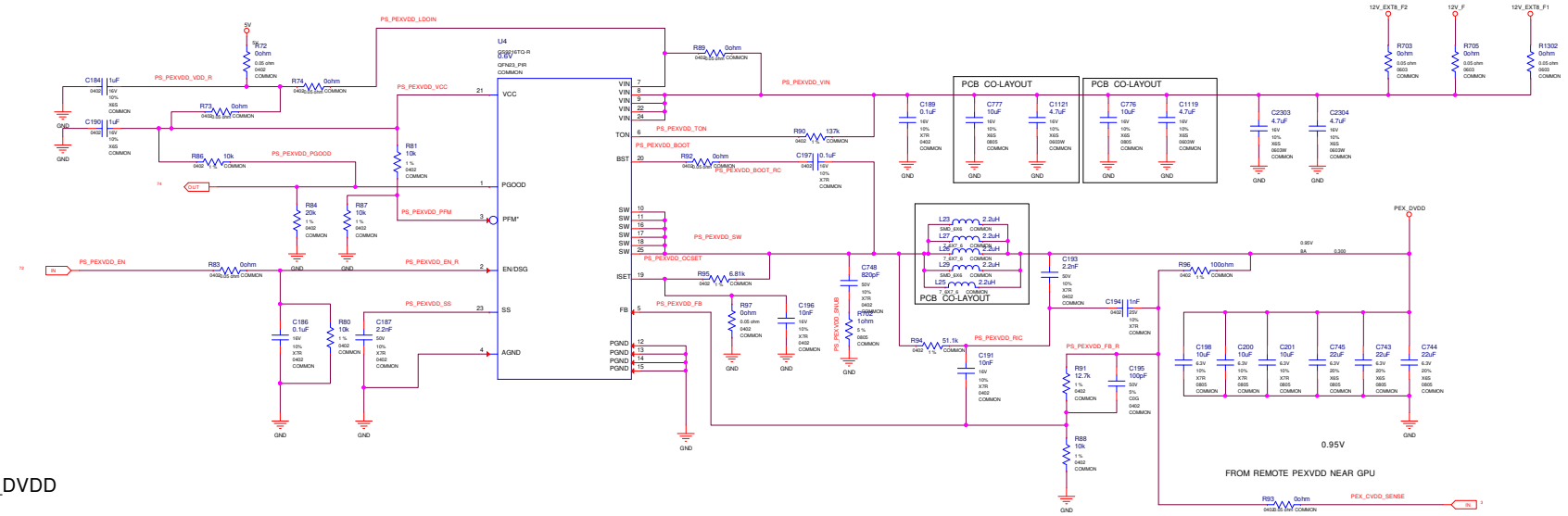
PS: PEX_DVDD 1V8 Rail



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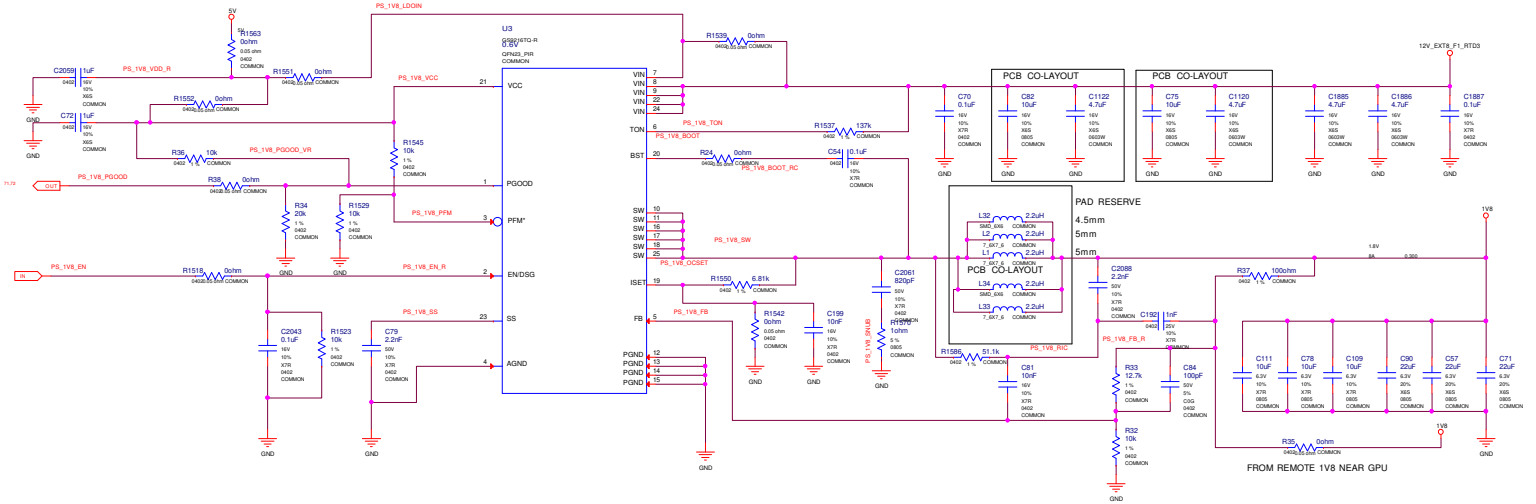

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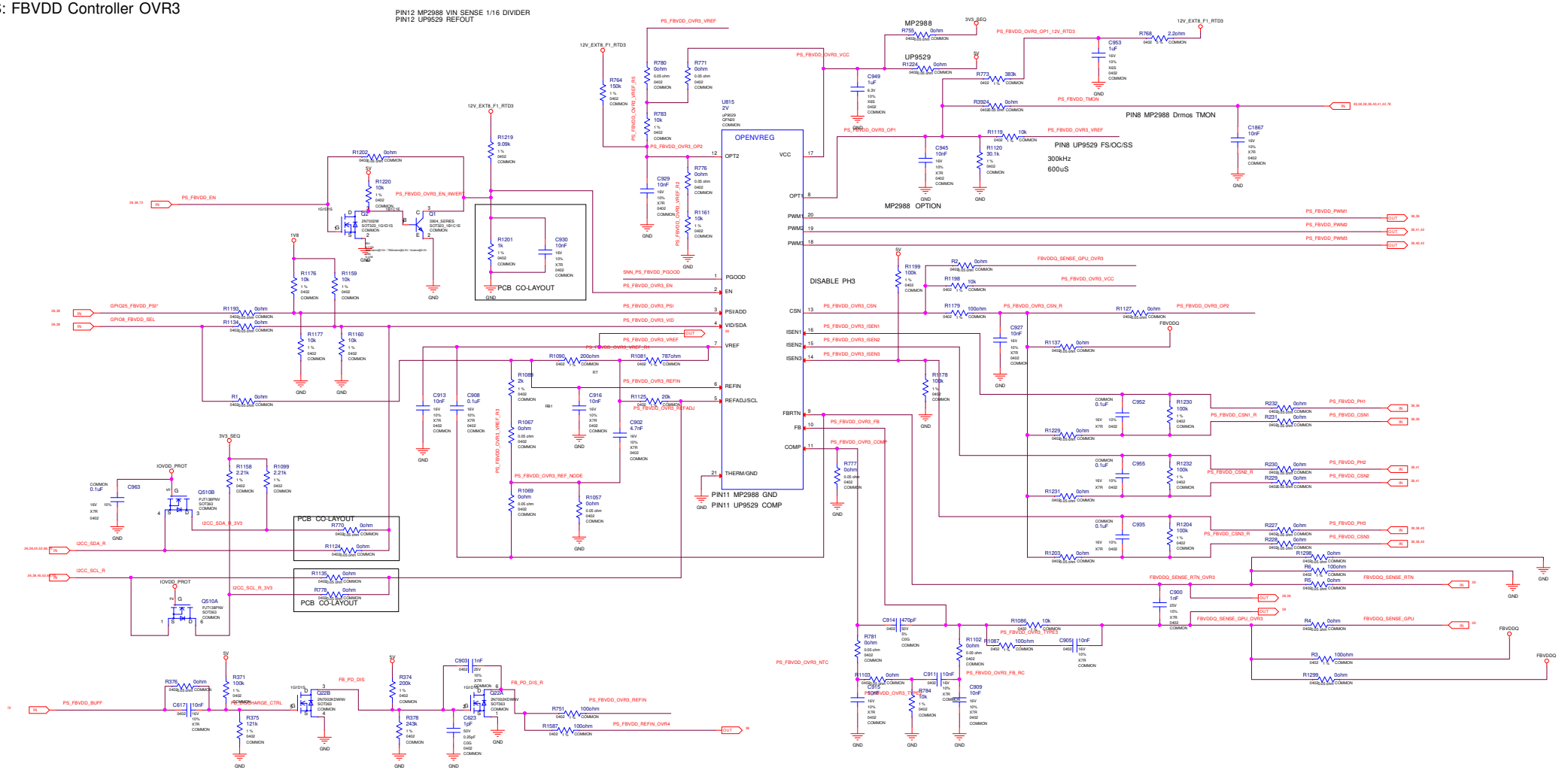
PS: FBVDD Controller OVR3



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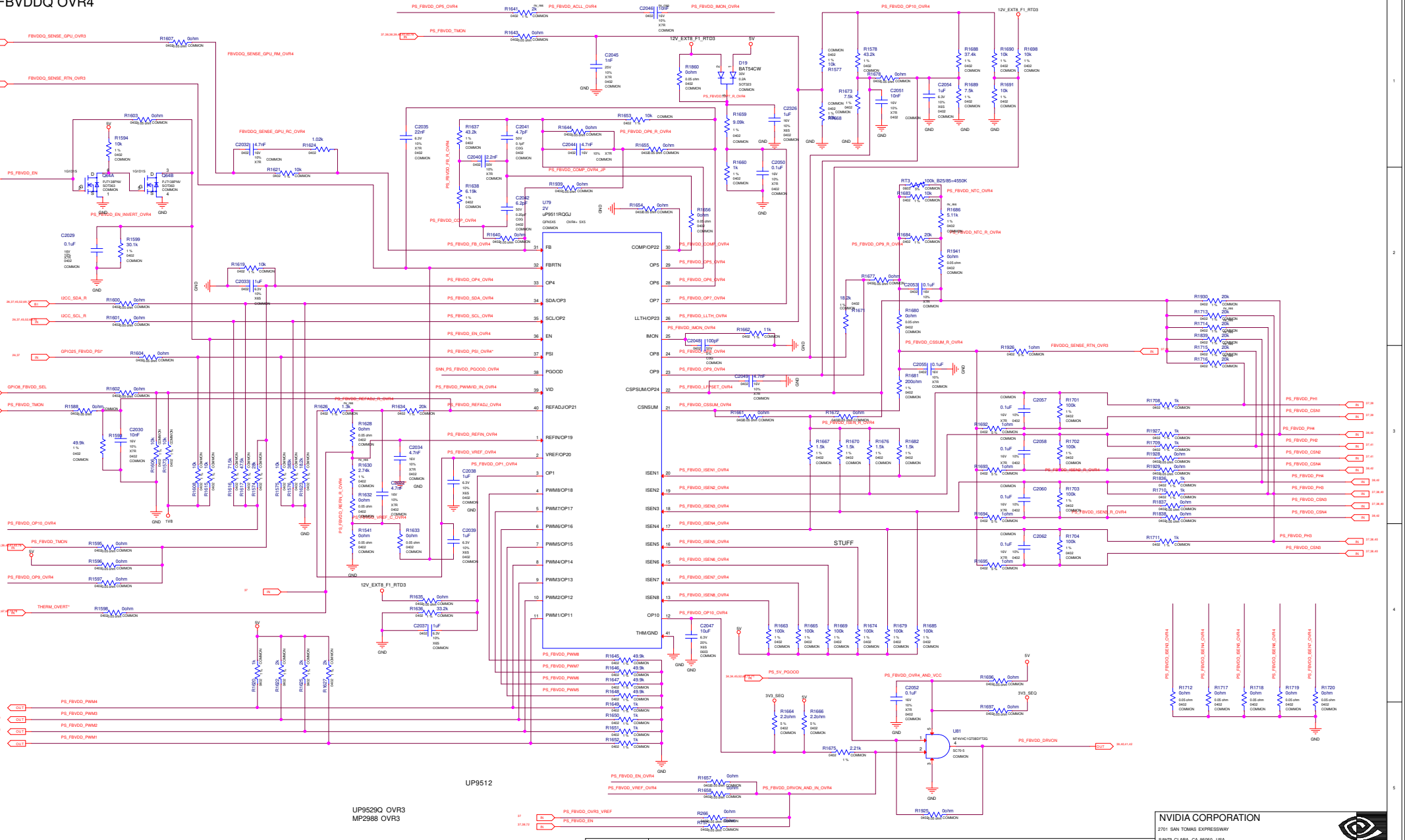
PS:FBVDDQ OVR4



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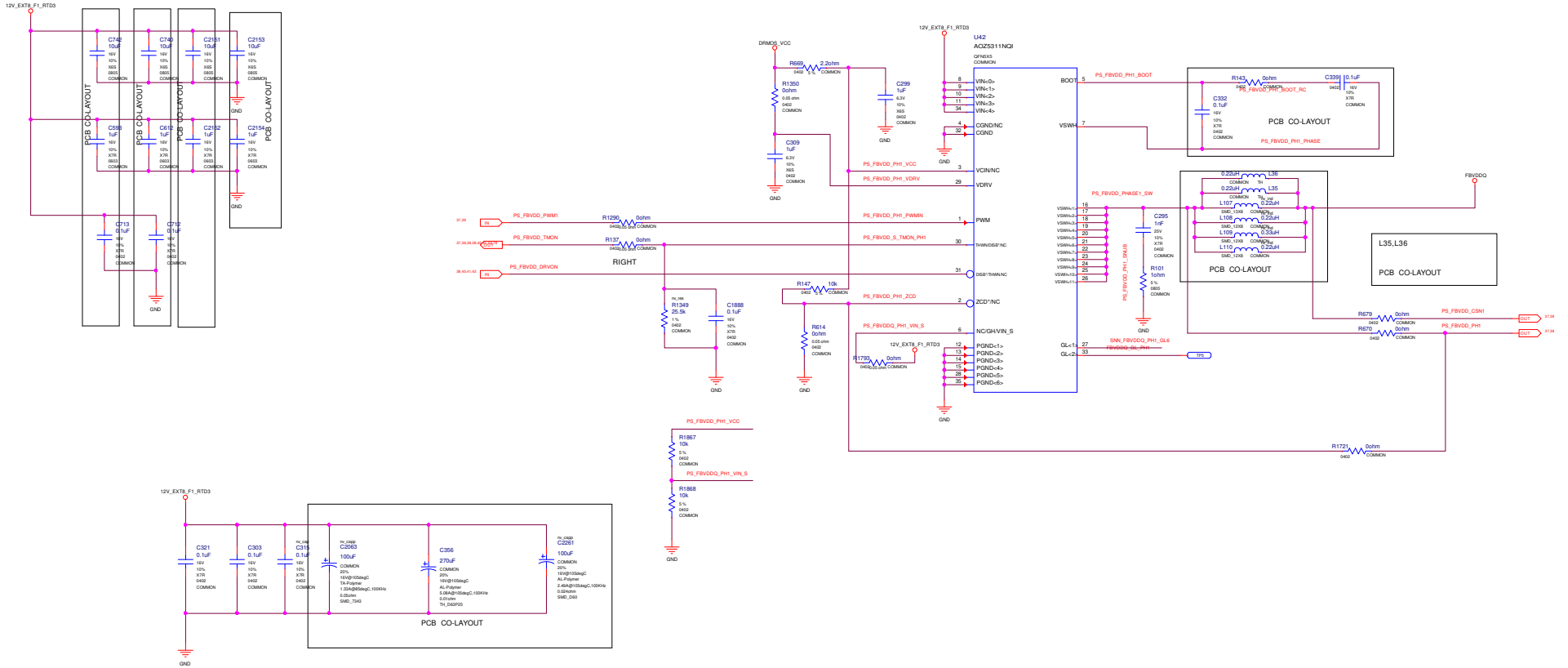
PS: FBVDD PH1



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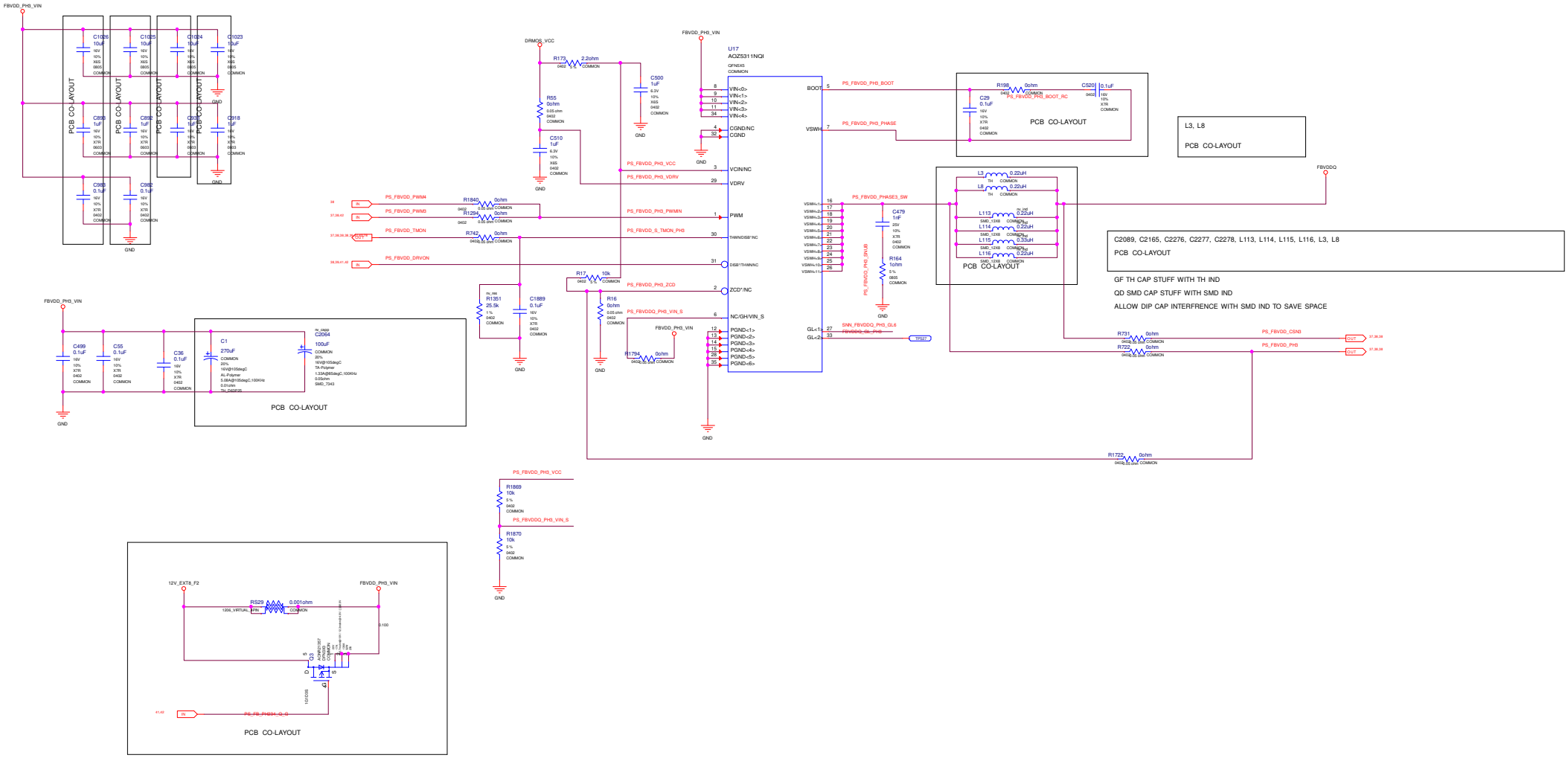
PS: FBVDD PH3



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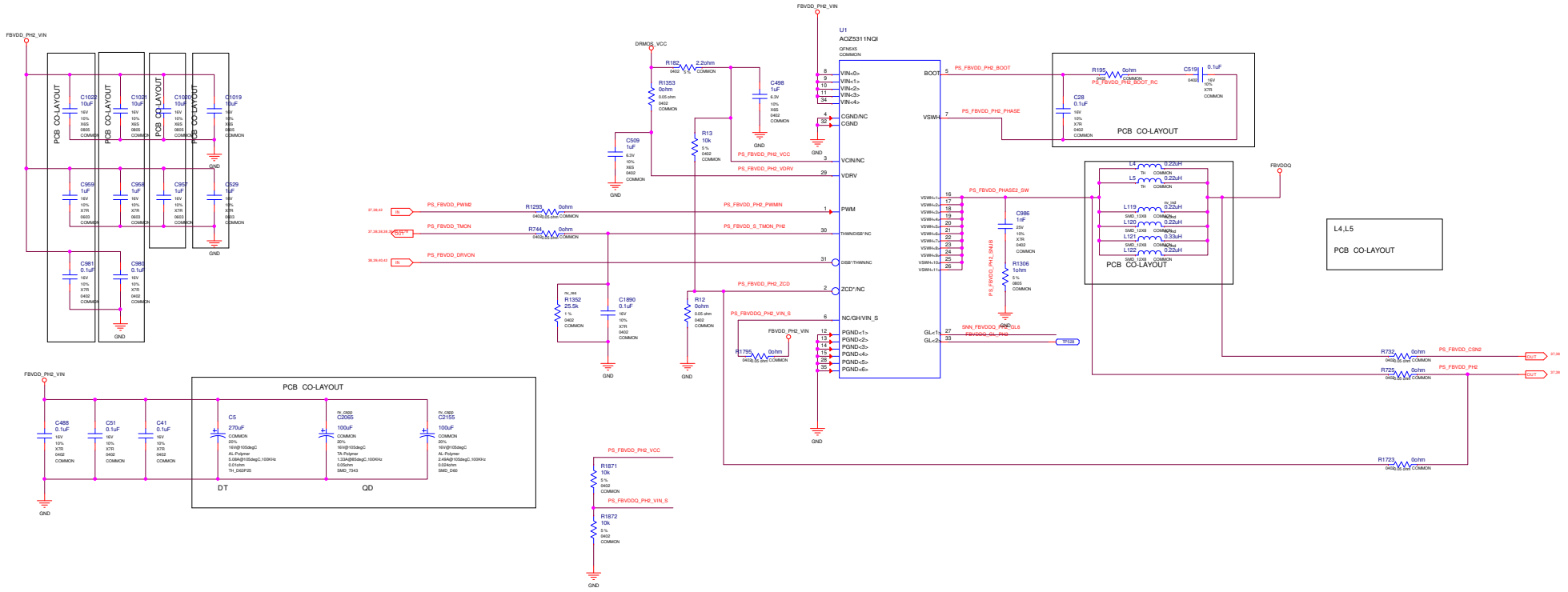

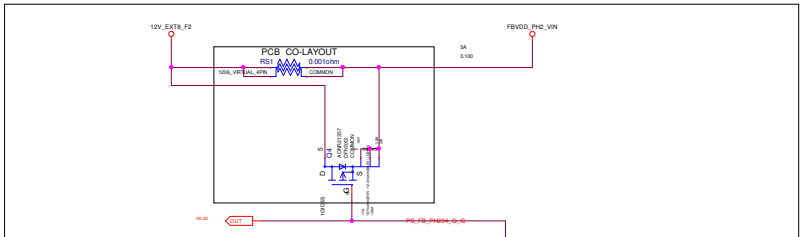

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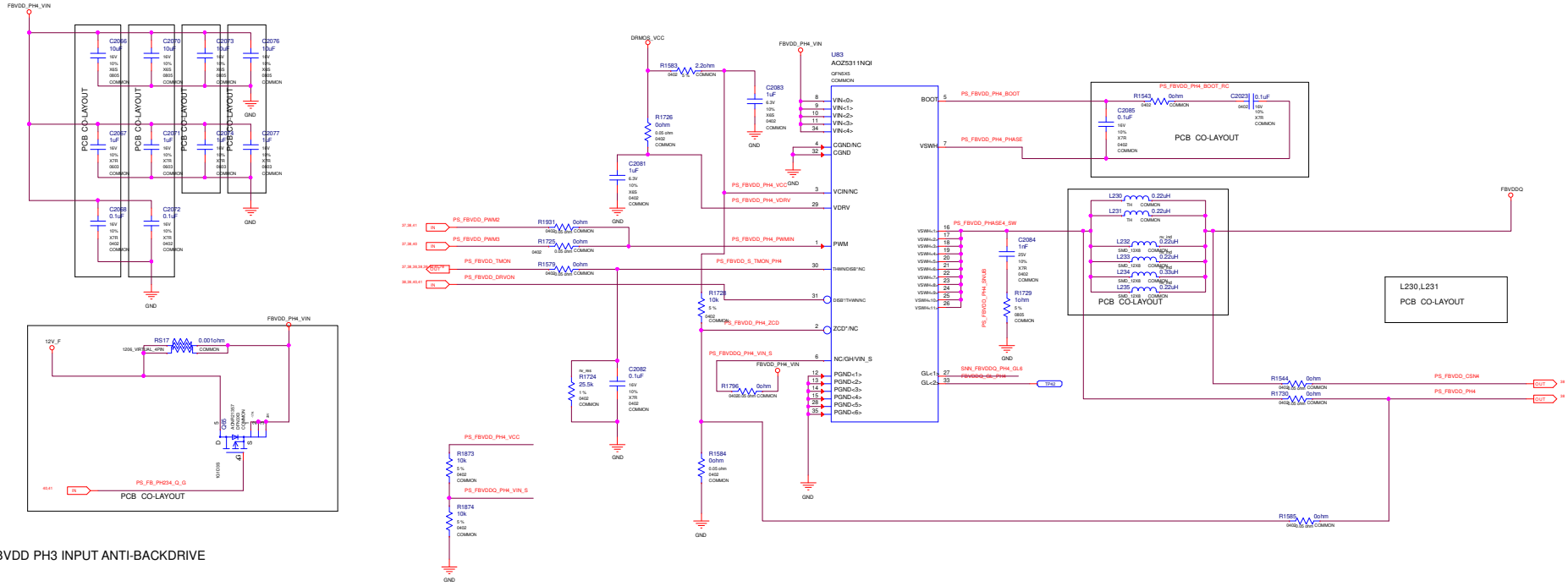

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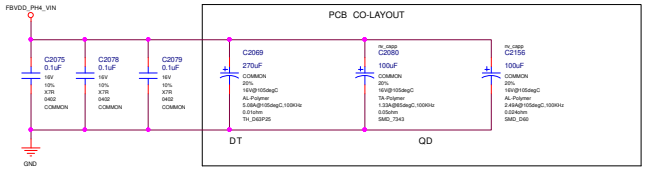

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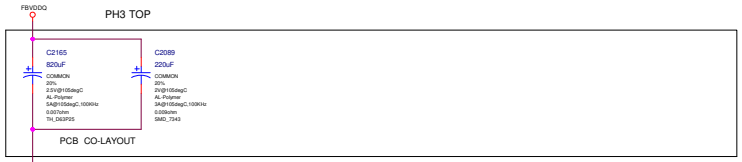
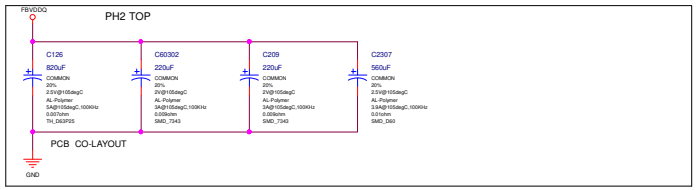
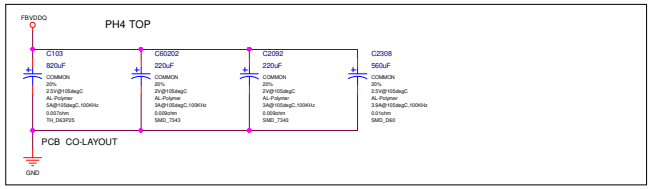
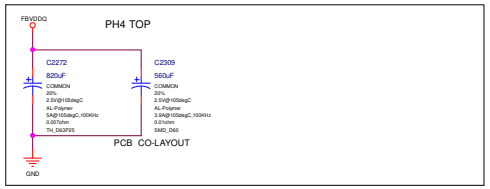
PS: FBVDD OUTPUT CAP

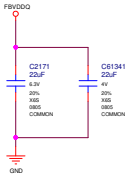
3x 820uF TH FBVDD OUTPUT BULK CAPS











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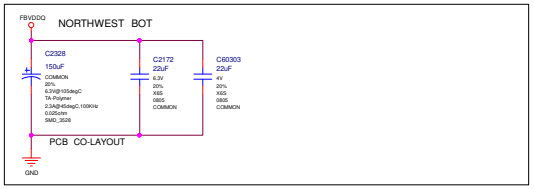

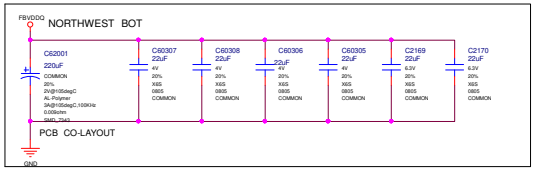

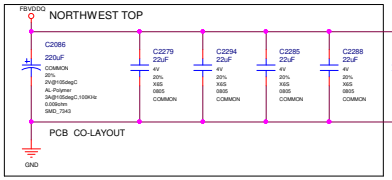

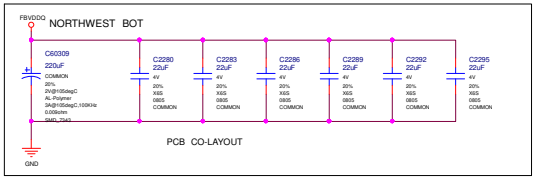

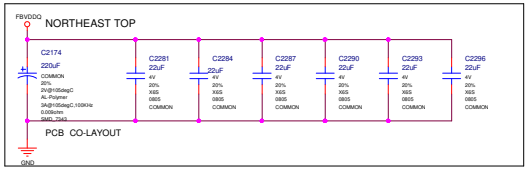

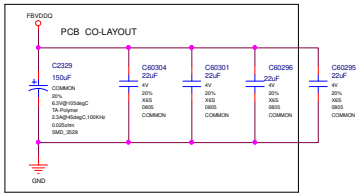

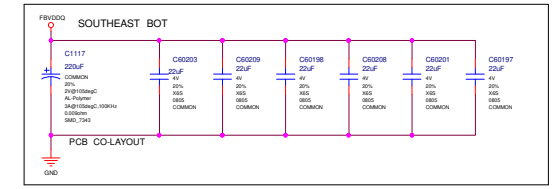

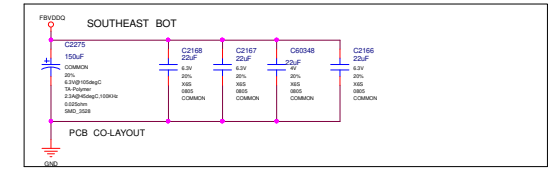

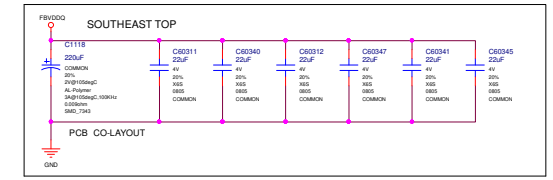

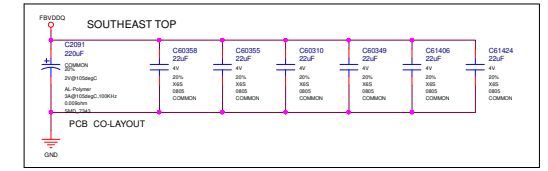

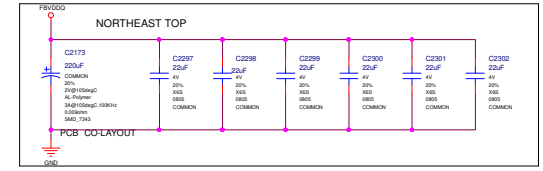

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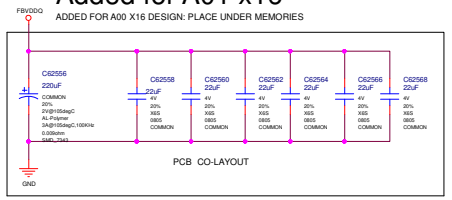
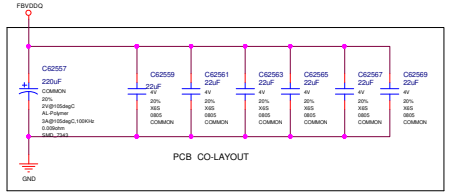
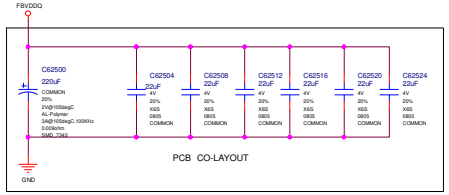
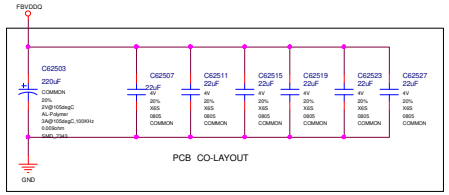
Added for A01 x16

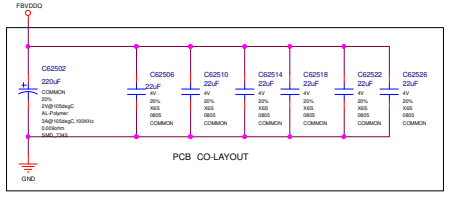
ADDED FOR A00 X16 DESIGN: PLACE UNDER MEMORIES

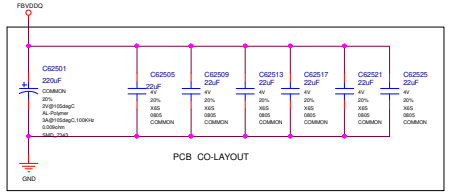


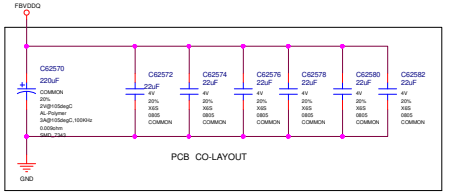


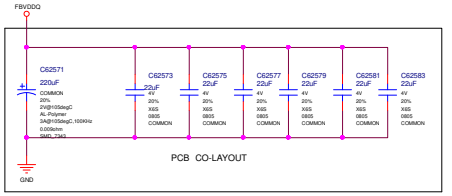


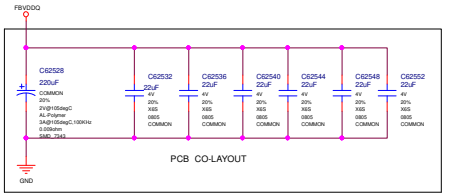


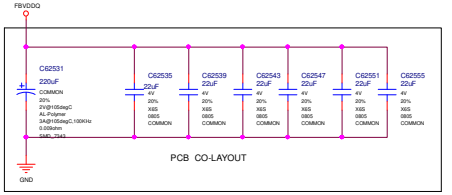


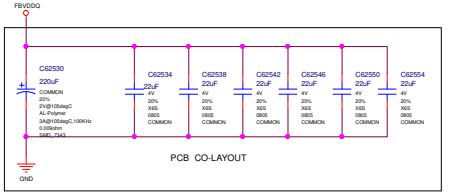


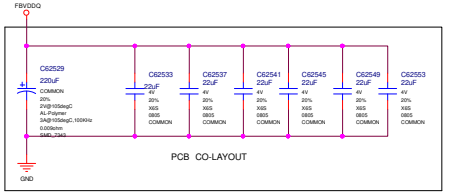












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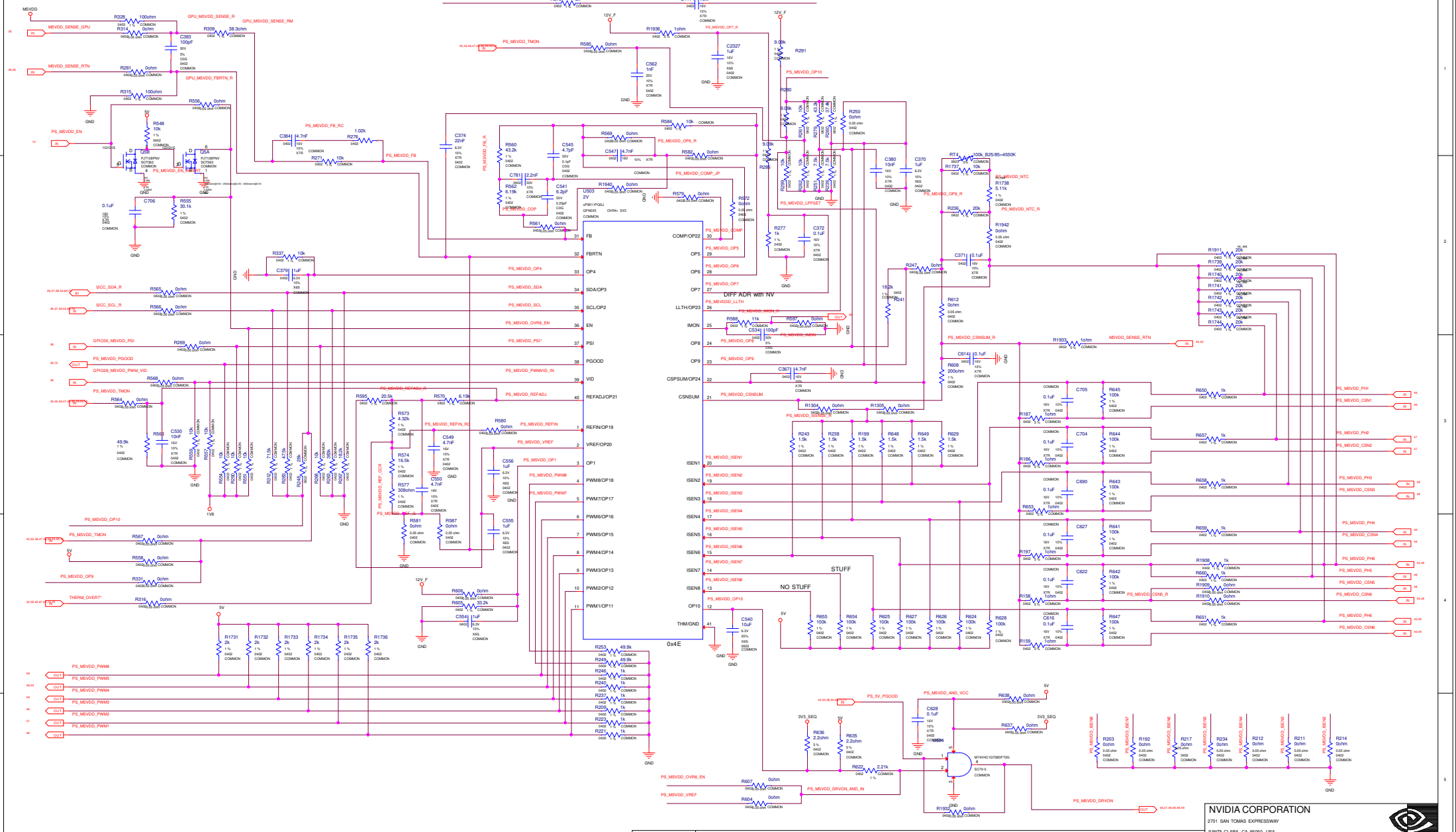

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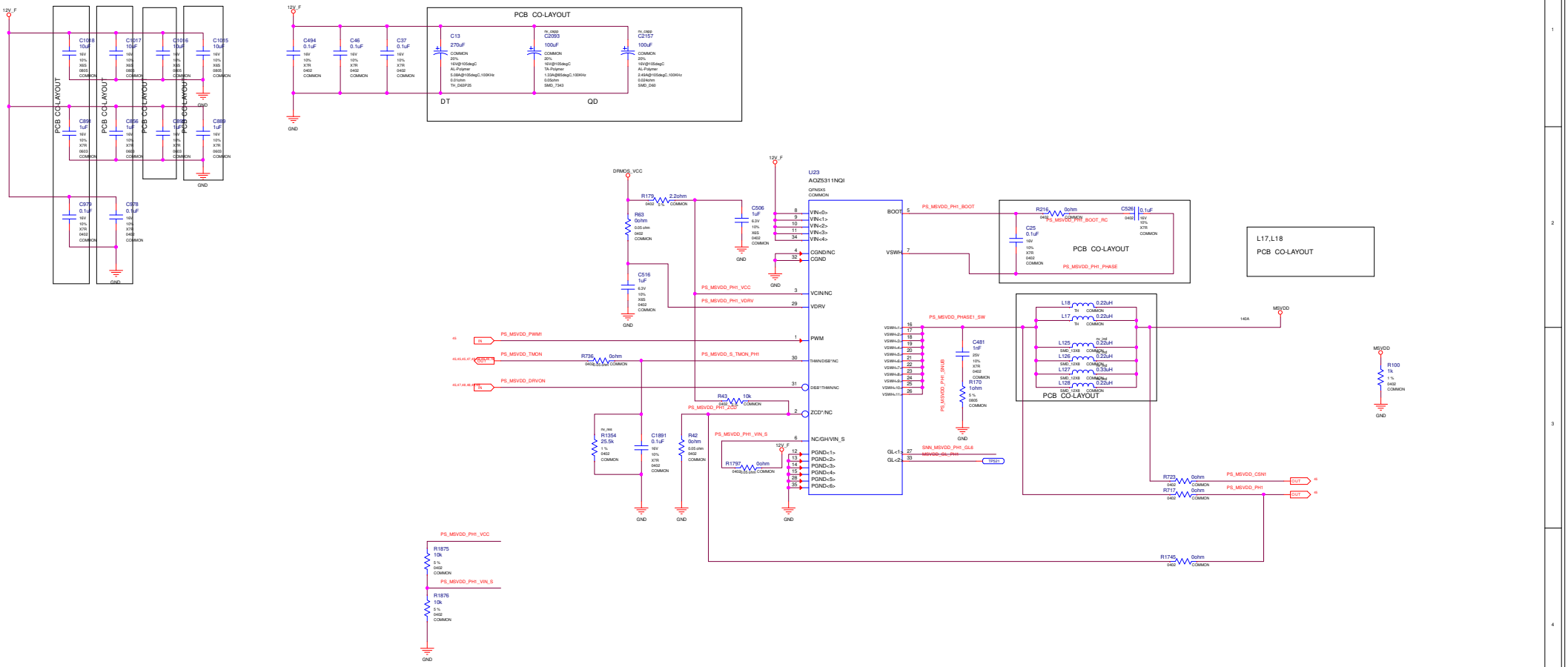
PS: MSVDD Phase 1



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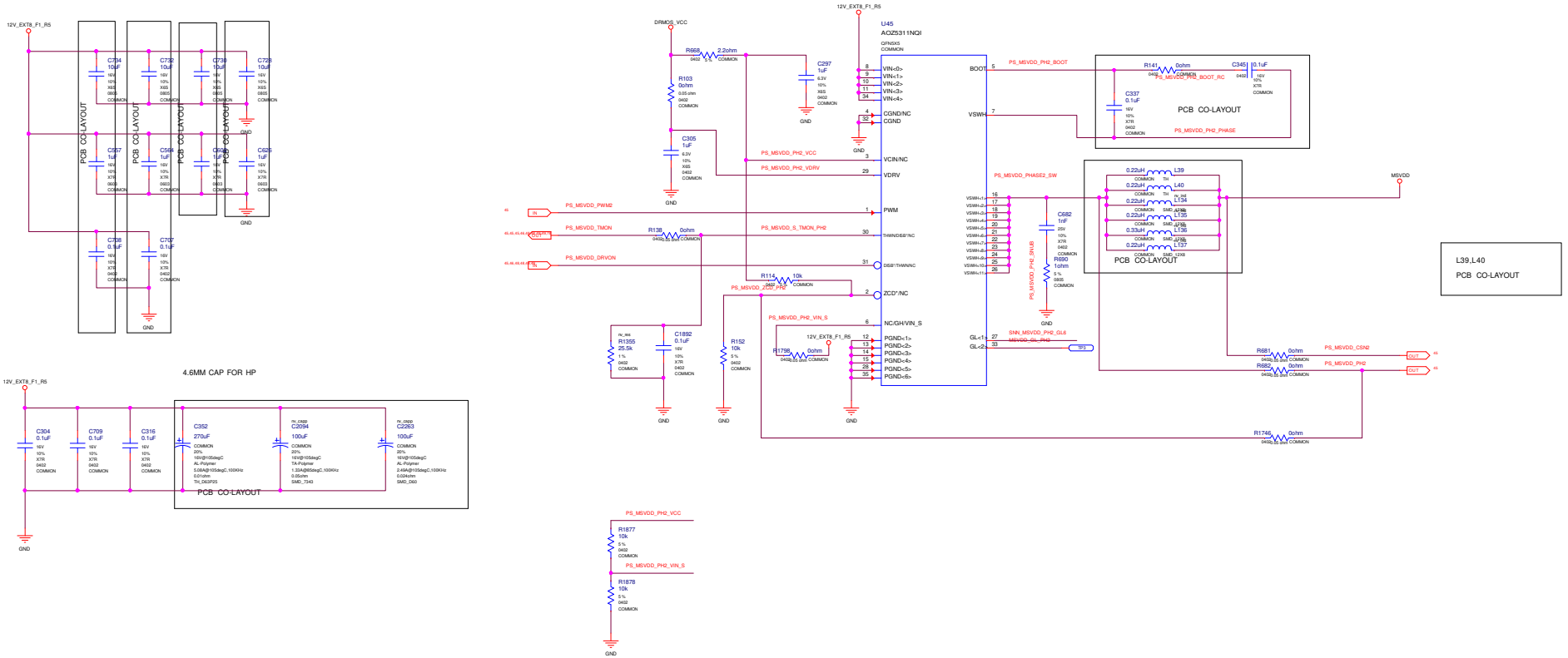
PS: MSVDD PH 2



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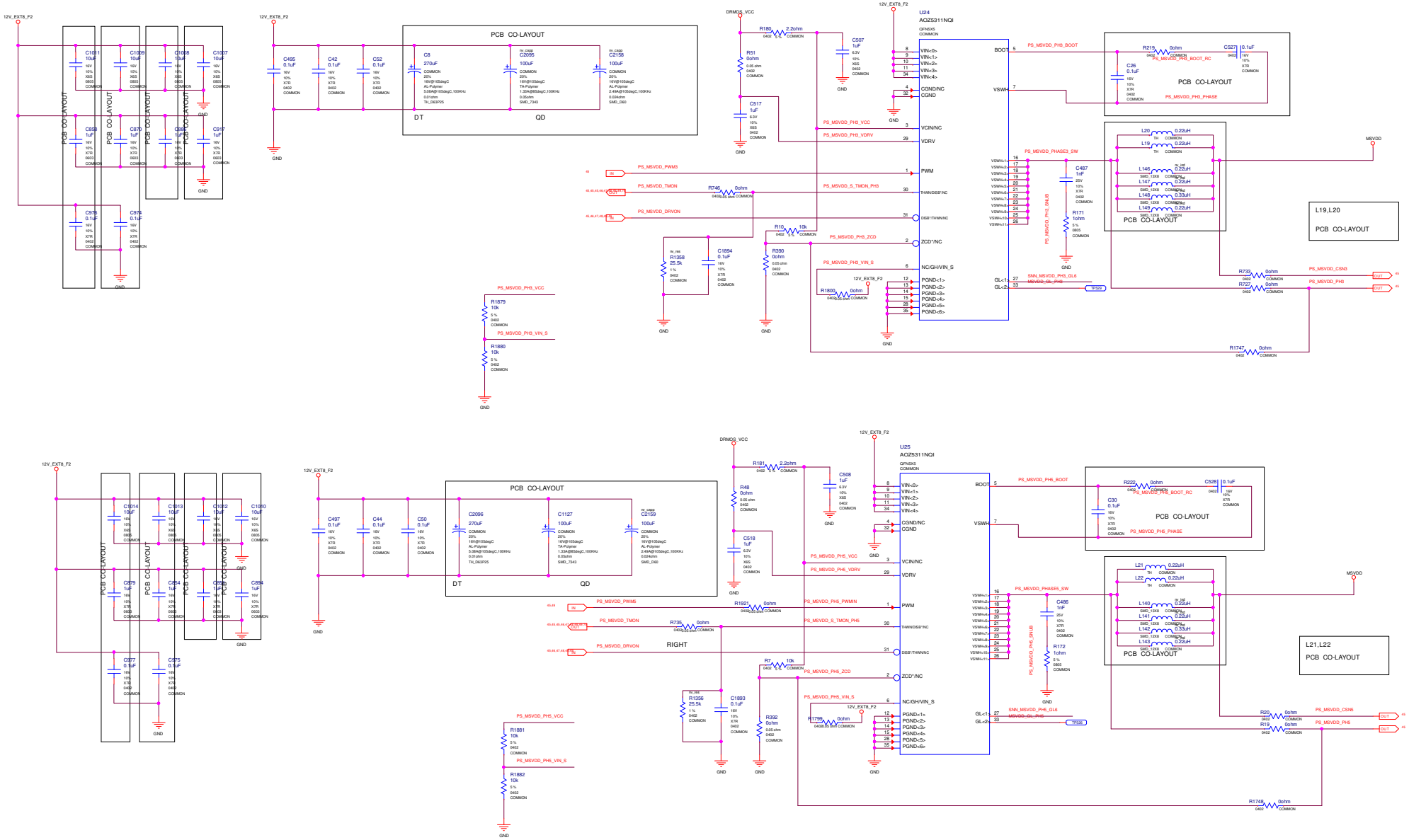

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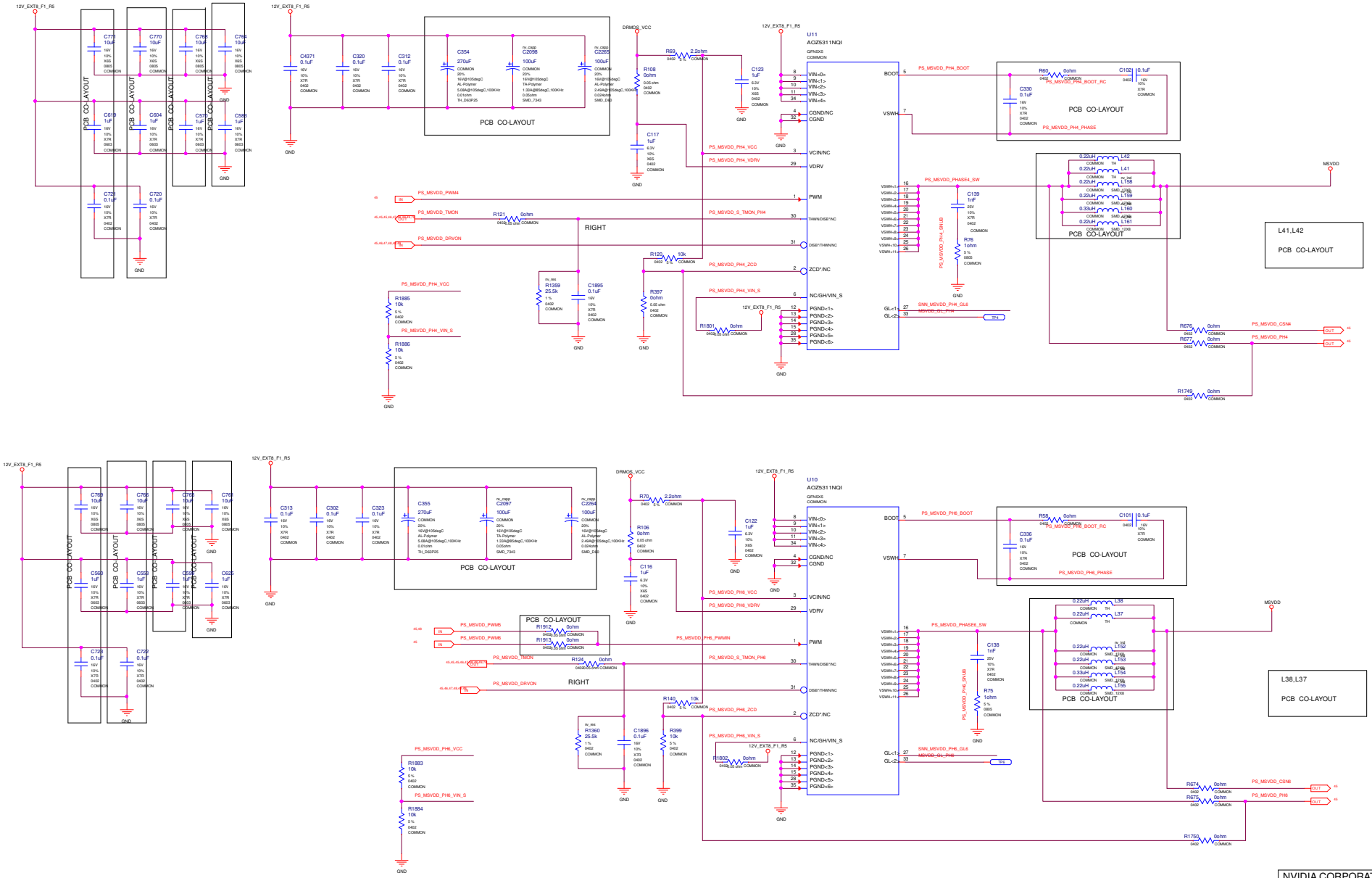

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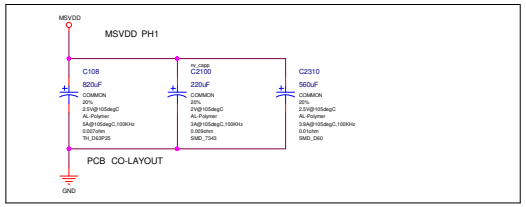

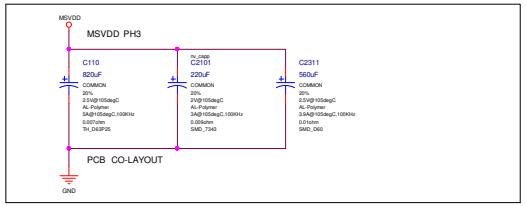

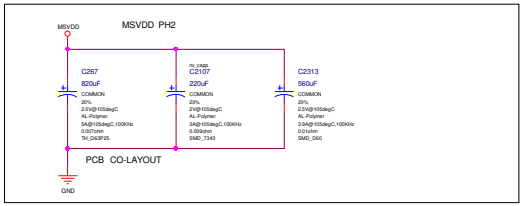

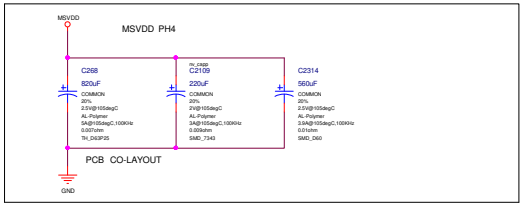

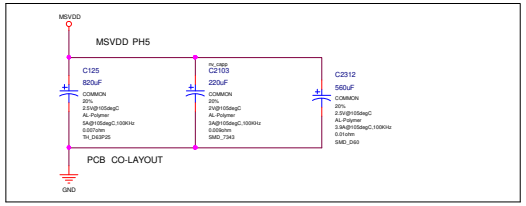

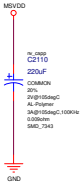

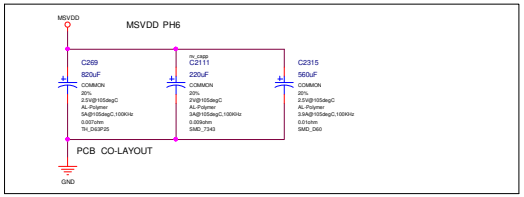

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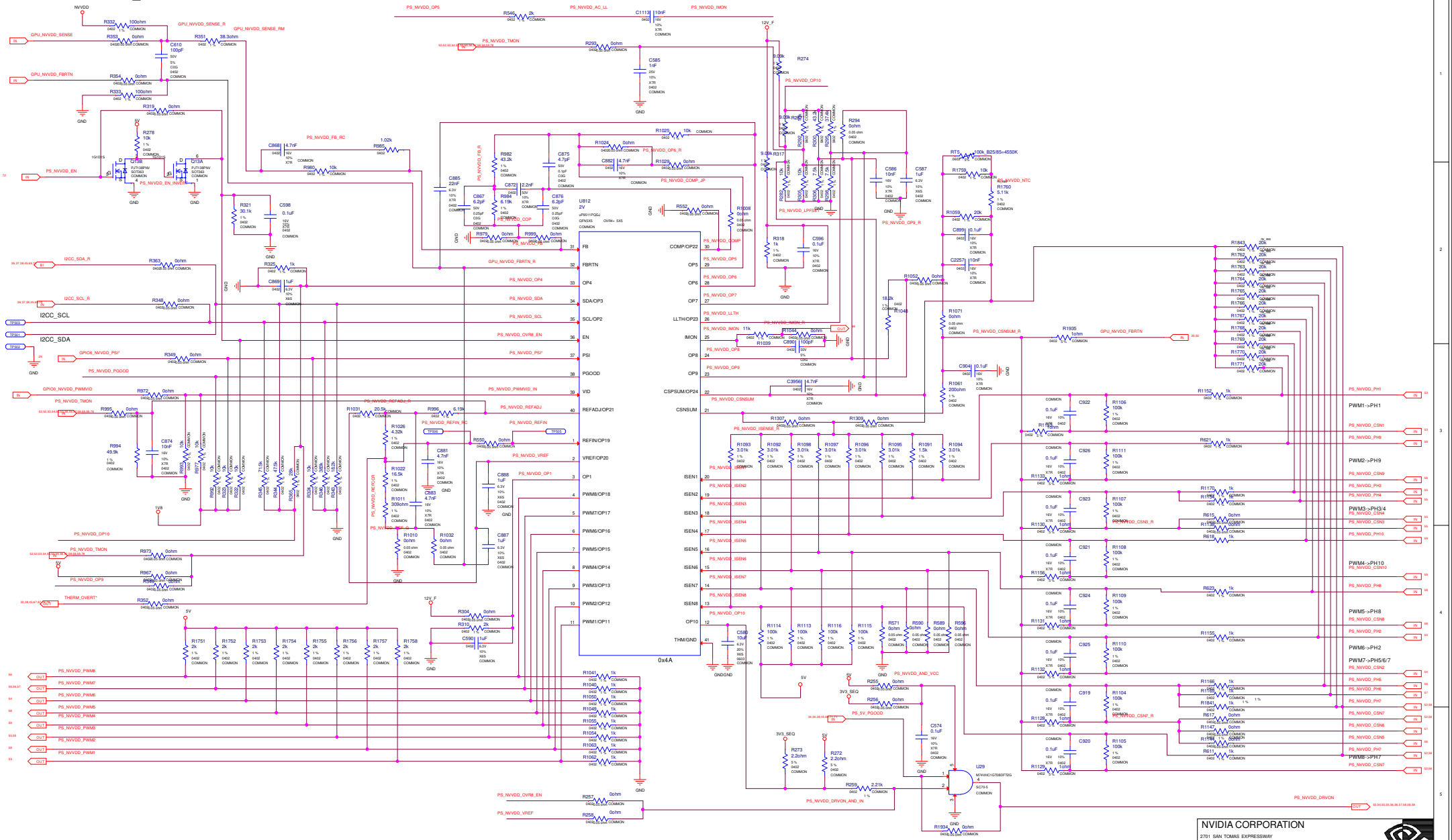

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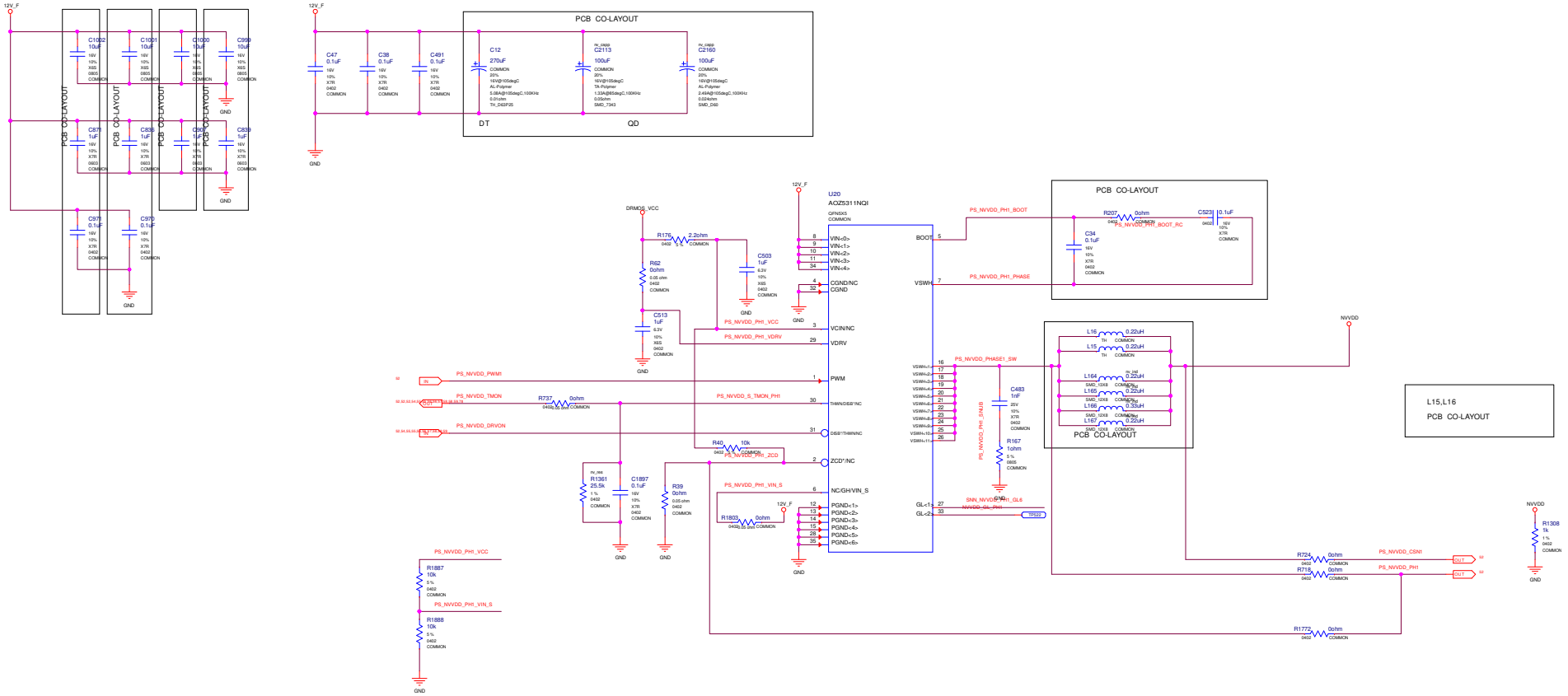
PS: NVVDD Phase 1



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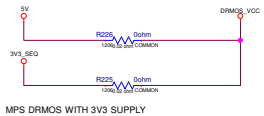
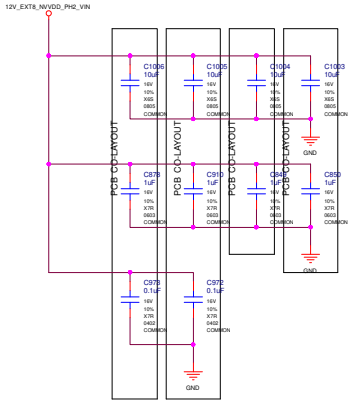
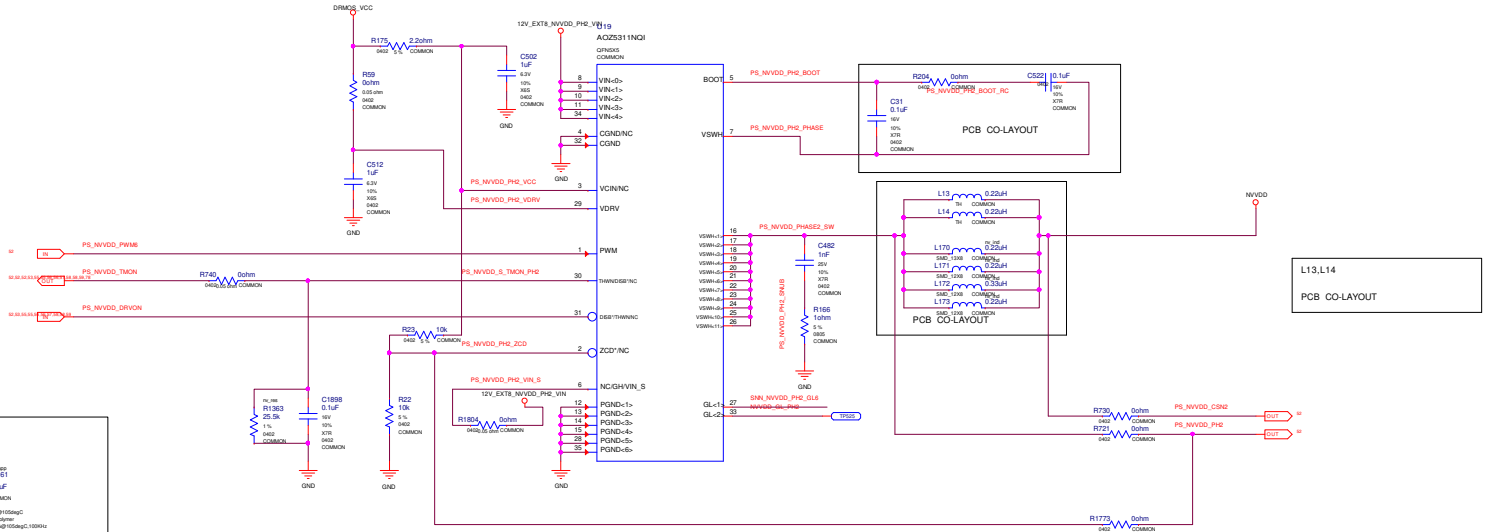
PS: NVVDD Phase 2



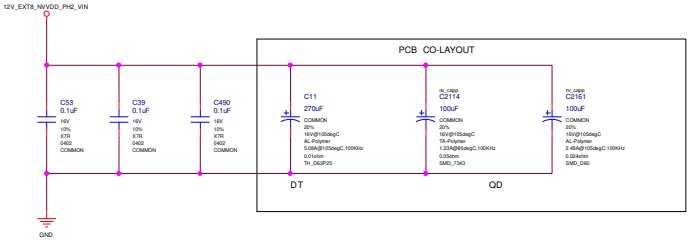
MPS DRMOS WITH 3V3 SUPPLY

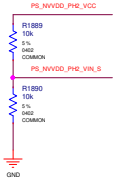


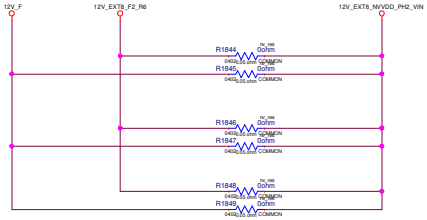


L13,L14

PCB CO-LAYOUT







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PAGE_DETAIL	PS: NVVDD PH2(PWM6)

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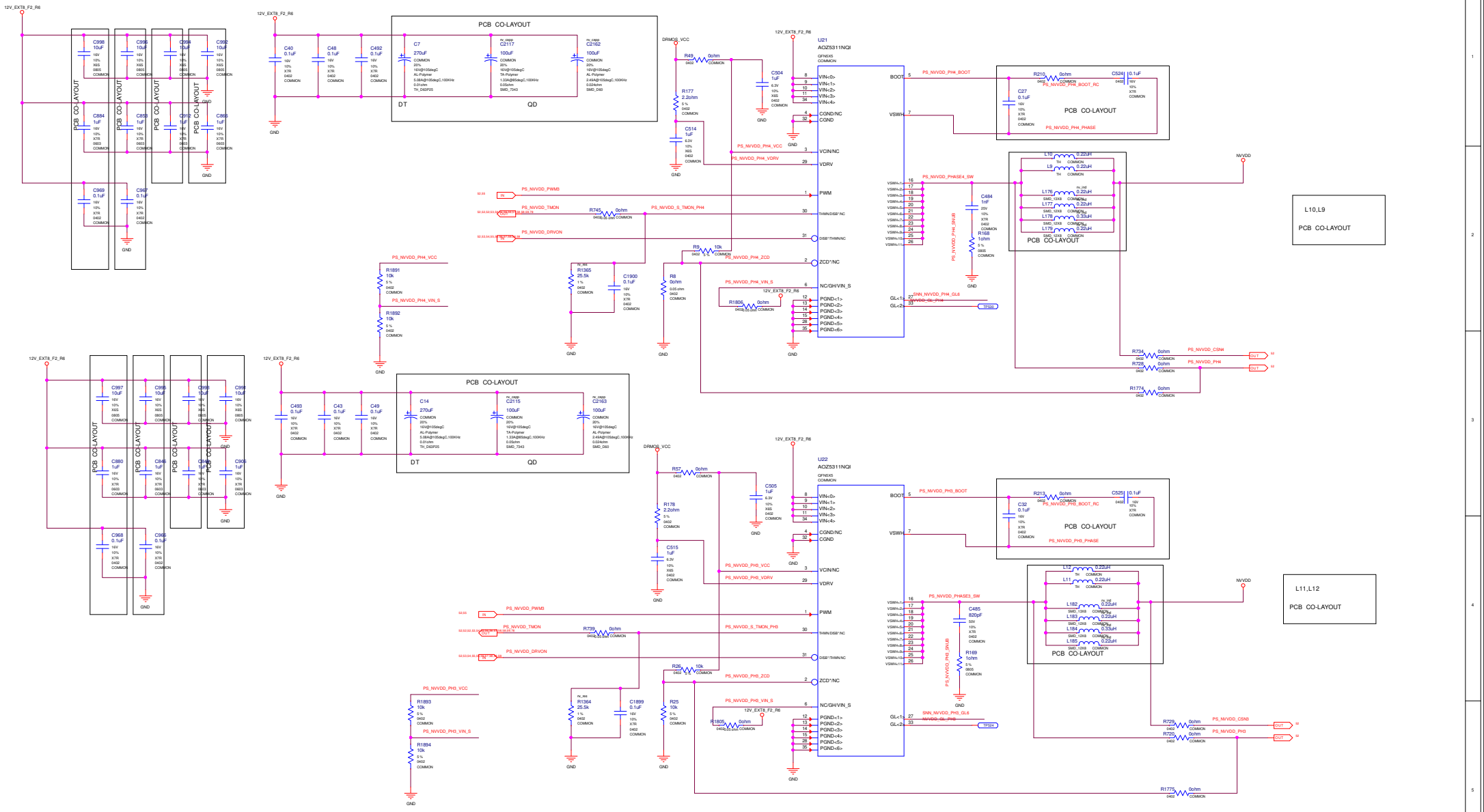
PS: NVVDD Phase 3 (PWM6), PHASE 4(PWM2)



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PAGE DETAIL	PS: NVDD PH3 (PWM3) and PH4 (PWM5)

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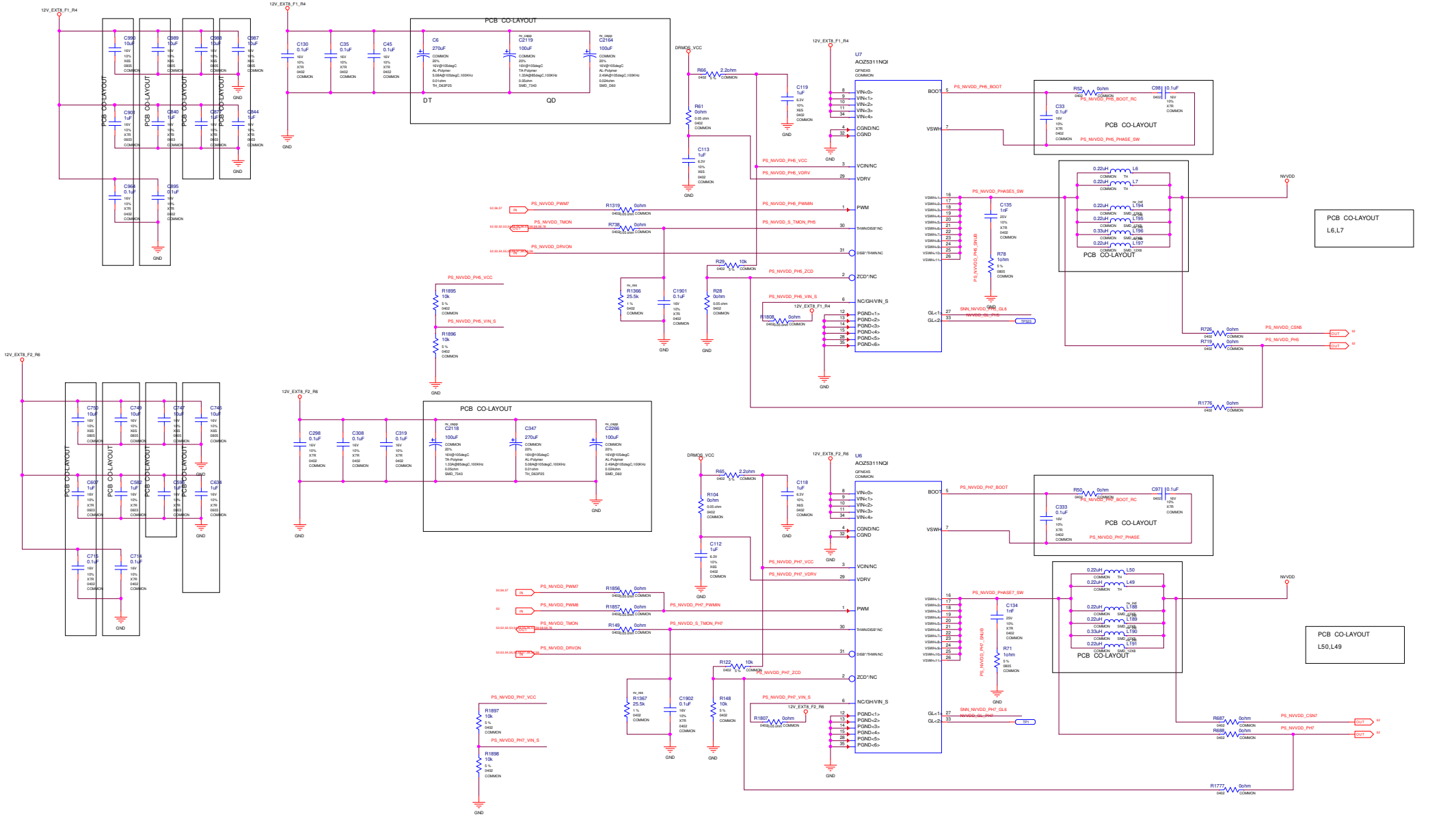
PS: NVVDD PH 5(PWM2), PH7(PWM3)



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PAGE DETAIL	PS: NVDD PH5(PWM7) and PH7(PWM8)

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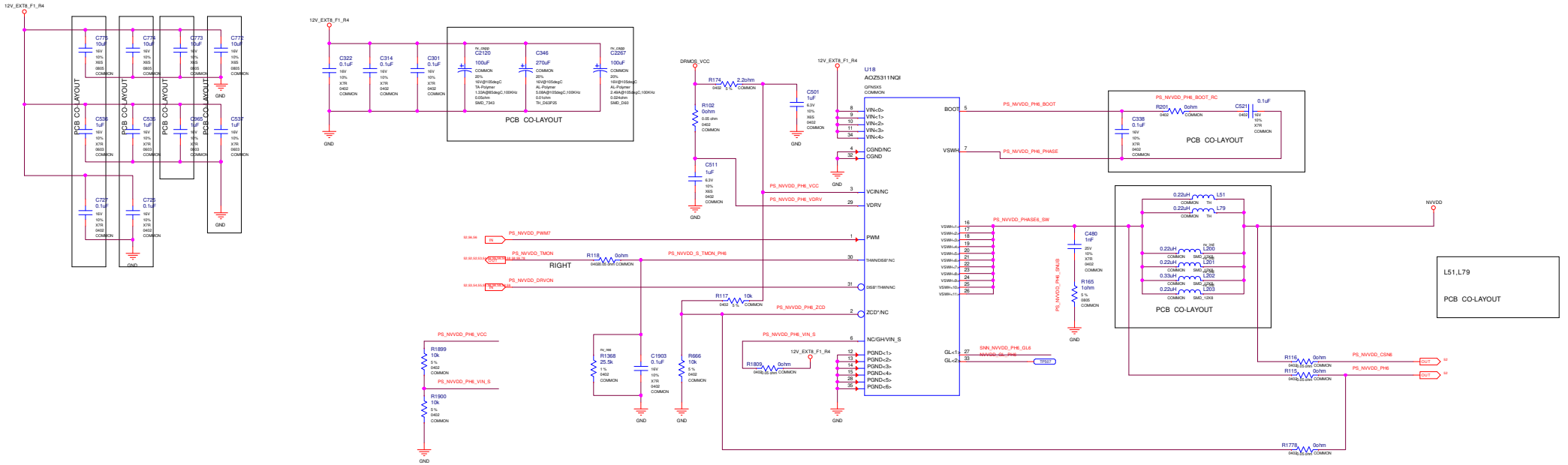
PS: NVVDD Phase 6(PWM7)



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PAGE DETAIL	PS: NVDD PH6 (PWM7)

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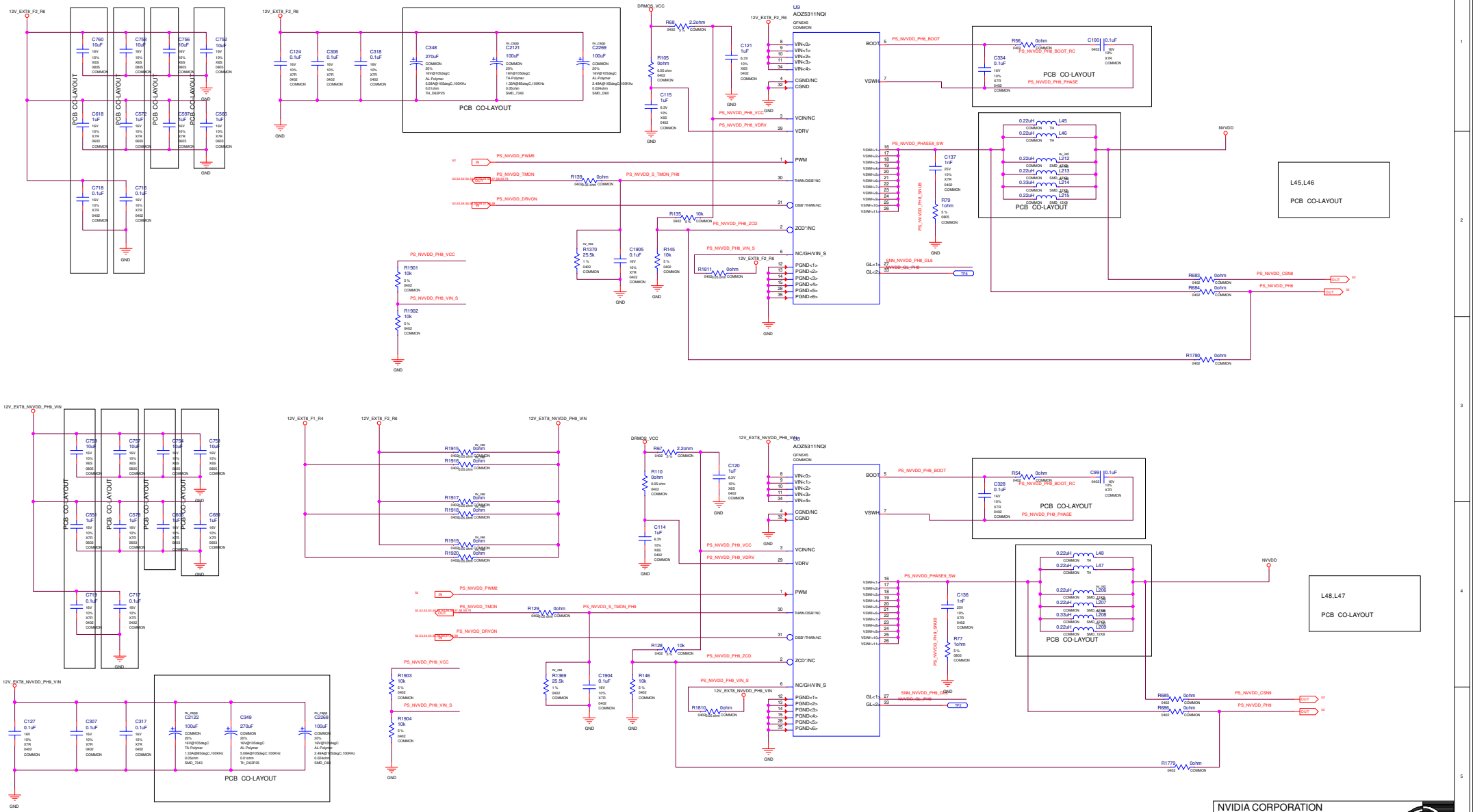
PS: NVVDD PH 8 (PWM5), PH 9(PWM8)



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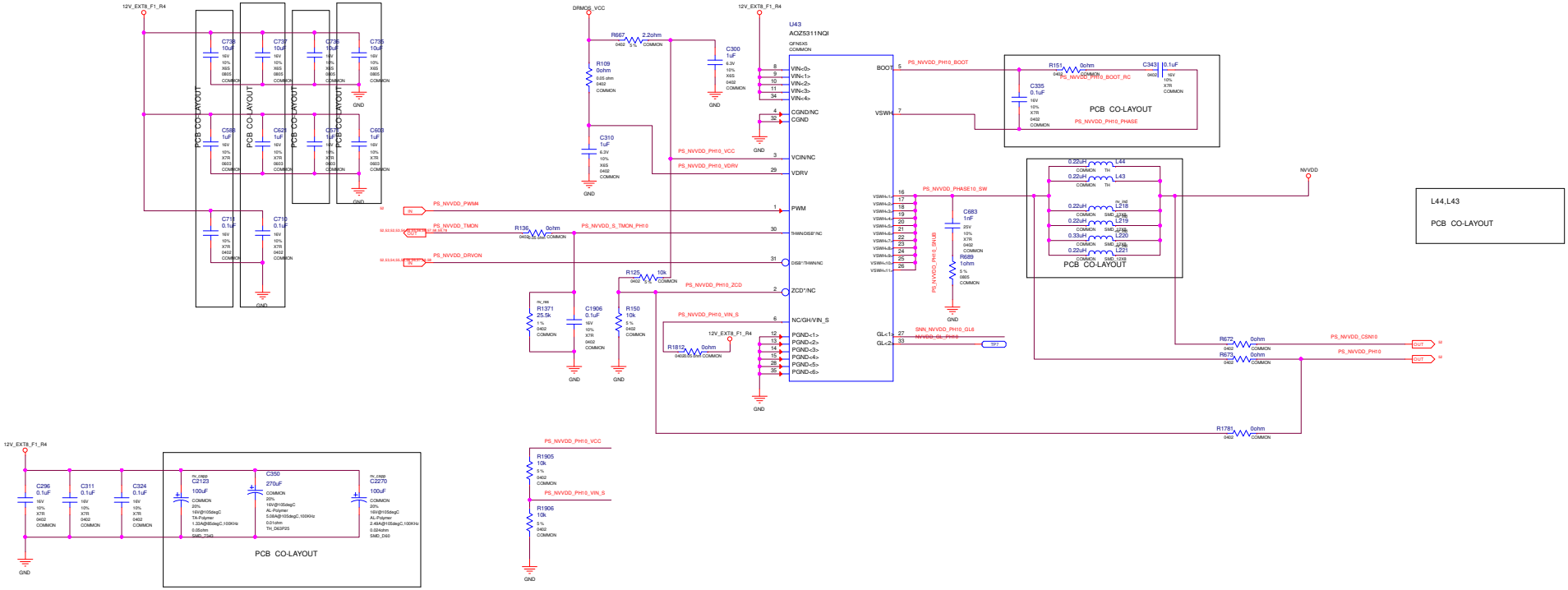
PS: NVVDD Phase 10 (PWM8)



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PCB CO-LAYOUT

C131, C132, C133, C140, C141, C142, C2106, C2107, C2133, C2134, C2135, C2137, C264, C265, C266, C267, C61, C64, C65, C66, C67, C68, C69, C77, C80, C83, C88

PCB CO-LAYOUT

C103, C105, C106, C107, C108, C110, C1208, C125, C1254, C1256, C1267, C128, C144, C145, C146, C151, C152, C153, C154, C159, C160, C161, C162, C170, C173, C2092, C2100, C2101, C2102, C2103, C2104,
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PCB CO-LAYOUT

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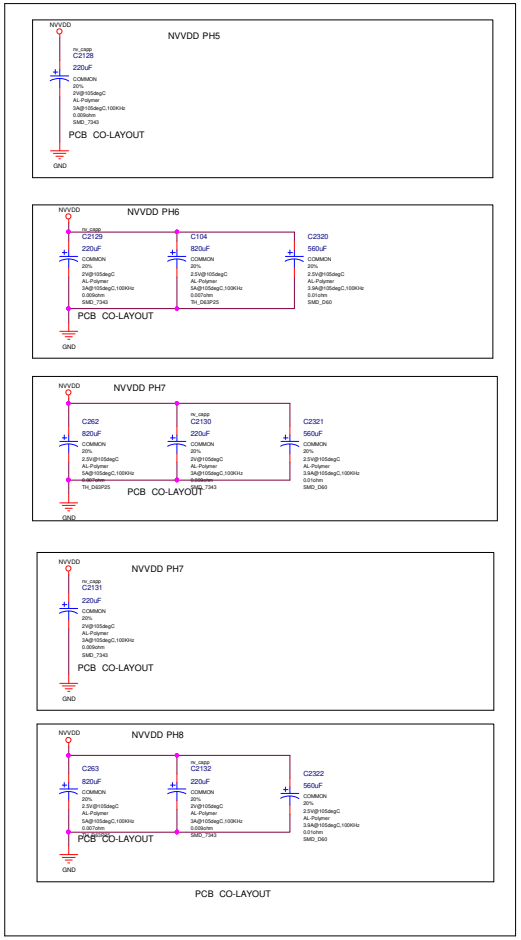

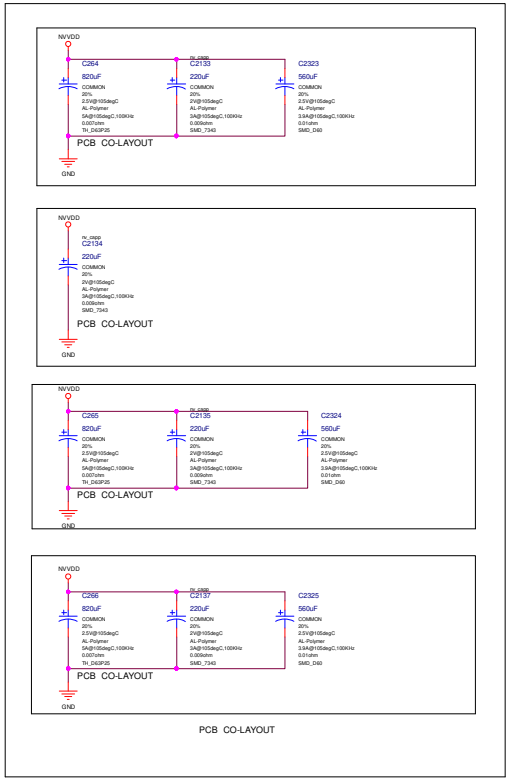

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PS: INPUT SWITCH RTD3

AND GATE LOGIC FOR P-BOARD

GPIO1	GPIO23	SWITCH	VOUT
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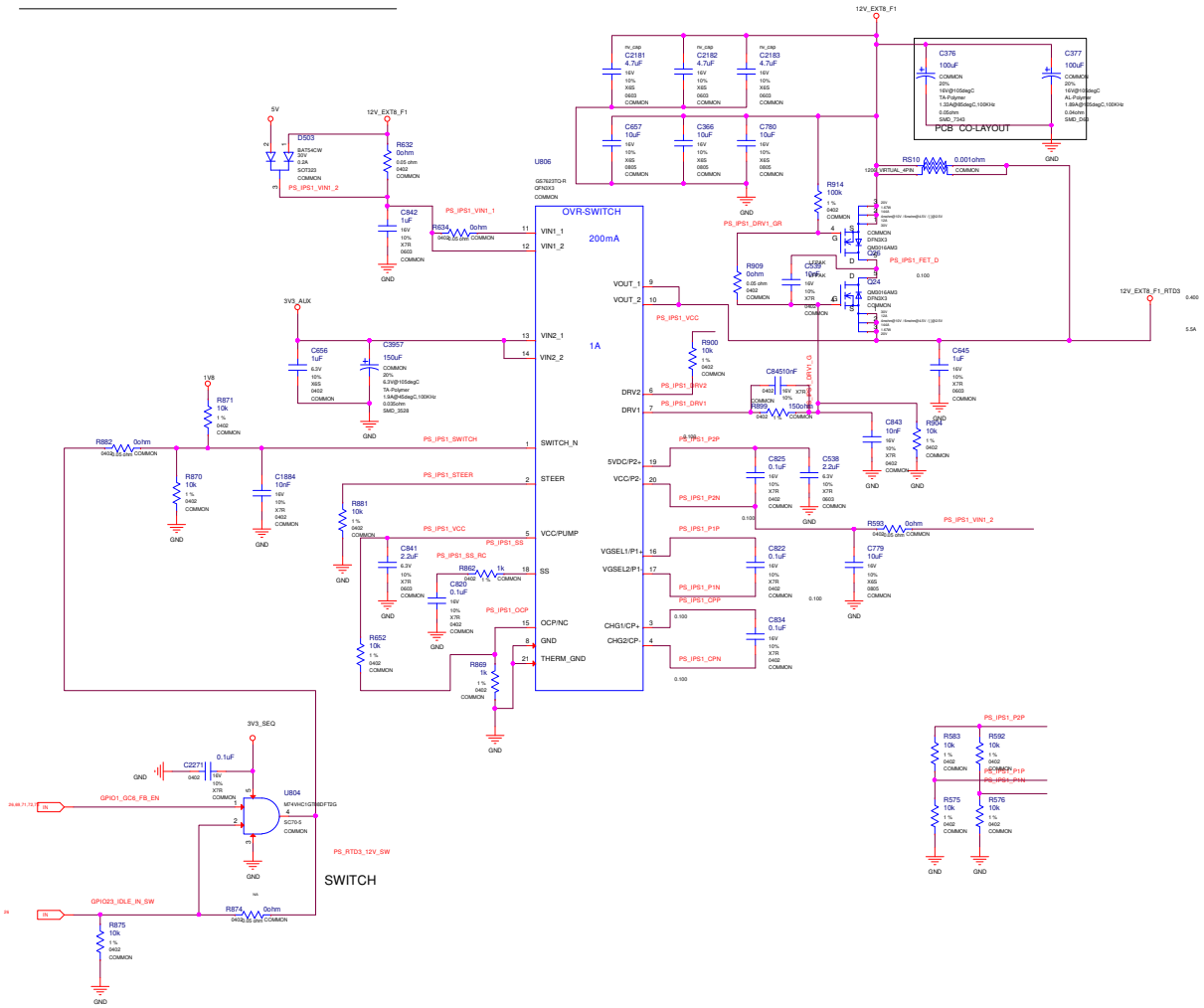
0	1	0	12V_F
1	0	0	12V_F
1	1	1	3V3A



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PAGE DETAIL	PS: INPUT SWITCH RTD3

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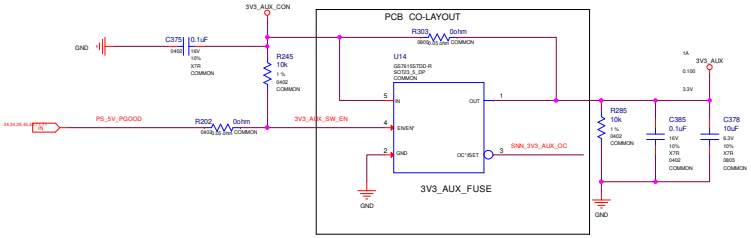
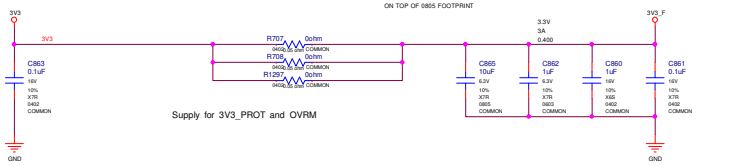


PEX 3V3 INPUT - 10W



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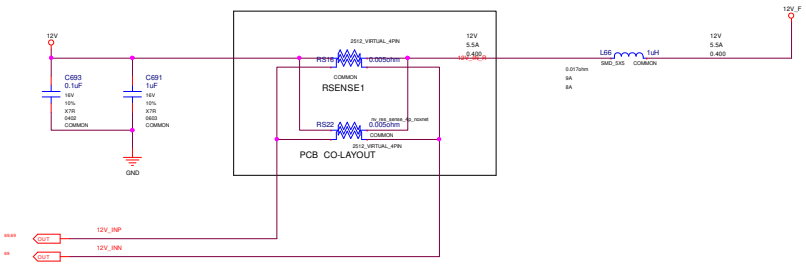

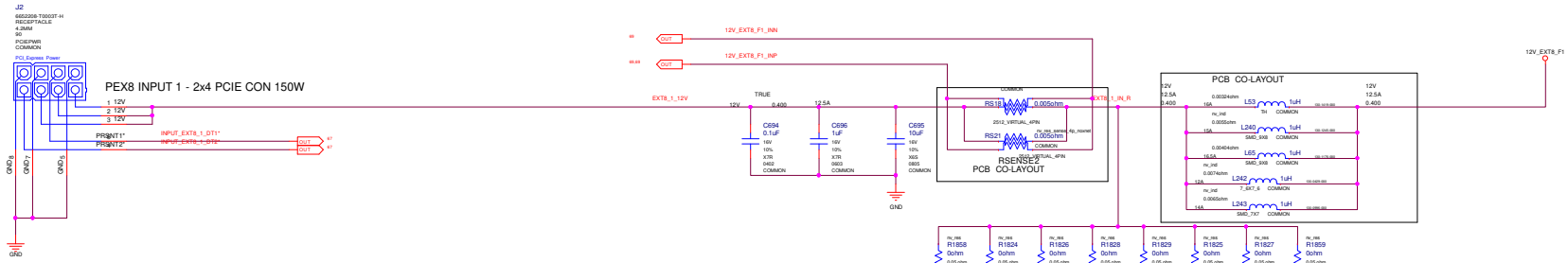

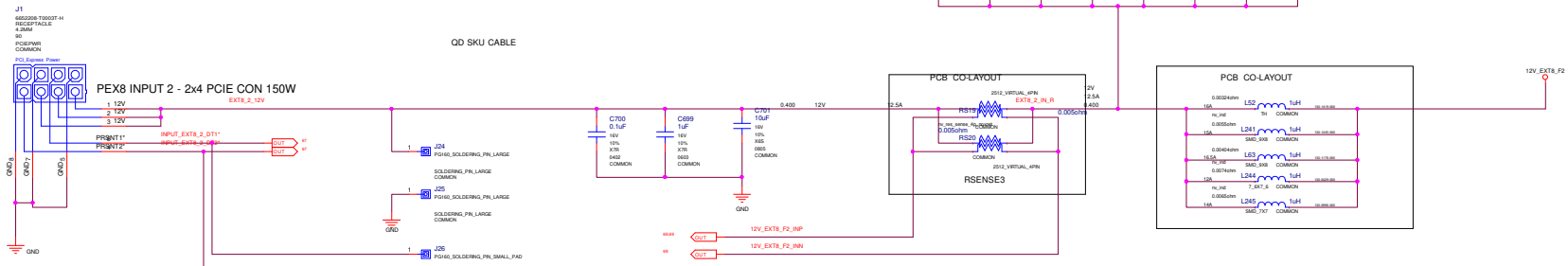

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PAGE_DETAIL	PS: INPUTS, FILTERING, and, MONITORING

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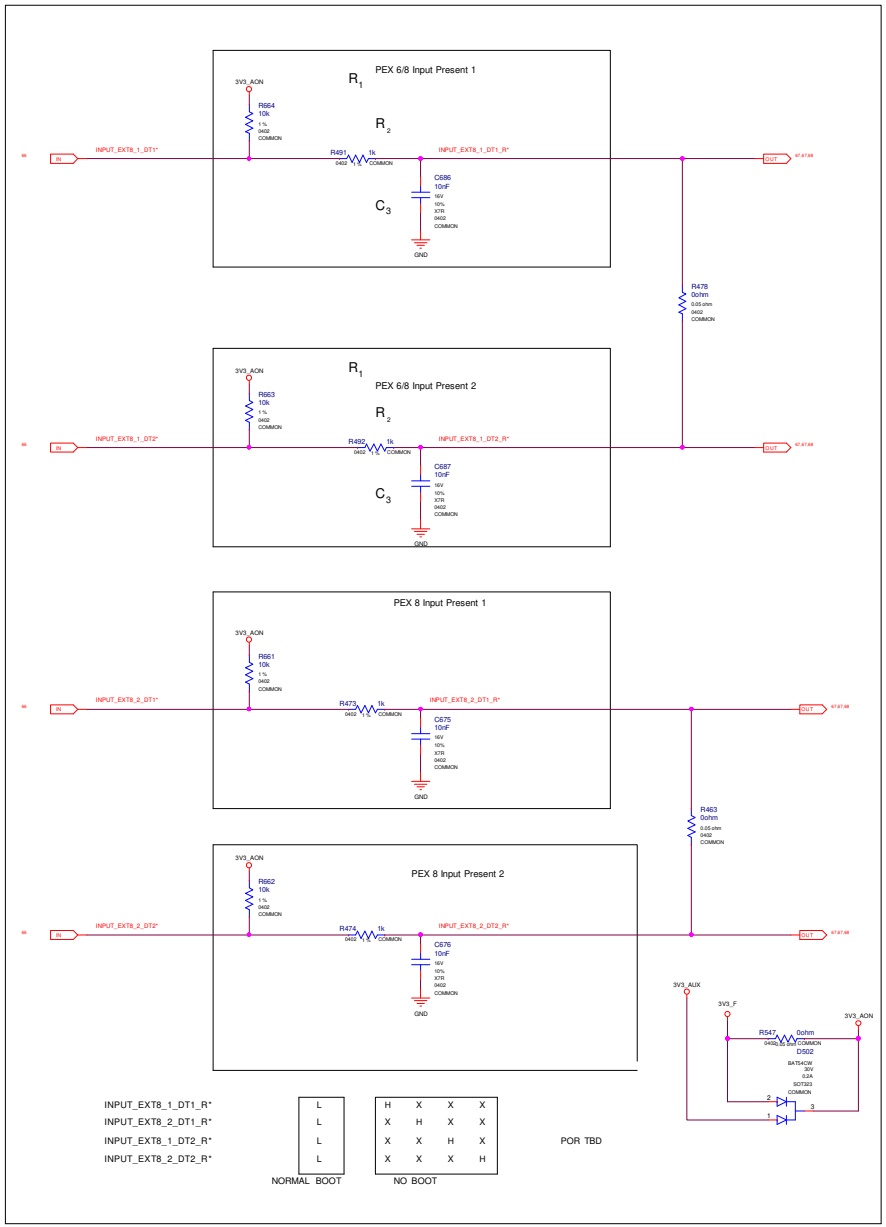
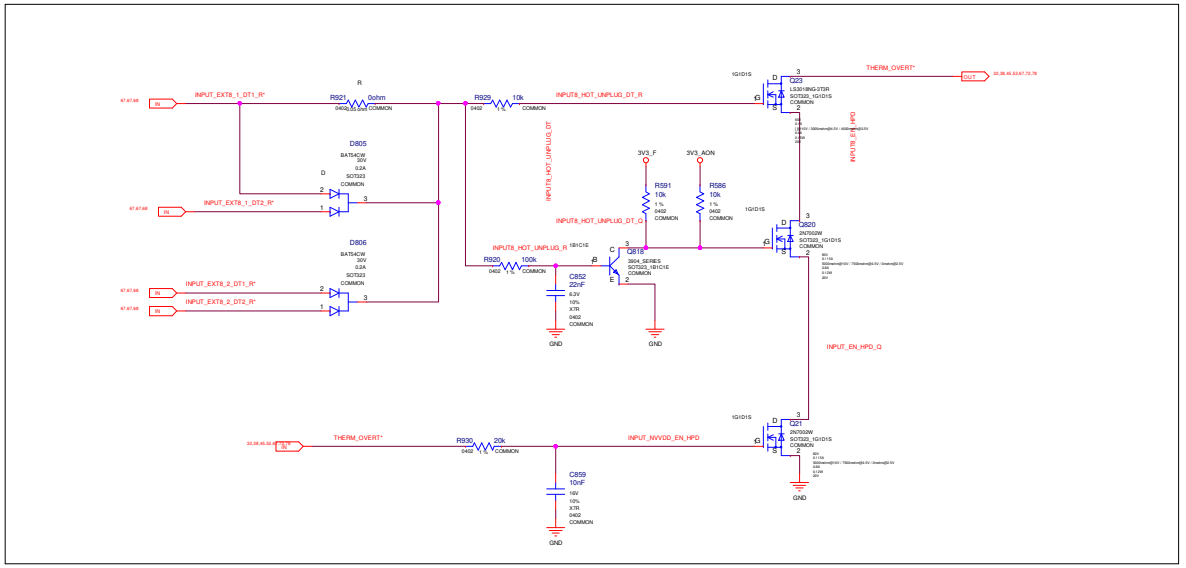
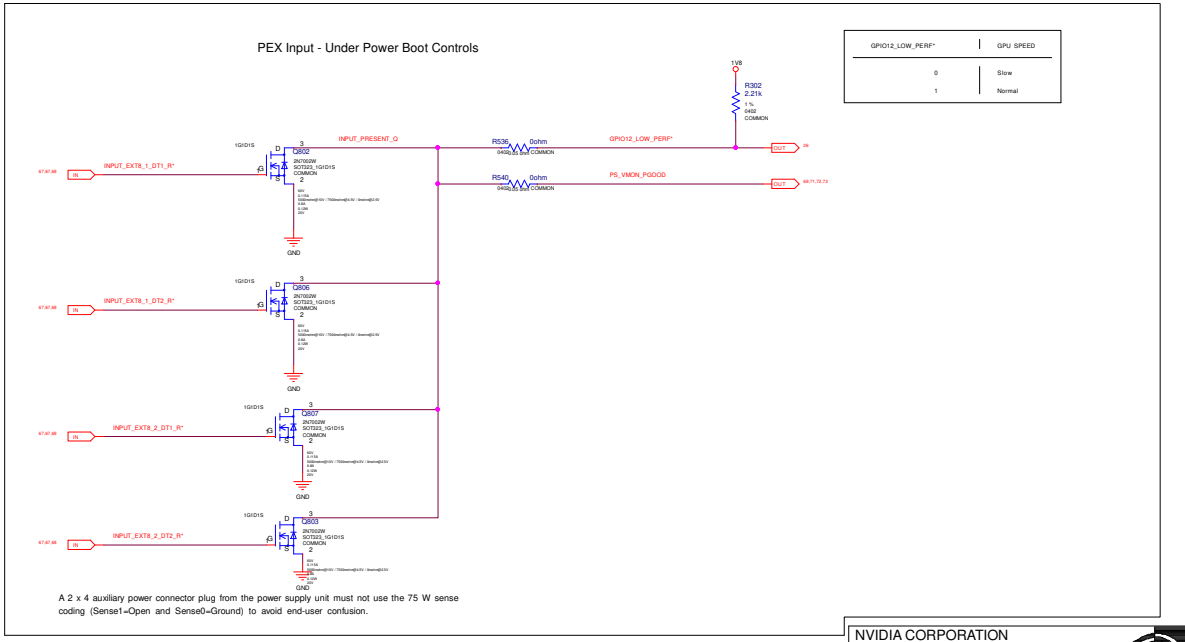
PS: 12V Current Steering & Hot Unplug Detect







ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE_DETAIL	PS: HOT UNPLUG

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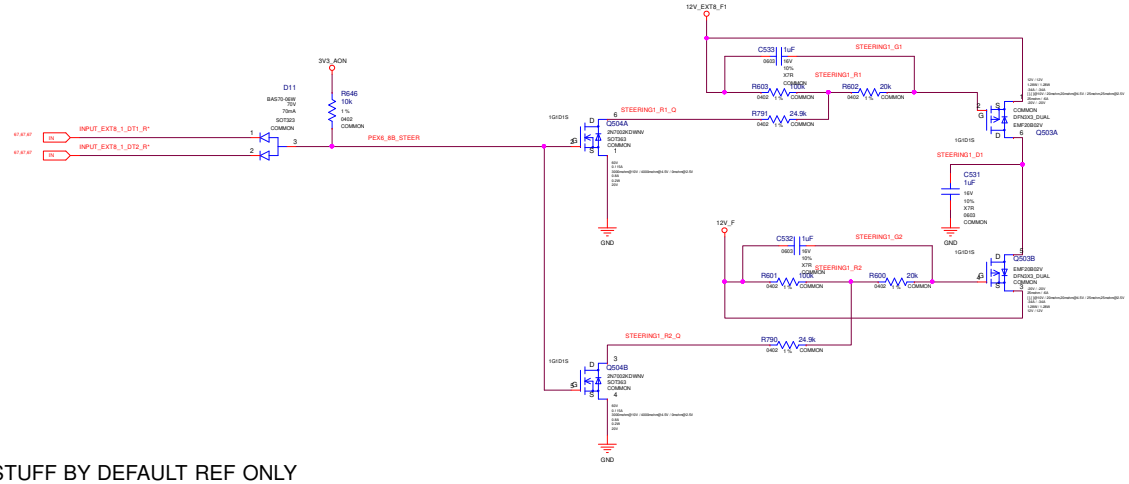
PS: Discrete Steering

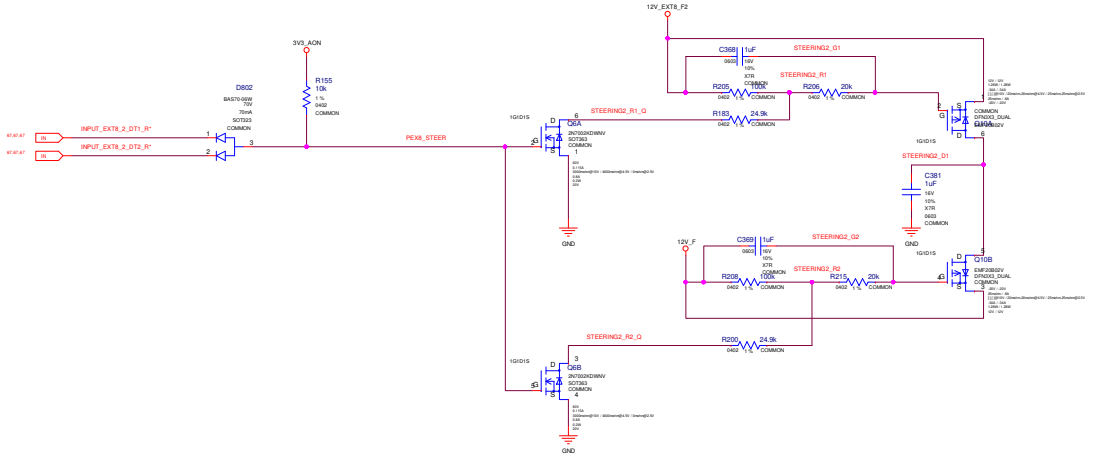
12V CURRENT STEERING (UNDER POWER BOOT):

PEX12V AND 12V_EXT8_F1



NO STUFF BY DEFAULT REF ONLY

PEX12V AND 12V_EXT8_F2



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE_DETAIL	PS: Discrete Power Steering

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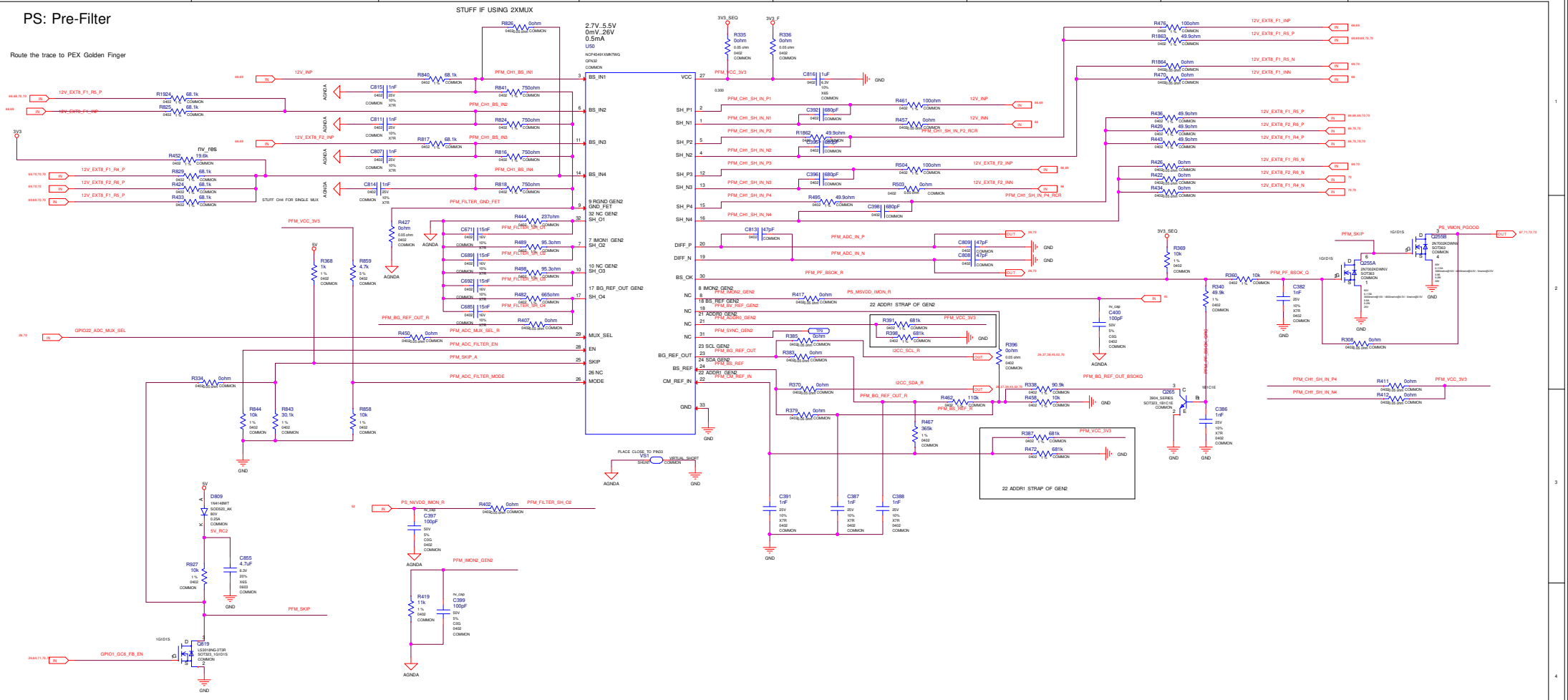
PS: Pre-Filter

Route the trace to PEX Golden Finger



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PREFILTER

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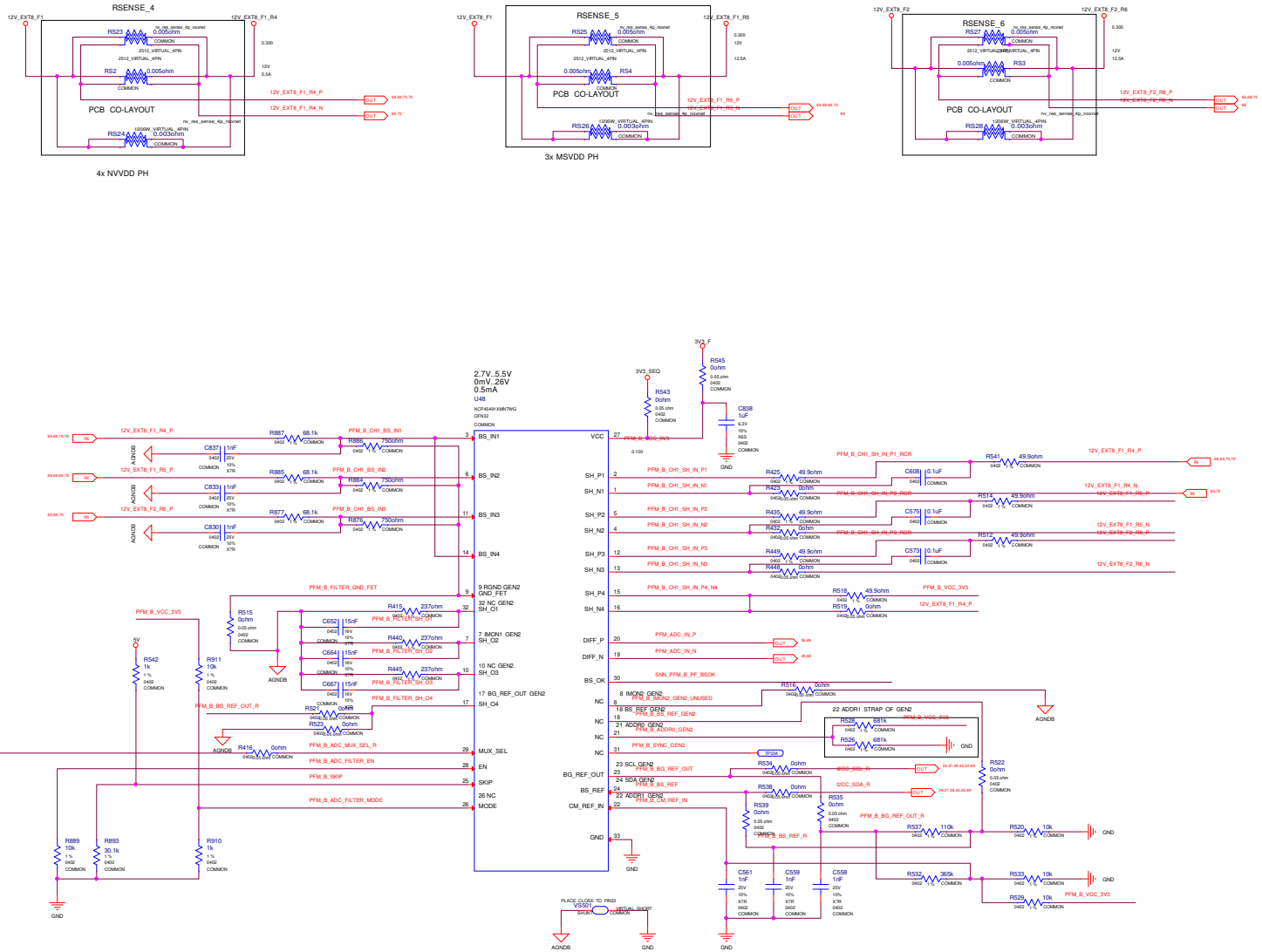
PS: Pre-Filter B



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	PS: PREFILTER B

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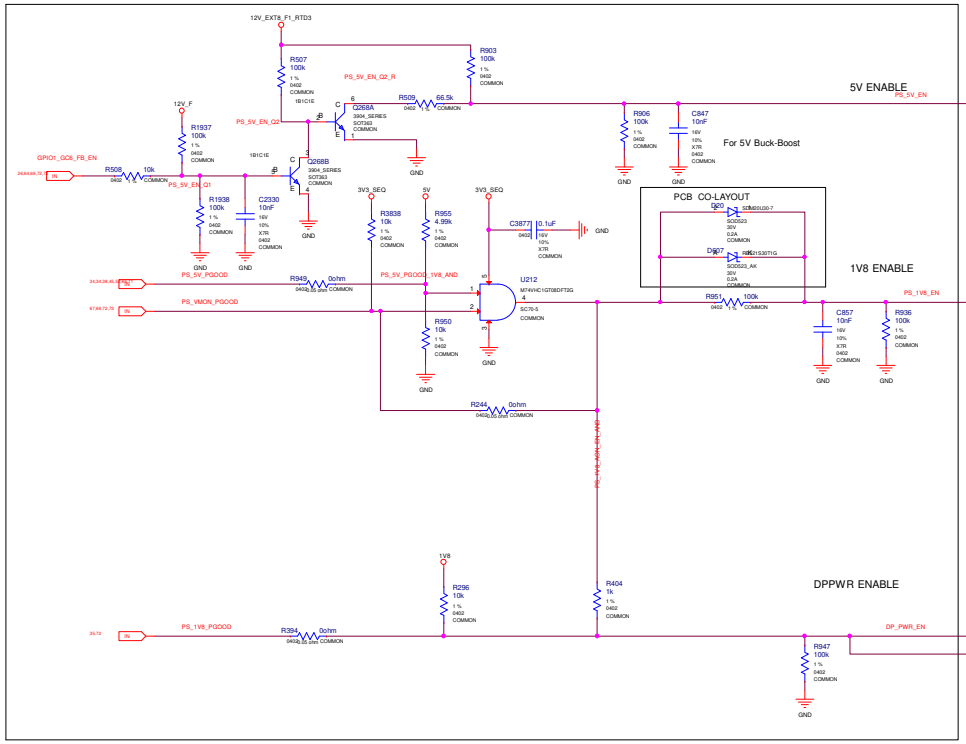
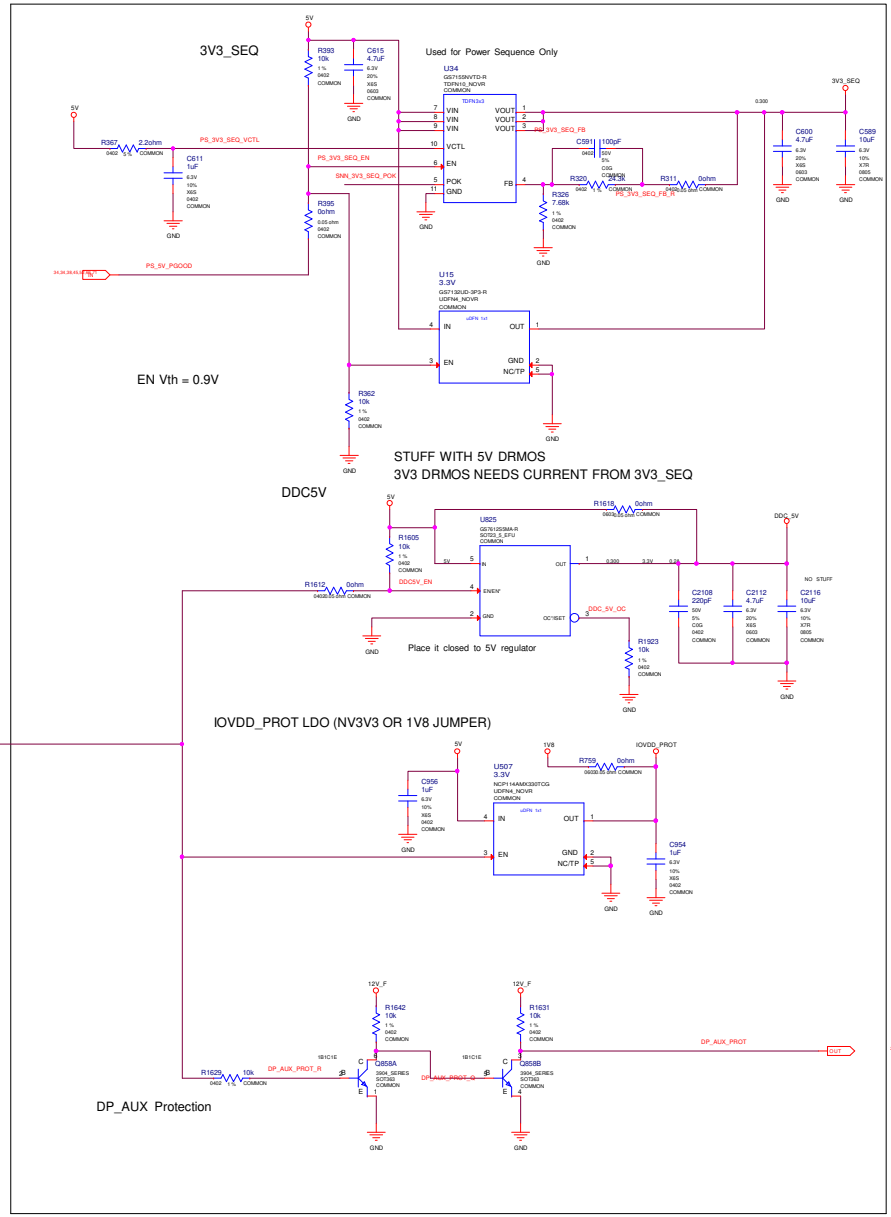
SEQUENCE:5V,1V8,3V3_SEQ ENABLE





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PAGE DETAIL	Sequence: 5V, 1V8, 3V3_SEQ

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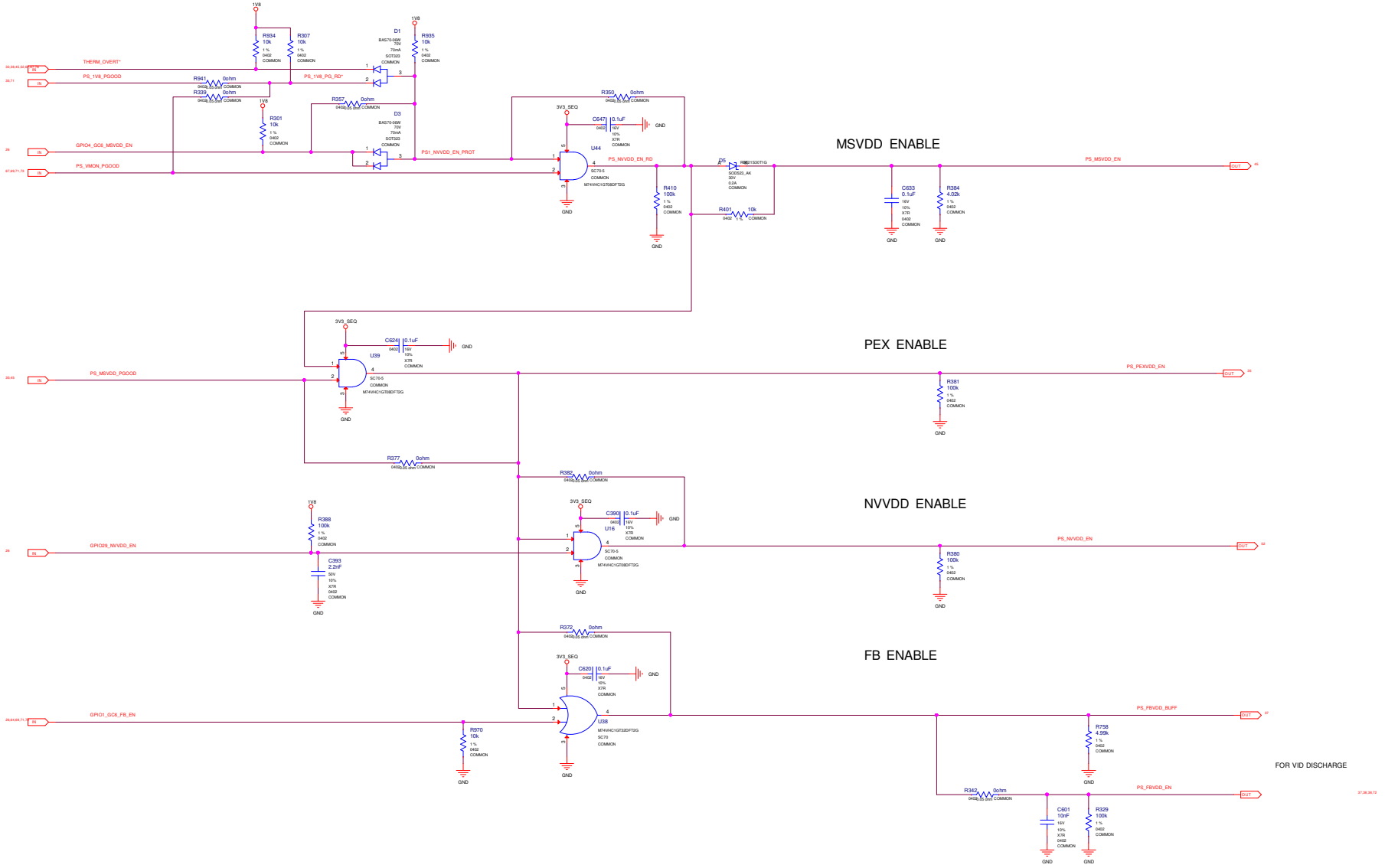
SEQUENCE:NV,PEX,FB ENABLE



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Sequence: NV, PEX, FB EN

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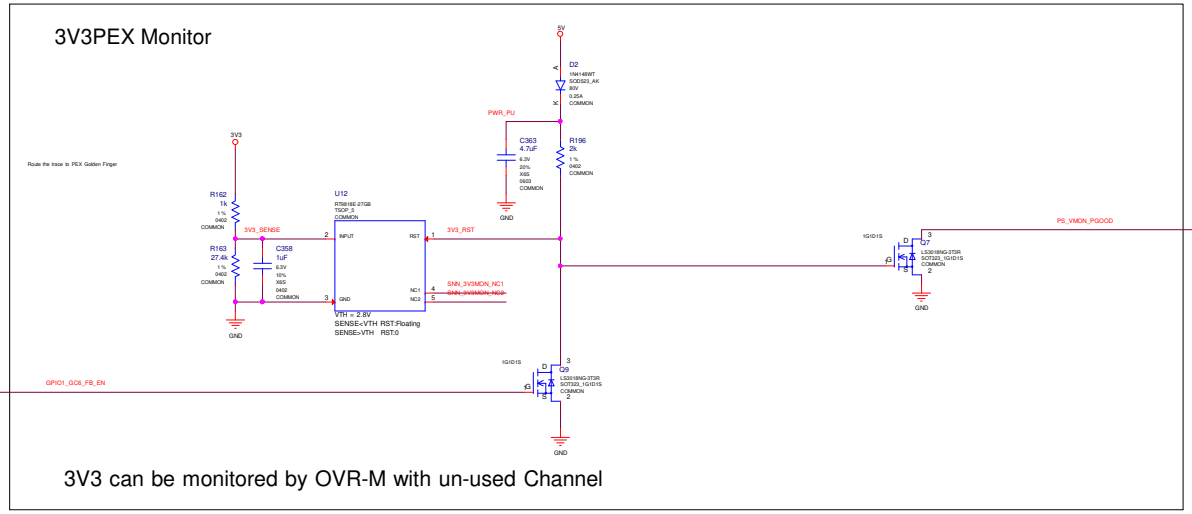
Sequence: 3V3 MONITOR



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	Sequence: 3V3 MONITOR

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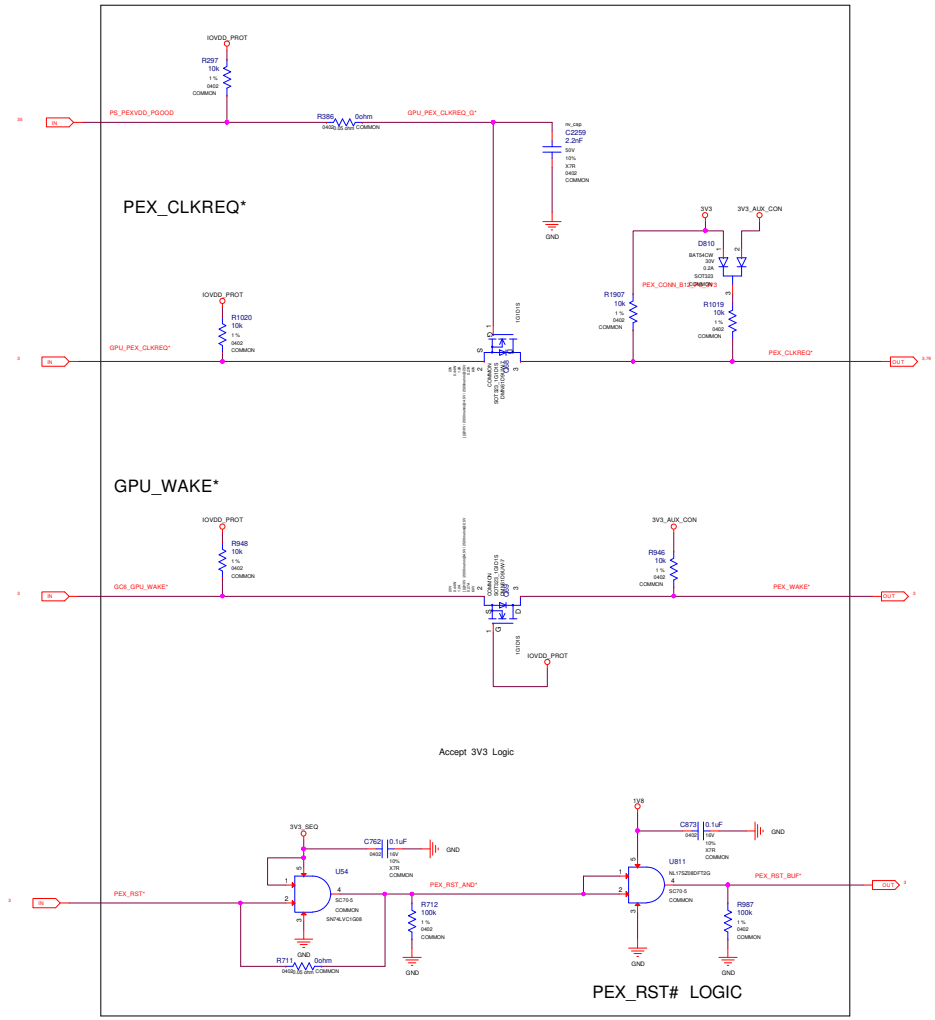
SEQUENCE:MISC



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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE_DETAIL	Sequence: MISC

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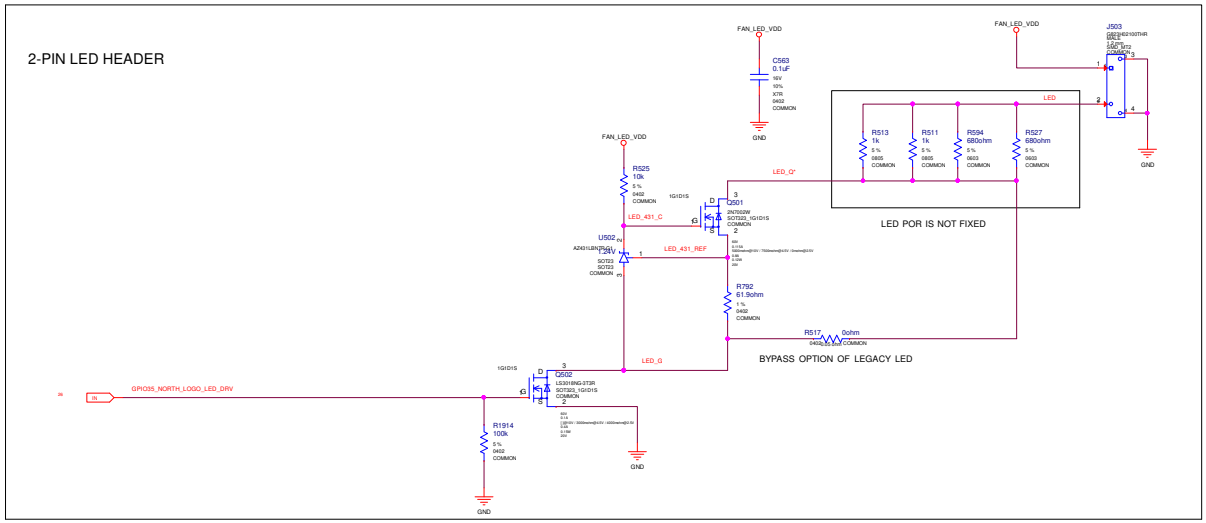
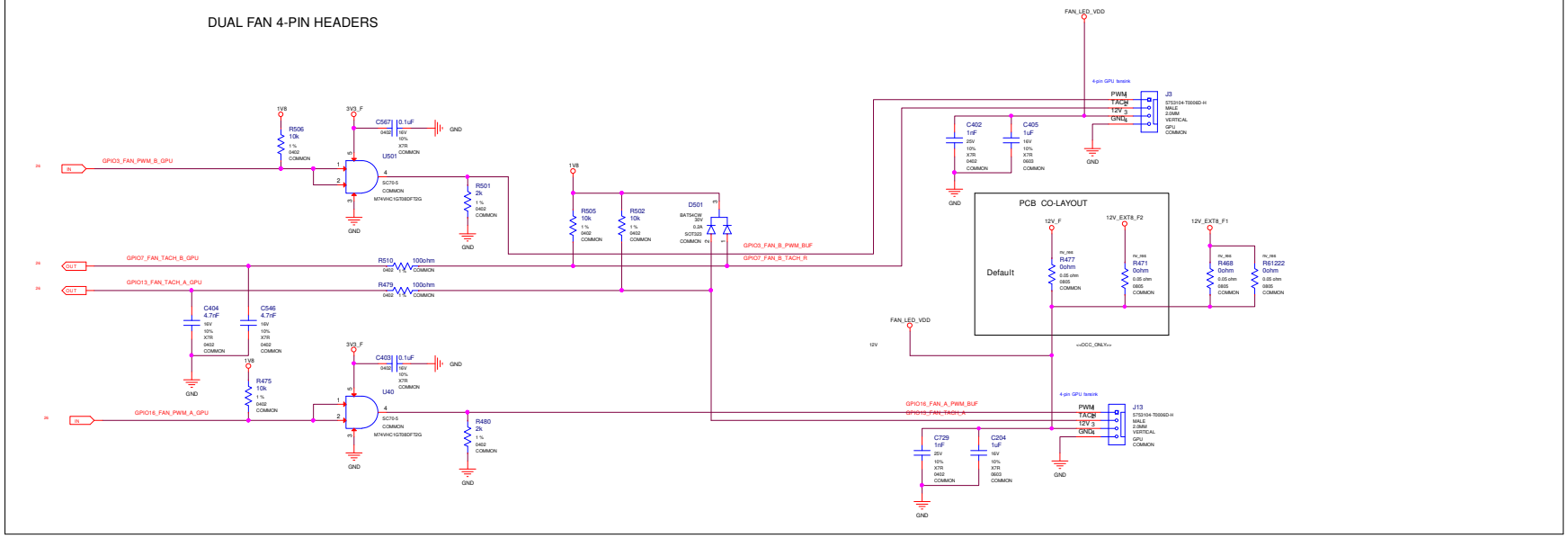
MISC: LED & FAN

2-PIN LED HEADER



DUAL FAN 4-PIN HEADERS



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE_DETAIL	MISC: LED & FAN

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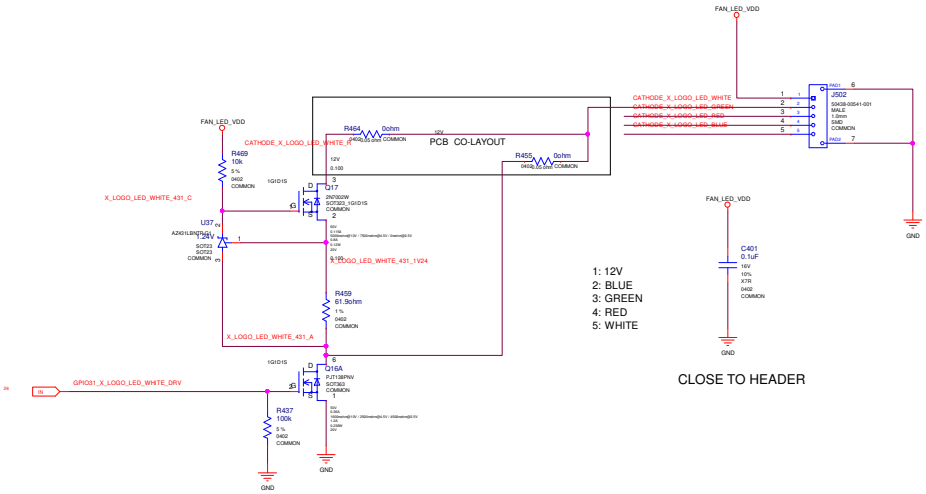
MISC: RGBW LED REF

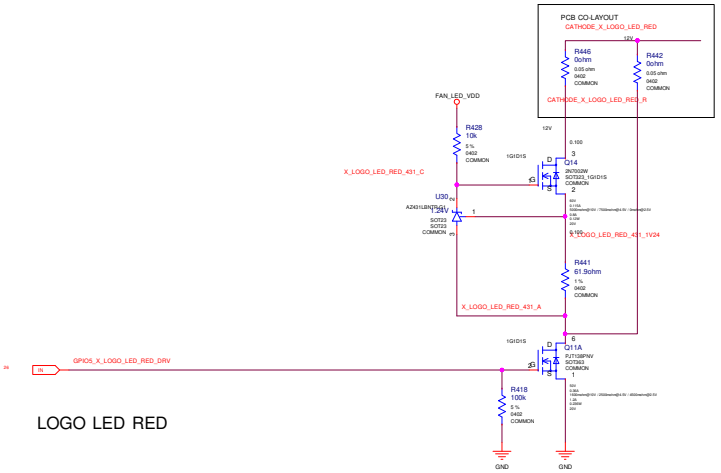


1: 12V
2: BLUE
3: GREEN
4: RED
5: WHITE

CLOSE TO HEADER

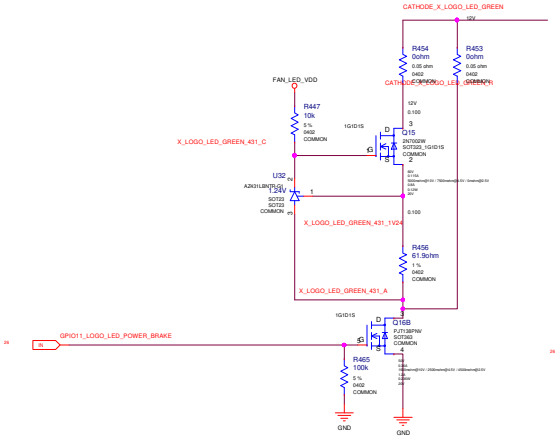
CONNECTOR SIZE TO FIT LAYOUT
ALL CIRCUIT NO STUFF BY DEFAULT
ALIGN WITH PASH
IF ADDTIONAL POWER CONSUPTION R NEEDED, IT SHOULD BE ON LED MOD.

WHITE DRIVE

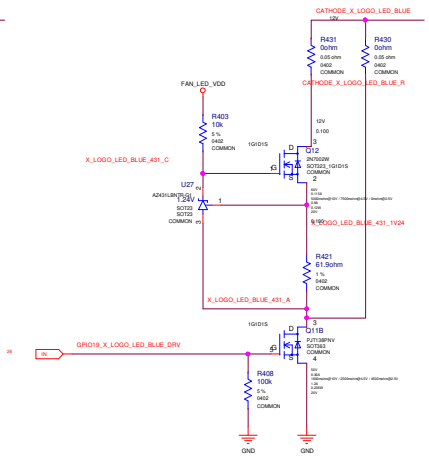


LOGO LED RED

RED DRIVE



GREEN DRIVE



BLUE DRIVE

ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	RGBW LED REF

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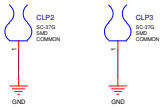
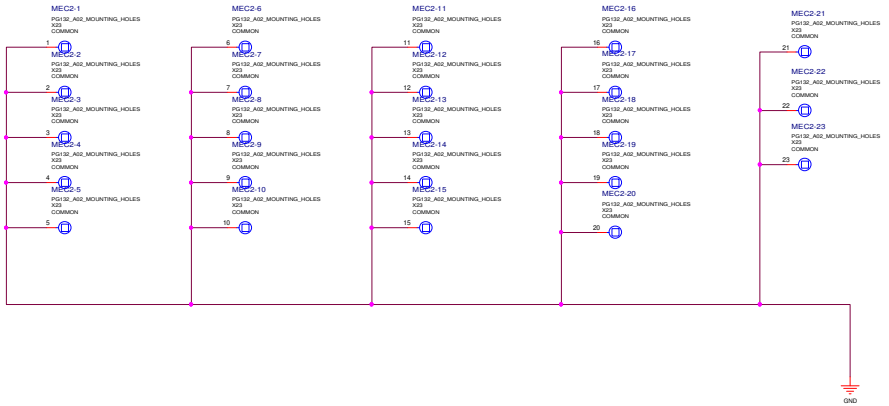
Mechanical: Mounting holes





ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	MECH

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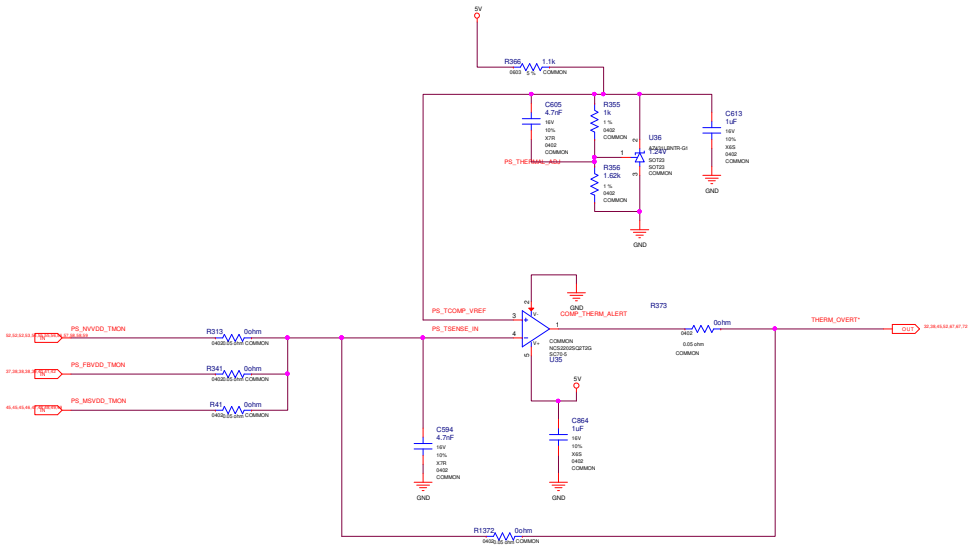
VR THERMAL PROTECTION



ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE_DETAIL	VR Thermal Protection

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PCI TERM

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE_DETAIL	PCIE_TERM

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