

PG141-H00

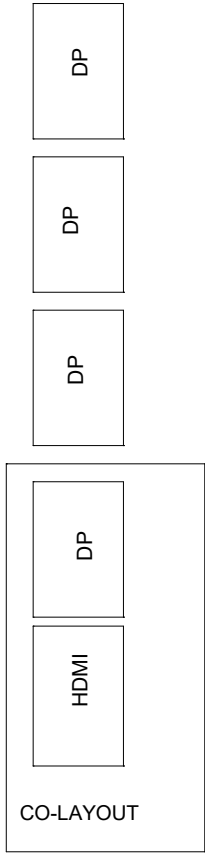
GA104/NP GB5/5B-256 DESIGN, 16GB GDDRx, 256b, X16
DP + DP + DP + HDMI/DP

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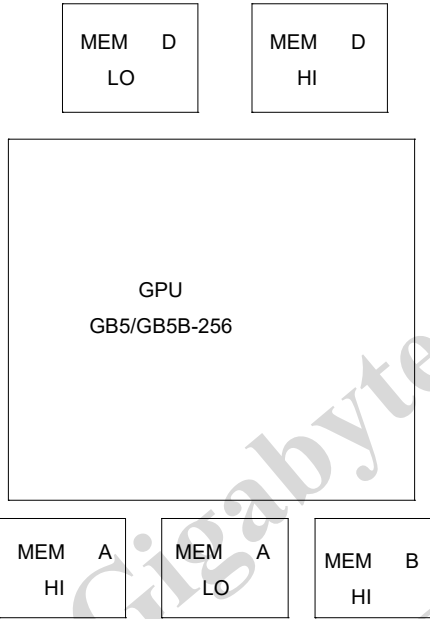
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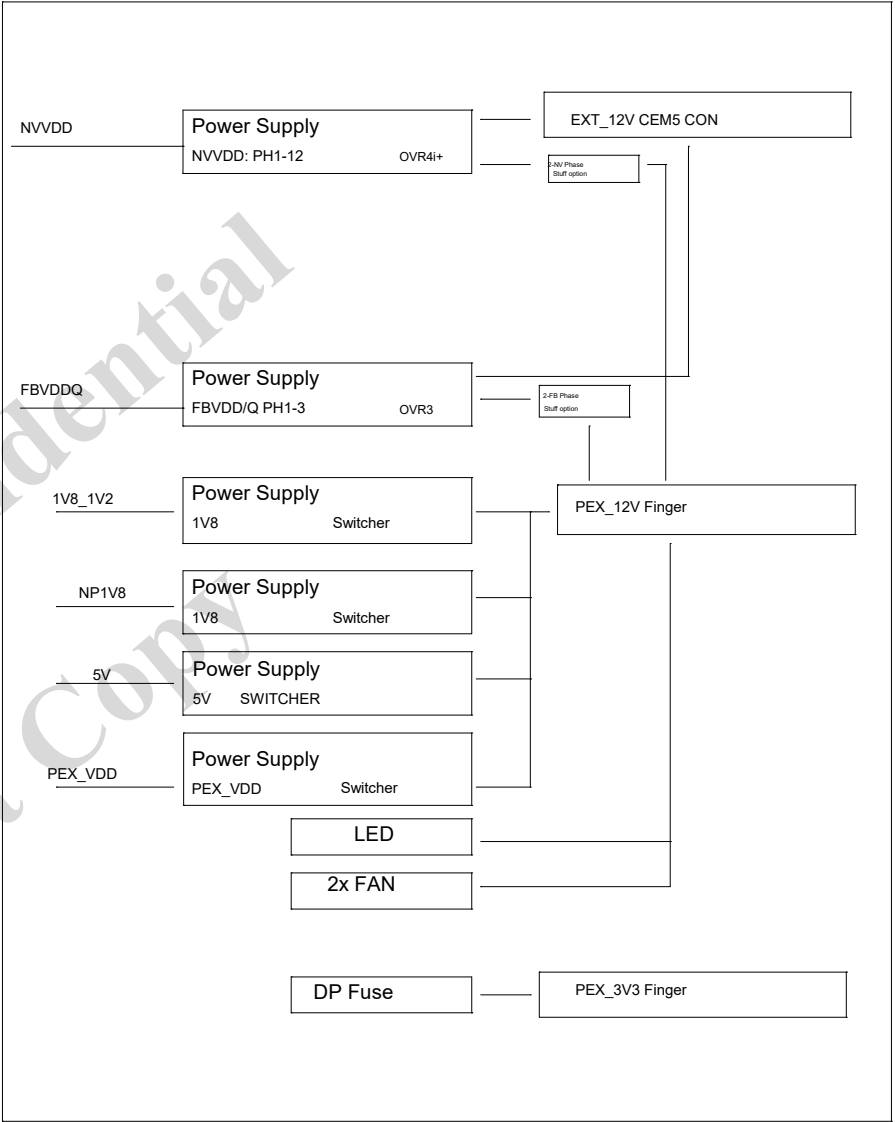
Block Diagram



NV POWER SUPPLY



FB POWER SUPPLY



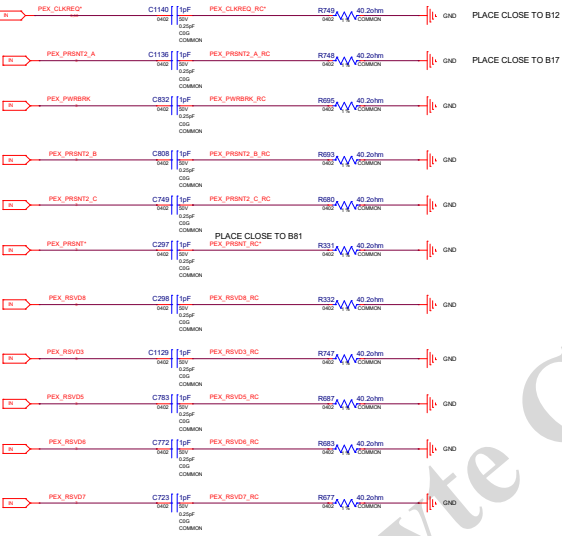
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ASSEMBLY
PAGE DETAIL

ASSEMBLY DESCRIPTION
BLOCK DIAGRAM

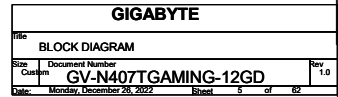
GIGABYTE			
Title			
BLOCK DIAGRAM			
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PCIE GEN4 RC TERMINATIONS

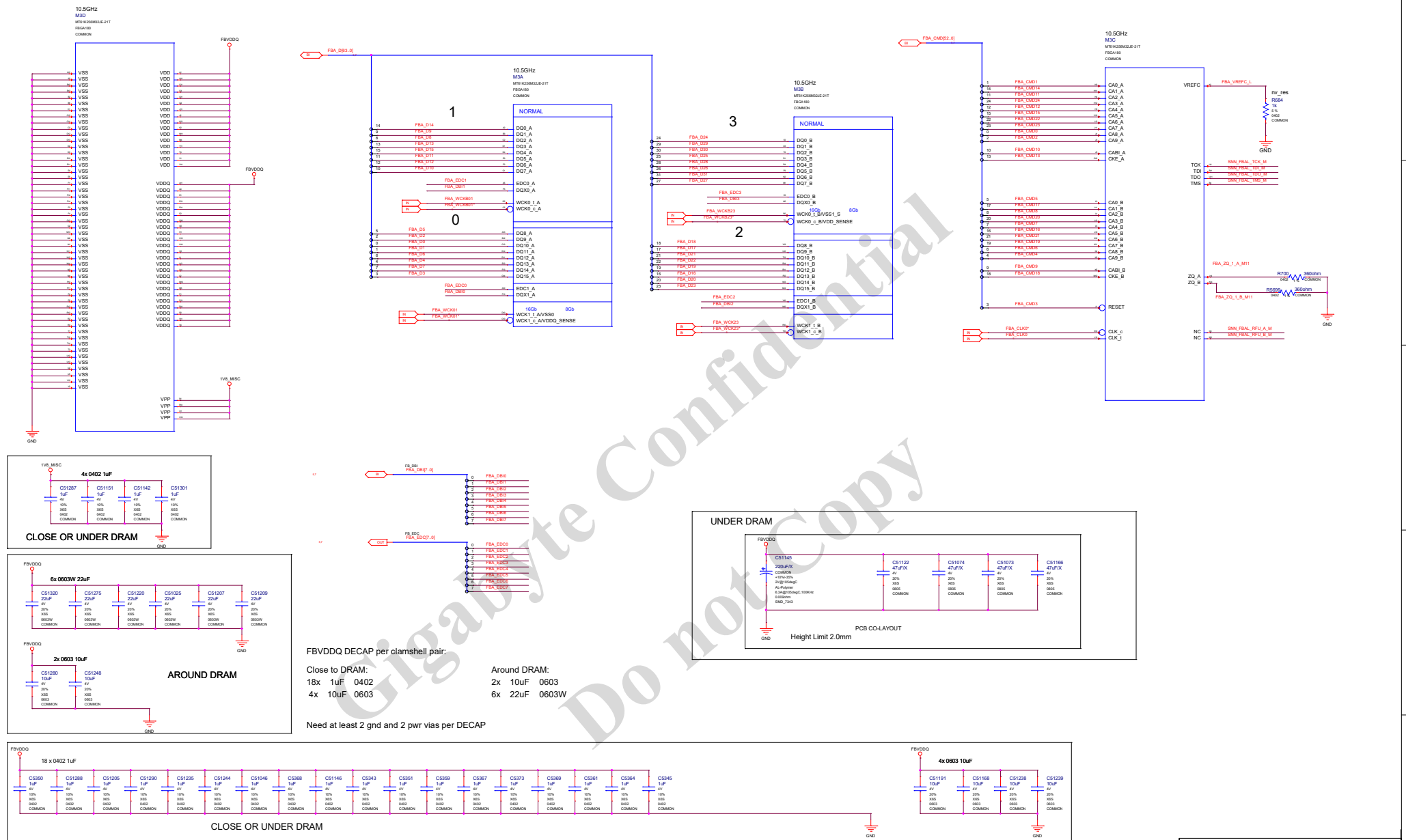


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Title BLOCK DIAGRAM			
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MEMORY: FBA Partition 31..0

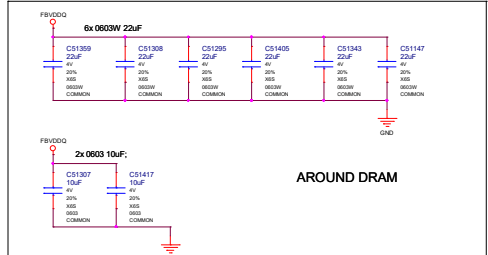
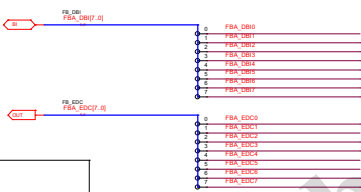
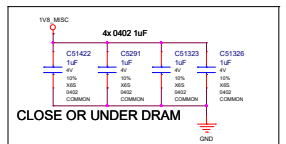
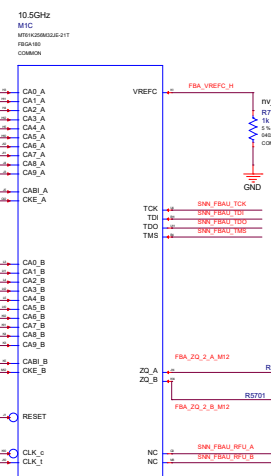
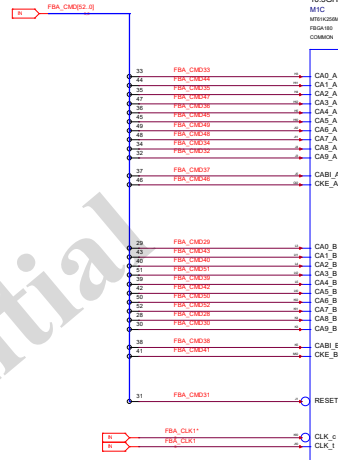
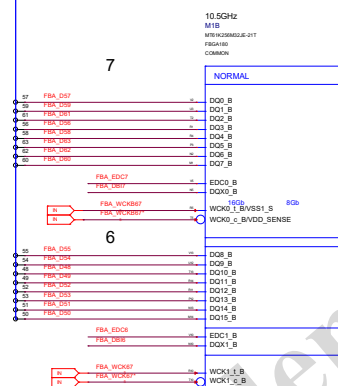
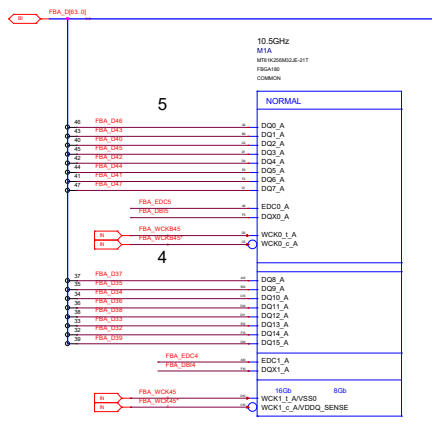
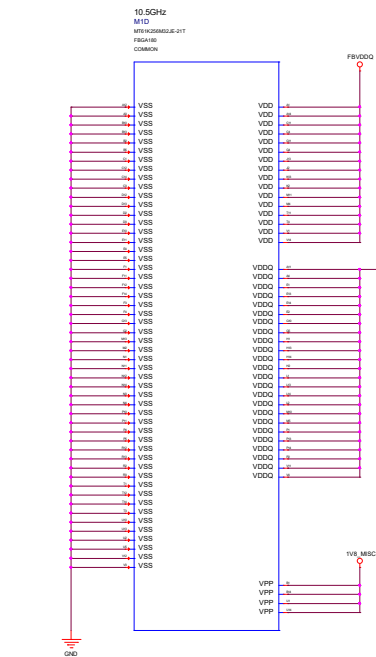


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ASSEMBLY PAGE DETAIL
 ASSUMES: DESIGNER/PCB LAYOUT ONLY
 MEMORY: FBA(31:0)

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MEMORY: FBA Partition 63..32

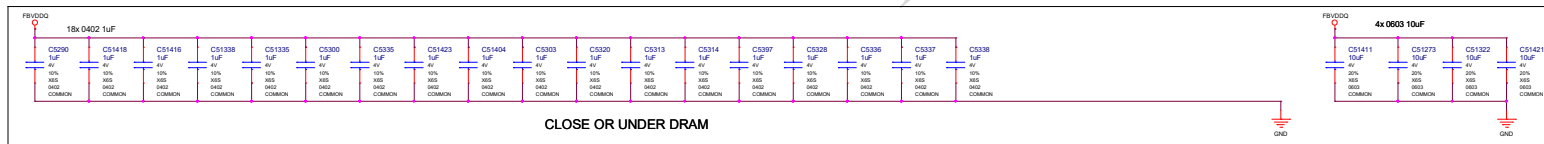


FBVDDQ DECAP per clamshell pair:

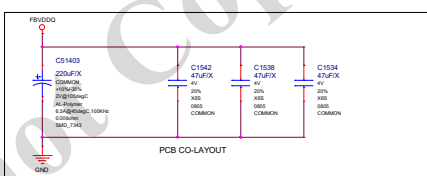
Close to DRAM:
18x 1uF 0402
4x 10uF 0603

Around DRAM:
2x 10uF 0603
6x 22uF 0603W

Need at least 2 gnd and 2 pwr vias per DECAP

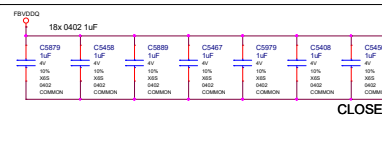
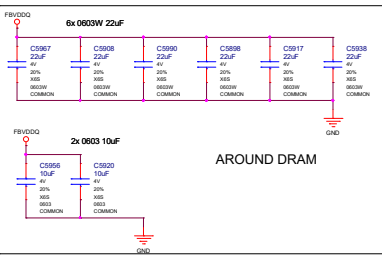
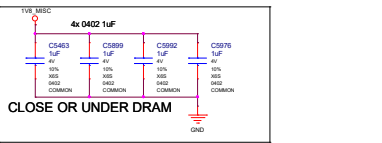


UNDER DRAM



GIGABYTE			
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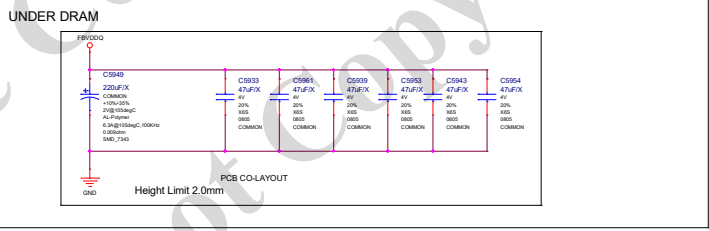
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FBVDDQ DECAP per clamshell pair:

Location	Capacitor Value	Quantity
Close to DRAM:	1uF 0402	18x
Around DRAM:	10uF 0603	2x
	22uF 0603W	6x

Need at least 2 gnd and 2 pwr vias per DECAP

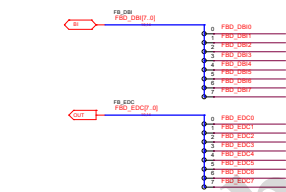
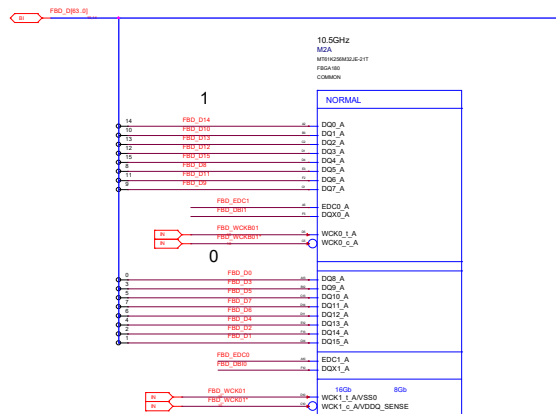
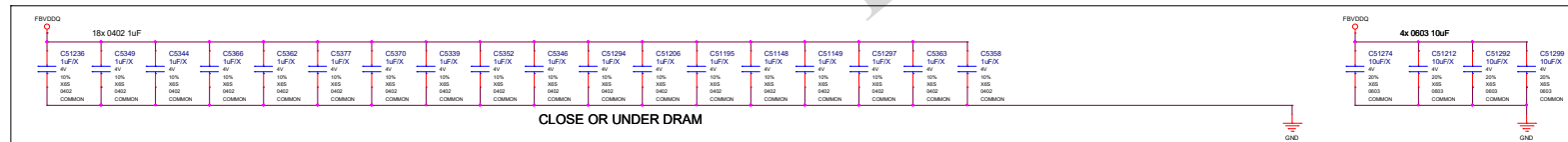
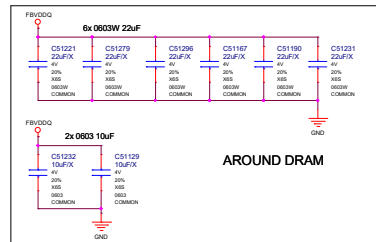
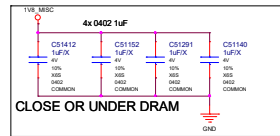
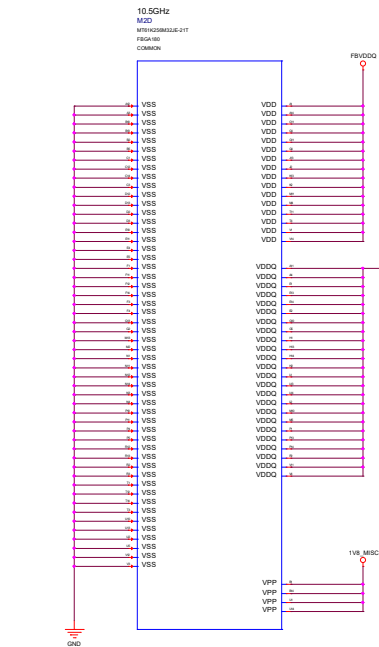


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ASSEMBLY PAGE DETAIL
MEMORY: FBC[31:0]

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File	BLOCK DIAGRAM		
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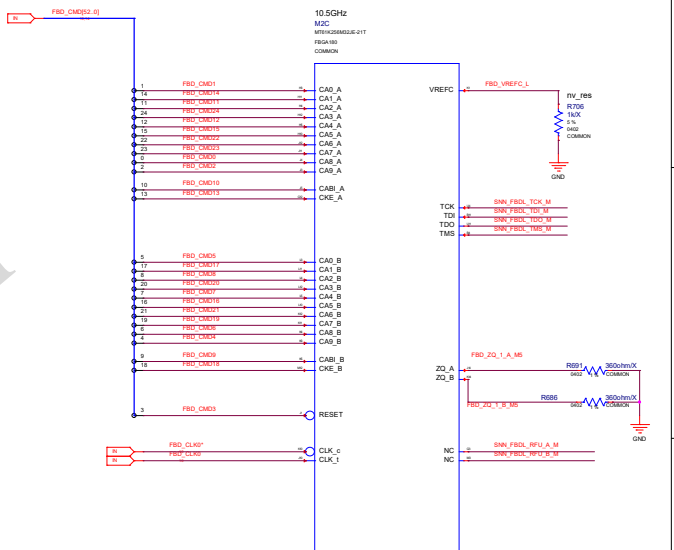
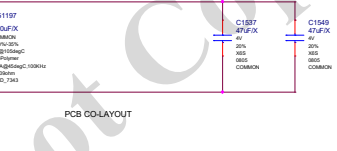
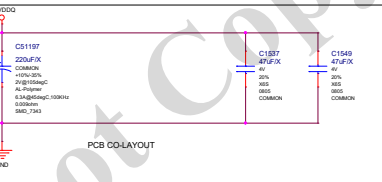
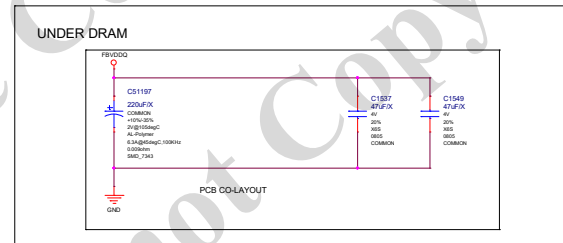
MEMORY: FBD Partition 31..0



FBVDDQ DECAP per clamshell pair:

Close to DRAM: 18x 1uF 0402 4x 10uF 0603
Around DRAM: 2x 10uF 0603 6x 22uF 0603W

Need at least 2 gnd and 2 pwr vias per DECAP

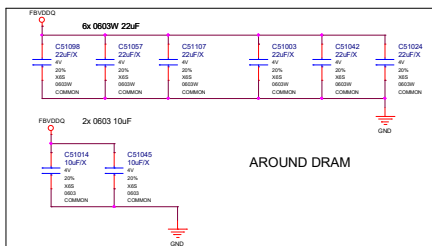
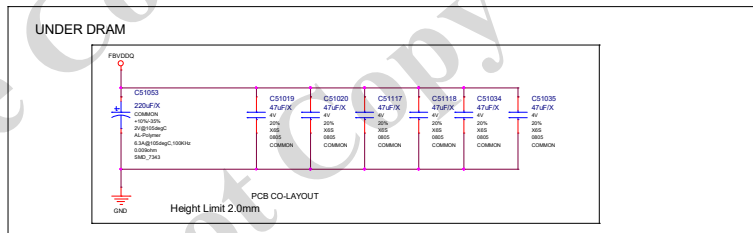
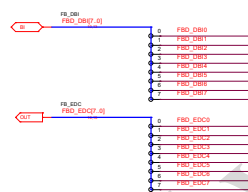
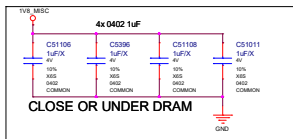
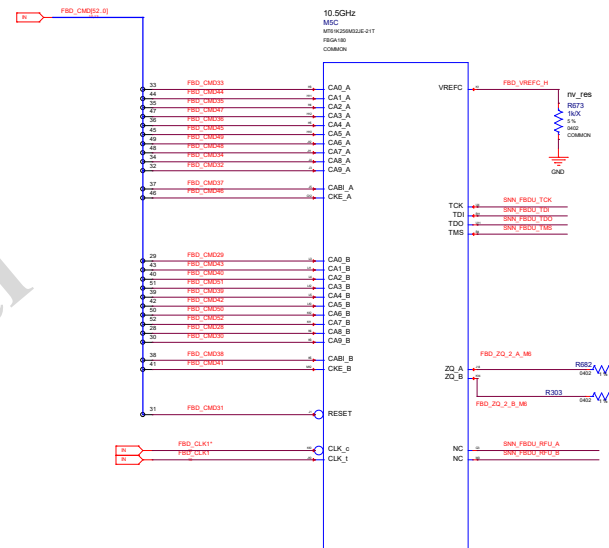
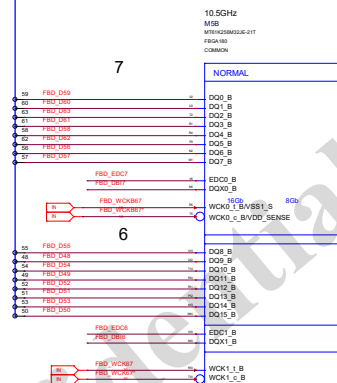
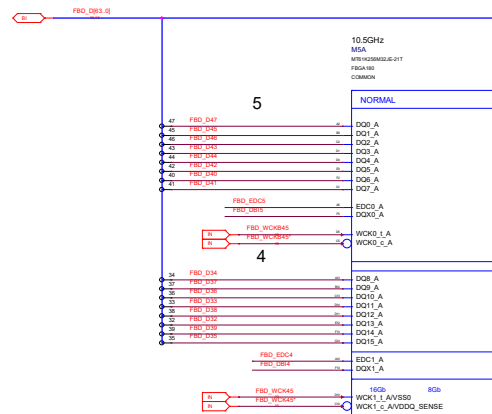
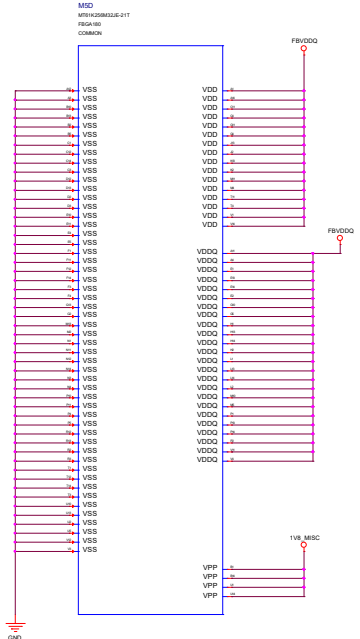


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ASSEMBLY PAGE DETAIL
MEMORY: FBD(31..0)

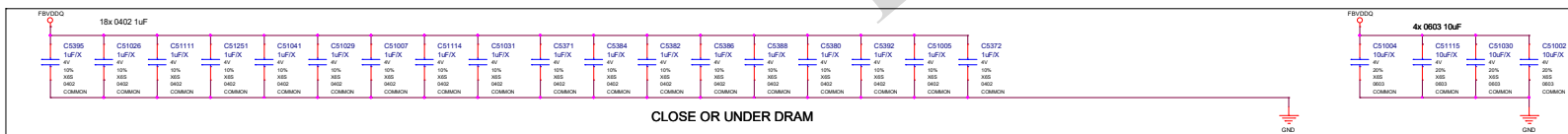
MEMORY: FBD Partition 63..32



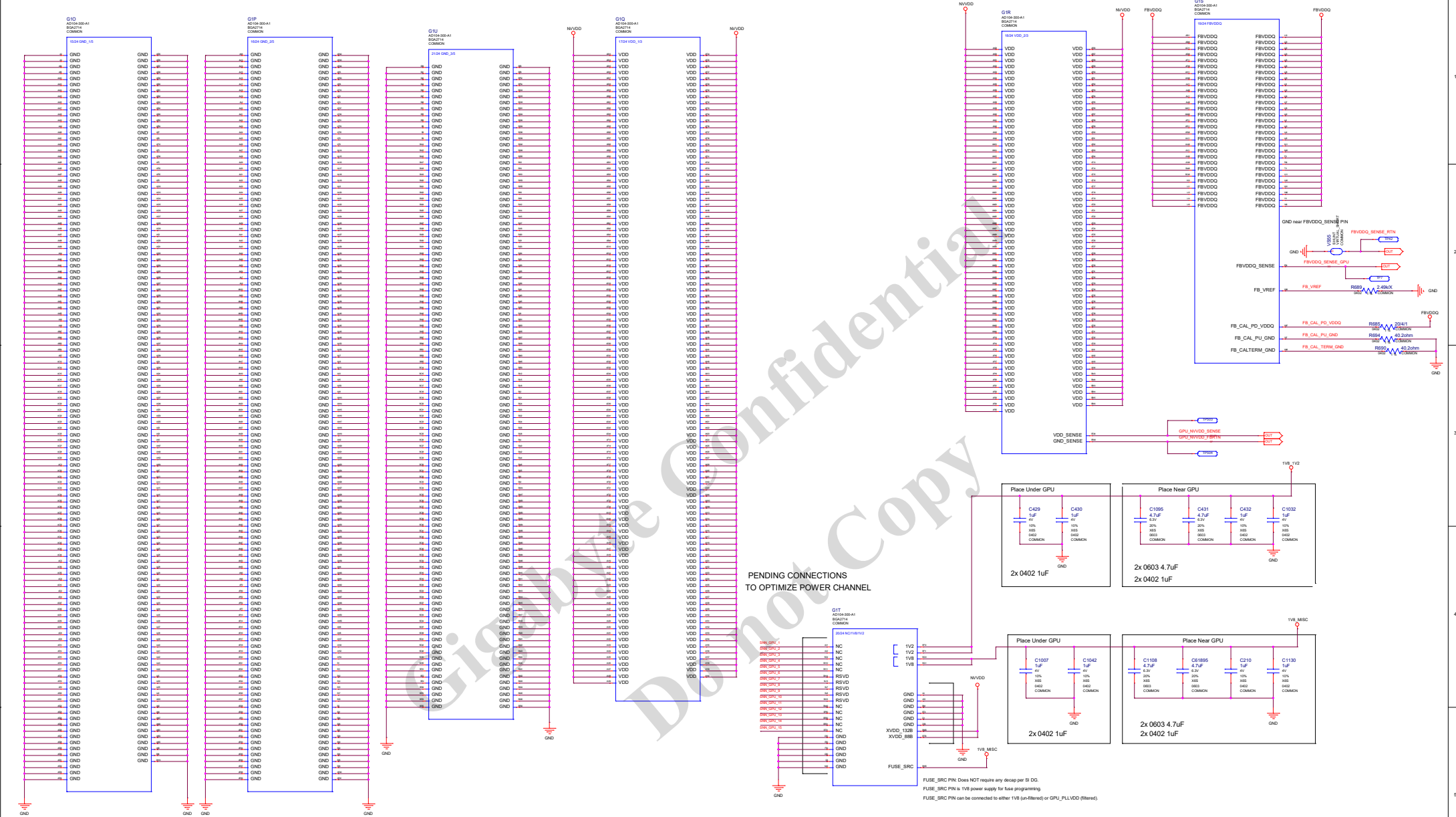
FBVDDQ DECAP per clamshell pair:

Close to DRAM:	Around DRAM:
18x 1uF 0402	2x 10uF 0603
4x 10uF 0603	6x 22uF 0603W

Need at least 2 gnd and 2 pwr vias per DECAP



GPU PWR and GND

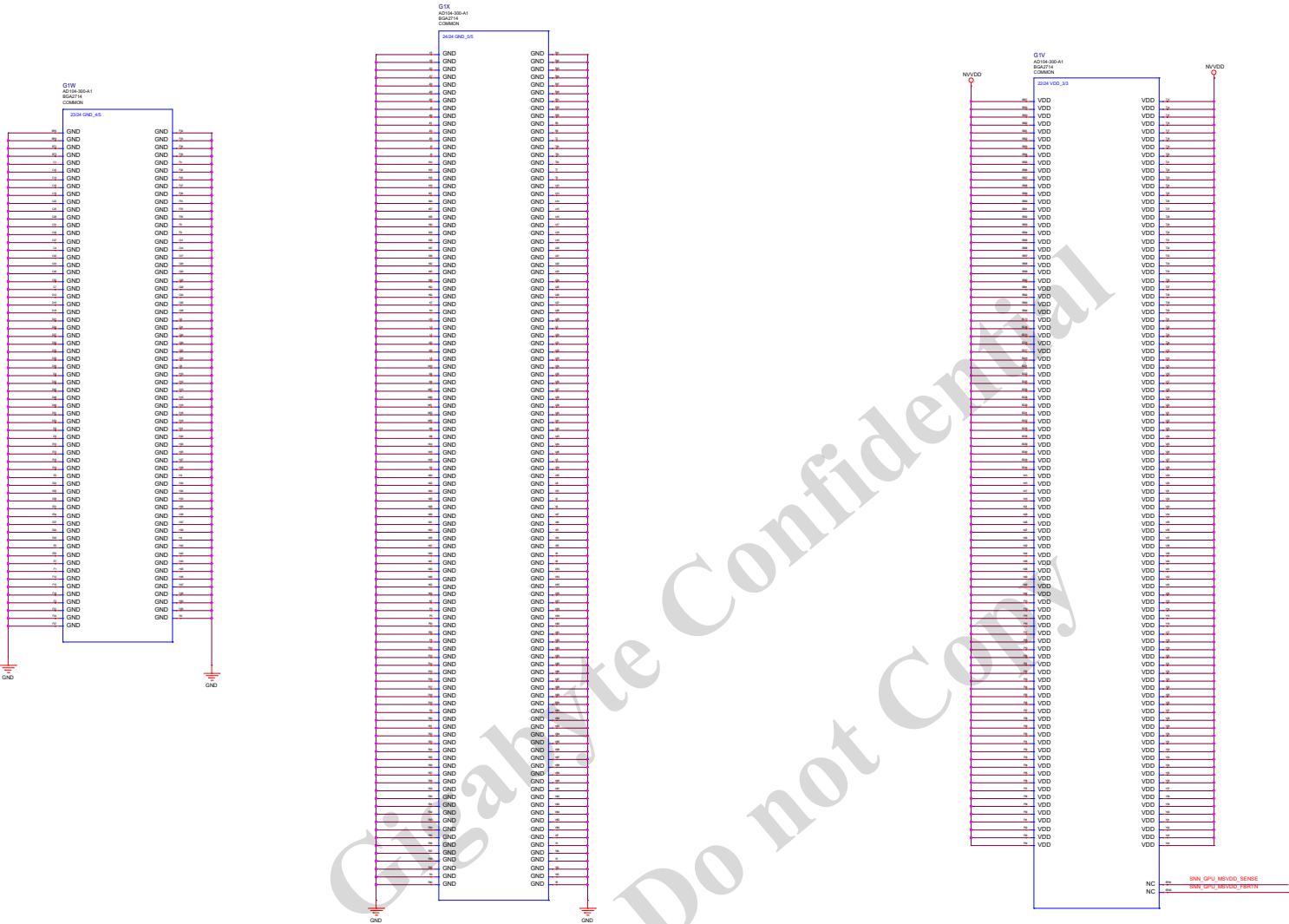


PENDING CONNECTIONS
TO OPTIMIZE POWER CHANNEL

FUSE_SRC PIN: Does NOT require any decap per SI DG.
FUSE_SRC PIN is 1V8 power supply for fuse programming.
FUSE_SRC PIN can be connected to either 1V8 (un-filtered) or GPU_PL1VDD (filtered).

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BLOCK DIAGRAM			
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GPU PWR and GND 2



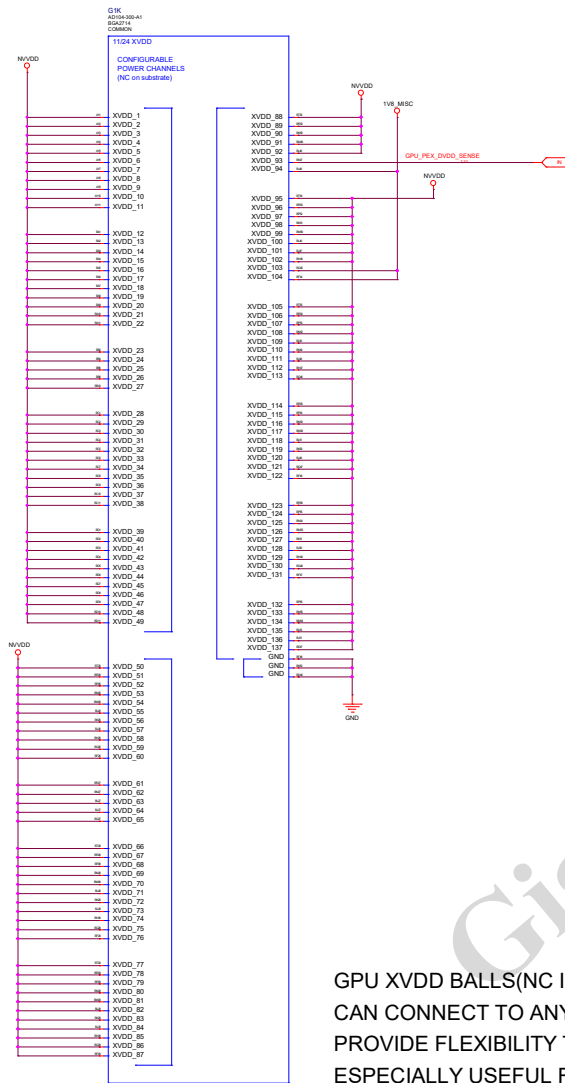
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ASSEMBLY
PAGE DETAIL

ASSEMBLY DESCRIPTION
GPU PWR & GND 2

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BLOCK DIAGRAM			
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XVDD



GPU XVDD BALLS(NC IN SUBSTRATE):
CAN CONNECT TO ANY POWER NET(NV/MS/1V8/PEX,etc) ON SYSTEM BOARD,
PROVIDE FLEXIBILITY TO OPTIMIZE POWER CHANNELS ON SYSTEM BOARD,
ESPECIALLY USEFUL FOR LOW-COST DESIGN WITH REDUCED PCB LAYERS.

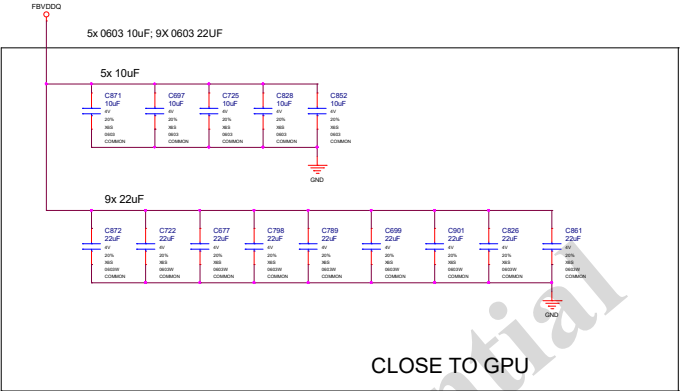
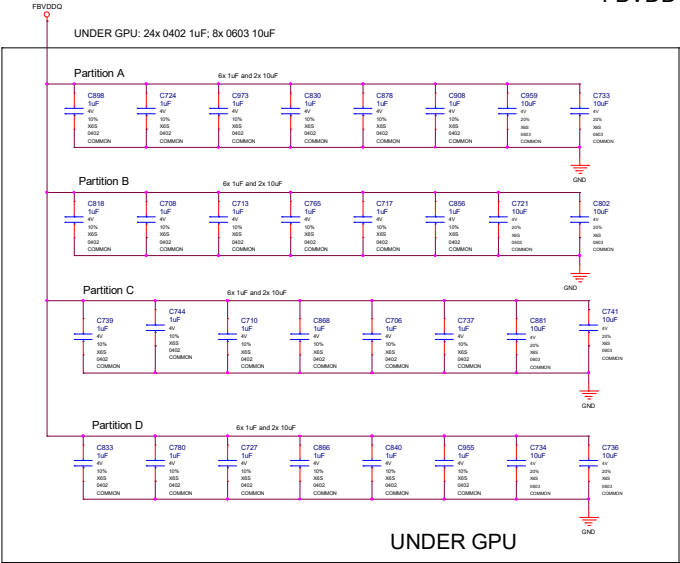
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ASSEMBLY
PAGE DETAIL

~ASSEMBLY DESCRIPTION~
GPU PWR & GND 3 (XVDD)

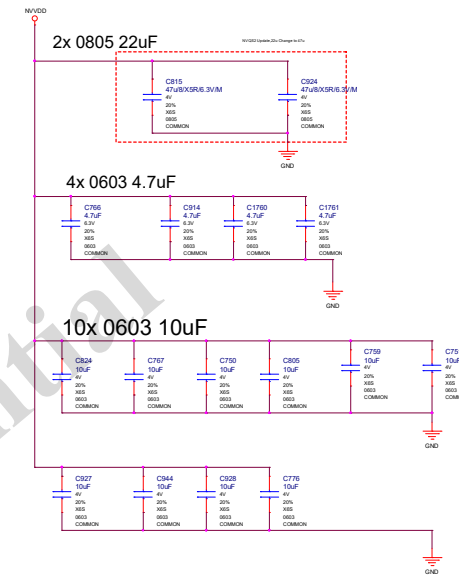
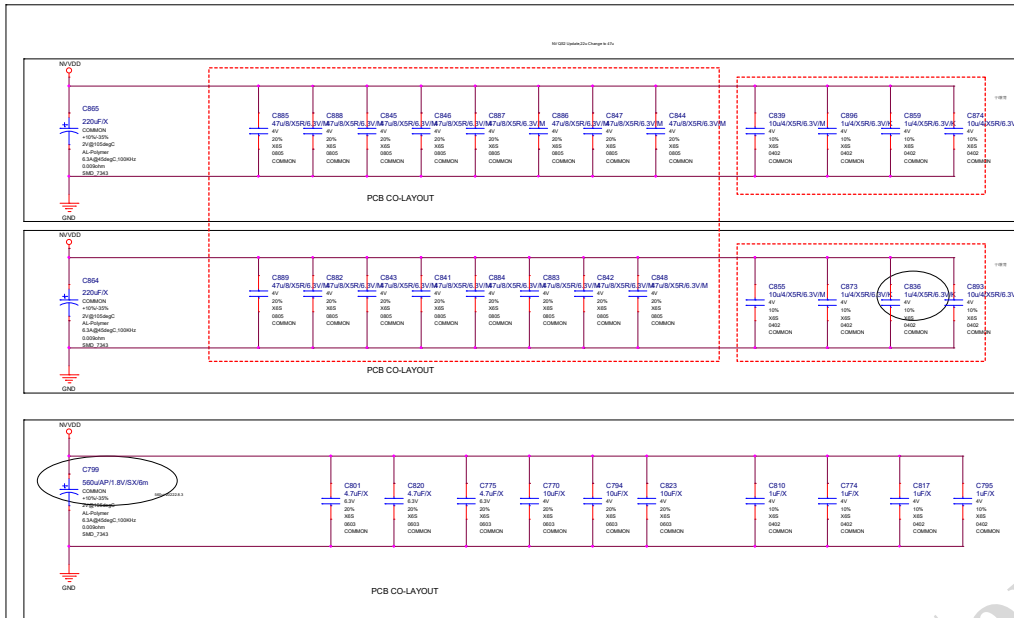
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FBVDDQ

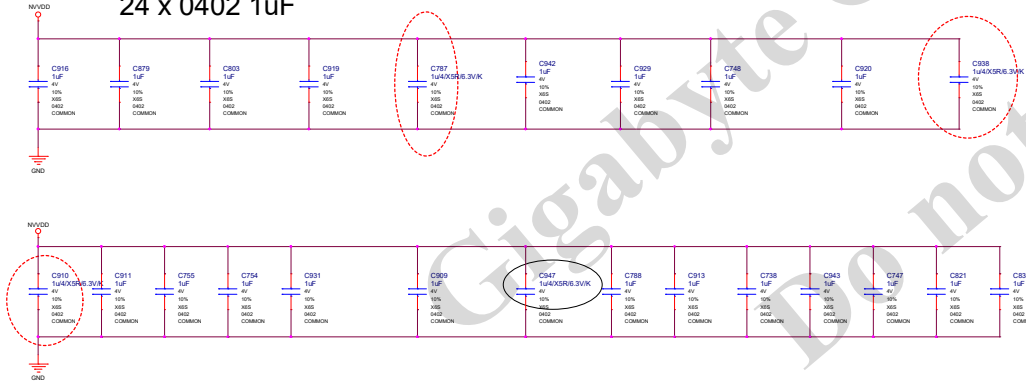


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GPU DECOUPLING NVDD



24 x 0402 1uF



UNDER GPU

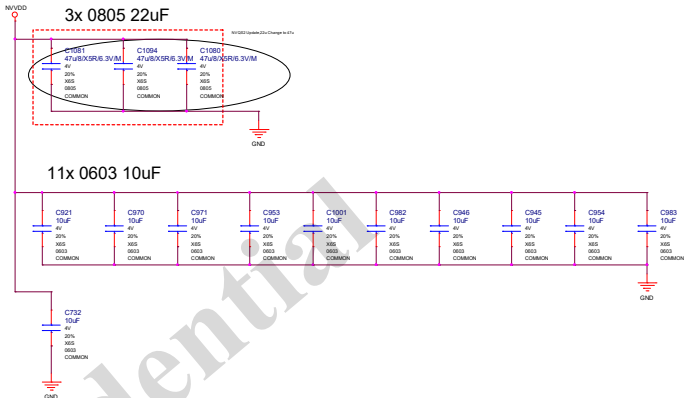
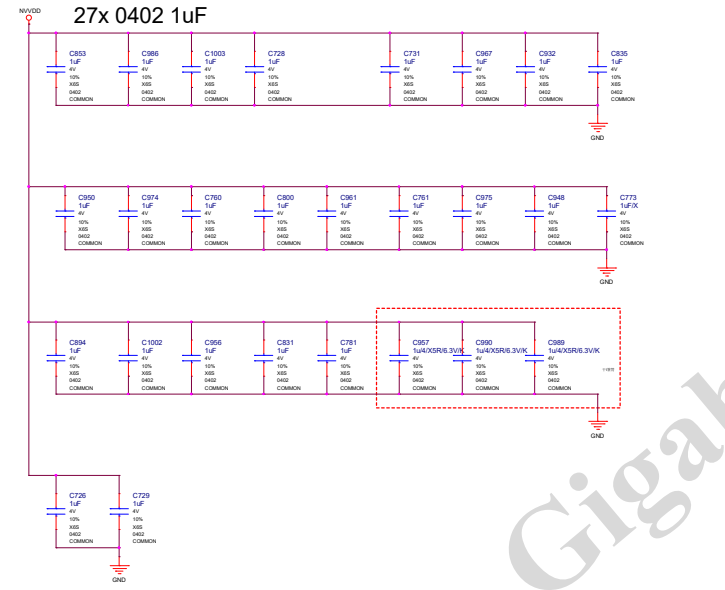
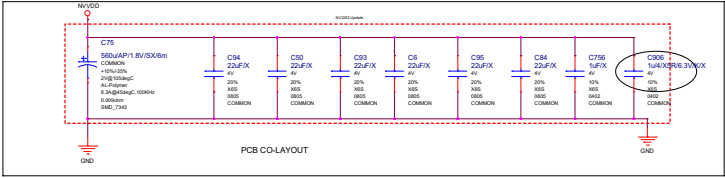
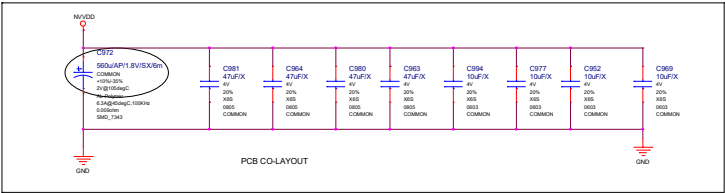
GIGABYTE

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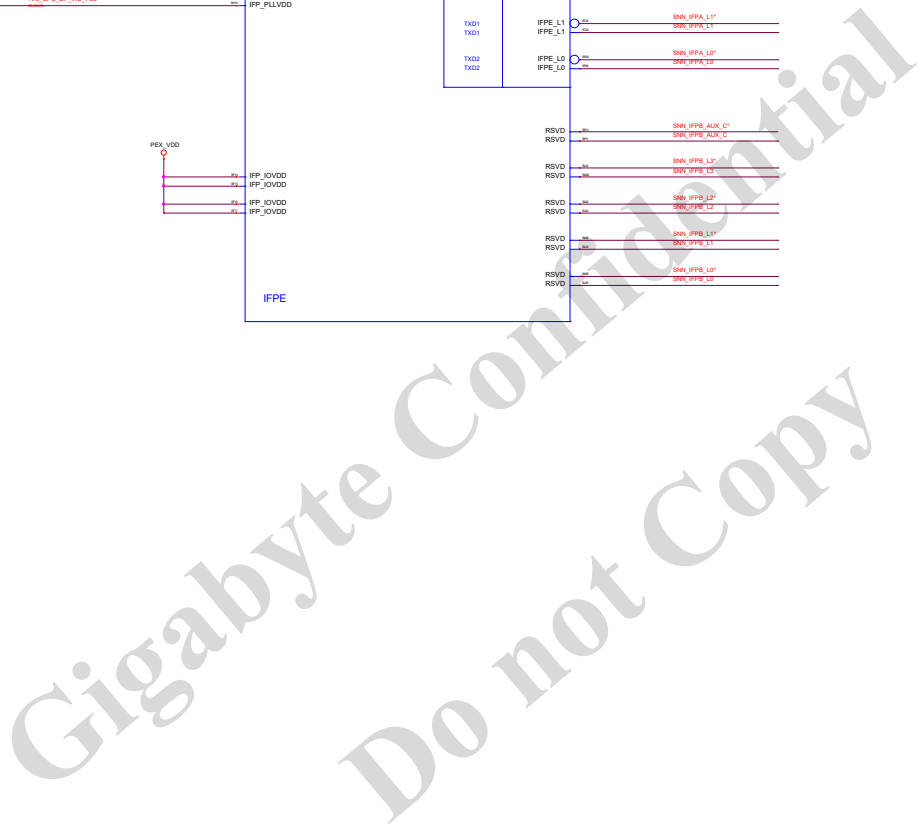
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PAGE DETAILASSEMBLY DESCRIPTION
GPU DECOUPLING NVDD

GPU DECOUPLING NVVDD

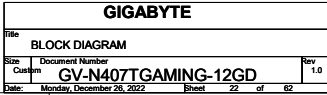


UNDER GPU

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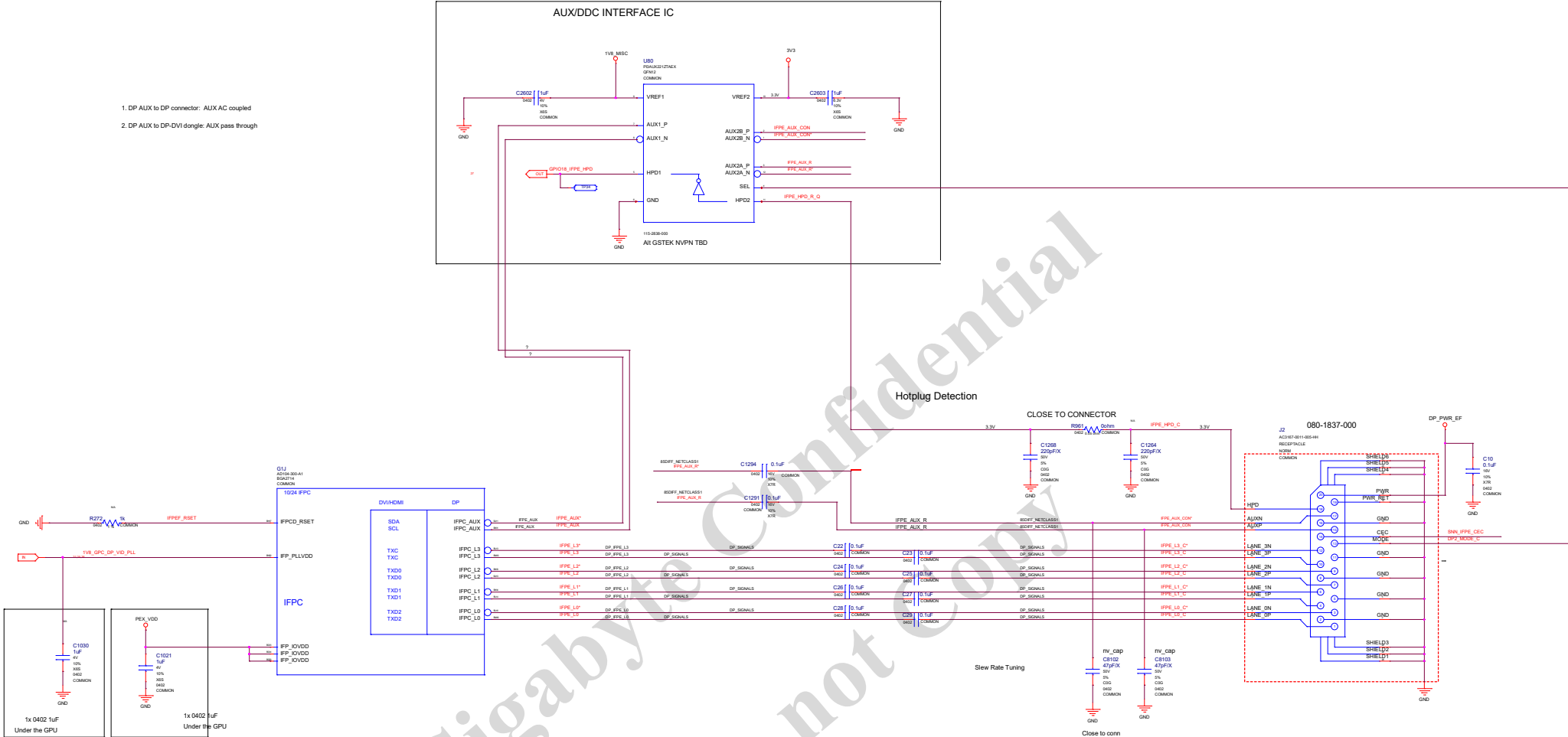


Gigabyte Com
Do not Copy



GA IFPE/NP IFPC DP

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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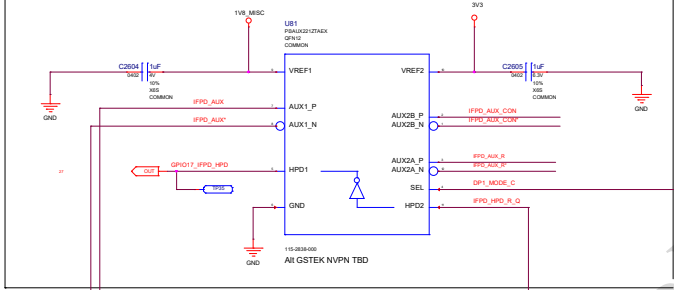
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ASSEMBLY DESCRIPTION
IO: GA IFPE/NP IFPC DP

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1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through

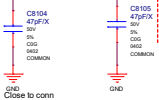
AUX/DDC INTERFACE IC



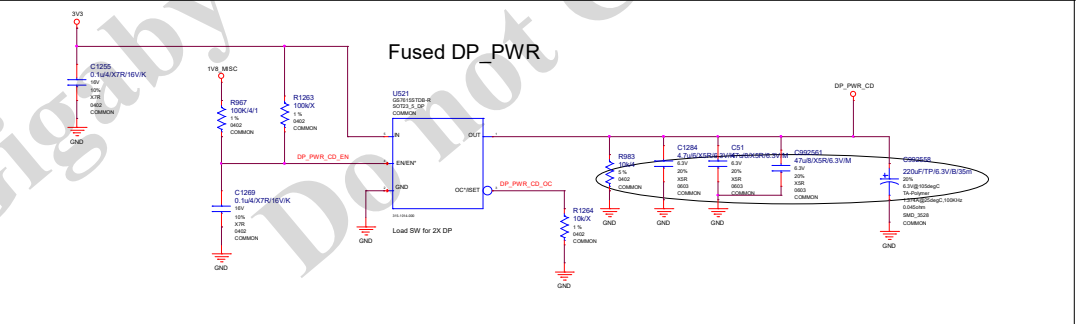
Hotplug Detection



Slew Rate Tuning



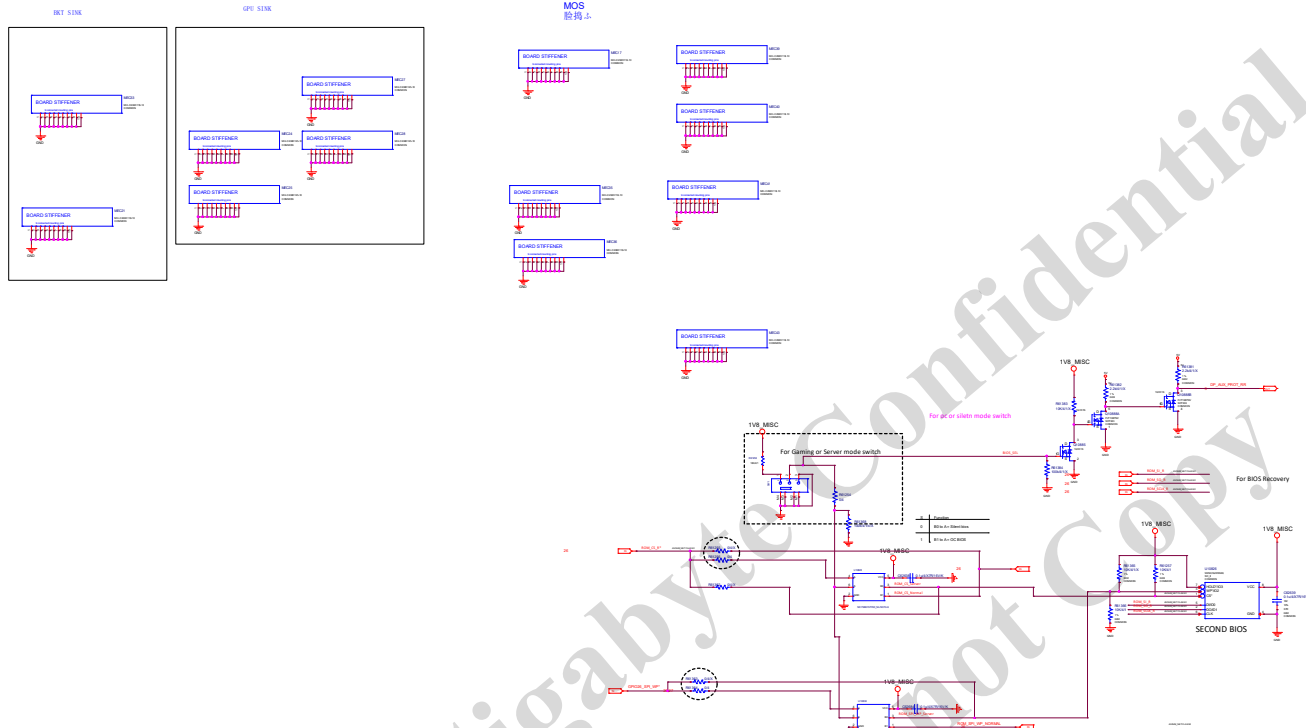
Fused DP_PWR



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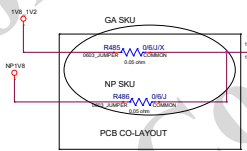
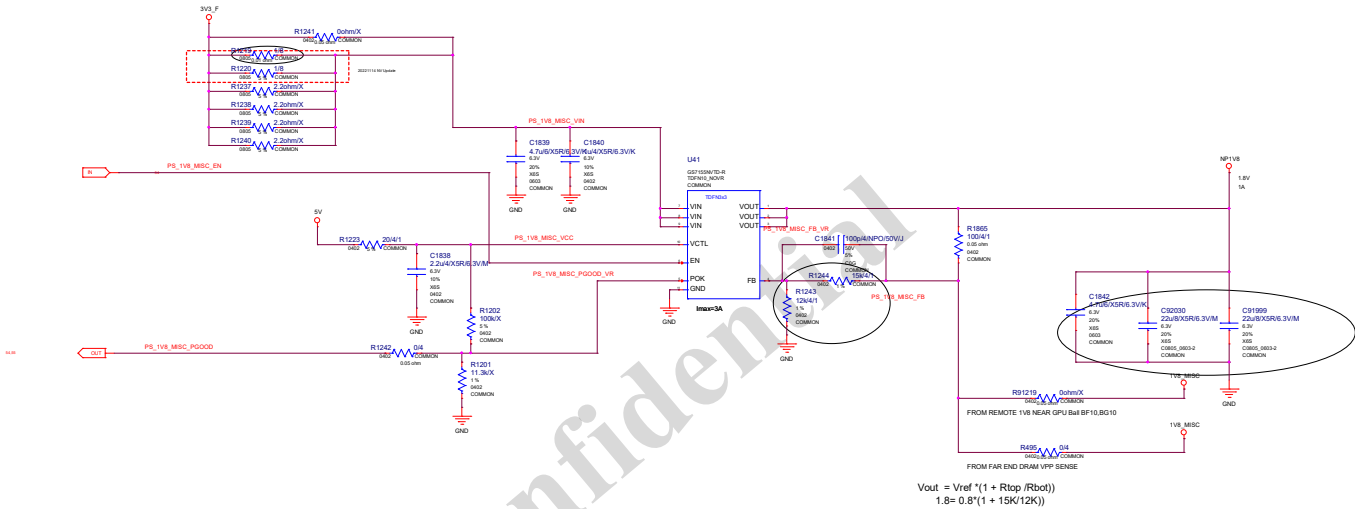


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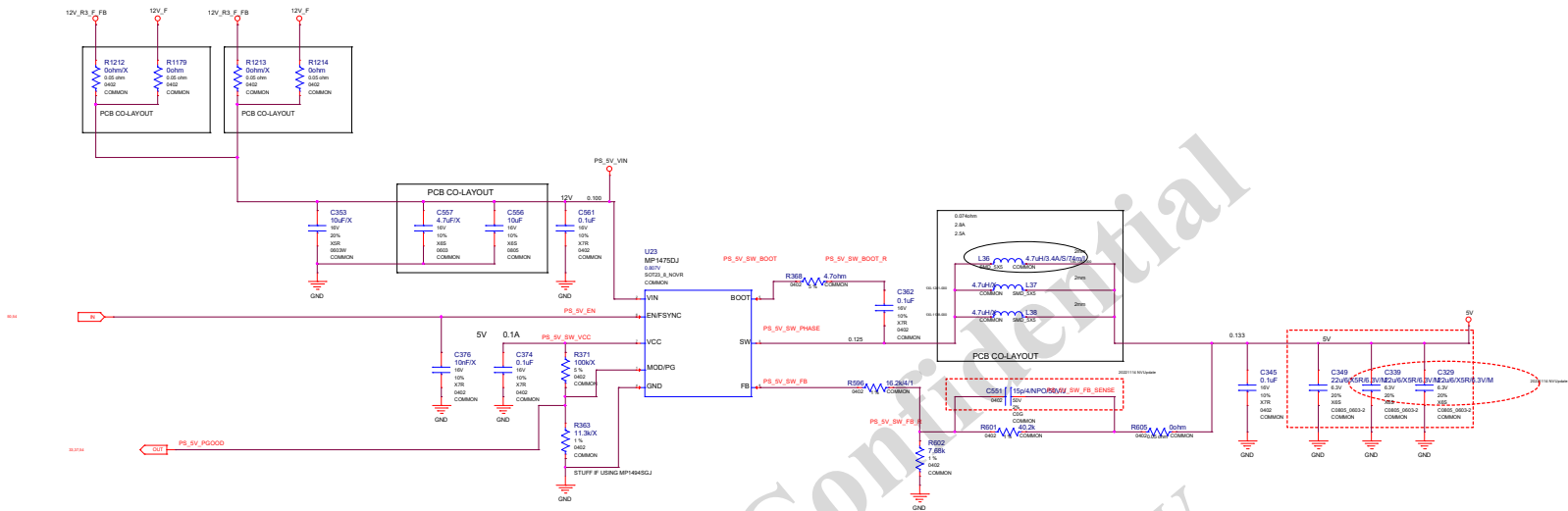
NP1V8



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ASSEMBLY PAGE DETAIL
PS:NP1V8,1V8_MISC

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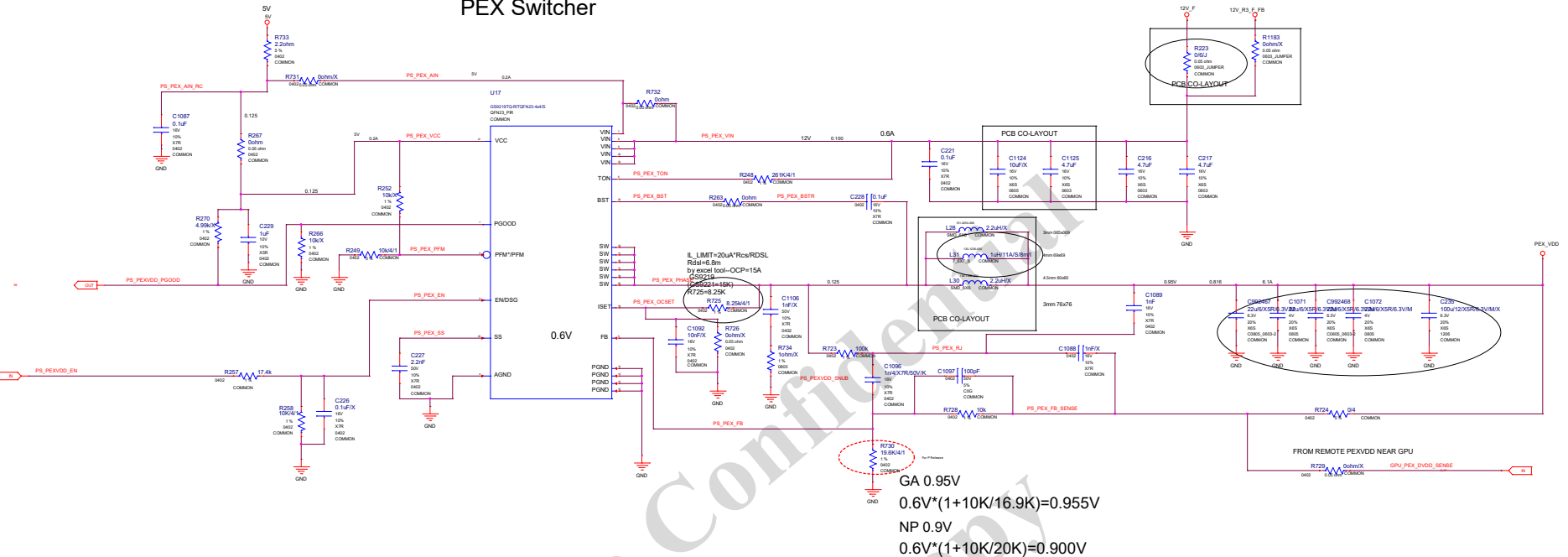
$$V_{out} = V_{ref} \cdot (1 + R_{top}/R_{bot})$$
$$0.807V \cdot (1 + 40.2K/7.68K) = 5.03V$$

RIIPPLE CURRENT=1.24A FOR 12V->5V 500KHZ 4.7uH

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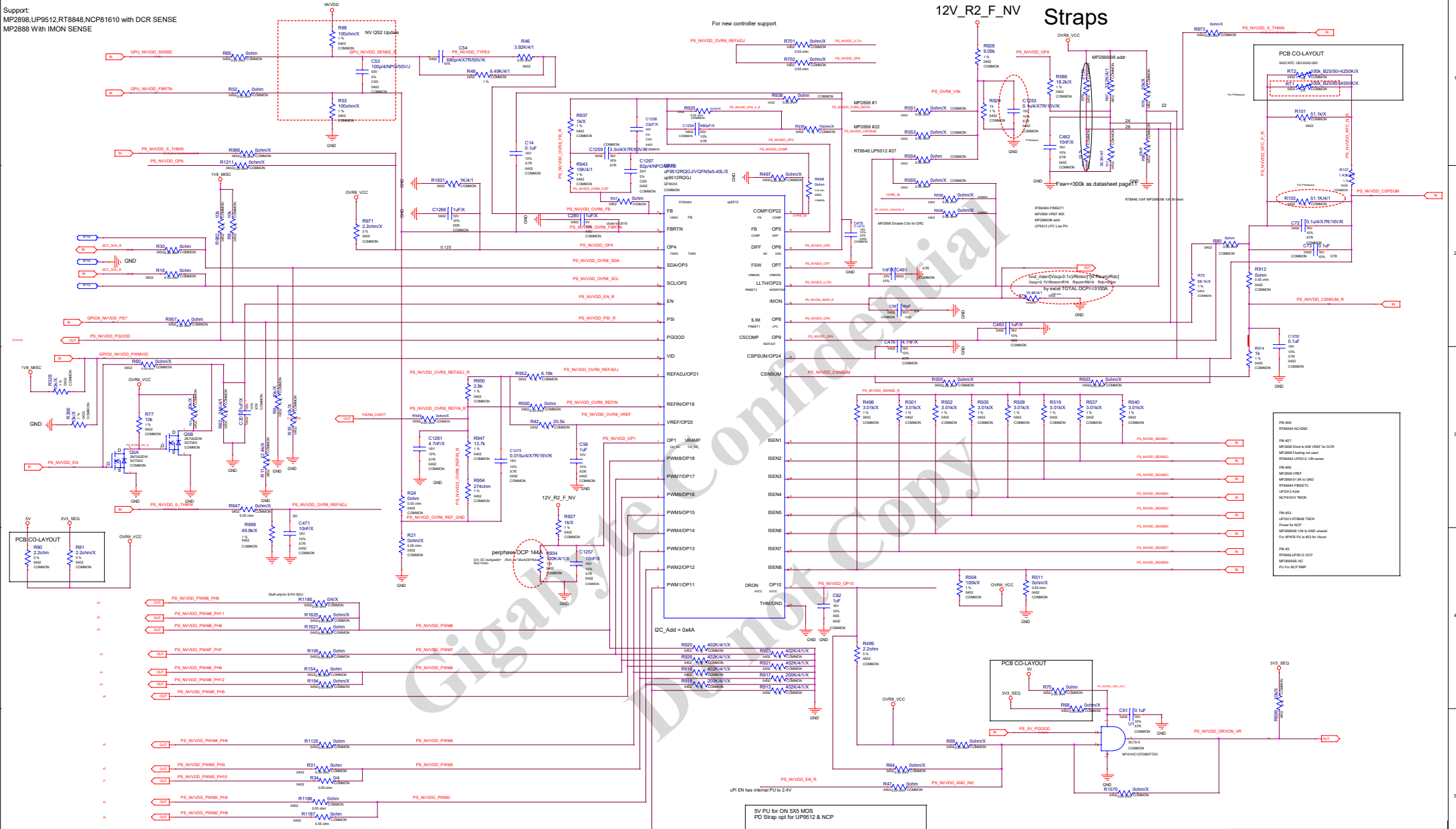
PEX Switcher



GA 0.95V
 $0.6V \cdot (1 + 10K/16.9K) = 0.955V$
 NP 0.9V
 $0.6V \cdot (1 + 10K/20K) = 0.900V$

NVDD CTR

Support:
MP2898,UP9512,RT8848,NCP81610 with DCR SENSE
MP2888 With IMON SENSE



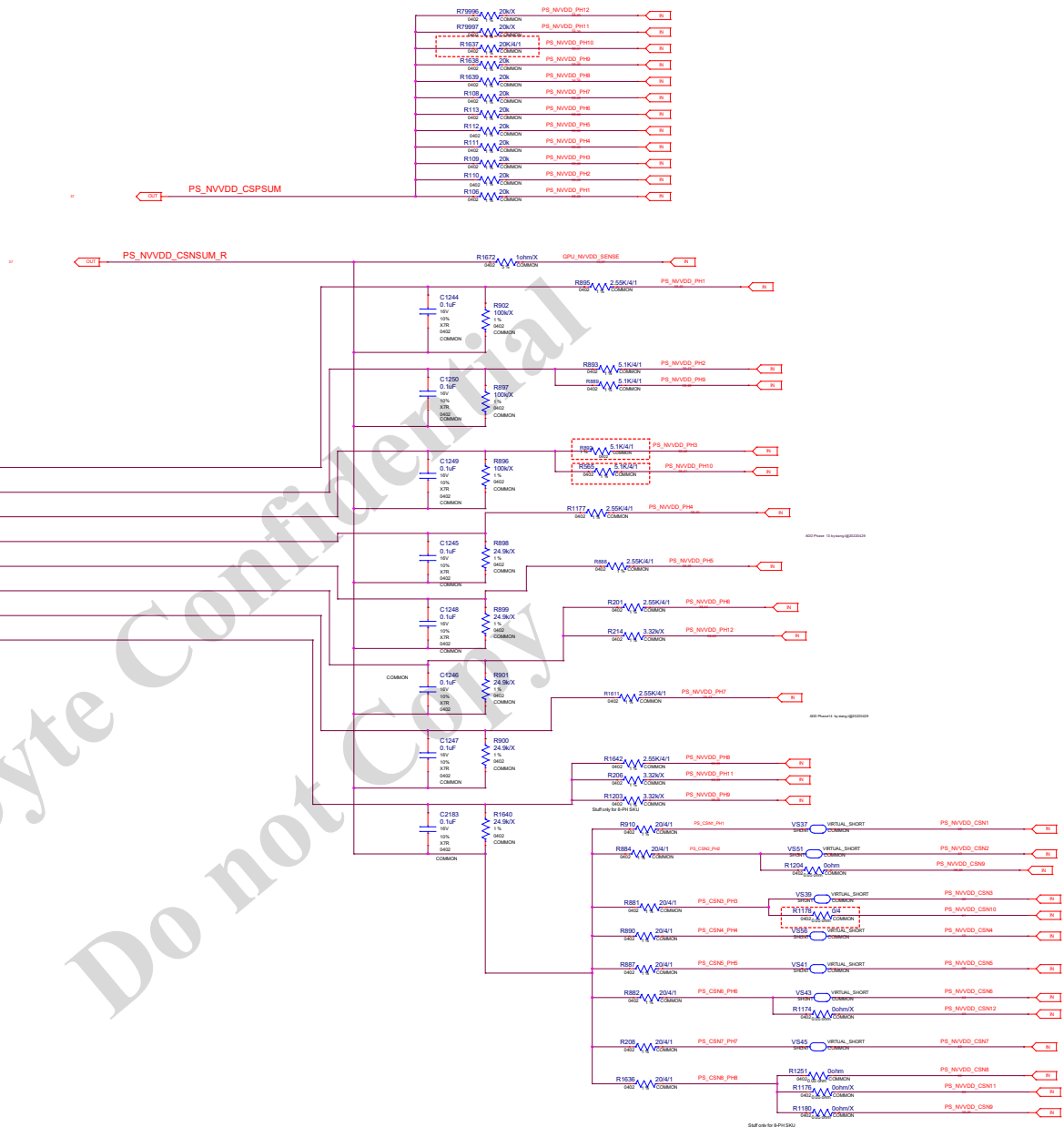
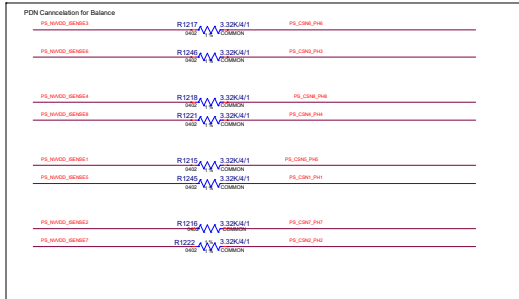
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ASSEMBLY
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ASSEMBLY DESCRIPTION
PS NVDD Controller

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NVVDD PDN Cancellation



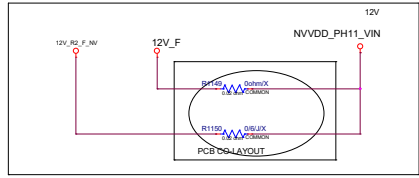
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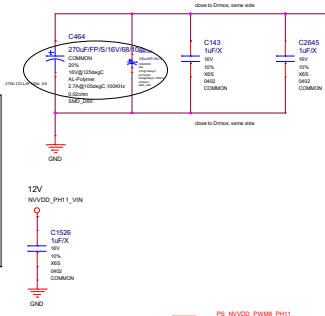
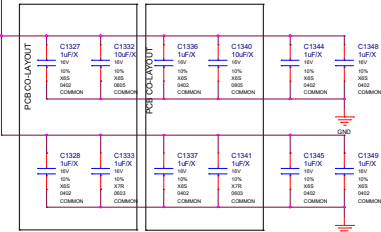
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Size	Document Number	Rev	1.0
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NVDD PH11 & PH8

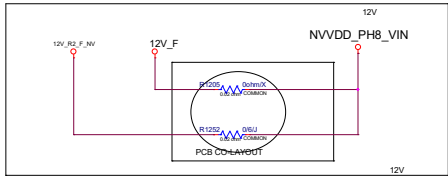
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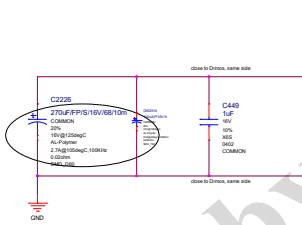
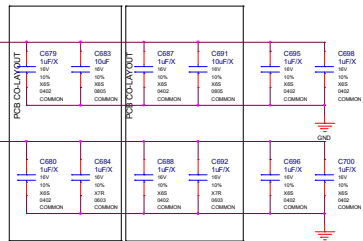
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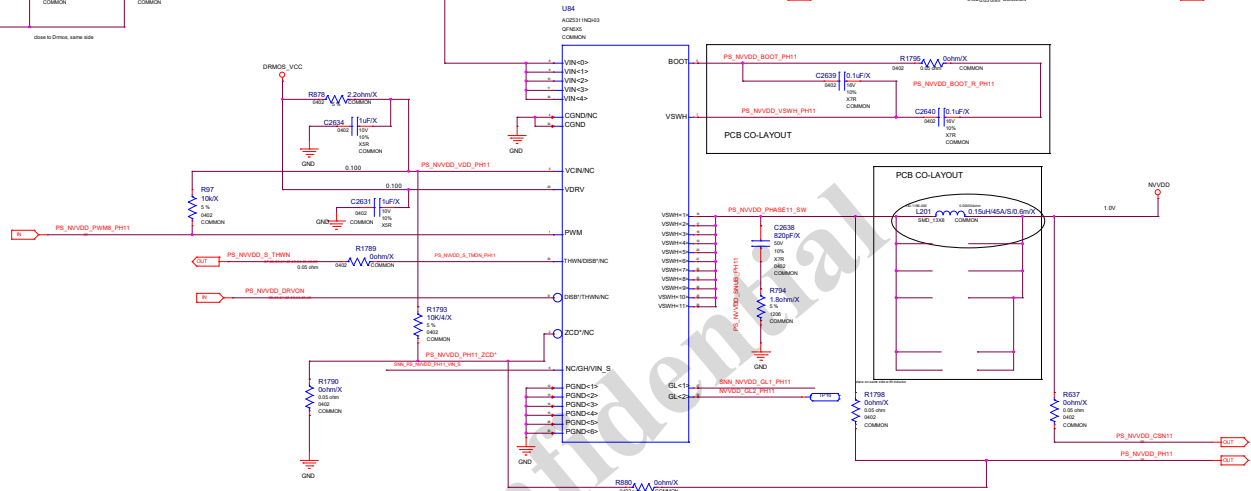
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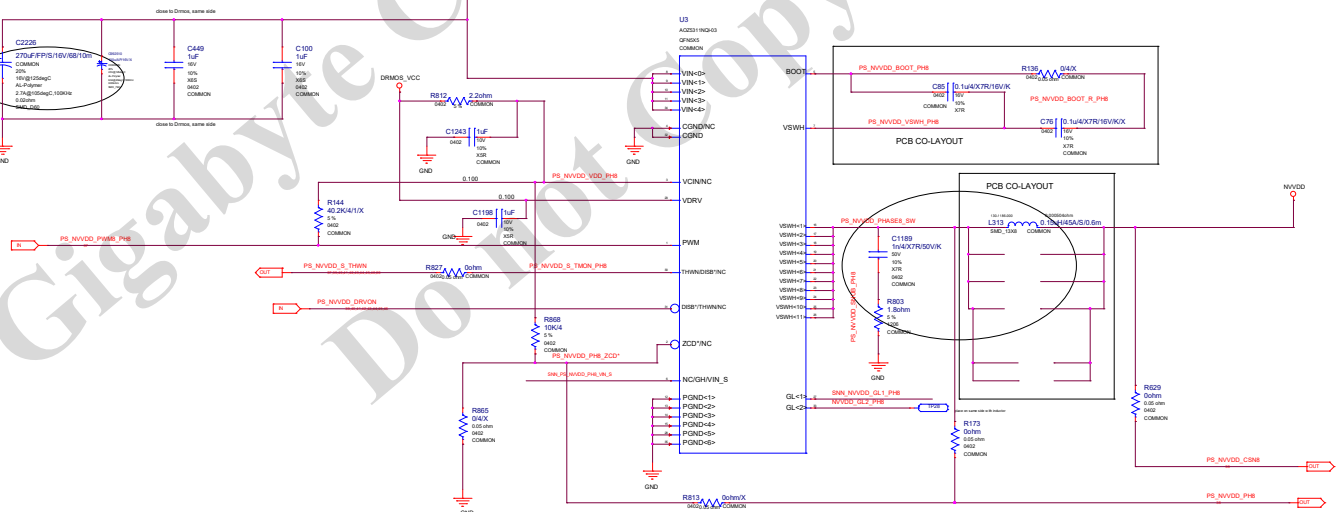
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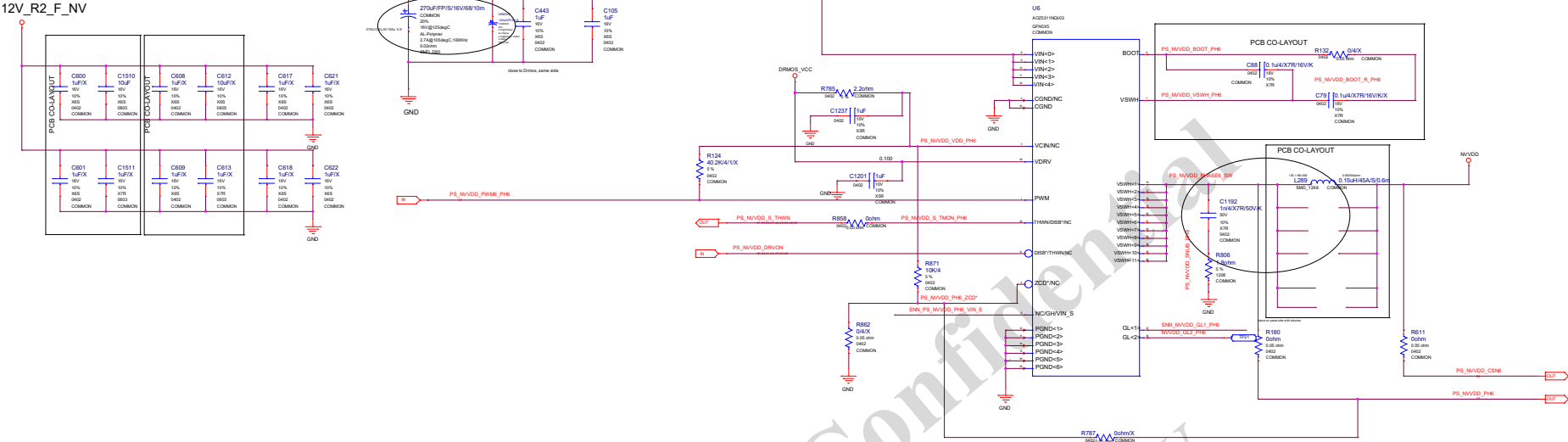


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ASSEMBLY PAGE DETAIL
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NVVDD PH6(PWM6)



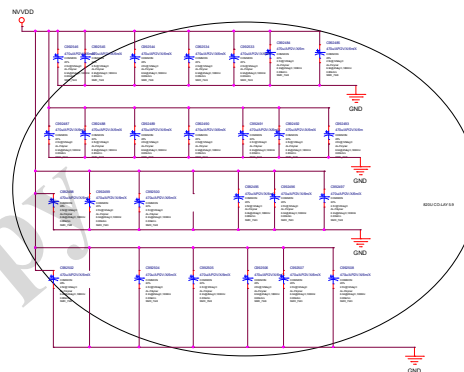
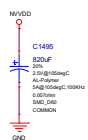
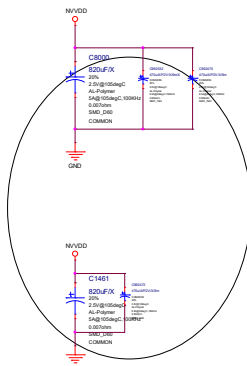
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PS: NVVDD PH6

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NVDD OUTPUT CAP 1

12xD60



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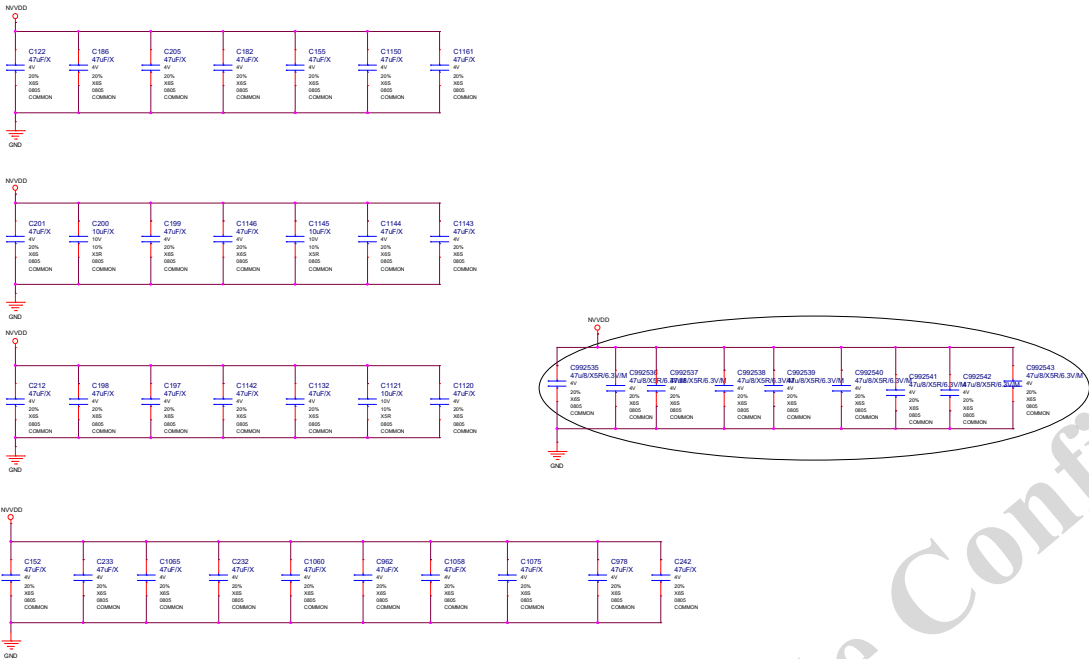
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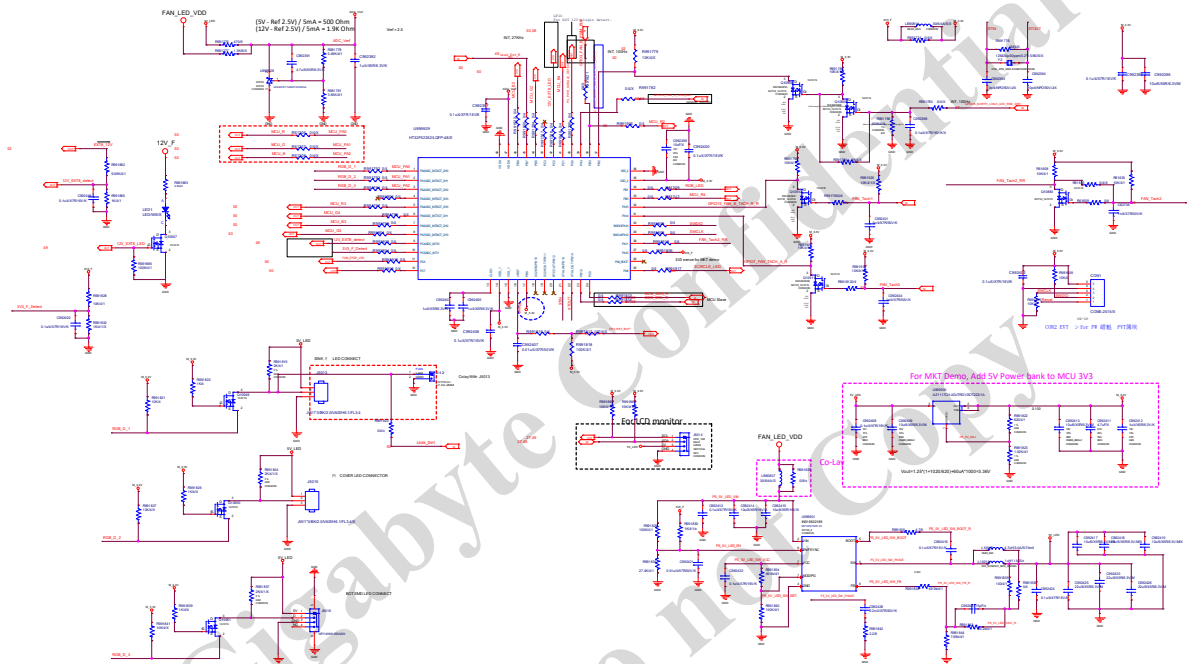
NVDD OUTPUT CAP 2



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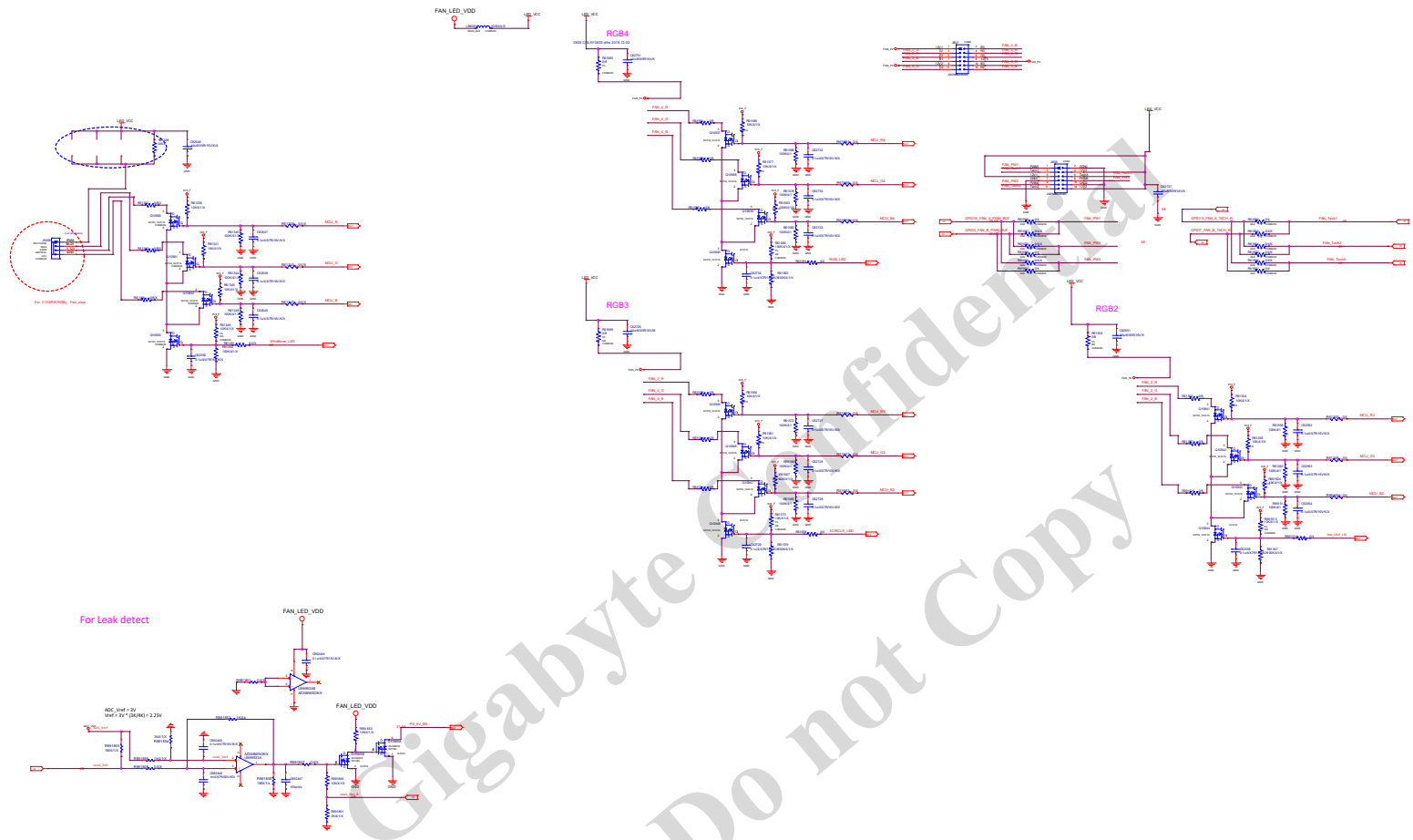
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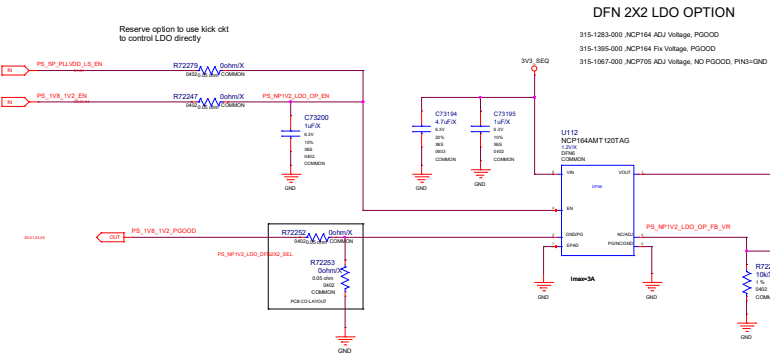


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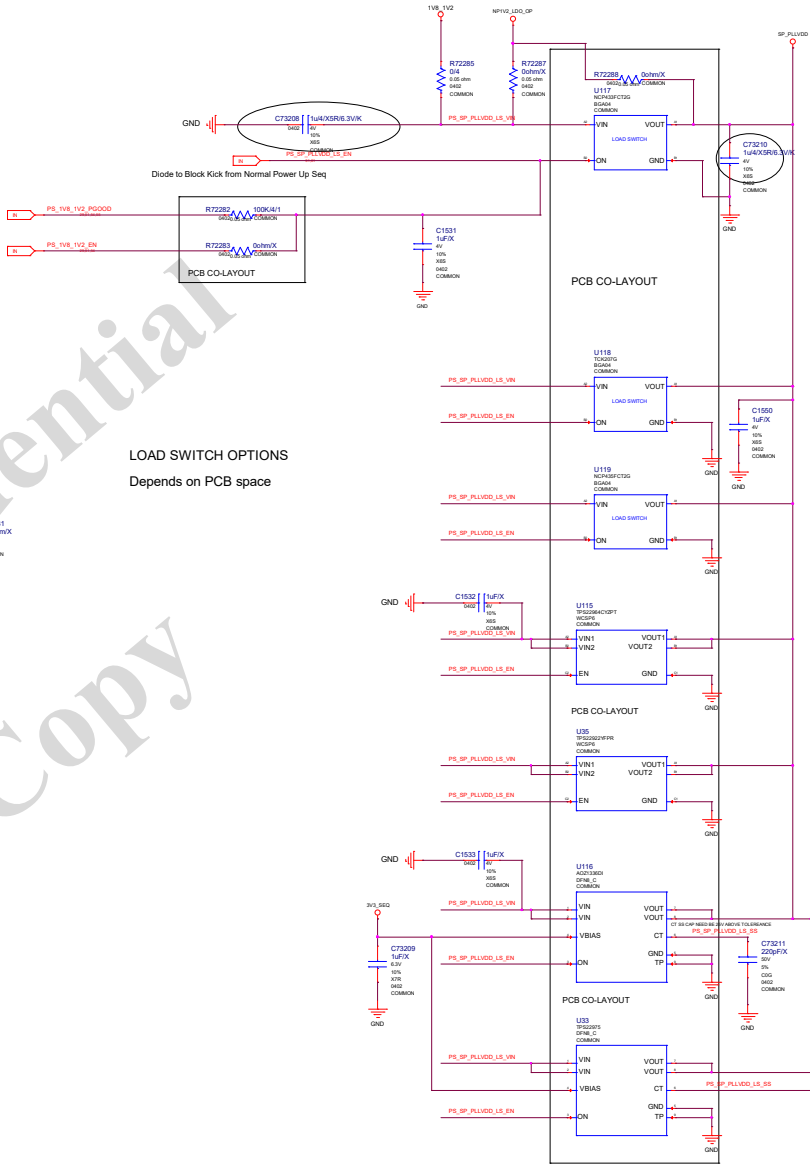
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SPPLLVD_LDO_LOADSWITCH



Bleeder option for faster discharge

LOAD SWITCH OPTIONS
Depends on PCB space



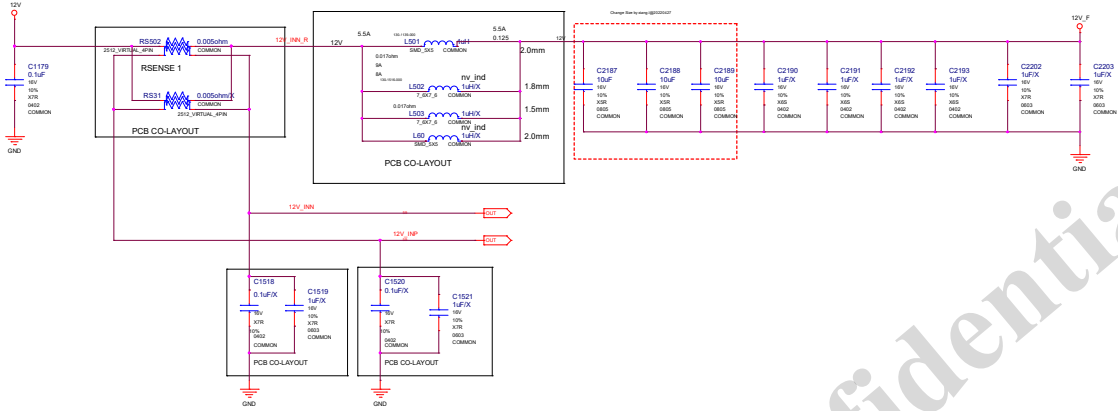
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ASSEMBLY PAGE DETAIL
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PS_SP_PLLVDD_LDO_LOADSWITCH

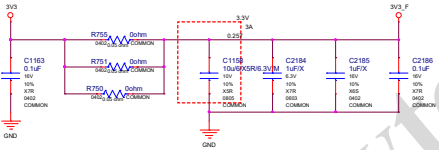
GIGABYTE			
File	BLOCK DIAGRAM		
Size	Document Number	Rev	1.0
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PEX_INPUT & FILTERING, PEX_3V3

PEX_12V INPUT - 66W



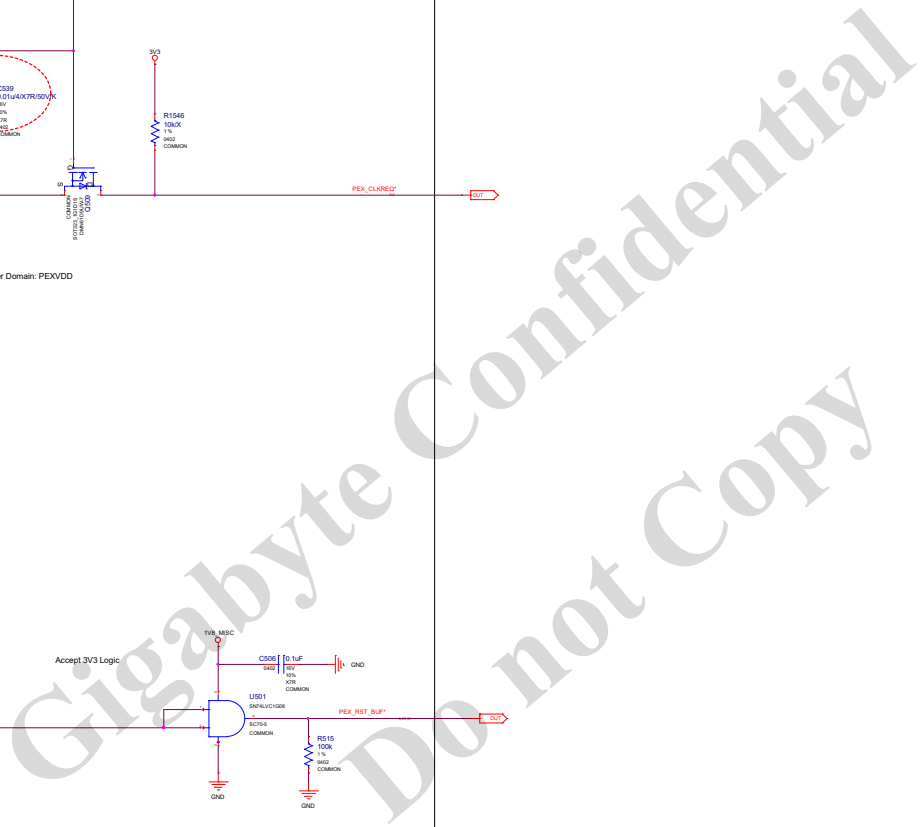
PEX 3V3 INPUT - 10W



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ASSEMBLY PAGE DETAIL
-ASSEMBLY DESCRIPTION-
PIS_PEX_12V_PEX_3V3 AND AV3_AUX

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ASSEMBLY	<ASSEMBLY_DESCRIPTION>
PAGE DETAIL	SEQ: MISC

RT9818E-2TGS:

- I_b=3μA (typ), 8μA (Max)
- V_{reset}=(1+R_{top}/R_{bot})*(V_{ih}+R_{tbp}*I_b)
- V_{reset} (typ)=(1+0)/2.7V÷1K·3μA=2.703V.

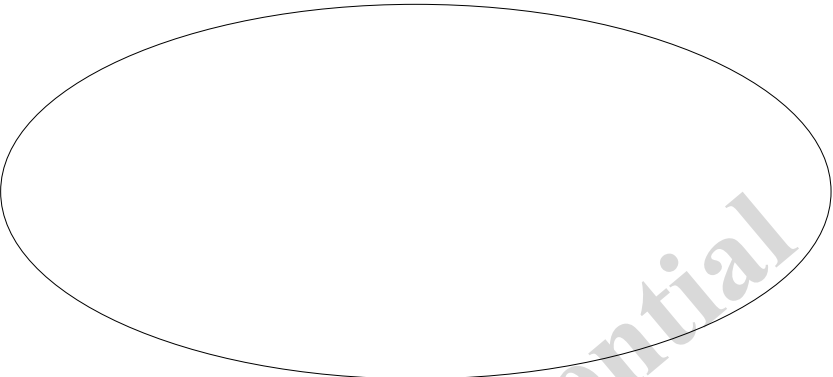
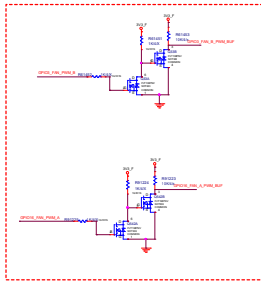
Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIe golden finger
12V	INPUT	Sense the 12V Voltage from PCIe golden finger
PS_VMON_PGOOD	OPEN-DRAIN	Floating(H) once both 3V3 and 12V reach V _{ih}
GCG_FB_EN	INPUT	Indicator for RTD3/GC6 residence.Use to Mask the VMON_PGOOD
PS_PF_SKP	INPUT	From IA3221(VPU) or Pre-filter(SKIP)
PS_FF_BSK	INPUT	From IA3221(PV) or Pre-filter(BS_OK)

Signal	Direction	Function
3V3	INPUT	Sense the 3V3 Voltage from PCIe golden finger
12V	INPUT	Sense the 12V Voltage from PCIe golden finger
PS_VMON_FG000	OPEN-DRAIN	Floating(I) once both 3V3 and 12V reach Vb
GC8_FB_EN	INPUT	Indicator for RTD3/GC8 residence,Use to Mask the VMON_FG000
PS_PF_SKIP	INPUT	From INA321(VPU) or Pre-filter(SKIP)
PS_PF_BSK0	INPUT	From INA322(PV) or Pre-filter(BS_OK)

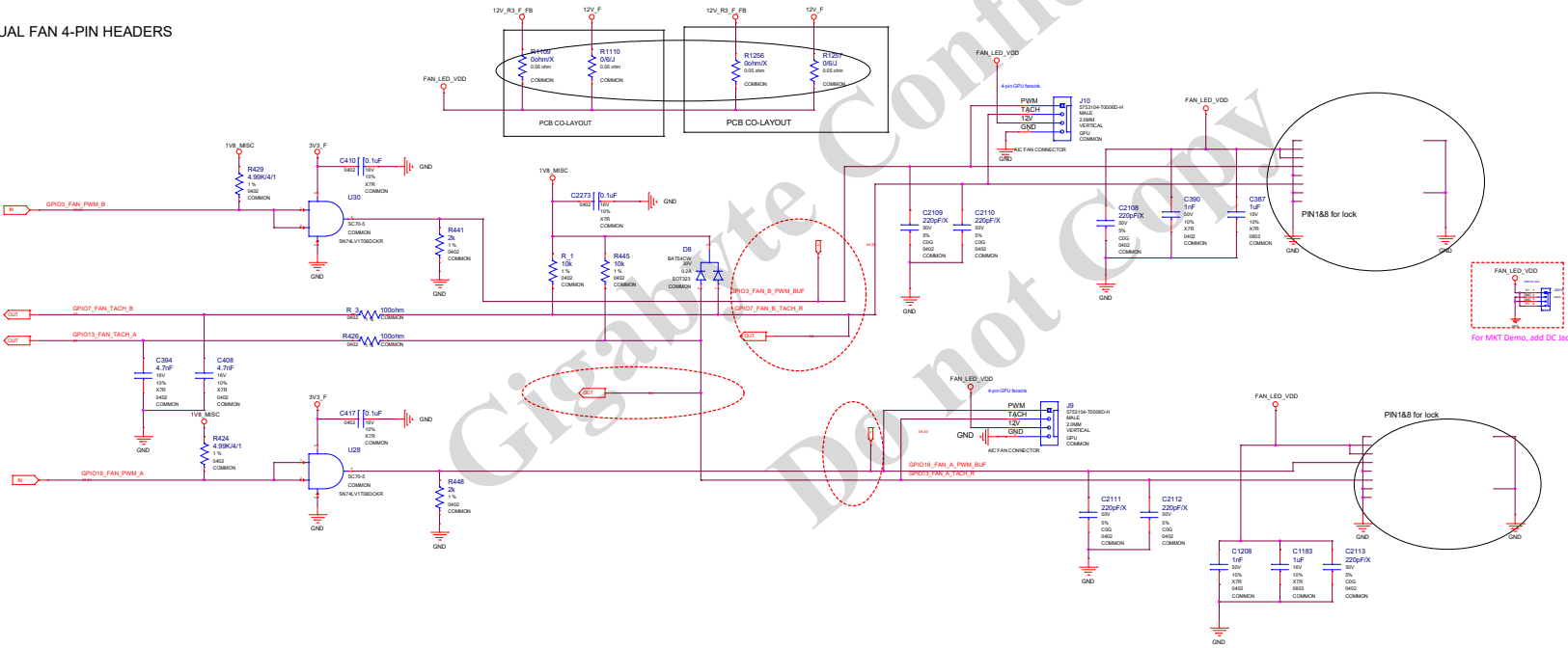
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PAGE DETAIL	SEQ: 3V3 VOLTAGE MONITOR

FAN&NORTH LED

2-PIN LED HEADER



DUAL FAN 4-PIN HEADERS

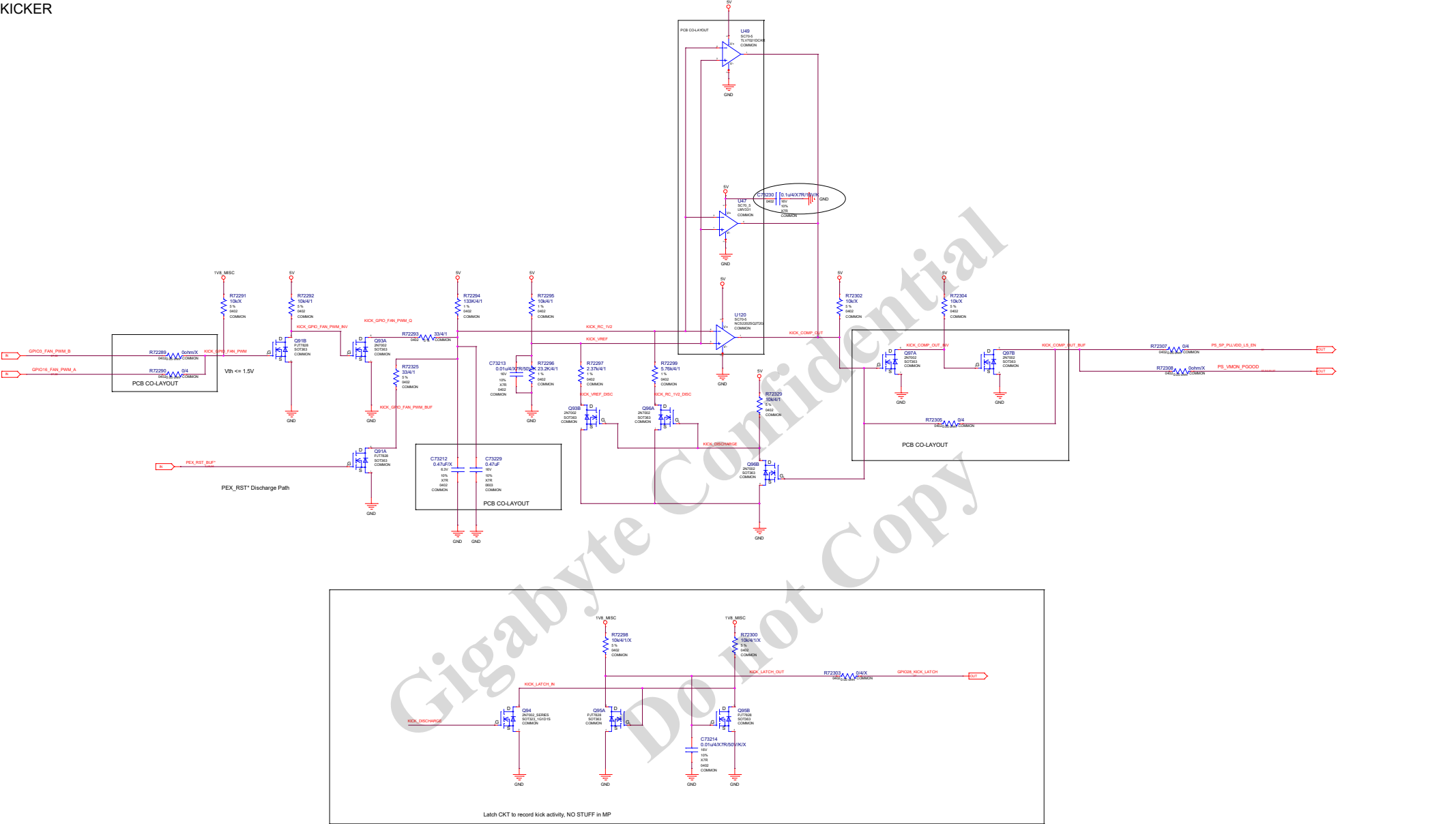


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ASSEMBLY PAGE DETAIL
FAN & NORTH LED

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KICKER



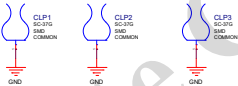
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ASSEMBLY PAGE DETAIL
KICKER

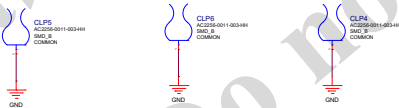
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MOUNTING HOLES

Top:3x EMI CLIPS



Bot:2x RETENTION SPRINGS



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ASSEMBLY
PAGE DETAIL

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