GA102/NP, GeForce SKU P-BOARD

450W/600W, 384bit, GDDR6x x16 24GB

DP + DP + DP + HDMI/DP

TABLE OF CONTENTS

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<OrgName>	Engineer:	Hariston_huang	
Size: Custom	Project Name: CG1393PBI2		Rev: 1.00X
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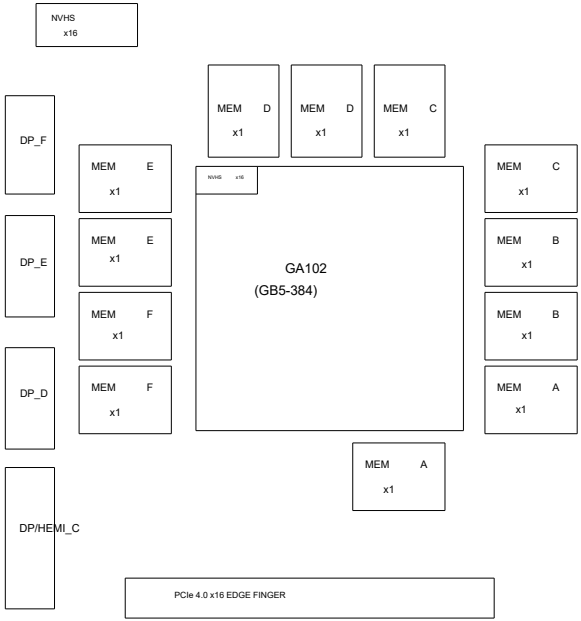
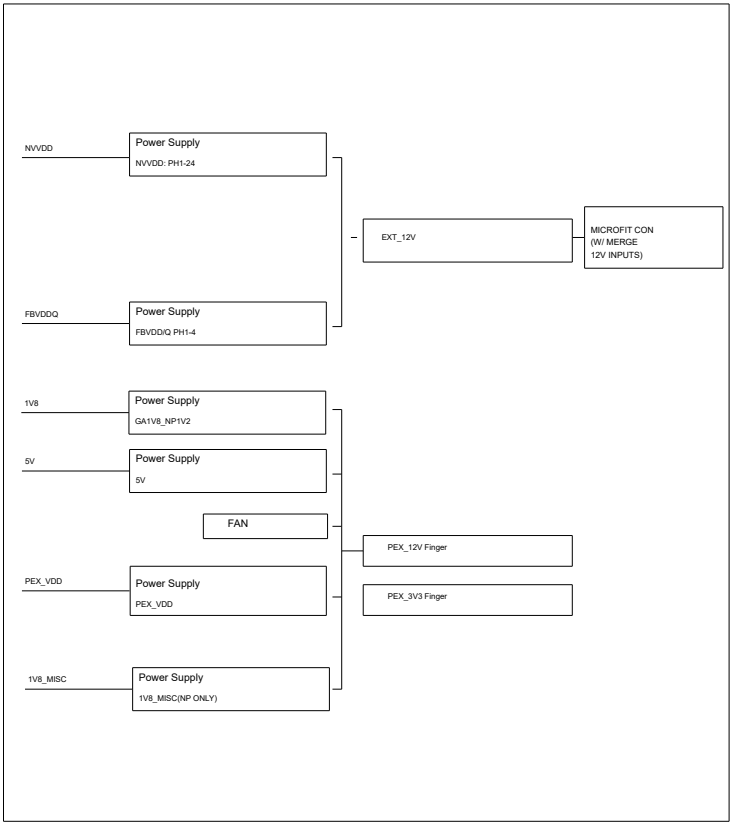
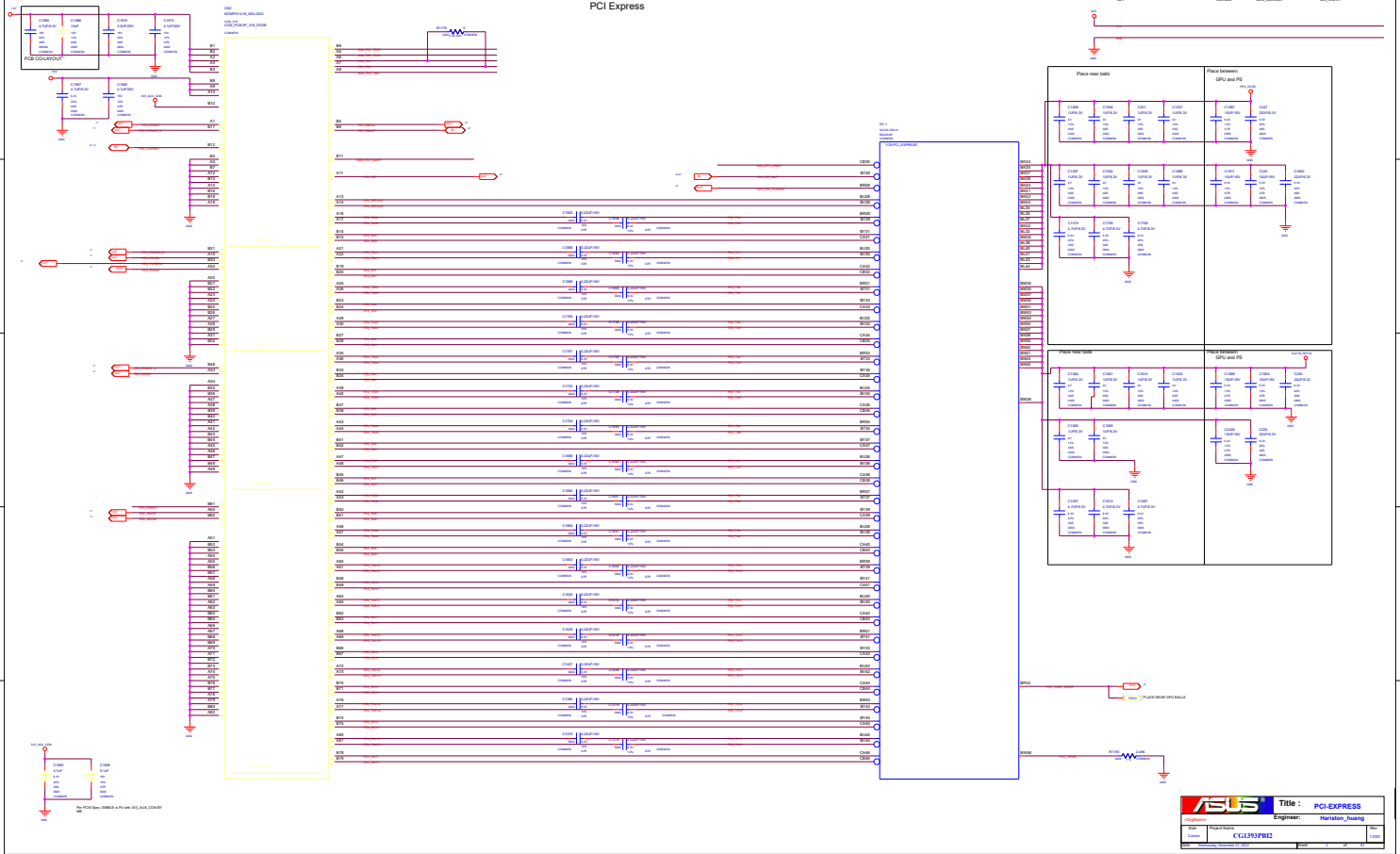


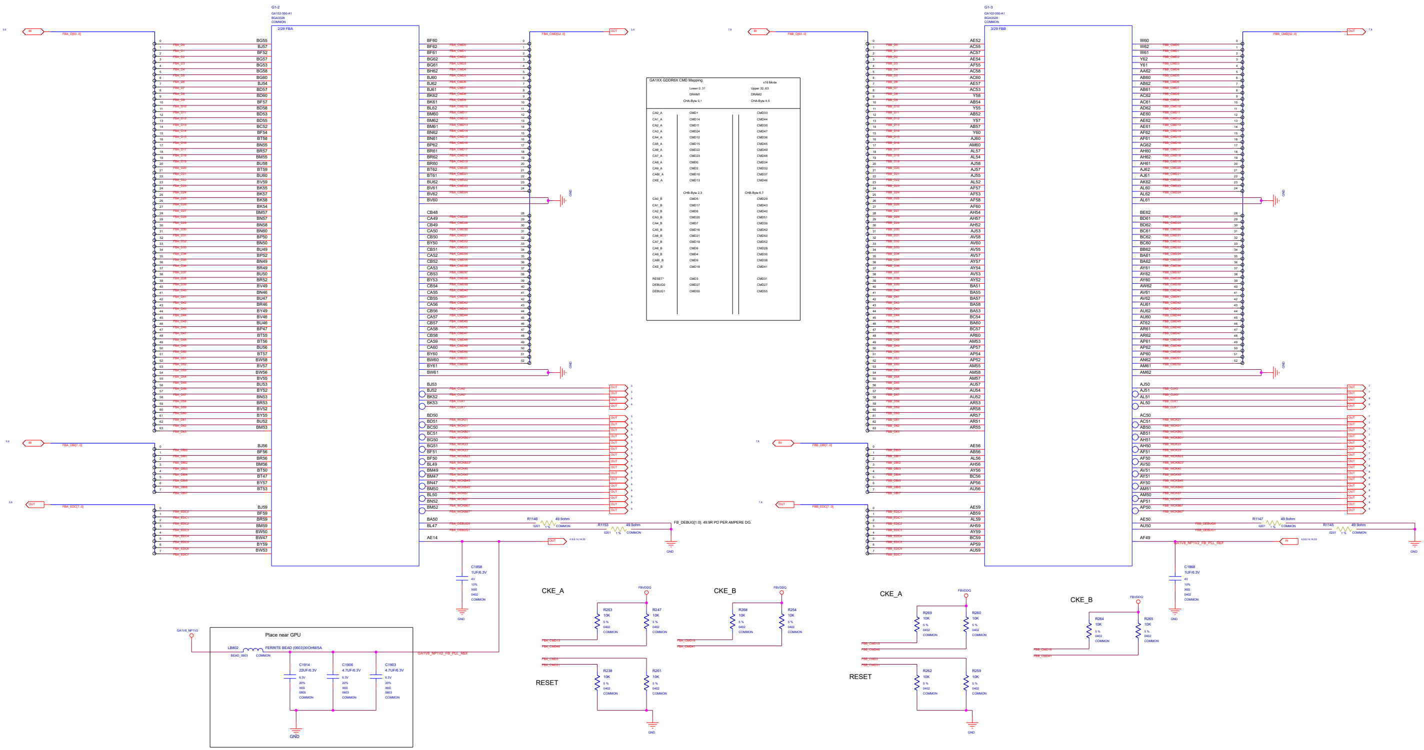


Title :	Block Diagram		
Engineer:	Hanston_huang		
Size: Custom	Project Name: CG1393PH12		Rev: 1.00D
Date: Wednesday, December 01, 2021	Sheet 2 of 61		

Page 3: PCI-EXPRESS



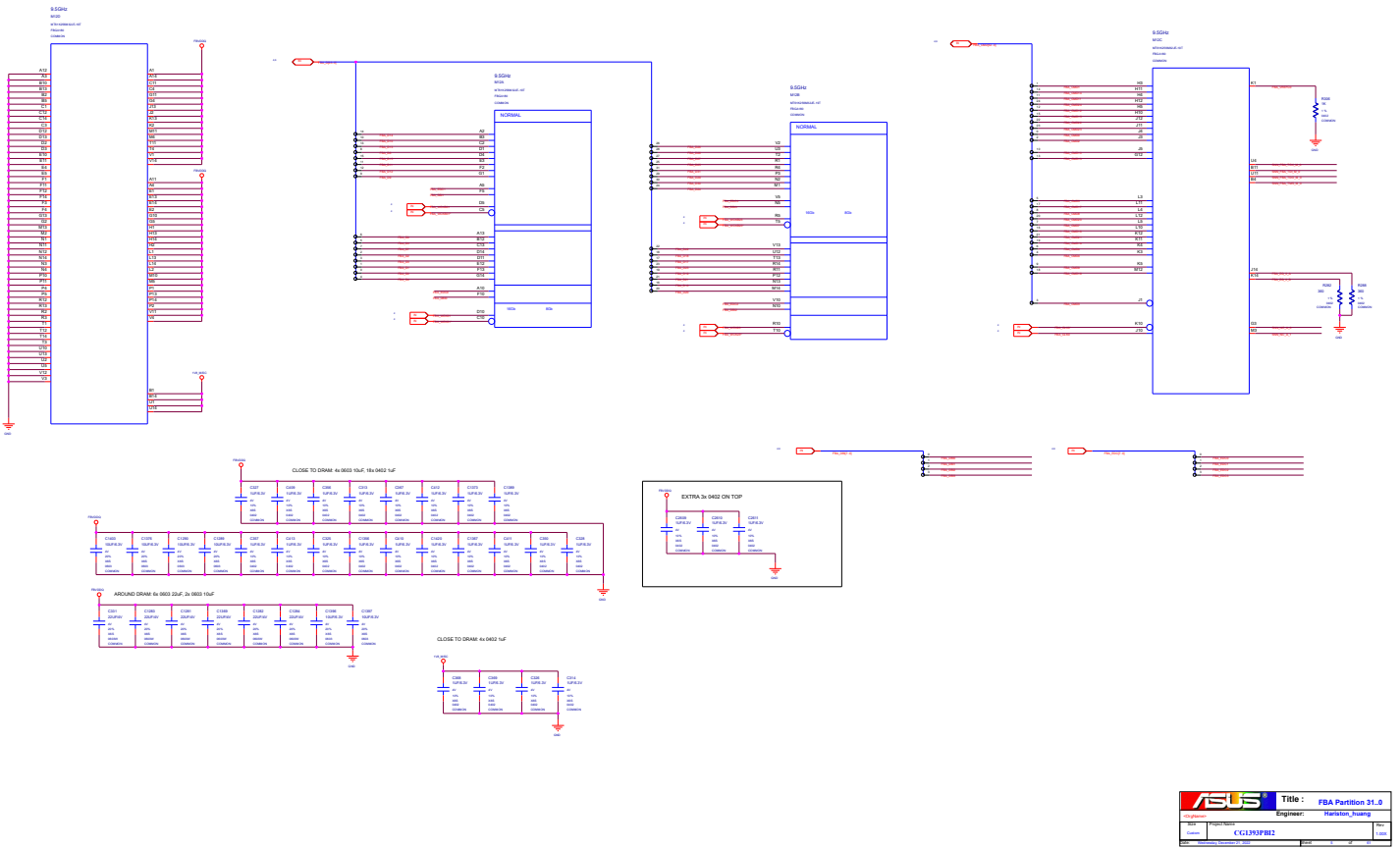
Page 4: MEMORY: GPU Partition A/B

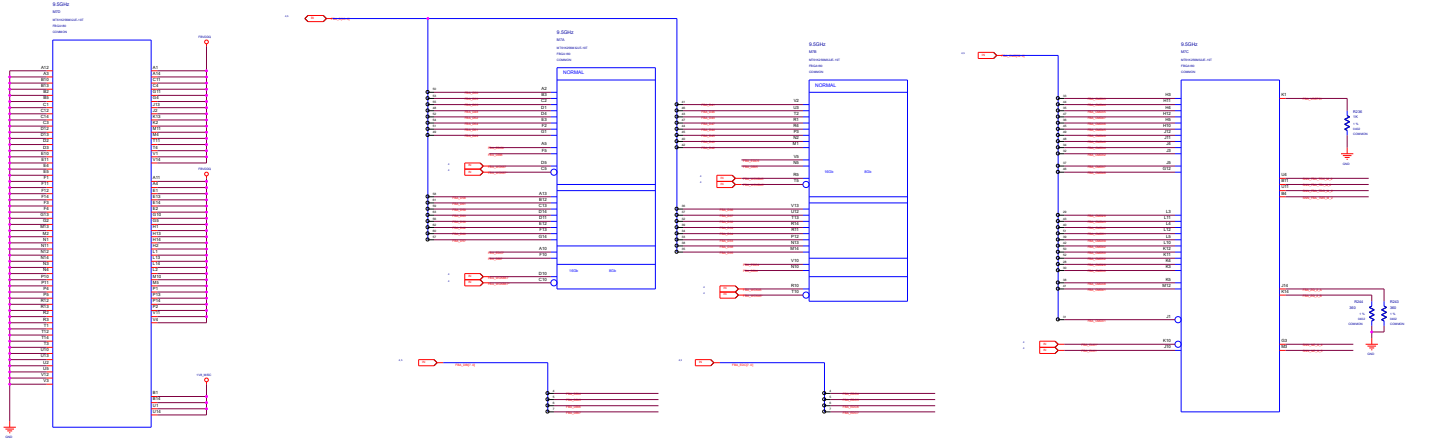


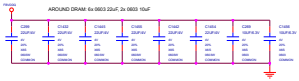
GA1XX GDDR6X CMD Mapping

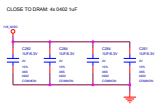
	x16 Mode	
	Lower 0..31	Upper 32..63
	DRAM1	DRAM2
	CHA-Byte 0,1	CHA-Byte 4,5
CA0_A	CMD1	CMD33
CA1_A	CMD14	CMD44
CA2_A	CMD11	CMD35
CA3_A	CMD24	CMD47
CA4_A	CMD12	CMD36
CA5_A	CMD15	CMD45
CA6_A	CMD22	CMD49
CA7_A	CMD23	CMD48
CA8_A	CMD0	CMD34
CA9_A	CMD2	CMD32
CABI_A	CMD10	CMD37
CKE_A	CMD13	CMD46
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD5	CMD29
CA1_B	CMD17	CMD43
CA2_B	CMD8	CMD40
CA3_B	CMD20	CMD51
CA4_B	CMD7	CMD39
CA5_B	CMD16	CMD42
CA6_B	CMD21	CMD50
CA7_B	CMD19	CMD52
CA8_B	CMD6	CMD28
CA9_B	CMD4	CMD30
CABI_B	CMD9	CMD38
CKE_B	CMD18	CMD41
RESET*	CMD3	CMD31
DEBUG0	CMD27	CMD27
DEBUG1	CMD55	CMD55

Title: Partition A/B
<OrgName>
Engineer: Hariston_huang
Size: Custom | Project Name: CG1393PBI2 | Rev: 1.00X
Date: Wednesday, December 21, 2022 | Sheet 4 of 61

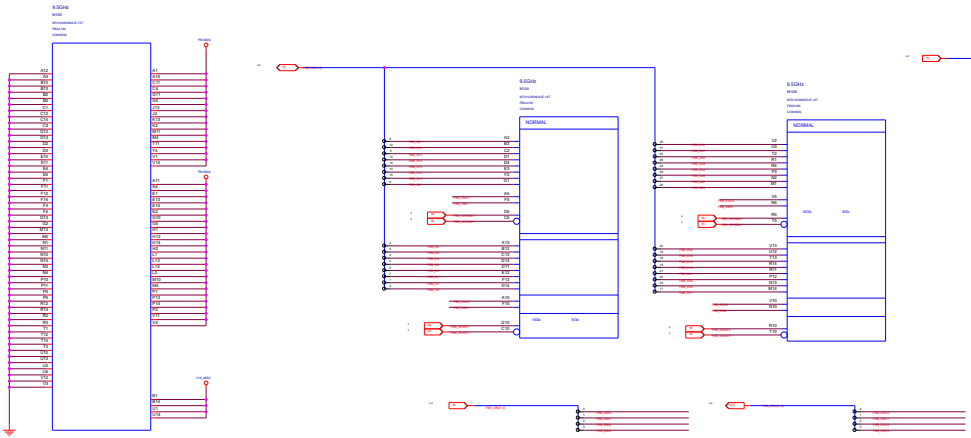

9.5GHz
NORMAL
CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF
EXTRA 3x 0402 ON TOP
AROUND DRAM: 6x 0603 22uF, 2x 0603 10uF
CLOSE TO DRAM: 4x 0402 1uF
Title : FBA Partition 31..0
Engineer: Harlston_huang
CG1393PBI2







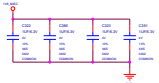
ASUSTeK Computer Inc.	Title :	FBA Partition 63..32	
	Engineer:	Herkston_huang	
Size: Custom	Project Name: CG1393PB12		Rev: 1.00
Date: Wednesday, December 07, 2022	Sheet 6 of 37		



CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF

AROUND DRAM: 6x 0603 22uF, 2x 0603 10uF

CLOSE TO DRAM: 4x 0402 1uF



Title :	FBB Partition 31..0		
Engineer:	Harlston_huang		
Size	Project Name	Rev	
Custom	CG1393PBI2	1.00A	
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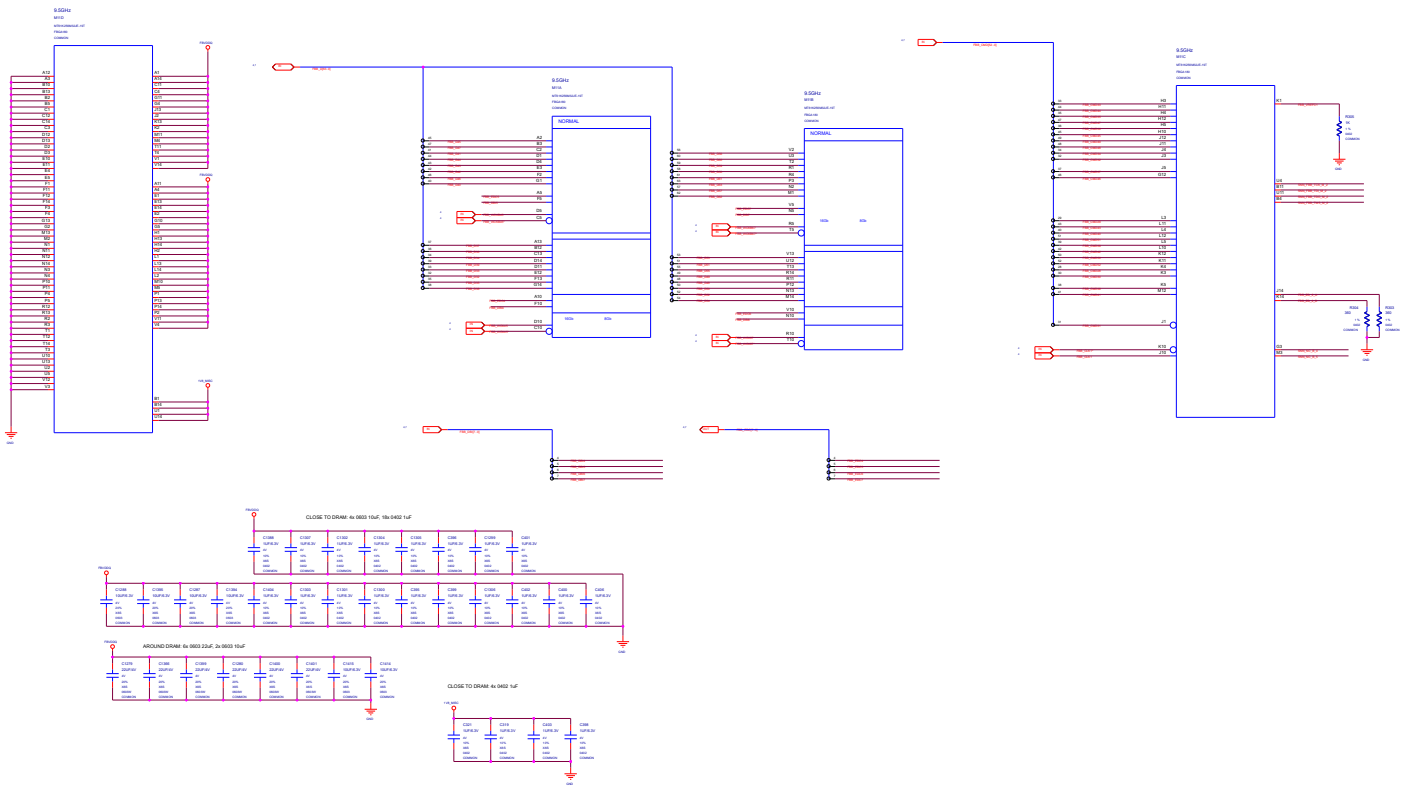
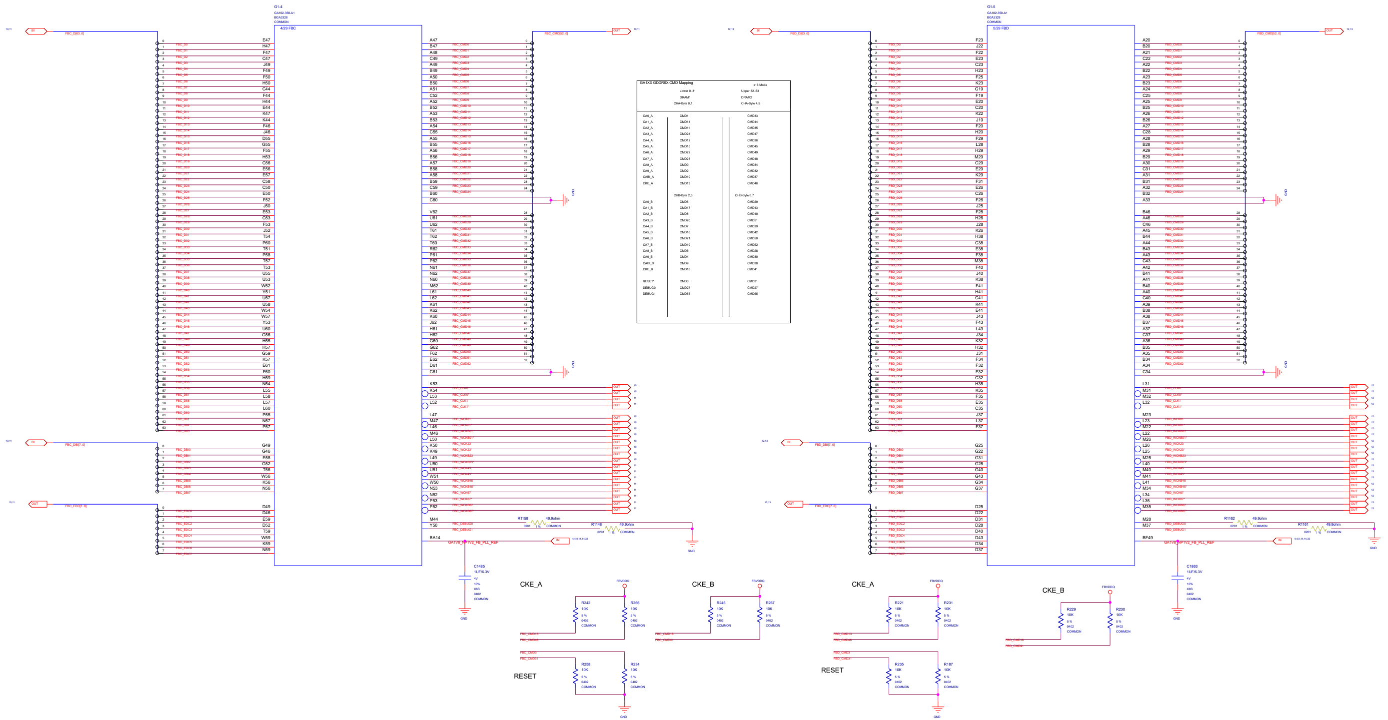
Page8: MEMORY: FBB Partition 63..32

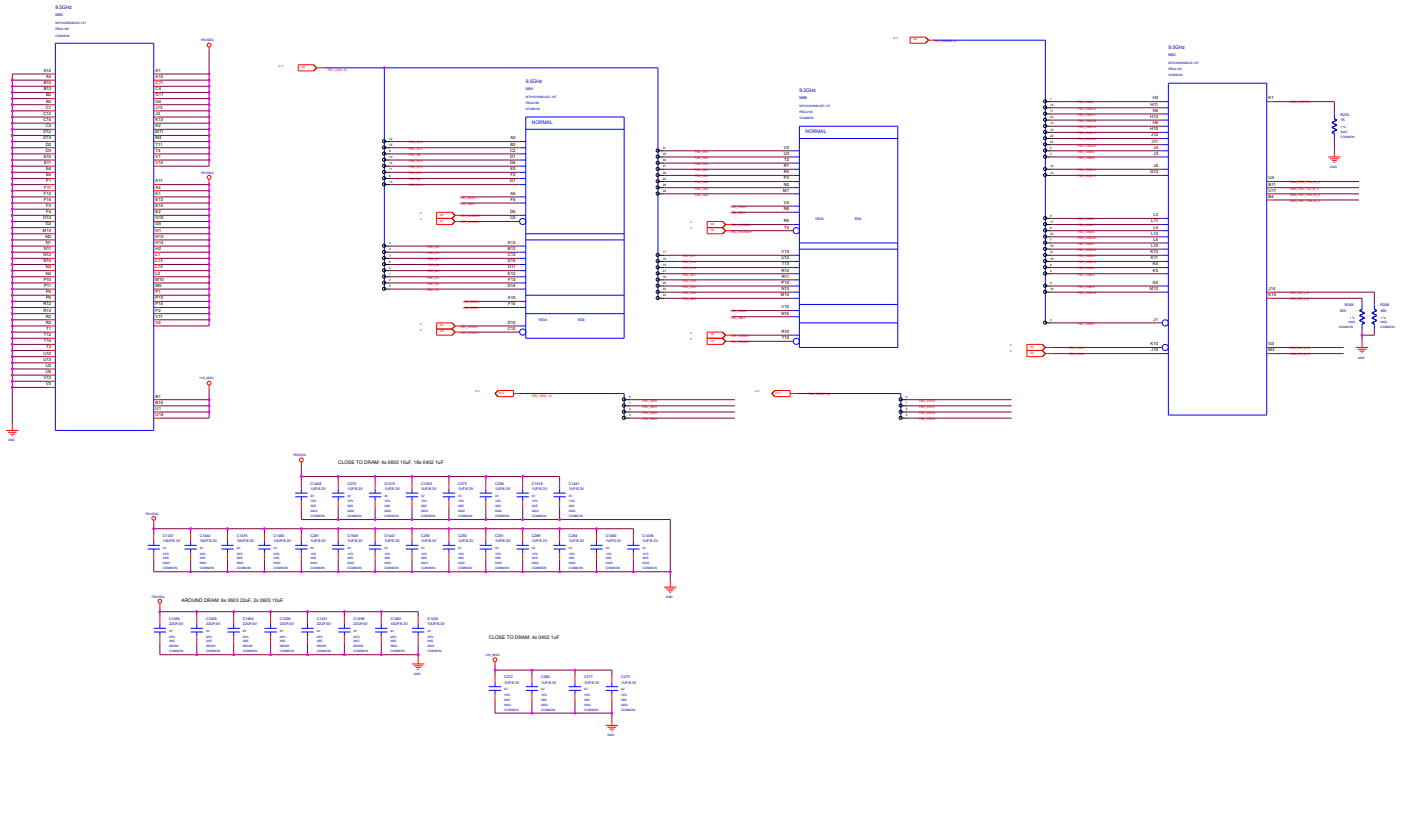


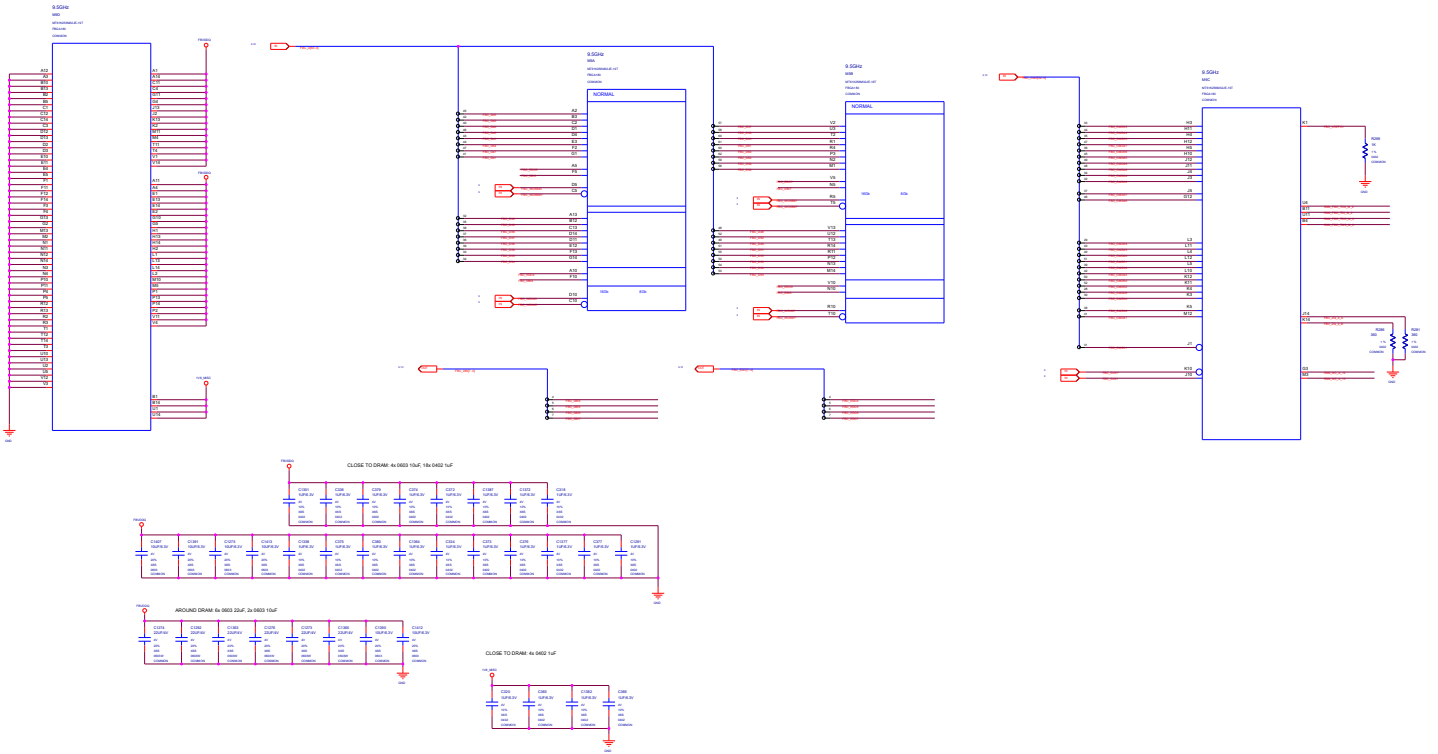
Page 9: MEMORY: GPU Partition C/D



GA1XX GDDR6X CMD Mapping

	x16 Mode	
	Lower 0..31	Upper 32..63
	DRAM1	DRAM2
	CHA-Byte 0,1	CHA-Byte 4,5
CA0_A	CMD1	CMD33
CA1_A	CMD14	CMD44
CA2_A	CMD11	CMD35
CA3_A	CMD24	CMD47
CA4_A	CMD12	CMD36
CA5_A	CMD15	CMD45
CA6_A	CMD22	CMD49
CA7_A	CMD23	CMD48
CA8_A	CMD0	CMD34
CA9_A	CMD2	CMD32
CABI_A	CMD10	CMD37
CKE_A	CMD13	CMD46
	CHB-Byte 2,3	CHB-Byte 6,7
CA0_B	CMD5	CMD29
CA1_B	CMD17	CMD43
CA2_B	CMD8	CMD40
CA3_B	CMD20	CMD51
CA4_B	CMD7	CMD39
CA5_B	CMD16	CMD42
CA6_B	CMD21	CMD50
CA7_B	CMD19	CMD52
CA8_B	CMD6	CMD28
CA9_B	CMD4	CMD30
CABI_B	CMD9	CMD38
CKE_B	CMD18	CMD41
RESET*	CMD3	CMD31
DEBUG0	CMD27	CMD27
DEBUG1	CMD55	CMD55


9.5GHz
NORMAL
CLOSE TO DRAM: 4x 0603 10uF, 18x 0402 1uF
AROUND DRAM: 6x 0603 22uF, 2x 0603 10uF
CLOSE TO DRAM: 4x 0402 1uF
Title : FBC Partition 31..0
Engineer: Hariston_huang
CYG1393PB02



Title :	FBC Partition 63..32		
Engineer:	Hariston_huang		
Size:	Project Name:	Rev:	
Custom	CG1393PBI2	1.0(0)	
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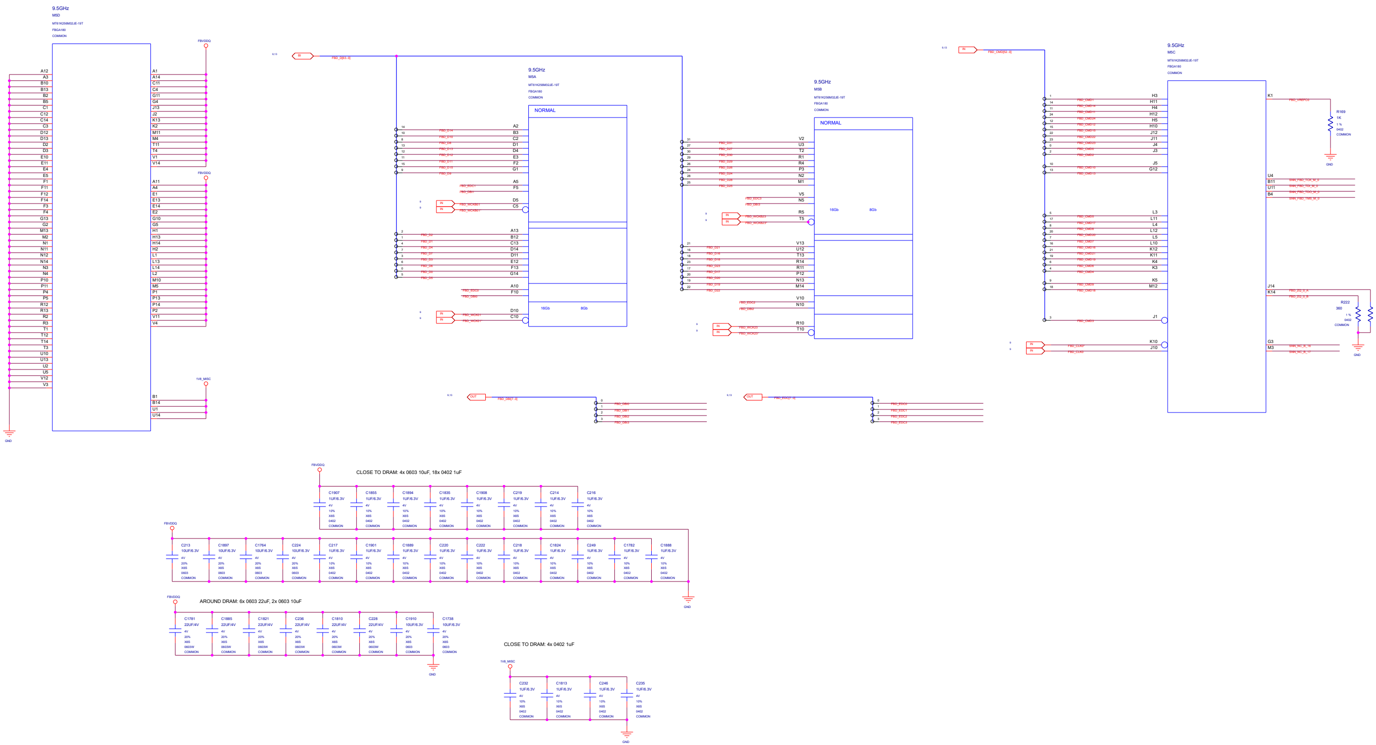
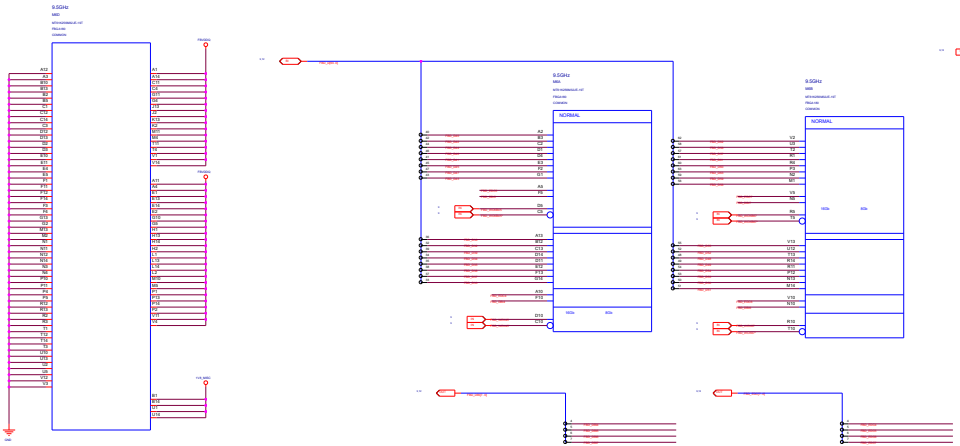
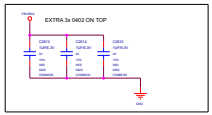
Page 12: MEMORY: FBD Partition 31..0

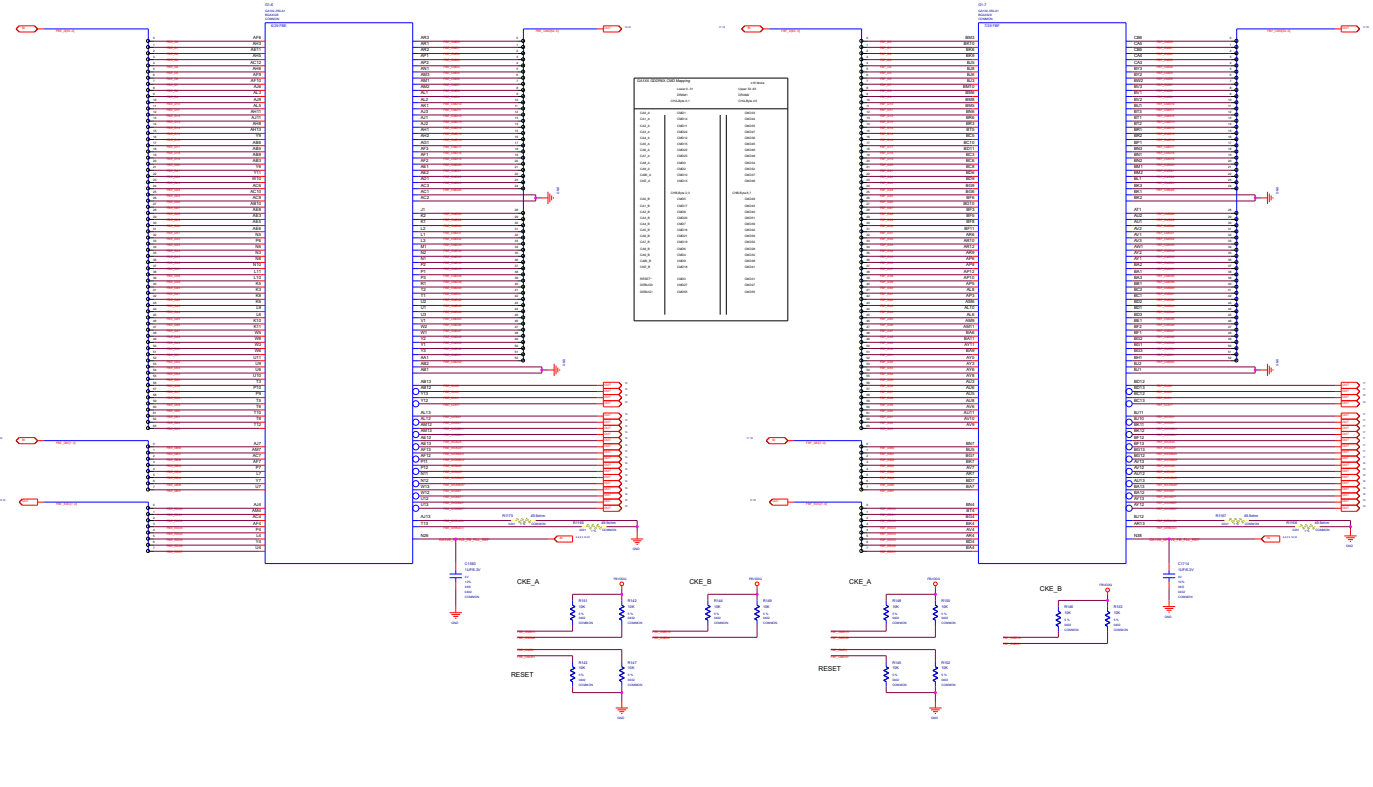


Title :	FBD Partition 31..0
<OrgName> Engineer:	Hariston_huang
Size: Custom	Project Name: CG1393PBI2
Rev	1.00X
Date:	Wednesday, December 21, 2022





Title :	FBD Partition 63..32		
Engineer:	Harlston_huang		
Size	Project Name		Rev
Custom	CG13993PB12		1.000
Date:	Wednesday, December 11, 2013	Sheet	13 of 21



ASUS	Title :	GPU Partition E/F	
<Engineer>	Engineer:	Harlston_huang	
Size: Custom	Project Name:	CG1393PBI2	Rev: 1.0XX
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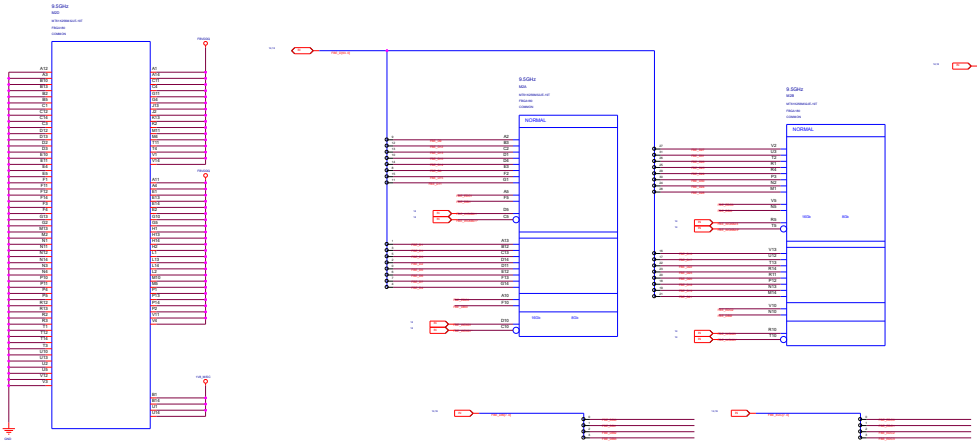
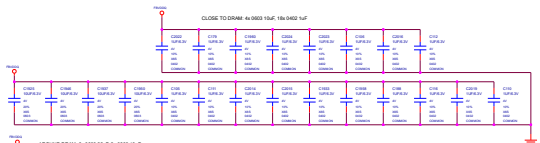
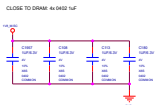
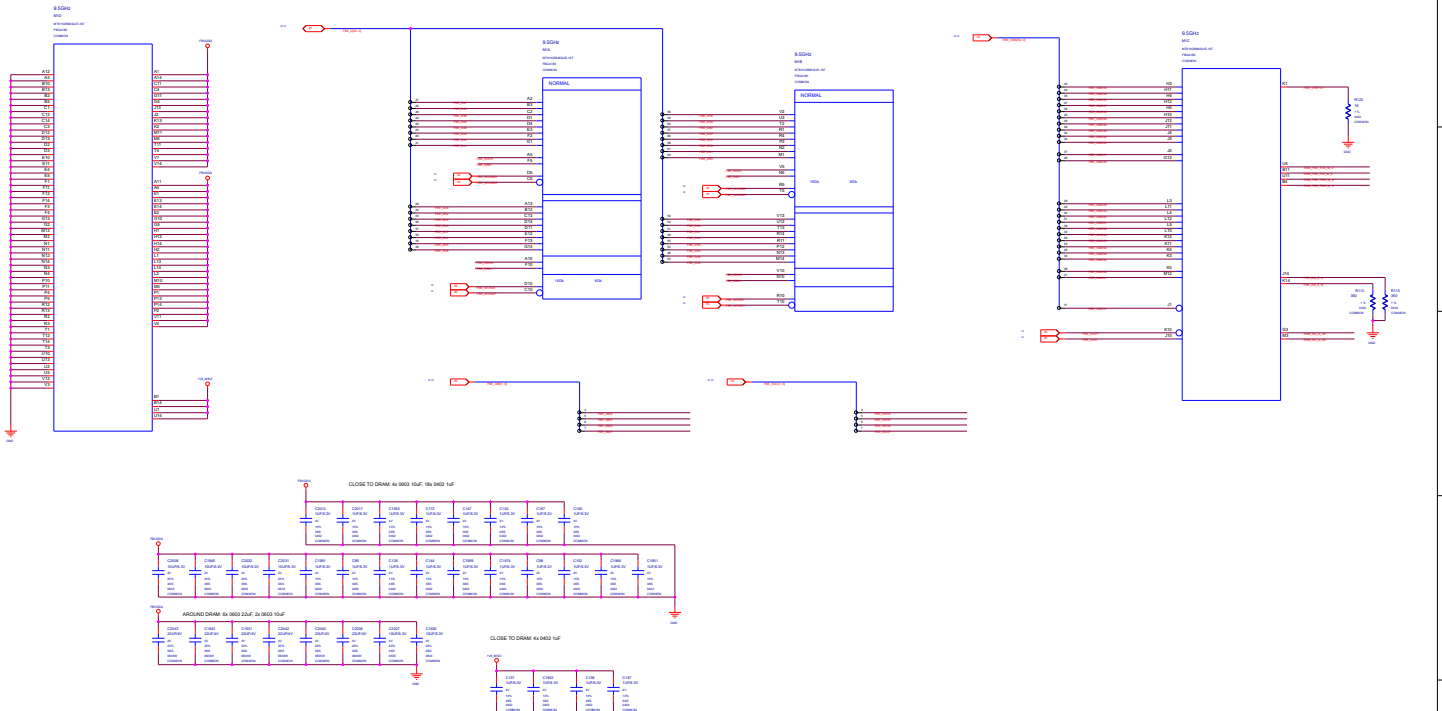



CLOSE TO DRAM: 4x 0603 10uF; 18x 0402 1uF
AROUND DRAM: 6x 0603 22uF; 2x 0603 10uF


CLOSE TO DRAM: 4x 0402 1uF


Title :
FBE Partition 31..0
Engineer:
Harlston_huang
Project Name:
CG1393PBI2
Rev:
1.000
Wednesday, December 22, 2021



Title :	FBE Partition 63..32		
Engineer:	Harlston_huang		
Size	Project Name		Rev
Custom	CG1393PBI2		1.0(0)
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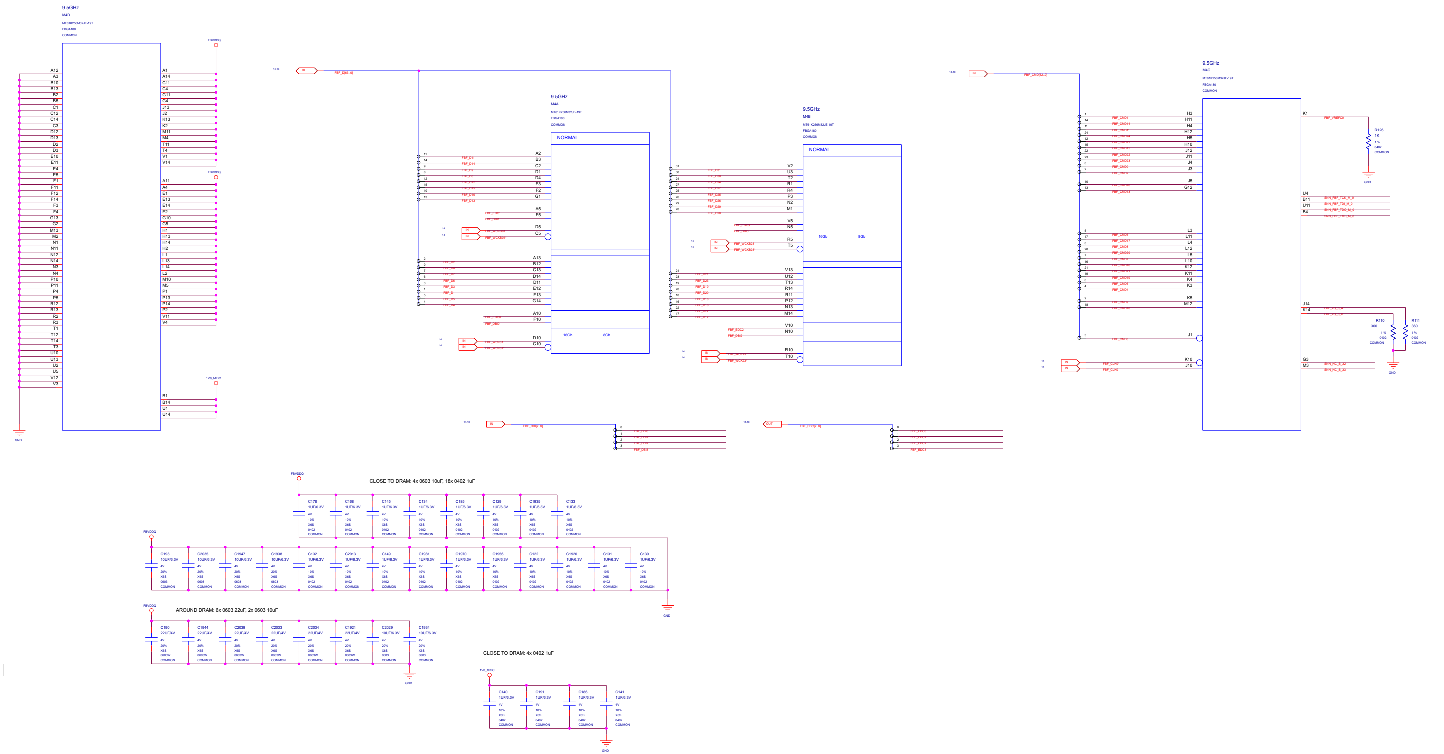
Page 17: MEMORY: FBF Partition 31..0



Title : FBF Partition 31..0

Engineer: Hariston_huang

<OrgName>

Size	Project Name	Rev
Custom	CG1393PBI2	1.00X

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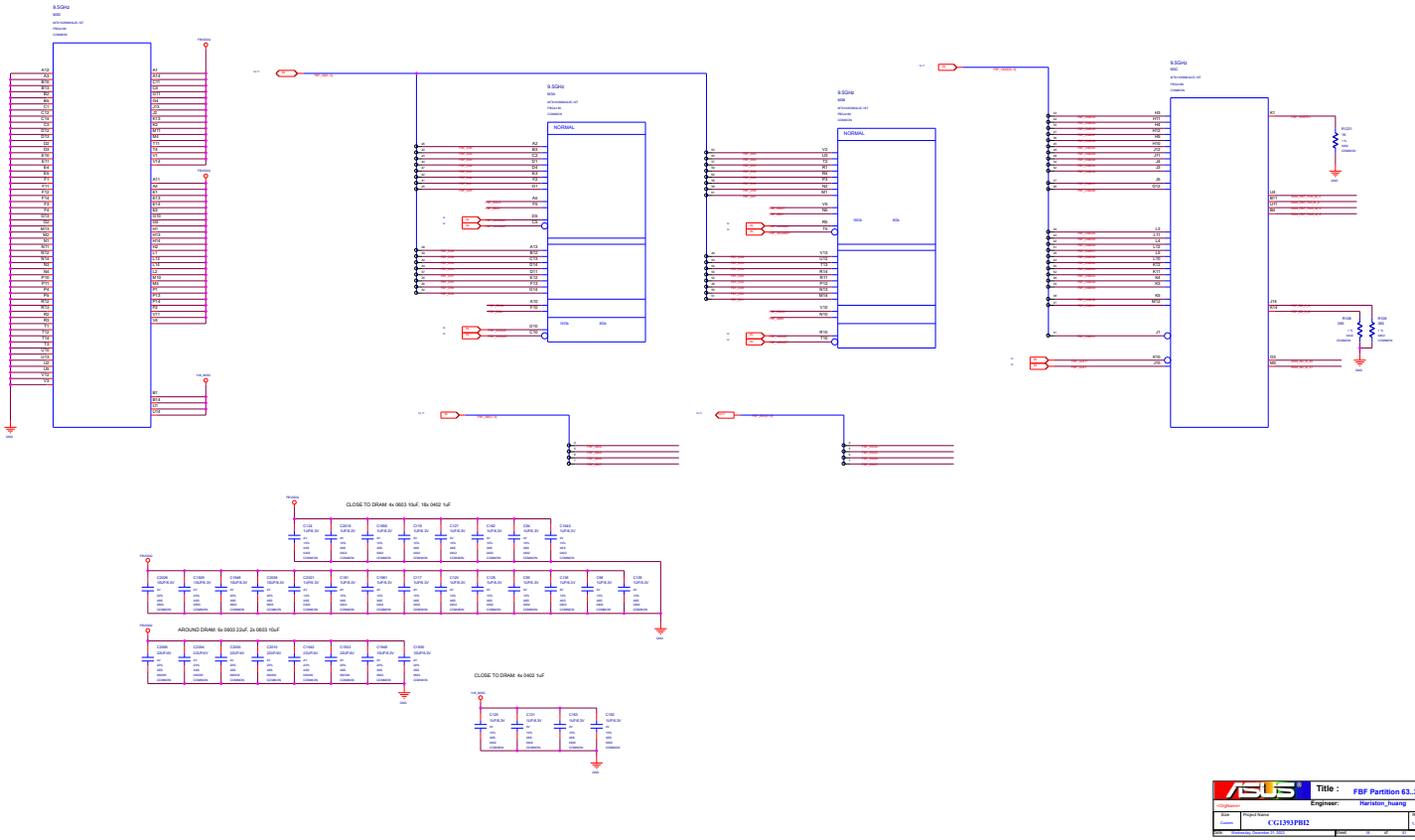
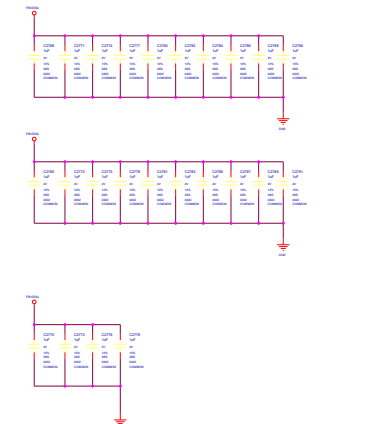


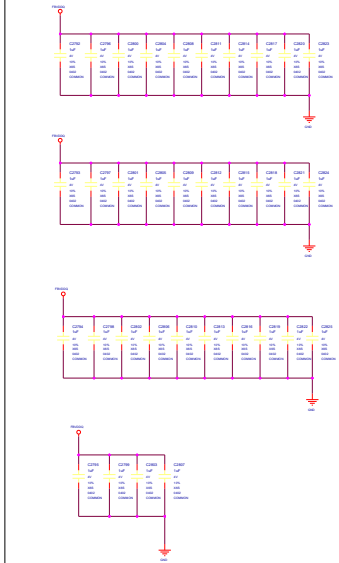
Title :	FBF Partition 63..32		
Engineer:	Harrison_huang		
Size	Project Name	Rev	
Custom	CG1393PBI2	1.0G0	
Date:	Wednesday, December 01, 2021	Sheet	18 of 37

Page 19: MEMORY DECOUPLING

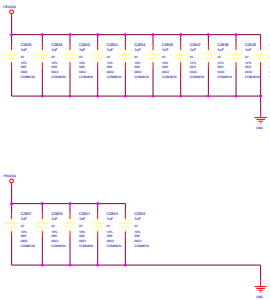
PER SI REQUIREMENT, RESERVE MORE 0402 1UF AROUND DRAM



PLACE AROUND WEST DRAM



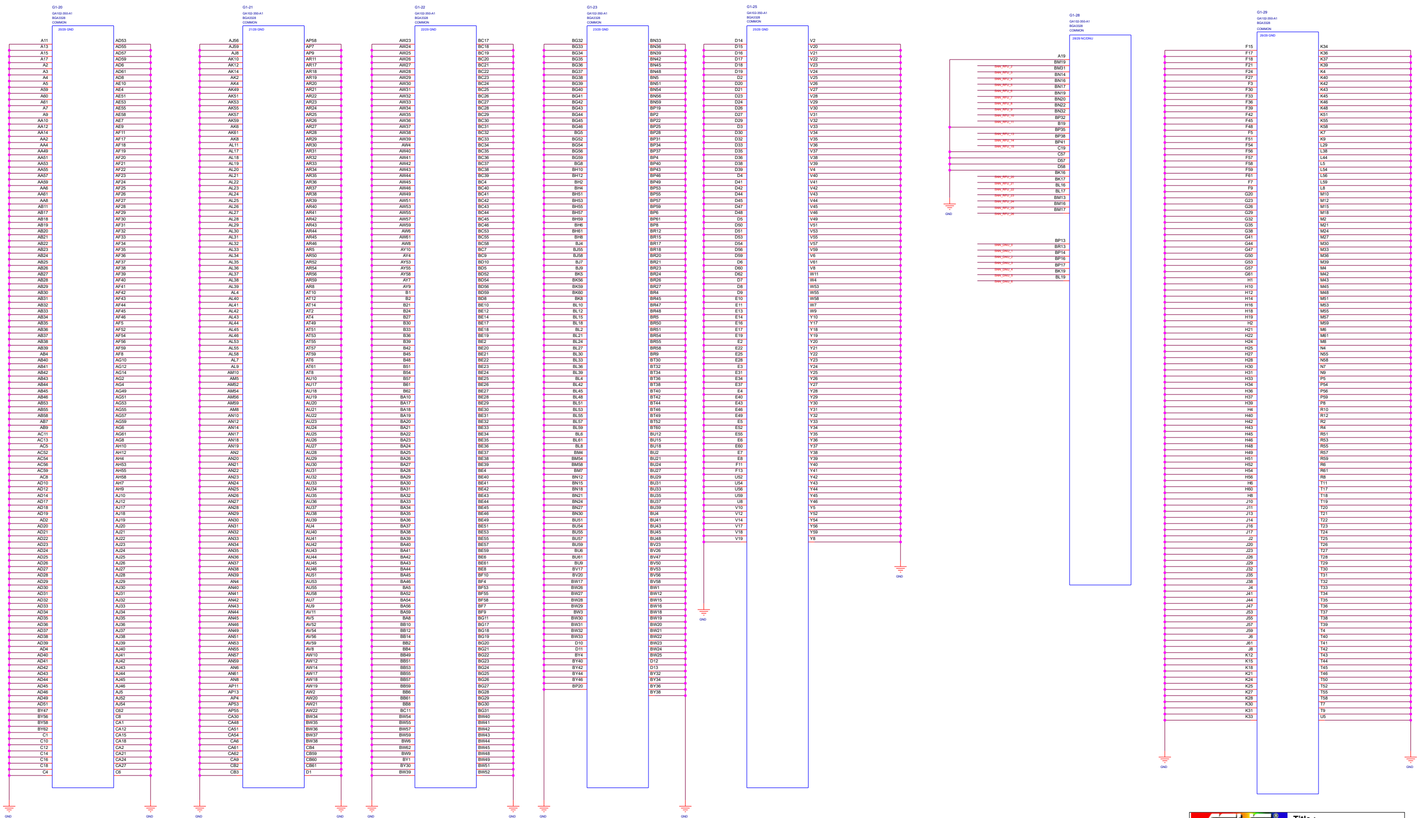
PLACE AROUND EAST DRAM



PLACE UPPER/LOWER MIDDLE

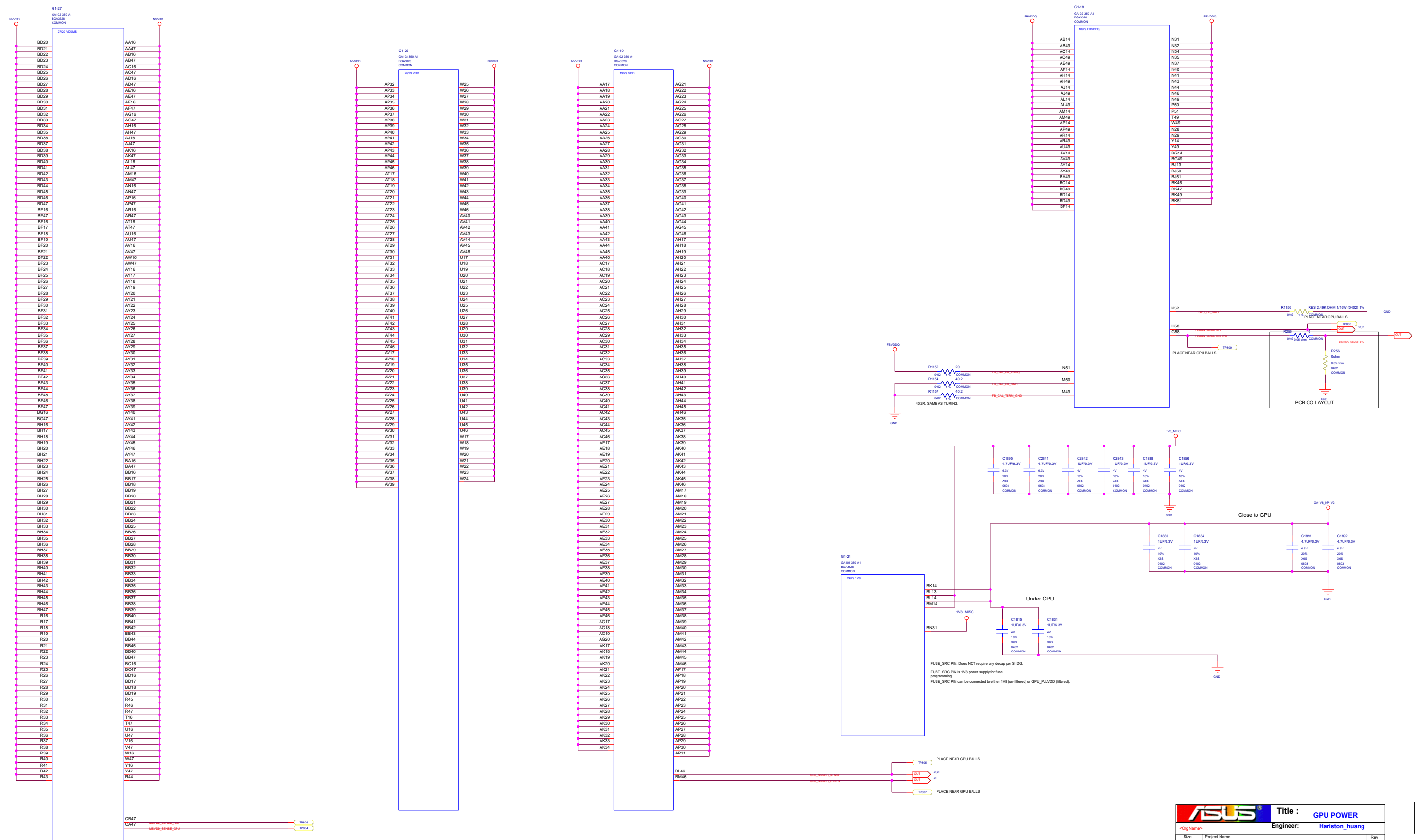
Title :	MEMORY DECOUPLING	
Engineer:	Harlston_huang	
Project Name:	CG1393PB12	Rev: 1.0G0
Date: Wednesday, December 01, 2010	Sheet	19 of 51

Page20: GPU: GND, NC



Title :	GPU: GND, NC
Engineer:	Hariston_huang
Size: Custom	Project Name: CG1393PBI2
Rev	1.00X
Date: Wednesday, December 21, 2022	Sheet 20 of 61

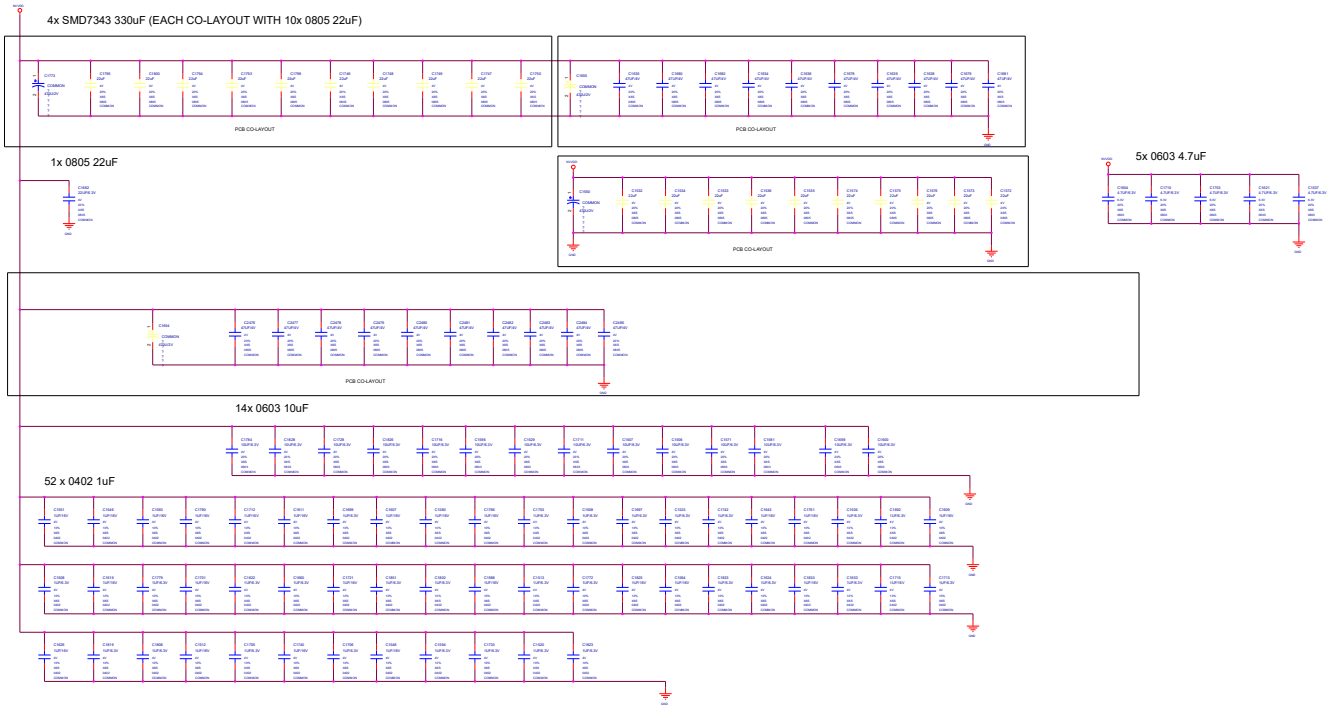
Page21: GPU POWER



ASUS	Title :	GPU POWER	
<OrgName>	Engineer:	Hariston_huang	
Size: Custom	Project Name: CG1393PBI2		Rev: 1.00X
Date: Wednesday, December 21, 2022	Sheet 21 of 61		

NVVDD

UNDER GPU

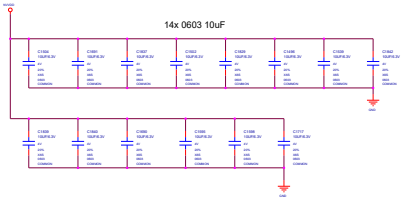


Title :	NVVDD DECOUPLING(1/2)		
<Orghierarchy>	Engineer:	Harrison_hsiang	
Size: Custom	Project Name: CG1393PB12		Rev: 1.0GS
Date: Wednesday, December 21, 2022	Sheet	of	

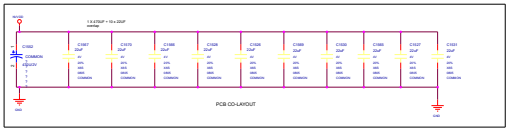
NVVDD

UNDER GPU

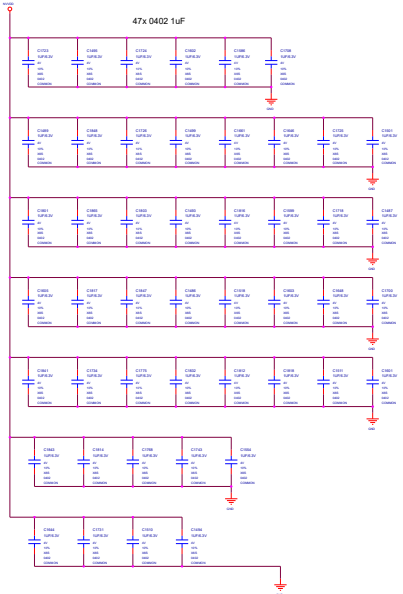
14x 0603 10uF



2x SMD7343 330uF (EACH CO-LAYOUT WITH 10x 22uF 0805)



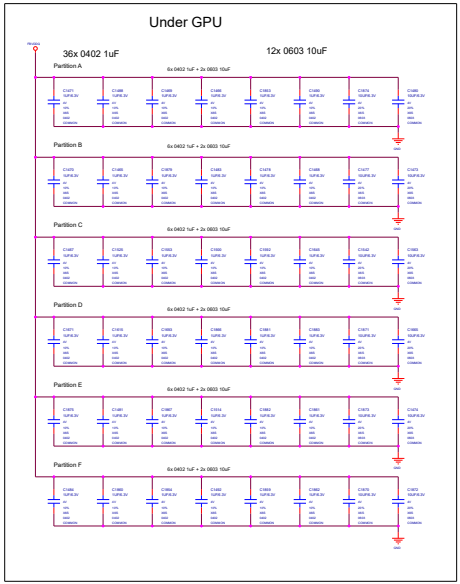
47x 0402 1uF

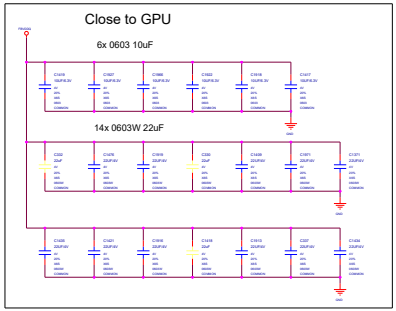


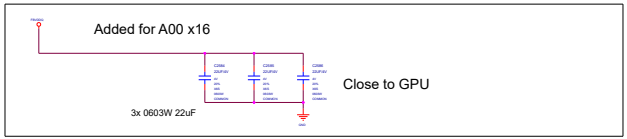
REMOVED 3X 1uF 0402 DUE TO SPACE RESTRICTION

Title :	NVVDD DECOUPLING(2/2)		
Engineer:	Harlston_huang		
Size: Custom	Project Name: CG1393PB12	Rev: 1.0GE	
Date: Wednesday, December 21, 2022	Sheet 23 of 33		

FBVDDQ

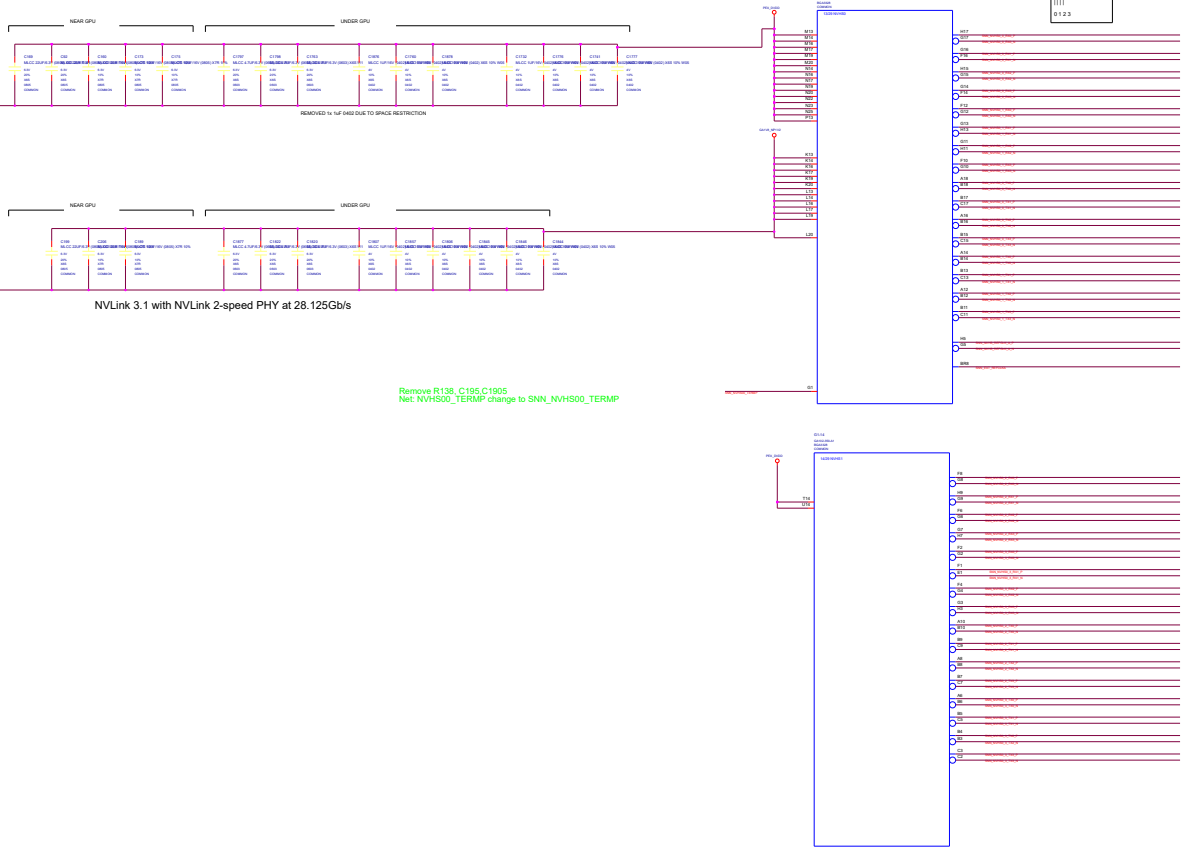




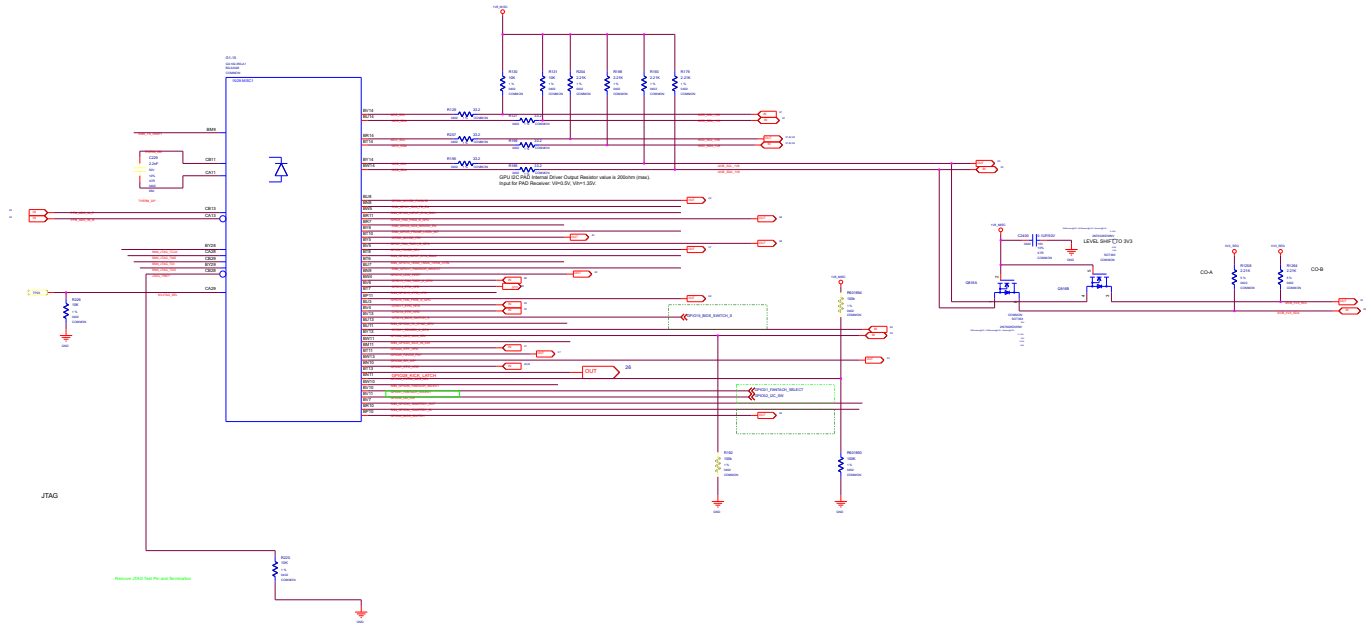


Title :	FBVDD DECOUPLING		
Engineer:	Harlston_huang		
Size	Project Name	Rev	
Custom	CG1393PB12	1.00A	
Date: Wednesday, December 04, 2019		Sheet 24 of 51	

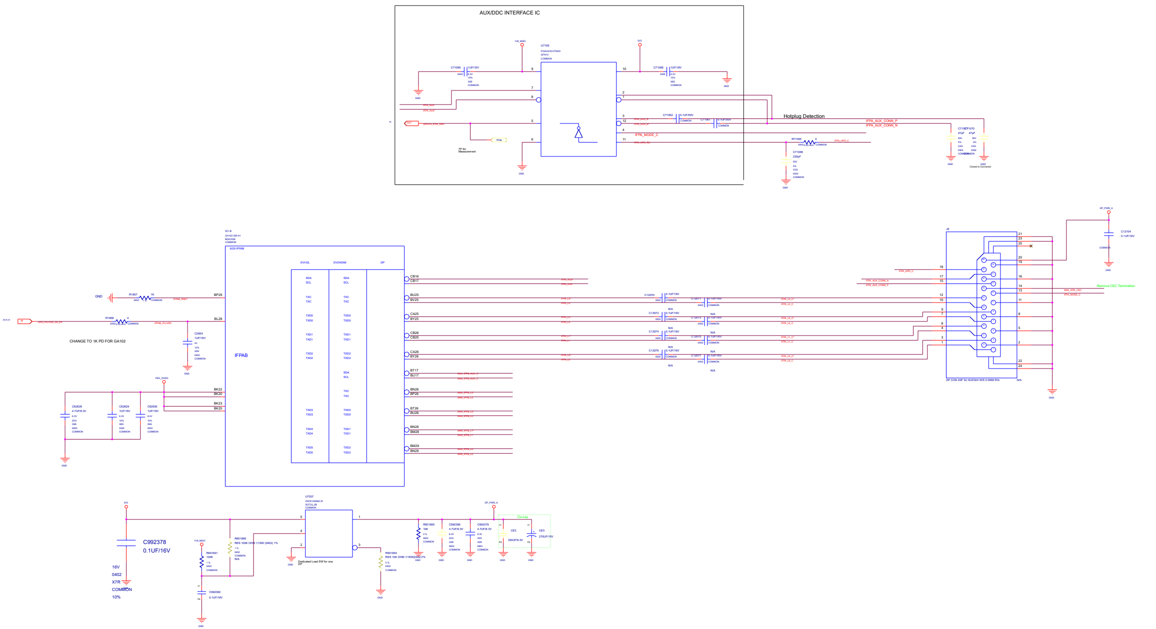
NVLINK Lane Reversal: 4xTX / 4xRX Lanes per NVLINK 3.1 Link can do Lane Reversal Independantly (to optimize routings)



Title :	NVHS x16		
Engineer:	Harrston_Huang		
Size	Project Name		Rev
Custom	CG1393PIB2		1.00A
Date:	Wednesday, December 21, 2022	Sheet	25 of 51



Title :	GPIO, THERMAL, JTAG		
<Org Name>	Engineer:	Harrison_huang	
Size: Custom	Project Name: CYG1393PBI2		Rev: 1.00X
Date: Wednesday, December 21, 2022	Sheet 26 of 30		



ASUS

Title : IFPAB (DP)

Engineer: Hariston_huang

Project Name: CG1393PBI2

Rev 1.00X

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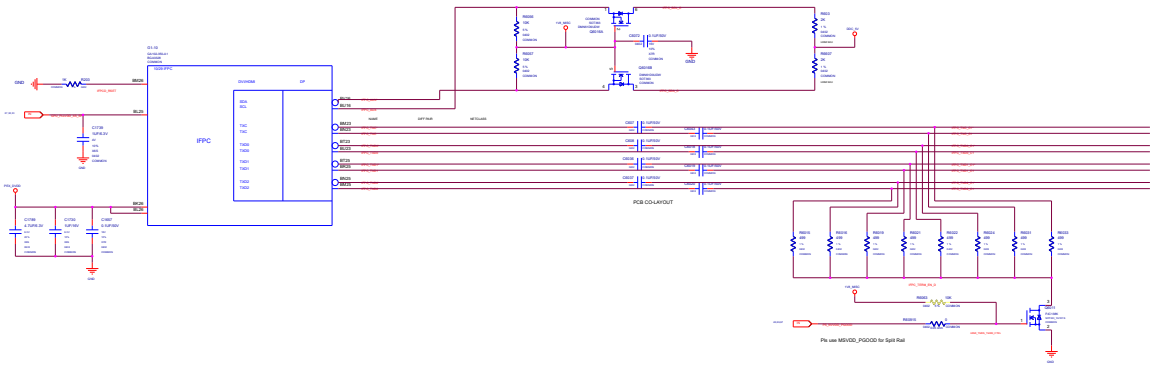
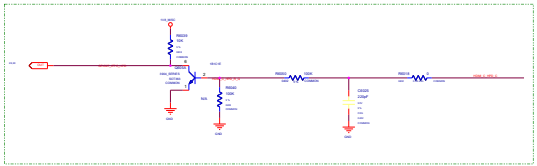
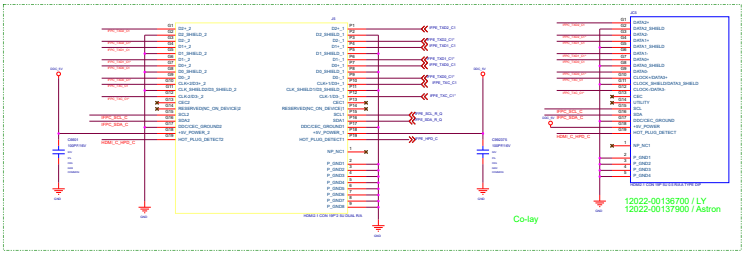
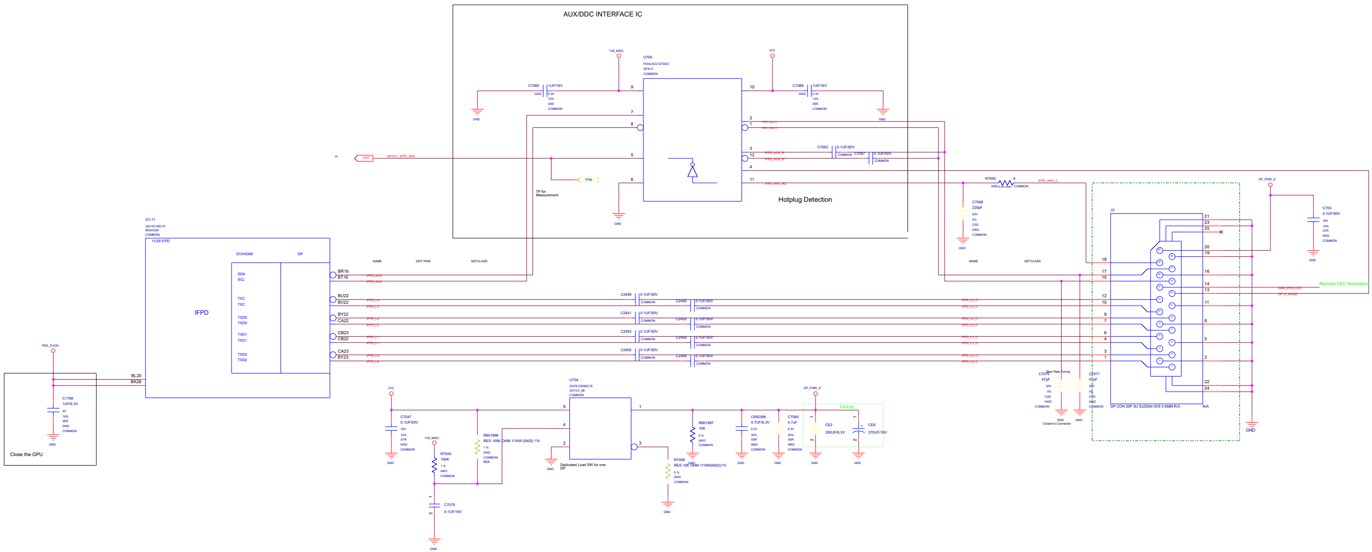




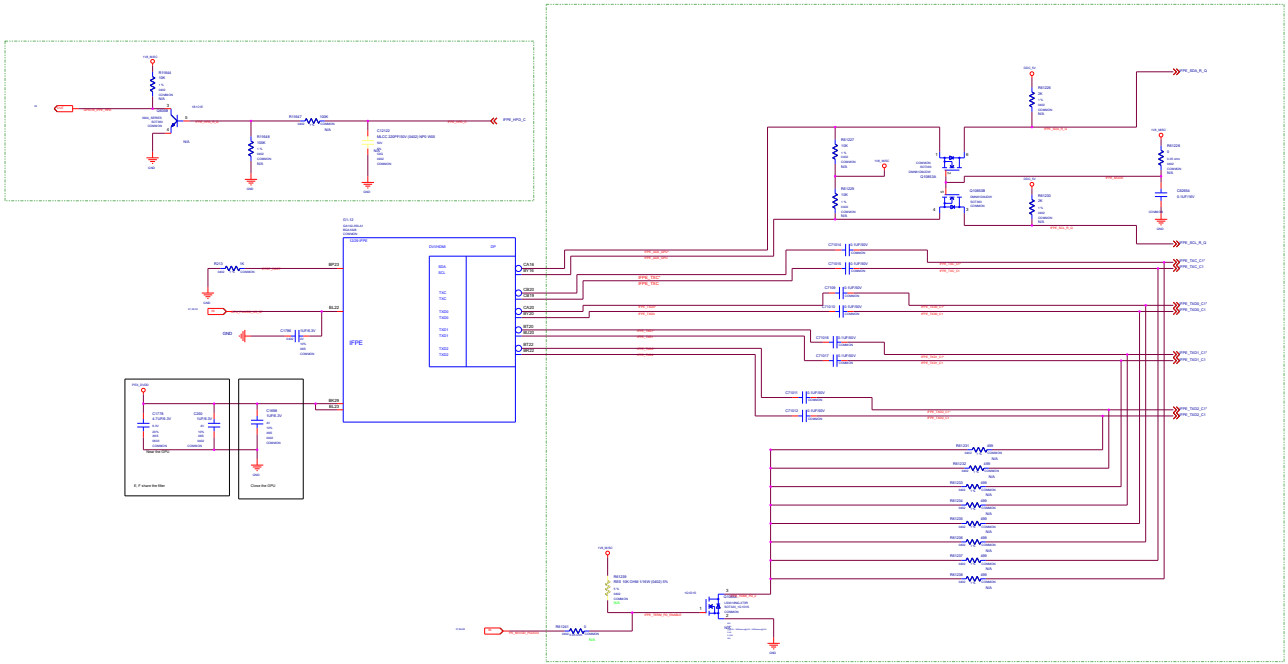


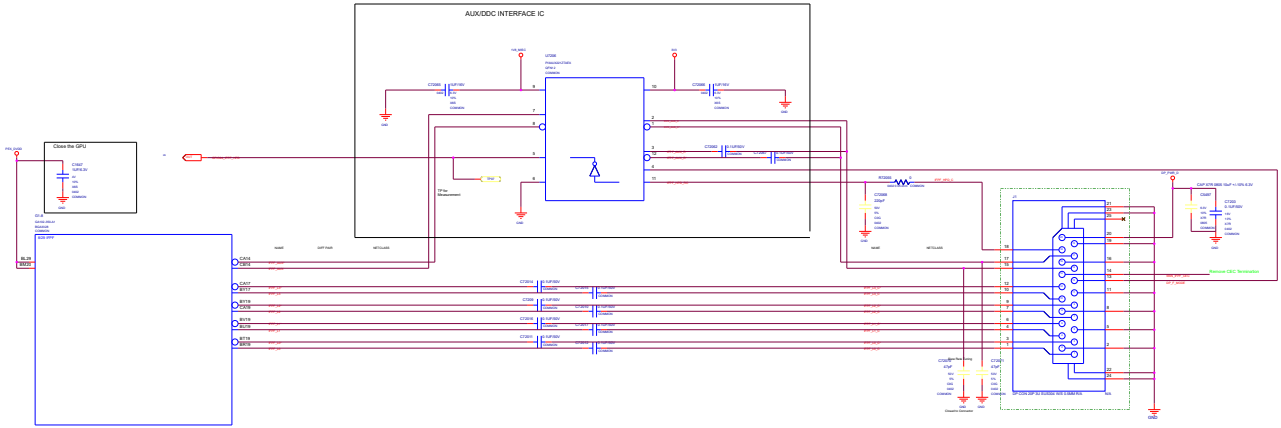
Title :	IFPC HDMI 2.1		
Engineer:	Harrison_huang		
Size	Project Name	Rev	
Custom	CG1393PH2	1.00A	
Date: Wednesday, November 01, 2023	Sheet 28 of 61		

Page 29: IFPD DP



<OrgName>	Title : IFPD DP		
	Engineer: Hariston_huang		
Size: Custom	Project Name: CG1393PBI2		Rev: 1.00X
Date: Wednesday, December 21, 2022	Sheet 29 of 61		


IFPE
Title : IFPE HDMI
Engineer: Harlston_huang
Project Name: CG1393PBI2
Rev: 1.00X
Wednesday, December 21, 2022



Title :	IFPF DP		
Engineer:	Hariston_huang		
Size: Custom	Project Name: CG1393PB12		Rev: 0.03
Date: Wednesday, December 21, 2022	Sheet 33 of 51		

Page 32: MISC: ROM, Straps

GROUP0

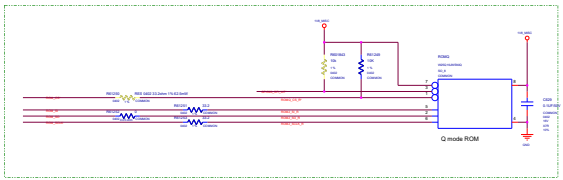
STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	
L	L	L	00000	RAMCFG MICRON 16Gb G6X x16 (161-0480-900)
L	L	H	00001	RAMCFG MICRON 16Gb G6X x16 (161-0479-900)
L	H	H	00011	
L	M	H	01010	
H	H	H	00111	

GROUP1

ROM_SO	ROM_SI	ROM_SCLK	SMARTFANZ:0[] FS_OVERT	
L	M	L	1001	FAN0/1=33%33%, FS_OVERT ENABLE

GROUP2

STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	PCIE_CFG	VGA_DEVICE
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1
L	L	L	0	0	0	0



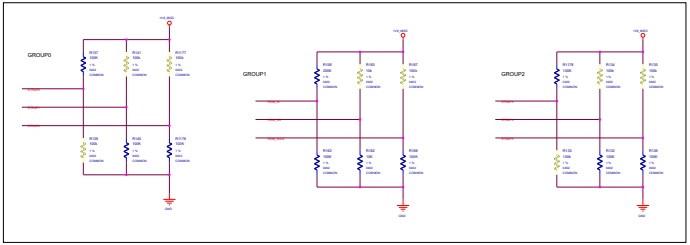
For NP, Middle Level should be 0.6V

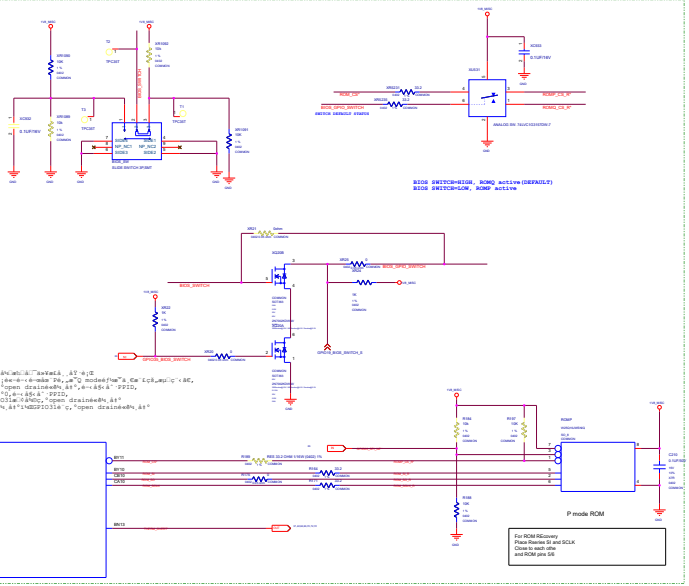
H=High :Tied to 1.8V

M=Middle:Tied to 0.9V

L=Low :Tied to 0V

DEFAULT





<=DEFAULT

1:SMB_ALT_ADDR ENABLE

0:SMB_ALT_ADDR DISABLE

1:DEVID_SEL REBRAND

0:DEVID_SEL ORIGNAL

1:PCIE_CFG LOW POWER

0:PCIE_CFG HIGH POWER

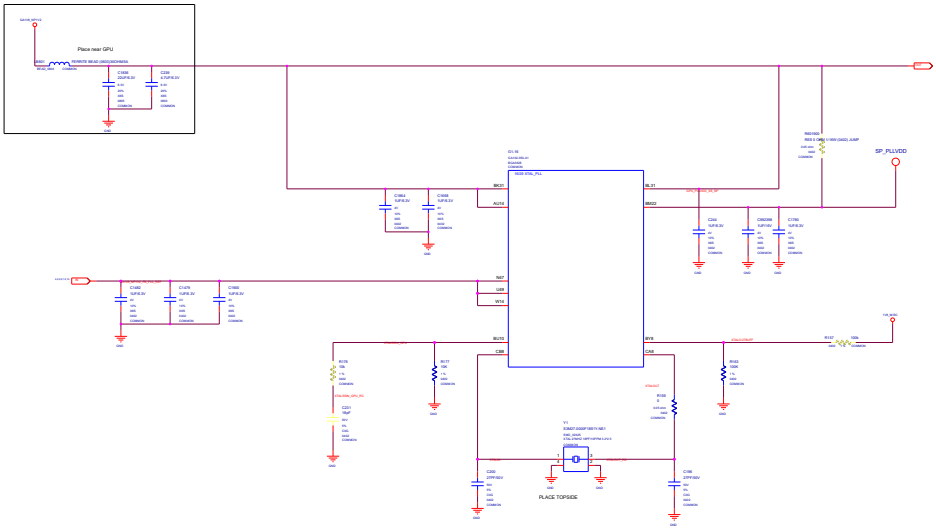
1:VGA_DEVICE ENABLE

0:VGA_DEVICE DISABLE

Default

SKU 200

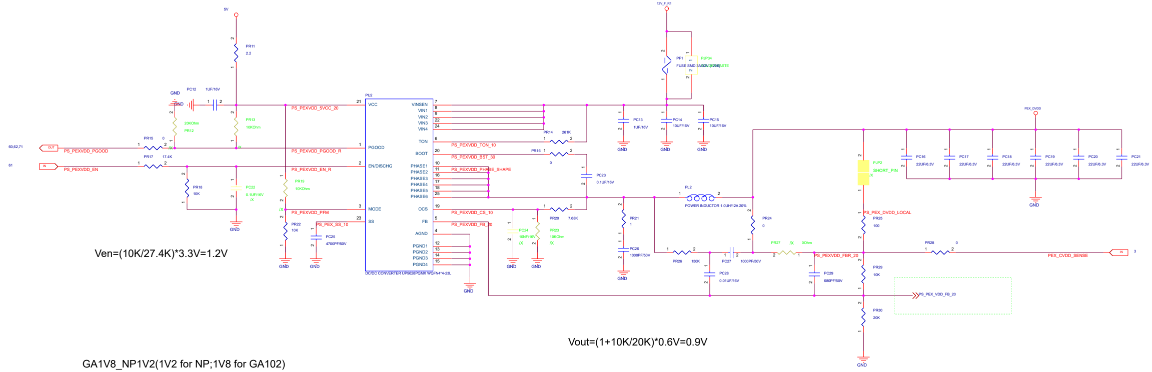
Size	Project Name				Rev	
Custom	CG1393PBI2				0.6A	
Date:	Wednesday, December 21, 2022	Sheet	32	of	52	



Title :	MISC: XTAL. PLL		
Engineer:	Harlston_huang		
Size	Project Name	Rev	
Custom	CG1393PB12	1.000	
Date:	Wednesday, December 22, 2010	Sheet	33 of 51

Page 35: PS: PEX_DVDD, GA1V8_NP1V2

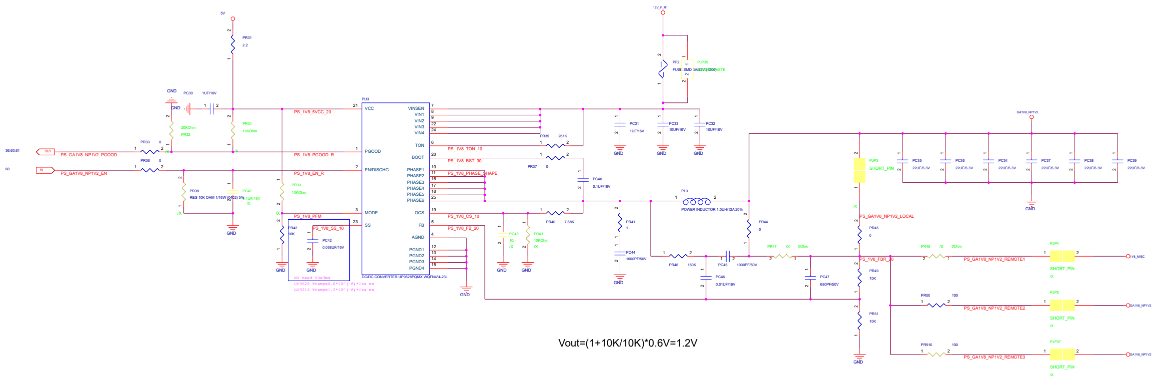
PEX_DVDD



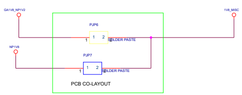
Ven=(10K/27.4K)*3.3V=1.2V

Vout=(1+10K/20K)*0.6V=0.9V

GA1V8_NP1V2(1V2 for NP;1V8 for GA102)

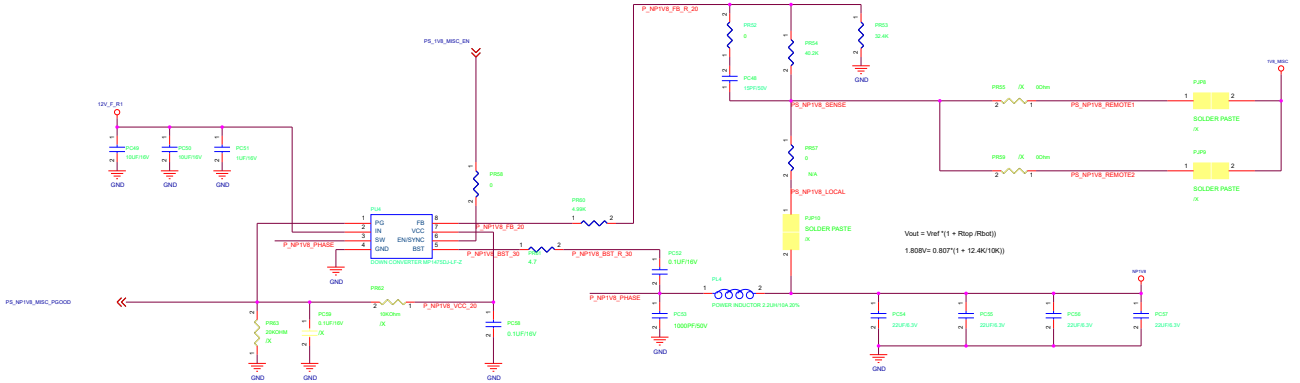


Vout=(1+10K/10K)*0.6V=1.2V



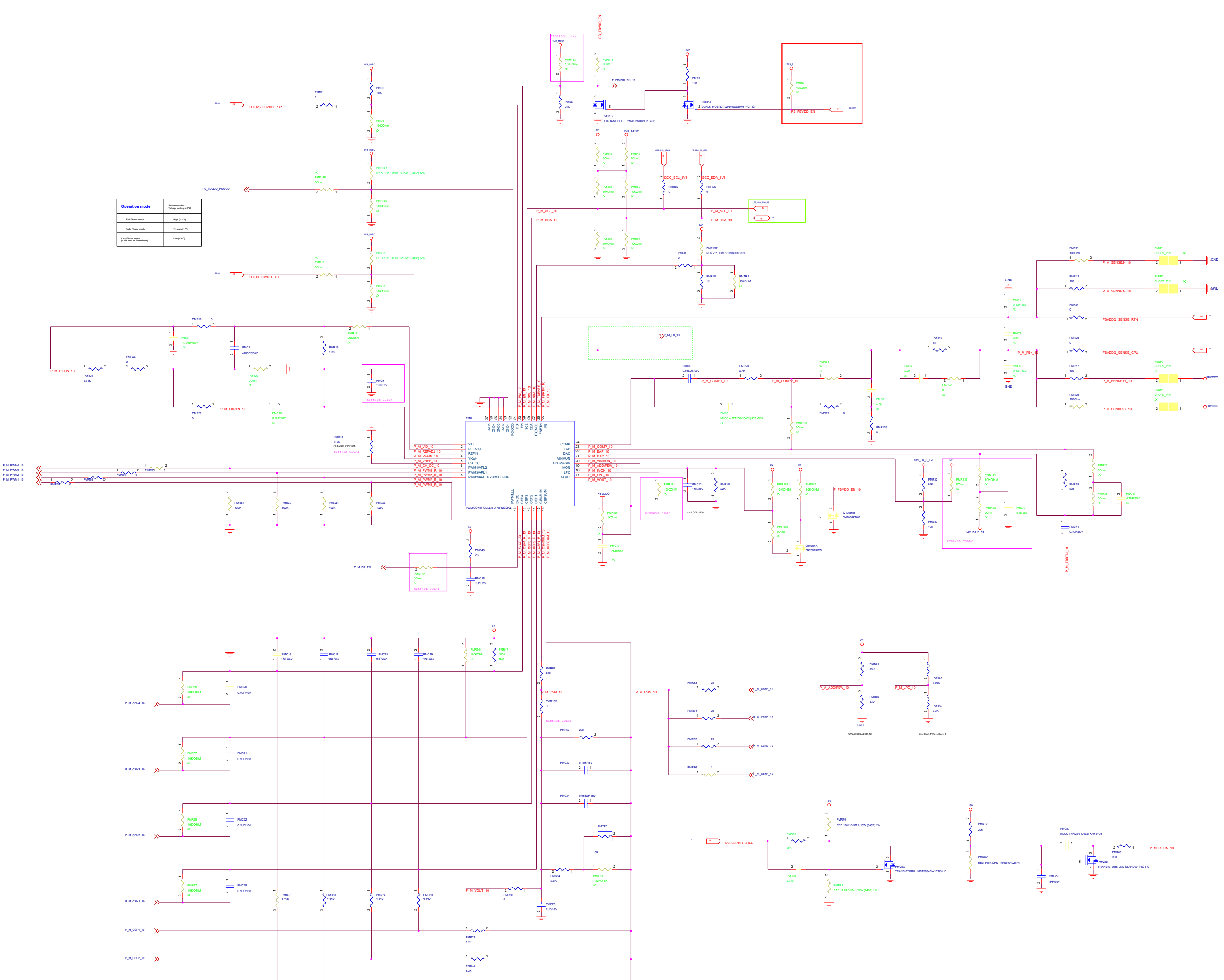
Title :	PEX_DVDD, GA1V8_NP1V2	
<OrgName>	Engineer: Hariston_huang	
Size: Custom	Project Name: CG1393PBI2	Rev: 1.00X
Date: Wednesday, December 21, 2022	Sheet 35 of 61	

Page 36: PS:NP1V8(NP ONLY),1V8_MISC



Vout=(1+40.2K/32.4K)*0.807V=1.808V

<OrgName>	Title :	NP1V8(NP ONLY),1V8_MISC	
	Engineer:	Hariston_huang	
Size: Custom	Project Name: CG1393PB12		Rev: 1.00X
Date: Wednesday, December 21, 2022	Sheet 36 of 61		

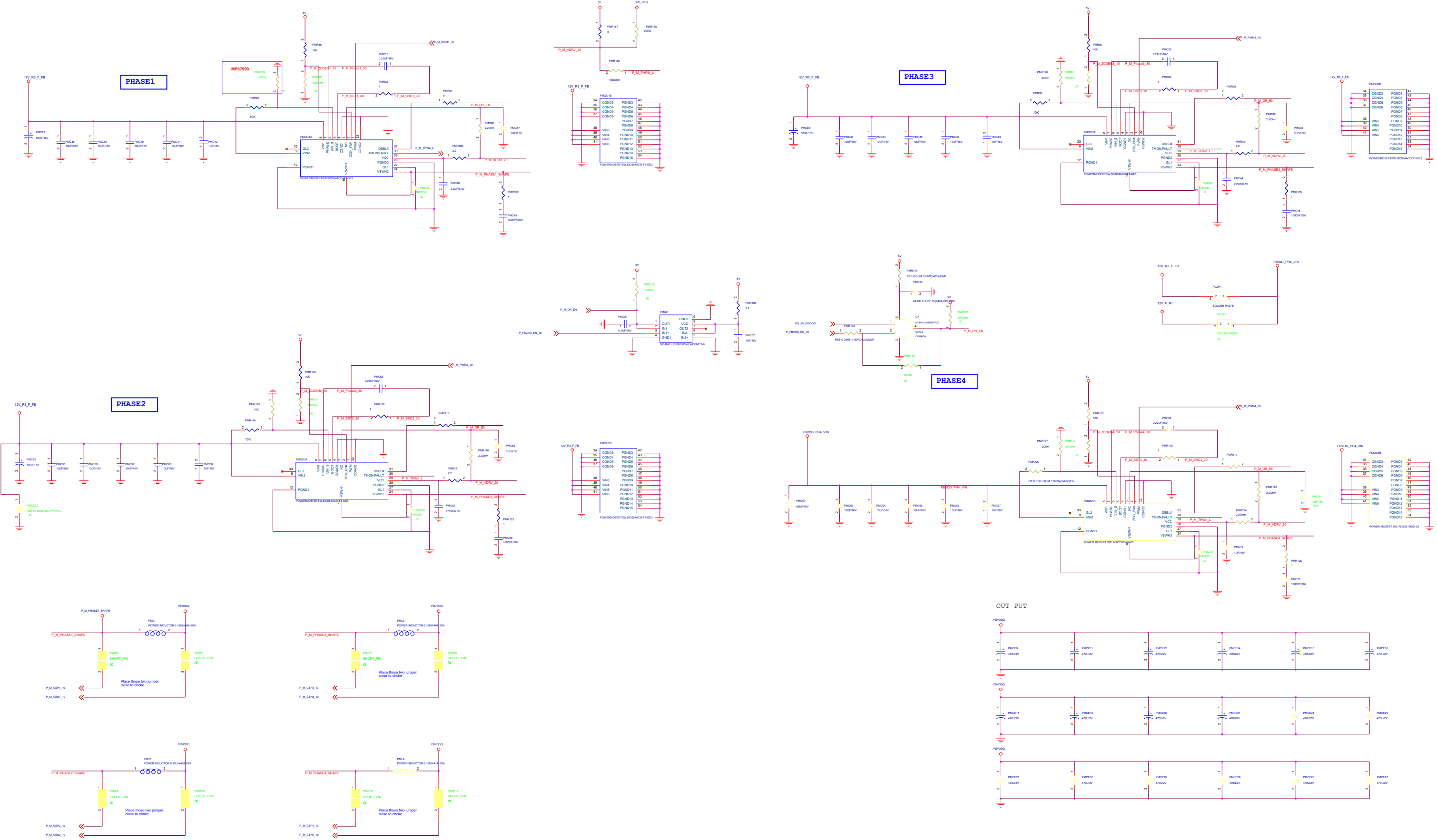


Operation mode	Recommended Voltage setting at PSI
Full-Phase mode	High (1.8 V)
Auto-Phase mode	Tri-state (1 V)
Low-Phase mode (Cold boot or Warm boot)	Low (GND)

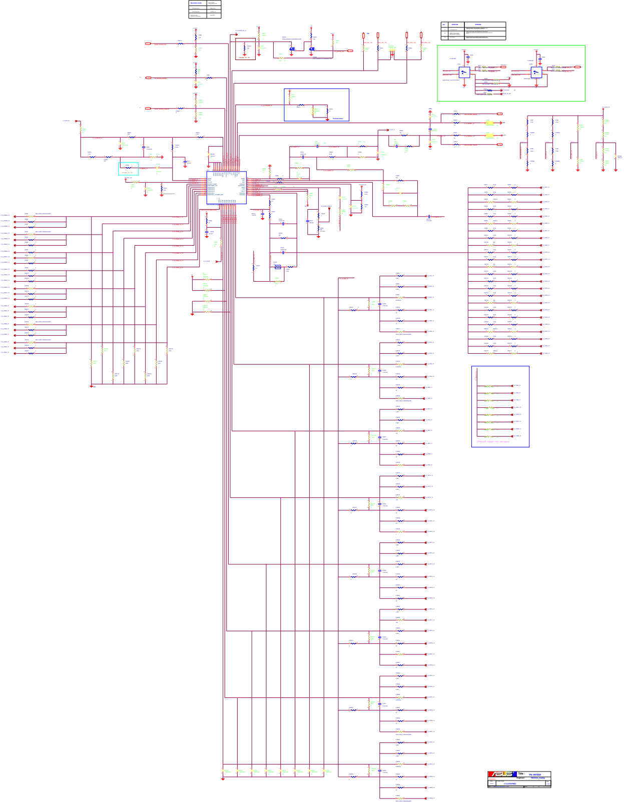
Title : PS: FBVDDQ
<OrgName>
Engineer: Hariston_huang

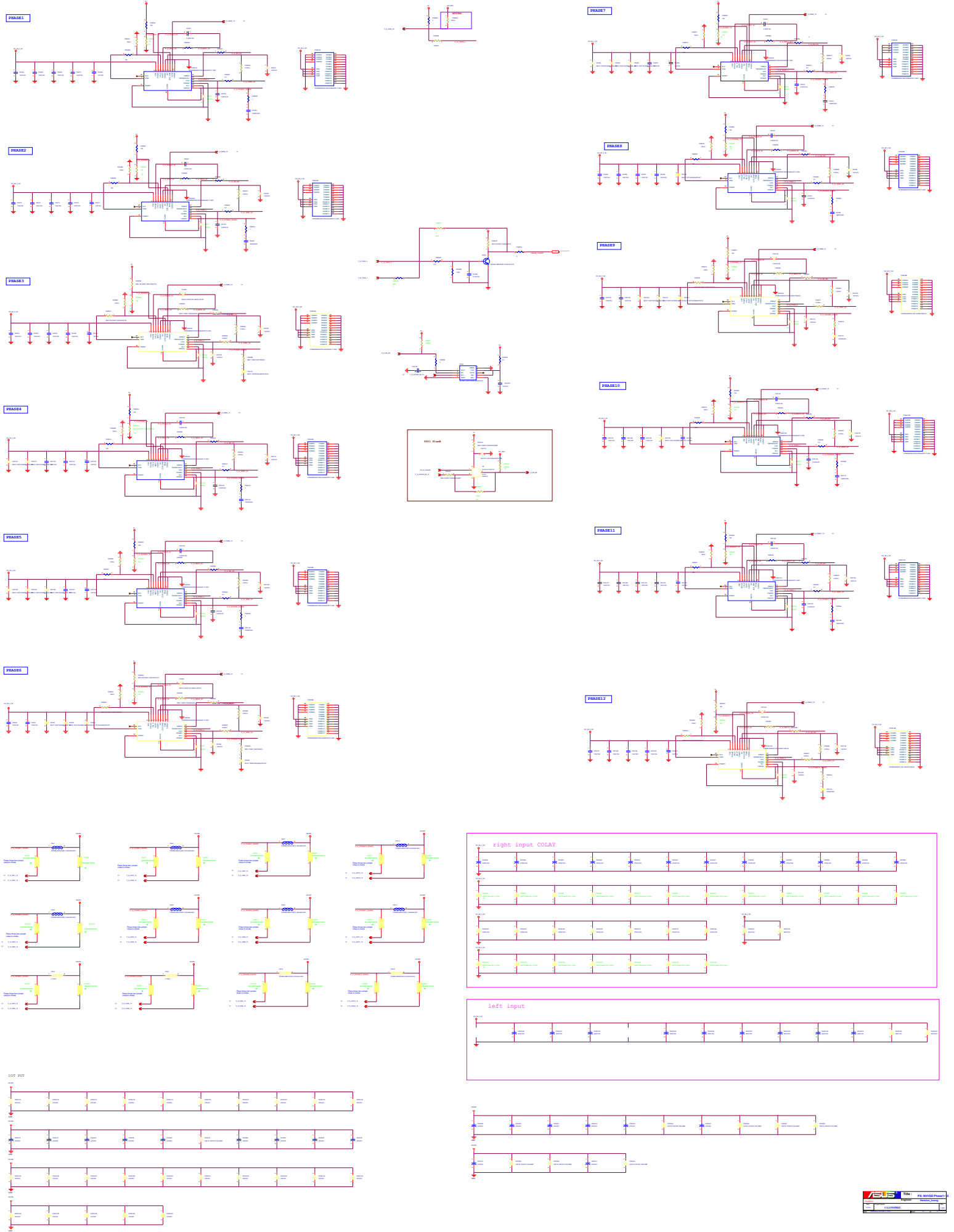
Size	Project Name	Rev
Custom	CG1393PBI2	1.00X

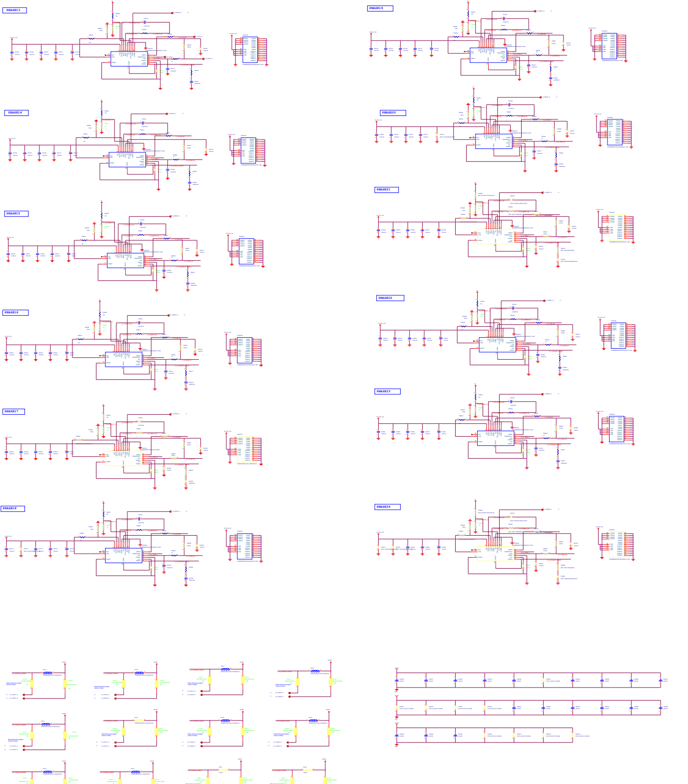
Date: Wednesday, December 21, 2022 Sheet 37 of 61



Title :	PS: FBVDDQ PH1~4		
<OrgName>	Engineer: Hariston_huang		
Size: D	Project Name: CG1393PBI2		Rev: 1.00X
Date: Wednesday, December 21, 2022	Sheet 38	of 61	


Operation mode
Title :
P8: NVVDD
Engineer:
Nelson_huang
CG32PXP8B2


PHASE1
PHASE2
PHASE3
PHASE4
PHASE5
PHASE6
PHASE7
PHASE8
PHASE9
PHASE10
PHASE11
PHASE12
SSD1 Flash
right input COLAY
left input
OUT PUT



Title : PS: NVVDD Phase13-24

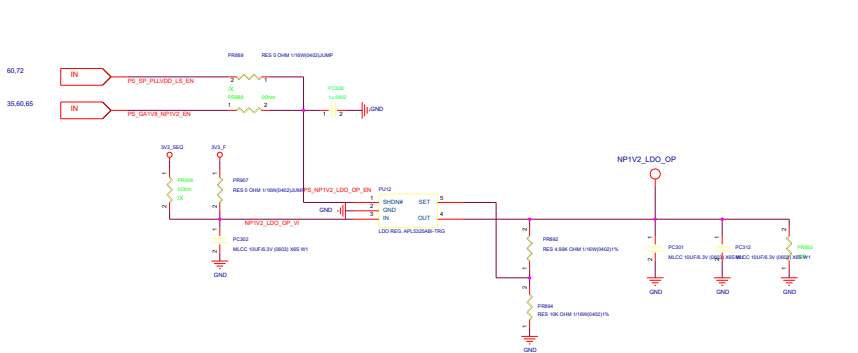
Engineer: Harision_huang

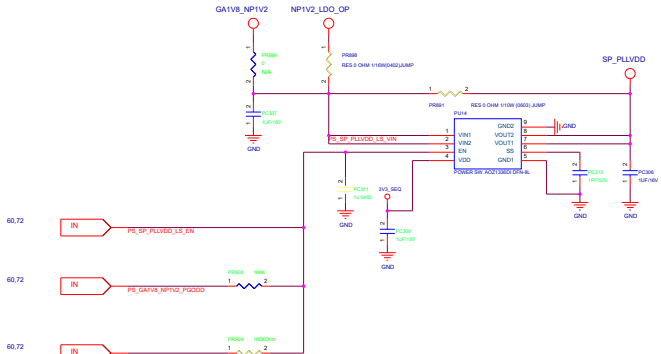
Page 41: PS: FBVDD OUTPUT CAP NEAR MEMORY

PLACE NEAR MEMORY

Title :	FBVDD OUTPUT CAP		
Engineer:	Hariston_huang		
Size	Project Name	Rev	
Custom	CG1393PB12	1.00A	
Date:	Wednesday, December 21, 2022	Sheet	41 of 71

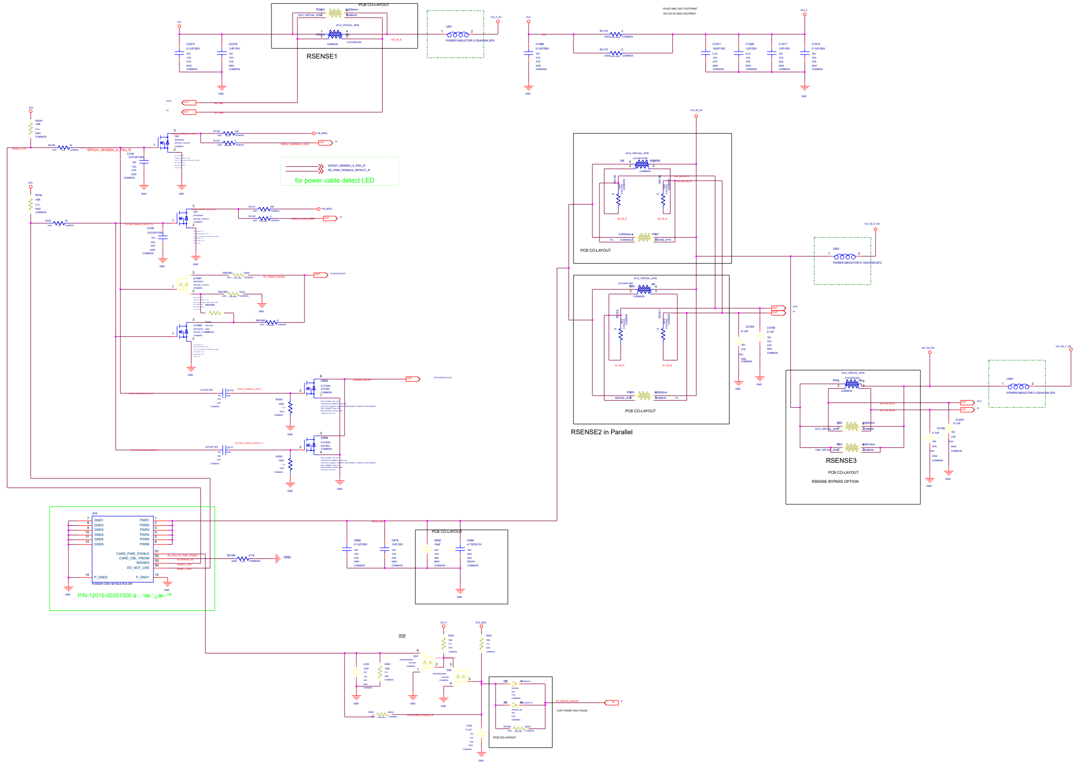
Page 60: SPPLLVDD_LDO_LOADSWITCH



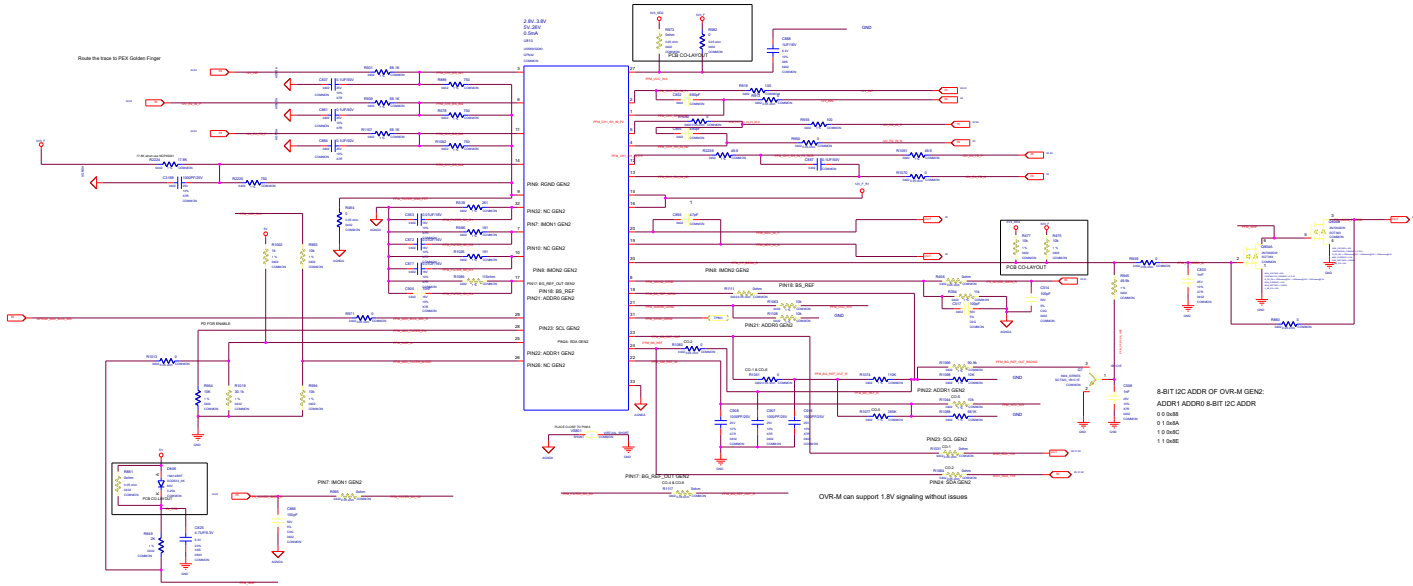


<OrgName>	Title : SPPLLVDD_LDO_LOADSWITCH		
	Engineer: Kenny_Chih		
Size: Custom	Project Name: CG1393PBI2		Rev: 1.00X
Date: Wednesday, December 21, 2022	Sheet 49 of 65		

Page 62: PS: INPUTS, FILTERING, MONITORING



Title : PS: INPUTS
Engineer: Hariston_huang
Project Name: CG1393PBI2
Date: Wednesday, December 21, 2022 Sheet 44 of 61



OVR-M GEN2 SUPPORT

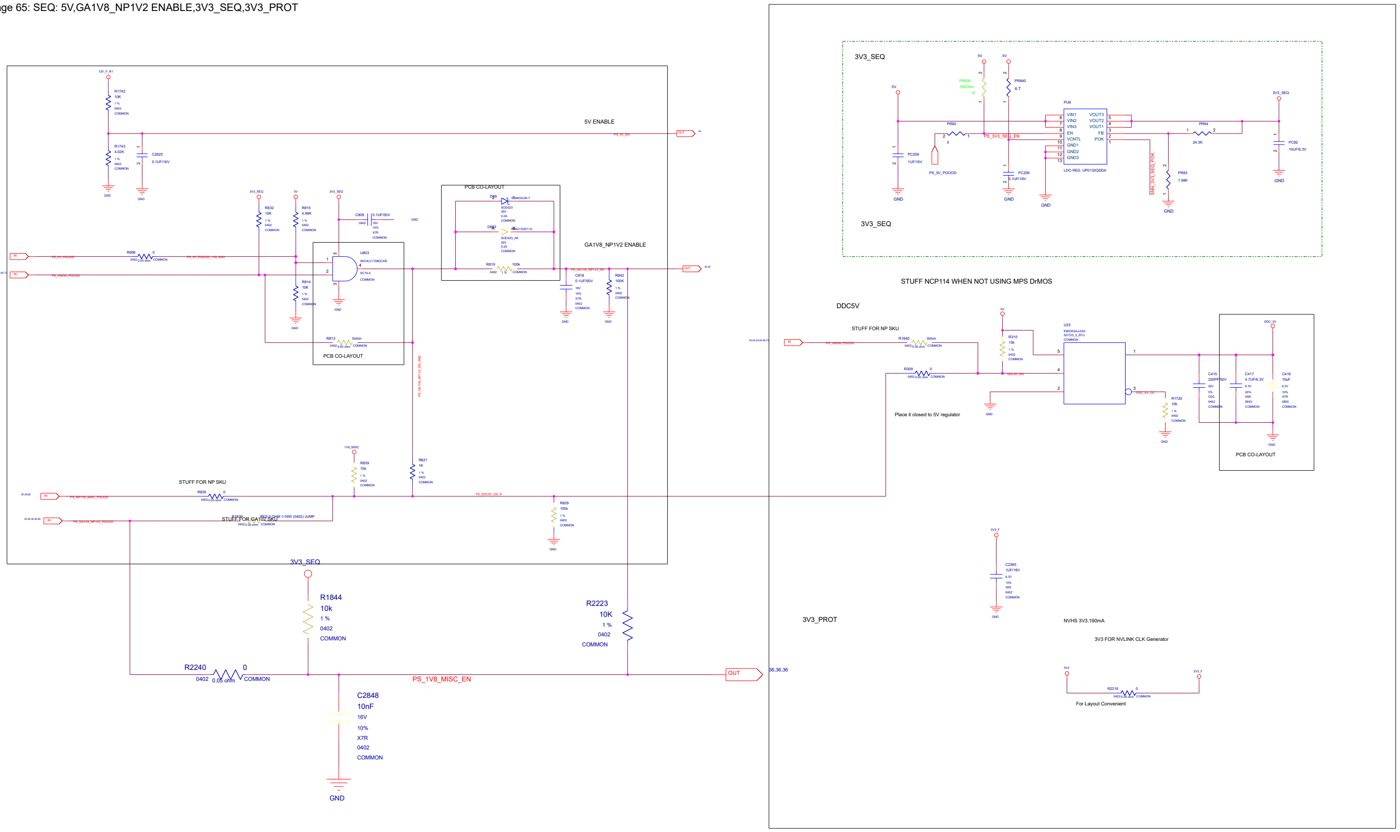
OVR-M GEN2:

PIN 7, 8, 9, 10, 17, 18, 21, 22, 23, 24, 26, 32

are different from GEN1 OVRM,

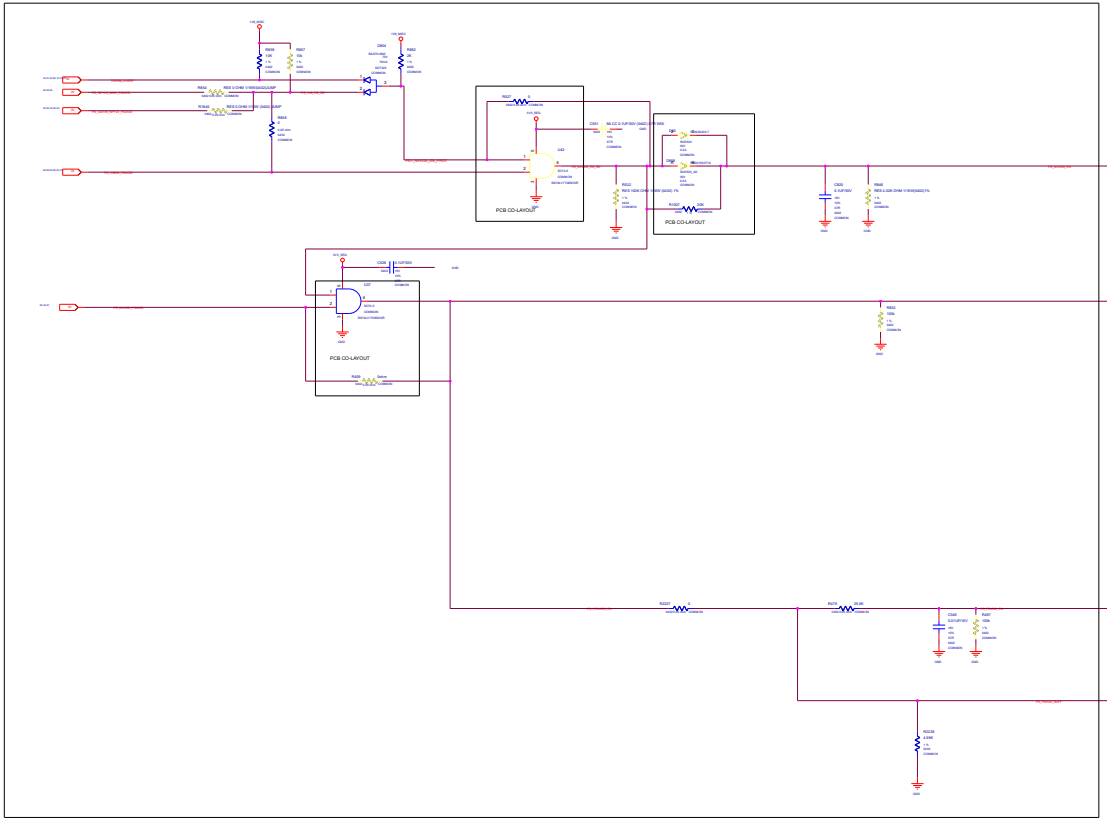
ASUS	Title :	PREFILTER	
<Engineer>	Engineer:	Harlston_huang	
Size: Custom	Project Name: EG1393PBI2		Rev: 1.00A
Date: Wednesday, December 21, 2022	Sheet	63 of 80	

Page 65: SEQ: 5V,GA1V8_NP1V2 ENABLE,3V3_SEQ,3V3_PROT



Title :	SEQ: 5V,GA1V8_NP1V2
Engineer:	Hariston_huang
Size	Custom
Project Name	CG1393PBI2
Rev	1.00X
Date:	Wednesday, December 21, 2022
Sheet	46 of 61

<OrgName>



Title : SEQ: NV,PEX,FB EN

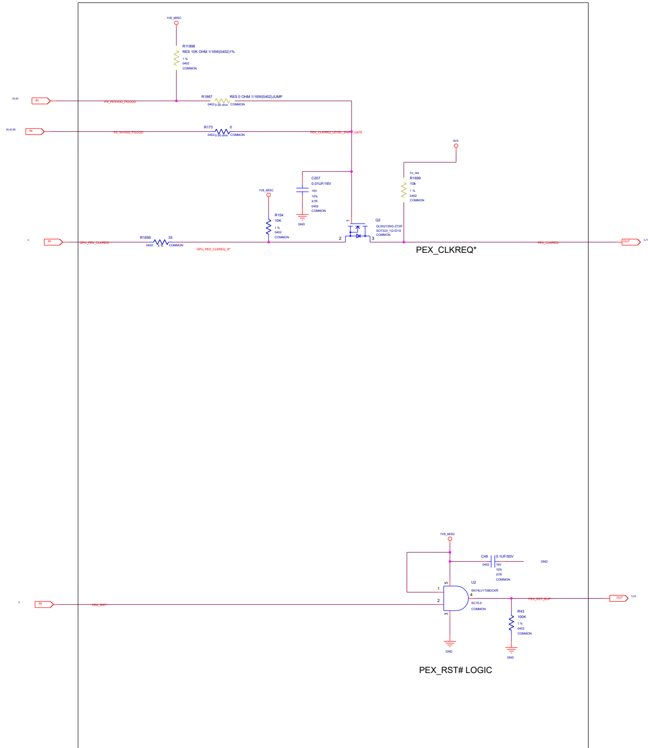
Engineer: Harlston_huang

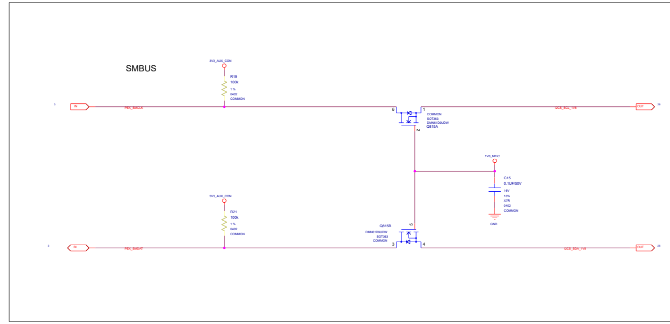
Project Name: CG1393FB12

Rev: 1.00

Date: Wednesday, December 01, 2021

Page 67: SEQUENCE: MISC, PEX3V3 MONITOR

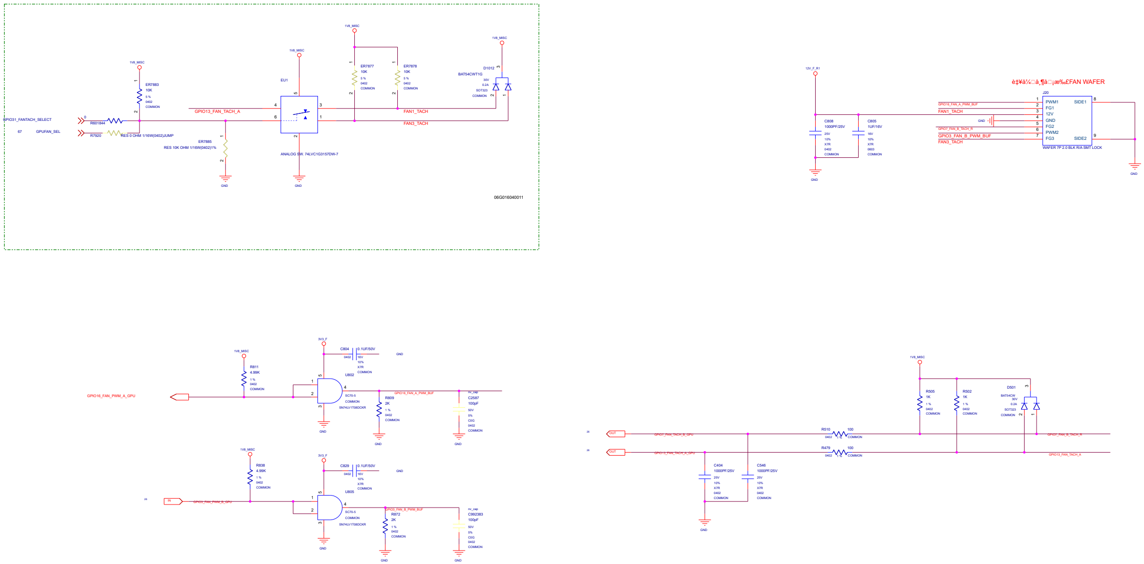




REMOVE PEX3V3 MONITOR

ASUS	Title :	SEQUENCE: MISC	
<OrgName>	Engineer:	Hariston_huang	
Size: Custom	Project Name: CG1393PBI2		Rev: 1.00X
Date: Wednesday, December 21, 2022	Sheet 48 of 61		

Page 68: FAN



Title : FAN

Engineer: Hariston_huang

Size: Custom

Project Name: CG1393PBI2

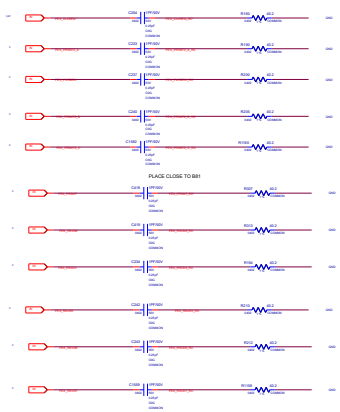
Rev: 1.00X

Date: Wednesday, December 21, 2022

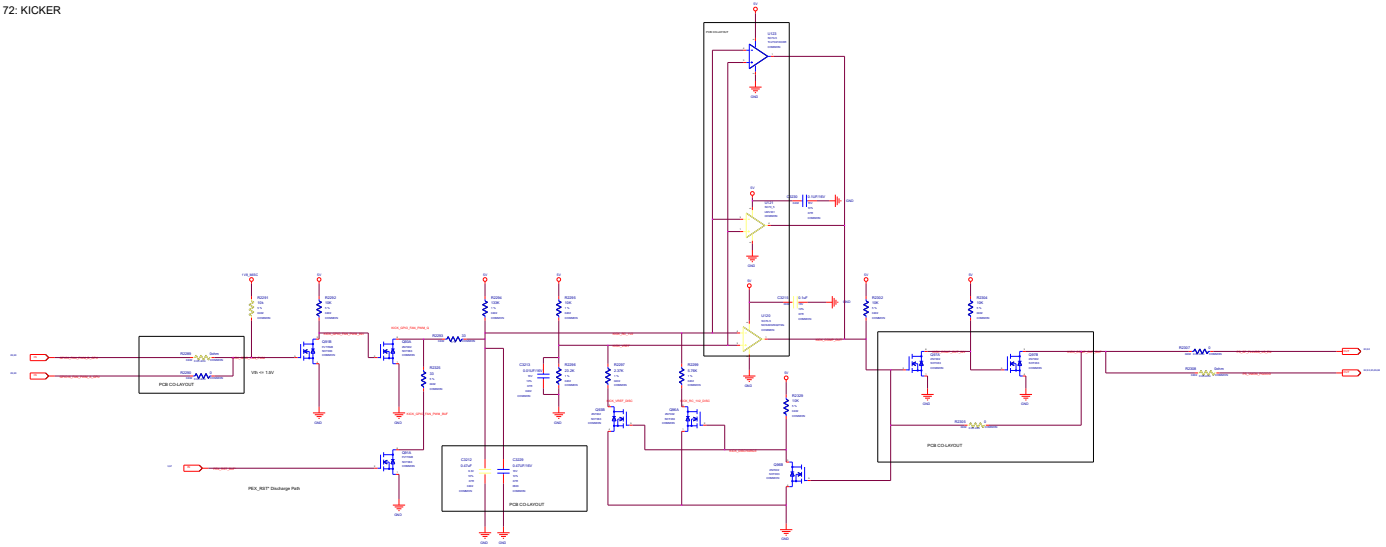
Sheet 49 of 61

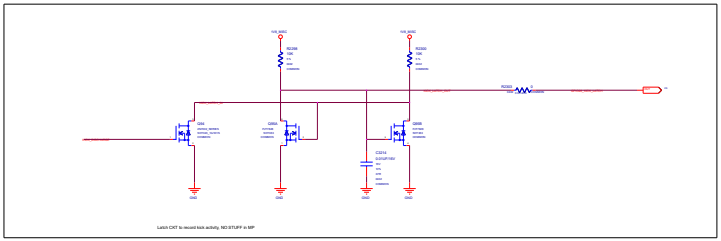
Page 70:VR THERMAL PROTECTION

Title :	VR THERMAL PROTECTION	
Engineer:	Hariston_huang	
Size: Custom	Project Name: EG1393PBI2	Rev: 1.0G
Date: Wednesday, December 21, 2022	Sheet 33 of 51	



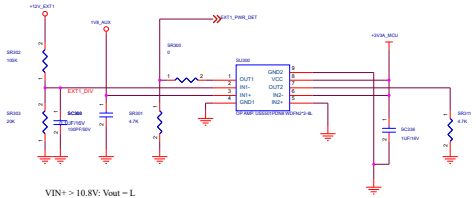
Title :	PCI TERM
Engineer:	Hanston_huang
Size:	Project Name: CG1393PBH2
Rev:	1.002
Date:	Wednesday, December 07, 2022
Sheet:	71 of 71


PCB CO-LAYOUT
PCB CO-LAYOUT
PCB CO-LAYOUT
PBX_RST* Discharge Path


Latch CKT to record kick activity. NO STUFF in MP

PSU DETECT

EXT1



VIN+ > 10.8V: Vout = L

VIN+ < 10.8V: Vout = H

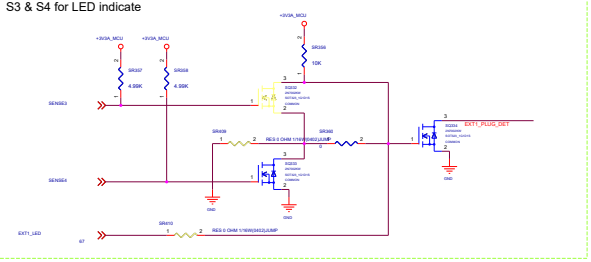
10.8V x 20Kohm / (100Kohm+20Kohm) = 1.8V

300/450/600w Boot Up BOM Stuffing

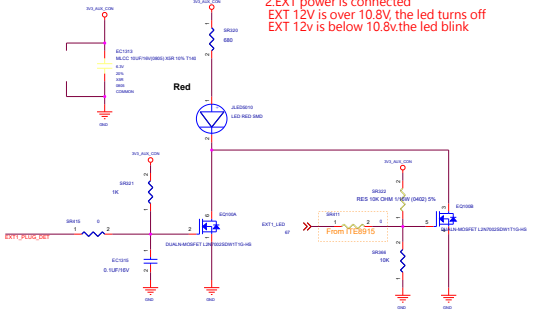
	Sense0	Sense1	GPIO21(0)	GPIO12(1)	PS_VMON_PGOOD
600w	0	0	1	1	1
450w	1	0	0	1	1
300w	0	1	1	0	1
150w	1	1	0	0	0

Green = ON, Red = OFF

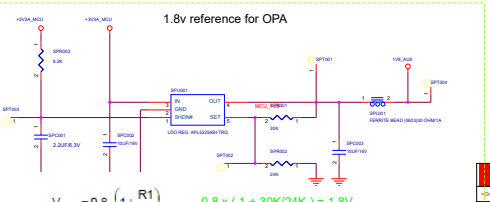
S3 & S4 for LED indicate



1.EXT power is not connected, the led is always on
2.EXT power is connected
EXT 12V is over 10.8V, the led turns off
EXT 12v is below 10.8v.the led blink



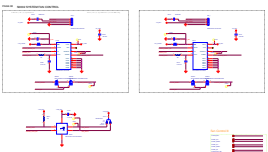
1.8v reference for OPA



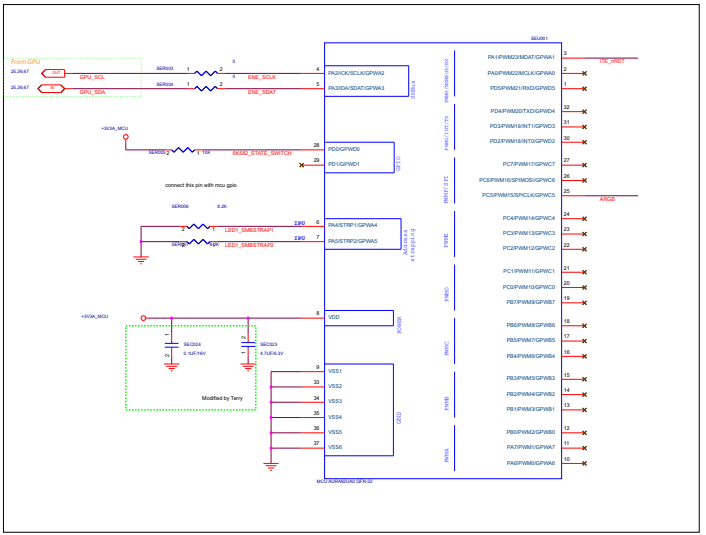
$$V_{OUT} = 0.8 \cdot \left(1 + \frac{R1}{R2}\right)$$

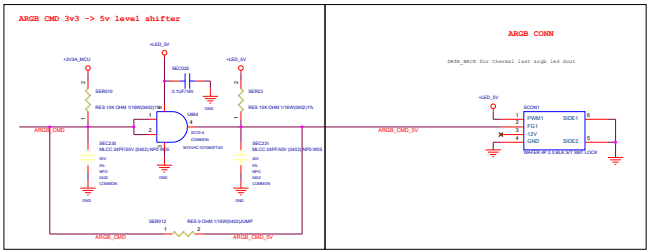
0.8 x (1 + 30K/24K) = 1.8V

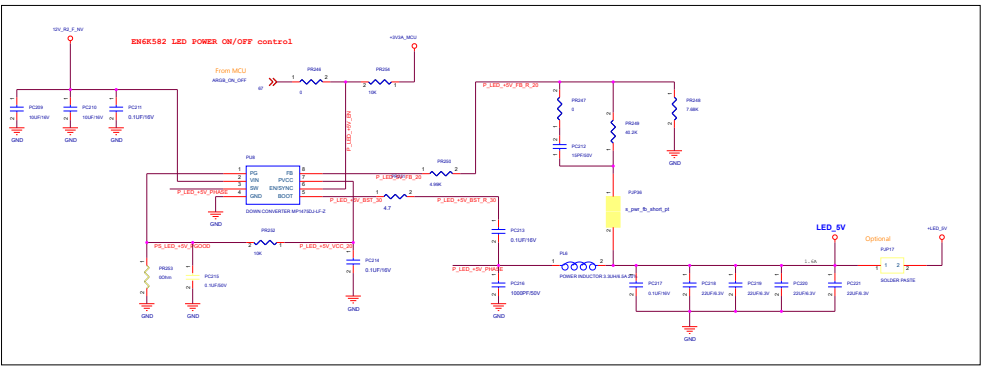
ASUS	Title :	STRIX_PSU DETECT	
<OrgName>	Engineer:	Hariston_huang	
Size: C	Project Name: CG1393PB12		Rev: 1.00A
Date: Wednesday, December 21, 2022	Sheet: 55	of: 61	



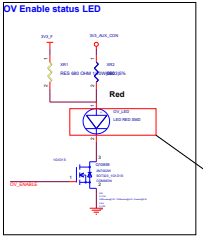
EN6K582

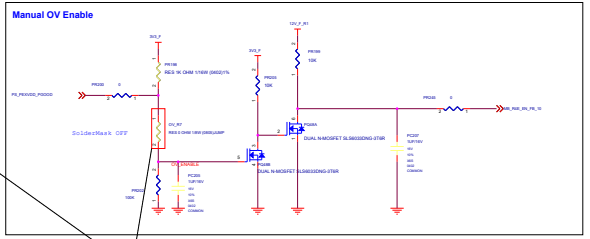




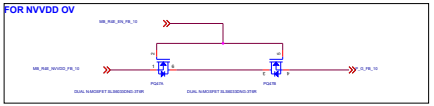


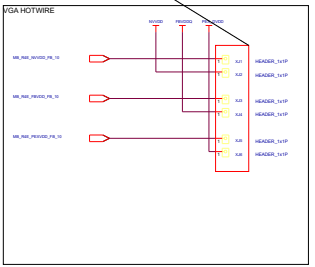
ASUS	Title :	STRIX_AURA82UA0	
<Doc Number>	Engineer:	Hariston_huang	
Size: C	Project Name: CG1393PB12		Rev: 1.00X
Date: Wednesday, December 21, 2022	Sheet 57 of 61		

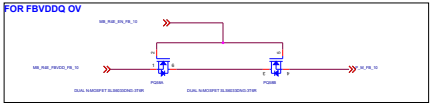


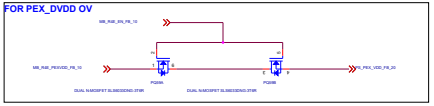


PLACE TOGETHER









Title :	STRIX_HOTwire R4E		
Engineer:	Harriston_huang		
Size: A2	Project Name: CG1393PBI2		Rev: 1.00X
Date: Wednesday, December 01, 2021	Sheet: 58 of 83		

ASUS VGA Screws and PCB Holes

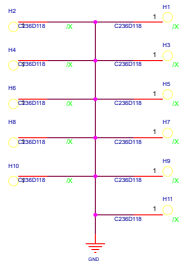
X-clip Holes for GPU Thermal Module

Drill: 3.8mm
Top Circle: 6mm
Bottom Circle: 10mm

Note: If you need to use Spring screws for Thermal Module, DON'T use these parts!
Please discuss this with your ME RD.

Screws for Back Plate
Screw P/N: 13050-72805045

Drill: 3mm
Top Circle: 6mm
Bottom Circle: 6mm



Note: Please change the hole quantity according to actual requiement.

ASUSTEK COMPUTER INC	Title : Screws & Holes	
	Engineer: Alex Luo	
Size	Project Name: ASUS VGA Logo and Holes	Rev: 1.00
Date: Wednesday, December 21, 2022	Sheet 59 of 61	

ASUS VGA PCB Logo

LOGO1 CE /X

LOGO8 UKRAINE /X

LOGO2 VCCI /X

LOGO9 PCB_MADE_IN_CHINA /X

PCB MADE IN CHINA

LOGO3 EMI_D33005_H /X

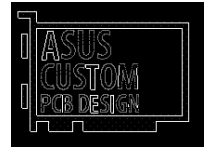
LOGO10 SMARK_L S_MARK_L /X

LOGO4 FCC /X

LOGO11 WEEE_LOGO WEEE_LOGO /X

ASUS Re-design logo
Do not place this on reference board

LOGO13 ASUS_CUSTOM_PCB /X



LOGO5 RCM /X

LOGO6 CAN_ICES-003(B)/NMB-003(B) /X

CAN ICES-003(B)/NMB-003(B)

LOGO12 SFIS /X

LOGO14 SFIS /X

SFIS

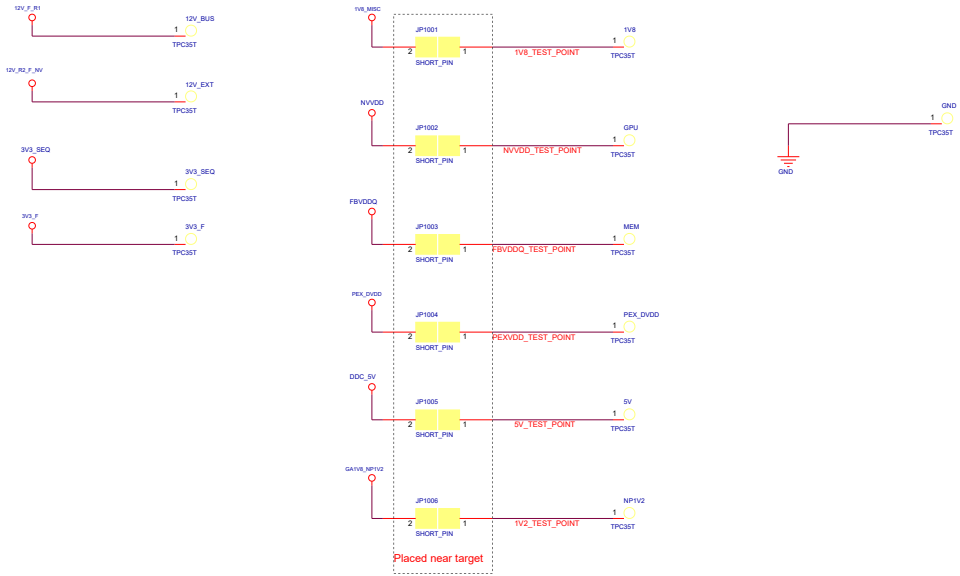
place two SFIS outlines on each side of PCB

LOGO7 KC_R_R_LOGO /X

LOGO15 UCKA_LOGO

ASUSTEK COMPUTER INC	Title :	PCB Logo	
	Engineer:	Alex Luo	
Size	Project Name	ASUS VGA Logo and Holes	Rev 1.00
Date: Wednesday, December 21, 2022	Sheet 60 of 61		

NOTE: connect power symbols to your actual design!



ASUSTEK COMPUTER INC	Title :	Power Test Point	
	Engineer:	Alex	
Size	Project Name	Power Test Point	Rev 1.00
Date: Wednesday, December 21, 2022	Sheet 61 of 61		