

PG301 A02

Comanche 192b GDDR5, <150W, 2-way SLI
Tall DVI-I + DP + DP + DP/HDMI + DP

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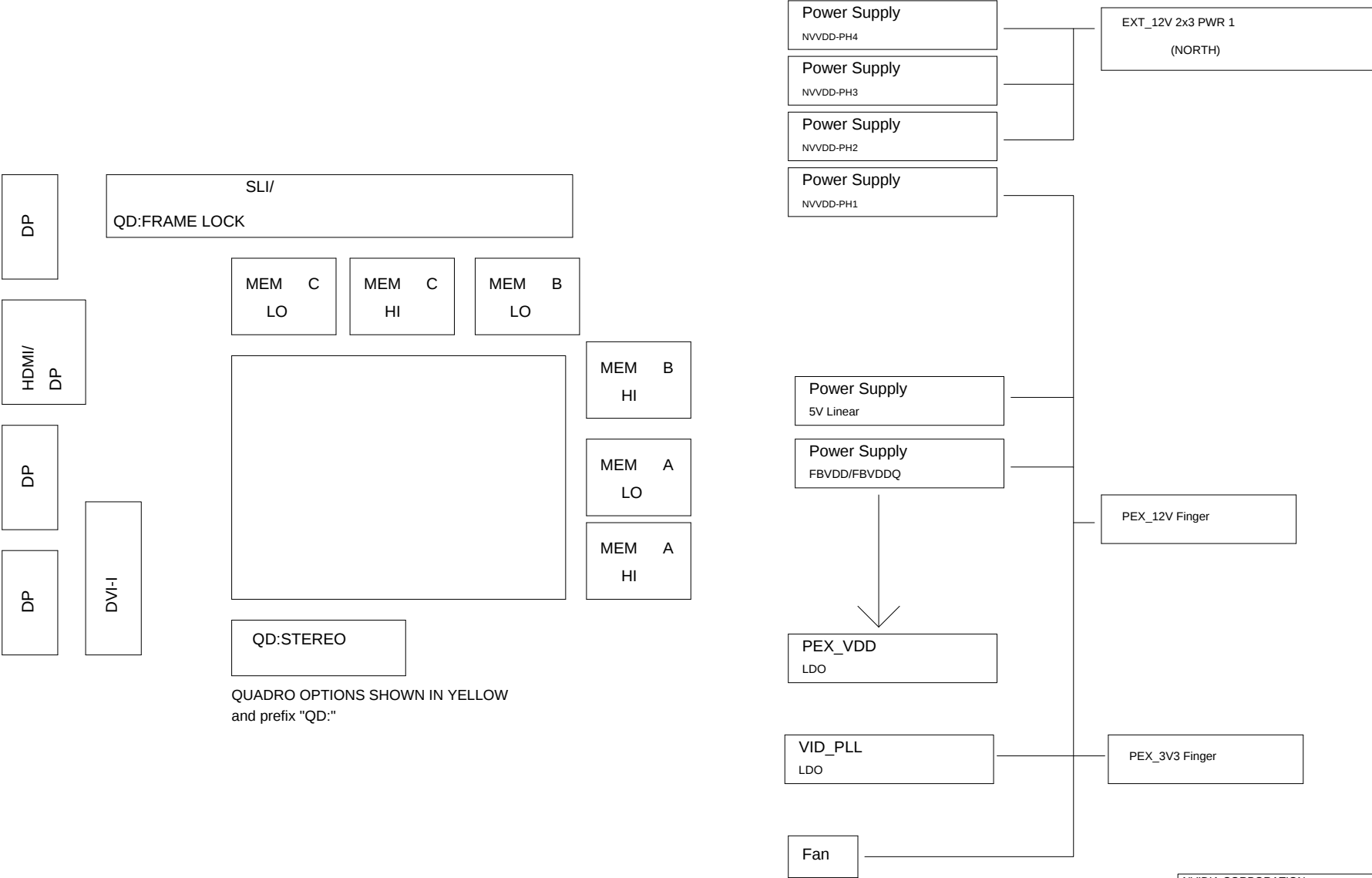
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Block Diagram



QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"

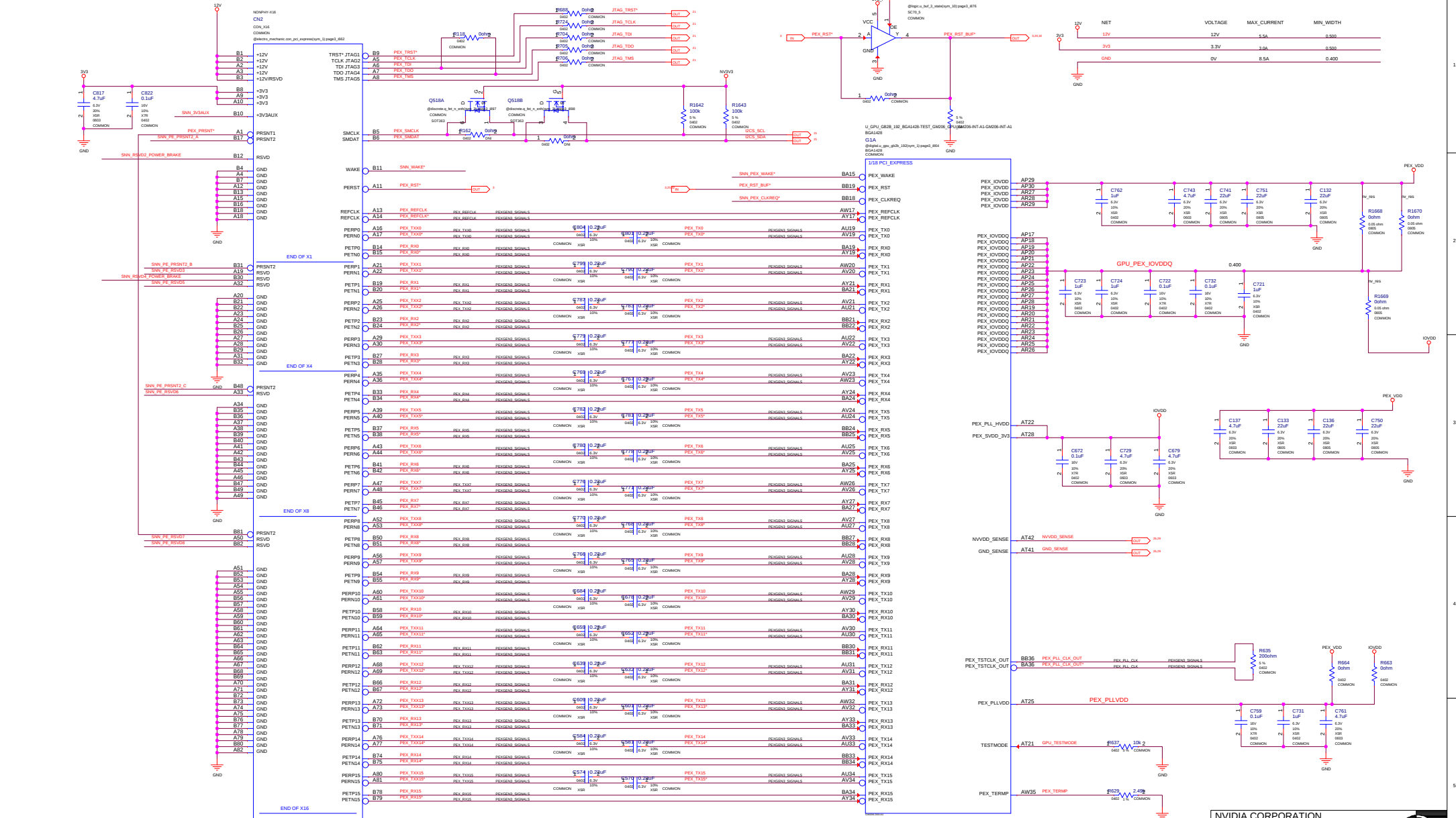
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PCI Express



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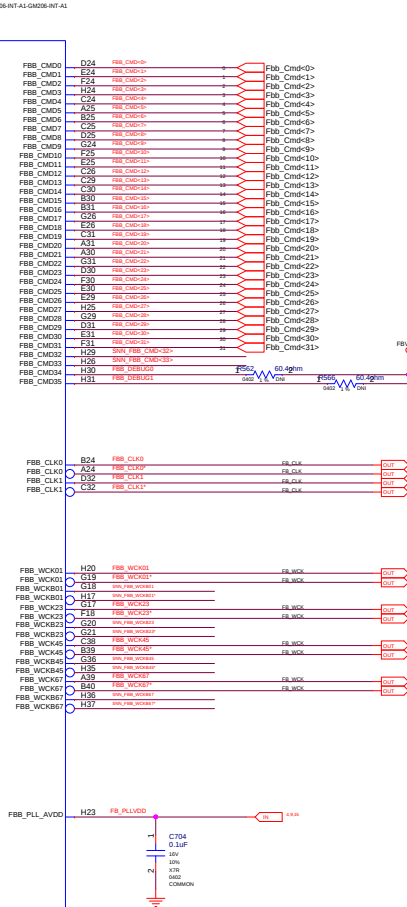
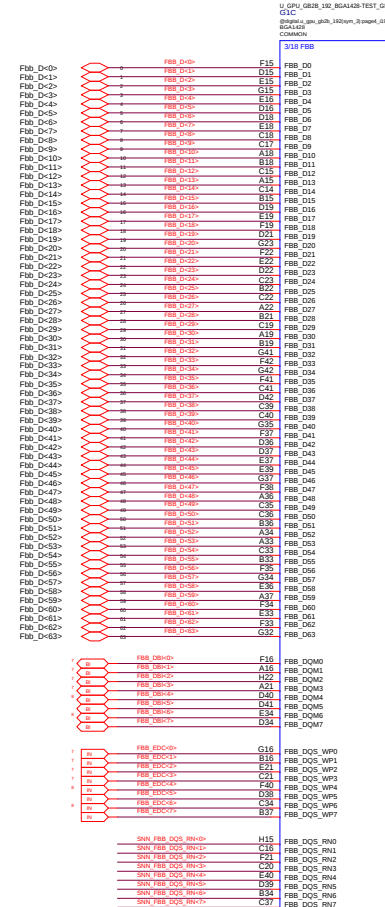
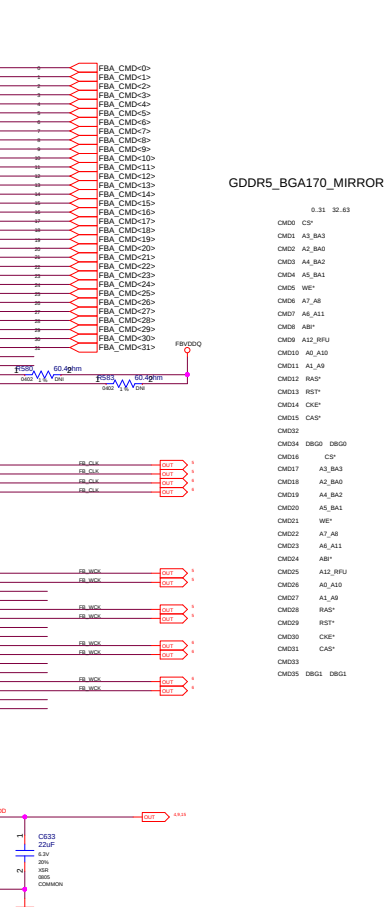
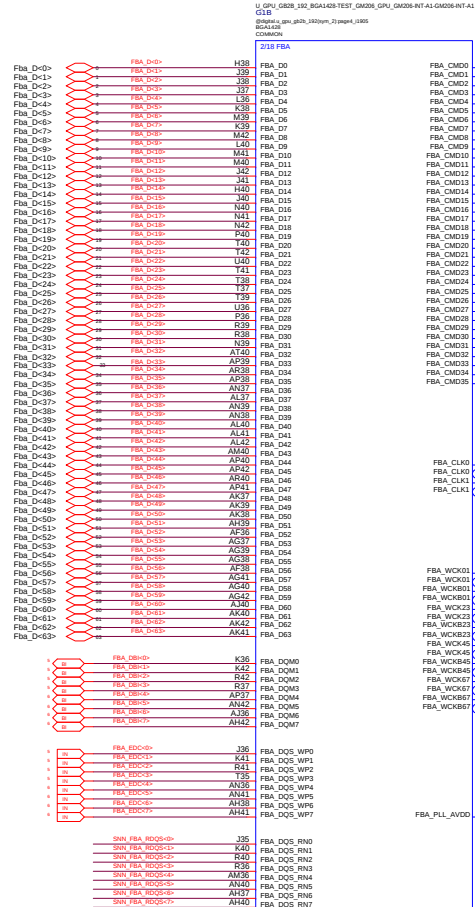
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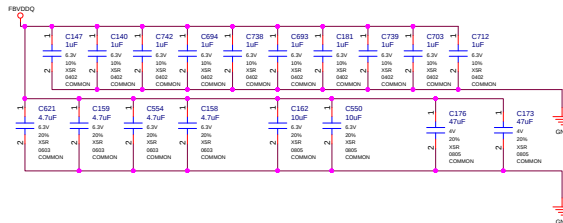
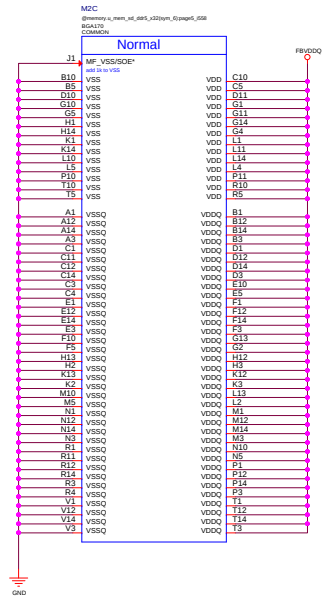
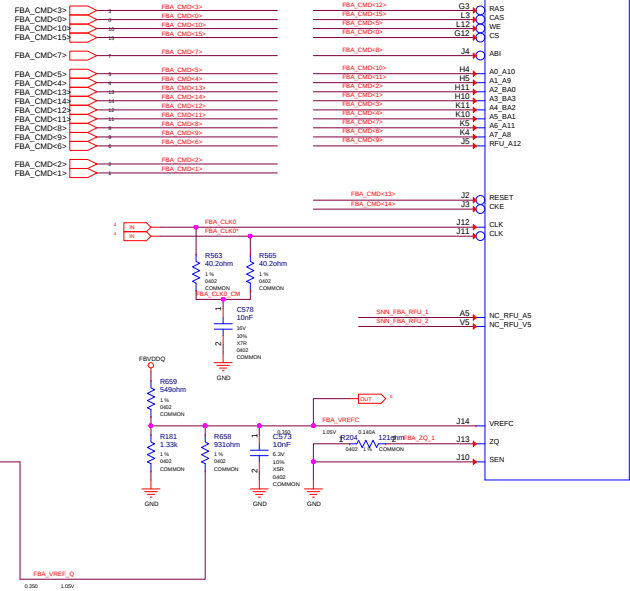
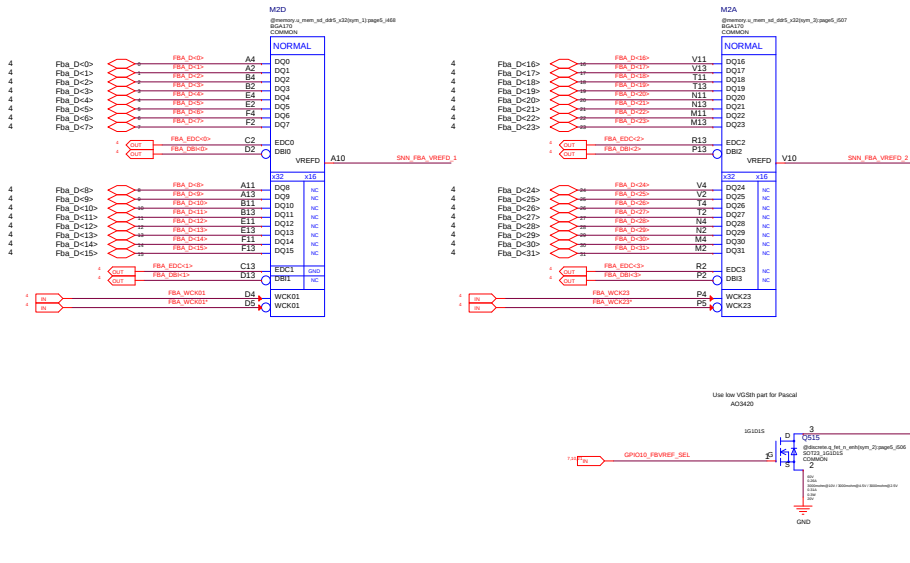
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MEMORY: GPU Partition A/B



MEMORY: FBA Partition 31..0

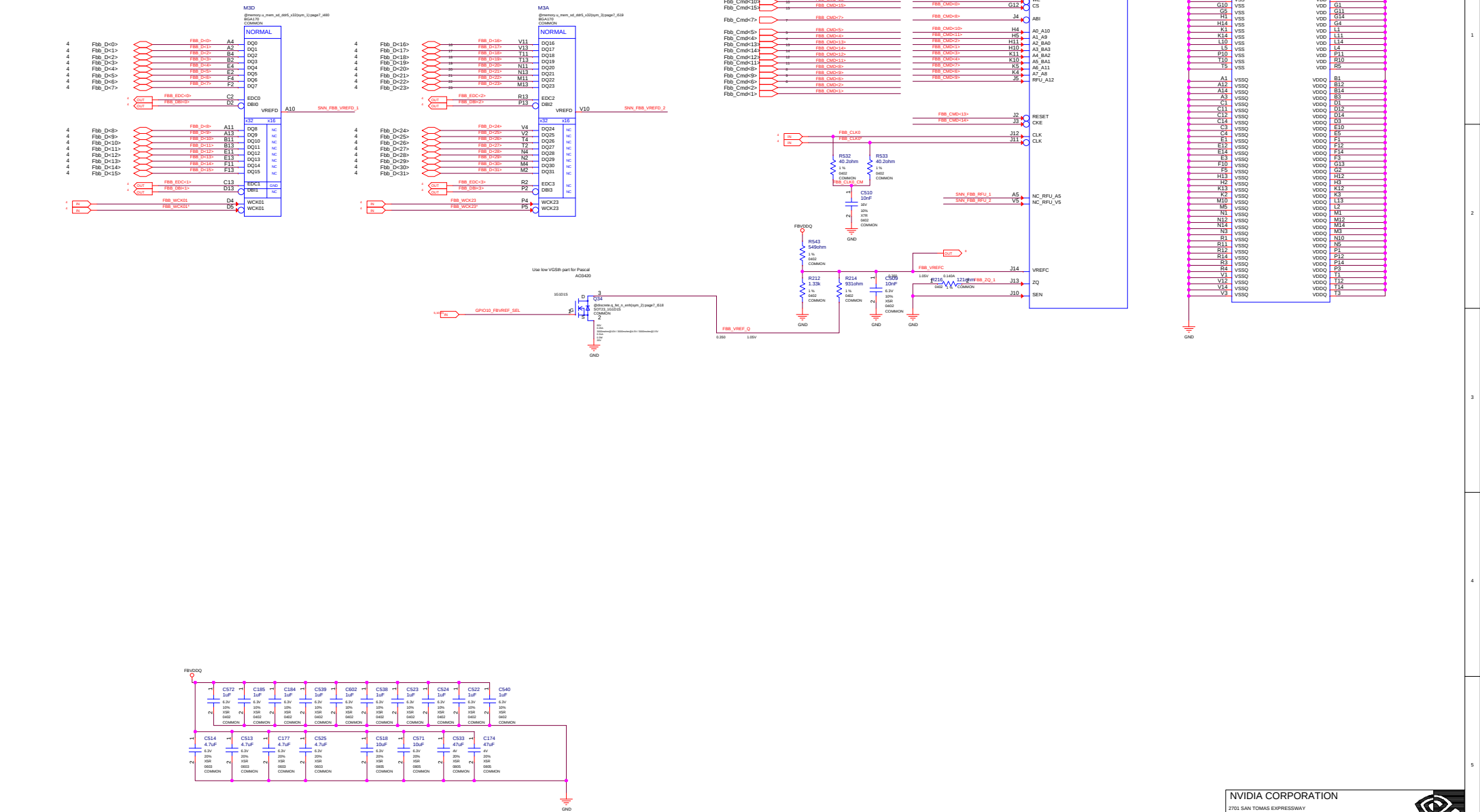


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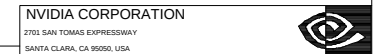
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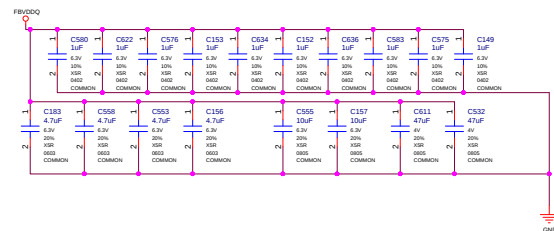
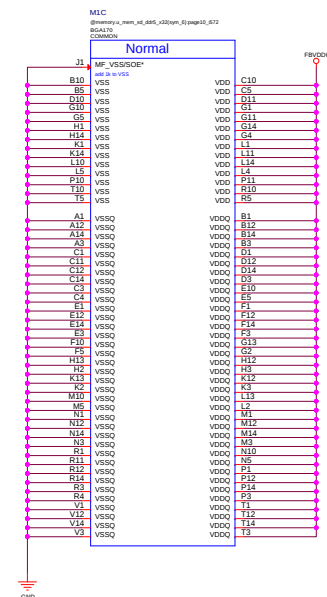
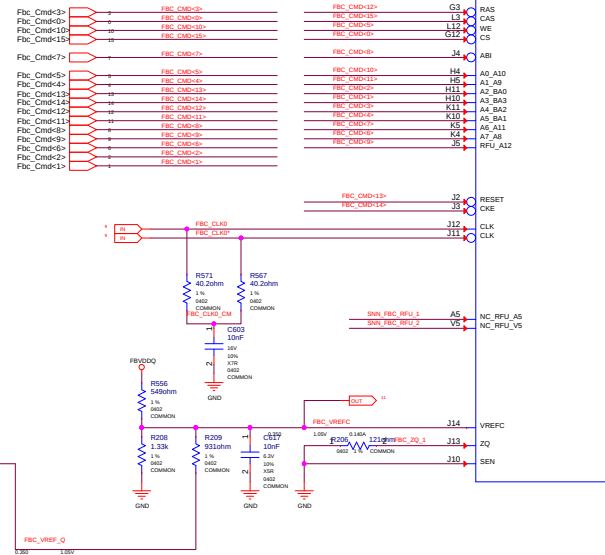
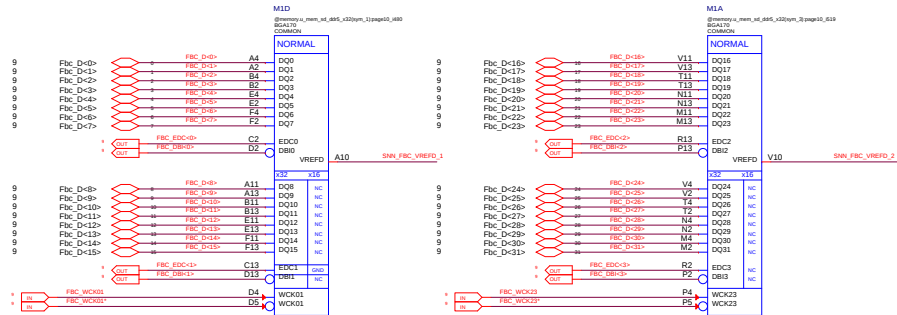
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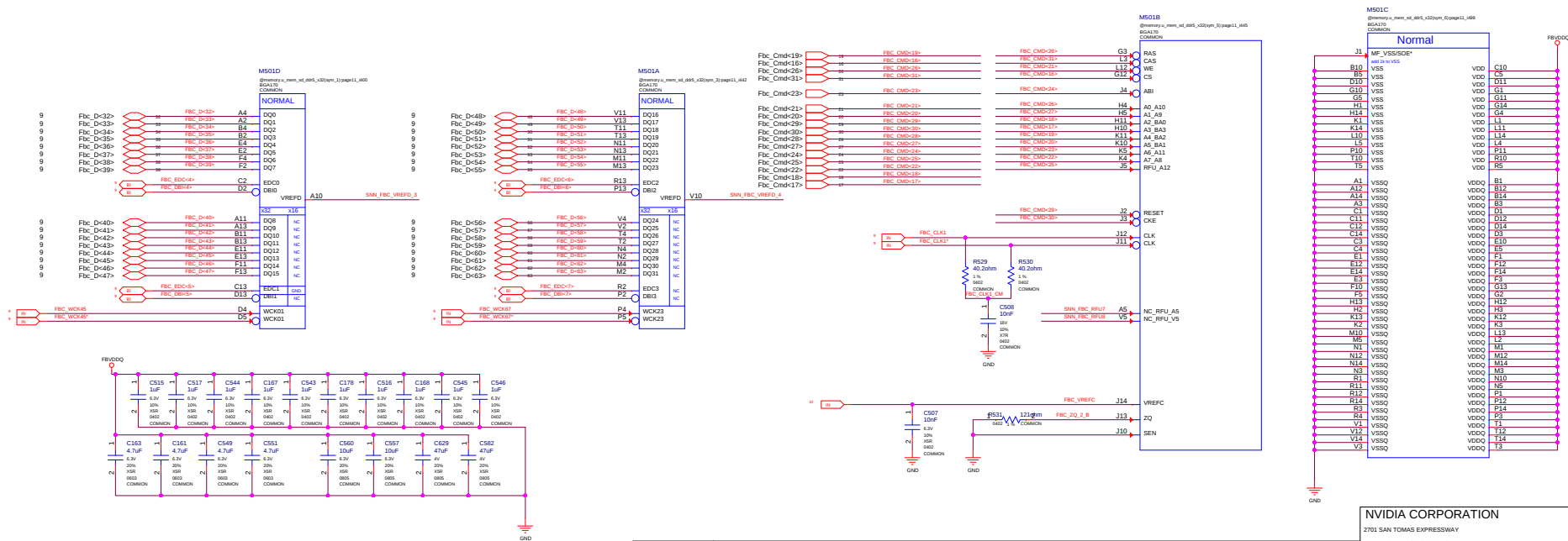
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GPU PWR and GND

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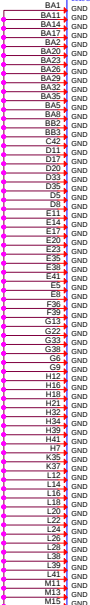
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BGA428

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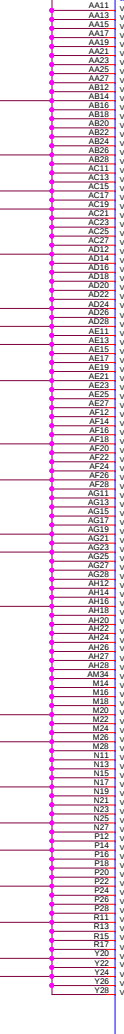
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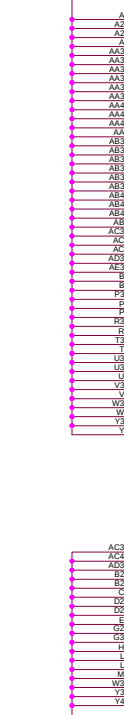
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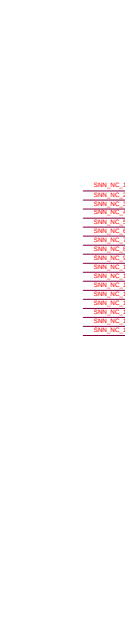
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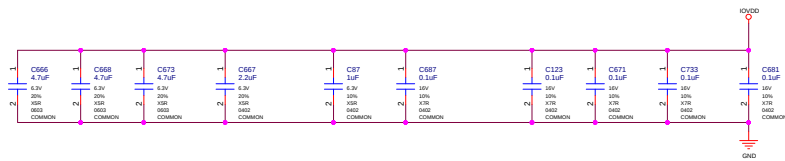
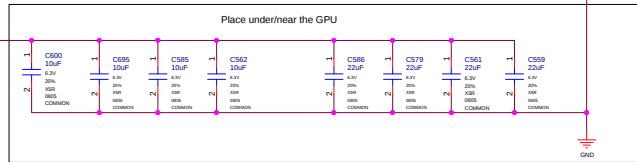
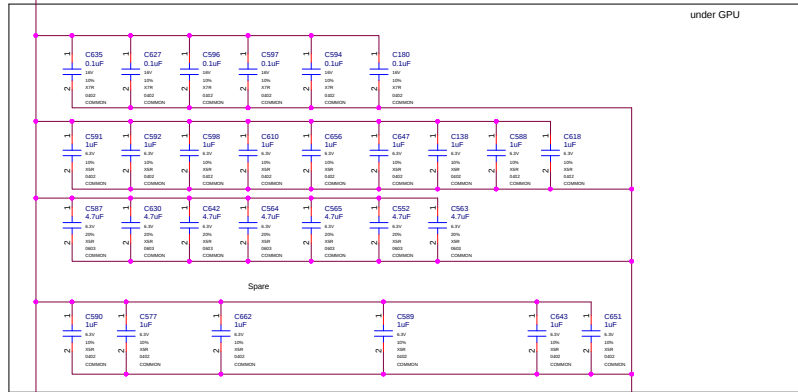
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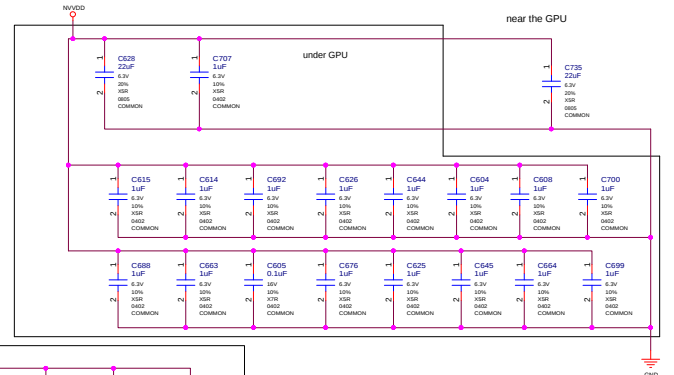
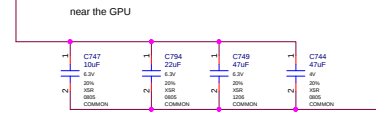
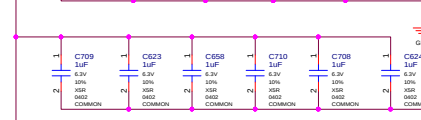
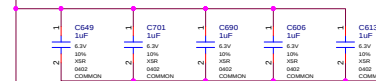
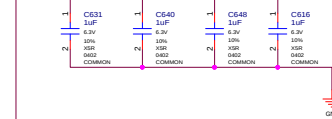
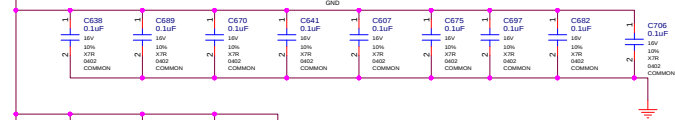
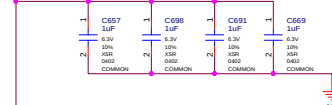
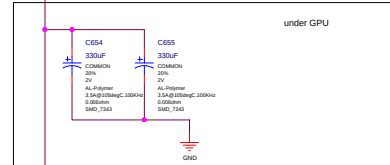
PAGE DETAIL GPU PWR and GND

GPU Decoupling

FBVDDQ



NVVD



NVVD	Under GPU	Near GPU
SVVD	90uF + 1x 330uF	88uF
Combined (Maxwell)	32uF	22uF
	122uF + 1x 330uF	110uF

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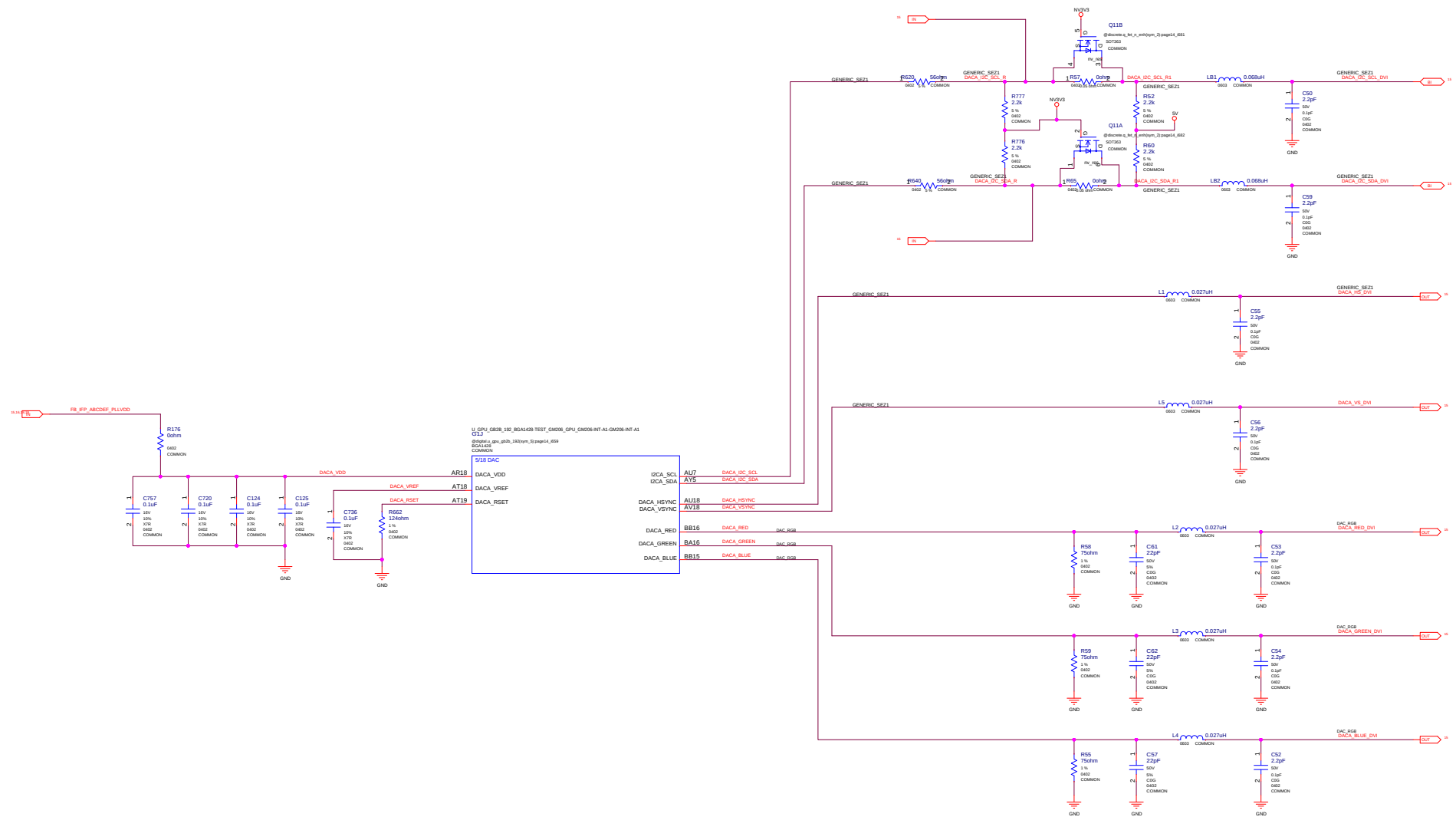
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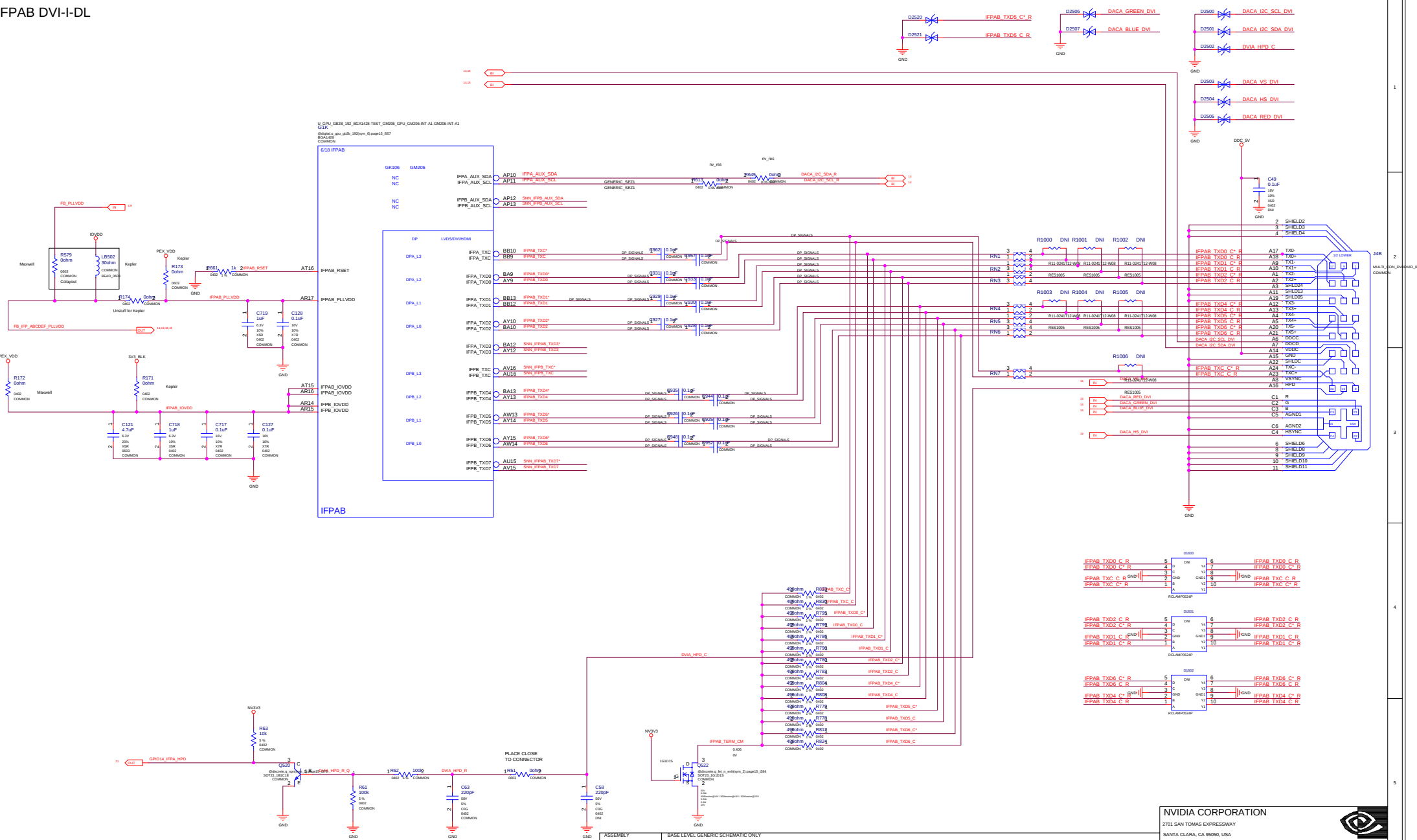
DACA Interface



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IFPAB DVI-I-DL



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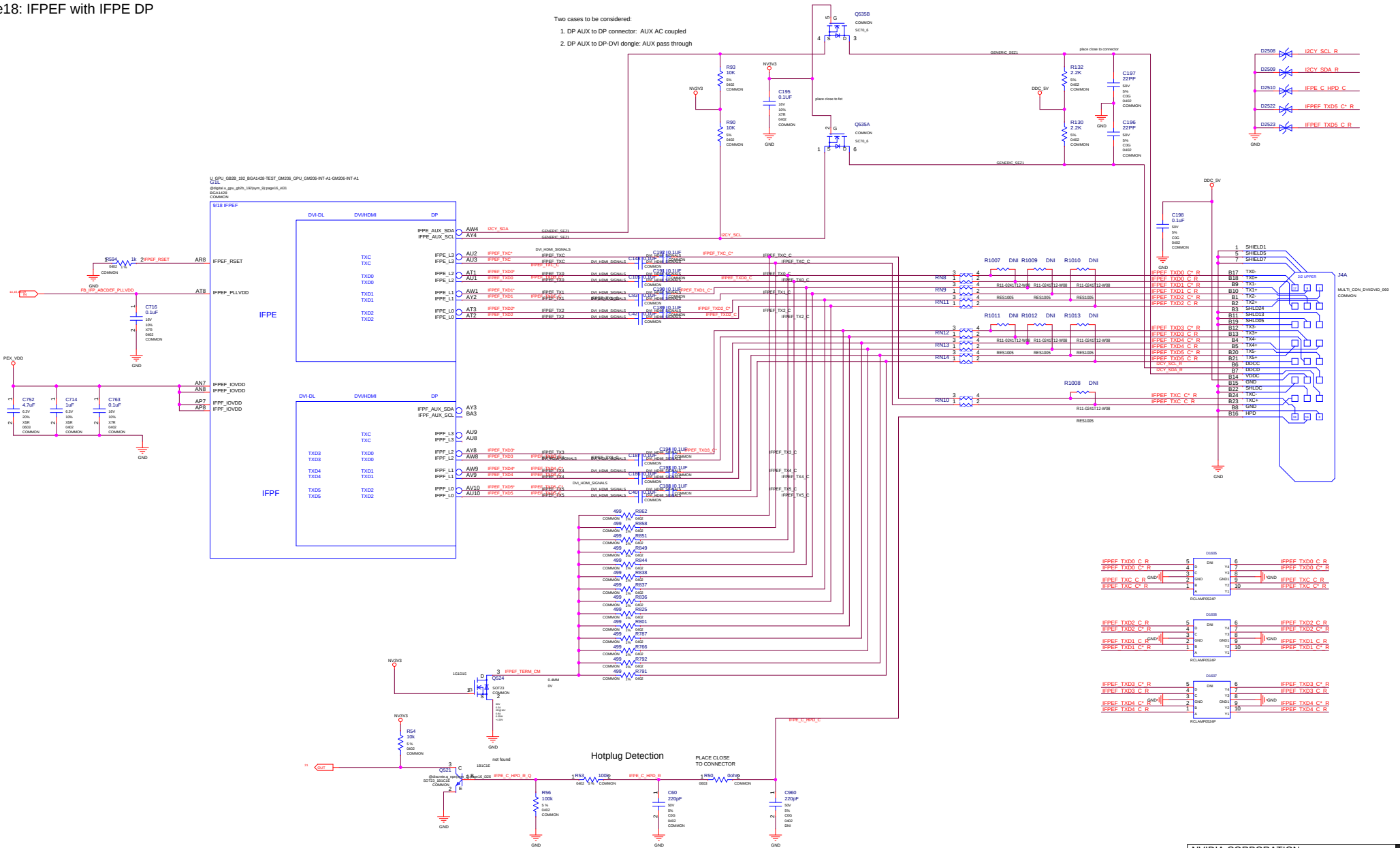
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Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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IFPF DP

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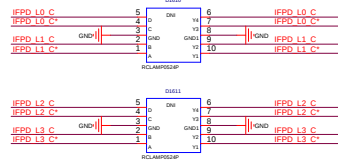
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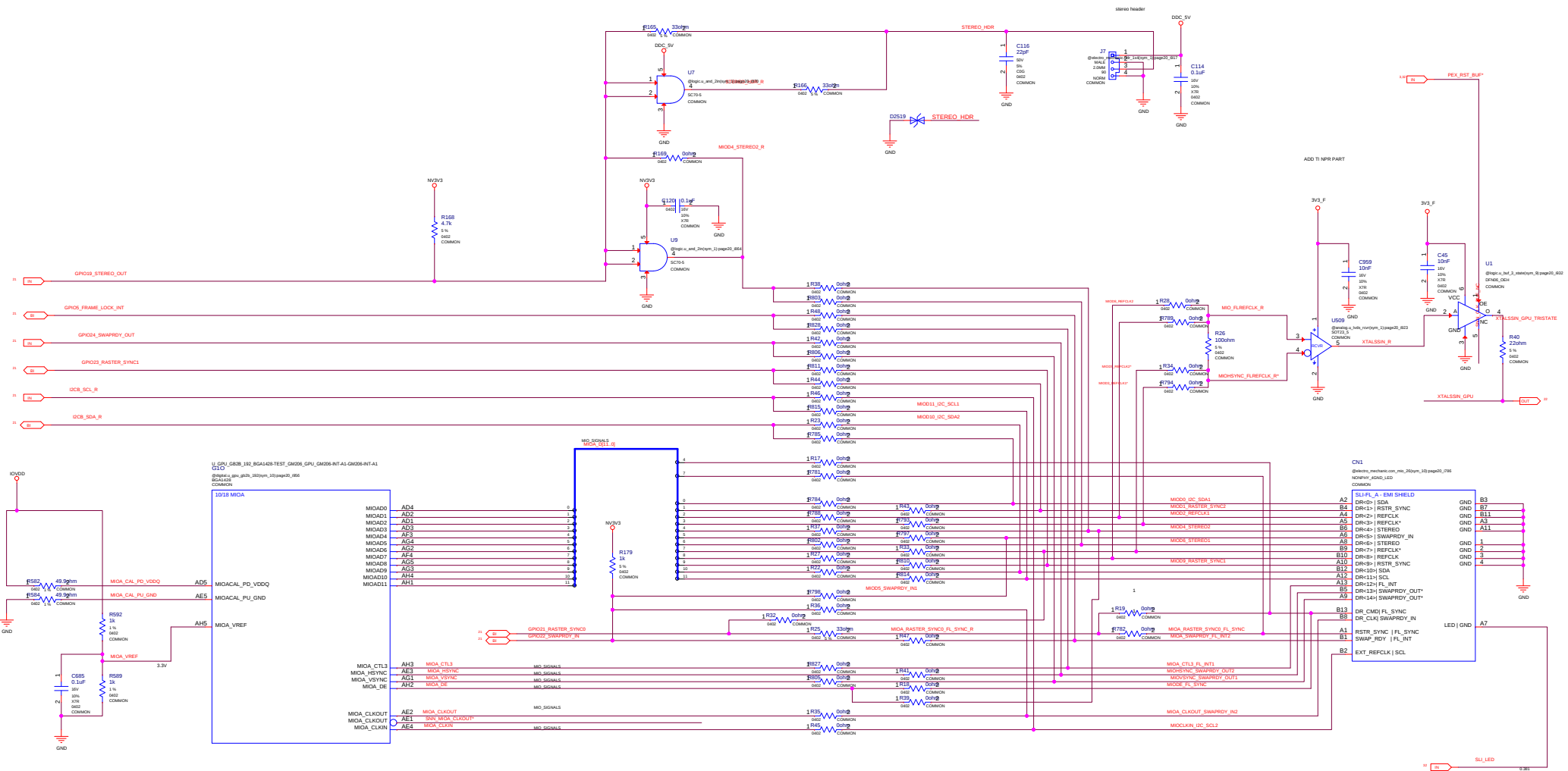


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MIOA/SLI Interface



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
SV	MIOA_VREF	3.3V	0.305
SV	MIOA_CAL_PD_VDDQ	2.5V	0.305
SV	MIOA_CAL_PD_GND	0.0V	0.305

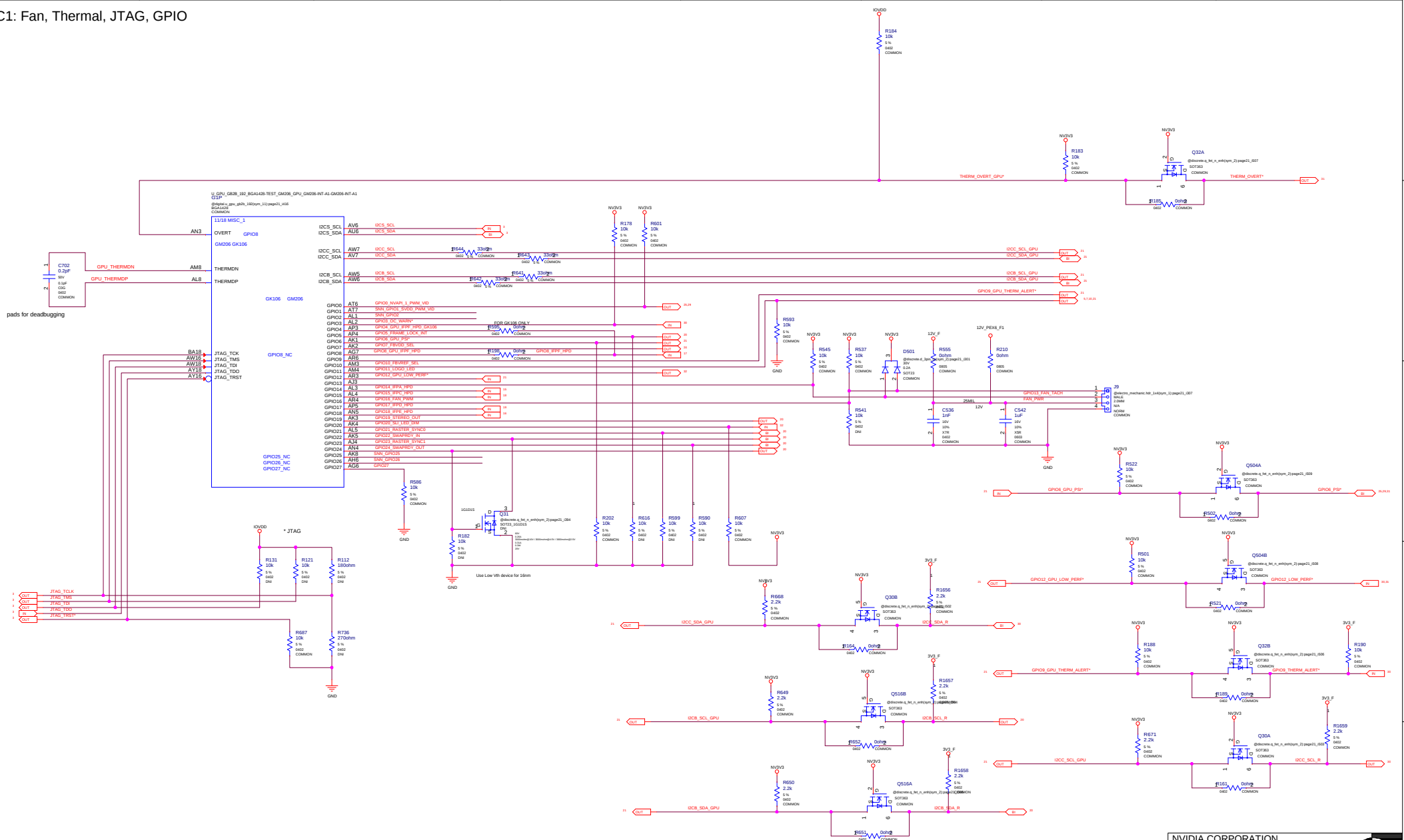
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MIOA

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MISC1: Fan, Thermal, JTAG, GPIO



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GPIO

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KEPLER

MAXWELL

MULTI_STRAP_REPO_GND	
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 0% TO GND

STRAP0		
3.3V	1.65V	0V
GC8+ ISLAND ENABLED	GC8+ DEBUG MODE	GC8+ ISLAND DISABLED

STRAP0

STRAP1

STRAP2

STRAP3

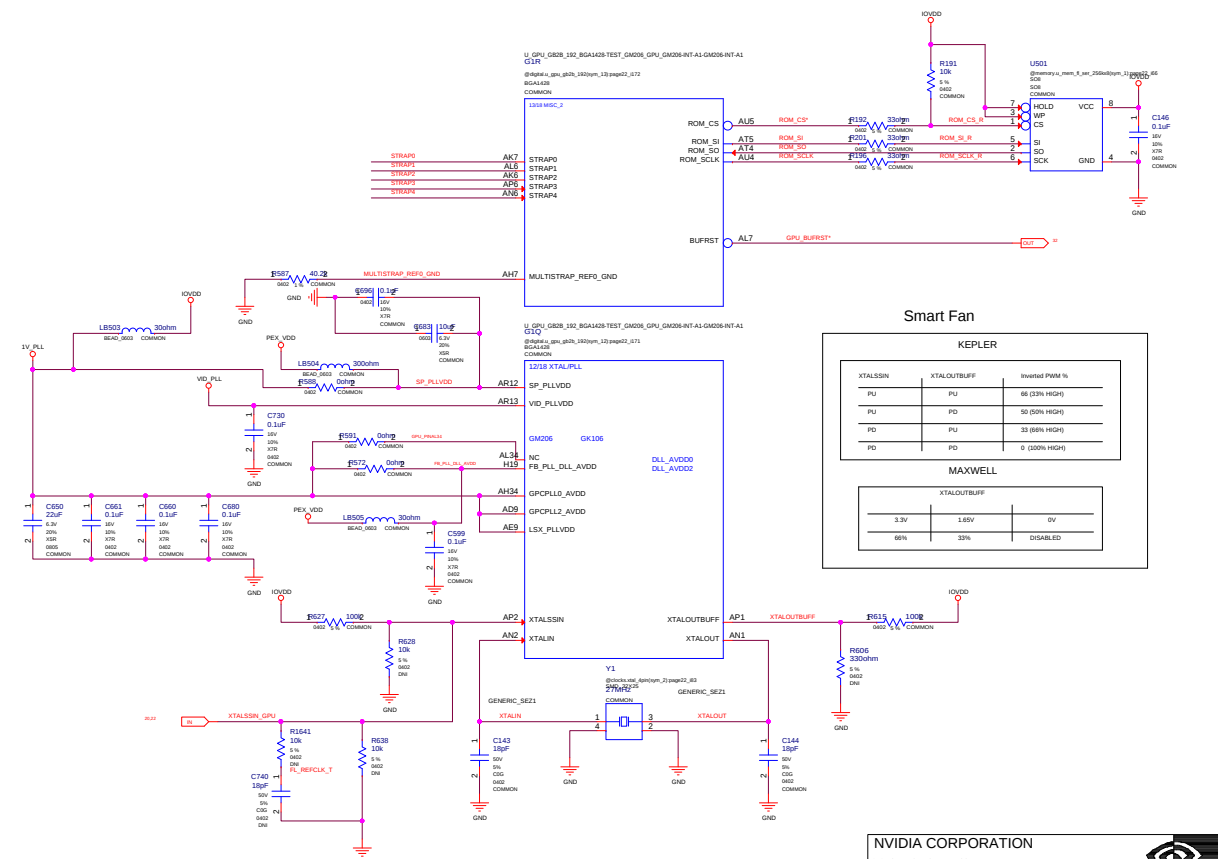
STRAP4

IOVDD

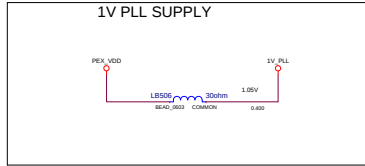
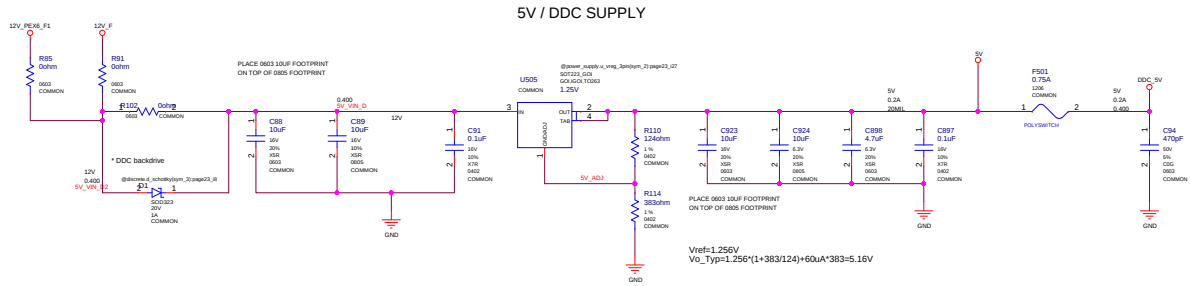
GND

ROM_SI		
SAMSUNG	HYNIX	ELPIDA
45.3k	PD	30.1k PD

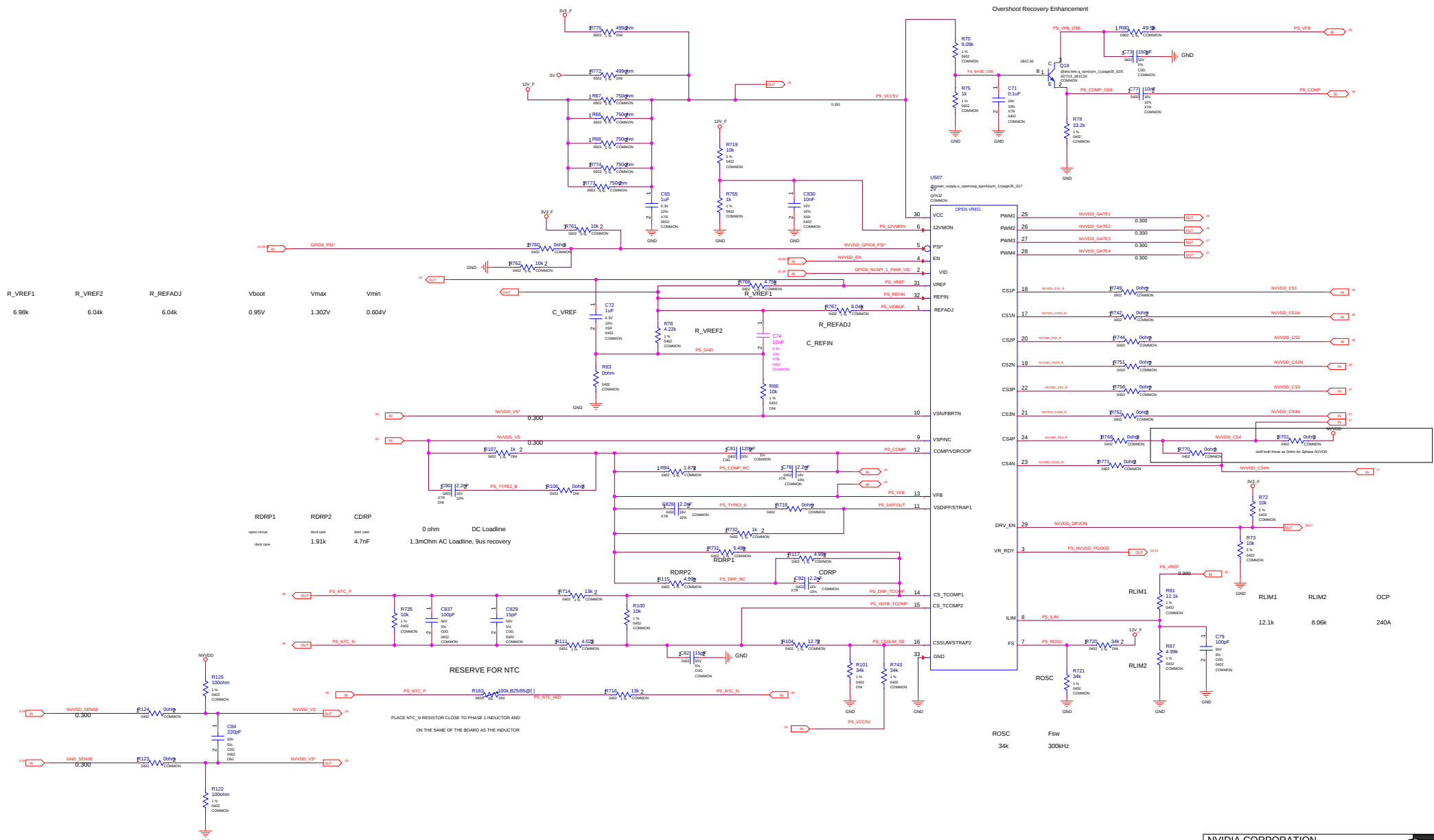
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY	SANTA CLARA, CA 95050, USA
PAGE DETAIL	MISC2 ROM_XTAL Straps	NV_PN 600-1G301-BASE-200
LD MAY		PCB REV P0301.A02
ELY DISCUMS ALL		PAGE 22 OF 24
TRY STANDARDS.		DATE 09-OCT-2014
		BOU REV A



PS: 5V, PEX_VDD



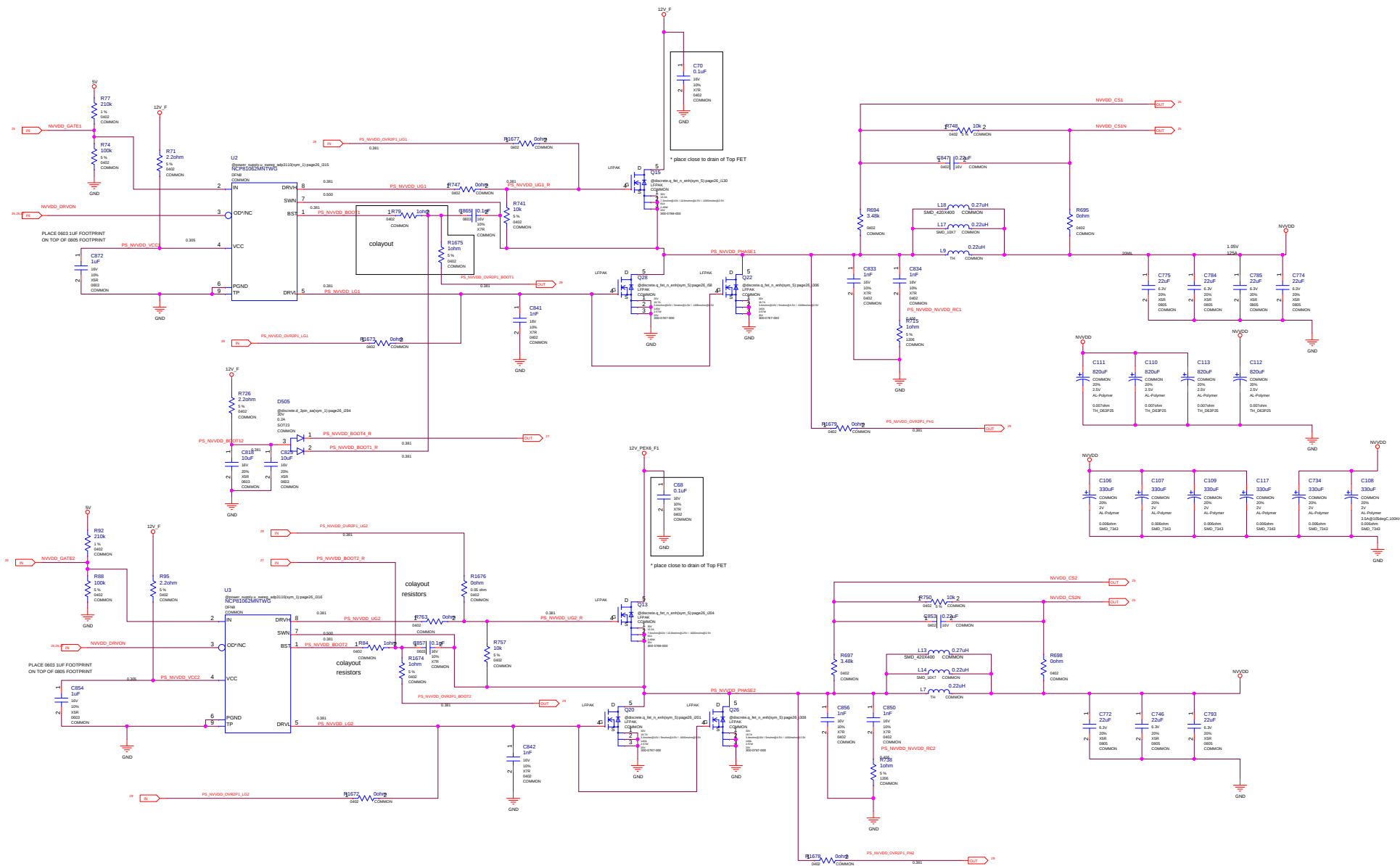
PS: NVVDD Controller



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY		SANTA CLARA, CA 95050, USA	
PAGE DETAIL	PS: NVVDD Controller OVRA option		NV_PN	600-1G301-BASE-200
SALES MAY LESSLY DISCLAIMS ALL INDUSTRY STANDARDS.			PCB REV BOM REV	HGS01-ADZ A
			PAGE	25 OF 34
			DATE	09-OCT-2024

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PS: NVVDD Phase 1,2



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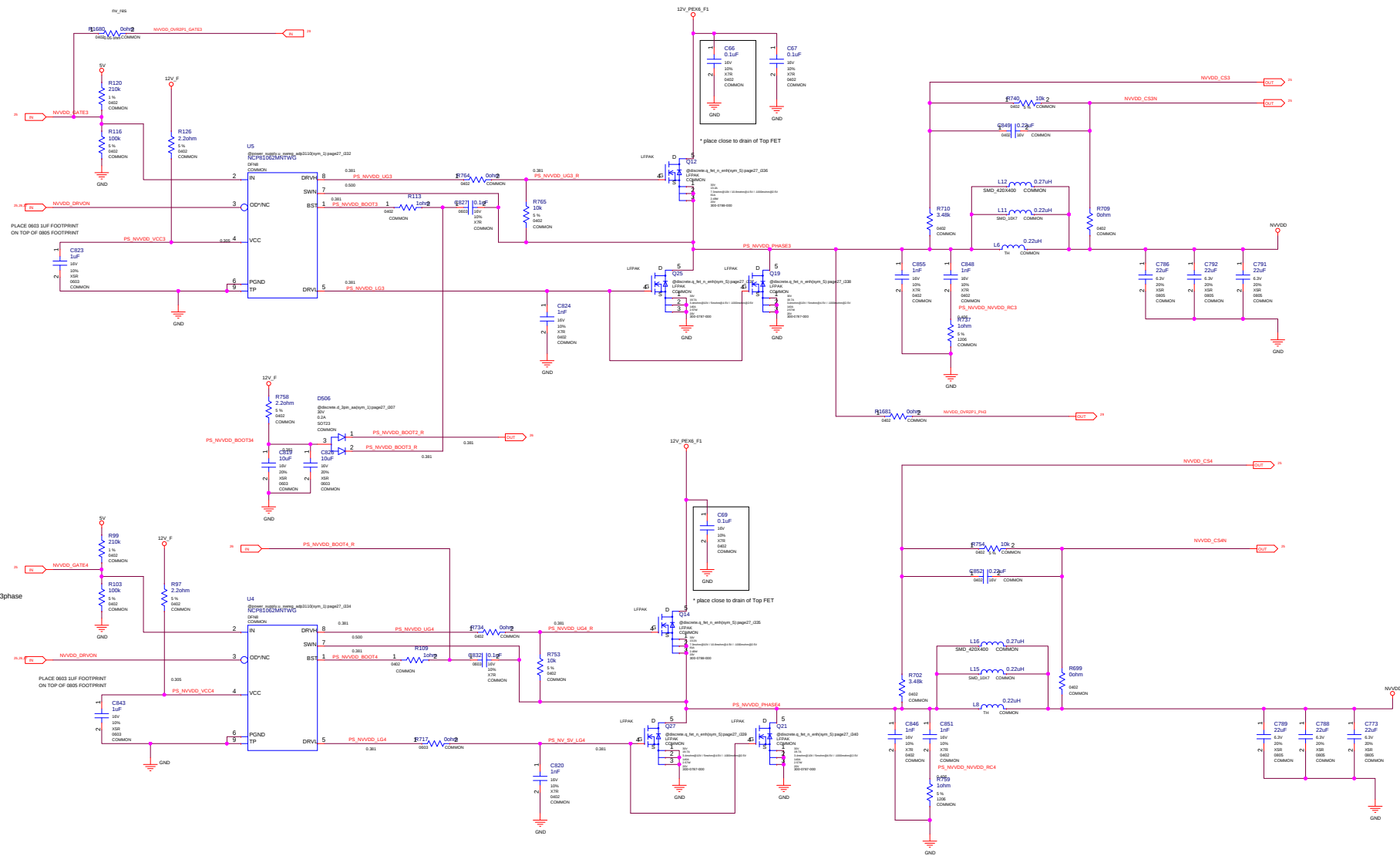
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PS: NVVDD Phase 3,4



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Phase 3,4

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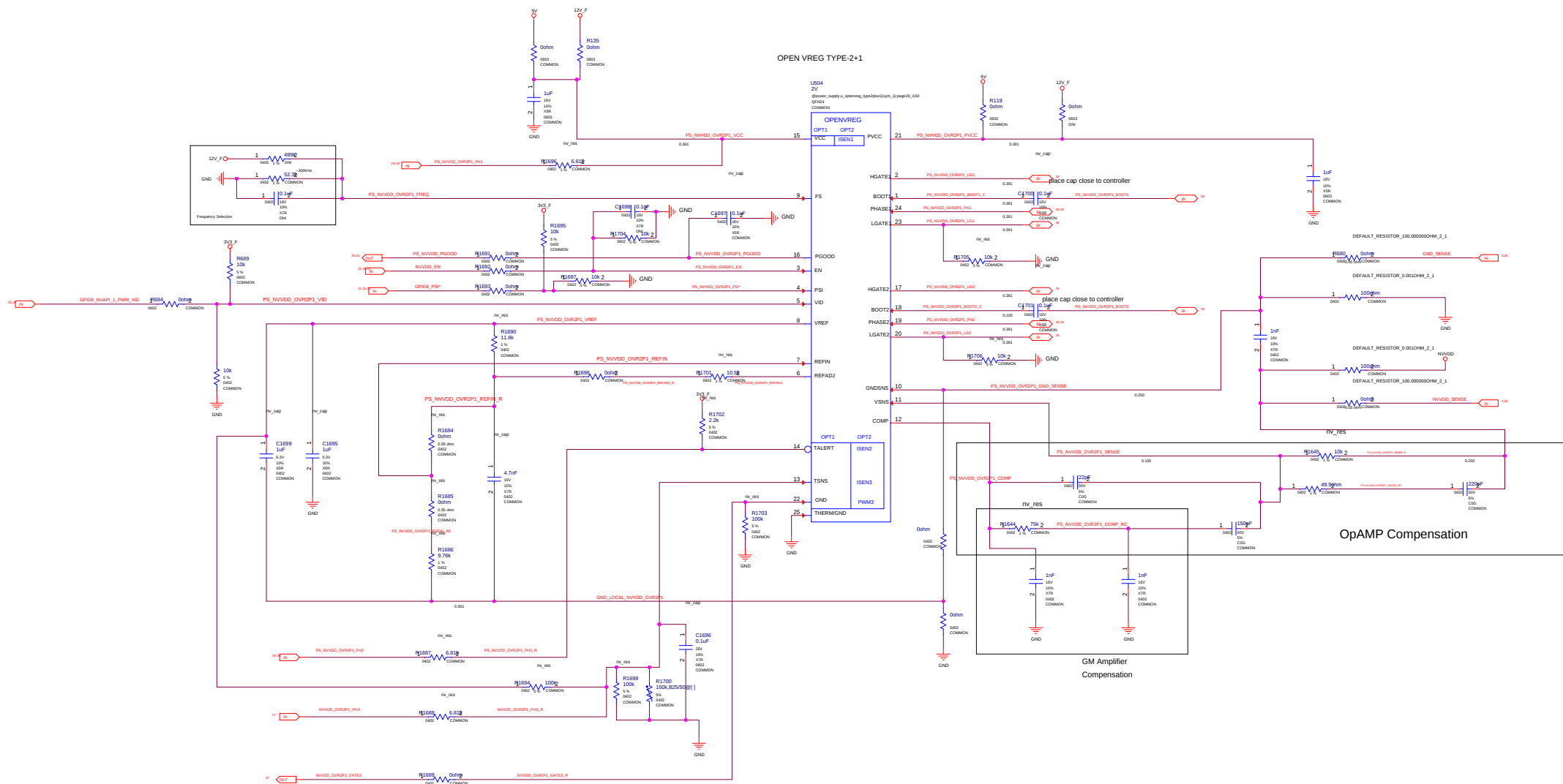
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[RESERVED]

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PS: NVVDD OVR2+1 POWER



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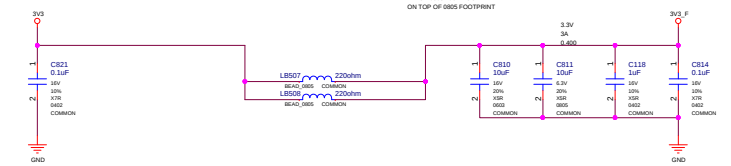
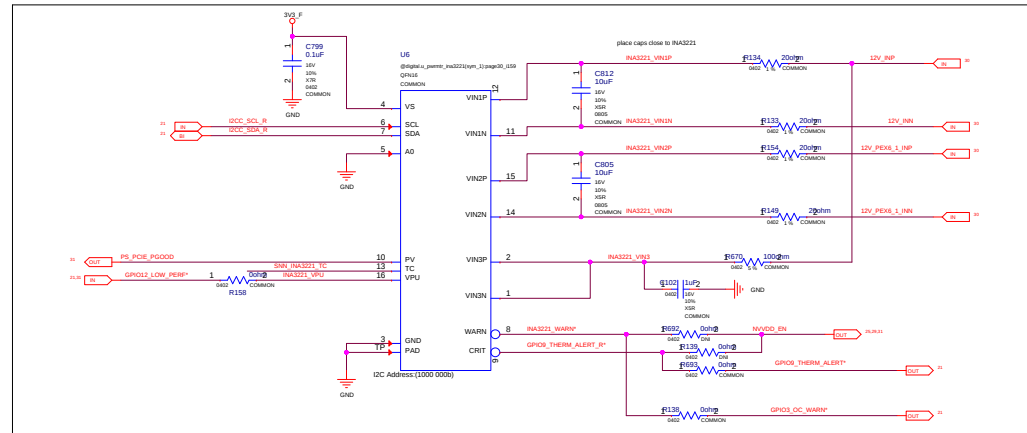
NV_PN	600-1G301-BASE-200
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BOM REV	A	DATE	09-OCT-2014

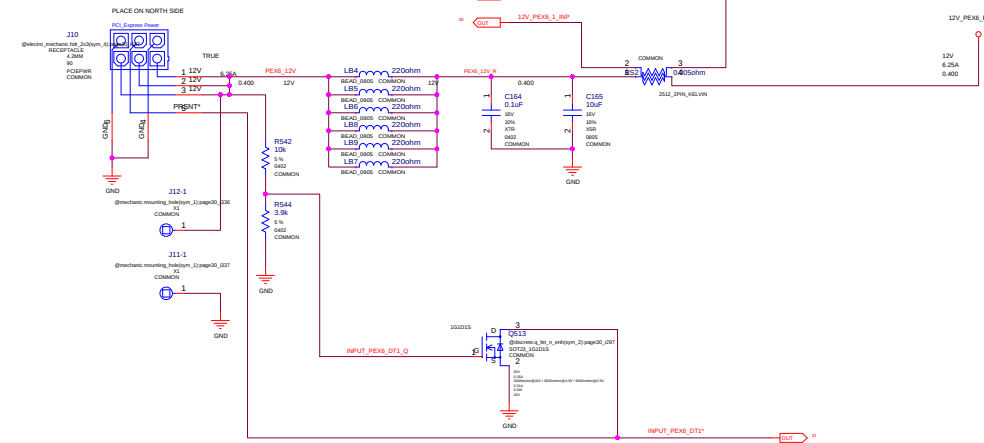
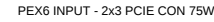
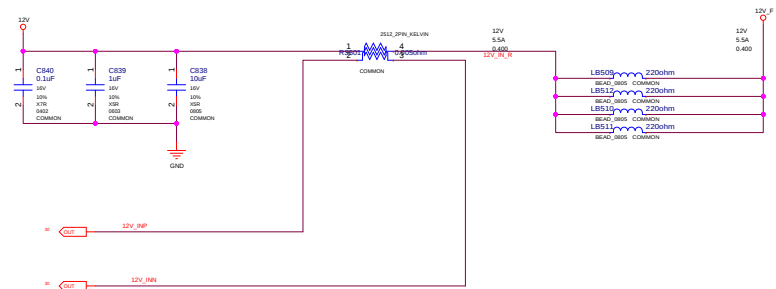
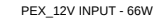
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD OVR2+1 option

PS: Inputs, Filtering, and Monitoring



PLACE 0603 10UF FOOTPRINT
ON TOP OF C005 FOOTPRINT



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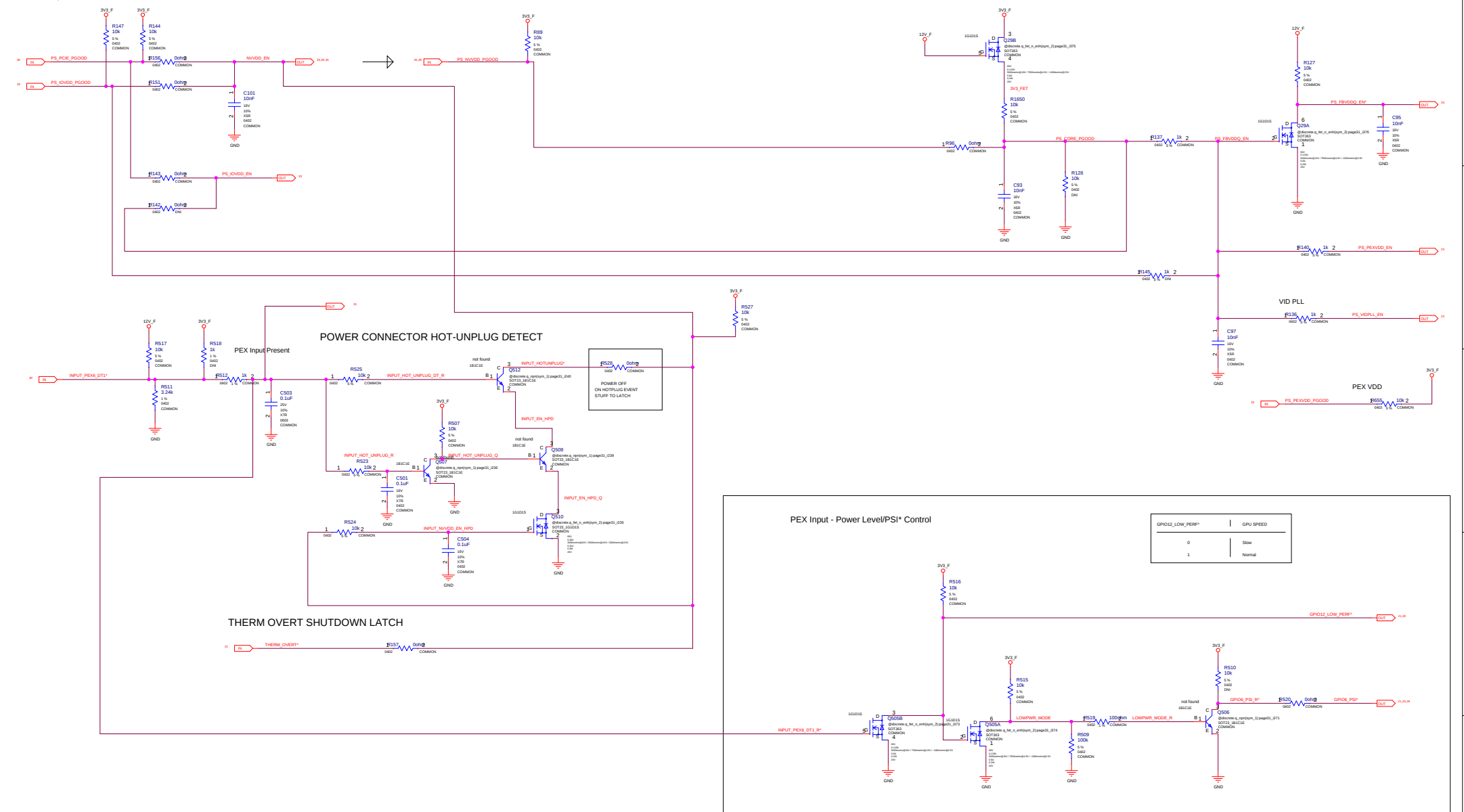
NV_PN	600-1G301-BASE-200
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Inputs, Filtering, and Monitoring

PS: Sequence and Shutdown



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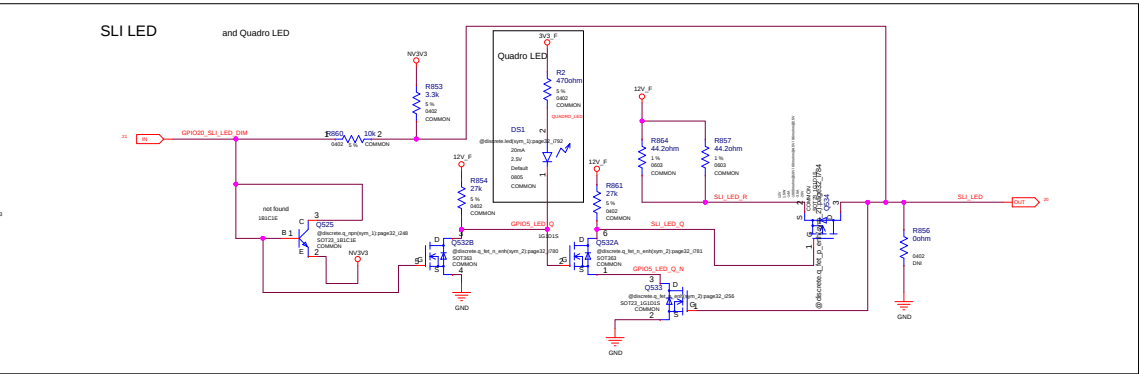
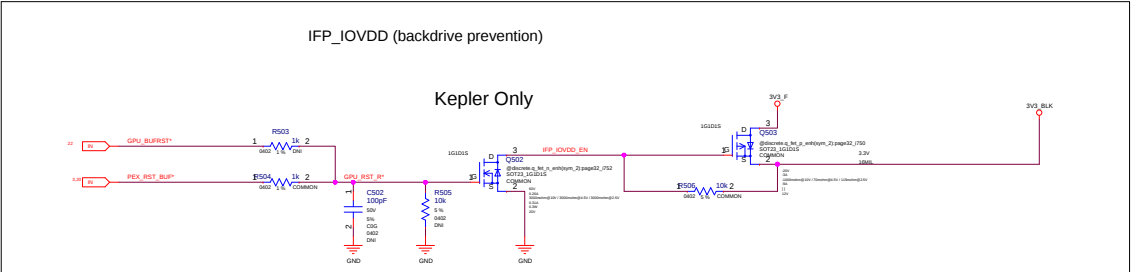
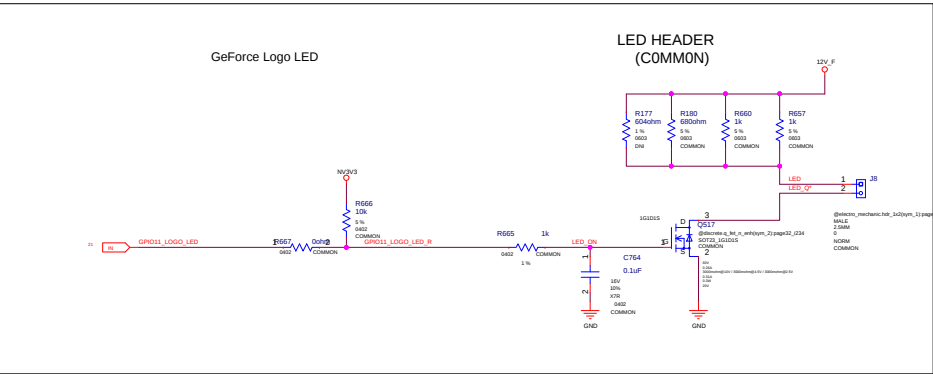


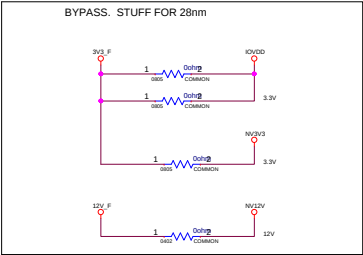
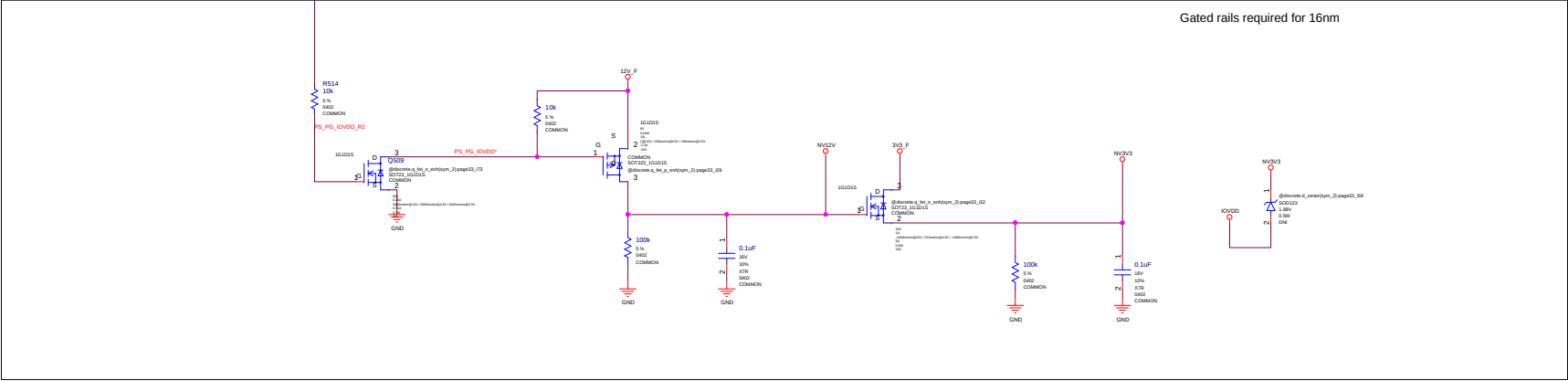
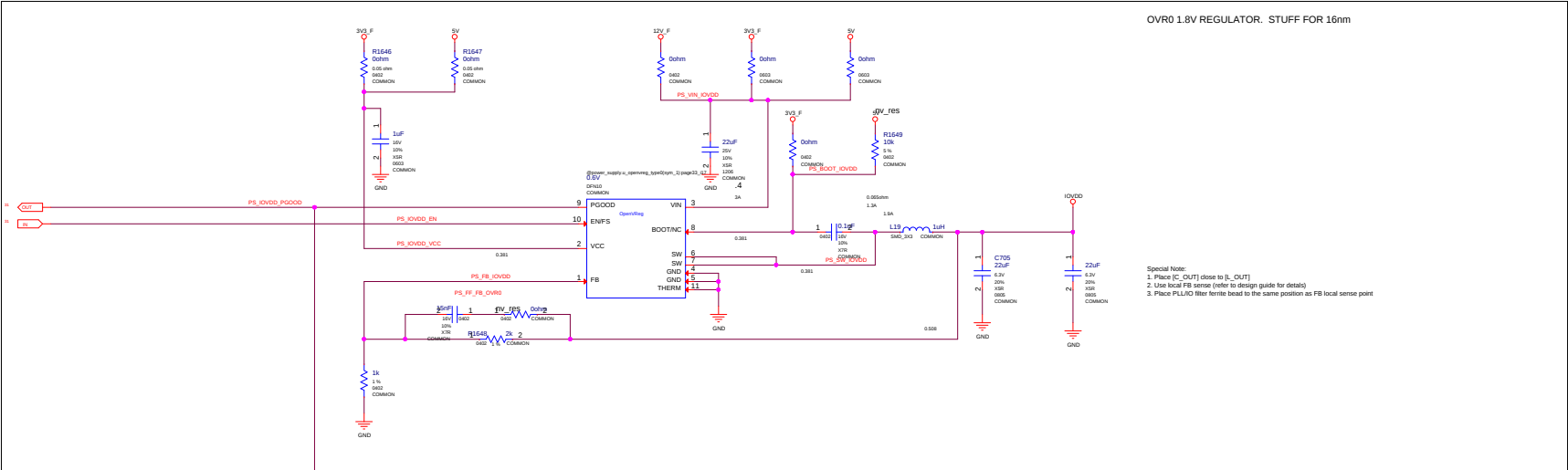
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Sequence and Shutdown

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LEDs





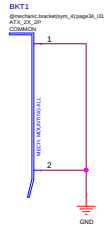
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: IOVDD Regulator

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Mechanical: Bracket/Thermal Solution

Brackets:

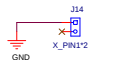


For DVI Connector

DVVDVI SCREWS with top tab



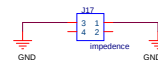
Reserve J3 - J20 for Impedance check



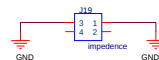
MEM Data
FBC_D<9>
Top
0.129mm / 47ohm +/- 10%
Reference L2 GND



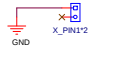
SLU Data
MOA_D7
L3
0.103mm / 52ohm +/- 10%
Reference L2 GND



MEM CLK
FBA_CLK<FBA_CLK1*
L3_inner
0.103mm / 52ohm +/- 10%
Reference L2_inner GND



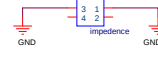
HDMI TMDS signals
IFPC_TXC<IFPC_TXC*
L4_inner
0.104mm / 26ohm / 95ohm +/- 10%
Reference L5_inner GND



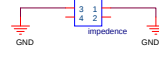
RGB signal
DACA_GREEN_DVI
Bottom
0.103mm / 52ohm +/- 10%
Reference L5_inner GND



MEM Address
FBC_CMD<4>
L4
0.127mm / 47ohm +/- 10%
Reference L5 GND



PEX_PCEI / DVI IFPEF
PEX_RX13<PEX_RX13* IFPEF_TXC_C*_RIIFEF_TXC_C_R
TOP
0.101mm / 123mm / 90ohm +/- 10%
Reference L2_inner GND



PEX_PCEI / DVI IFPAB
PEX_TX6<PEX_TX6* IFPAB_TXD1_C*_RIIFPAB_TXD1_C_R
Bottom
0.101mm / 123mm / 90ohm +/- 10%
Reference L5_inner GND



F_PAD_X



F_PAD_X



F_PAD_X



F_PAD_X



F_PAD_X



F_PAD_X



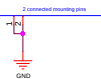
F_PAD_X



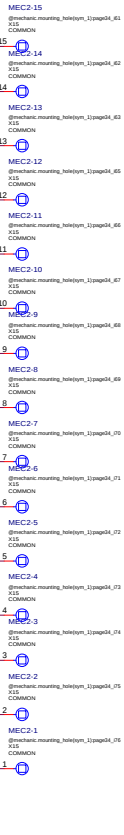
F_PAD_X

FET HS

COOLING SOLUTION



MEC1
[branch:mech_thermal_2_page04_01]
PWB
COMMON



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BOX REV	A

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