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	2. Add FBVDDQ decoupling capacitor
P13	Add NVVDD decoupling capacitor
P15	1. Add ESD PROTECTION
	2. Add AC Coupling capacitors
P16~18	Add ESD PROTECTION
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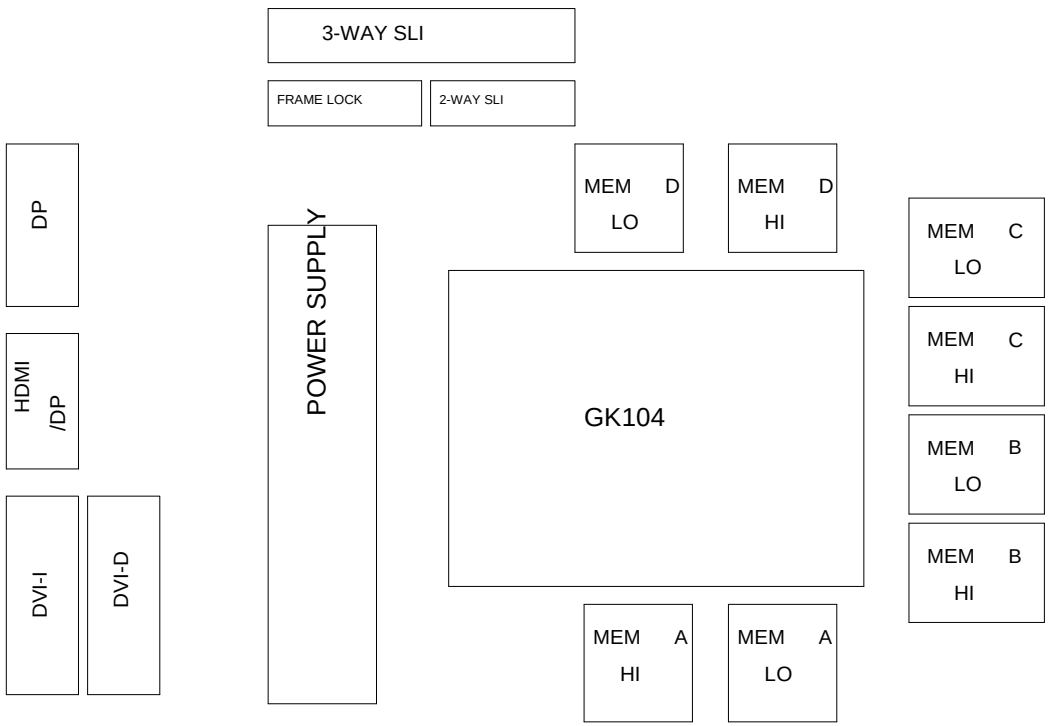

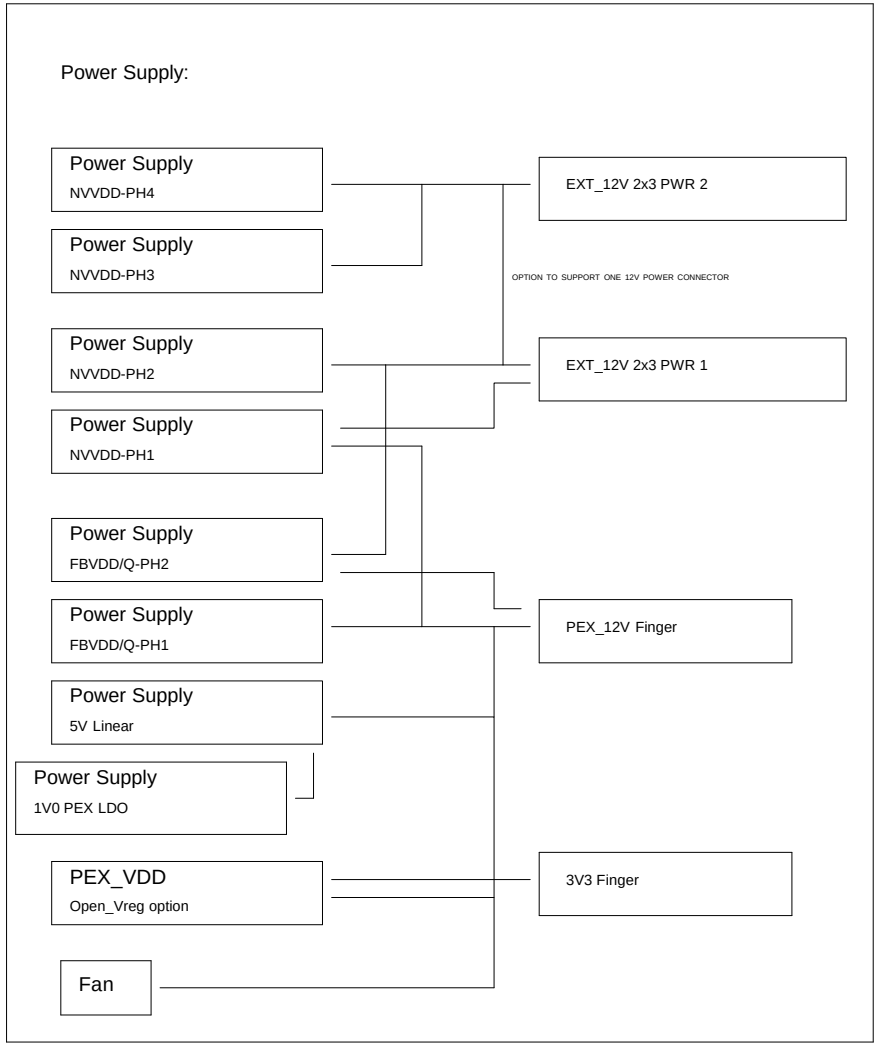

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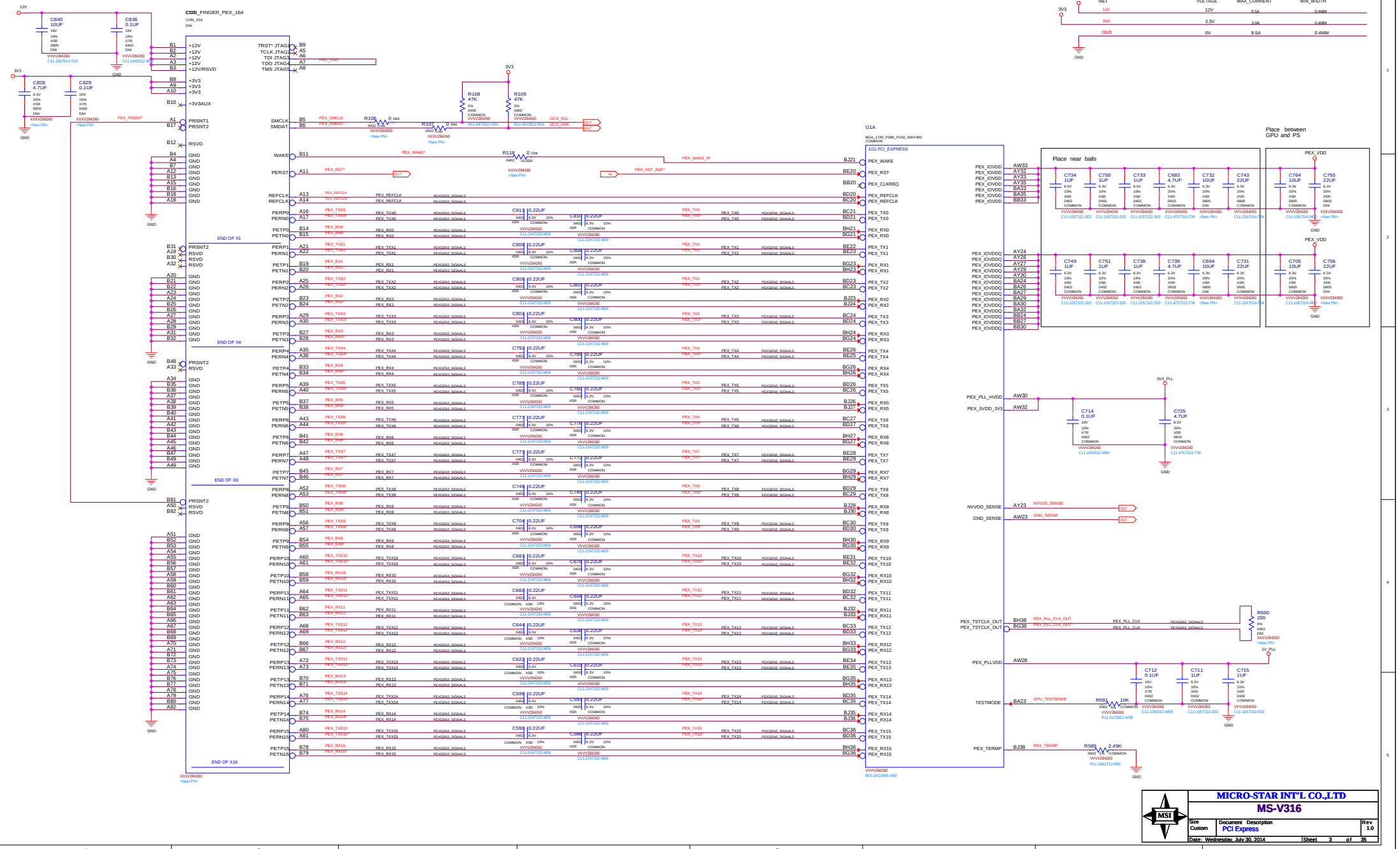
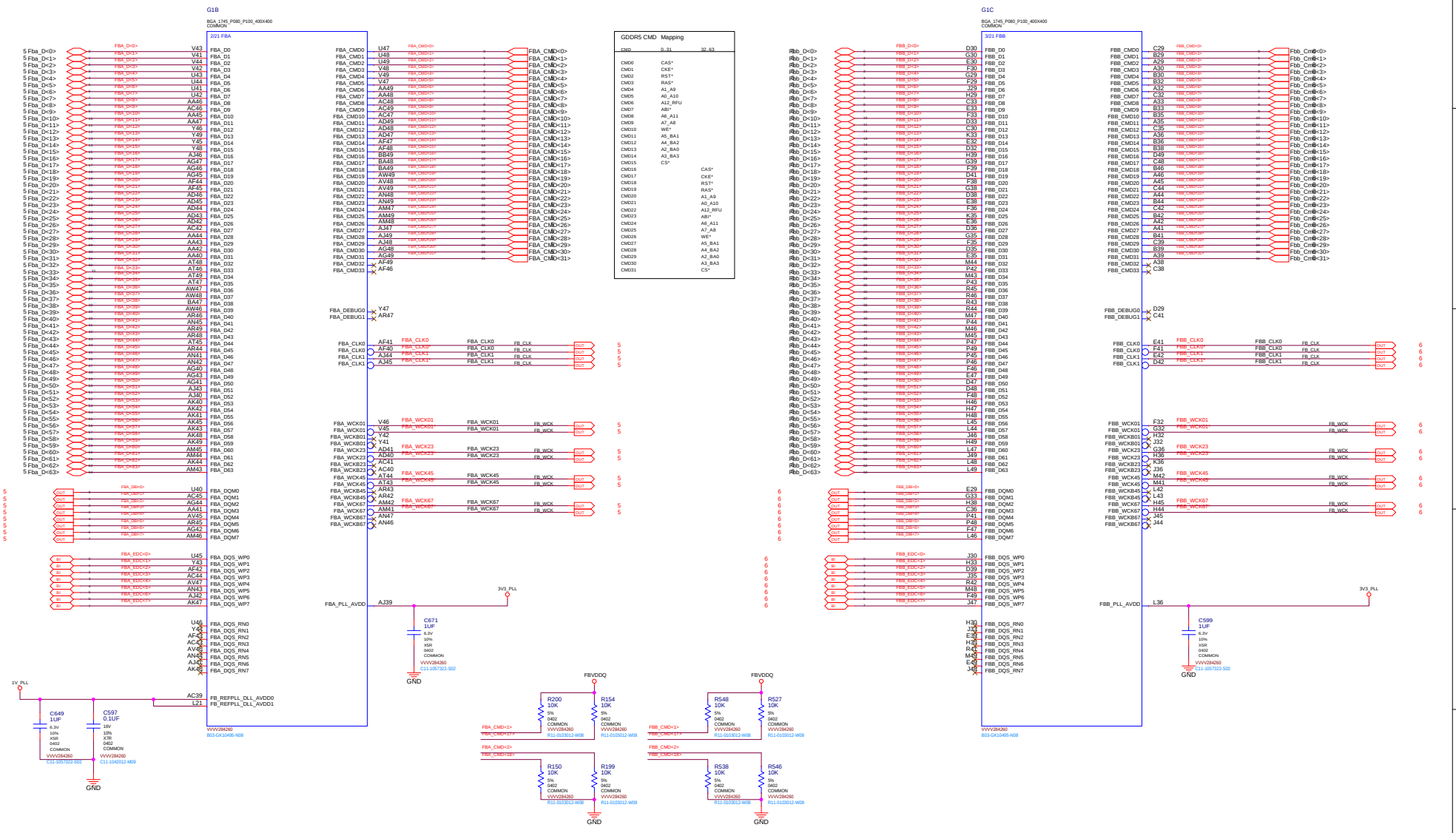
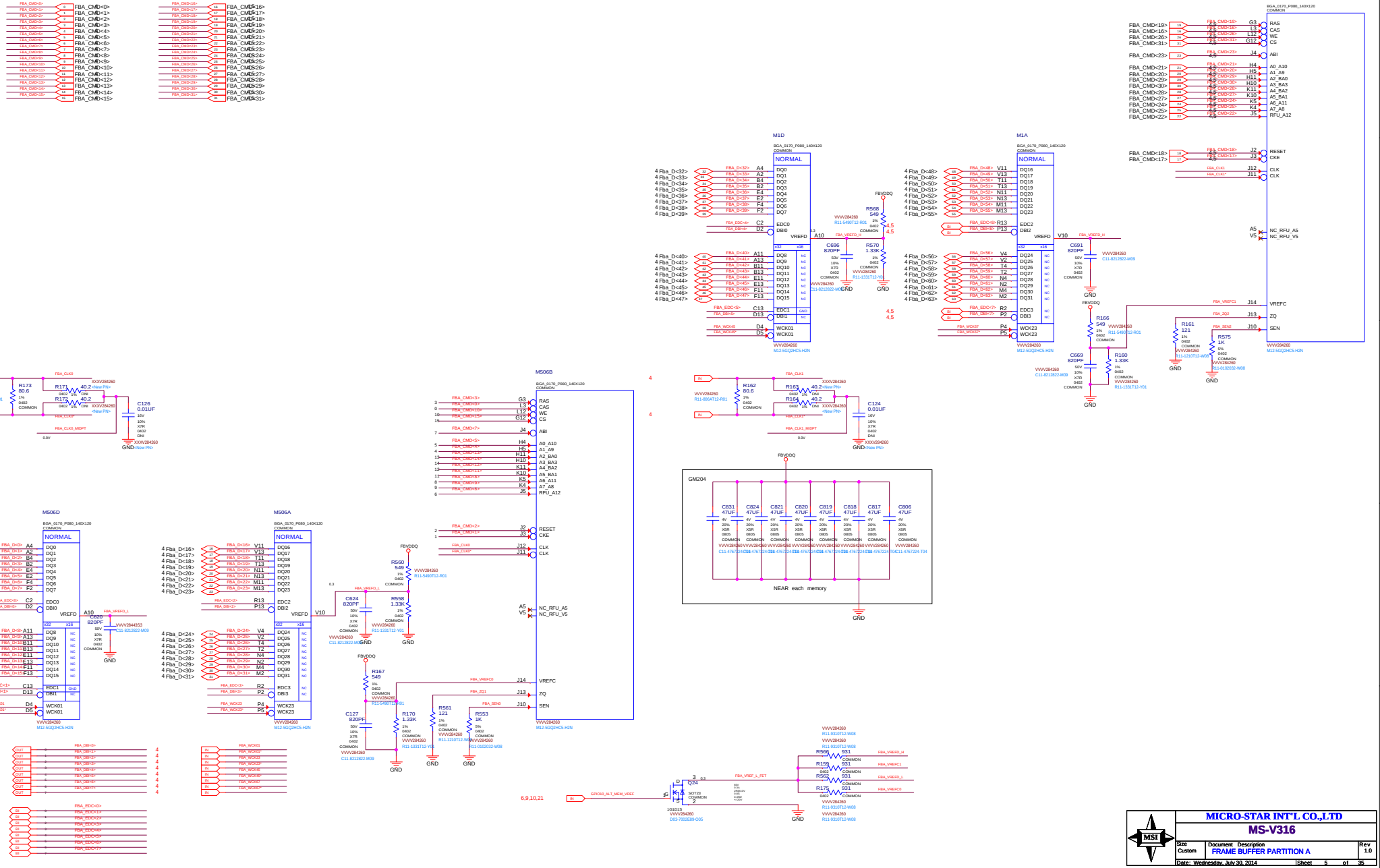
Page3: PCI Express



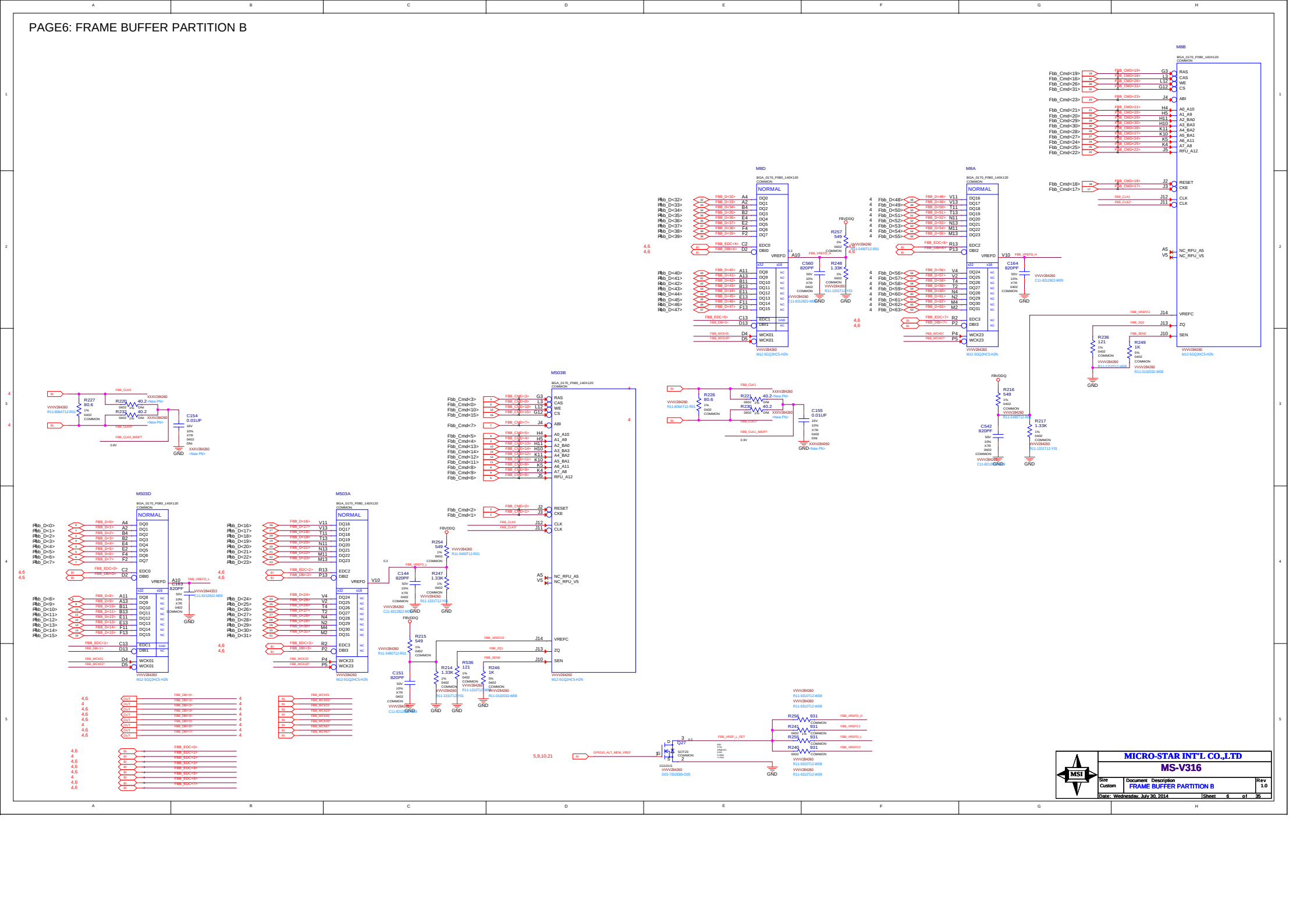
Page4: MEMORY: GPU Partition A/B



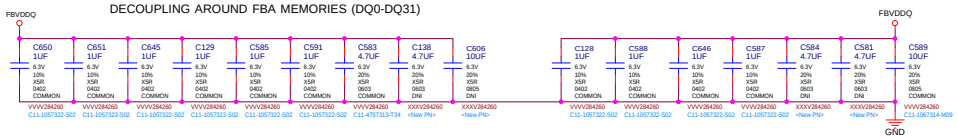
PAGE5: FRAME BUFFER PARTITION A

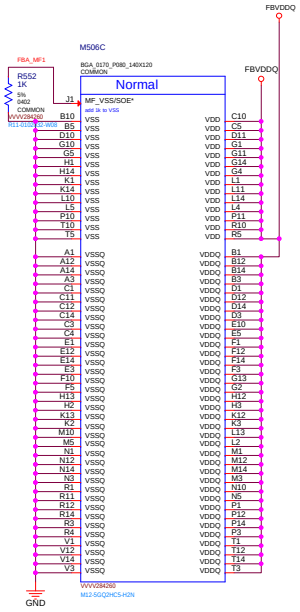


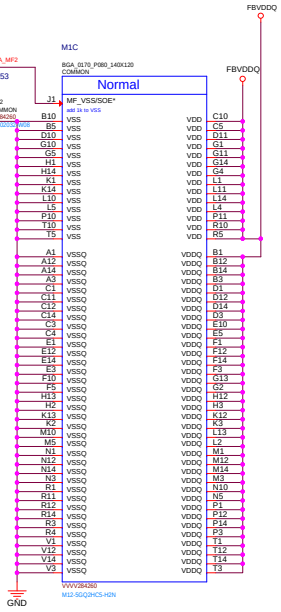
PAGE6: FRAME BUFFER PARTITION B

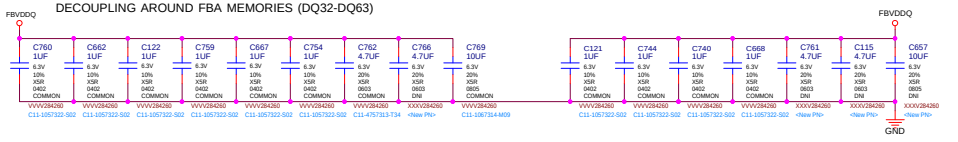


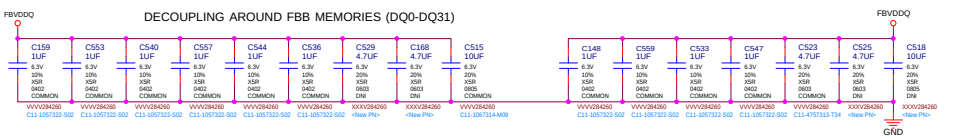
PAGE7: FRAME BUFFER PARTITION A/B DECOUPLING

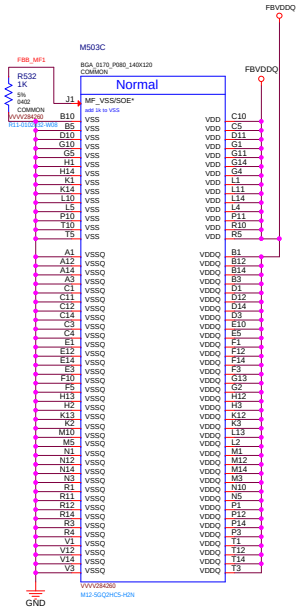


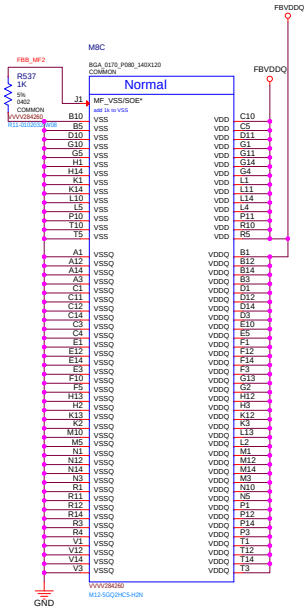


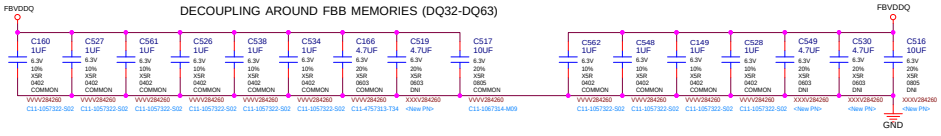












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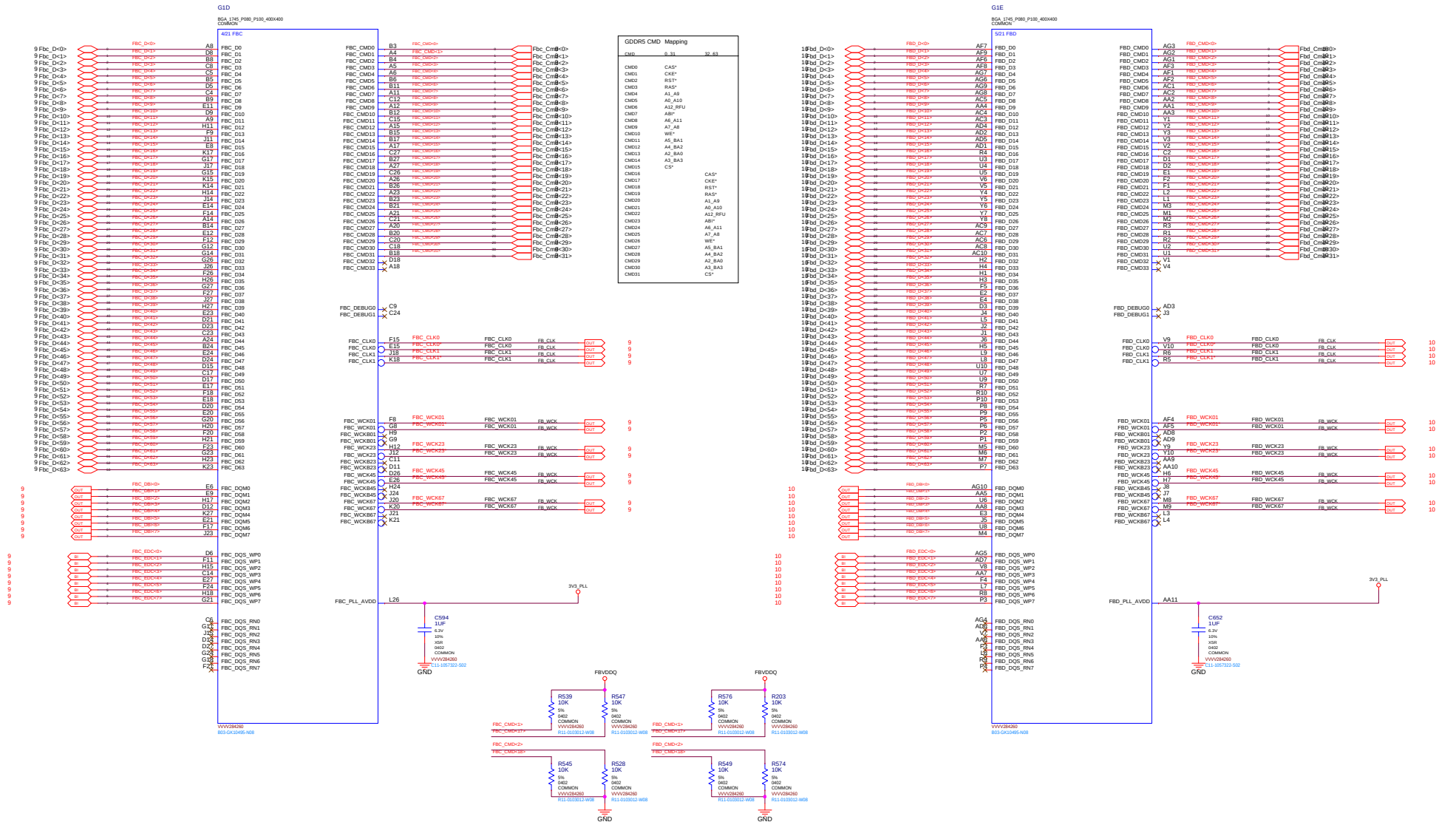
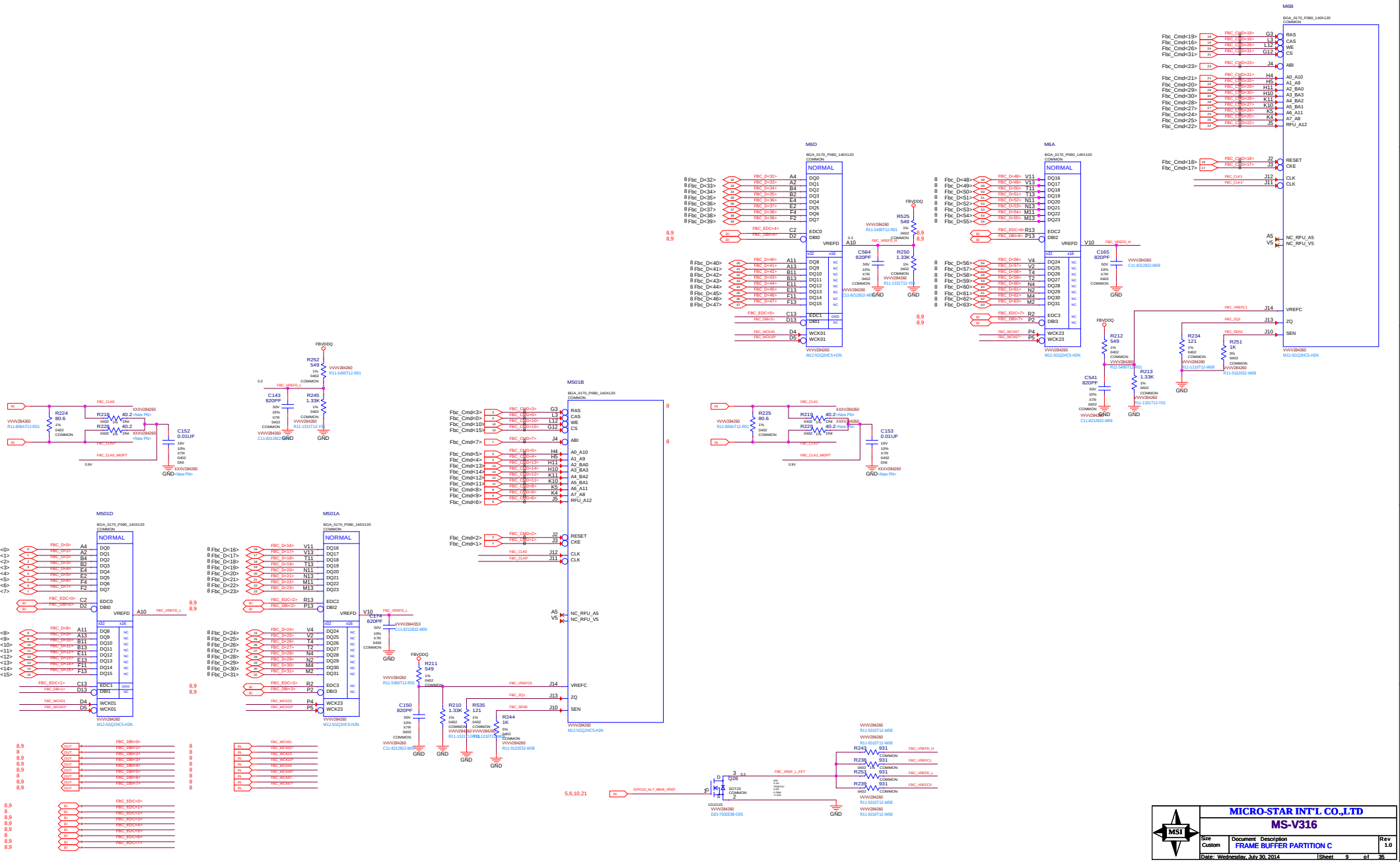
Page8: MEMORY: GPU Partition C/D



PAGE9: FRAME BUFFER PARTITION C



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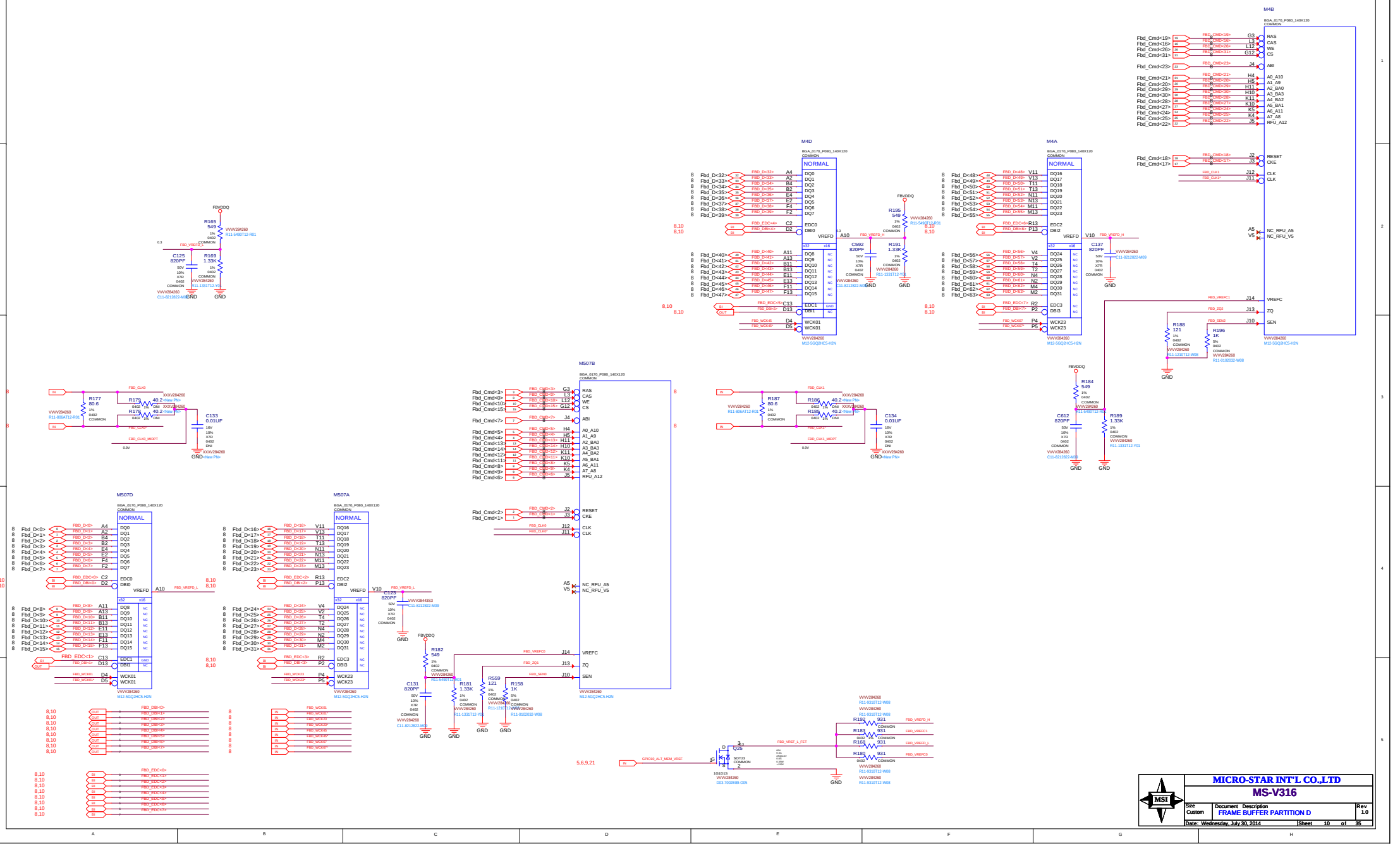
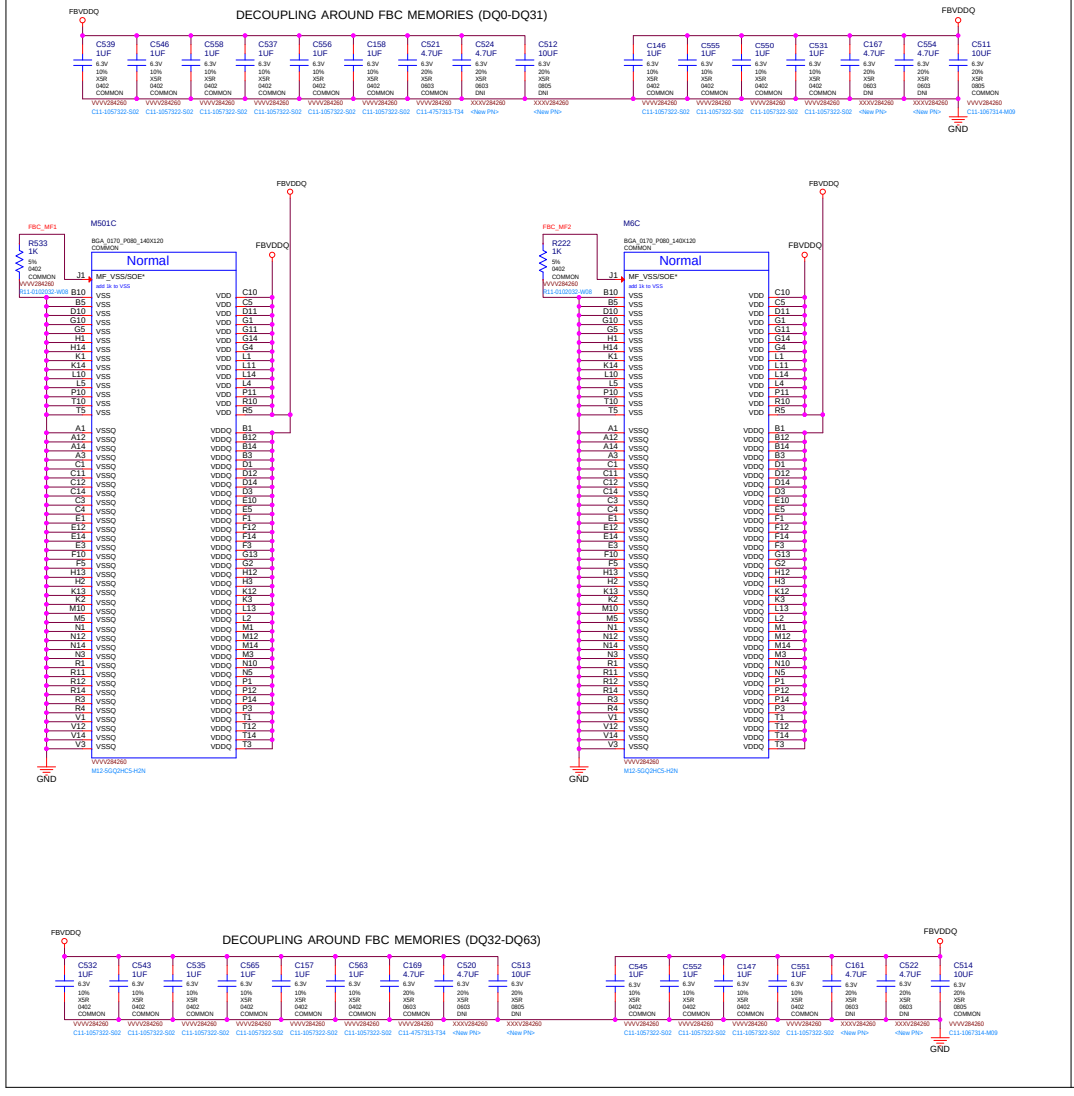
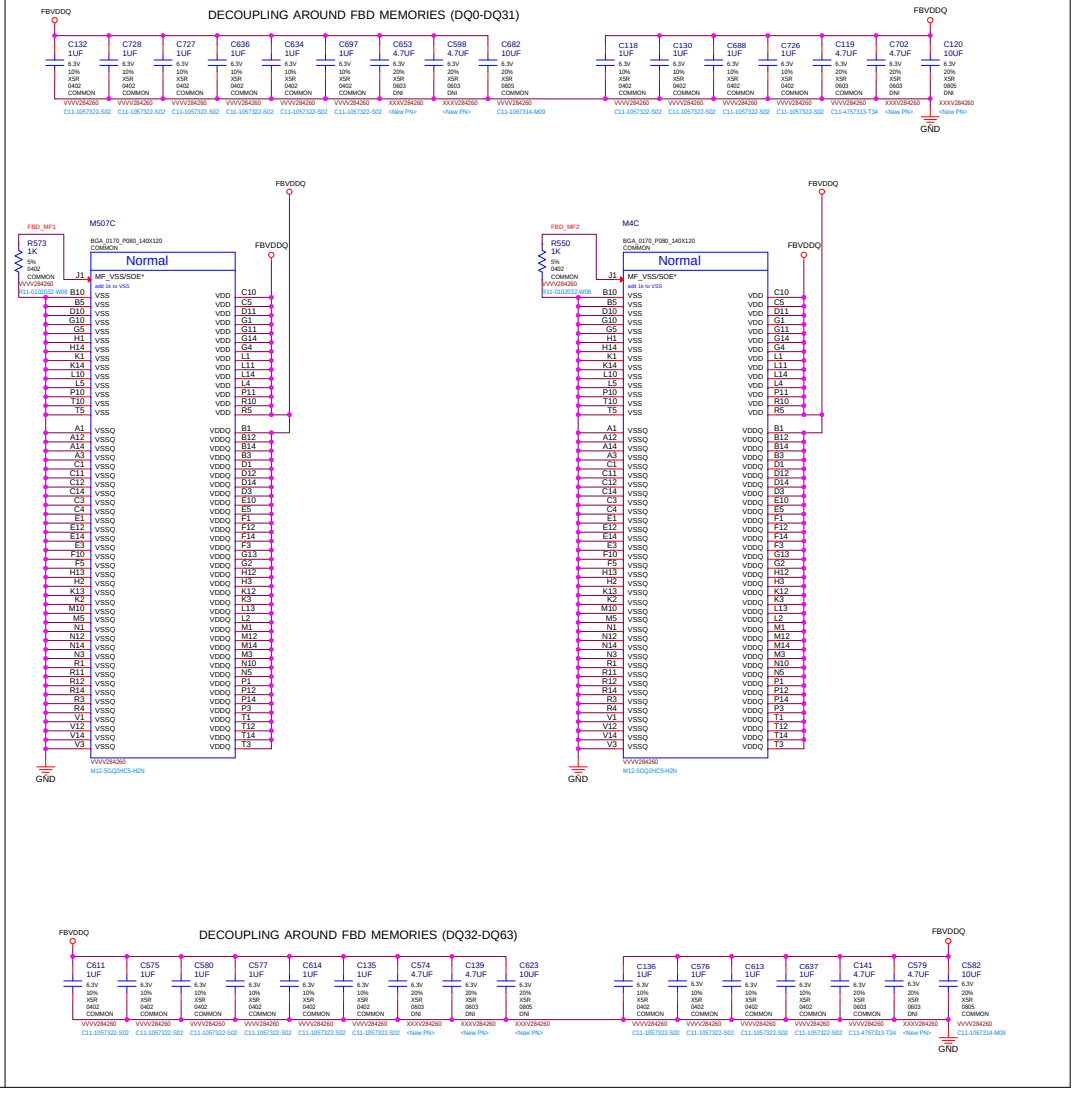
PAGE10: FRAME BUFFER PARTITION D



PAGE11: FRAME BUFFER PARTITION C/D DECOUPLING





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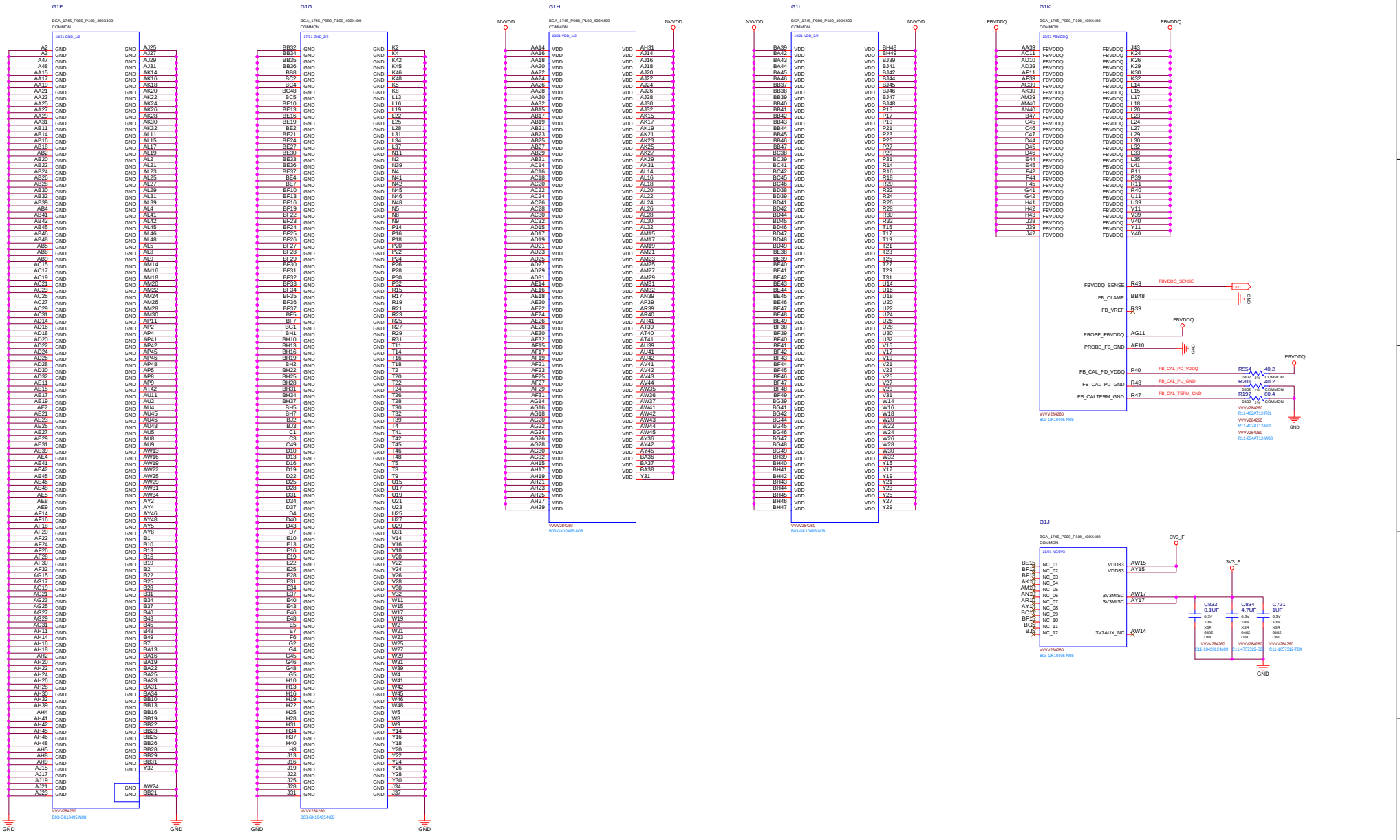
Page12: GPU PWR and GND



Page13: GPU Decoupling

Based on GB2-X GDDR5 FBVDDQ Decap Guideline

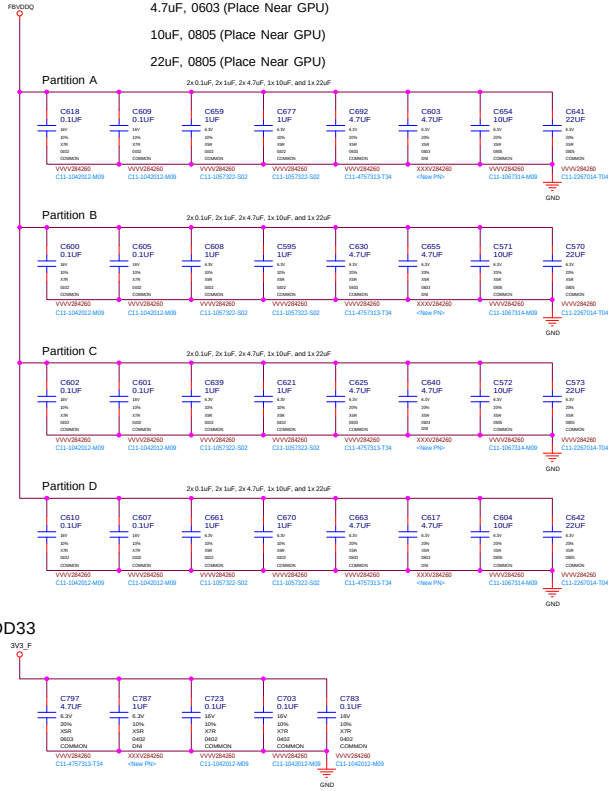
FBVDDQ

0.1uF, 0.47uF & 1uF, 0402 (Place Under GPU)

4.7uF, 0603 (Place Near GPU)

10uF, 0805 (Place Near GPU)

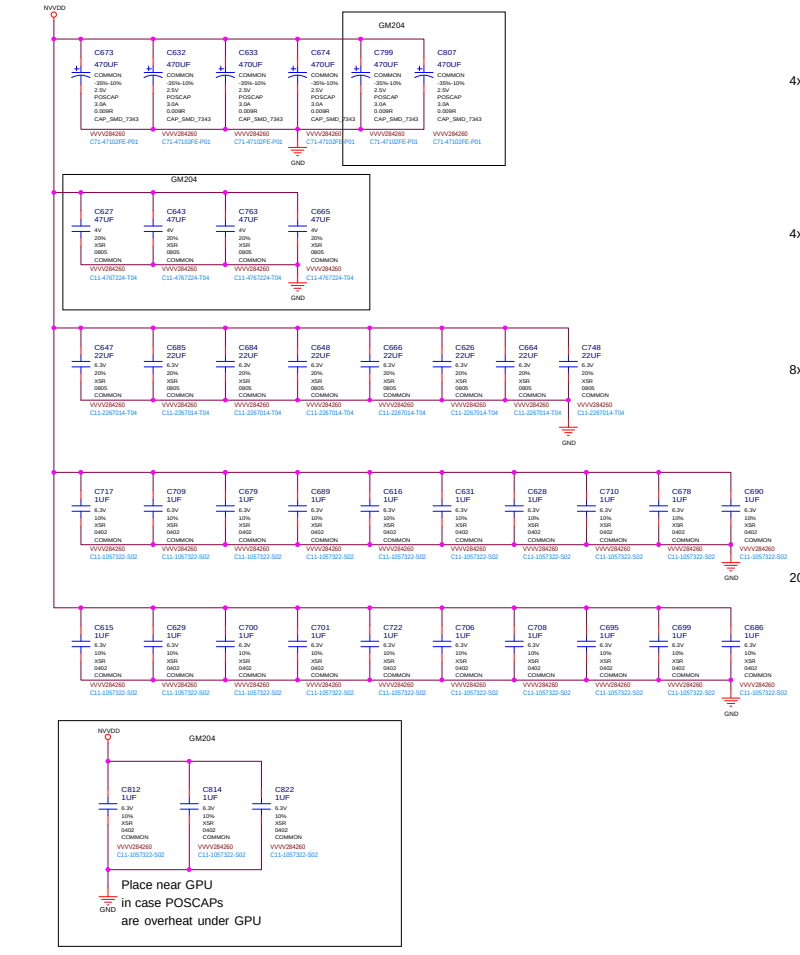
22uF, 0805 (Place Near GPU)



VDD33

NVVDD Decoupling caps. Place under GPU.

NVVDD



4x 330uF, 7343

4x 47uF, 0805

8x 22uF, 0805

20x 1uF, 0402

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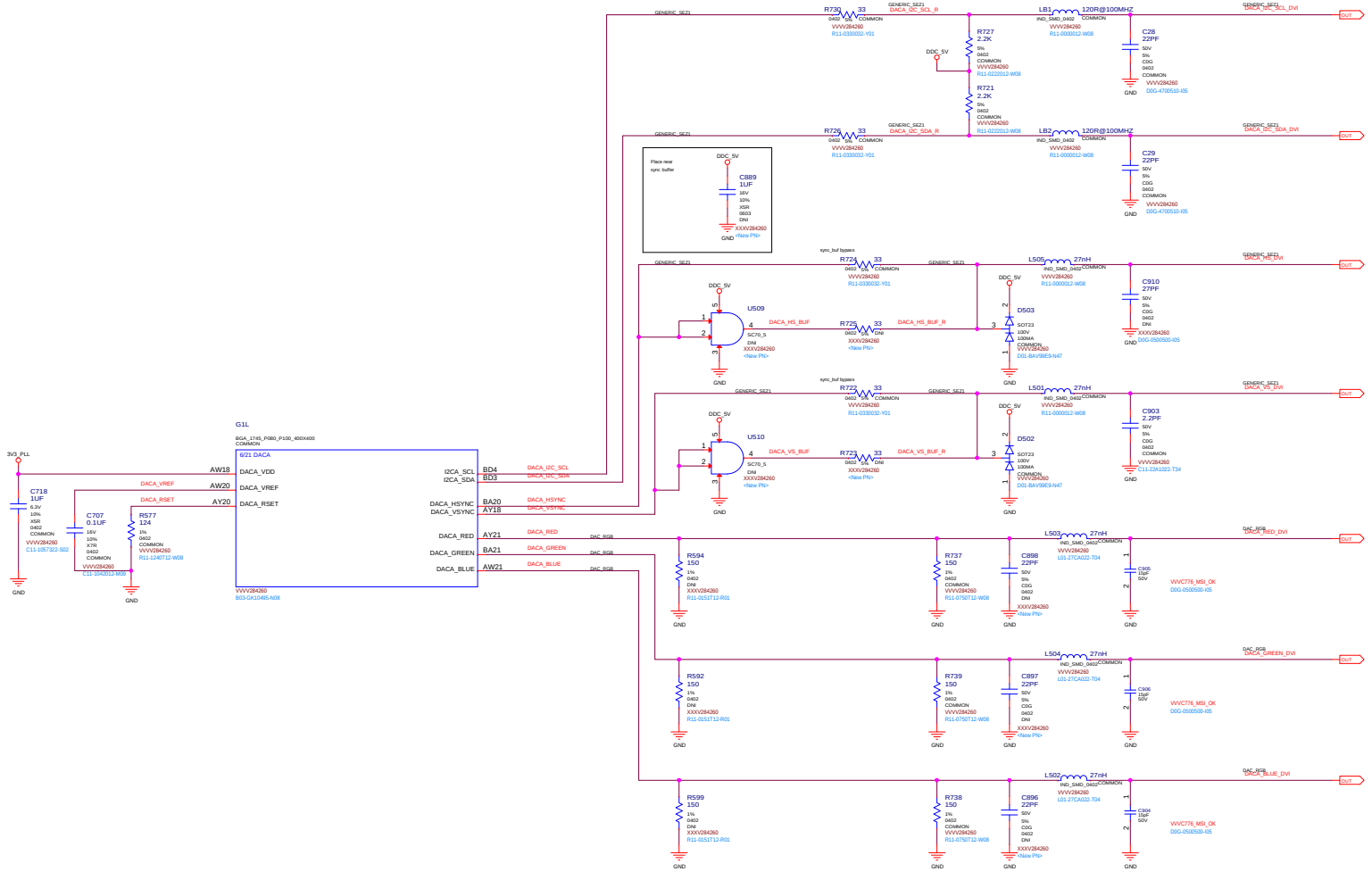
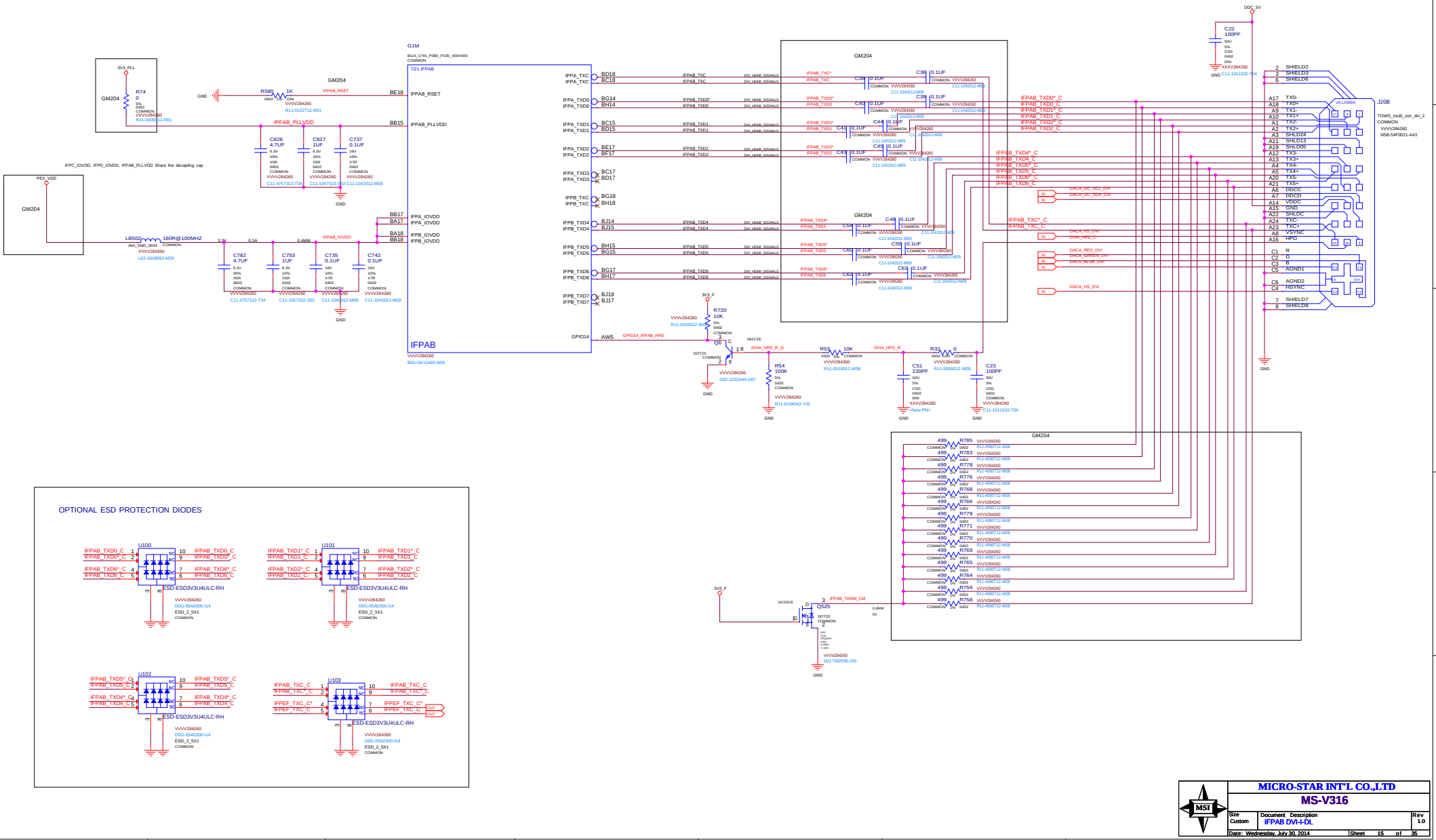
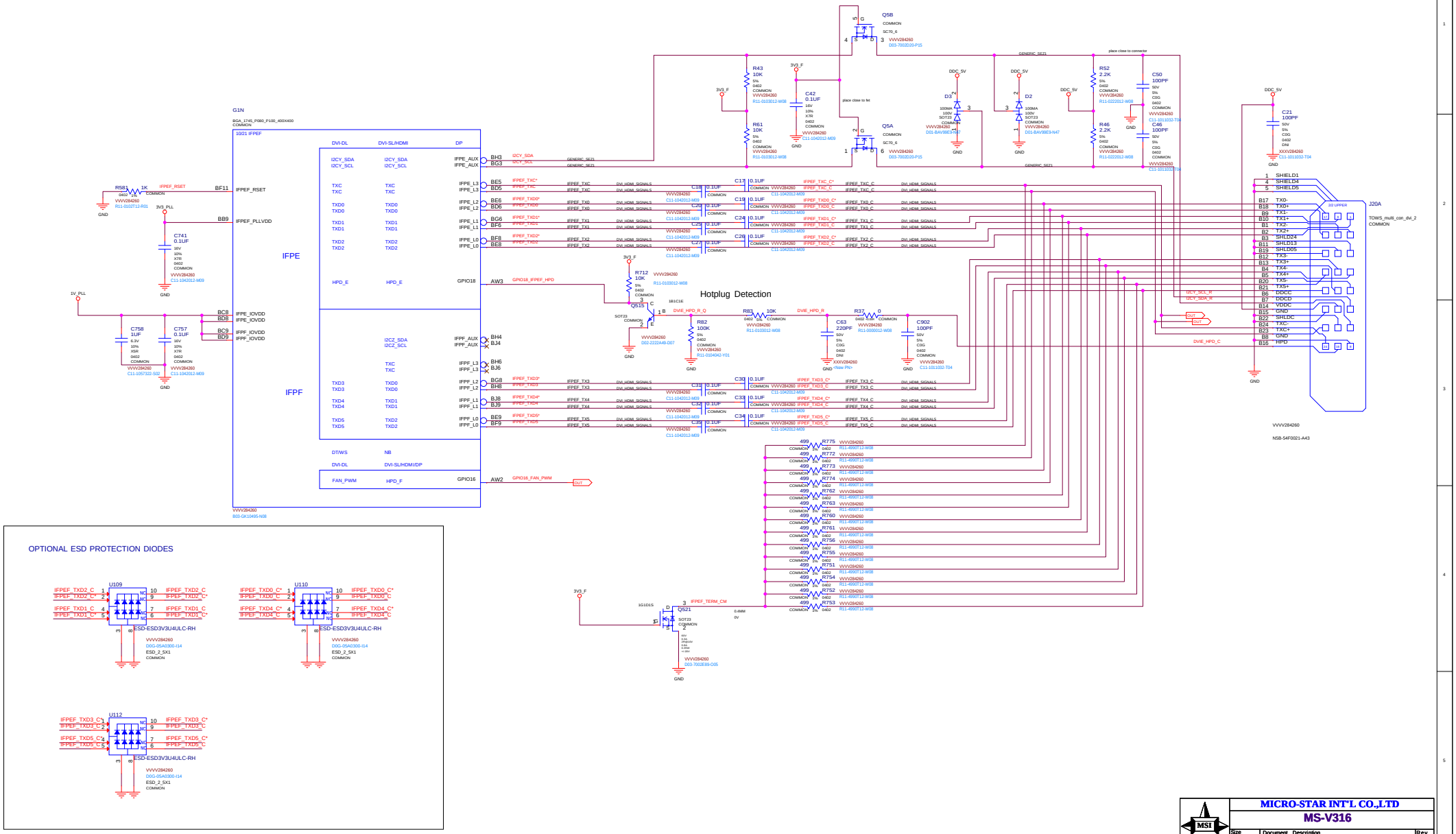
Page14: DACA Interface



Page15: IFPAB DVI-I-DL



Page16: IFPEF DVI-D-DL



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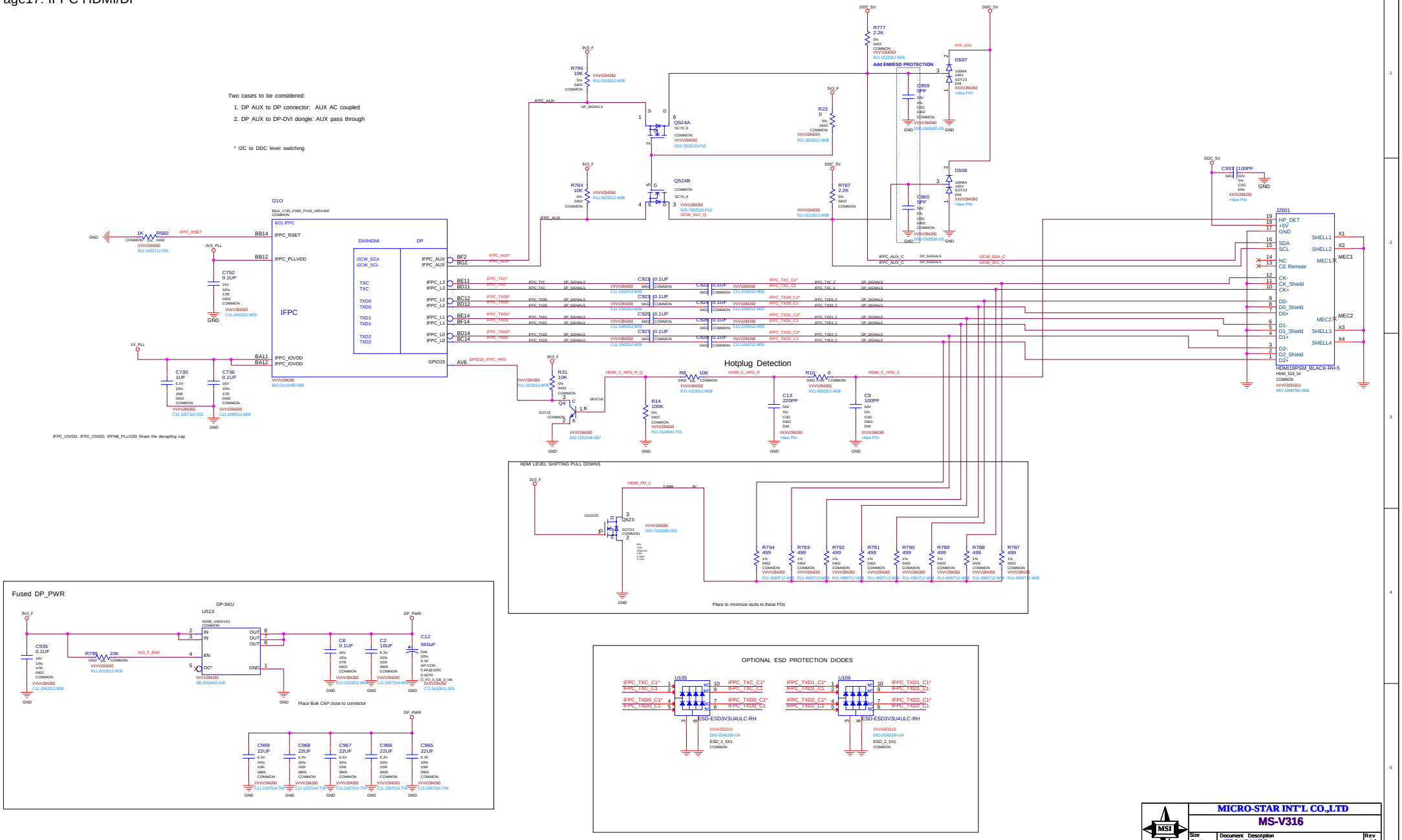
Page17: IFPC HDMI/DP



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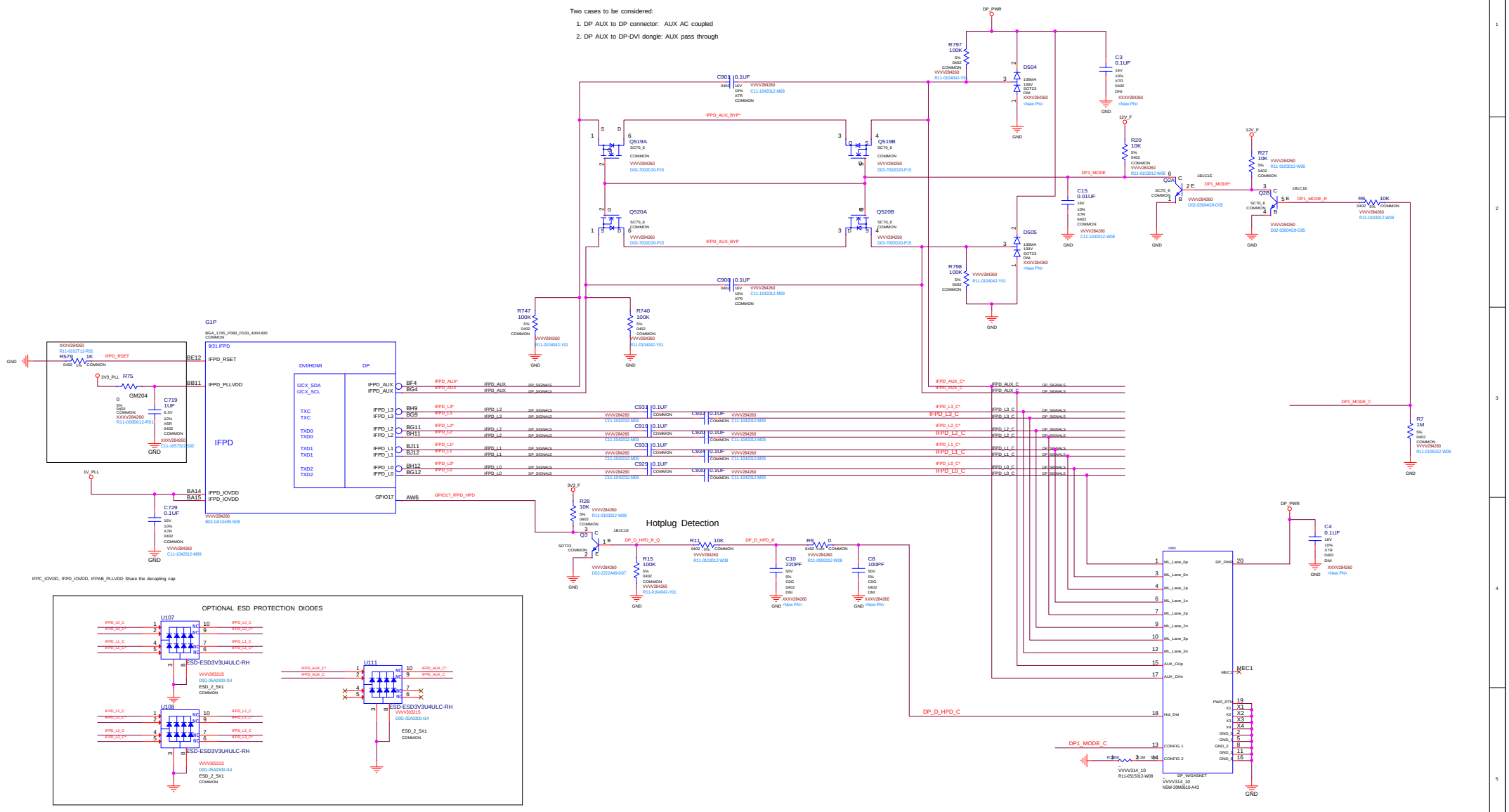
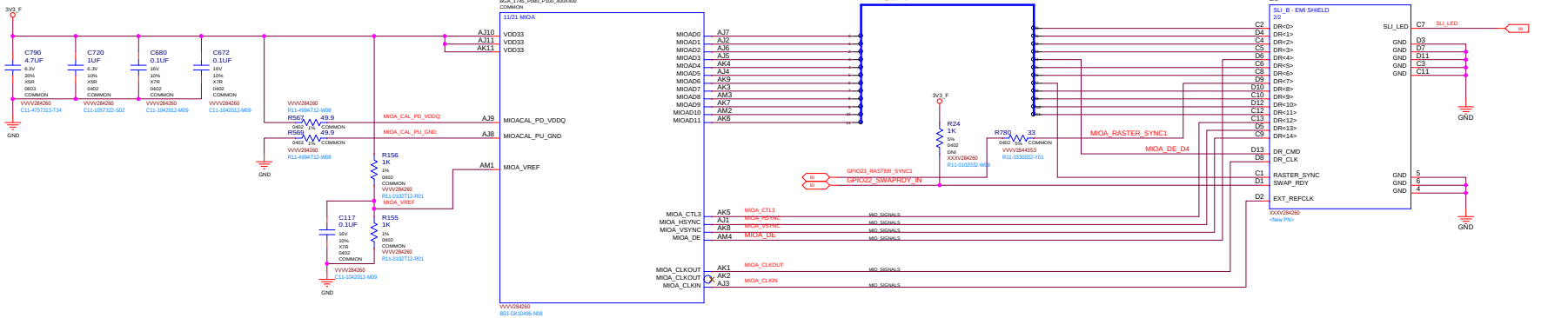
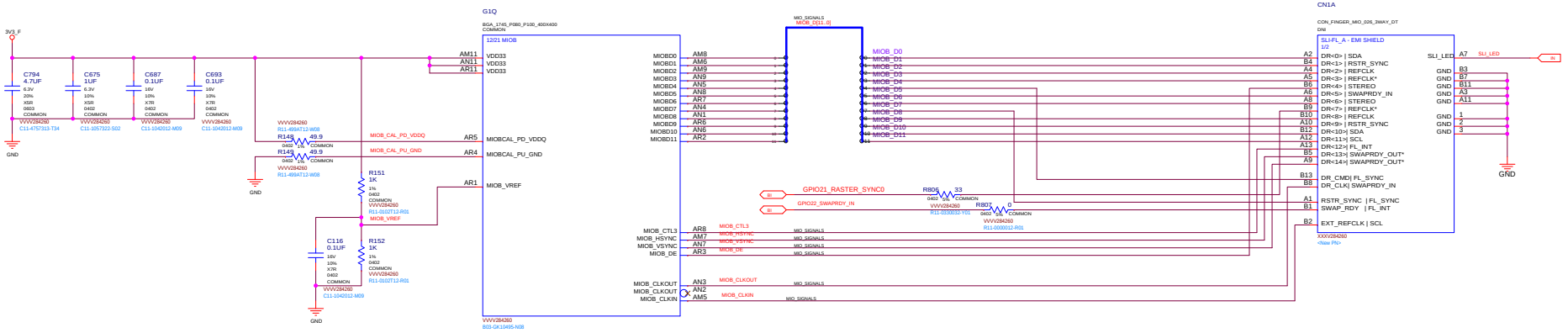
Page18: IFPD DP



Page19: MIOA/B Interface and Frame Lock





Page20: Stereo Connector

remove

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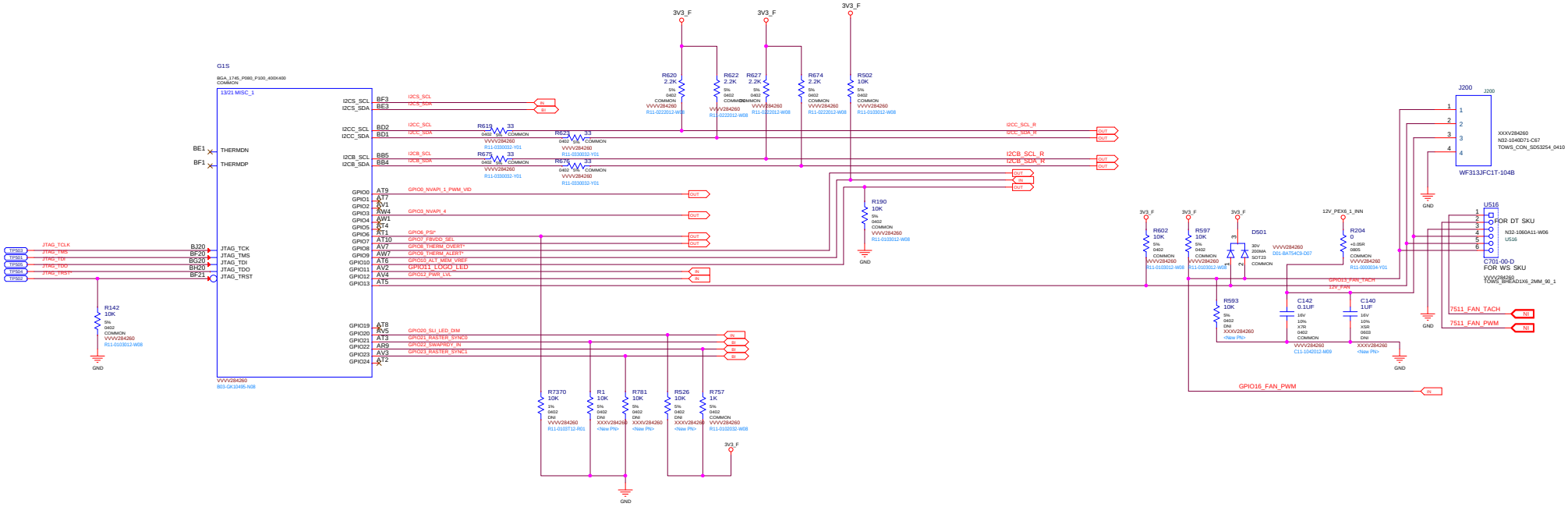
Page21: MISC1: Fan, Thermal, JTAG, GPIO



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Page22: MISC2: ROM, XTAL, Straps

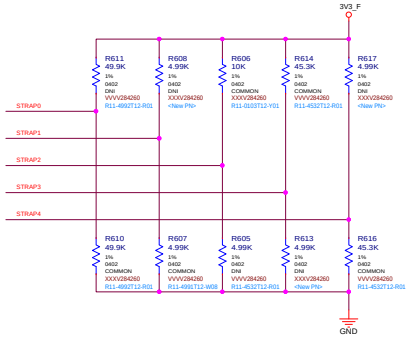
STRAP0	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	1001 - (0x1189)*	10K PU -325 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*
STRAP4	DP_PLL_VDD_33V*	1* FOR 3_3V*	
	PEX_MAX_SPEED*	1* FOR GEN2/3*	45K PD*
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	
	*		
ROM_SI	RAMCFG[0]*	0*	
	RAMCFG[1]*	1*	64Mx32 256 bit hynix for SKUS primary memory
	RAMCFG[2]*	1*	35K PD*
	RAMCFG[3]*	0*	
ROM_SO	VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	
	FB[0]_APERTURE_SIZE*	1* For 128MB*	30k PD*
	FB[1]_APERTURE_SIZE*	0* For 128MB*	
ROM_SCLK	PEX_PLL_EN_TERM100*	0* DISABLE*	
	PCI_DEVID_EXT[5]*	0* For 0x1189*	
	SUB_VENDOR*	1* Dedicated BIOS*	25K PD*
	PCI_DEVID_EXT[4]*	0* For 0x1189*	

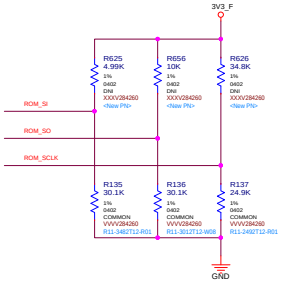
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

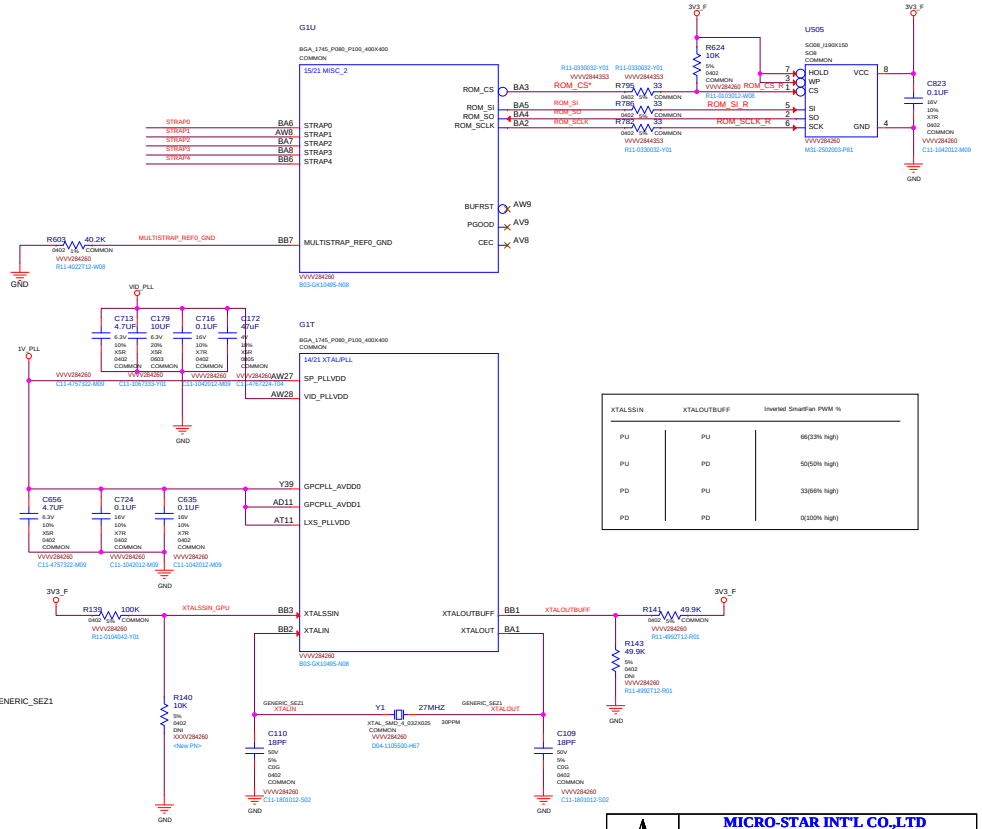
X32 MODE 256bit

CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	32Mx32 256-bit	Elpida
0010	32Mx32 256-bit	Hynix
0011	32Mx32 256-bit	Samsung
0100	Reserved	
0101	64Mx32 256-bit	Elpida
0110	64Mx32 256-bit	Hynix
0111	64Mx32 256-bit	Samsung

	MULTI_STRAP_REF0_GND
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND







XTALSSIN	XTALOUTBUFF	Inverted SmartFan PWM %
PU	PU	66(33% high)
PU	PD	50(50% high)
PD	PU	33(66% high)
PD	PD	0(100% high)

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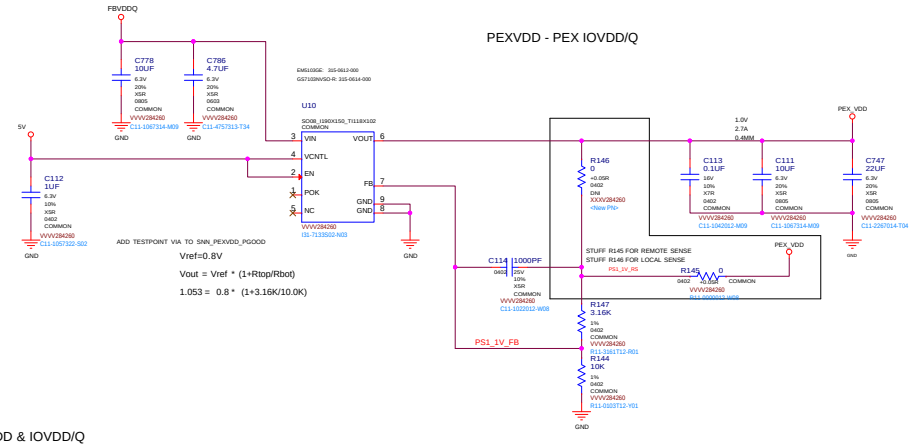
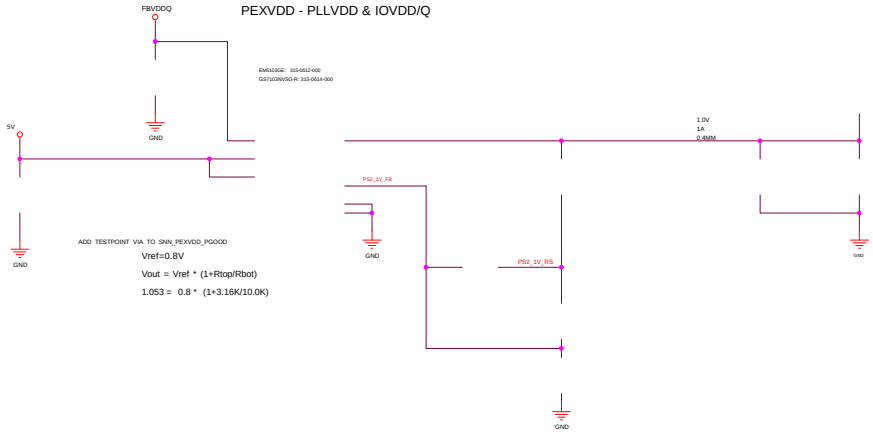
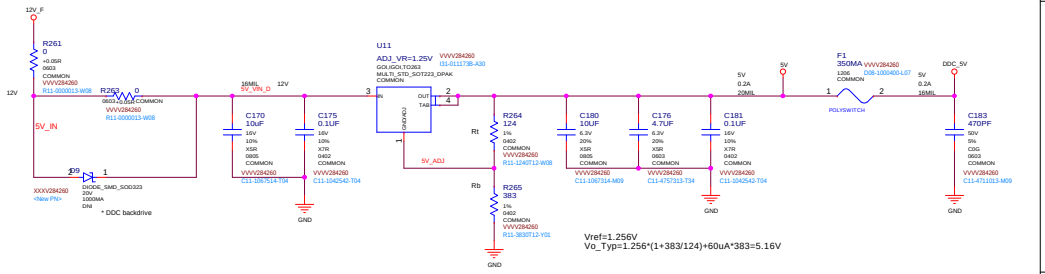
PEXVDD - PEX IOVDD/Q



PEXVDD - PLLVDD & IOVDD/Q



PEXVDD - PLLVDD & IOVDD/Q



REMOVE PEXVDD PWM

Vref=0.8V
Vo_Typ=0.8*(1+1K/3.09K)=1.059V

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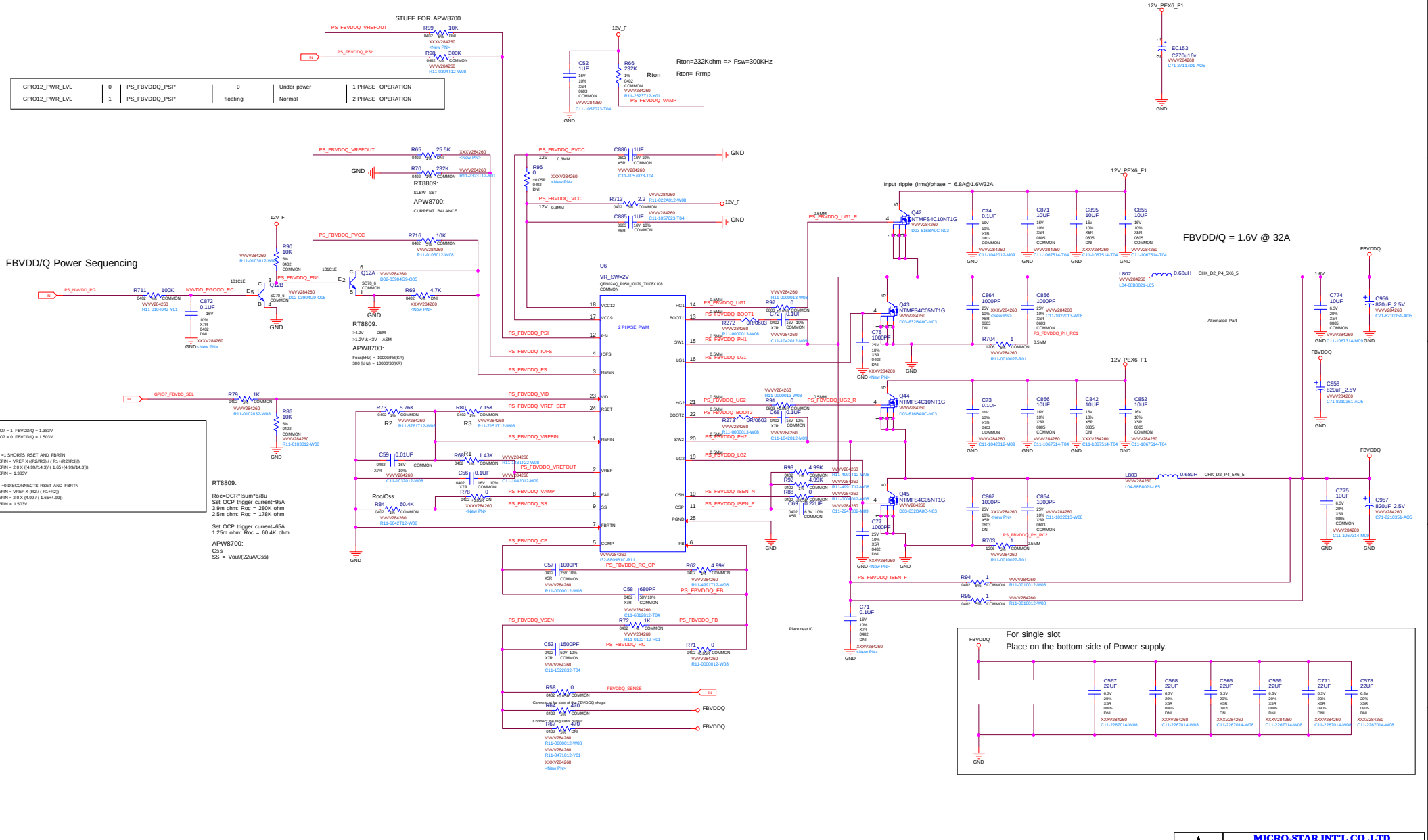
Page24: PS: FBVDD/Q



GPIO12_PWR_LVL	0	PS_FBVDDQ_PSI*	0	Under power	1 PHASE OPERATION
GPIO12_PWR_LVL	1	PS_FBVDDQ_PSI*	floating	Normal	2 PHASE OPERATION

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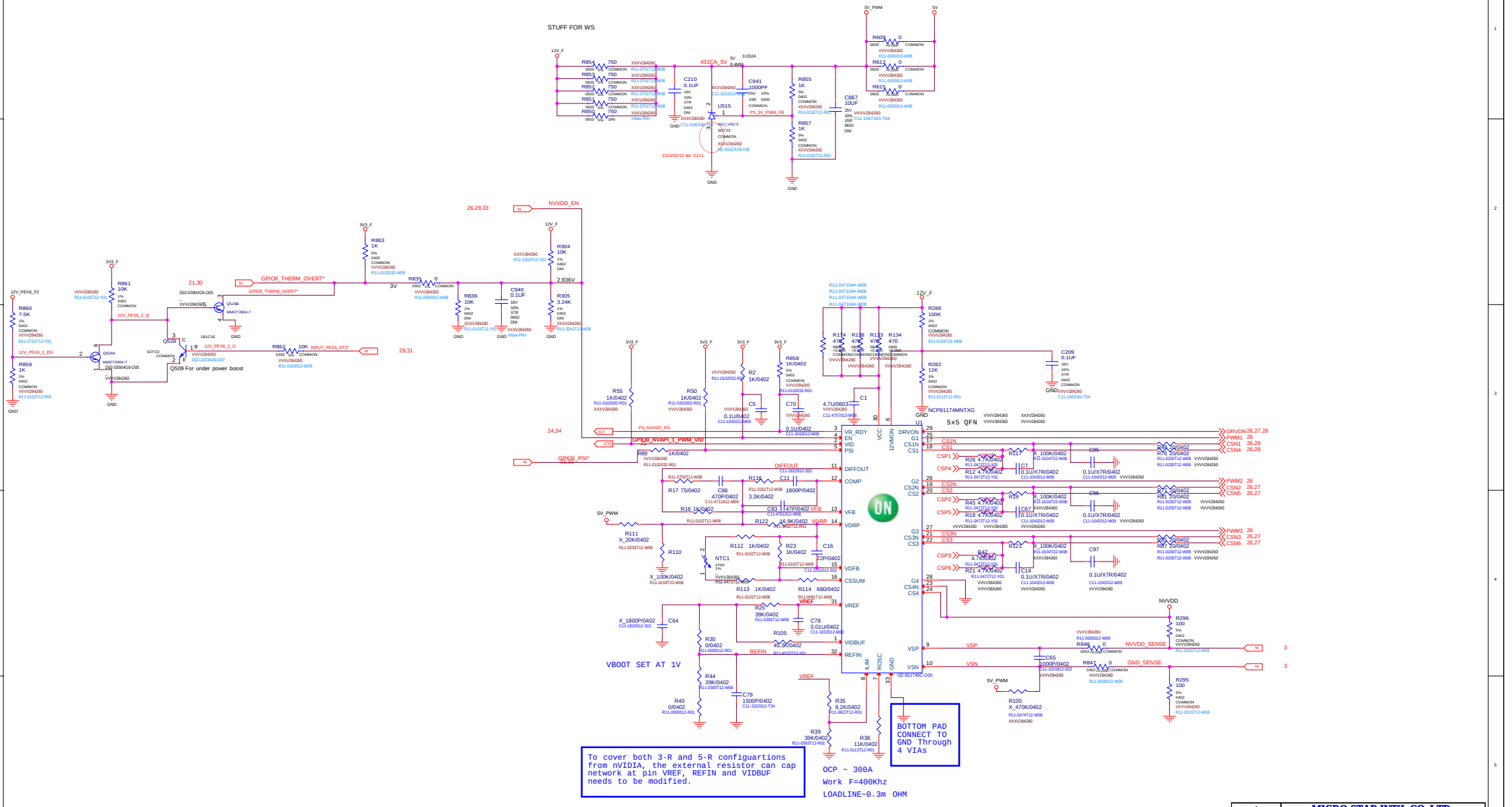
Page25: NVVDD Controller NCP81174



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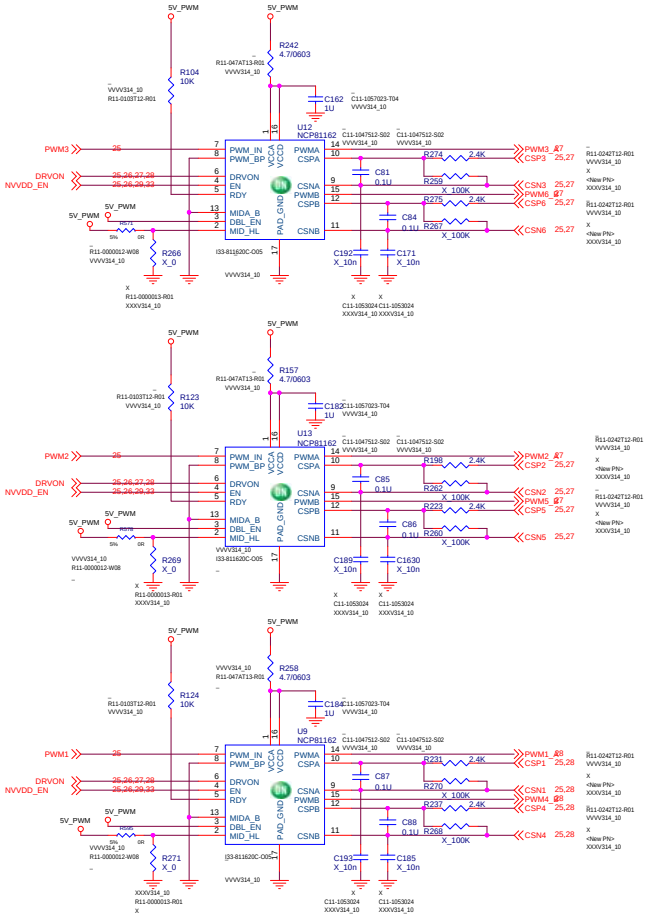
Page26: NVVDD PHASE DOUBLERS



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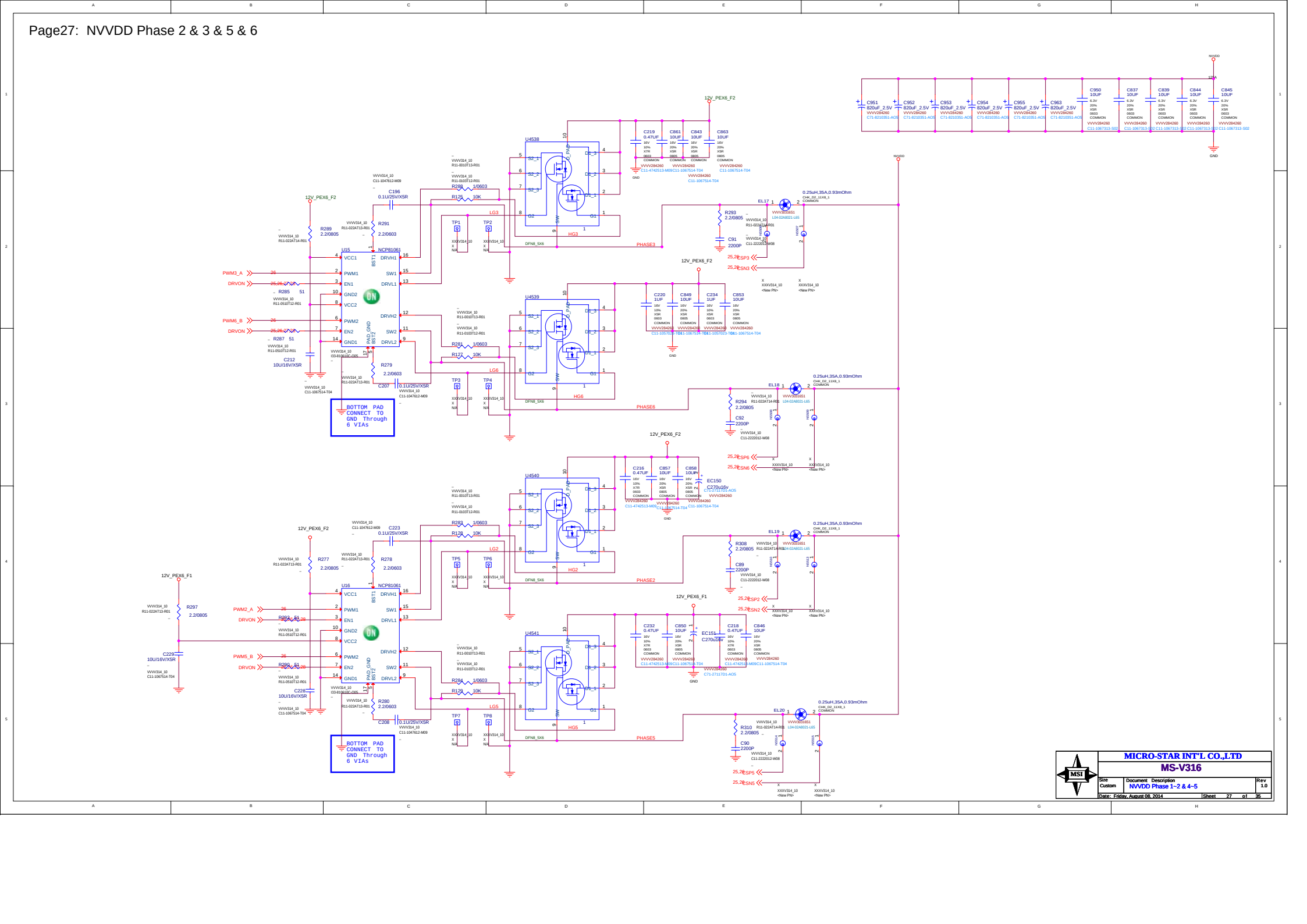
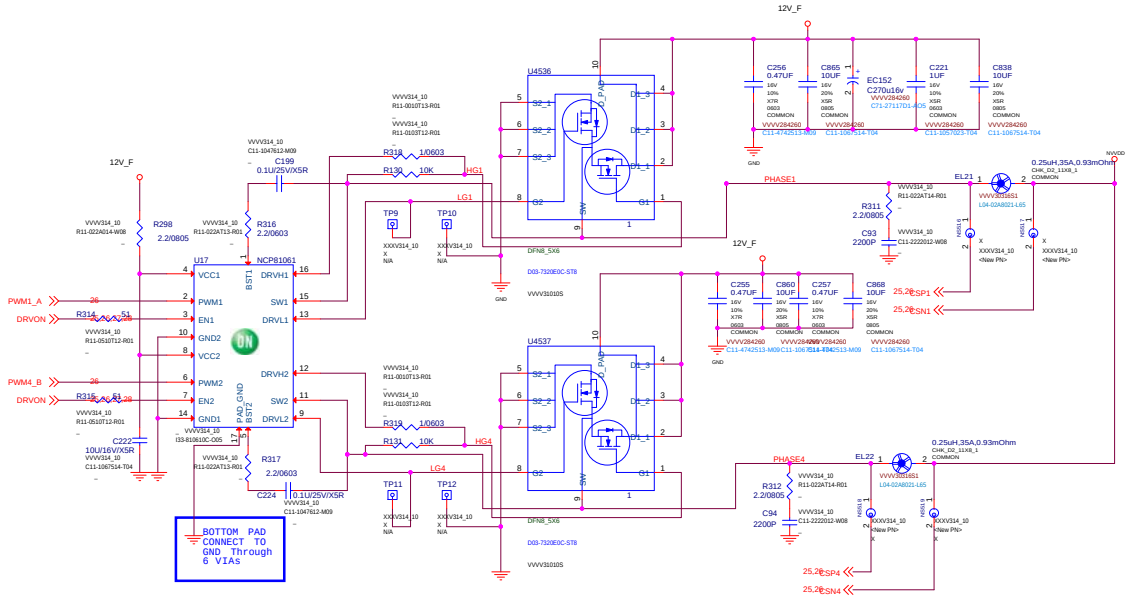
Page27: NVVDD Phase 2 & 3 & 5 & 6



Page28: NVVDD Phase 1 & 4



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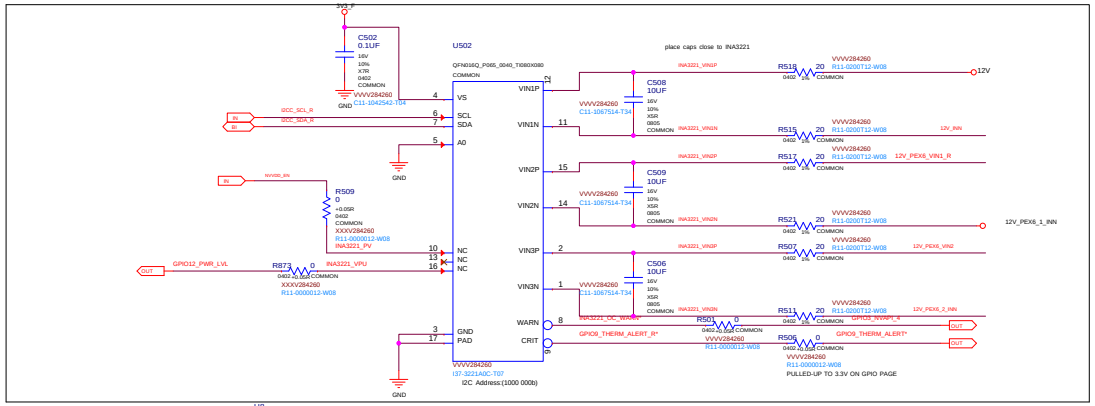
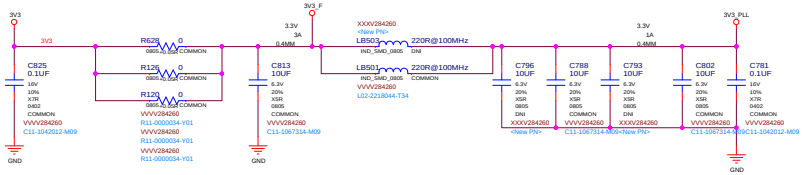
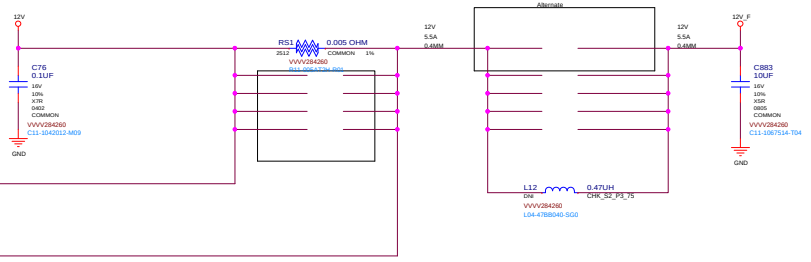
Page29: PS: Inputs, Filtering, and Monitoring



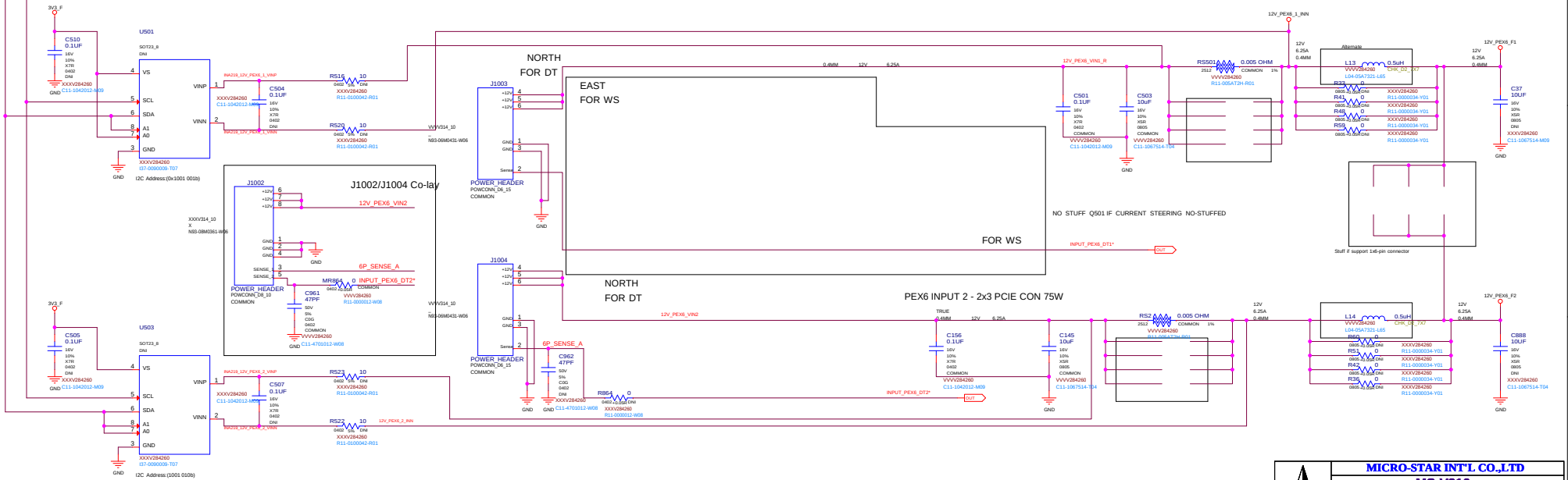
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX6 INPUT 2 - 2x3 PCIE CON 75W

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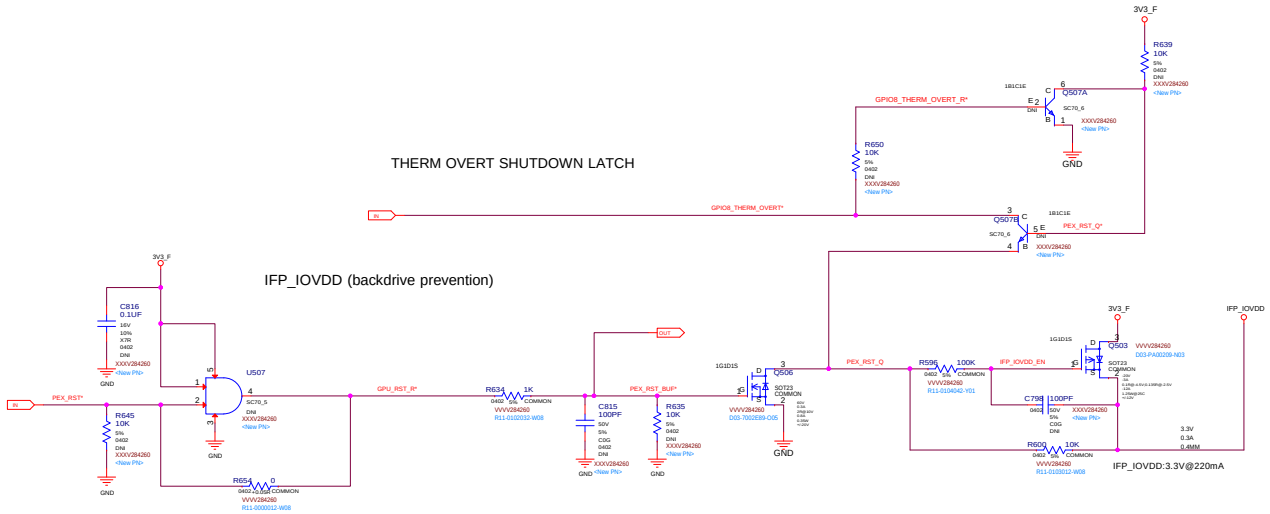
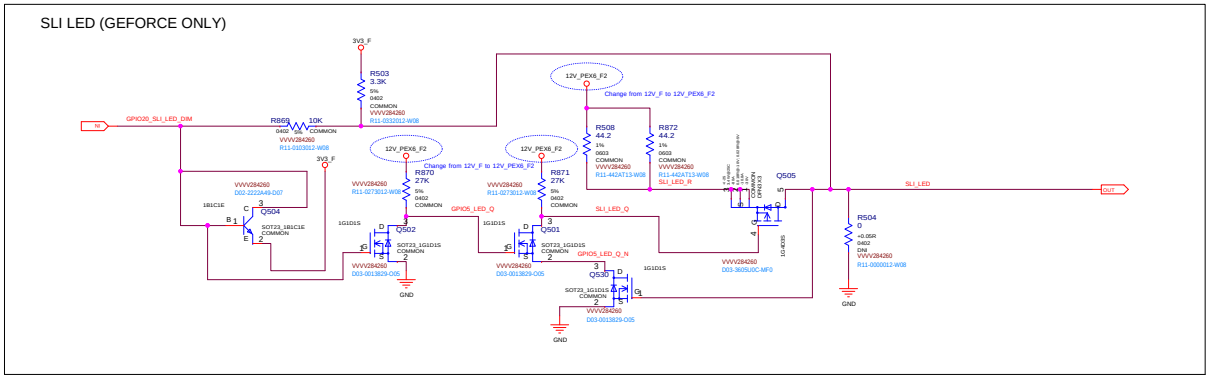
Page30: PS: Thermal Shutdown& Light SLI DRIVER





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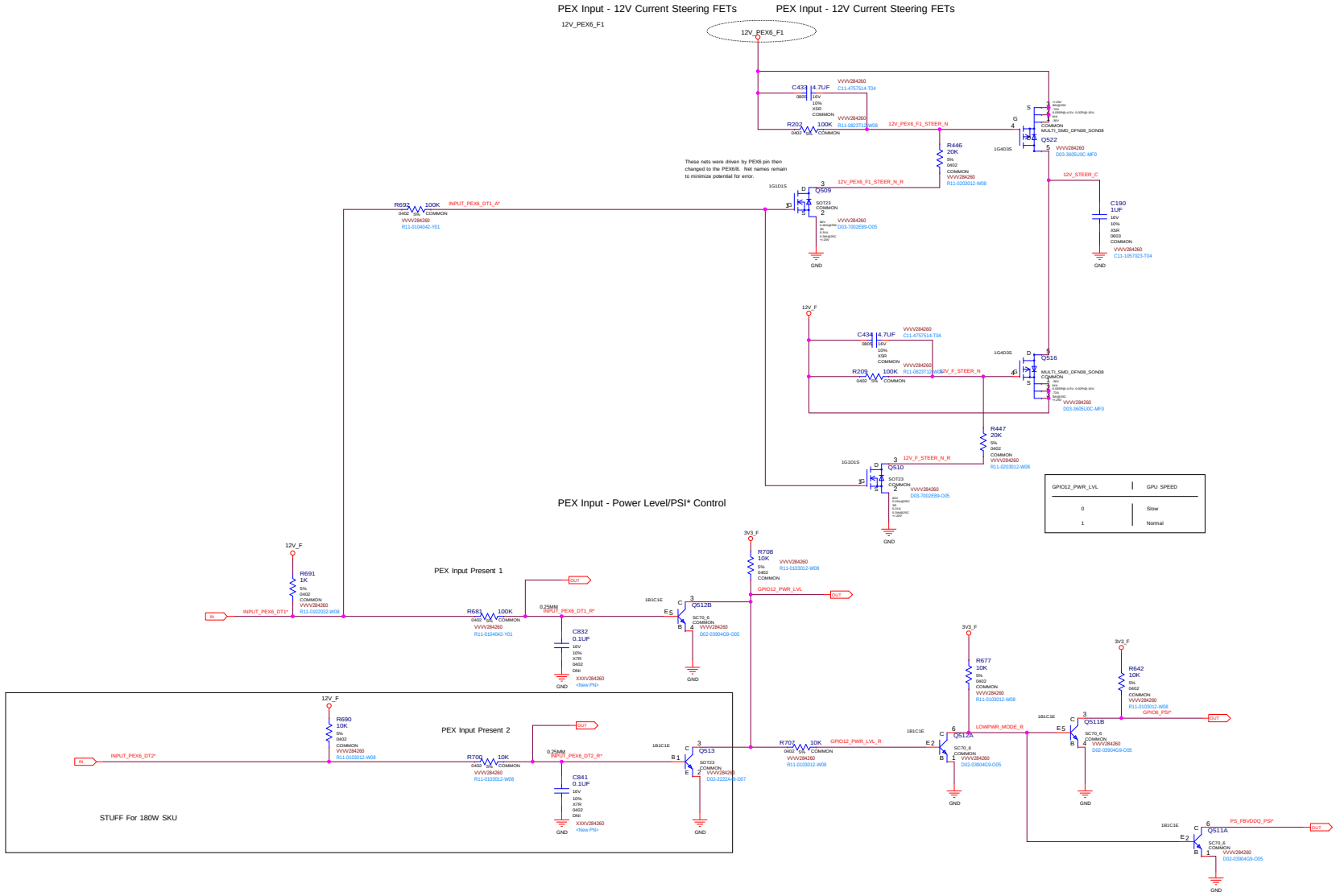
Page31: PS: 12V Current Steering



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Size: Custom	Document Description: PS: 12V Current Steering
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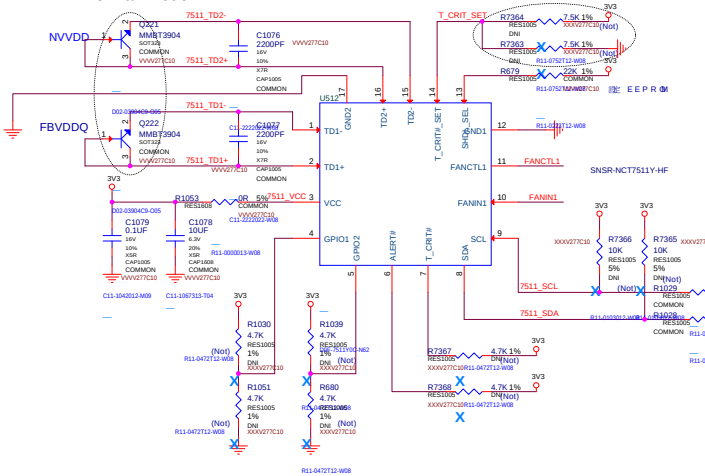
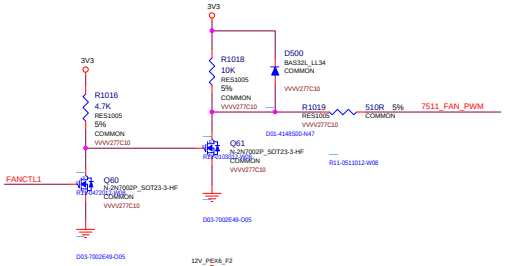
Thermal IC : NCT7511Y

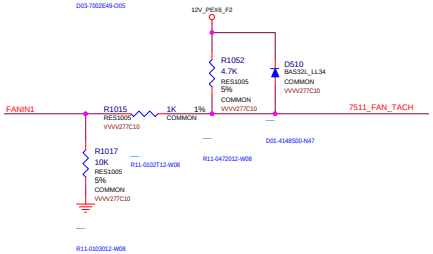
Layout notice :
*Add ground shielding for D+ and Dtraces.
*D+/D- route has to be away from the high noise area.
*The recommended traces width and ground shielding spacing are 10mils.

Please refer datasheet
TCRIT_SET Table
If floating,shutdown temp. set to 65℃

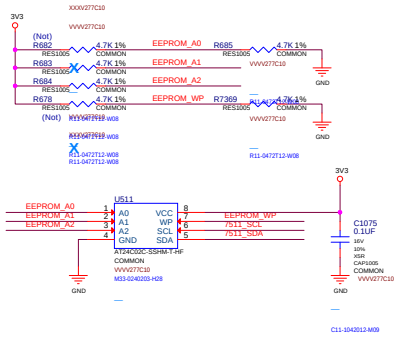
Thermal Diode



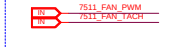




EEPROM



Fan connector option



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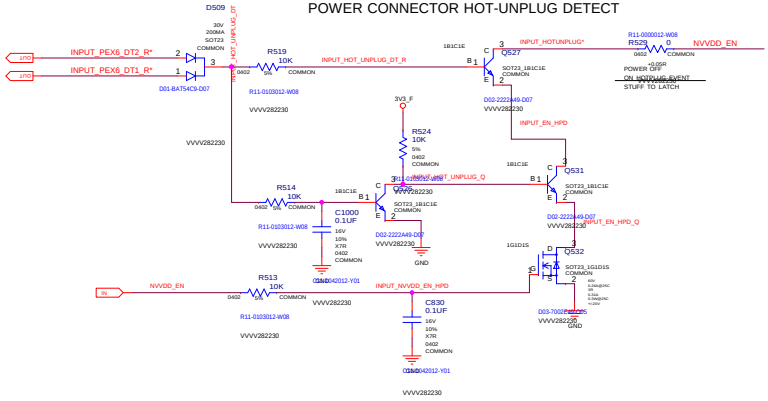
Page33: Power Connector Hot unplug

PEX Input - NVVDD Power Sequence

CURRENT STEERING

POWER CONNECTOR HPD

POWER CONNECTOR HOT-UNPLUG DETECT



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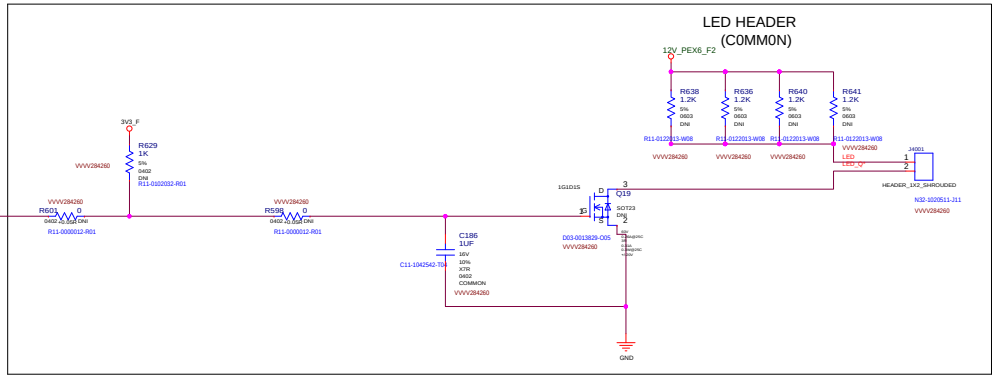
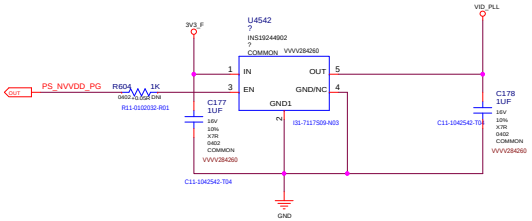
GeForce Logo LED





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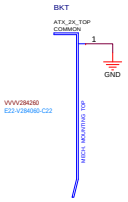
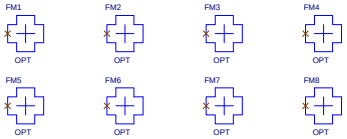
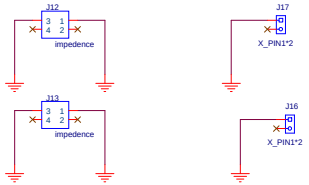
Brackets:



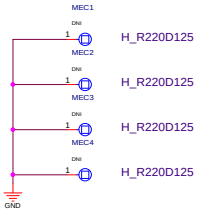
optical cross point



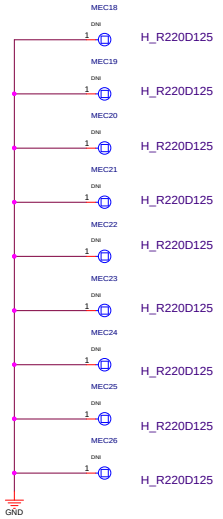
Top & bottom each layer set 4 points



GPU Stiffener:



MOUNTING HOLES FOR HS:



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