PG401 A02

4GB GDDR5, 256b, 128Mx32

Tall DVI-I + DP + DP + DP/HDMI + DP

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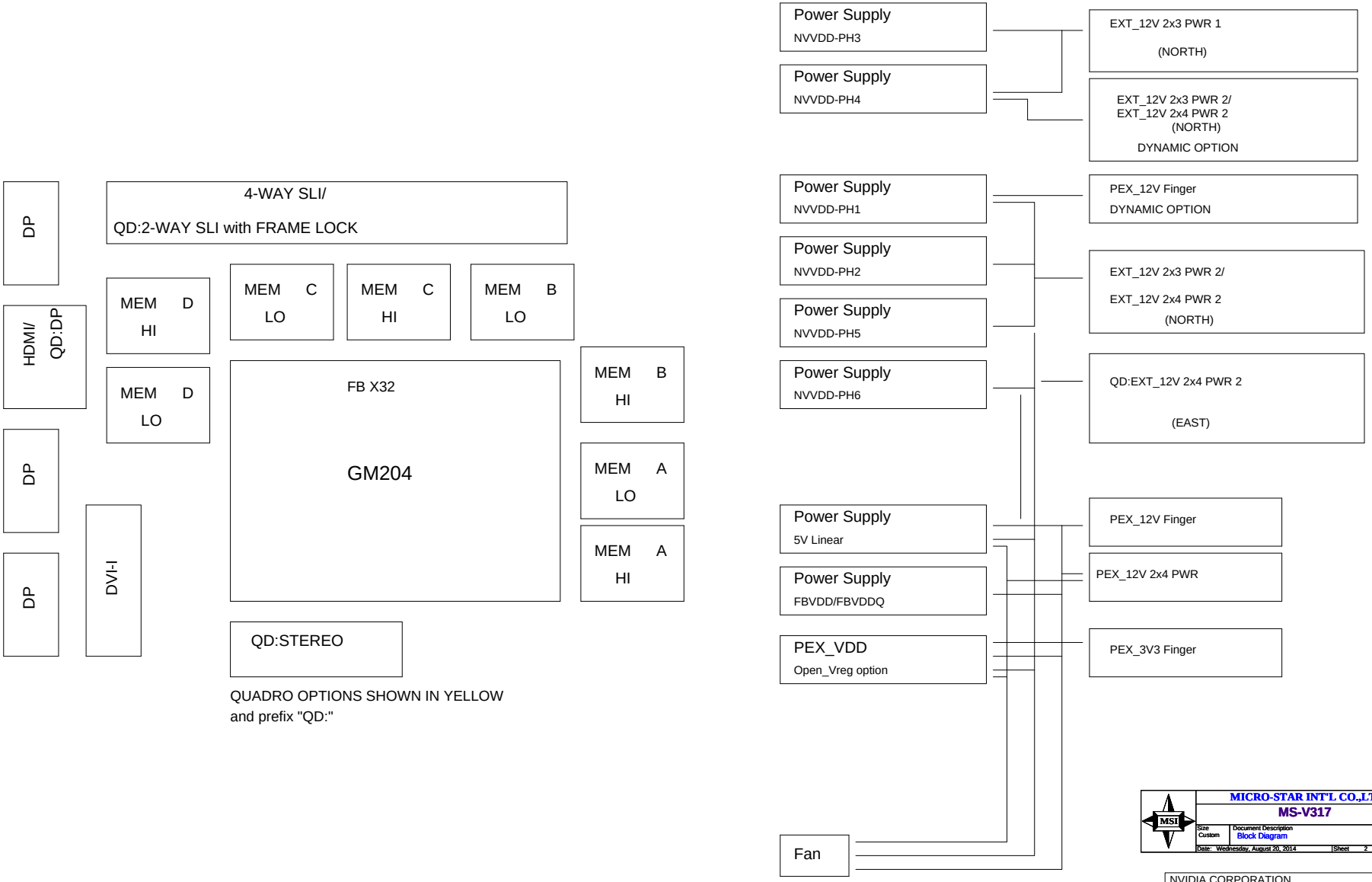
Page2: Block Diagram



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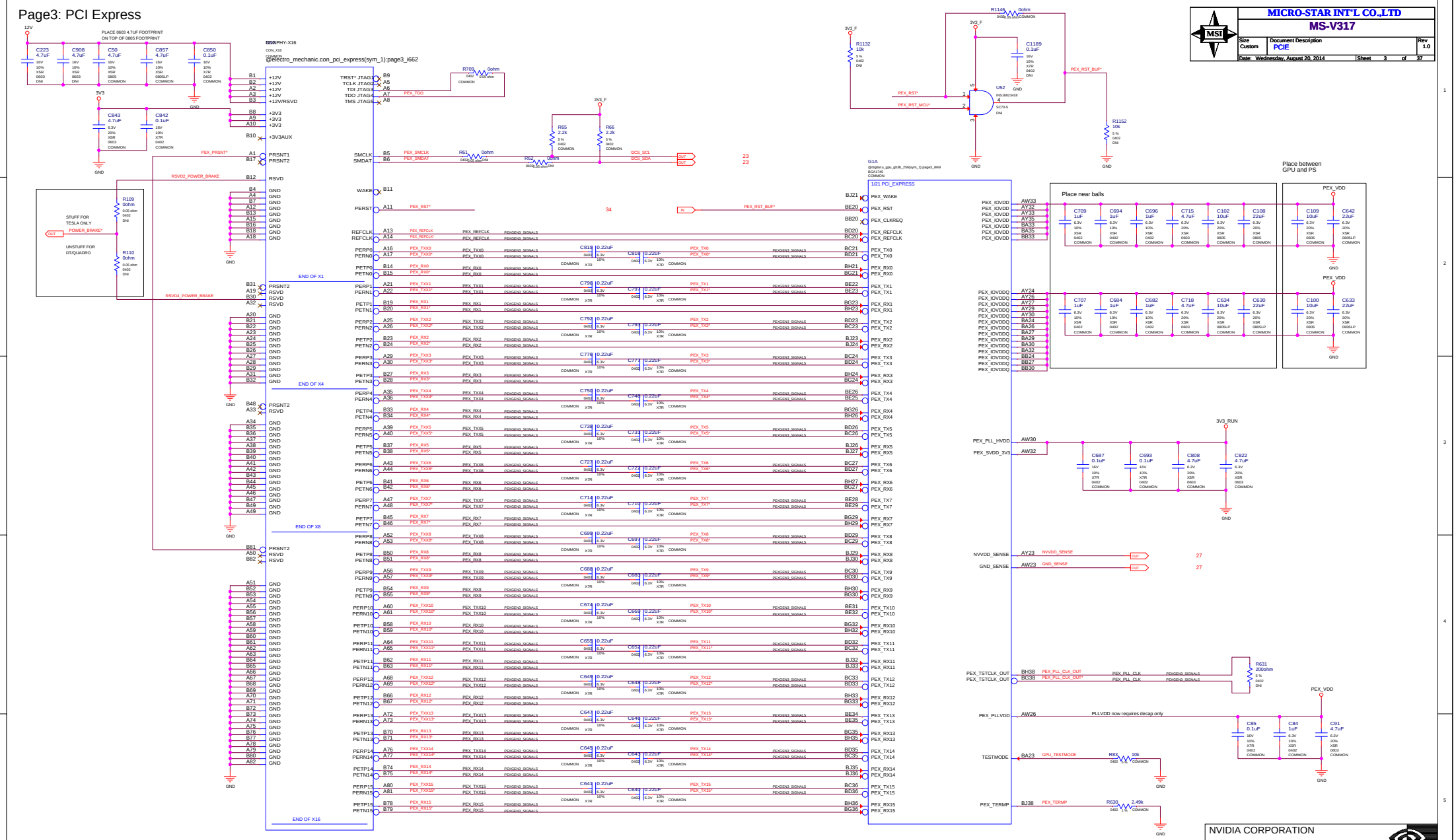

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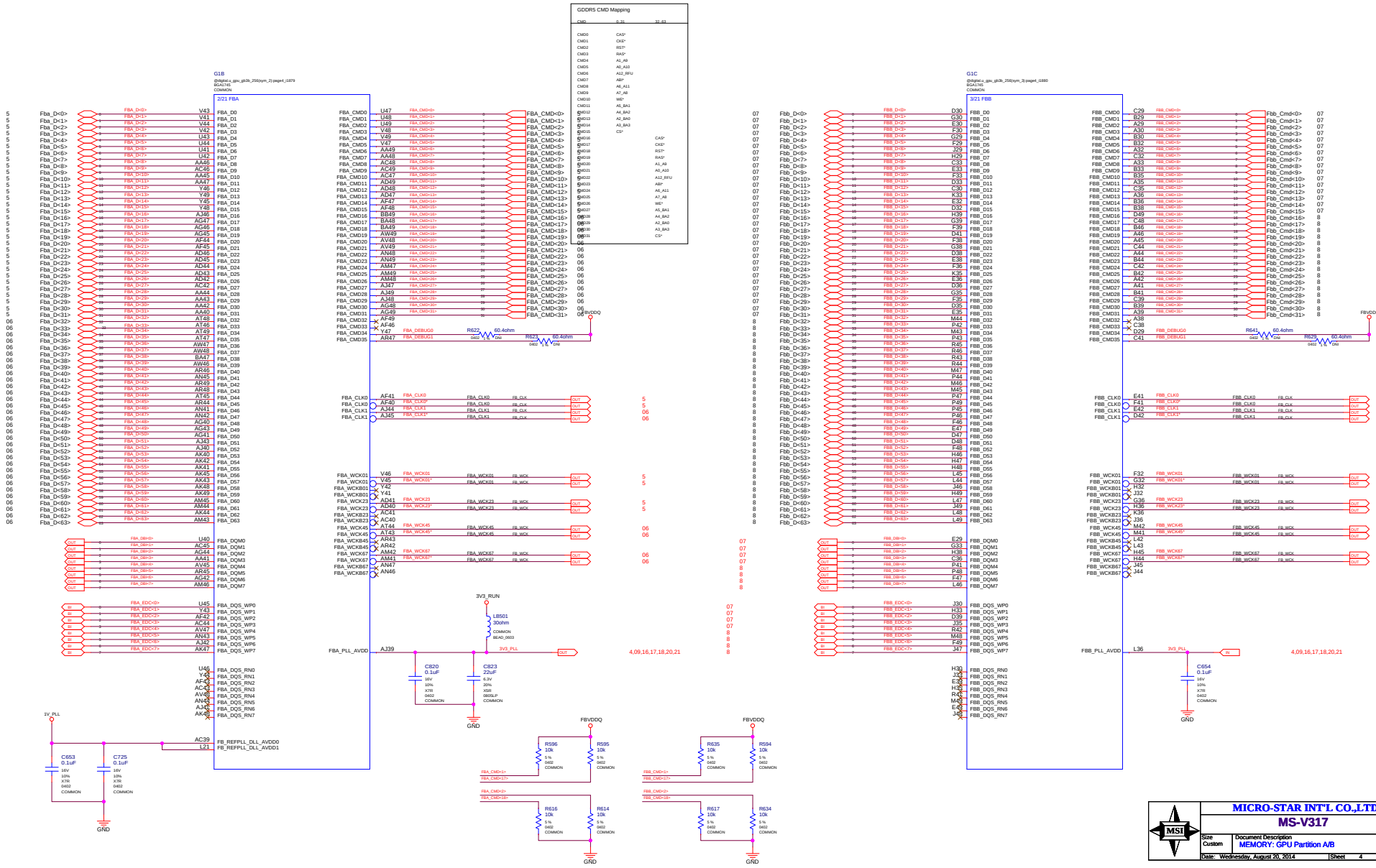

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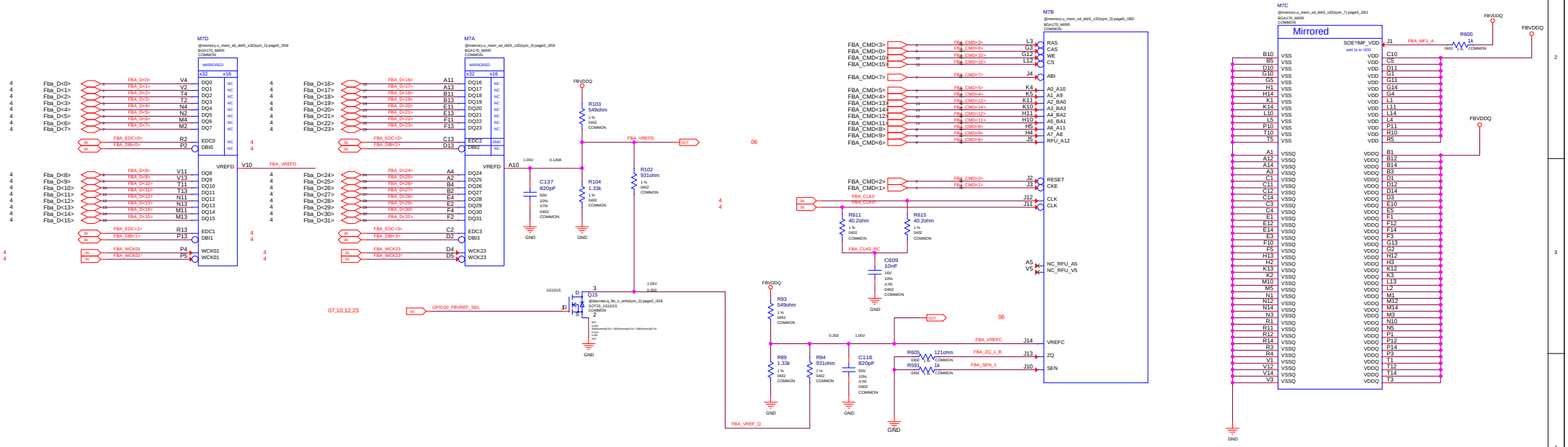

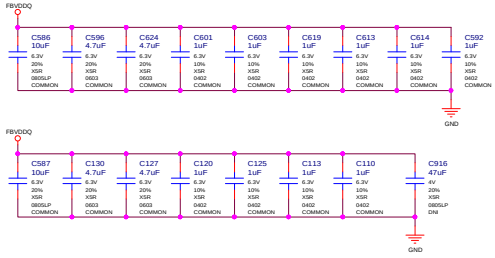

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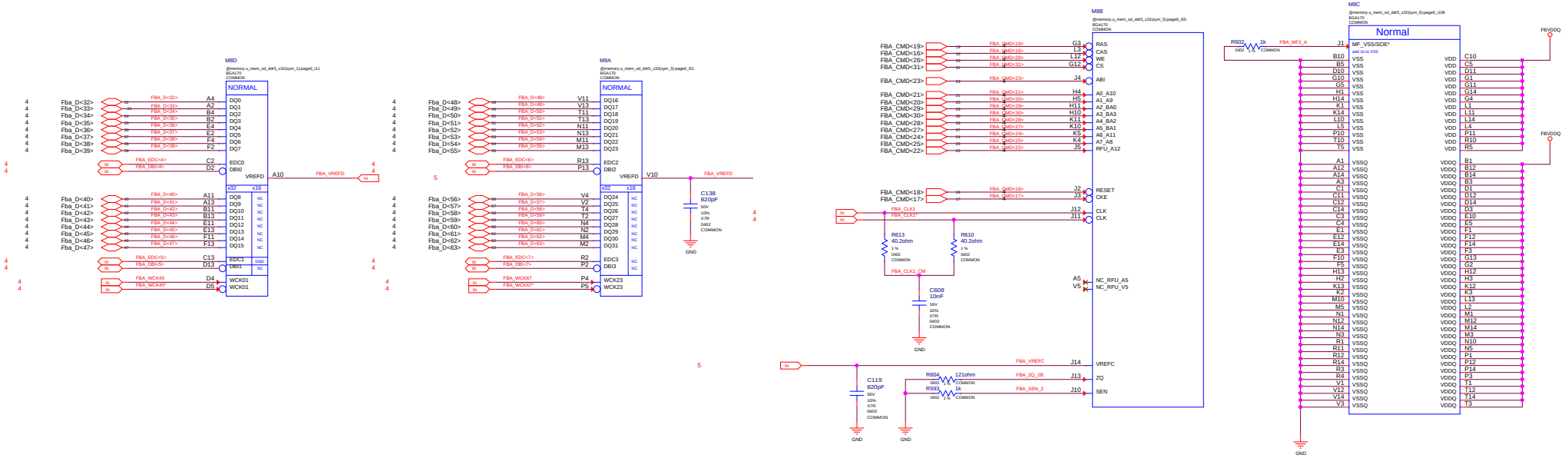

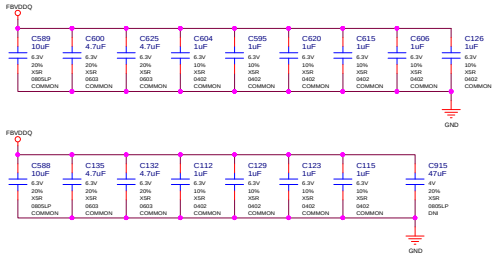

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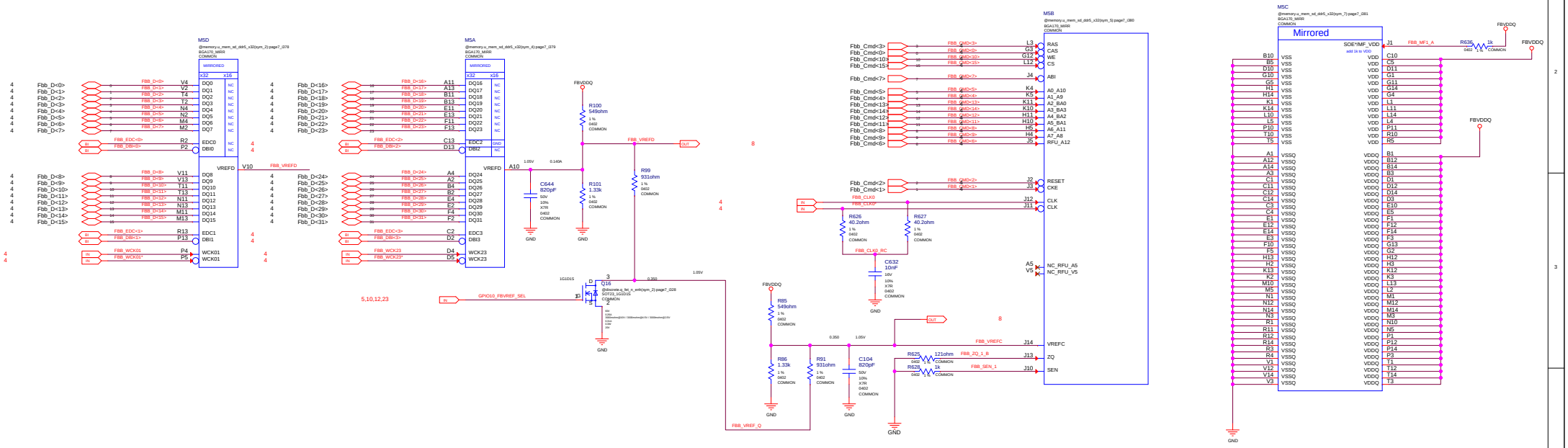

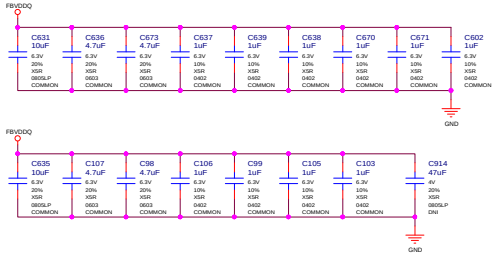

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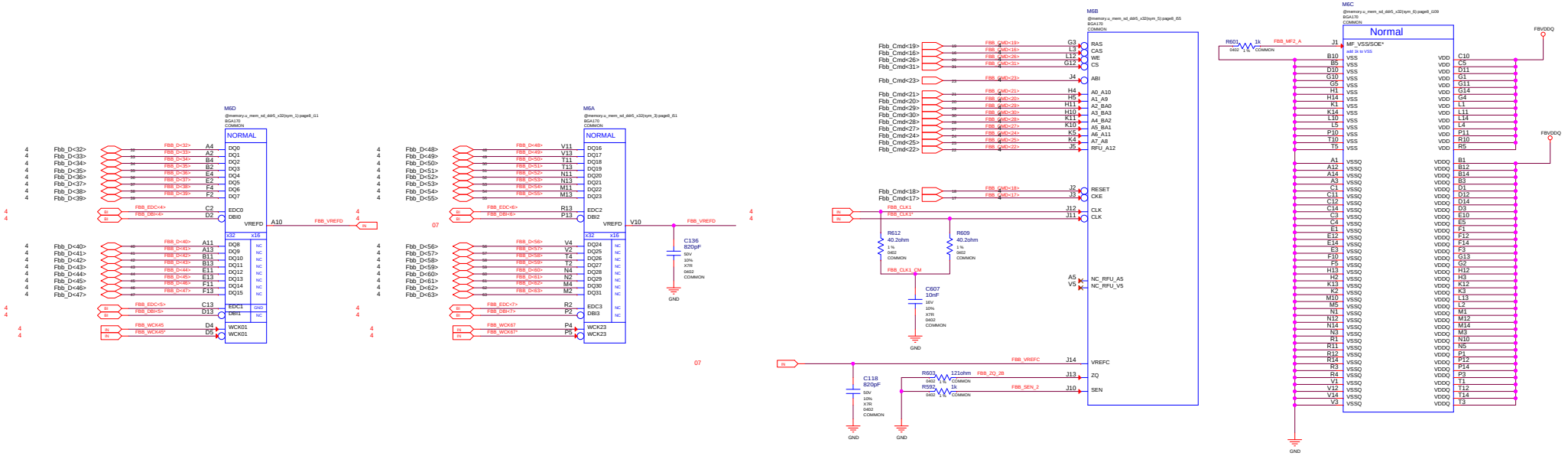

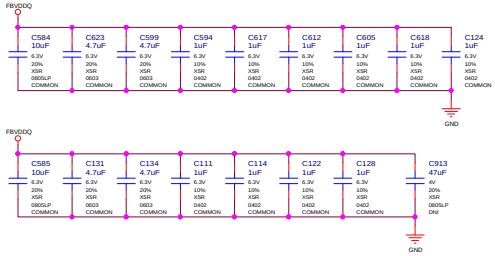

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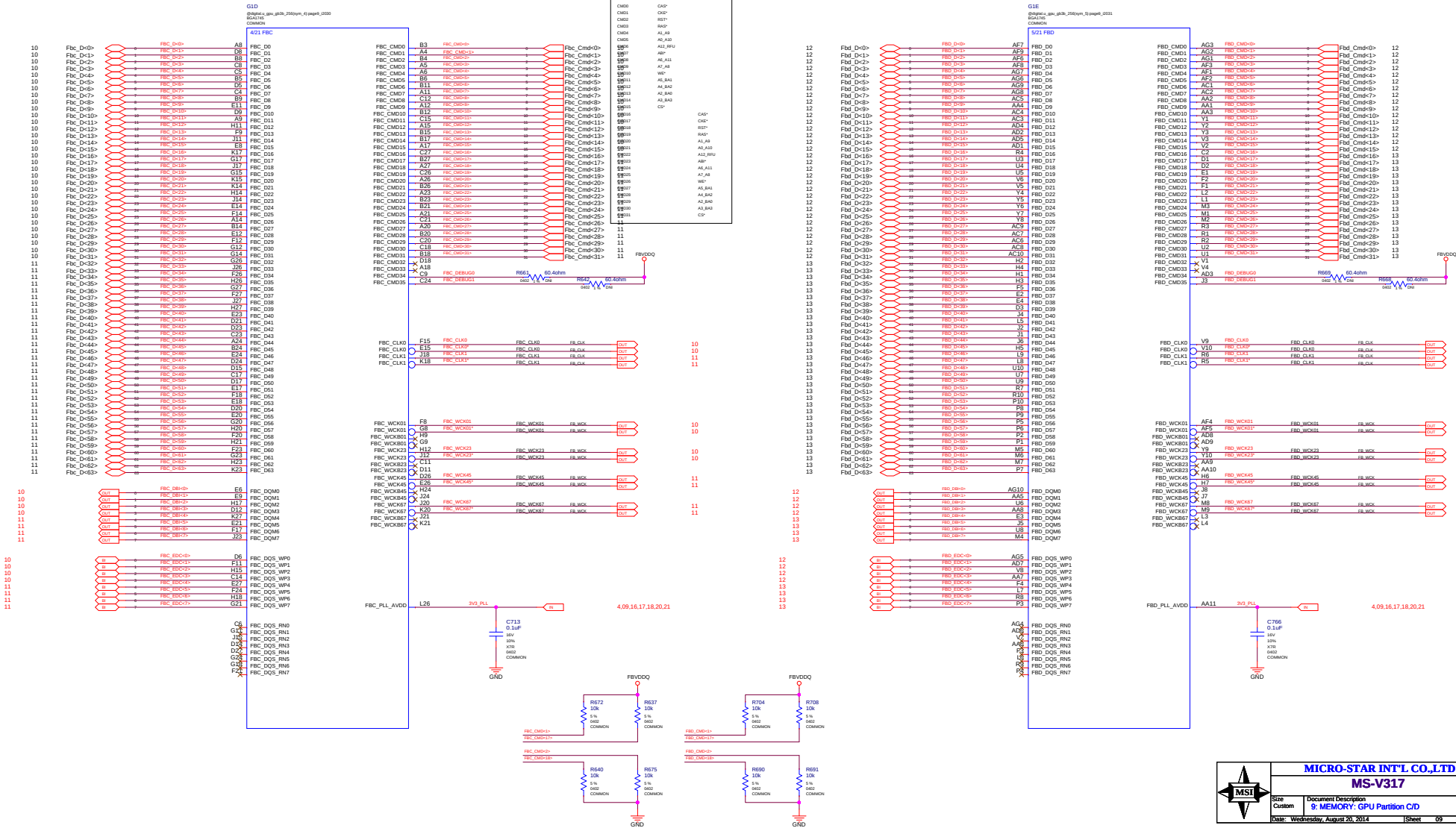

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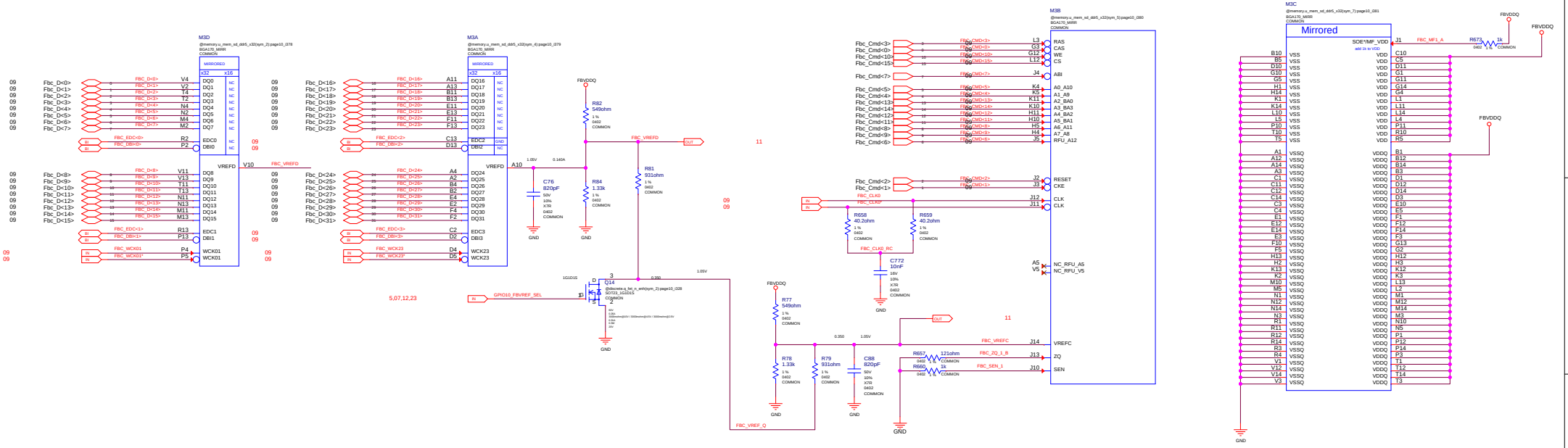

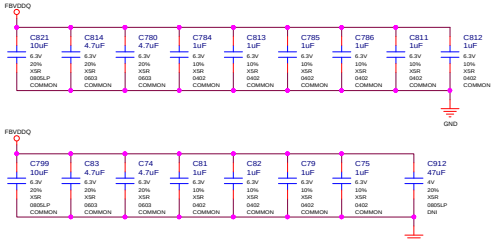

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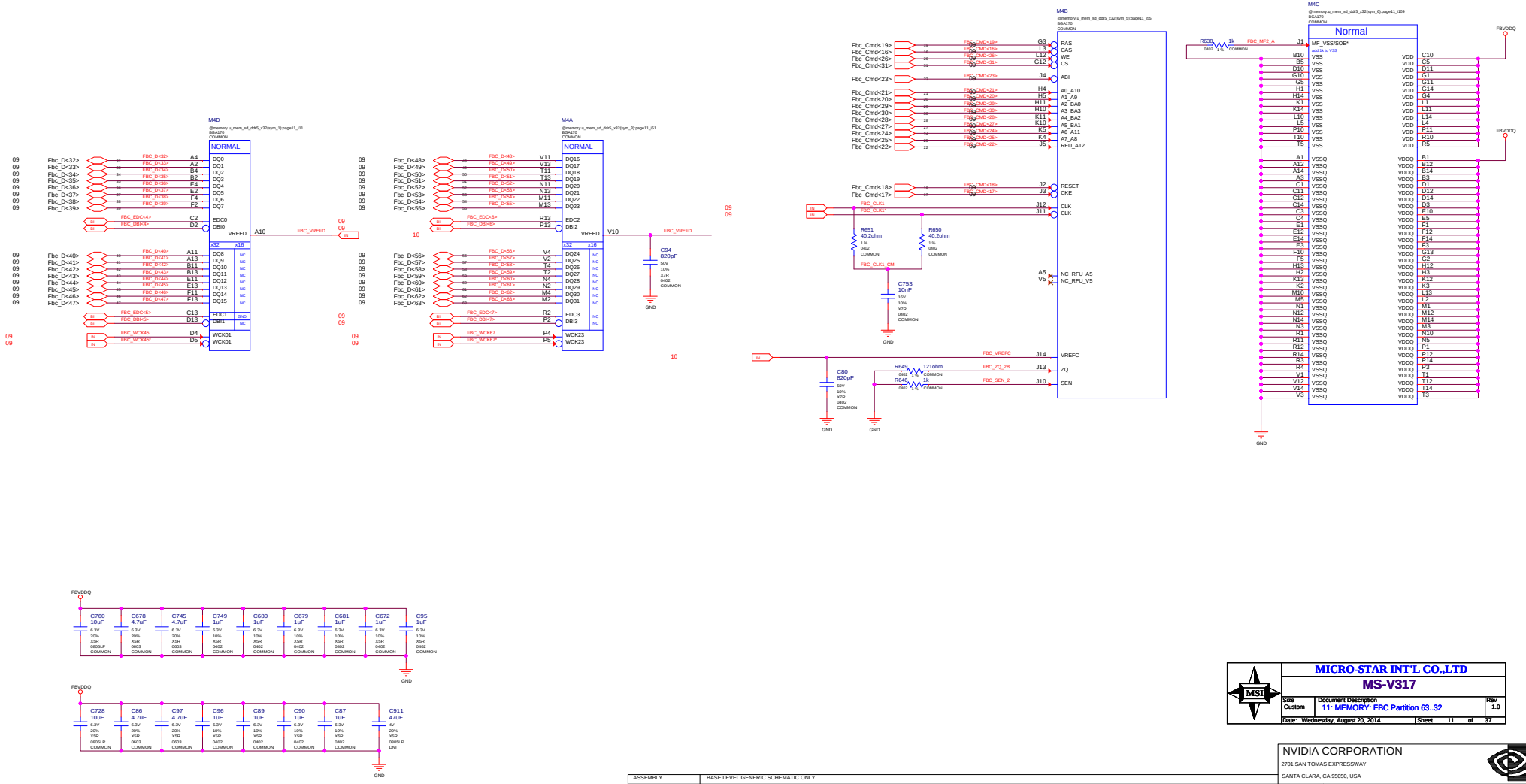

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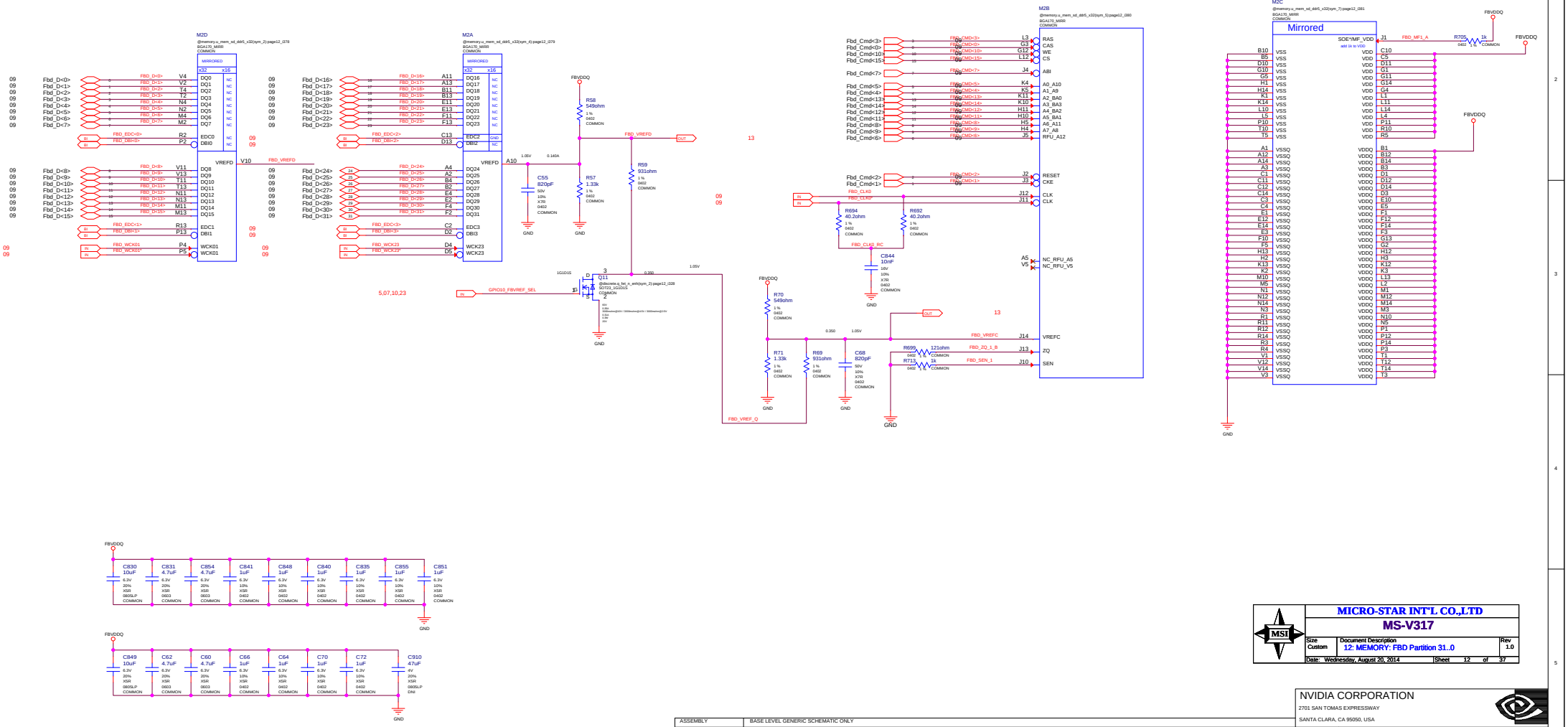

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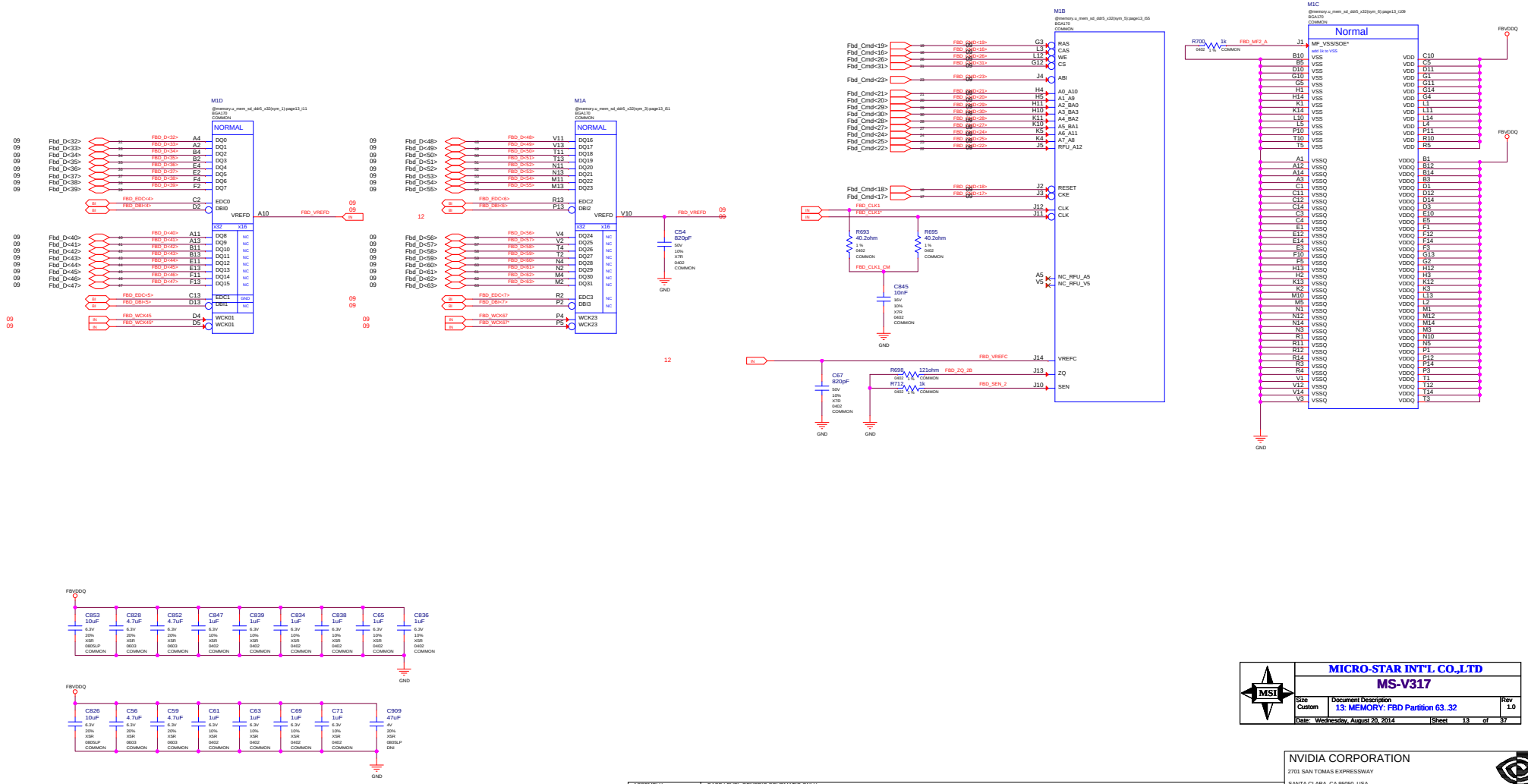

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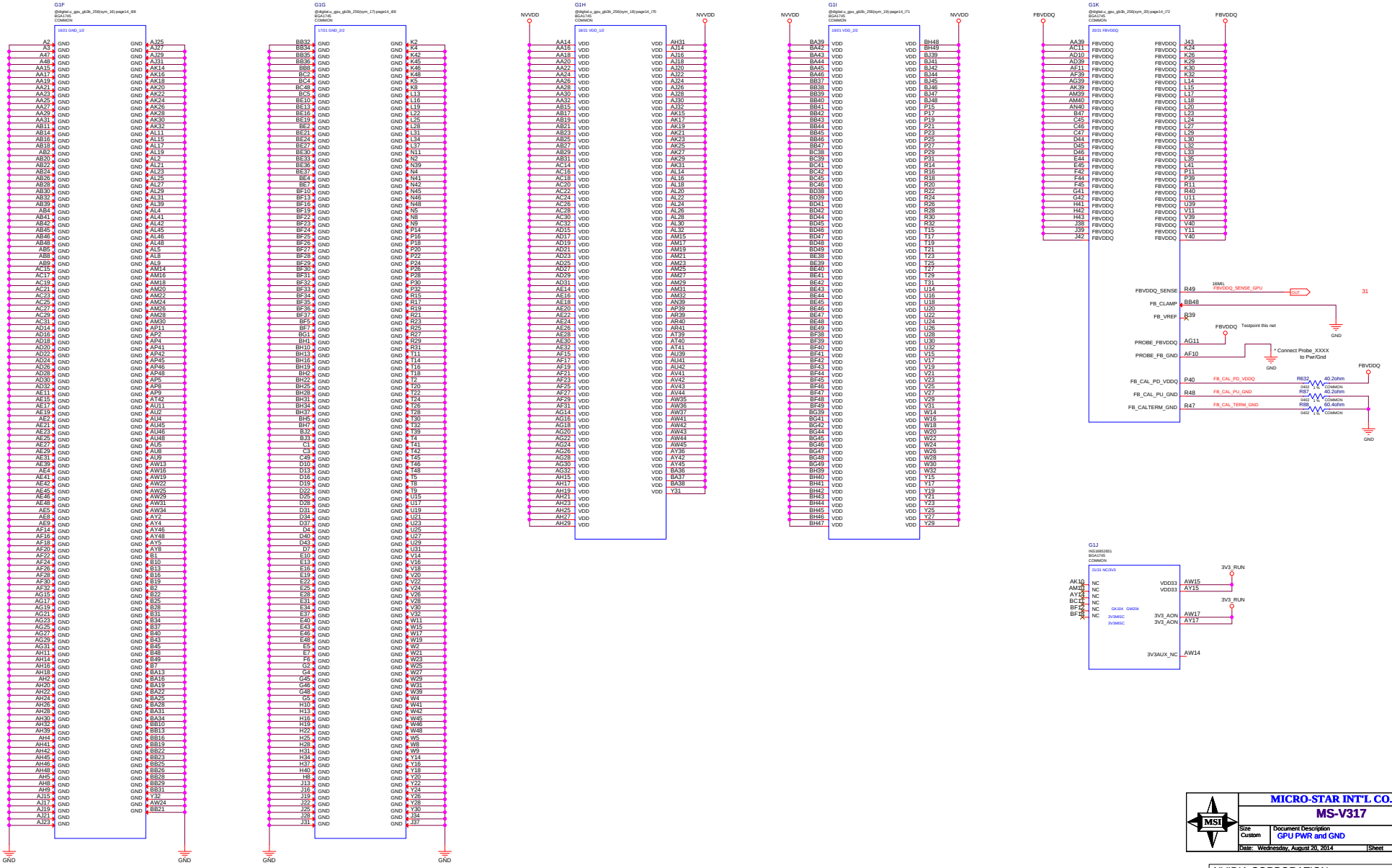

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPU PWR and GND

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Page15: GPU Decoupling

Based on GB2-X GDDR5 FBVDDQ Decap Guideline

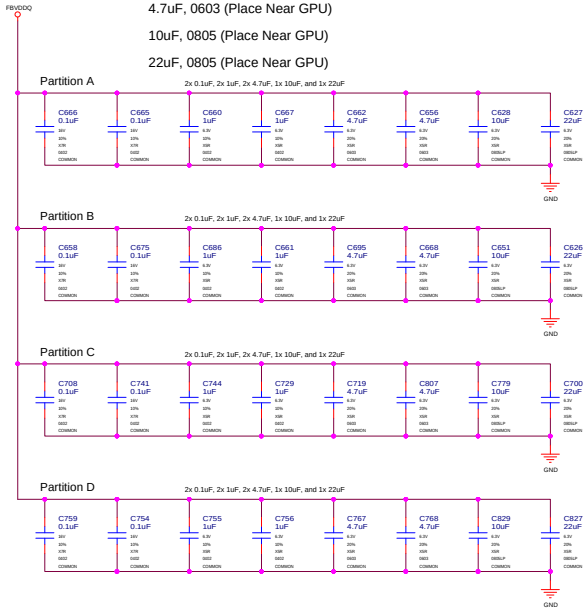
FBVDDQ

0.1uF, 0.47uF & 1uF, 0402 (Place Under GPU)

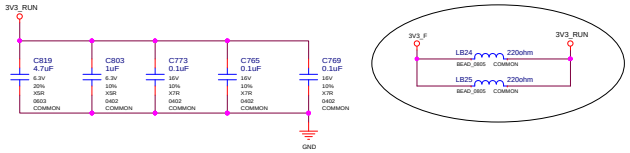
4.7uF, 0603 (Place Near GPU)

10uF, 0805 (Place Near GPU)

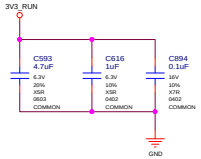
22uF, 0805 (Place Near GPU)



VDD33

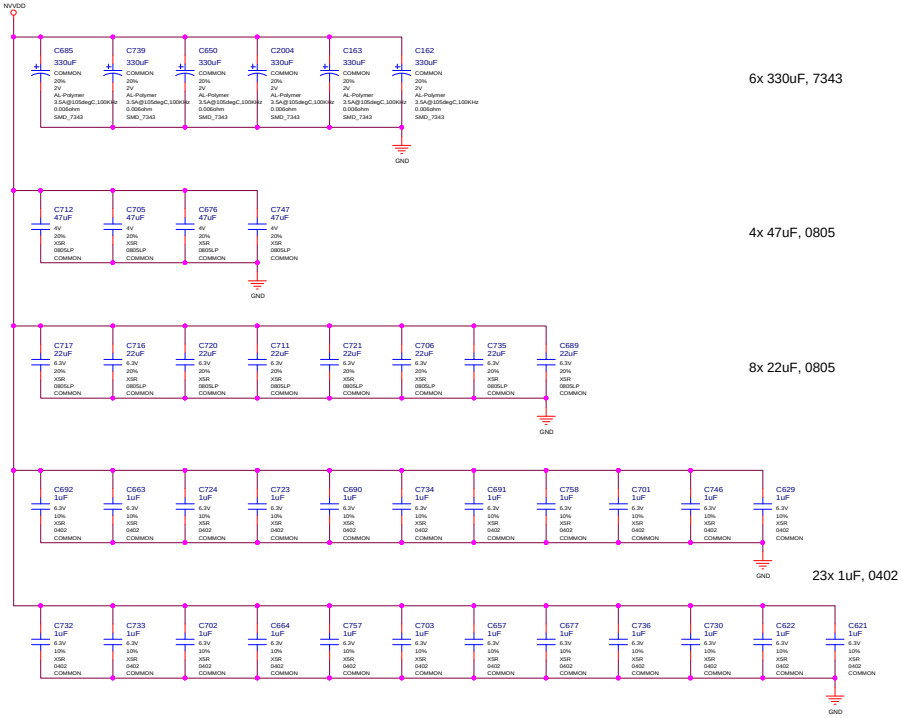


3V3_AON



NVVDD Decoupling caps. Place under GPU.

NVVDD



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPU Decoupling

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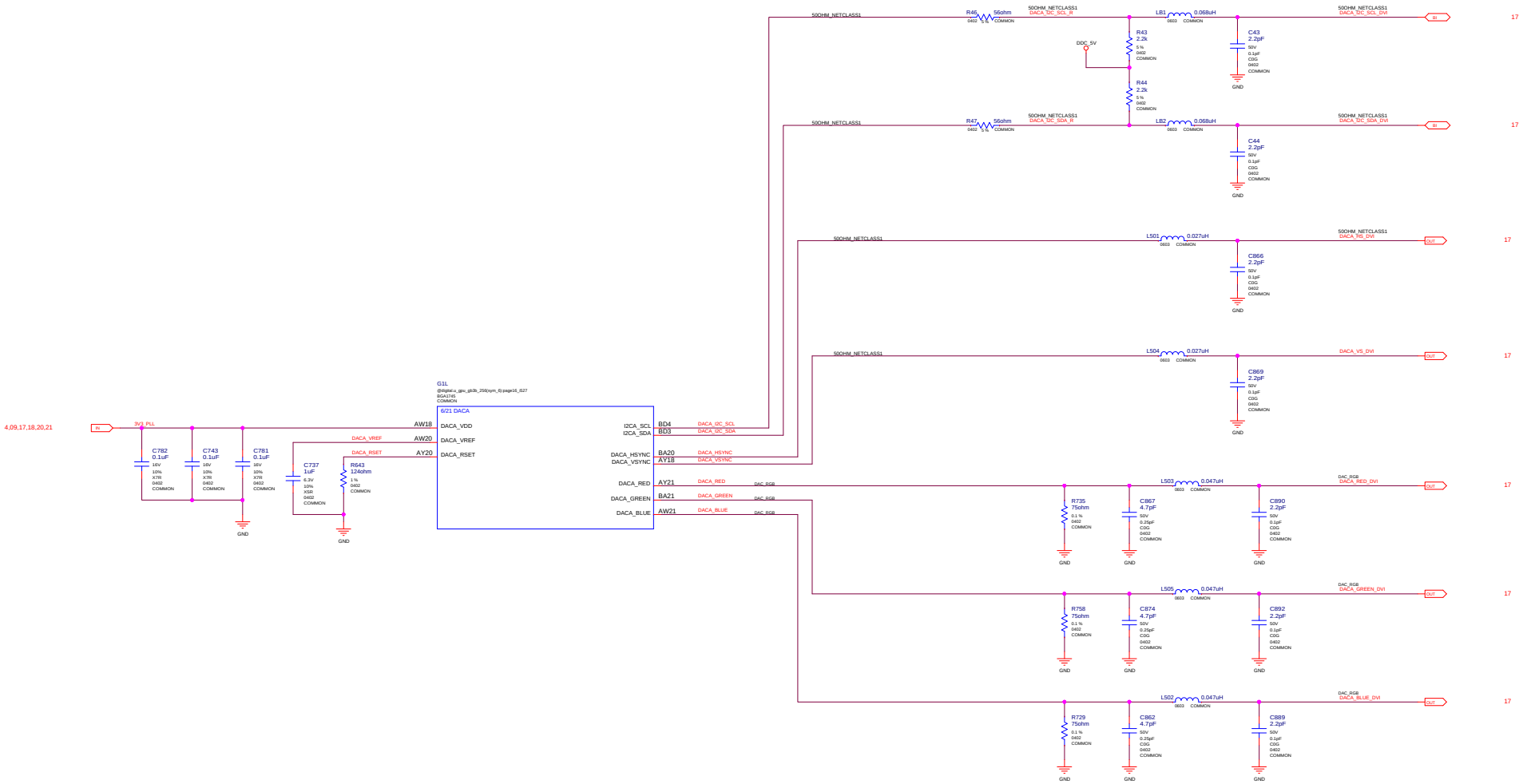
Page16: DACA Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	DACA Interface

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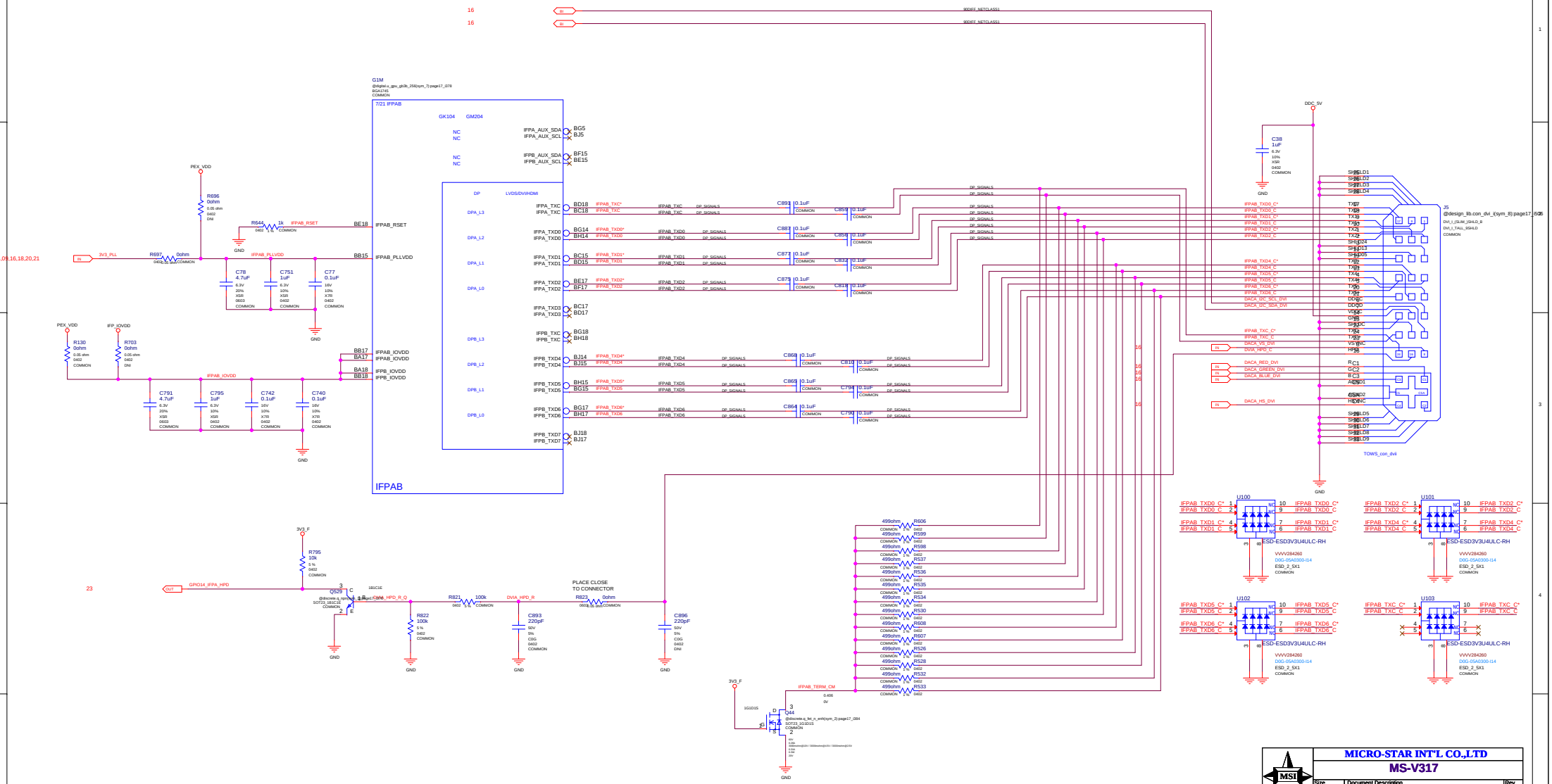
Page17: IFPAB DVI-I-DL



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPAB DVI-I-DL

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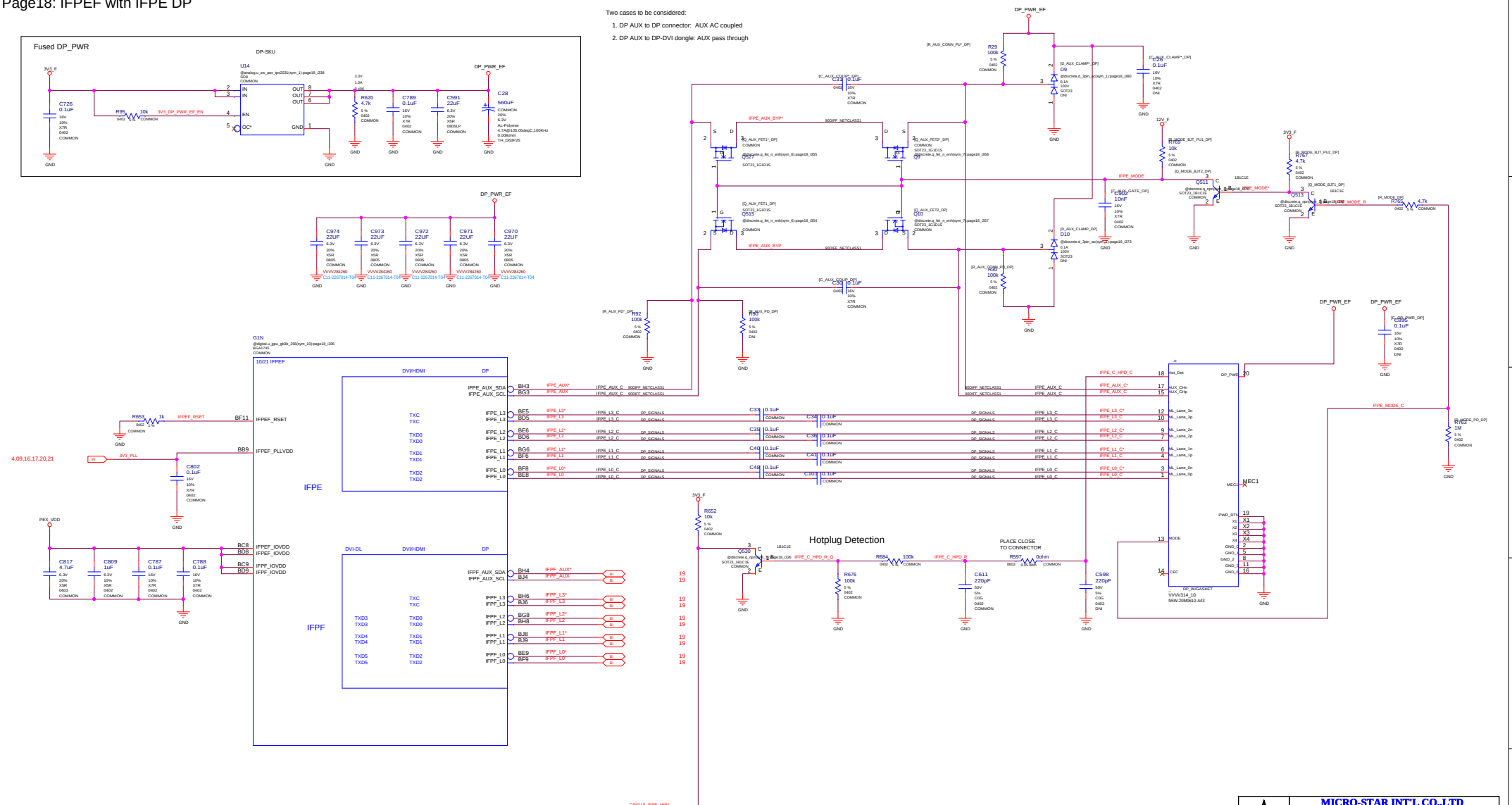
Page18: IFPEF with IFPE DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPEF with IFPE DP

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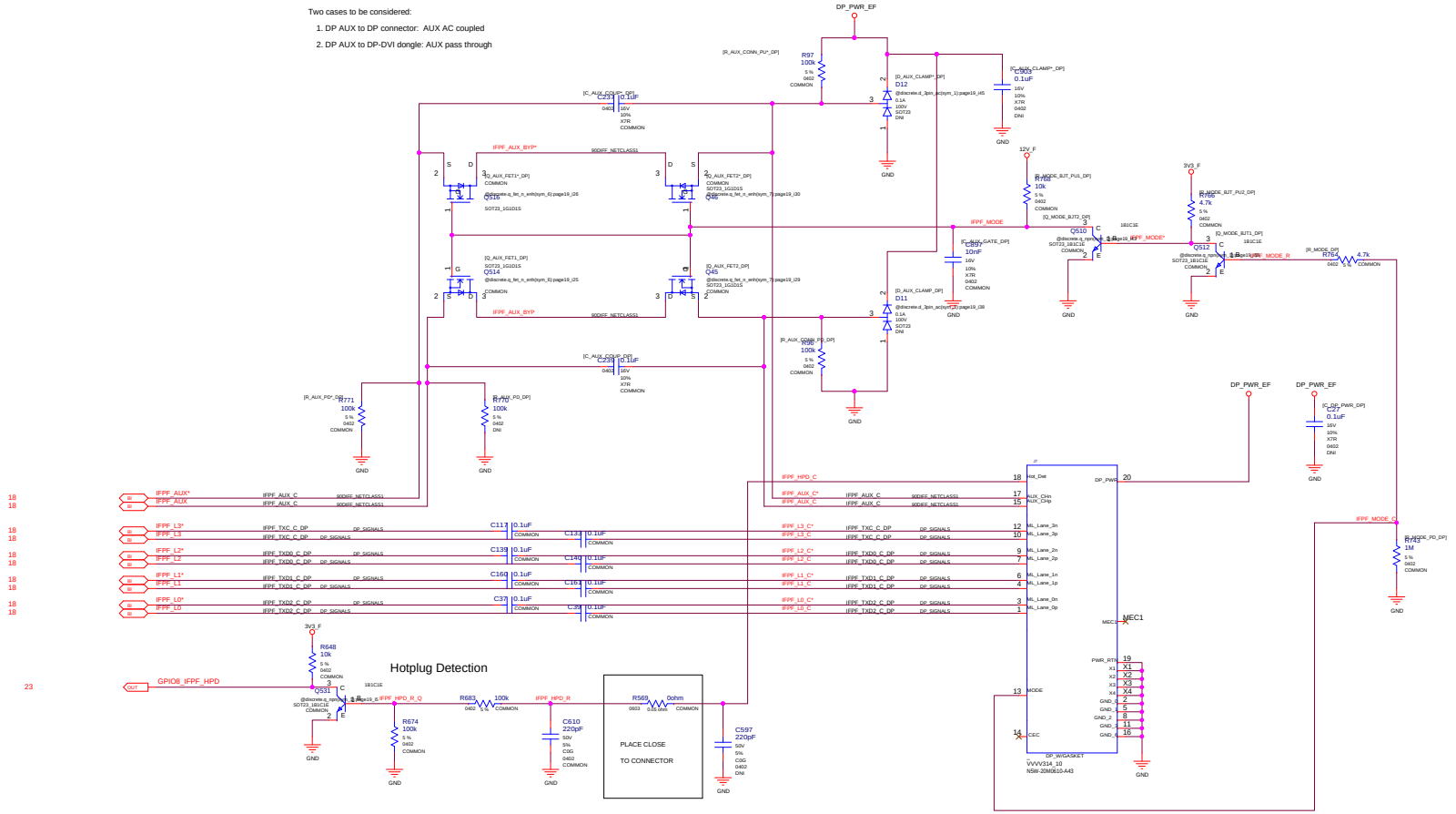
Page19: IFPF DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPF DP

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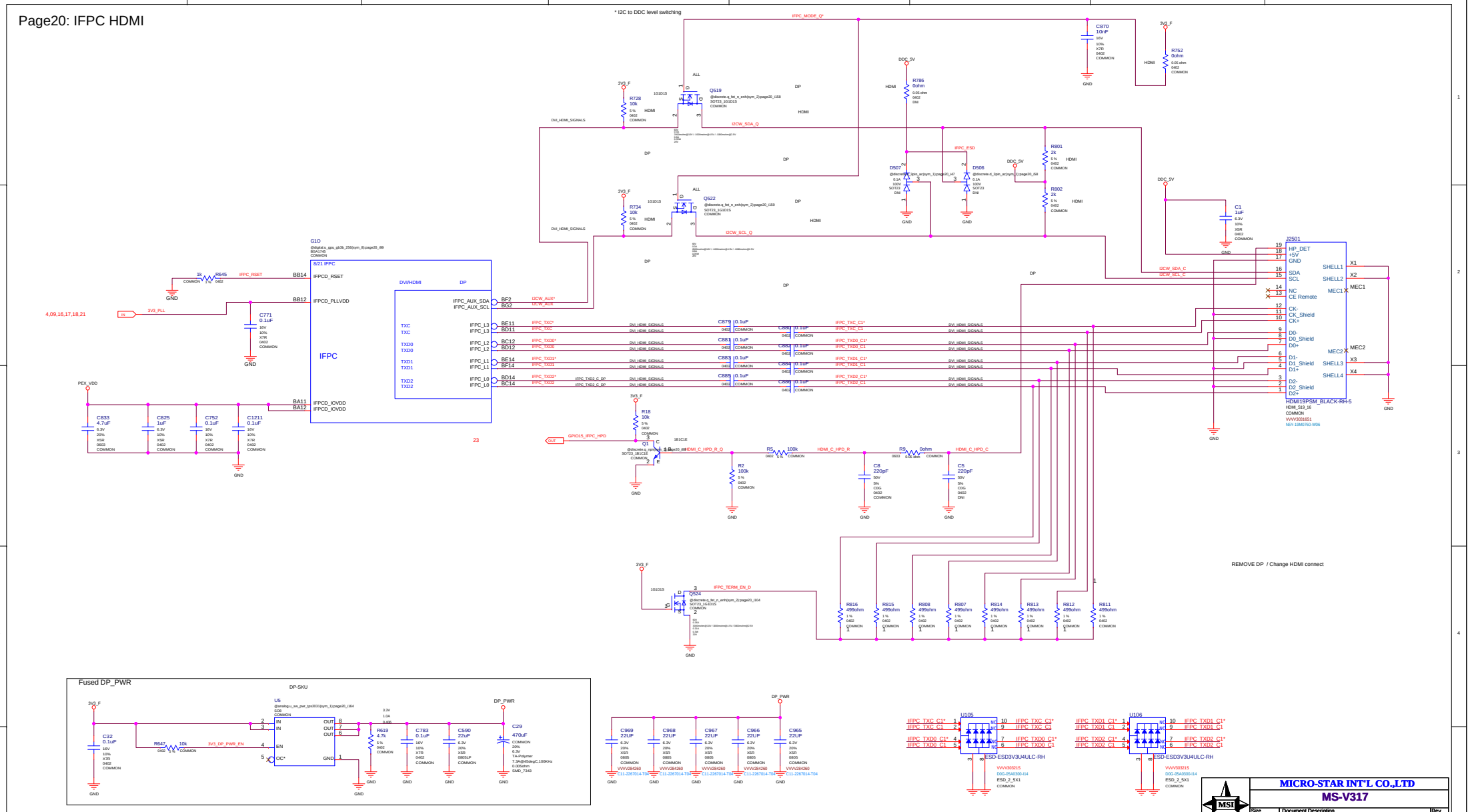
Page20: IFPC HDMI



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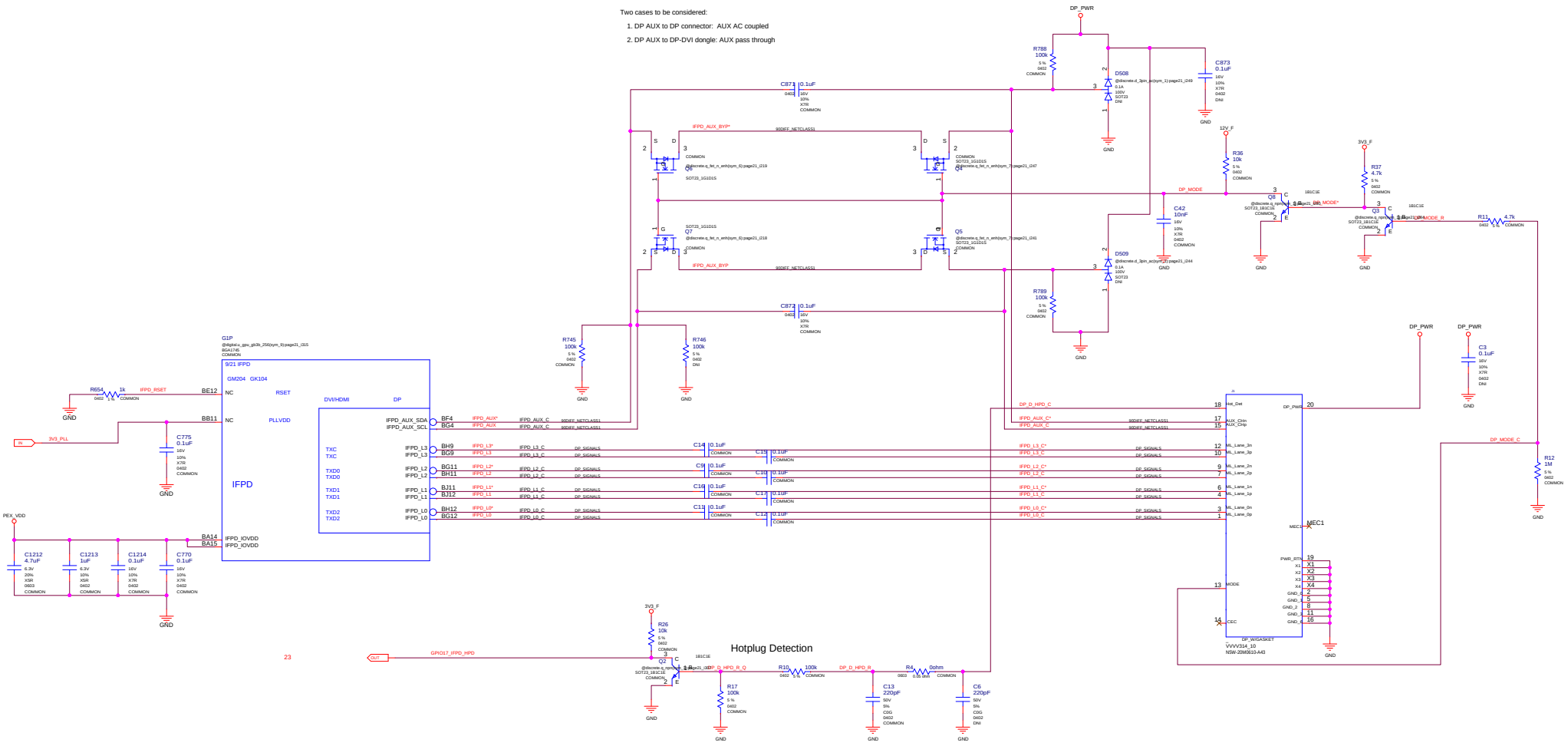
Page21: IFPD DP



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPD DP

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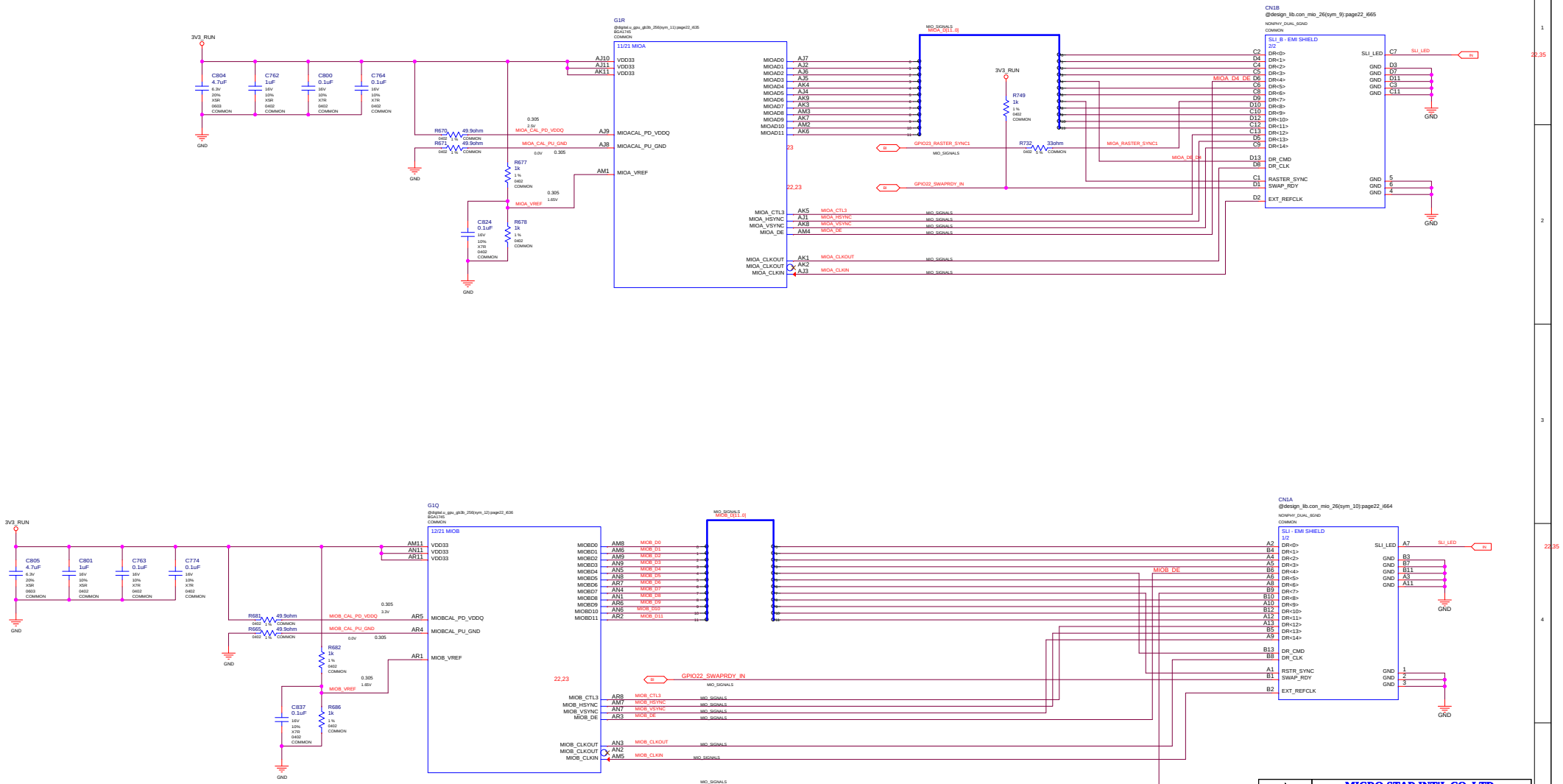
Page22: MIOA/B Interface and FRAME LOCK



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MIOA/B Interface and Frame Lock

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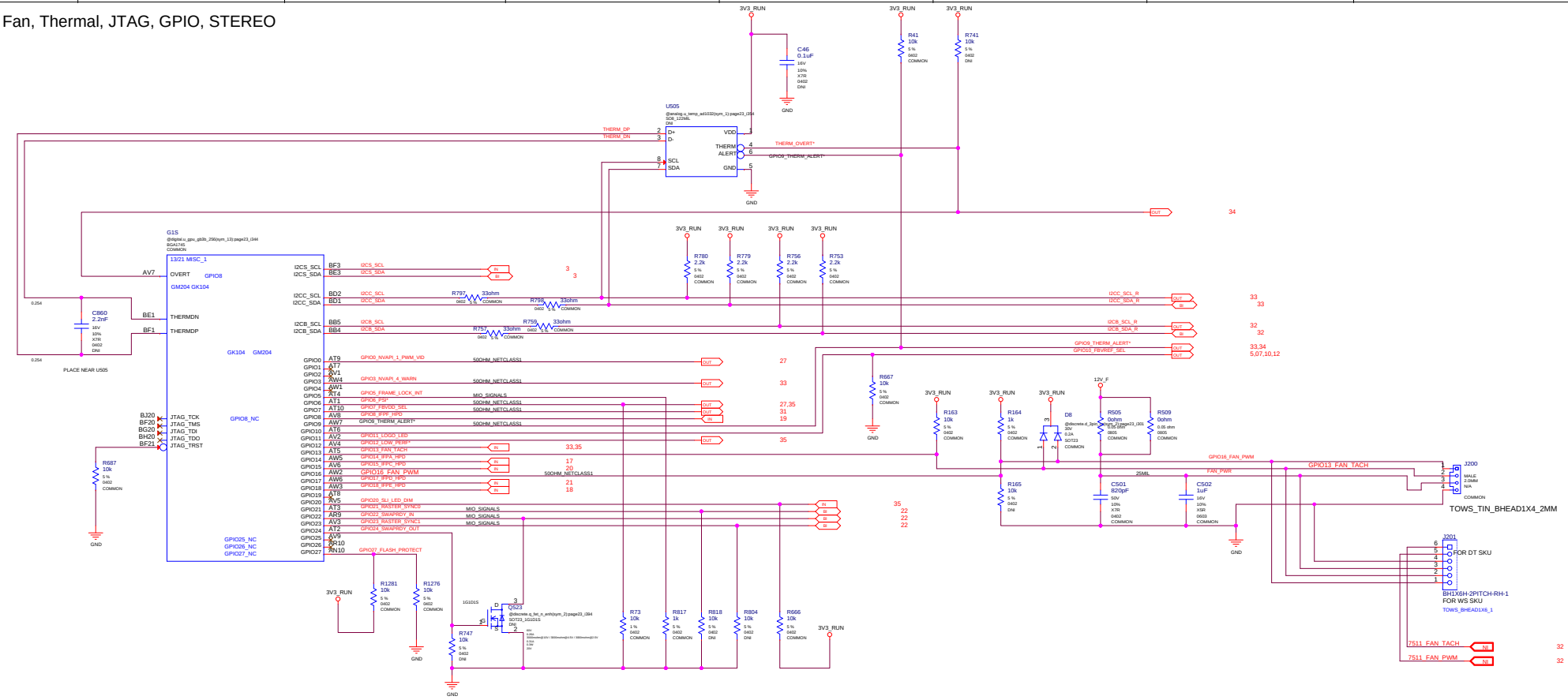
Page23: MISC1: Fan, Thermal, JTAG, GPIO, STEREO



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GPIO, Stereo

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Page24: MISC2: ROM, XTAL, Straps

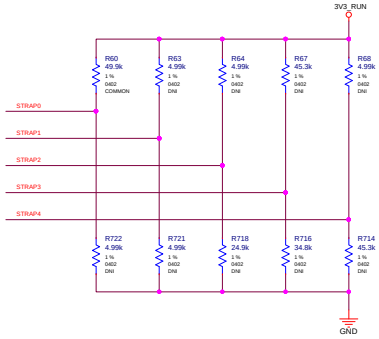
	KEPLER			MAXWELL		
STRAP0	USER_BIT [3:0]*	0000*	5K PD*	GC6	SEE TABLE BELOW	
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*			
STRAP2	PCI_DEVID [3:0]*	0100 - (0x1184)*	25K PD -42S GPU*			
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*			
STRAP4	DP_PLL_VDD_33V*	1*	FOR 3_3V*			
	PEX_MAX_SPEED*	1*	FOR GEN2/3*	45K PD*		
	PEX_SPD_CHANGE_GEN3*	1*	ENABLED*			
	*					
ROM_SI	RAMCFG[0]*	1*		RAMCFG[0]*	1*	
	RAMCFG[1]*	1*	0111 for 64Mx32 256 bit SAMSUNG SAMSUNG for SKU 0 primary memory	RAMCFG[1]*	1*	20K PD*
	RAMCFG[2]*	1*	45K PD*	RAMCFG[2]*	0*	
	RAMCFG[3]*	0*		RAMCFG[3]*	0*	
ROM_SO	VGA_DEVICE*	1*		VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	30k PD*	SMB_ALT_ADDR*	0*	10K PD*
	FB[0]_APERTURE_SIZE*	1*	For 128MB*	PCIE_CFG*	0*	
	FB[1]_APERTURE_SIZE*	0*	For 128MB*	DEVID_SEL*	0*	
ROM_SCLK	PEX_PLL_EN_TERM100*	0*	DISABLED*	SOR0_EXPOSED*	1*	
	PCI_DEVID_EXT[5]*	0*	For 0x1184*	SOR1_EXPOSED*	1*	45K PU*
	SUB_VENDOR*	1*	Dedicated BIOS*	SOR2_EXPOSED*	1*	
	PCI_DEVID_EXT[4]*	0*	For 0x1184*	SOR3_EXPOSED*	1*	

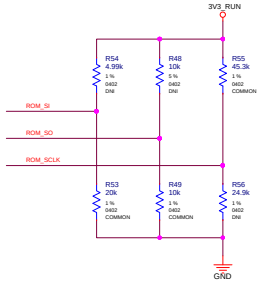
0x13C0

MULTI_STRAP_REF0_GND	
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND

MAXWELL

STRAP0		
3.3V	1.65V	0V
GC6+ ISLAND ENABLED	GC6+ DEBUG MODE	GC6+ ISLAND DISABLED





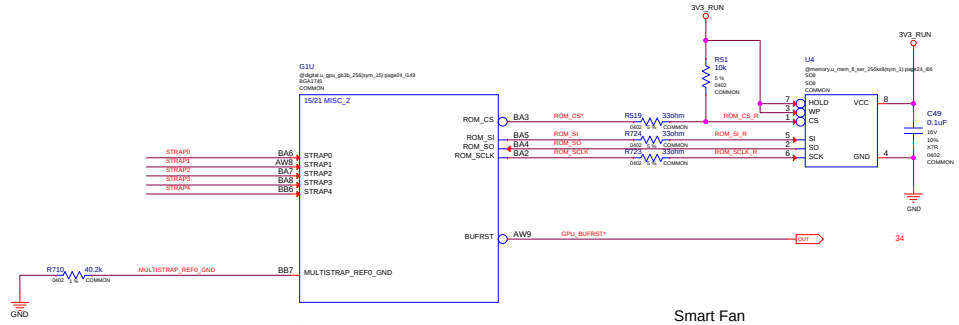
KEPLER

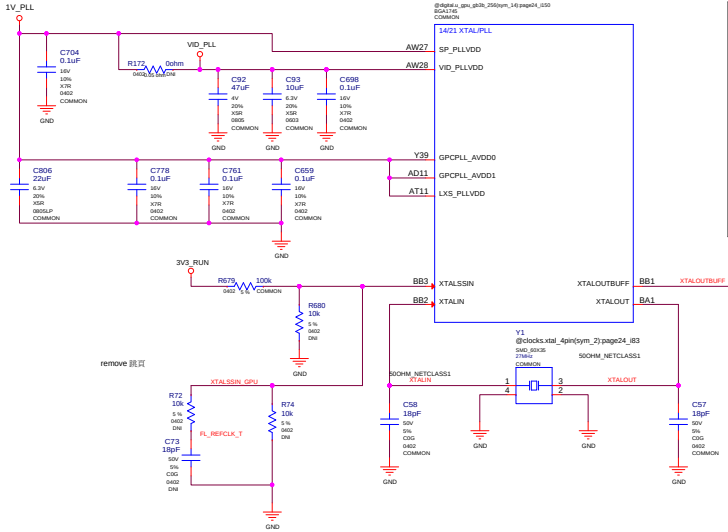
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	32Mx32 256-bit Elpida	
0010	32Mx32 256-bit Hynix	
0011	32Mx32 256-bit Samsung	
0100	Reserved	
0101	64Mx32 256-bit Elpida	
0110	64Mx32 256-bit Hynix	
0111	64Mx32 256-bit Samsung	
1000	Reserved	
1001	32Mx32 192-bit Elpida	
1010	32Mx32 192-bit Hynix	
1011	32Mx32 192-bit Samsung	
1100	Reserved	
1101	64Mx32 192-bit Elpida	
1110	64Mx32 192-bit Hynix	
1111	64Mx32 192-bit Samsung	

MAXWELL

CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	128Mx32 256-bit Elpida	
0010	128Mx32 256-bit Hynix	
0011	128Mx32 256-bit Samsung	
0100	Reserved	
0101	64Mx32 256-bit Elpida	
0110	64Mx32 256-bit Hynix	
0111	64Mx32 256-bit Samsung	





Smart Fan

KEPLER

XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)

MAXWELL

XTALOUTBUFF		
3.3V	1.65V	0V
66% PWM	33% PWM	DISABLED

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MISC2: ROM, XTAL, Straps

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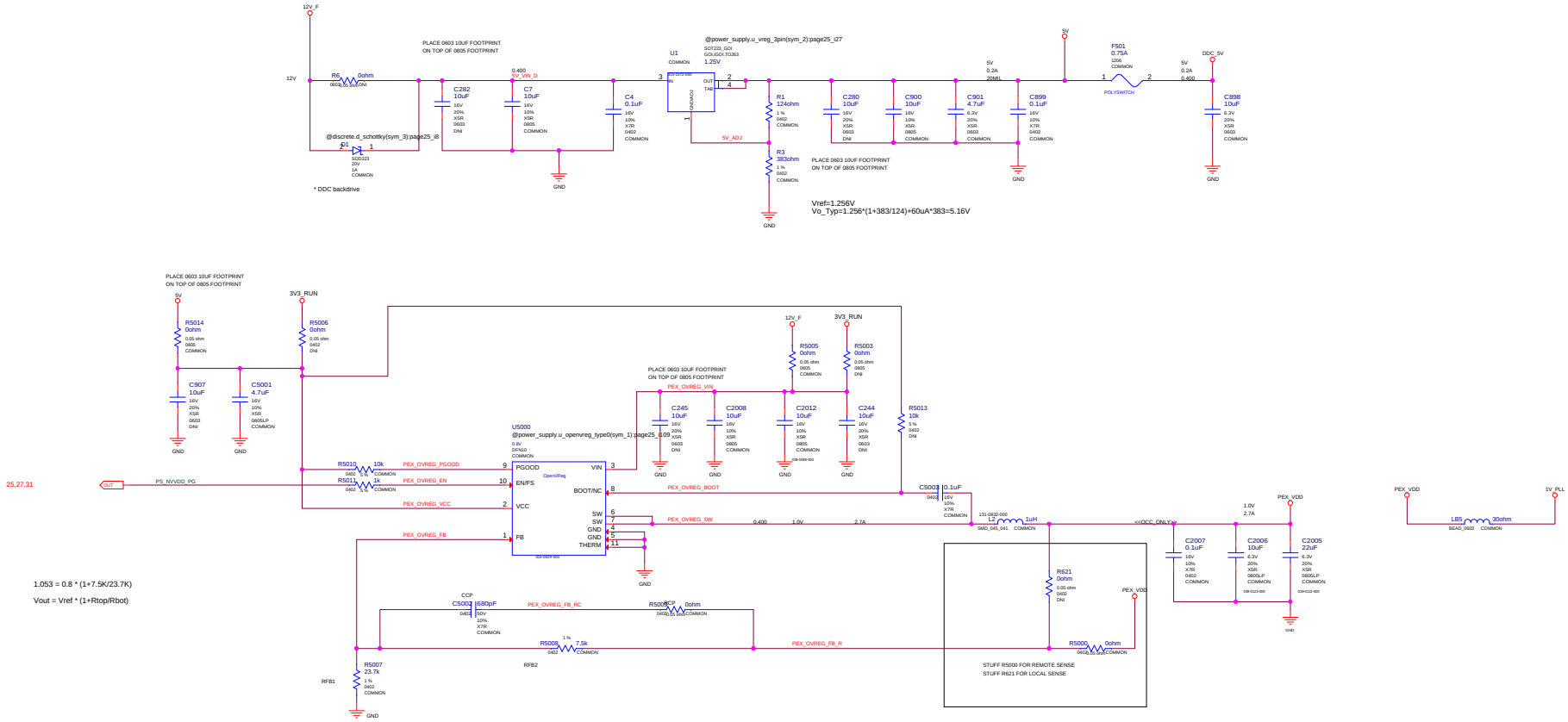
Page25: PS: 5V, PEX_VDD



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: 5V, PEX_VDD

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Custom	PS: 5V, PEX_VDD	1.0

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: FBVDDIQ

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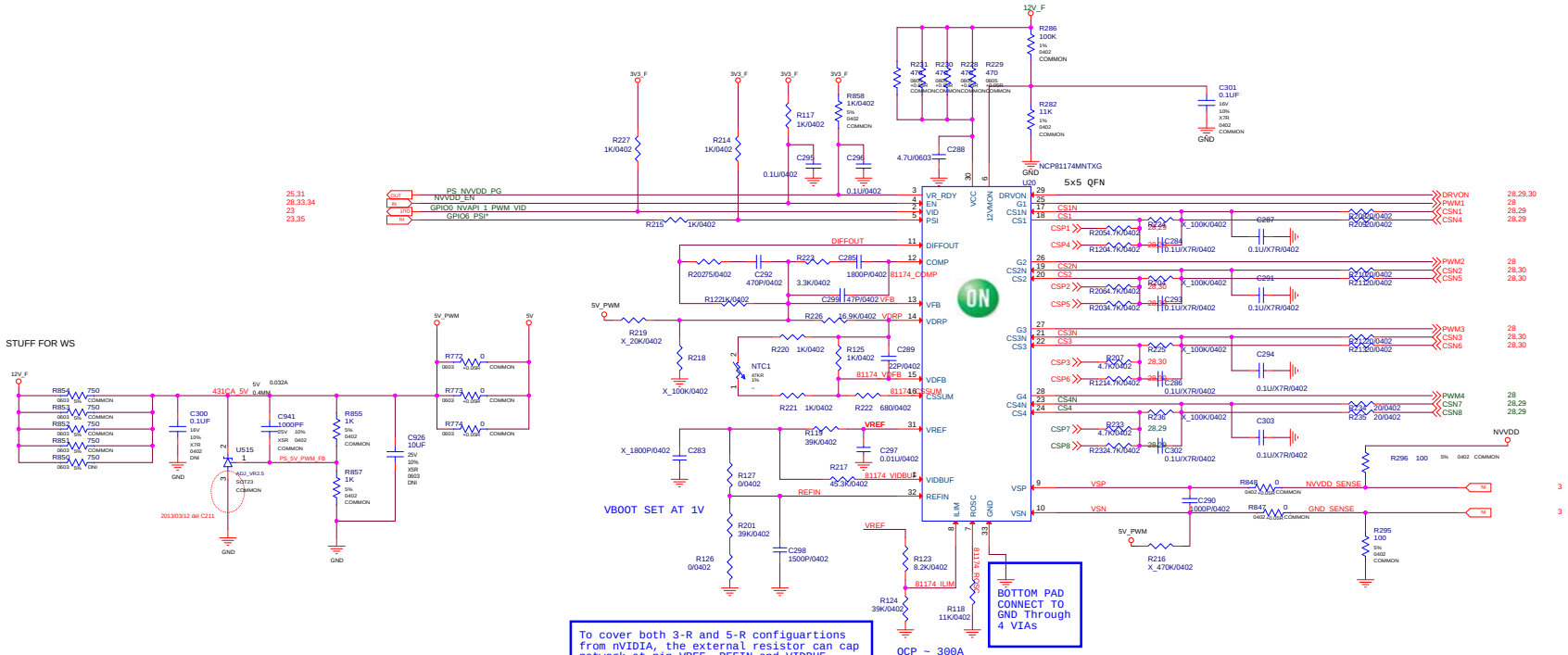
Page27: PS: NVVDD Controller



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Controller

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Custom	PS: NVVDD Controller	1.0

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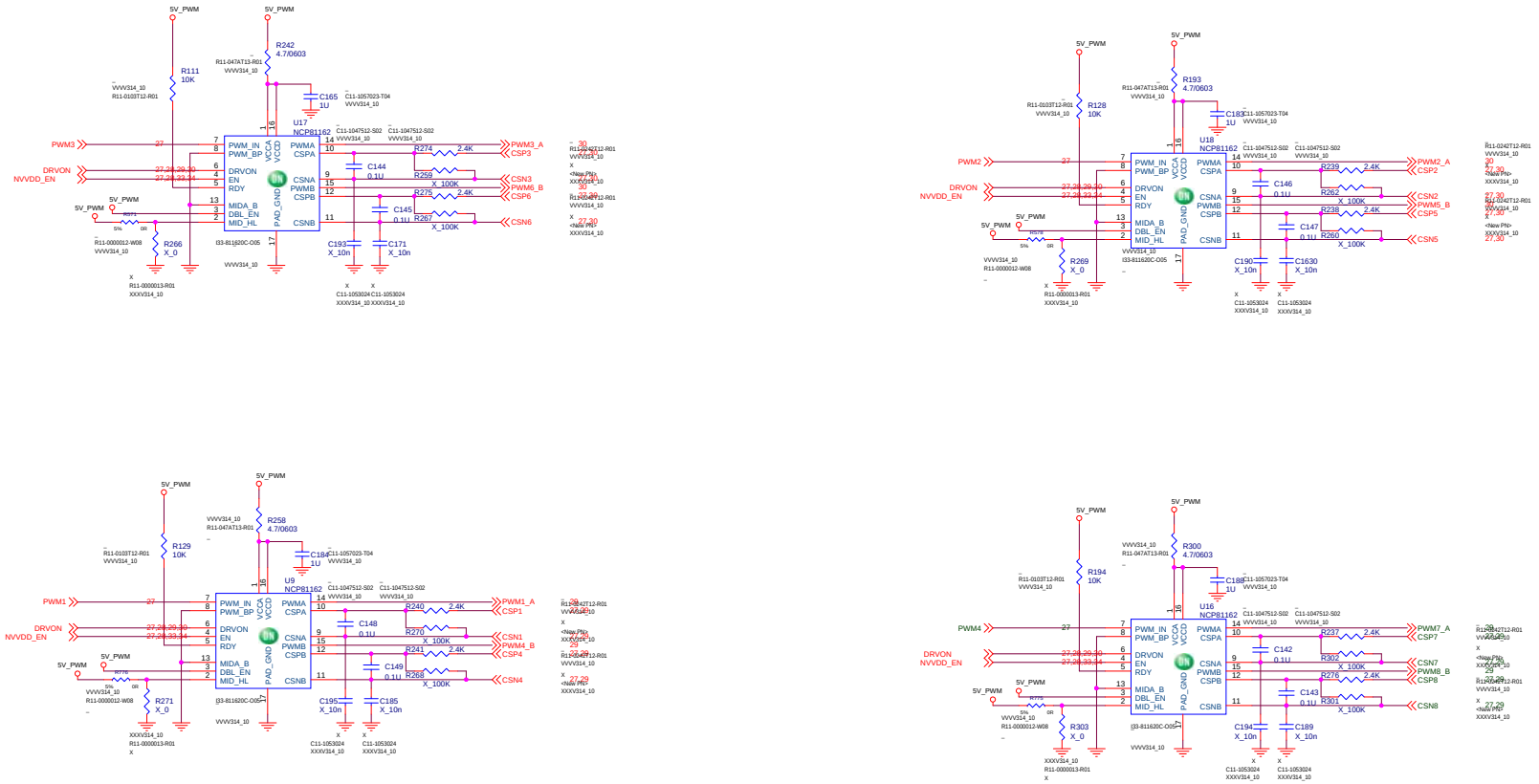
Page28: NVVDD PHASE DOUBLERS



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Phase 1,2

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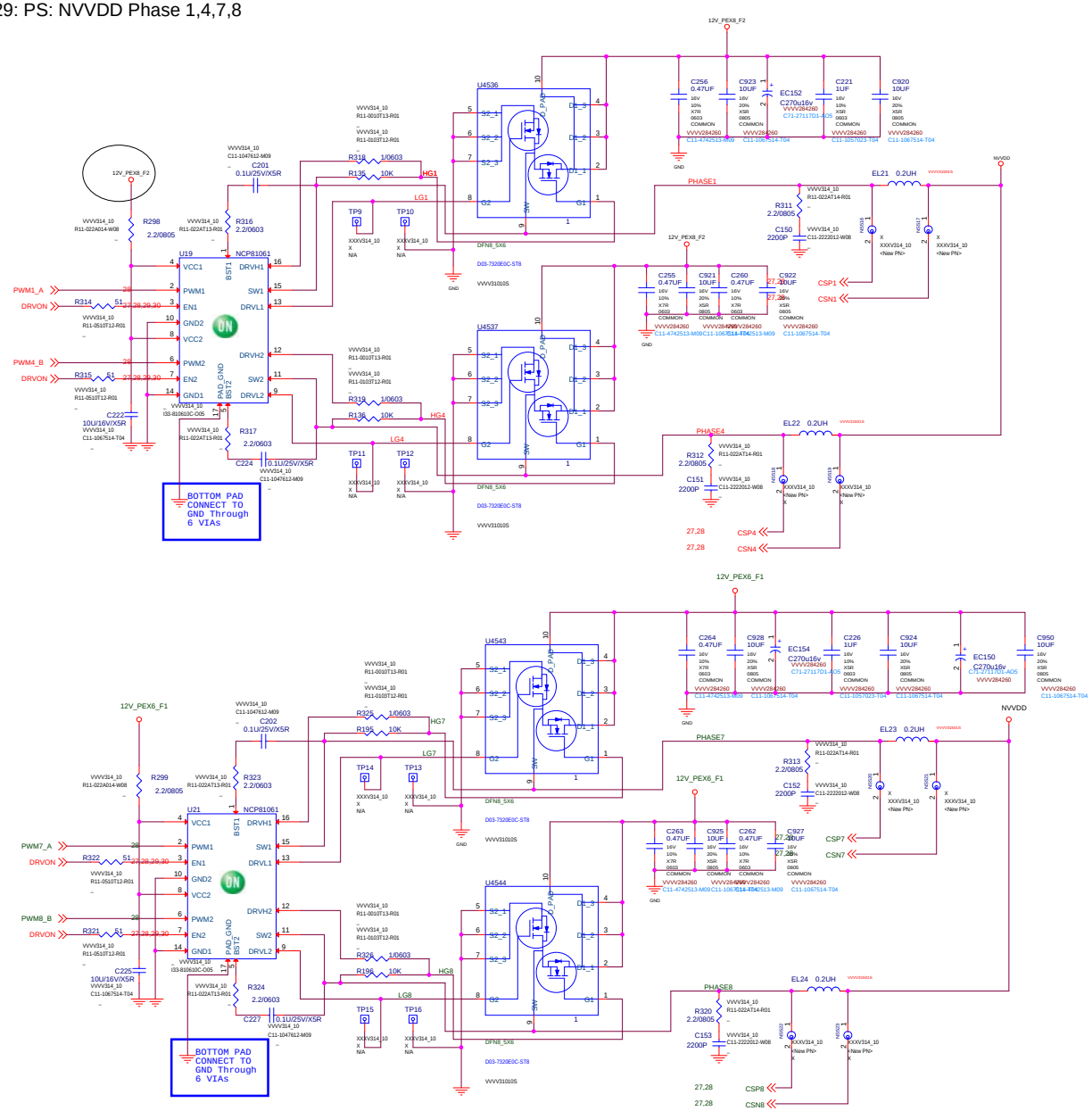
Page29: PS: NVVDD Phase 1,4,7,8



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PAGE DETAIL	PS: NVVDD Phase 3,4

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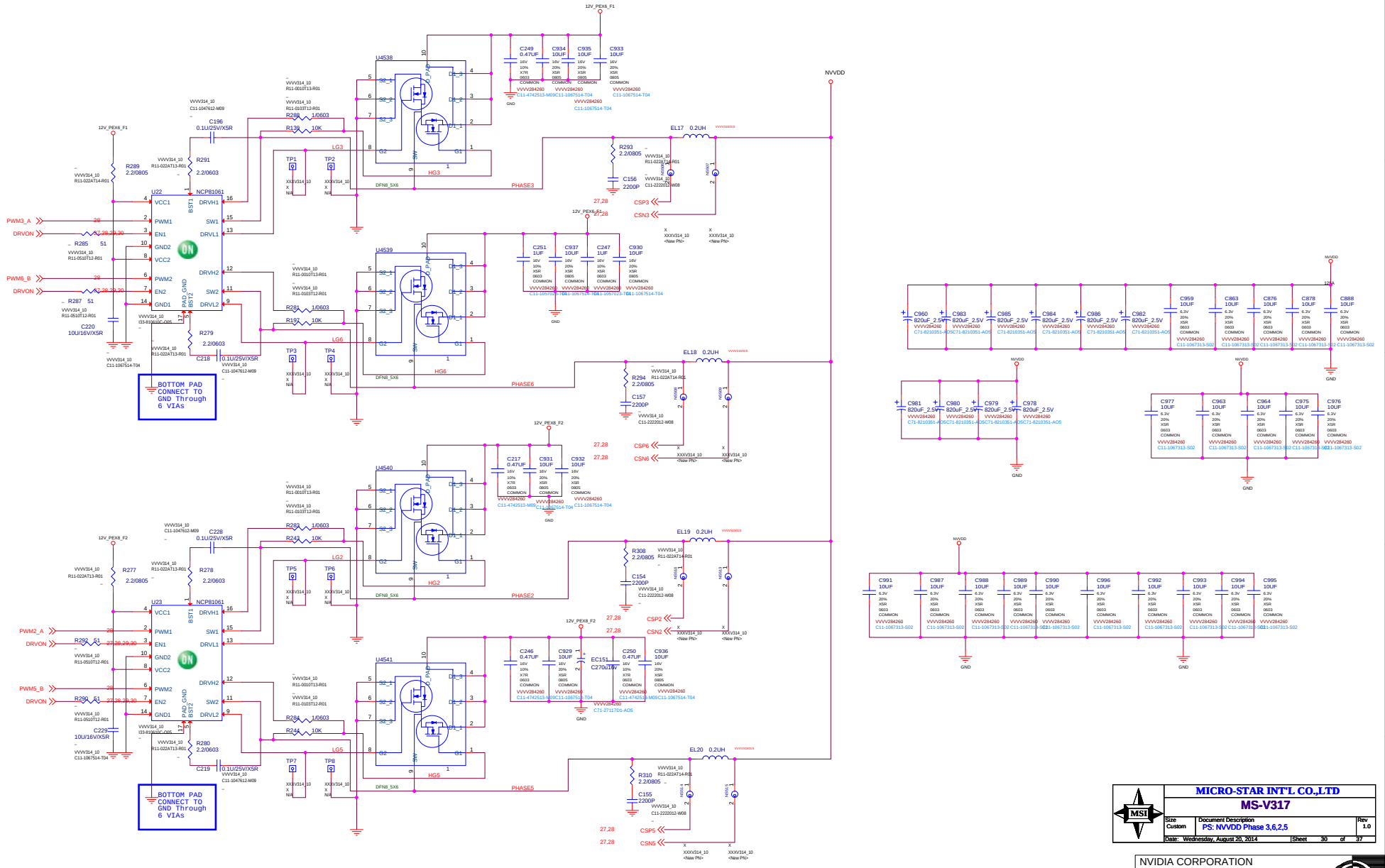
Page30: PS: NVVDD Phase 3,6,2,5



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Phase 5, 6

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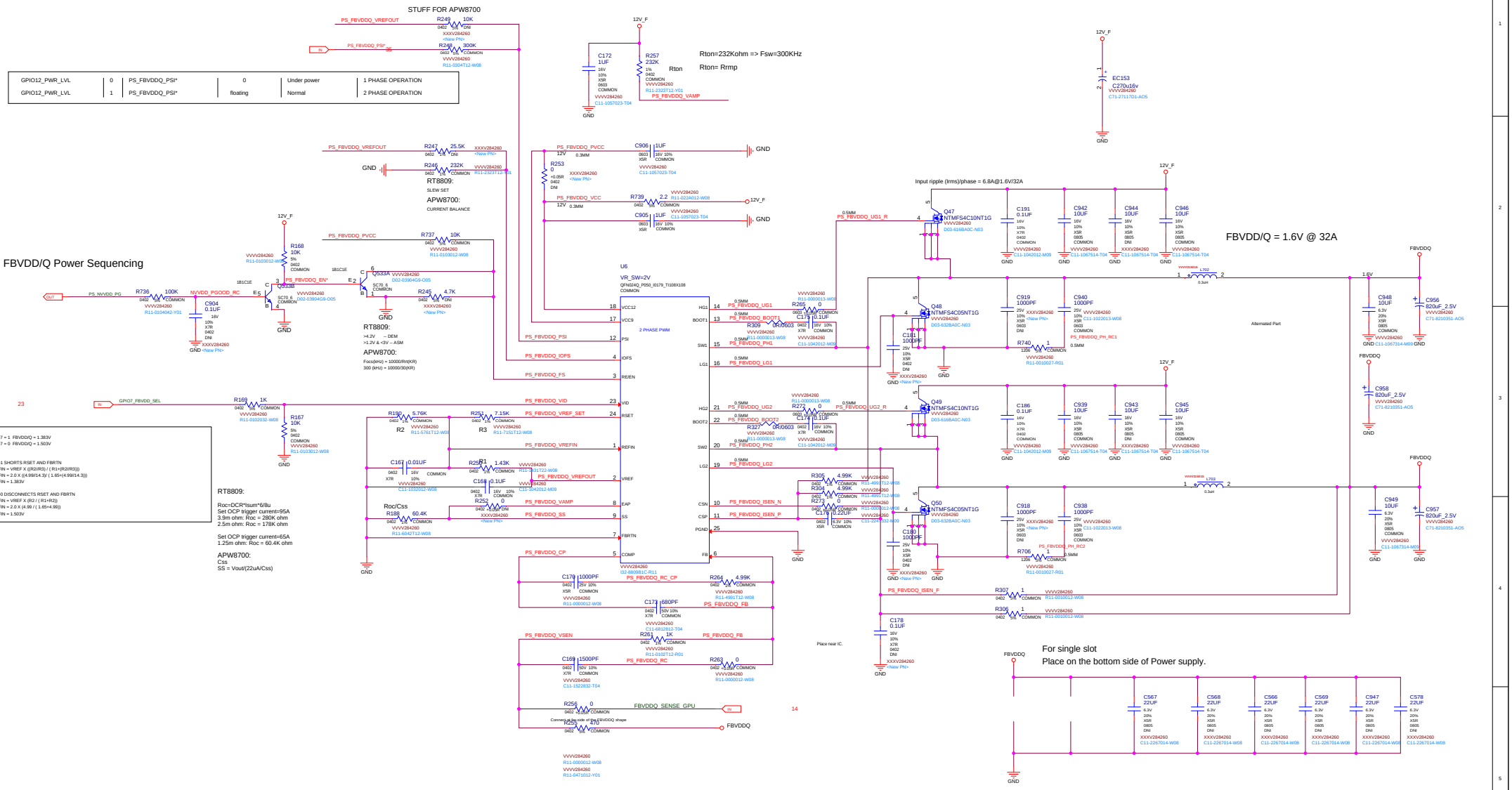
Page31: FBVDDQ



GPIO12_PWR_LVL	0	PS_FBVDDQ_PSI*	0	Under power	1 PHASE OPERATION
GPIO12_PWR_LVL	1	PS_FBVDDQ_PSI*	floating	Normal	2 PHASE OPERATION

GPIO7 = 1 FBVDDQ = 1.383V
GPIO7 = 0 FBVDDQ = 1.503V

VID =1 SHORTS RSET AND FBRTN
VREFIN = VREF X ((R2//R3) / (R1+(R2//R3)))
VREFIN = 2.0 X ((4.99/14.3)/ (1.65+(4.99/14.3)))
VREFIN = 1.383V

VID =0 DISCONNECTS RSET AND FBRTN
VREFIN = VREF X (R2 / (R1+R2))
VREFIN = 2.0 X (4.99 / (1.65+4.99))
VREFIN = 1.503V

RT8809:
Roc=DCR*Isum*6/8u
Set OCP trigger current=95A
3.9m ohm: Roc = 280K ohm
2.5m ohm: Roc = 178K ohm

Set OCP trigger current=65A
1.25m ohm: Roc = 60.4K ohm

APW8700:
Css
SS = Vout/(22uA/Css)

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PAGE DETAIL	PS: Dynamic Power Balance Logic

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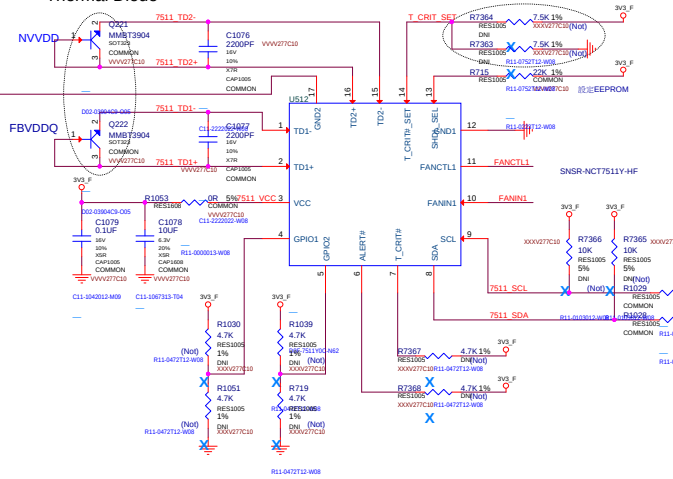
Page32: 7511-FAN

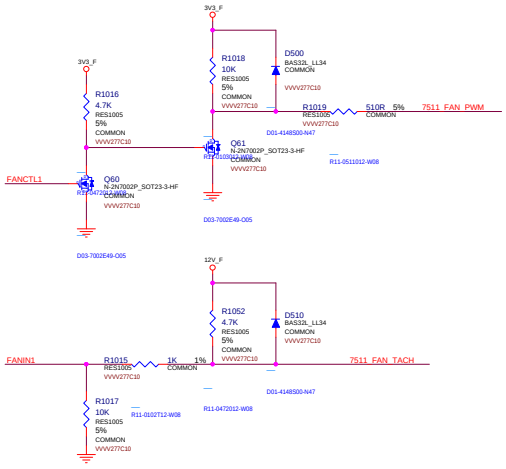
Thermal IC : NCT7511Y

Layout notice :
*Add ground shielding for D+ and Dtraces.
*D+/D- route has to be away from the high noise area.
*The recommended traces width and ground shielding spacing are 10mils.

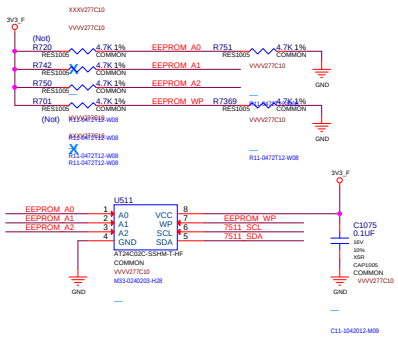
Please refer datasheet
TCRIT_SET Table
If floating,shutdown temp. set to 65℃

Thermal Diode

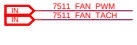




EEPROM



Fan connector option



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Dynamic Power Balance Phases

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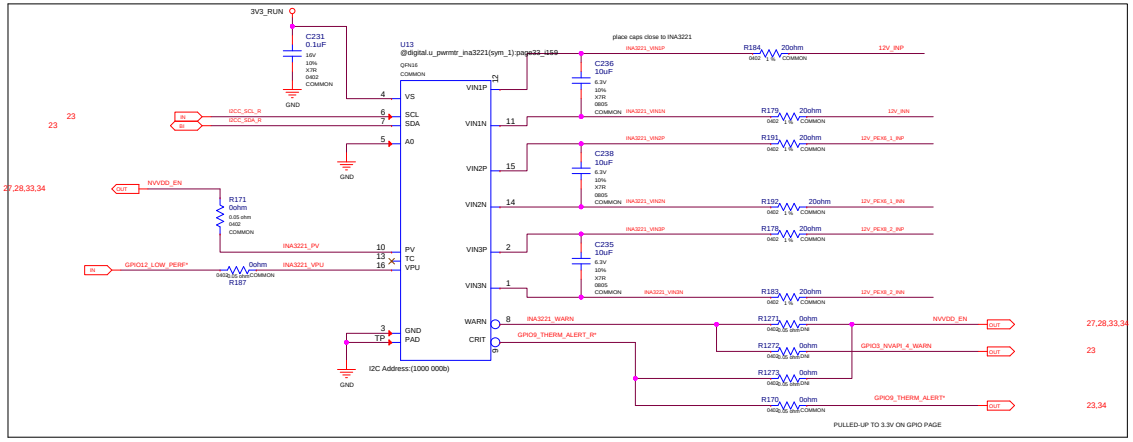
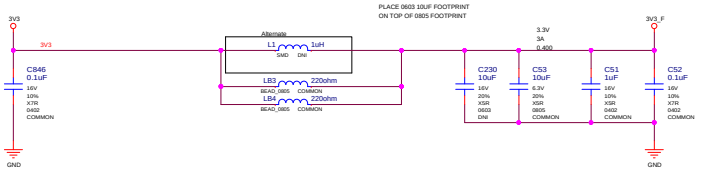
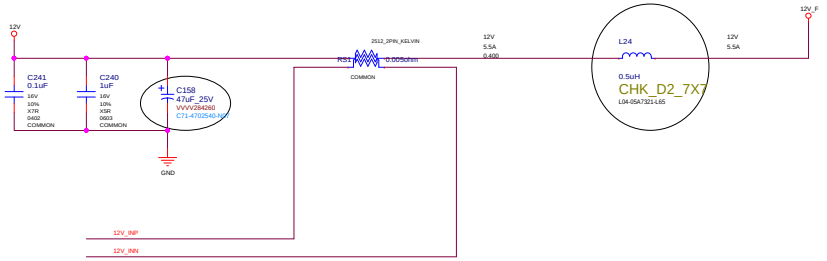
Page33: PS: Inputs, Filtering, and Monitoring



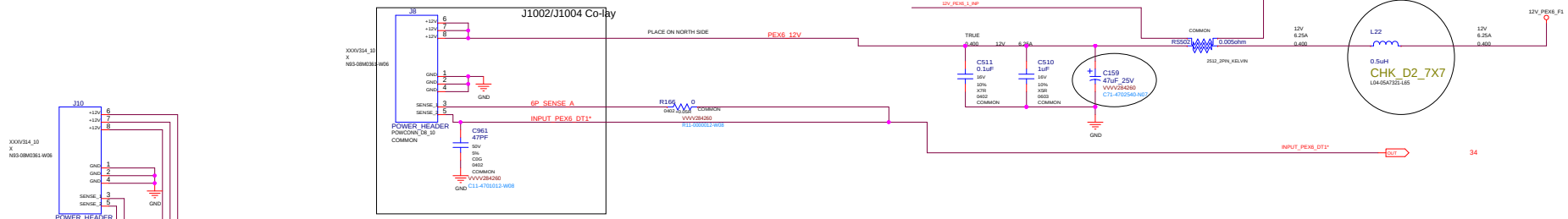
PEX 3V3 INPUT - 10W



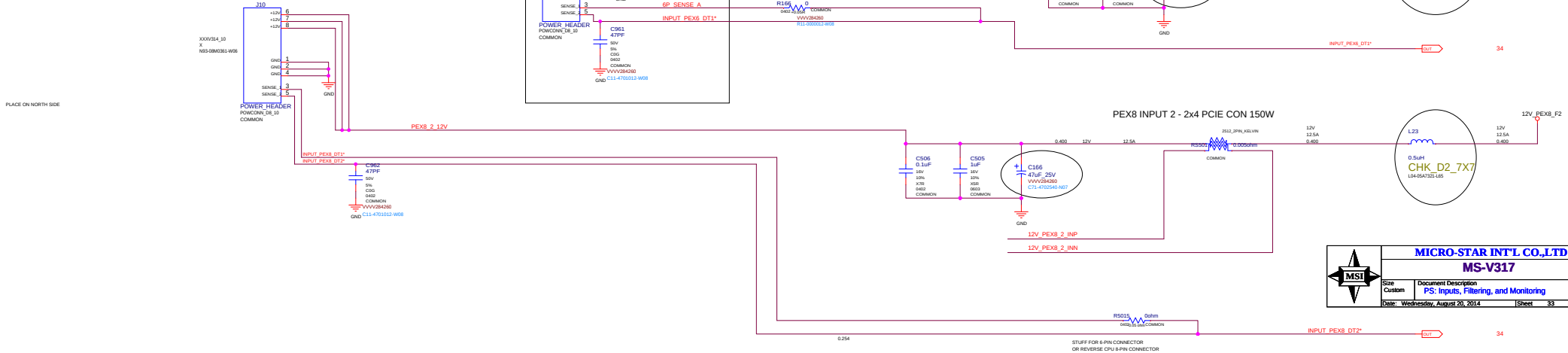
PEX_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PCIE CON 75W



PEX8 INPUT 2 - 2x4 PCIE CON 150W



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PAGE DETAIL	PS: Inputs, Filtering, and Monitoring

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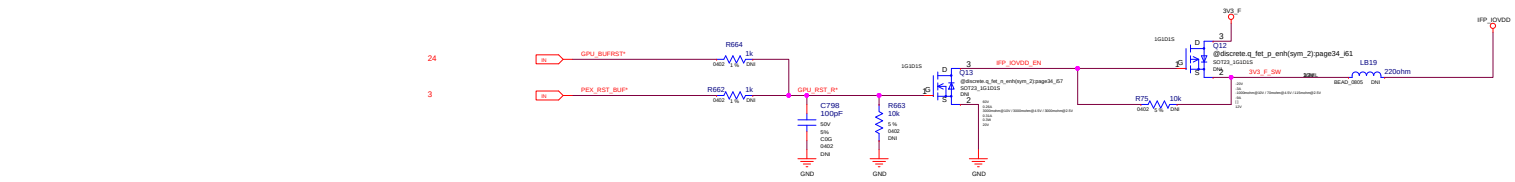
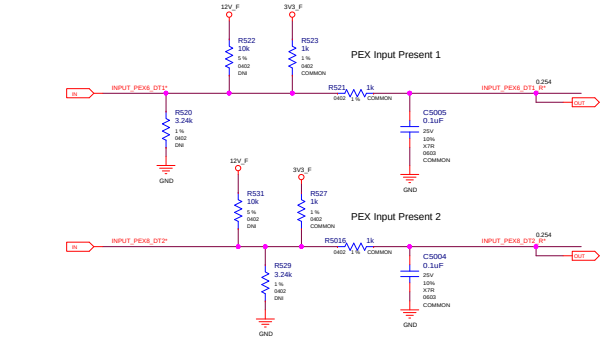
Page34: PS: Shutdown

THERM OVERT SHUTDOWN LATCH

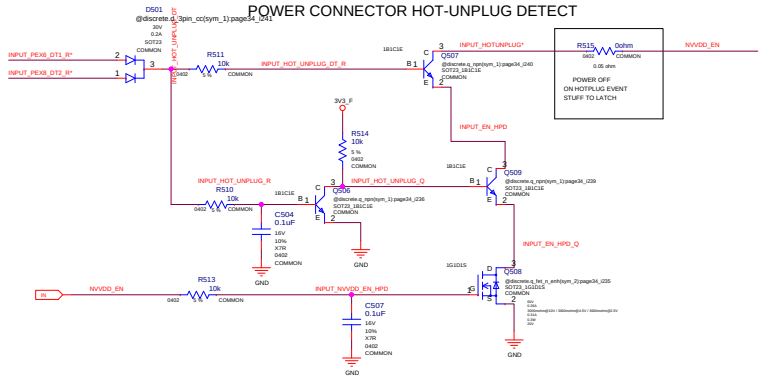
IFP_IOVDD (backdrive prevention)

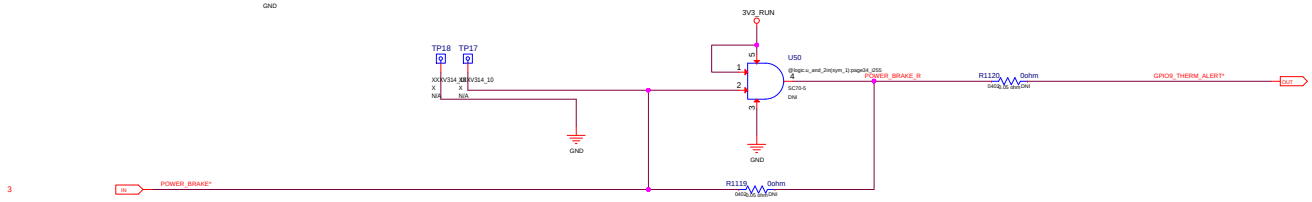


PEX Input - NVVDD Power Sequence



POWER CONNECTOR HOT-UNPLUG DETECT





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PAGE DETAIL	PS: Shutdown

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Page35: PS: 12V Current Steering, PSI Control, and LED

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Size: Custom	Document Description: 12V Current Steering, PSI Control, and LED	Rev: 1.0
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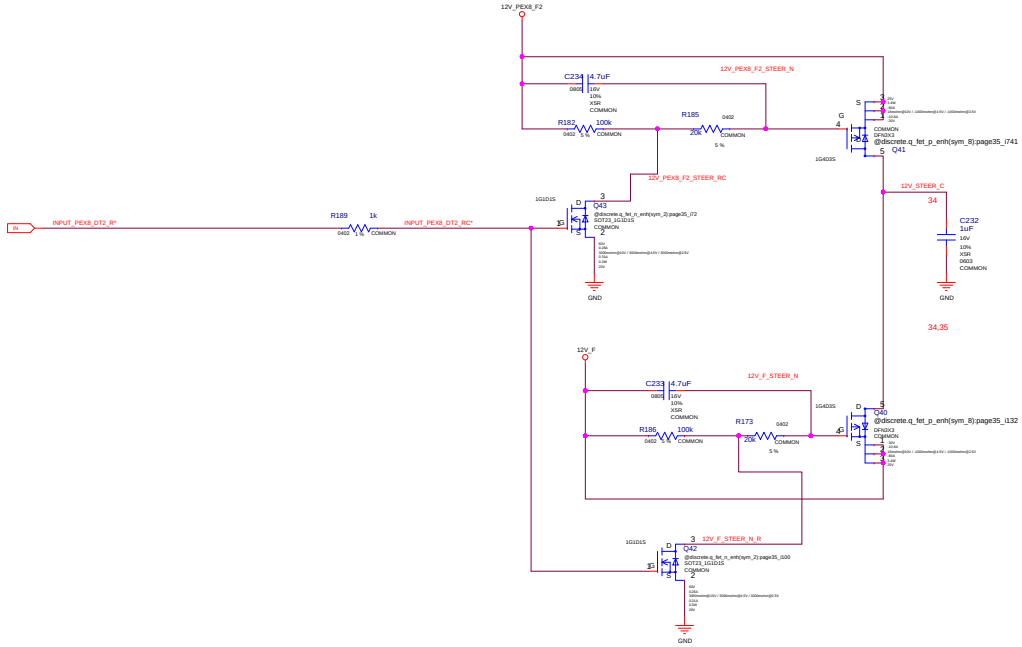
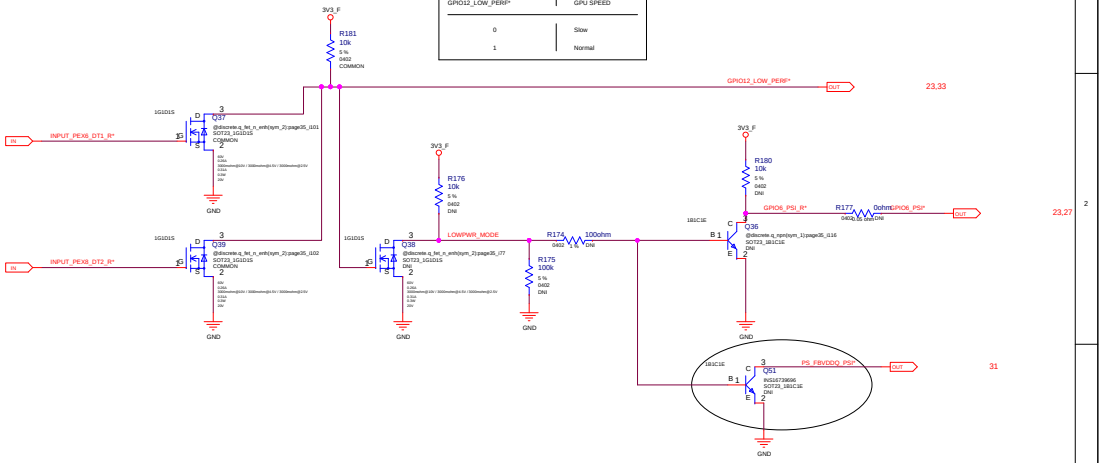
PEX Input - 12V Current Steering FETs



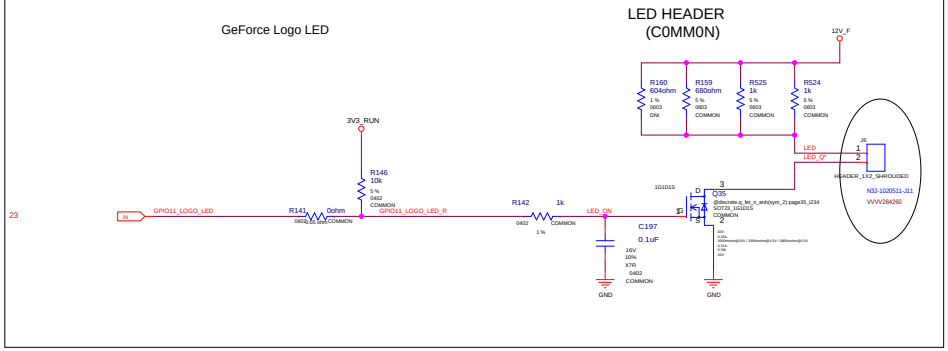
PEX Input - Power Level/PSI* Control

GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

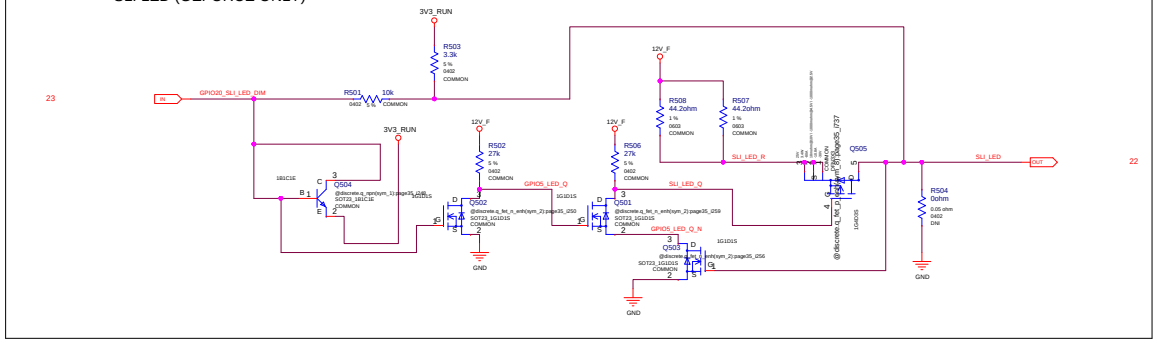


GeForce Logo LED

LED HEADER (C0MM0N)



SLI LED (GEFORCE ONLY)



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PAGE DETAIL	PS: 12V Current Steering PSI Control and LED

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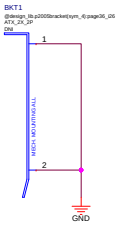
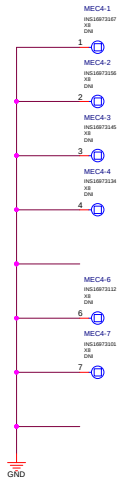
Page36: Mechanical: Bracket/Thermal Solution

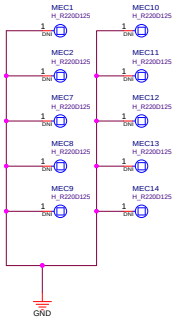
Brackets:

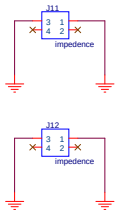


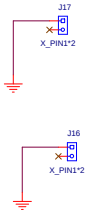
Bracket Screw

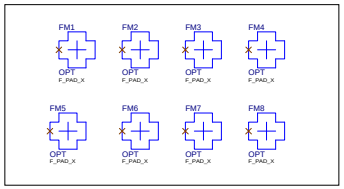


Mechanical Holes Symbol









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PAGE DETAIL	MECH: Bracket/Thermal

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Page37:
1.P17 增加DVI ESD
2.P18~P21 修改HDMI,DP footprint,　增加HDMI ESD
3.簡化ＳＬＩ線路
4.移除原本FBVDDQ線路
5.P27~P30 更換NVVD 線路
6.P31~32 移除dynamic power circuit/增加風扇7511線路
7.P33 更換反插8PIN,Input choke
8.P35 增加MEM PSI 晶體
9.Remove MICROCONTROLLER

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