

PG401 A02

4GB GDDR5, 256b, 128Mx32

Tall DVI-I + DP + DP + DP/HDMI + DP

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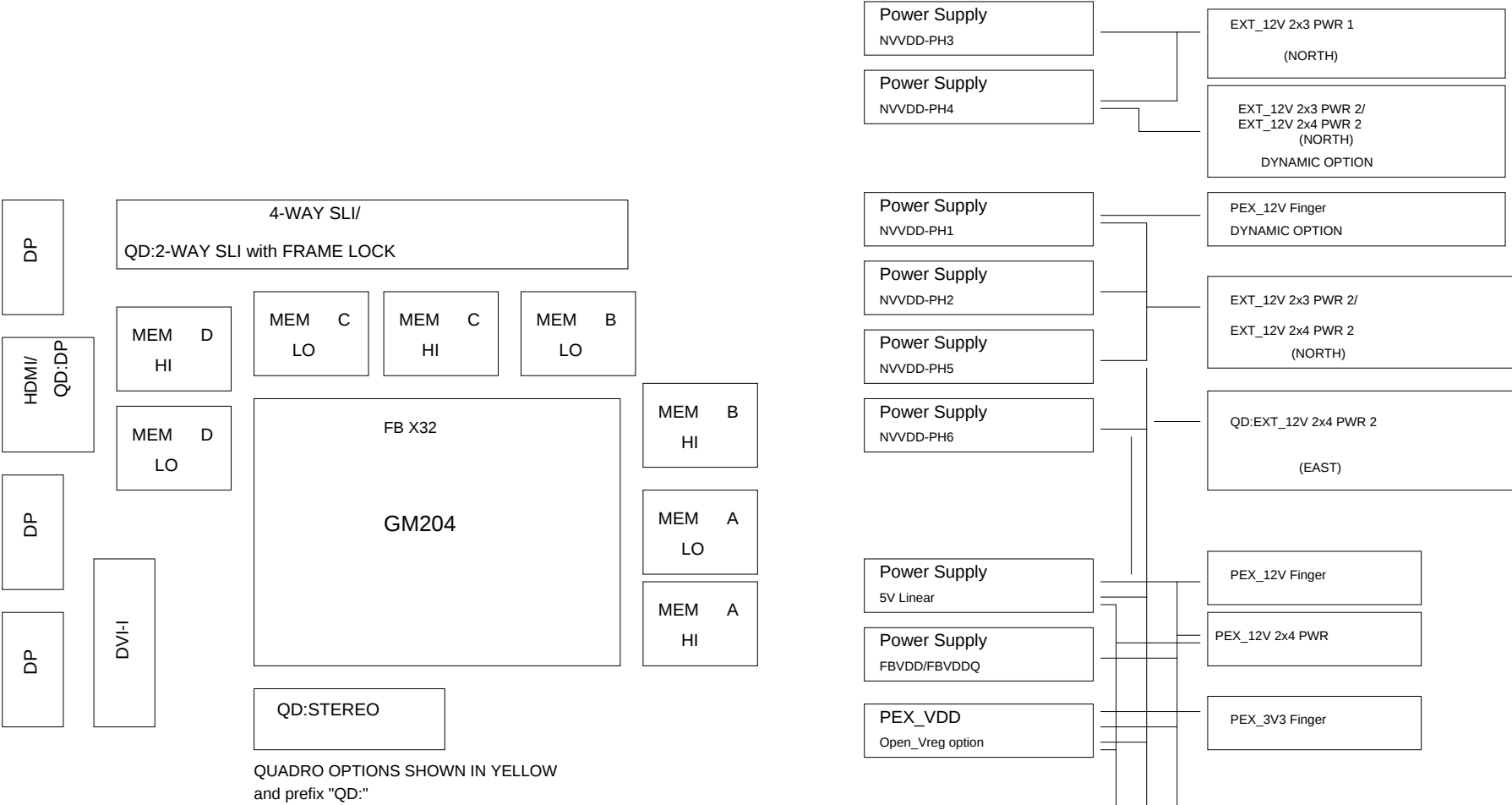
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QUADRO OPTIONS SHOWN IN YELLOW
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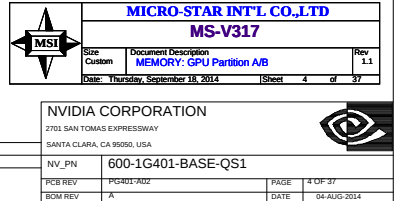


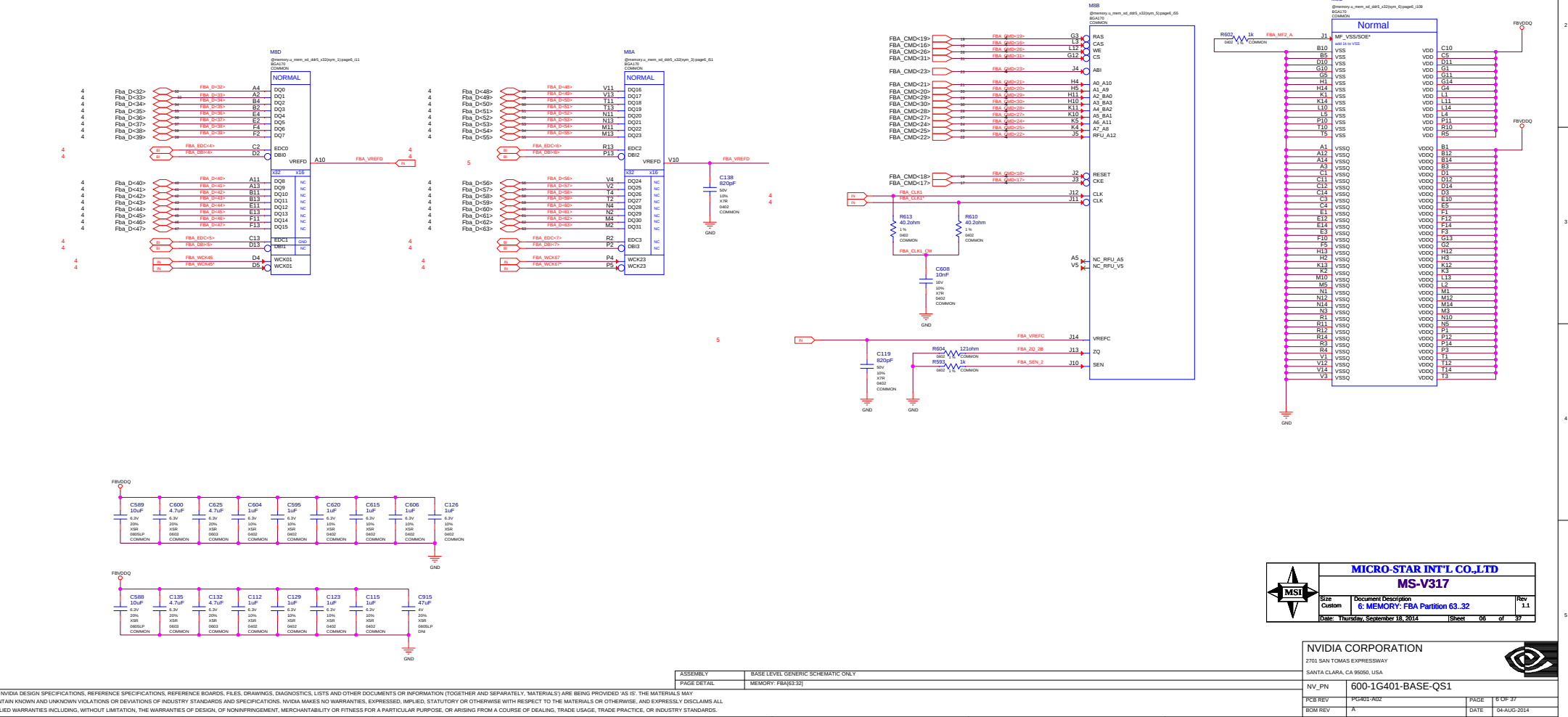
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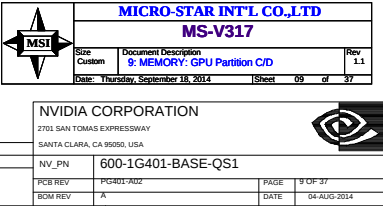
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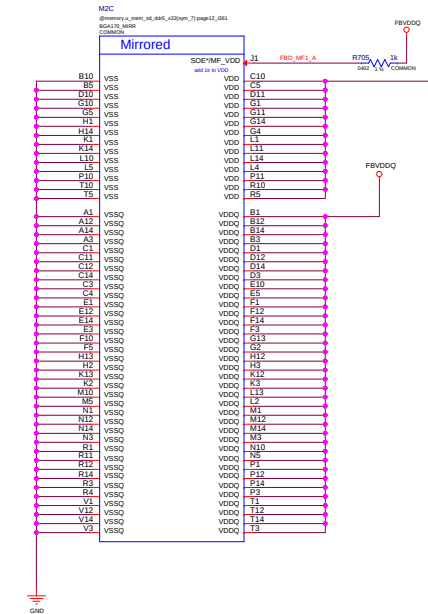
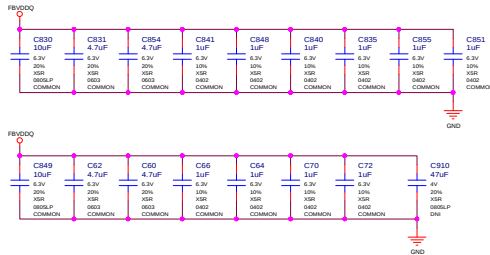


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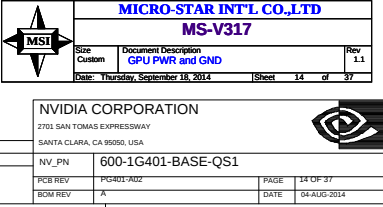


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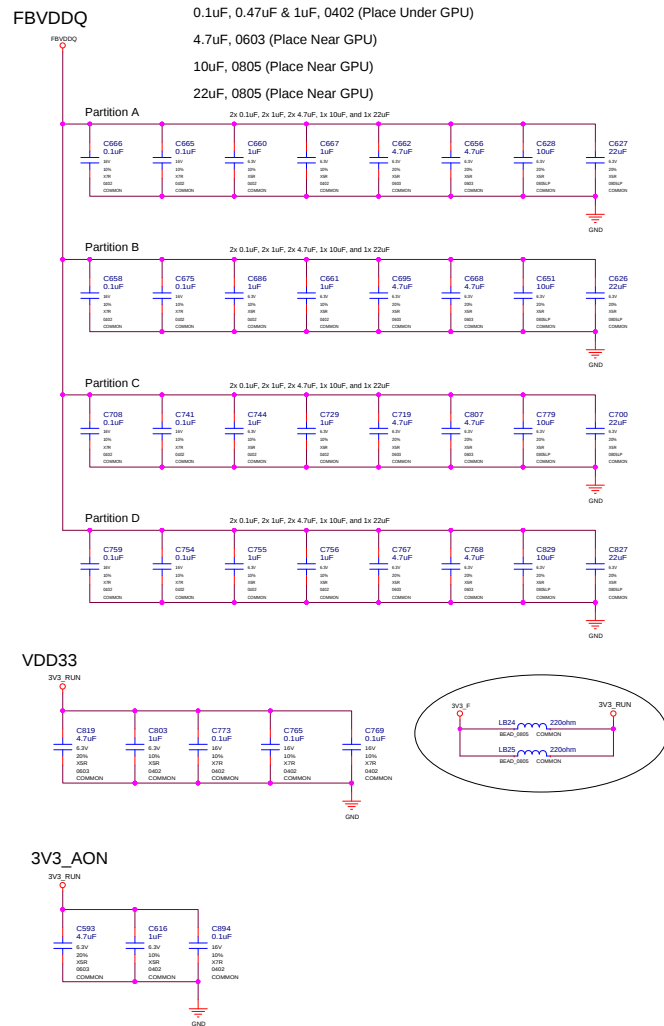
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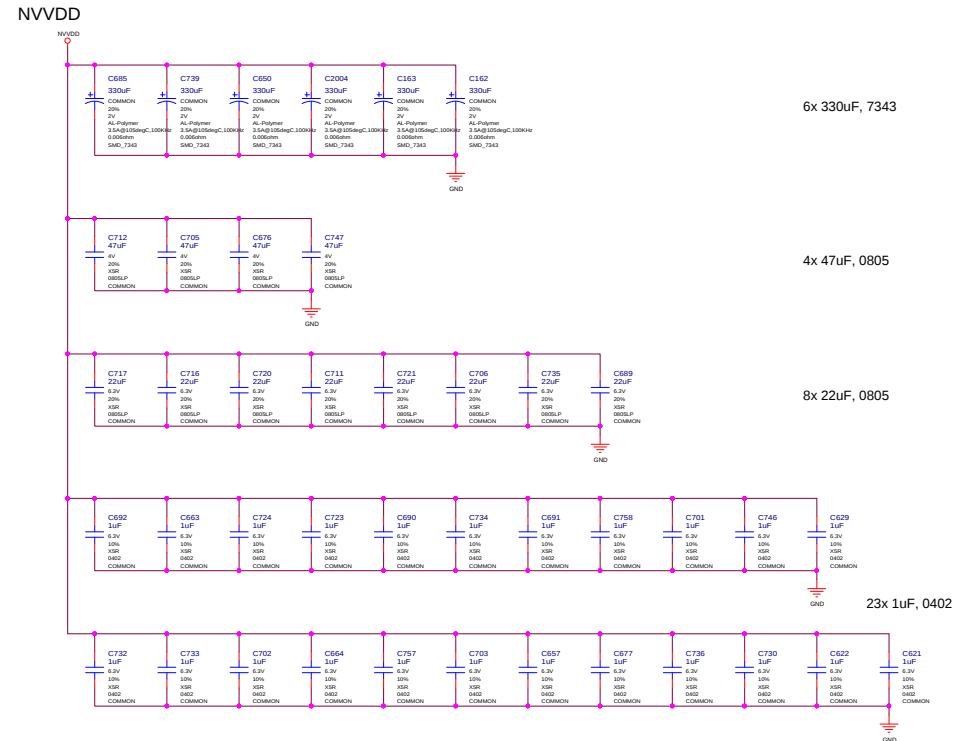
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PAGE DETAIL	MEMORY: FBD(31:0)



Based on GB2-X GDDR5 FBVDDQ Decap Guideline



NVVDD Decoupling caps. Place under GPU.



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPU Decoupling

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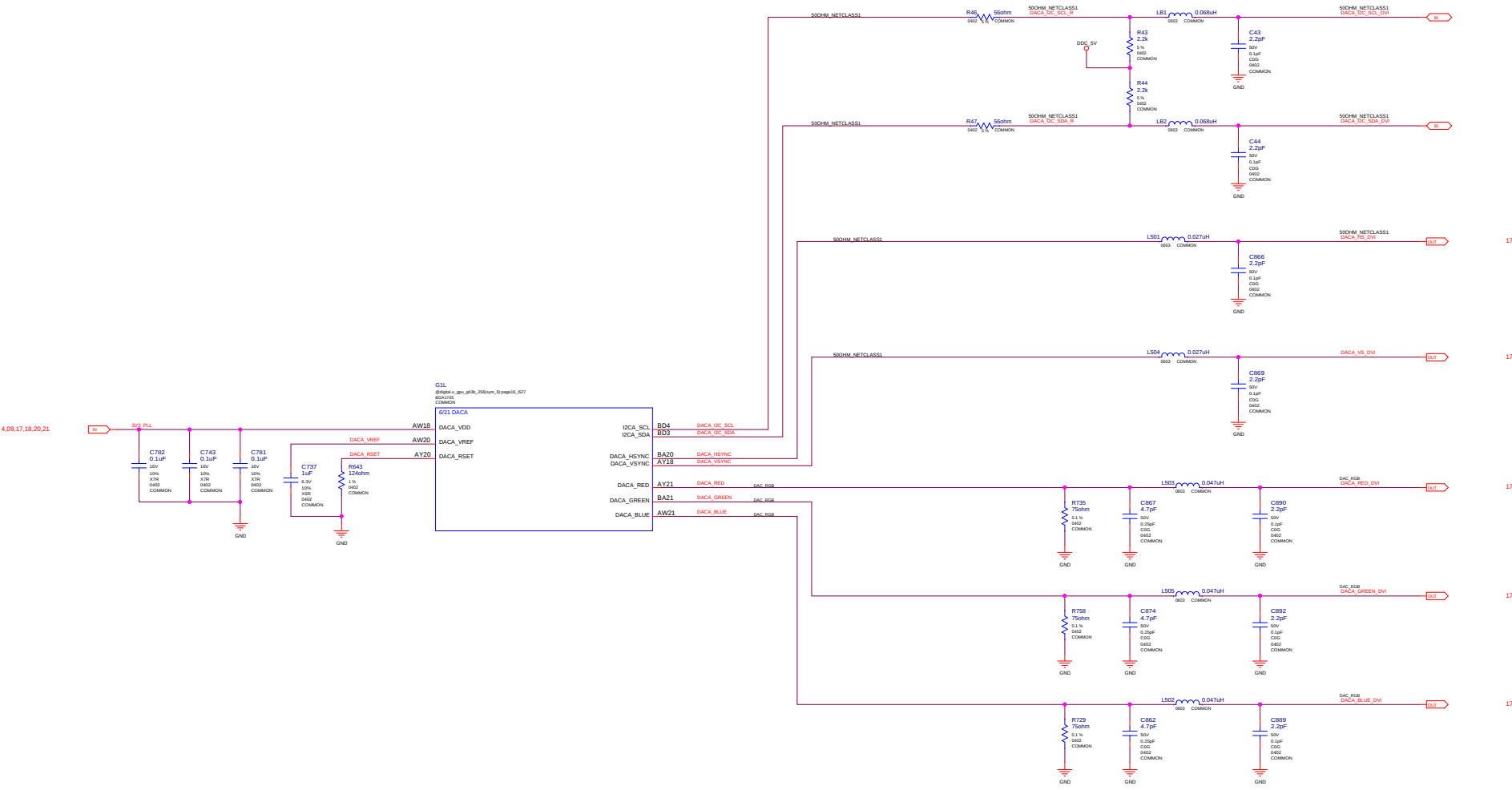
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PCB REV	PG401-A02
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PAGE DETAIL	DACA Interface



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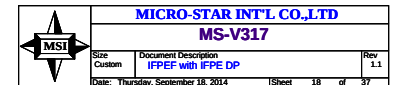
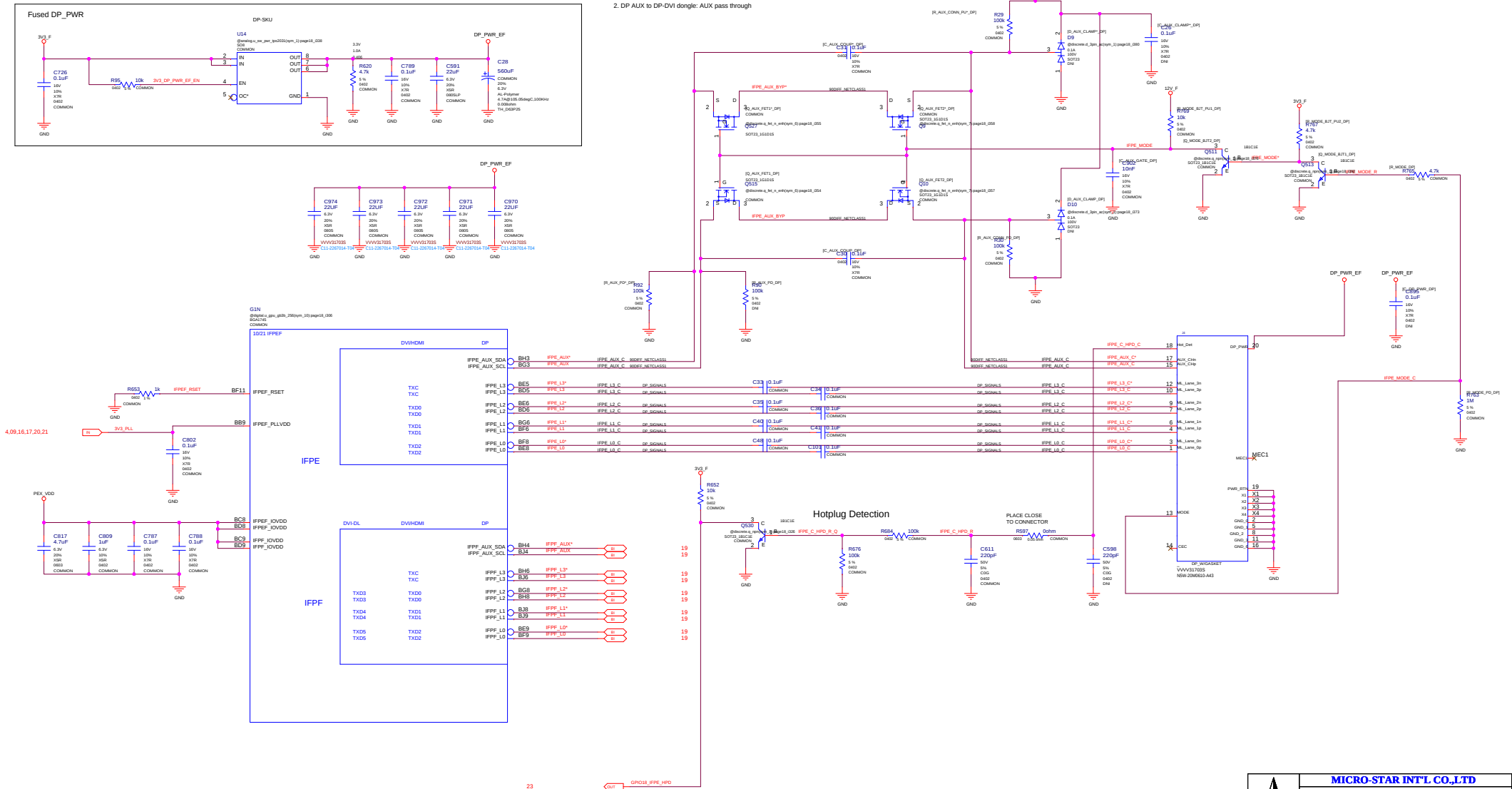


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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPAB DVI-I-DL

Two cases to be considered

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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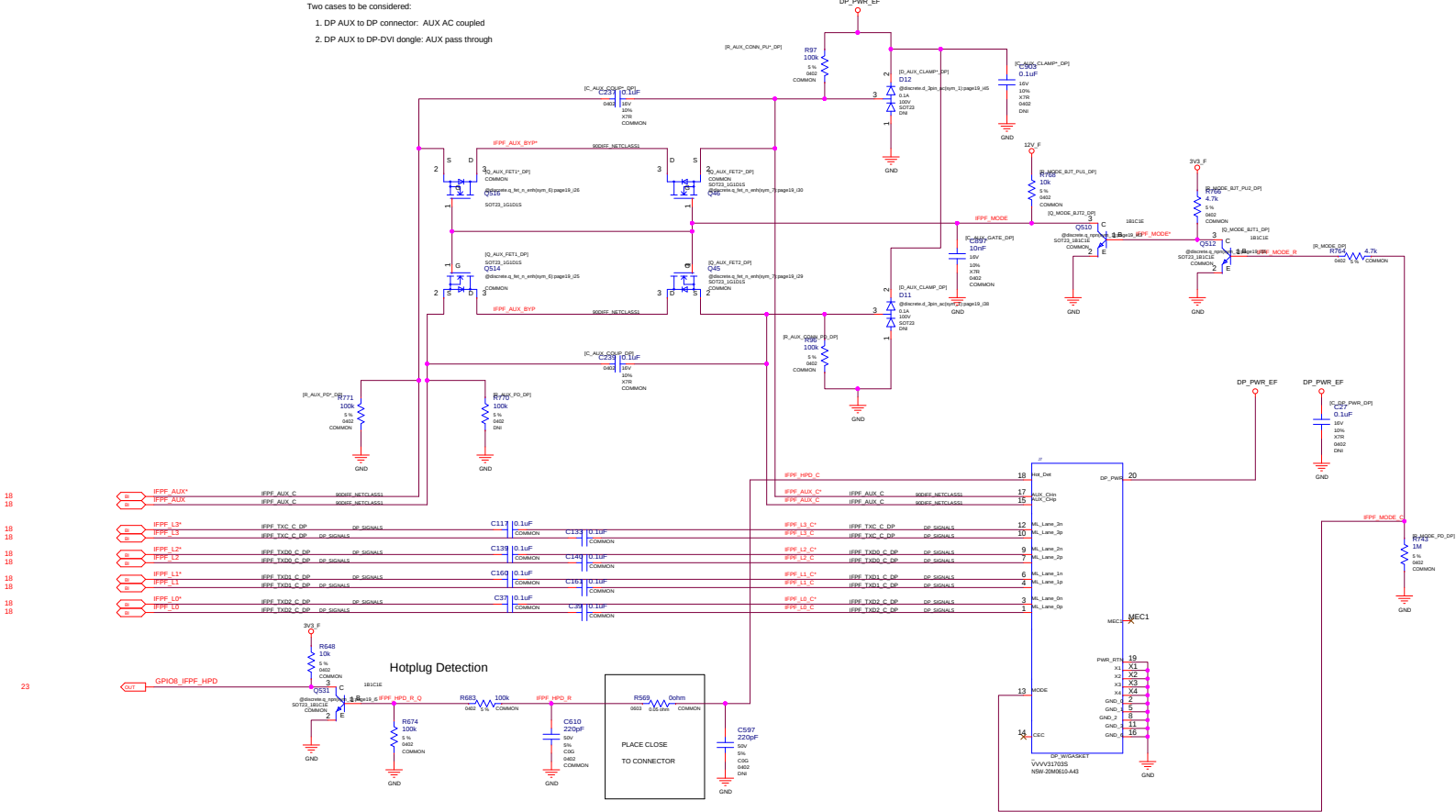
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPEF with IFPE DP

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- Two cases to be considered:
- 1. DP AUX to DP connector: AUX AC coupled
 - 2. DP AUX to DP-DVI dongle: AUX pass through



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PAGE DETAIL	IFPF DP



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PG401-A02

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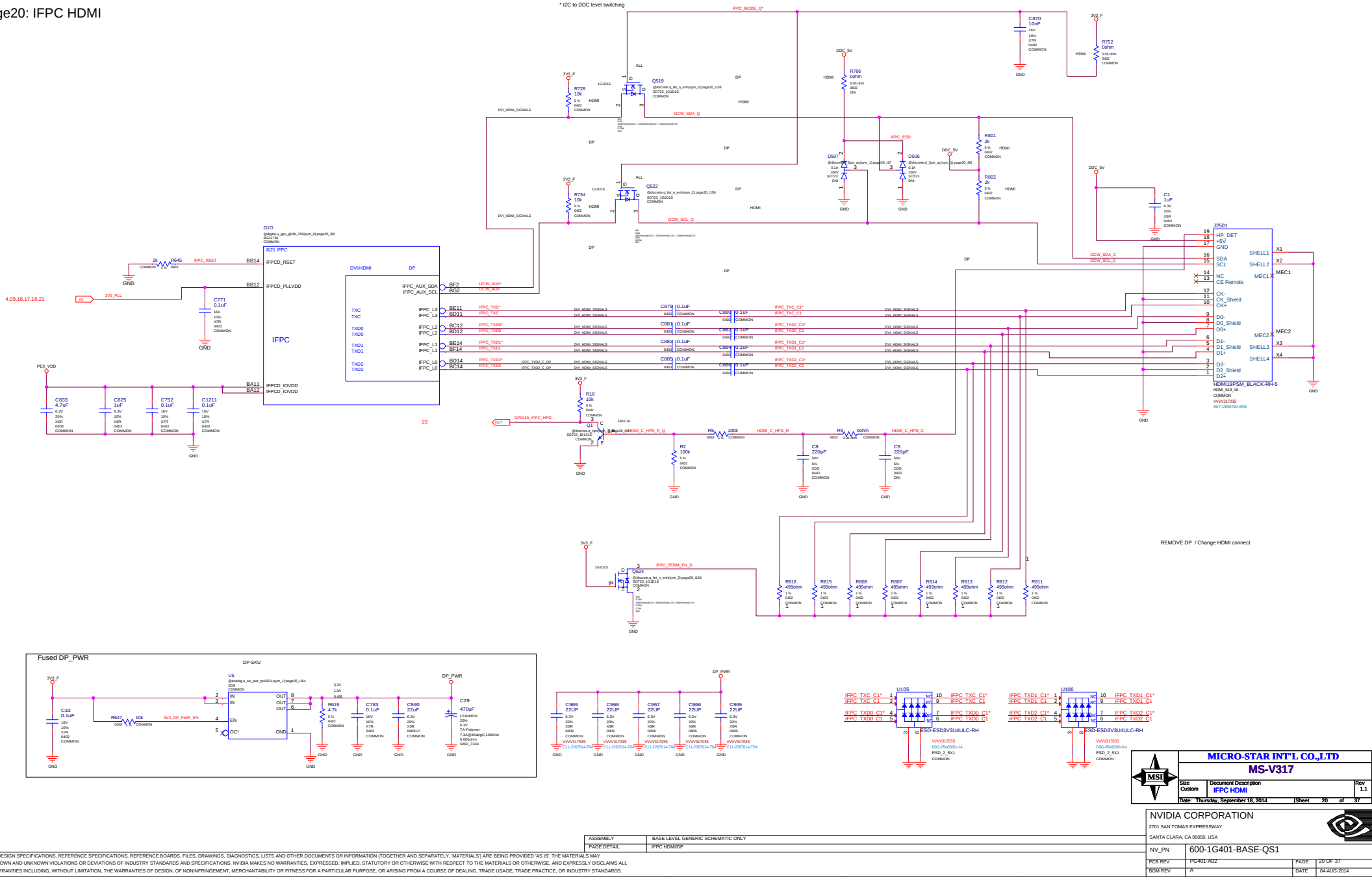
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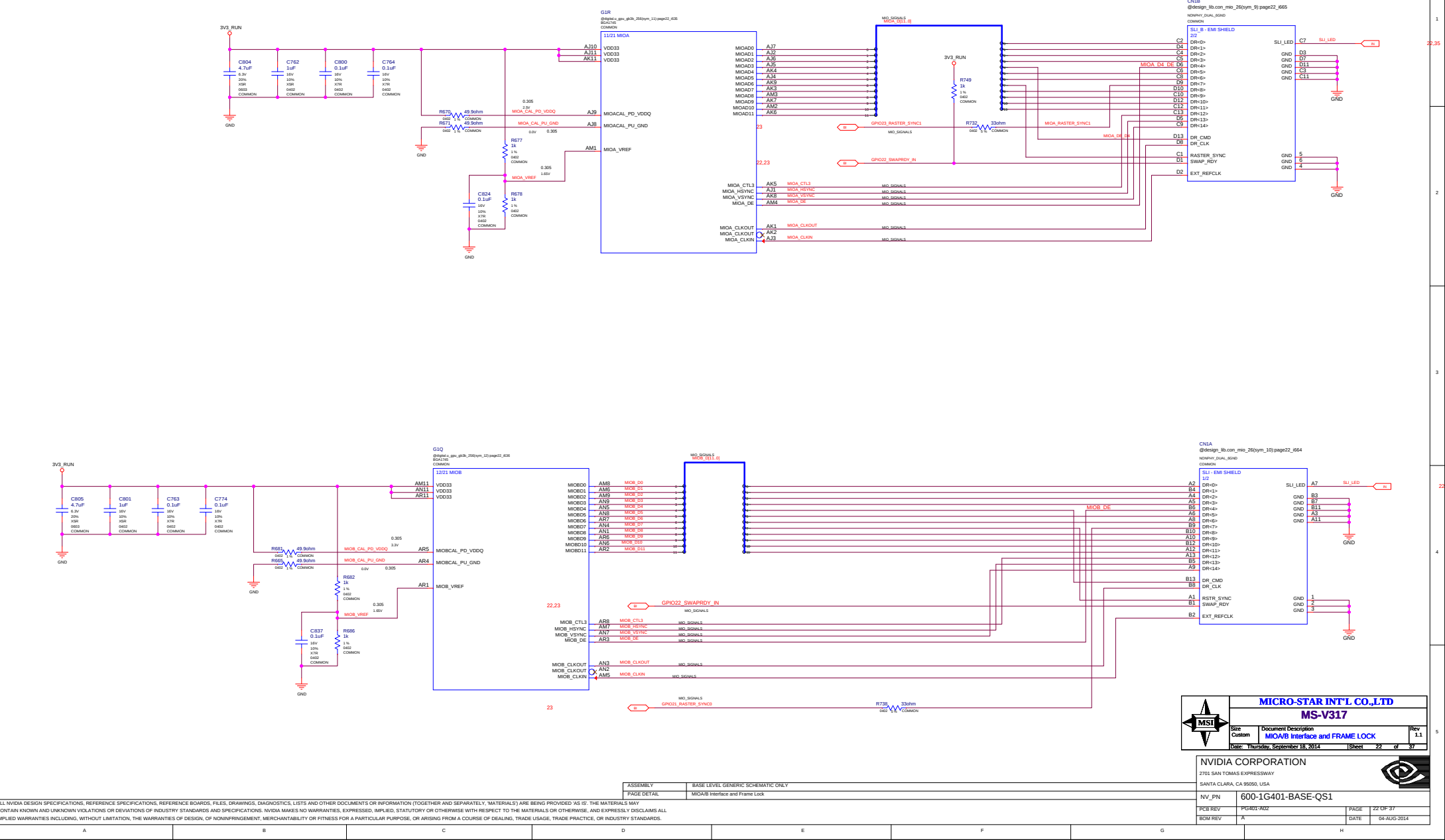


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1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



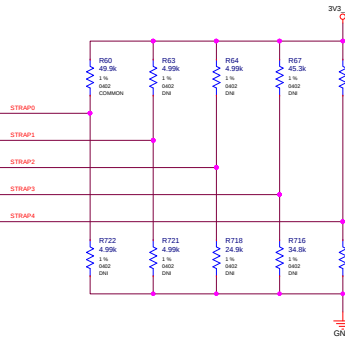
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PAGE DETAIL	IFPD DP



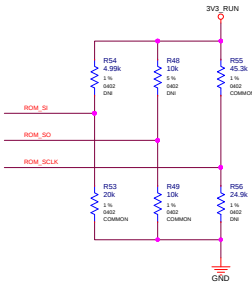
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KEPLER				MAXWELL			
STRAP0	USER_BIT [3:0]*	0000*	5K PD*	GC6	SEE TABLE BELOW		
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Developer*				
STRAP2	PCI_DEVID [3:0]*	0100 - (0x1184)*	25K PD - 425 GPU*				
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*				
STRAP4	DP_PLL_VDD_33V*	1*	FOR 3_3V*				
	PEX_MAX_SPEED*	1*	FOR GEN2/3*				
	PEX_SPD_CHANGE_GEN3*	1*	ENABLED*				
	*						
ROM_SI	RAMCFG[0]*	2*		RAMCFG[0]*	2*		
	RAMCFG[1]*	1*	0111 for 64Mx32 256-bit SAMSUNG SAMSUNG for SKH 0 primary memory	RAMCFG[1]*	1*		20K PD*
	RAMCFG[2]*	1*	45K PD*	RAMCFG[2]*	0*		
	RAMCFG[3]*	0*		RAMCFG[3]*	0*		
ROM_SO	VGA_DEVICE*	1*		VGA_DEVICE*	1*		
	SMB_ALT_ADDR*	0*	30K PD*	SMB_ALT_ADDR*	0*		10K PD*
	FB[0]_APERTURE_SIZE*	1*	For 128MB*	PCIE_CFG*	0*		
	FB[1]_APERTURE_SIZE*	0*	For 128MB*	DEVID_SEL*	0*		
ROM_SCLK	PEX_PLL_EN_TERM100*	0*	DISABLED*	SOR0_EXPOSED*	1*		
	PCI_DEVID_EXT[5]	0*	For 0x1184*	SOR1_EXPOSED*	1*		45K PU*
	SUB_VENDOR*	1*	Dedicated BIOS*	SOR2_EXPOSED*	1*		
	PCI_DEVID_EXT[4]*	0*	For 0x1184*	SOR3_EXPOSED*	1*		

MULTI_STRAP_REF0_GND	
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	45.3K 1% TO GND



MAXWELL		
STRAP0	STRAP1	STRAP2
3.3V	1.65V	0V
GC6P ISLAND ENABLED	GC6P DEBUG MODE	GC6P ISLAND DISABLED



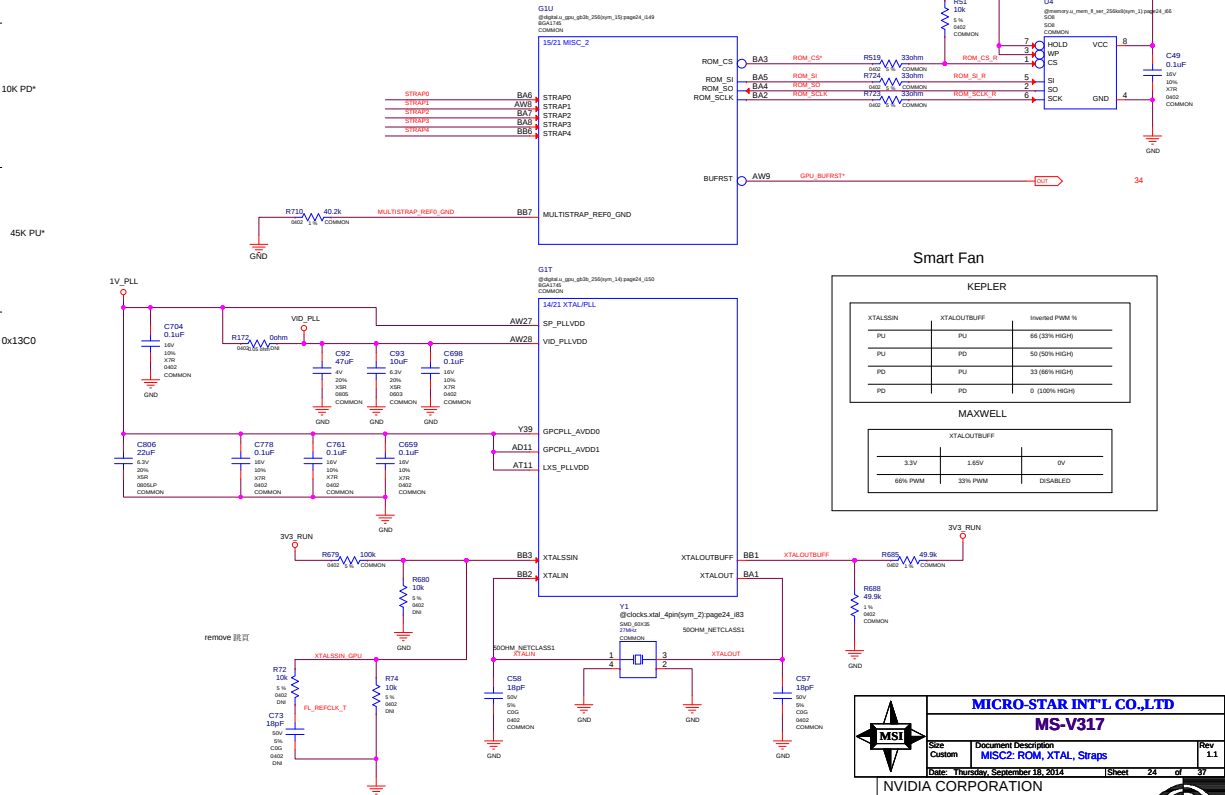
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5K	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

KEPLER

CFG[3:0]	Config	Width	Vendor
0000	Reserved		
0001	32Mx32 256-bit Elpida		
0010	32Mx32 256-bit Hynix		
0011	32Mx32 256-bit Samsung		
0100	Reserved		
0101	64Mx32 256-bit Elpida		
0110	64Mx32 256-bit Hynix		
0111	64Mx32 256-bit Samsung		
1000	Reserved		
1001	32Mx32 192-bit Elpida		
1010	32Mx32 192-bit Hynix		
1011	32Mx32 192-bit Samsung		
1100	Reserved		
1101	64Mx32 192-bit Elpida		
1110	64Mx32 192-bit Hynix		
1111	64Mx32 192-bit Samsng		

MAXWELL

CFG[3:0]	Config	Width	Vendor
0000	Reserved		
0001	128Mx32 256-bit Elpida		
0010	128Mx32 256-bit Hynix		
0011	128Mx32 256-bit Samsung		
0100	Reserved		
0101	64Mx32 256-bit Elpida		
0110	64Mx32 256-bit Hynix		
0111	64Mx32 256-bit Samsung		



Smart Fan		
KEPLER		
XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (50% HIGH)
PD	PD	50 (50% HIGH)
PD	PU	33 (50% HIGH)
PD	PD	0 (50% HIGH)
MAXWELL		
XTALOUTBUFF		
3.3V	1.65V	0V
66% PWM	33% PWM	DISABLED



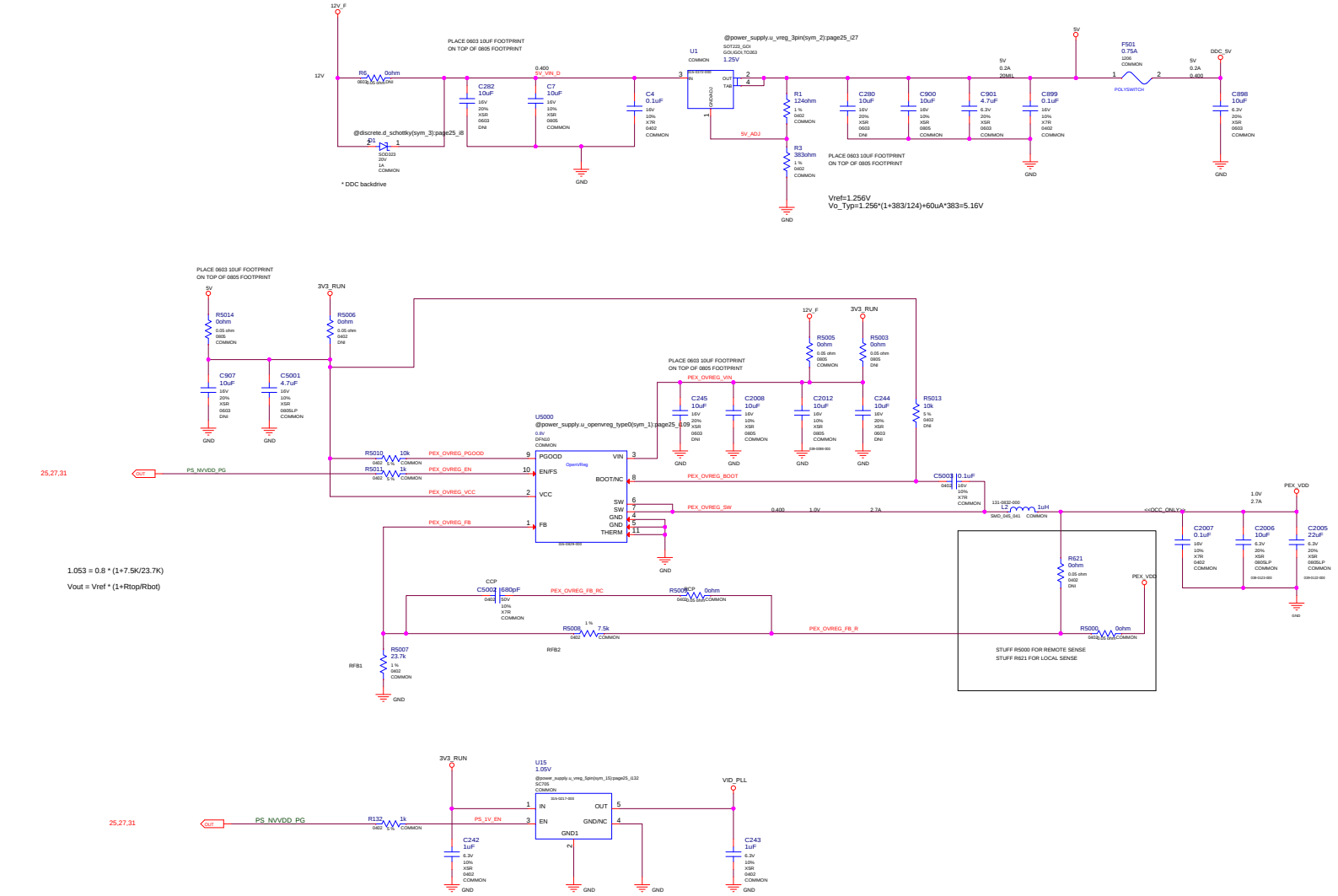
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PAGE DETAIL	PS: 5V, PEX_VDD

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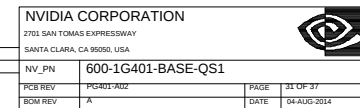
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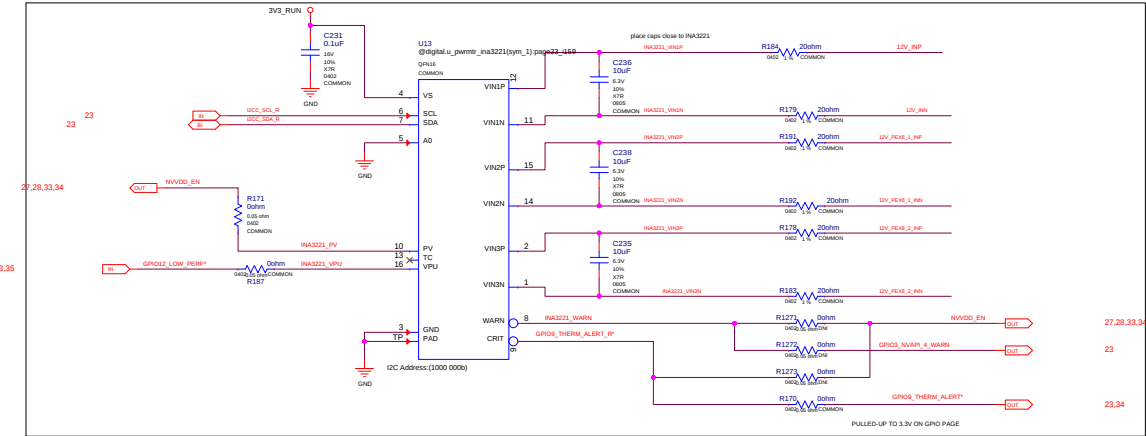
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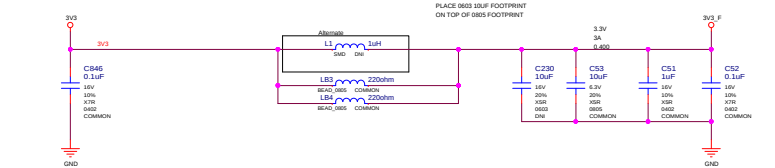
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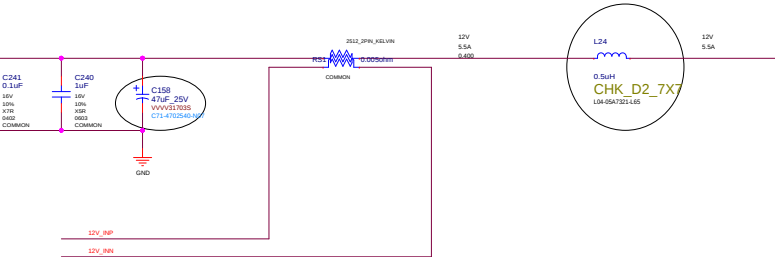
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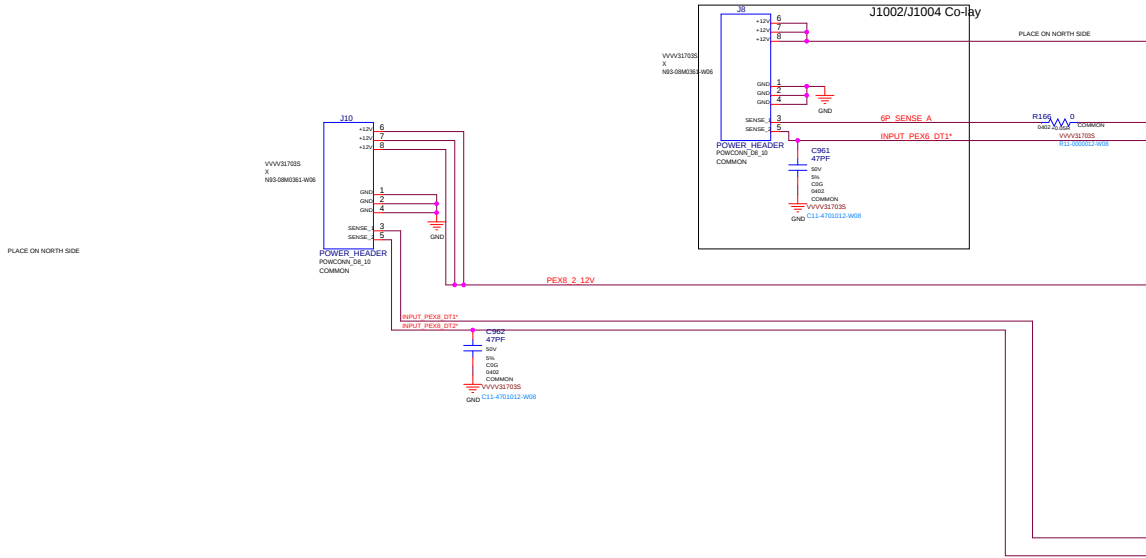
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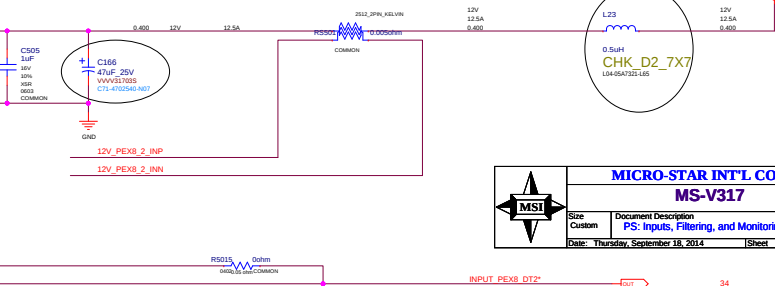
PEX_12V INPUT - 66W



PEX6 INPUT 1 - 2x3 PCIe CON 75W



PEX8 INPUT 2 - 2x4 PCIe CON 150W



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INV_PN	600-1G401-BASE-QS1	
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BCOM REV	A	DATE 04-AUG-2014

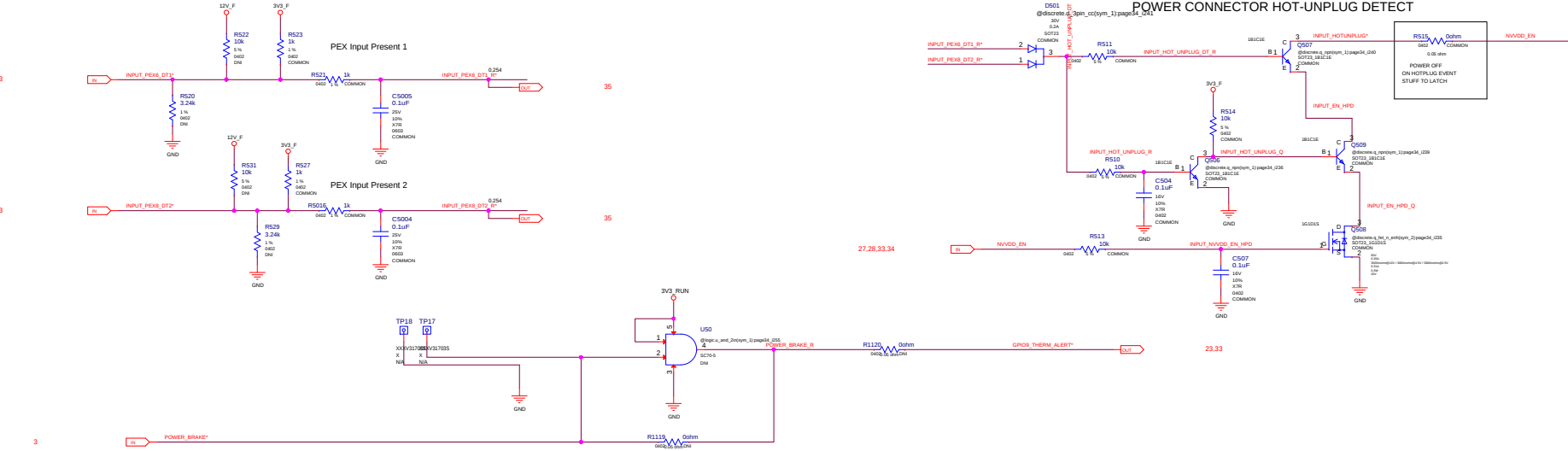
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THERM OVERT SHUTDOWN LATCH

IFP_IOVDD (backdrive prevention)

PEX Input - NVVDD Power Sequence



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PAGE DETAIL	PS: Shutdown

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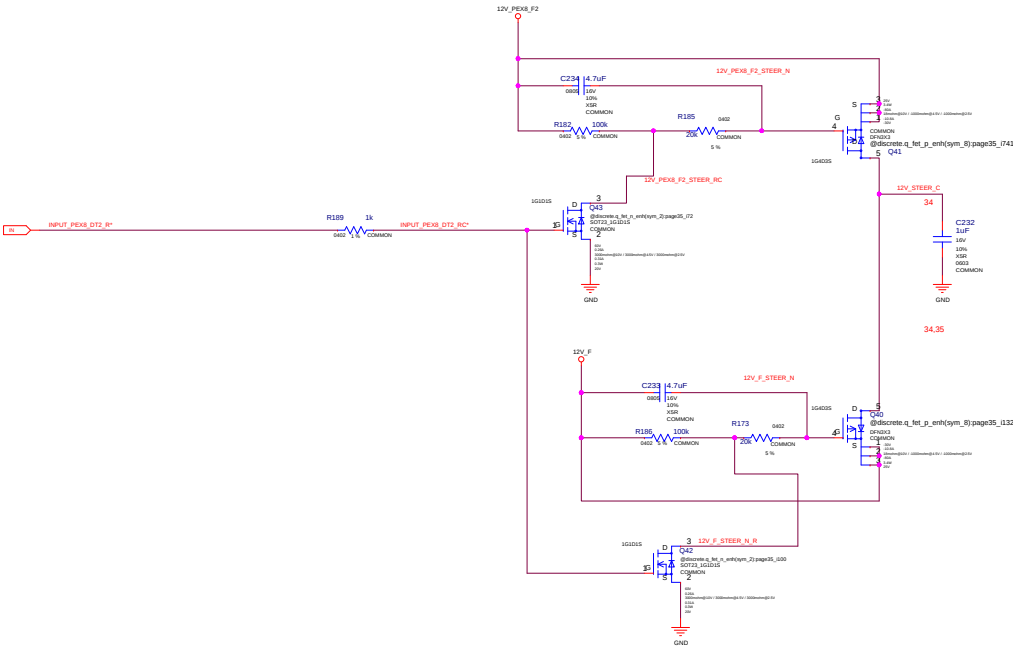
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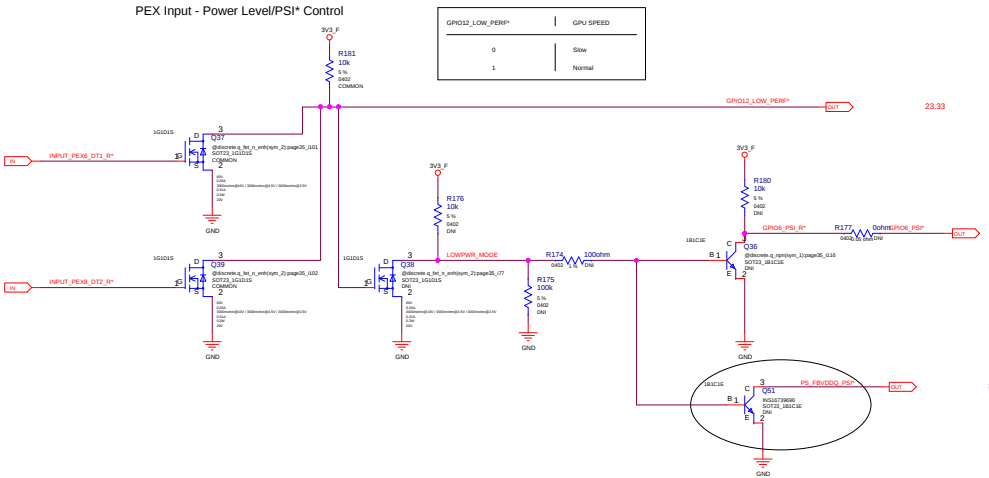
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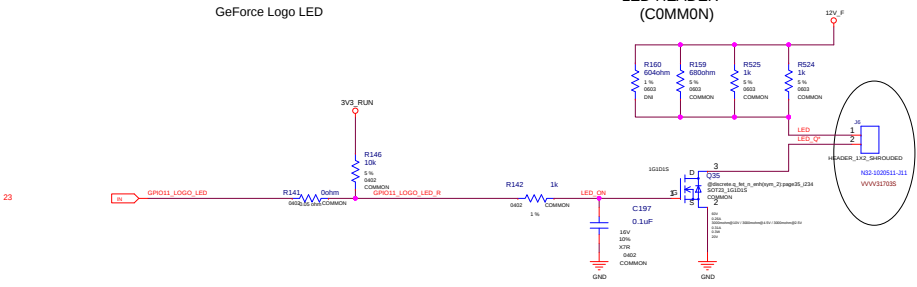
PEX Input - 12V Current Steering FETs



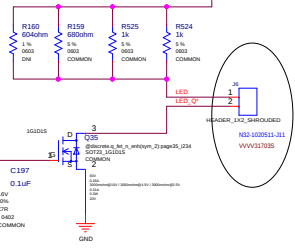
PEX Input - Power Level/PSI* Control



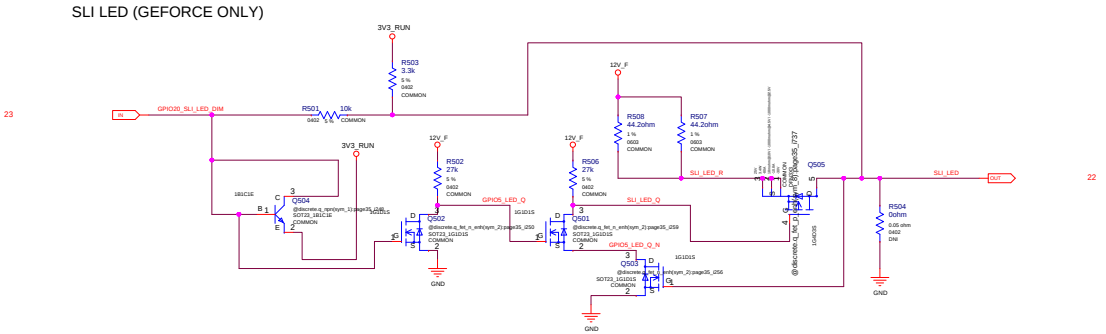
GeForce Logo LED



LED HEADER (COMMON)



SLI LED (GEFORCE ONLY)



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Document Description 12V Current Steering, PSI Control, and LED

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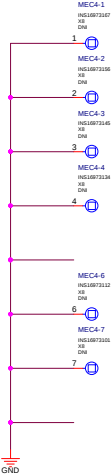
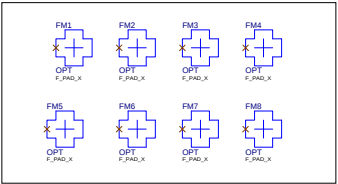
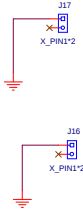
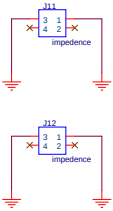
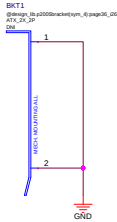
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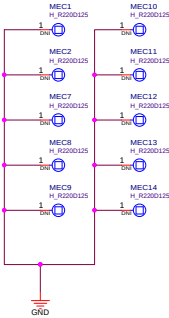
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Brackets:



Mechanical Holes Symbol



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- Page37:
- 1.P17 增加DVI ESD
 - 2.P18~P21 修改HDMI,DP footprint, 增加HDMI ESD
 - 3.简化S L I 線路
 - 4.移除原本FBVDDQ線路
 - 5.P27~P30 更換NVVD 線路
 - 6.P31~32 移除dynamic power circuit/增加風扇7511線路
 - 7.P33 更換反插8PIN,Input choke
 - 8.P35 增加MEM PSI 晶體
 - 9.Remove MICROCONTROLLER



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