

PG301 A02

Comanche 192b GDDR5, <150W, 2-way SLI
Tall DVI-I + DP + DP + DP/HDMI + DP

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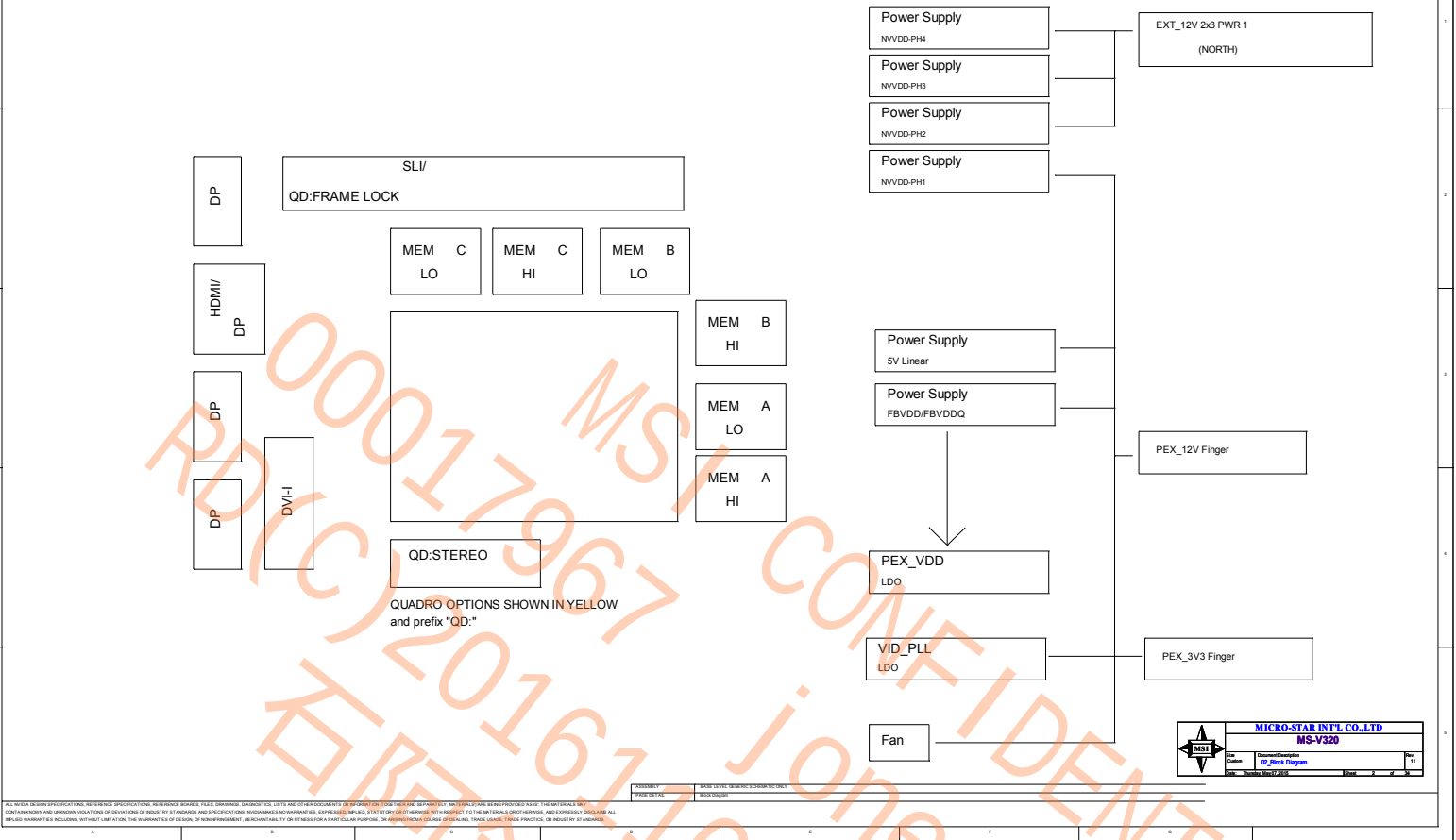
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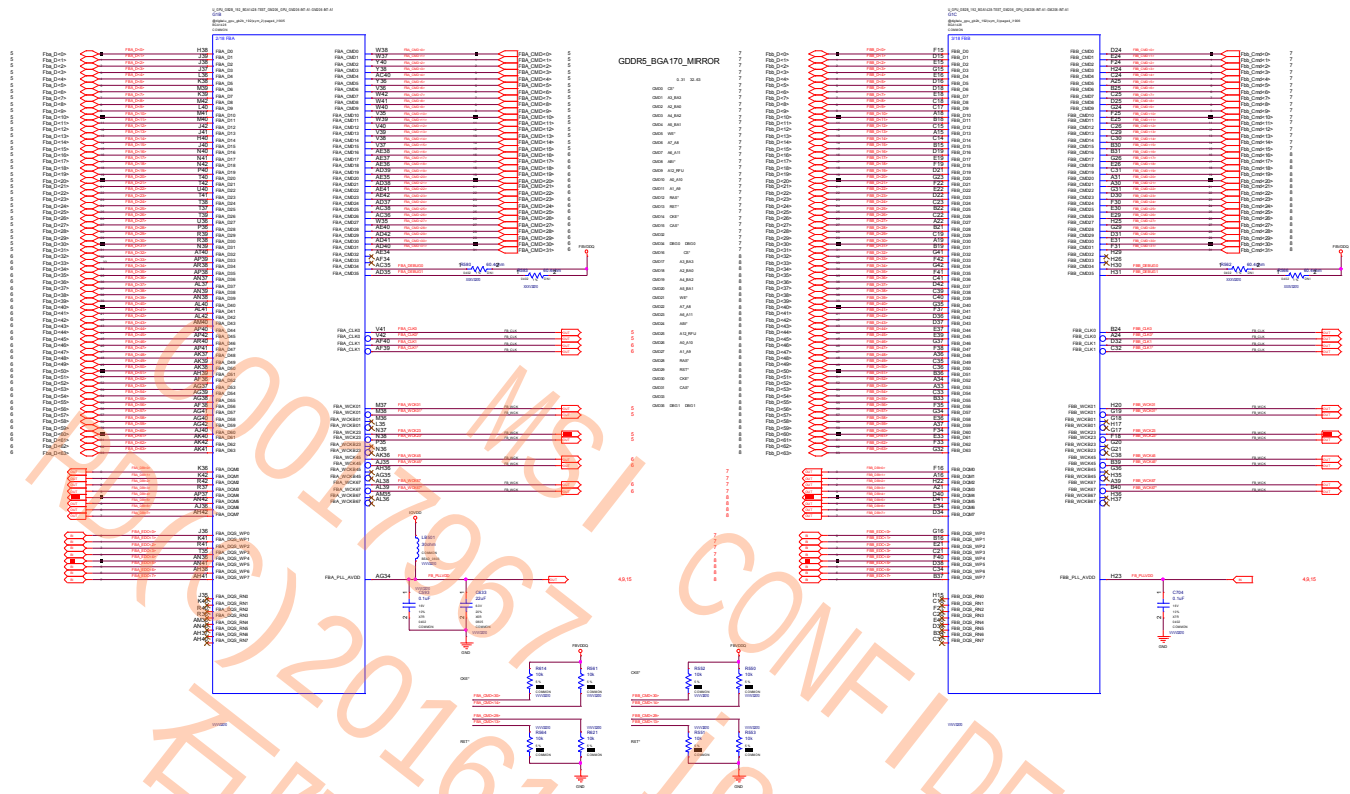
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- 2 page:8 增加跨頁符號
- 3 page:15 修改DVI footprint
- 4 page:16/17/19 修改DP footprint
- 5 page:18 修改HDMI footprint
- 6 page:26/27 修改output chike footprint



ASSEMBLY: 100017967
PRODUCT: 10802

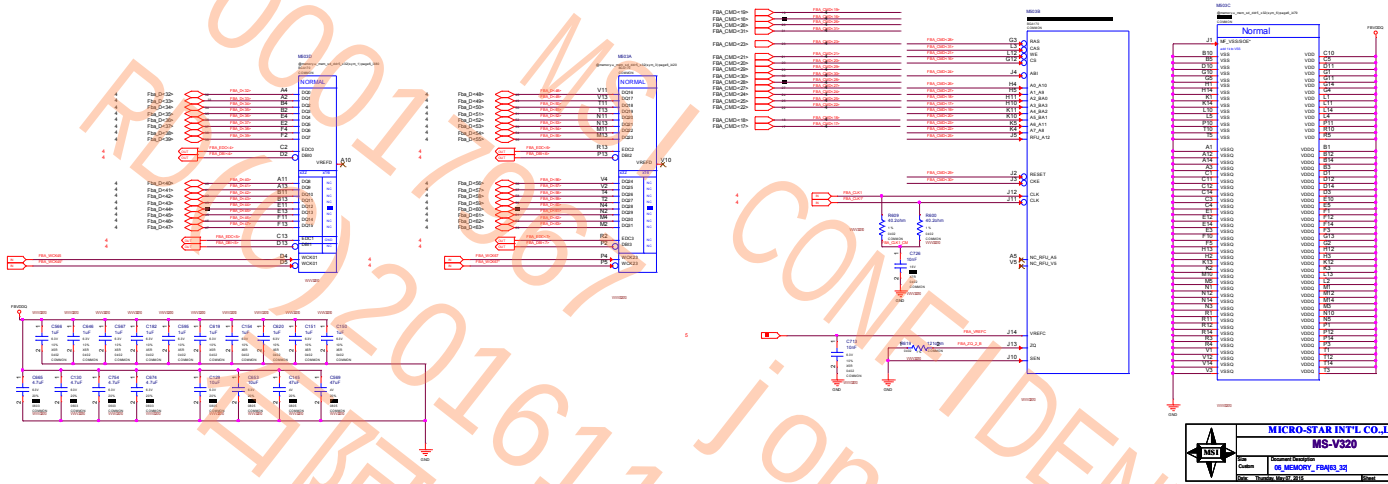
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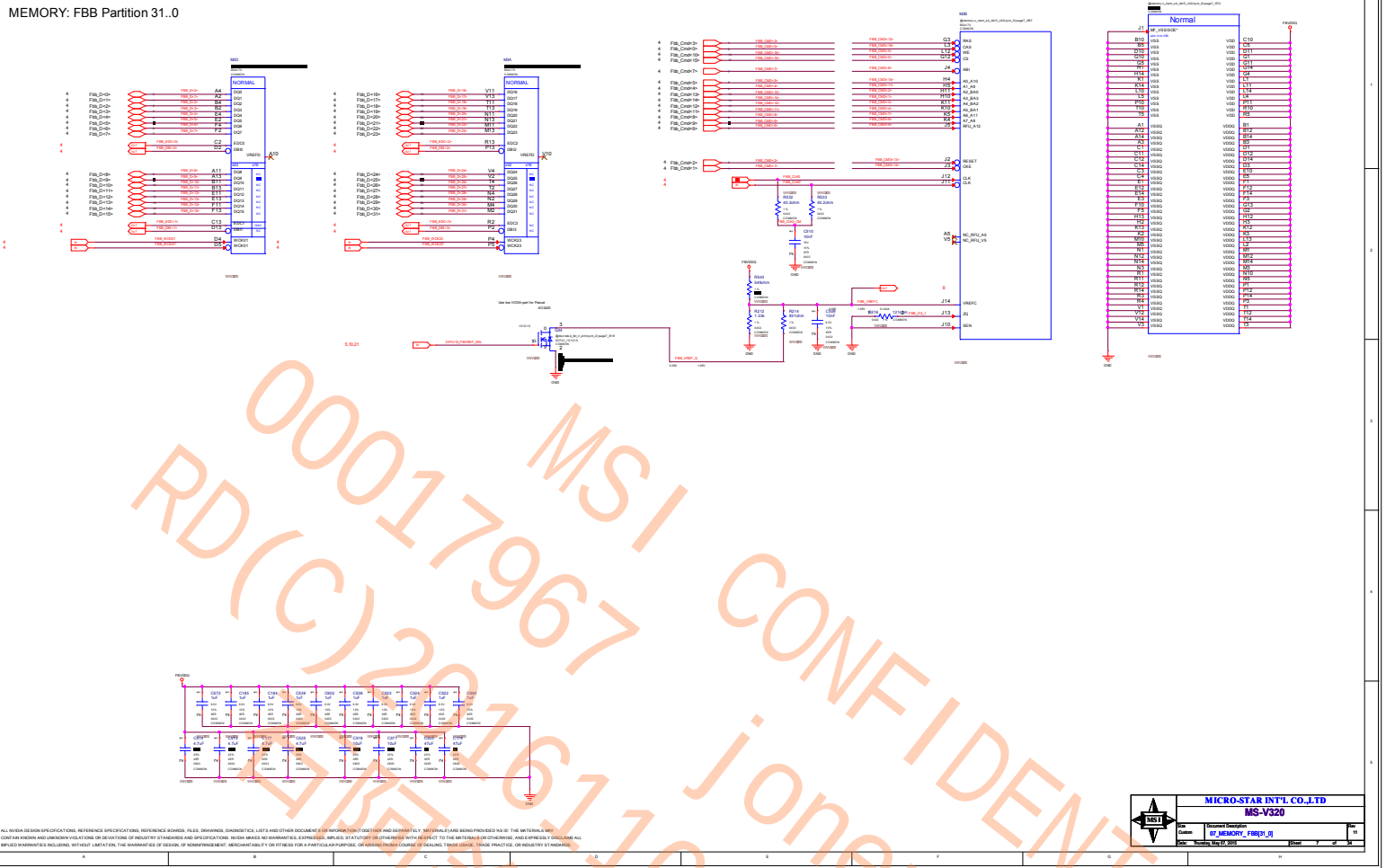


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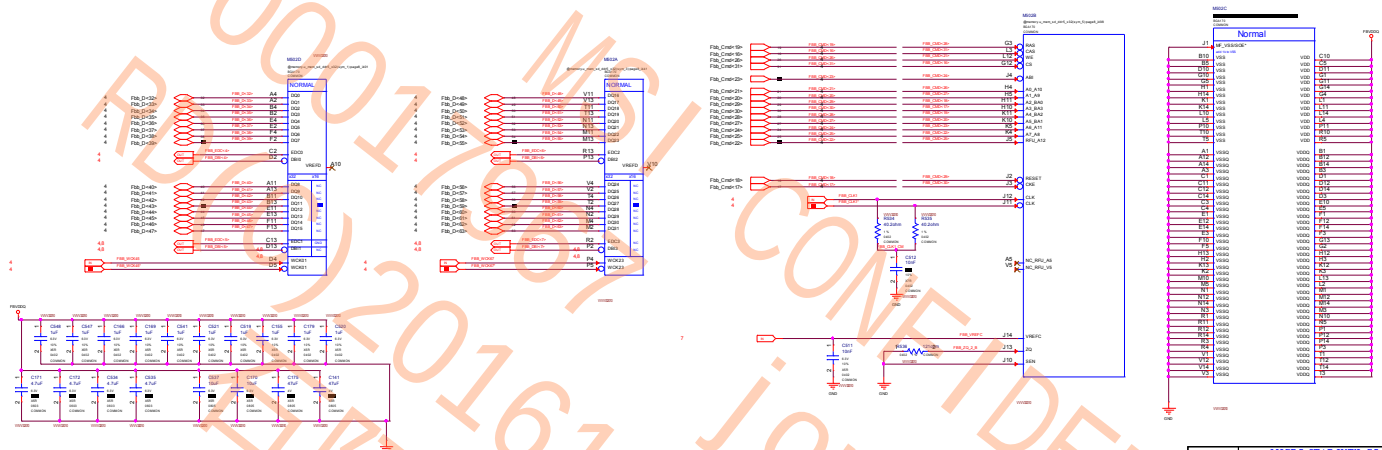


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MS-V320	
Doc No.	01_MEMORY_FBBP_01
Rev.	1.0
Date	2016.11.08
By	W. H. H. H.
Check	W. H. H. H.
Appr.	W. H. H. H.



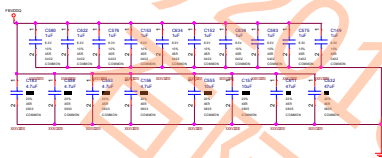
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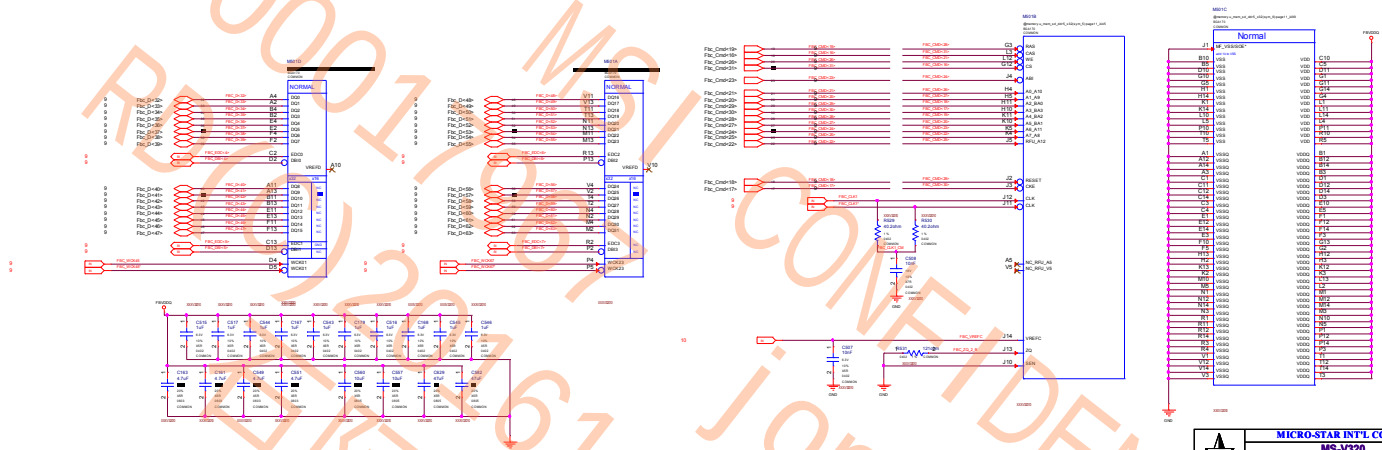
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MS-V320

Product Description

Memory Partition 63..32





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Rev: 1.0

DATE: 2008.05.20

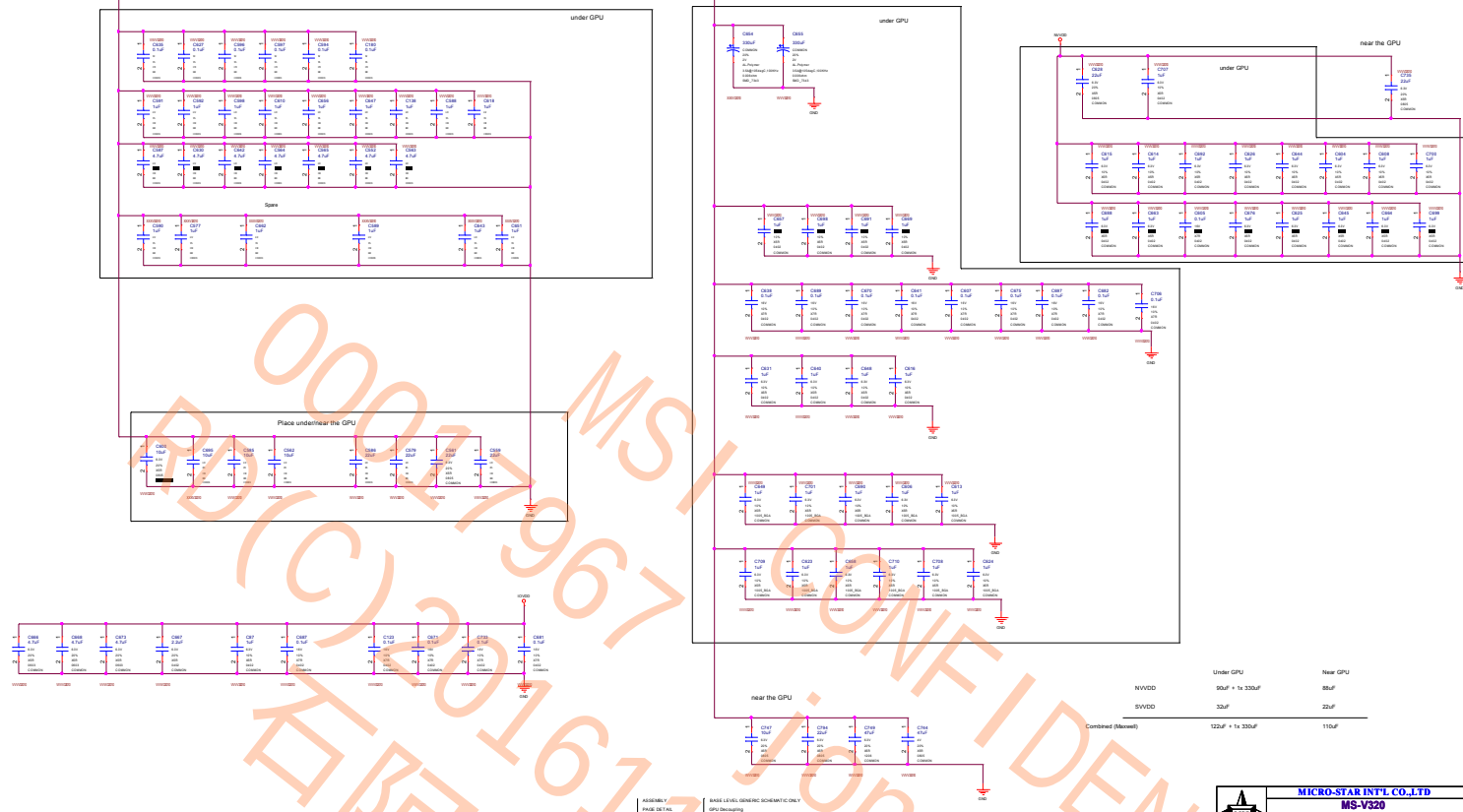
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GPU Decoupling

FBVDDQ

NVVDD



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ASSEMBLY

PAGE 01/01

POWER LEVEL SCHEMATIC ONLY

GPU Decoupling



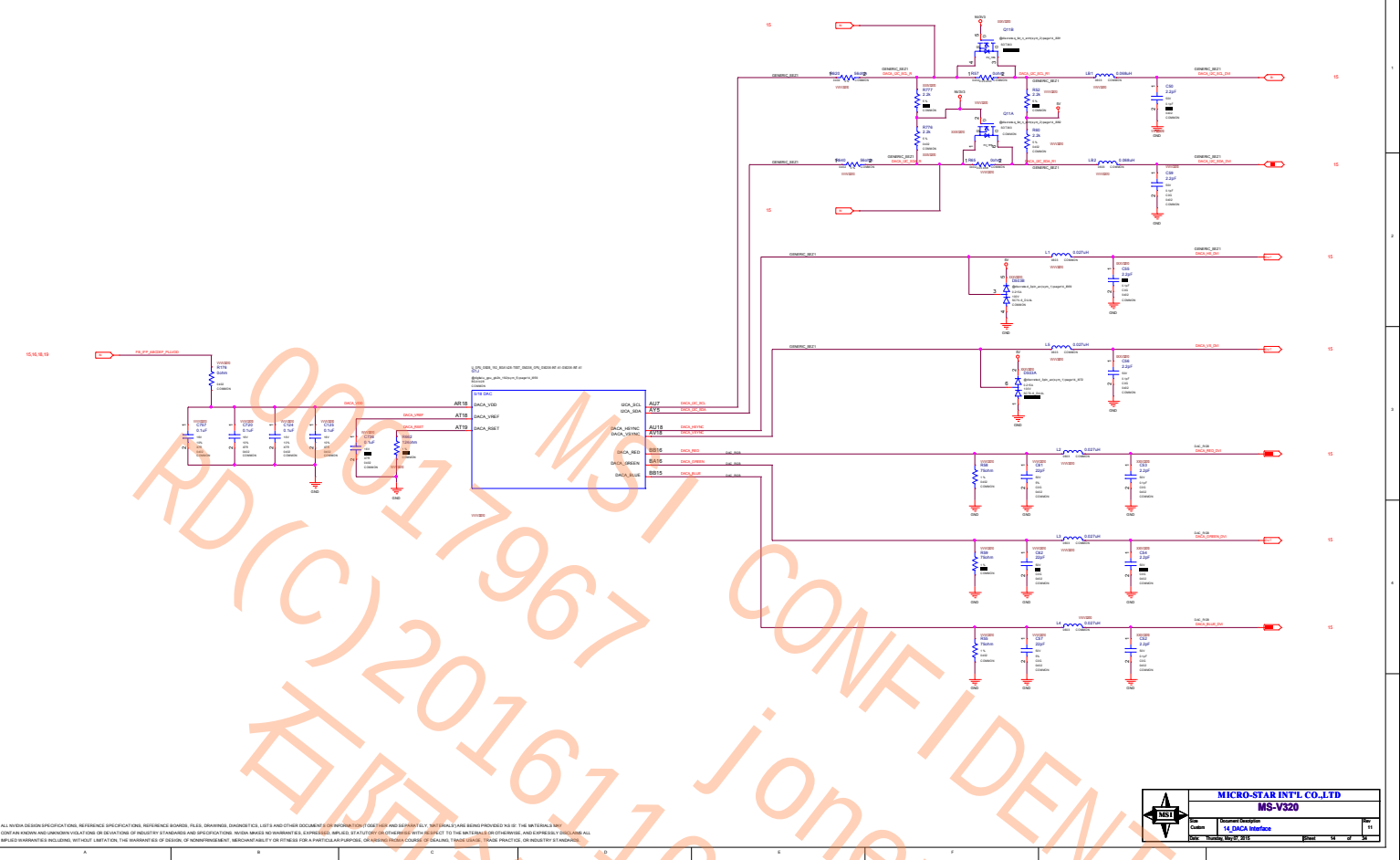
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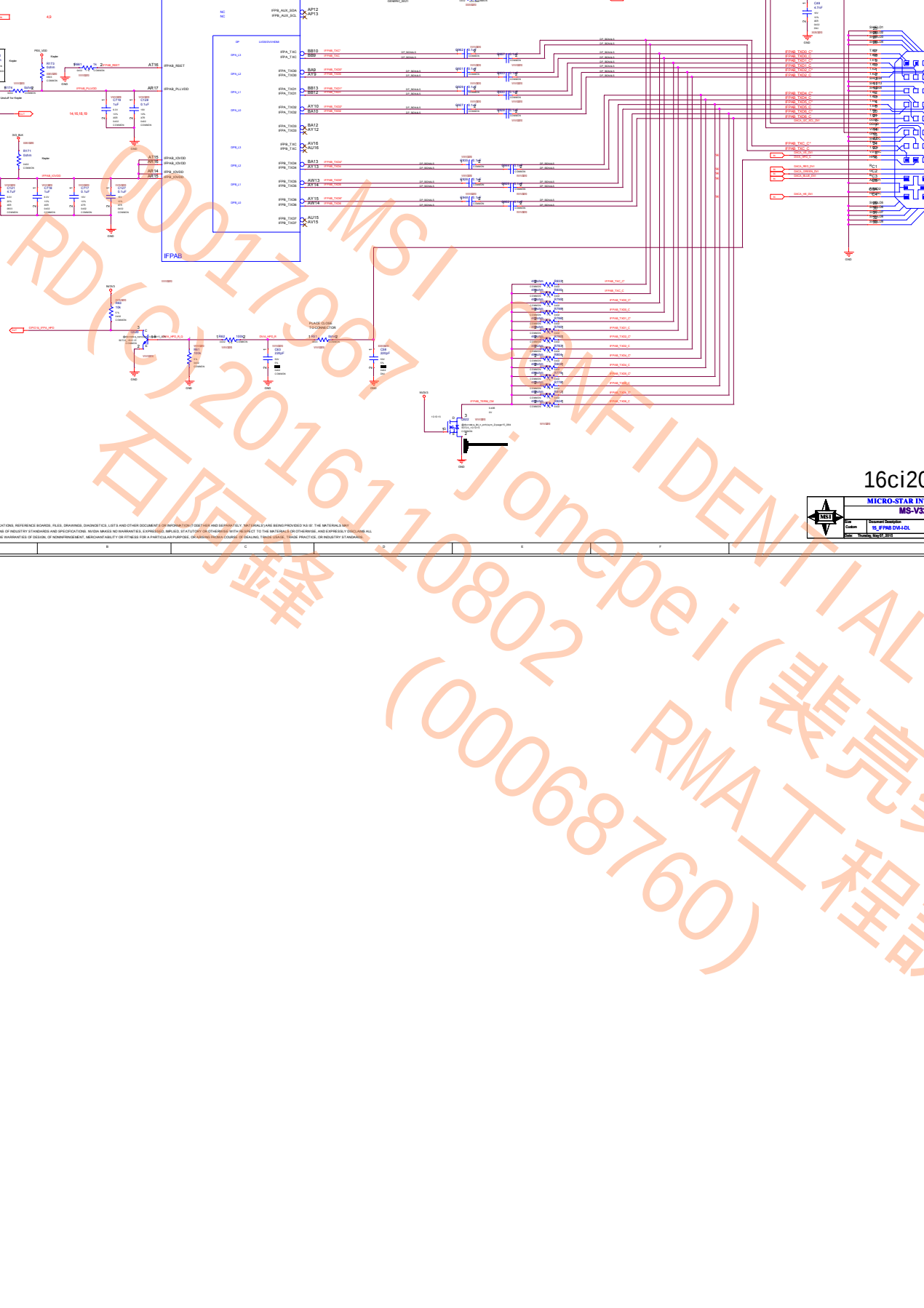
MS-V320

Date: 2019.12.11

13_GPU Decoupling

Rev: 01



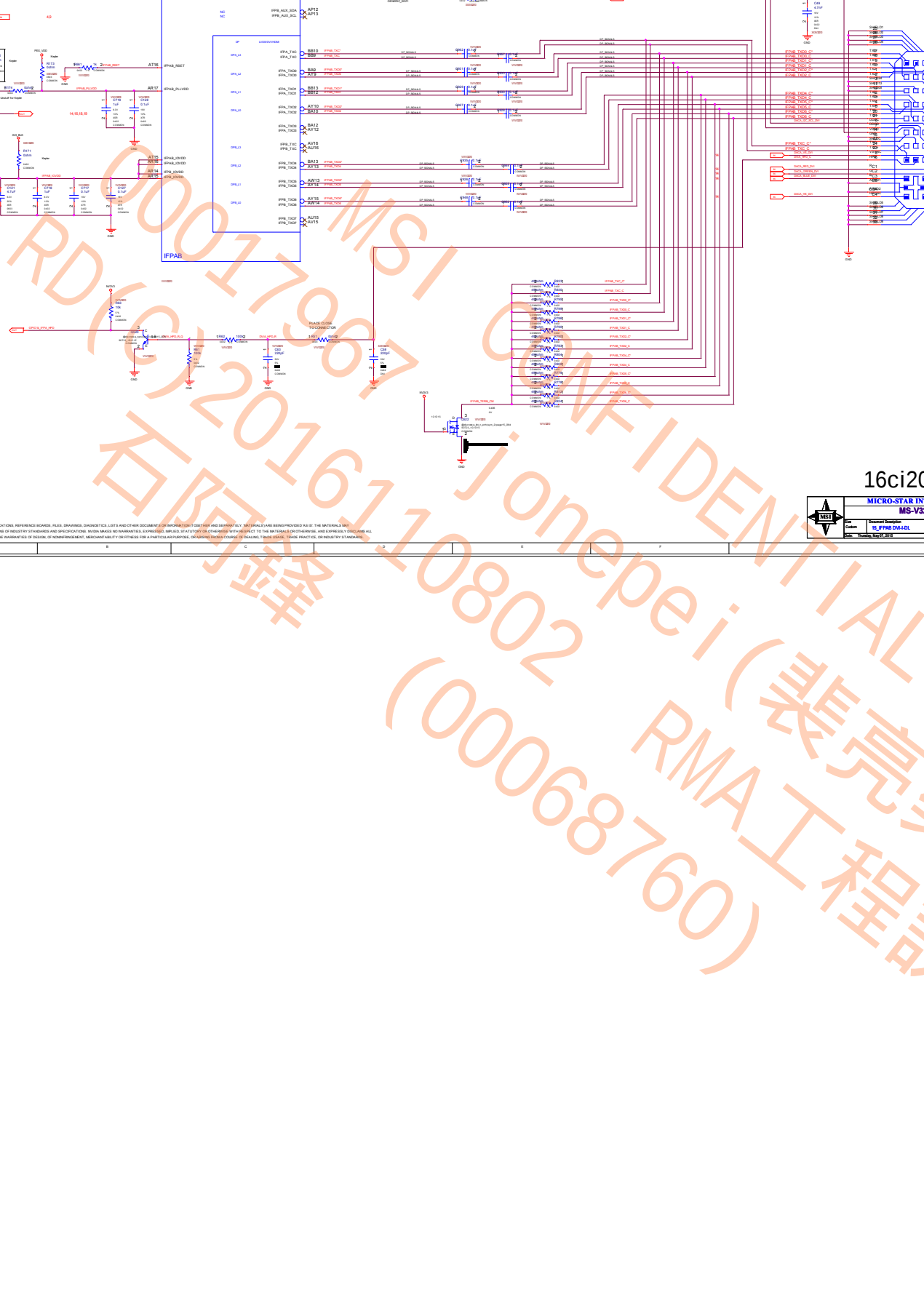


16ci20

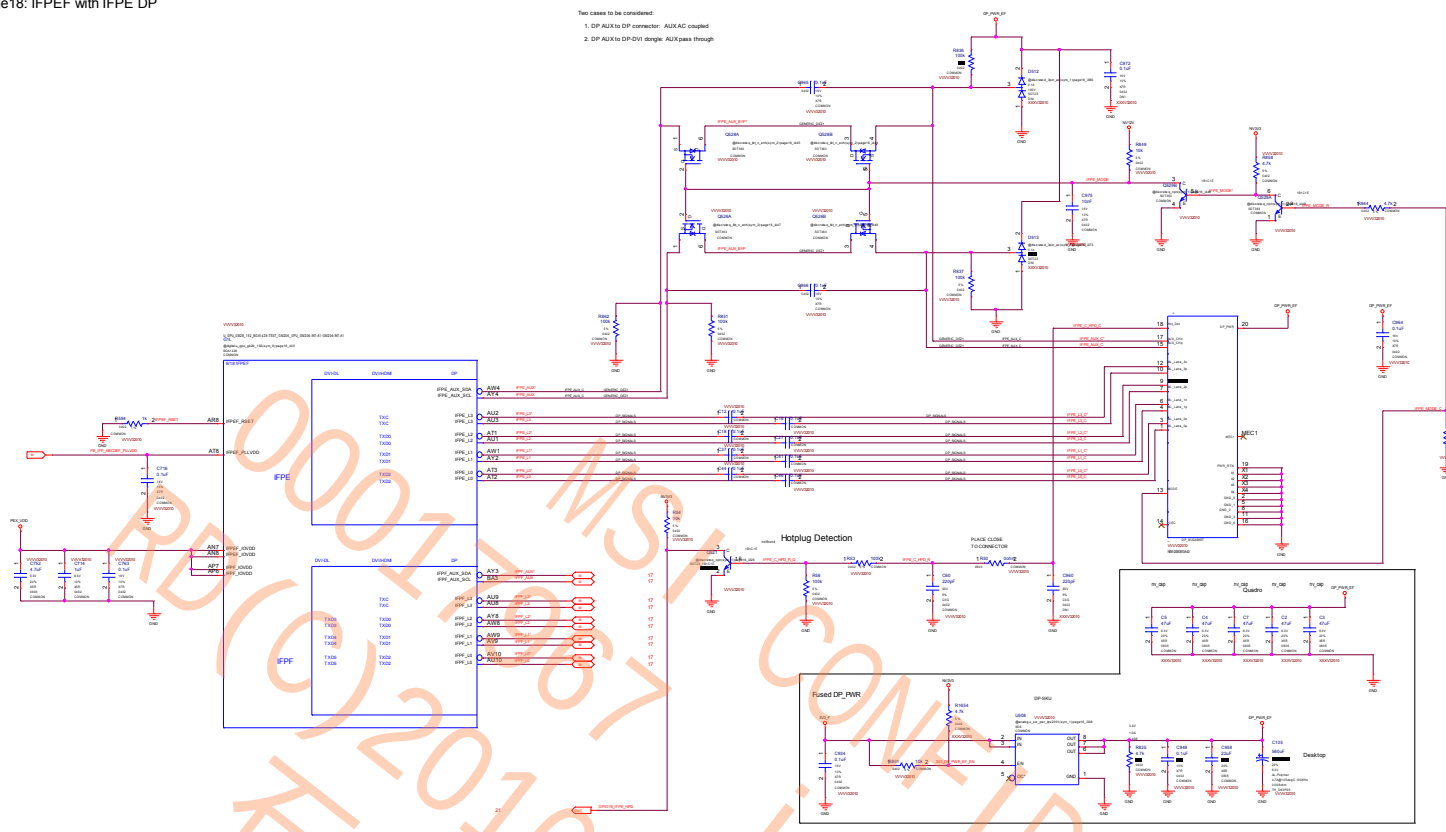
MICRO-STAR INTERNATIONAL
MS-V3

Component Location
16ci20-DIG-01

Component	Location
16ci20-DIG-01	16ci20-DIG-01



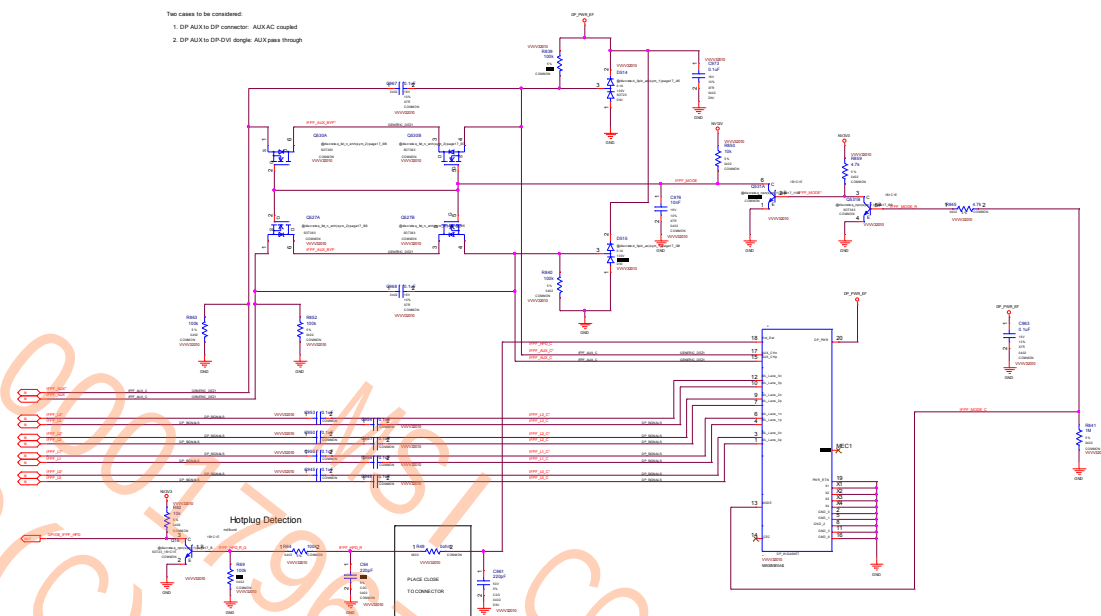
Two cases to be considered:
1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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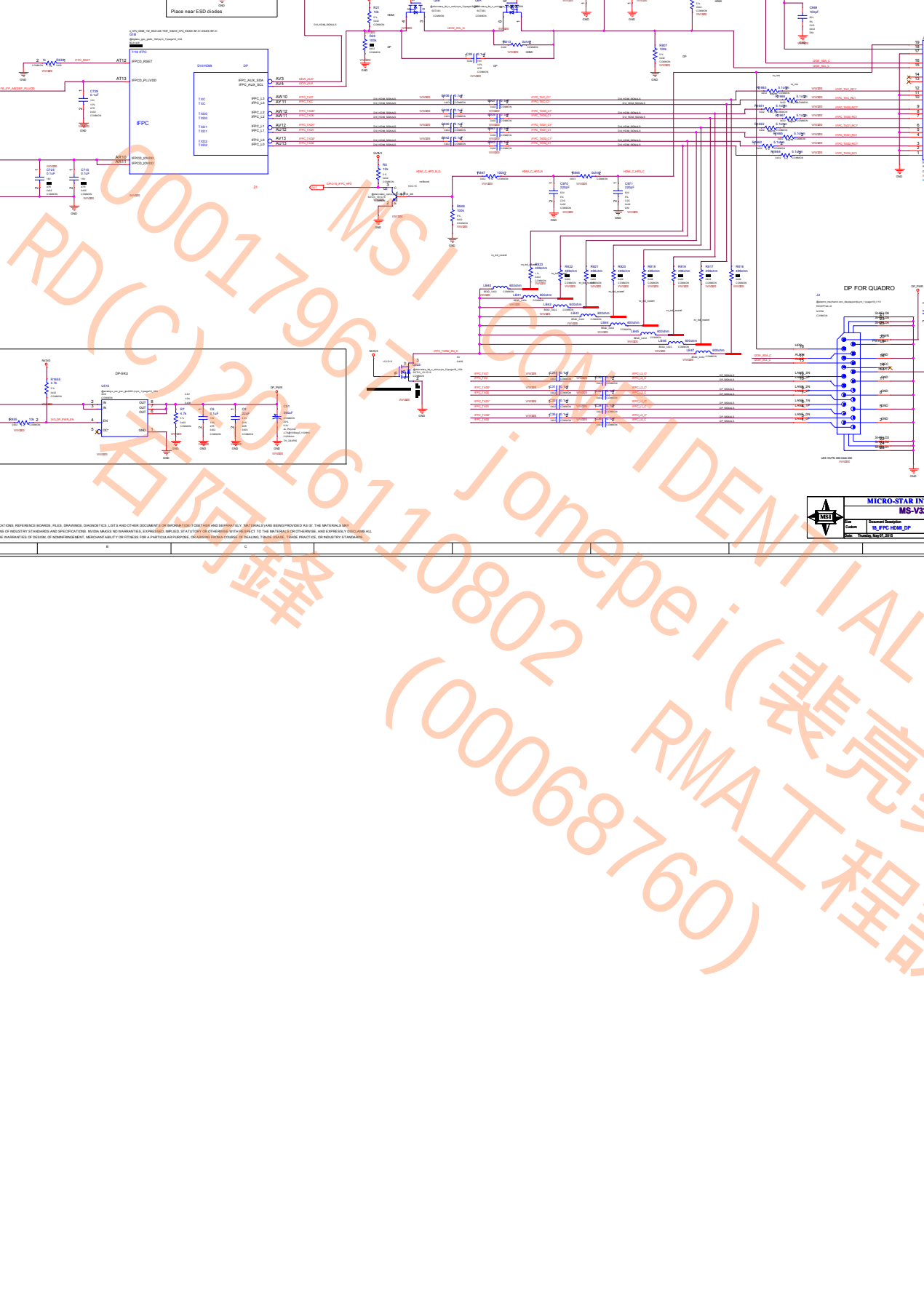
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MS-V320
Version: 1.0
Date: 2016/11/10
Author: RMA Engineering

- Two cases to be considered:
1. DP AUX to DP connector: AUXAC capped
 2. DP AUX to DP-DVI single: AUX pass through



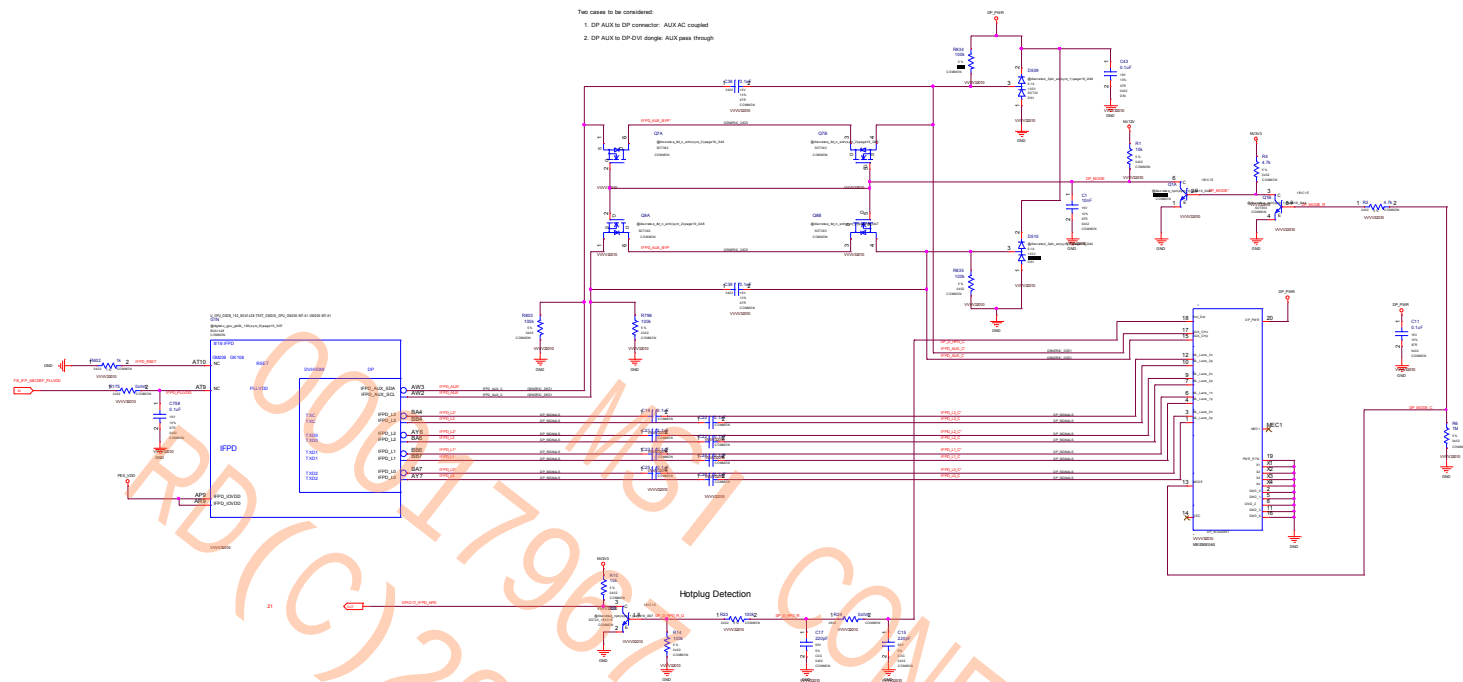
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Doc	01
Rev	01
Doc	01



Two cases to be considered

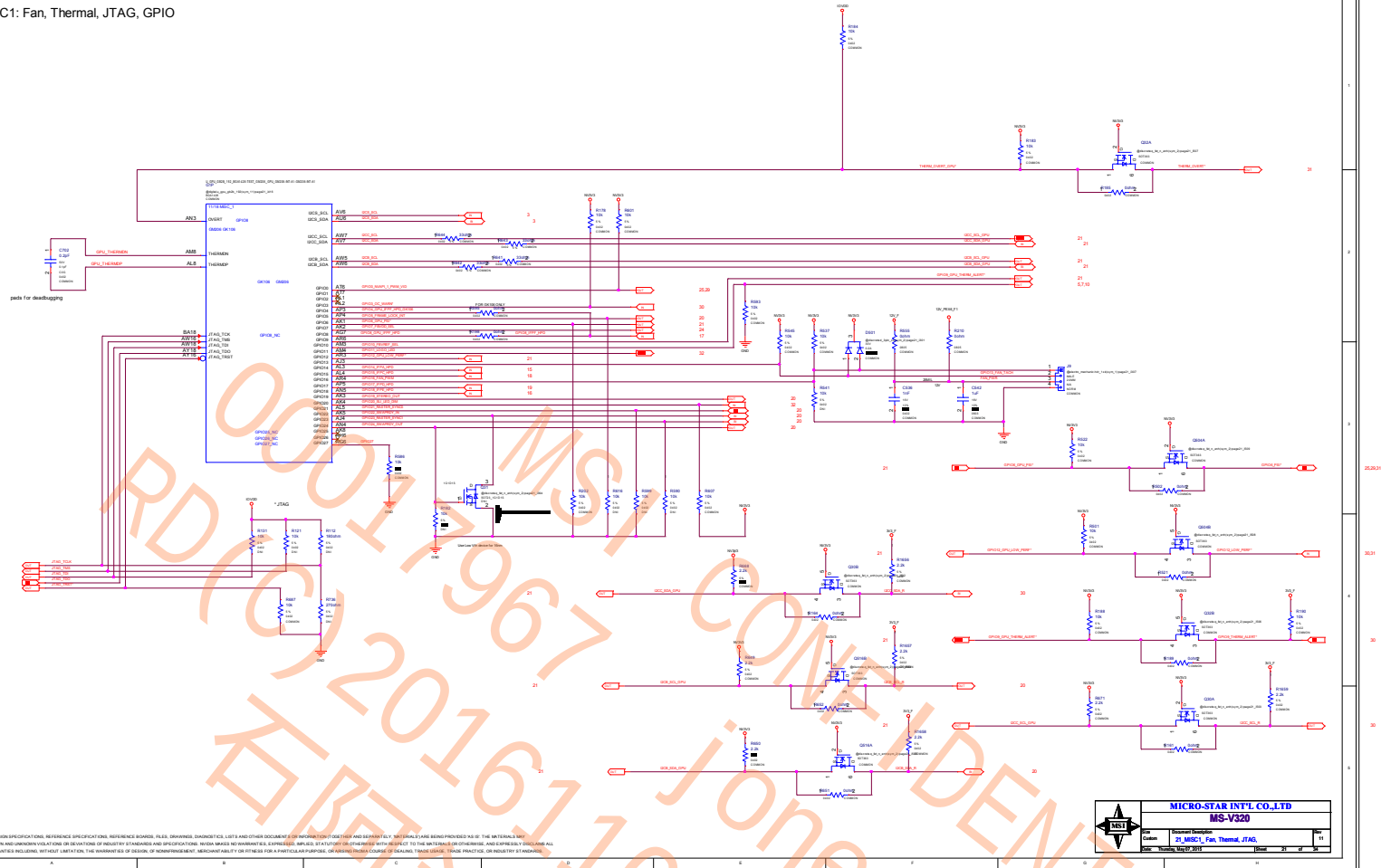
1. DP AUX to DP connector: AUXAC coupled
2. DP AUX to DP-DVI single: AUX pass through



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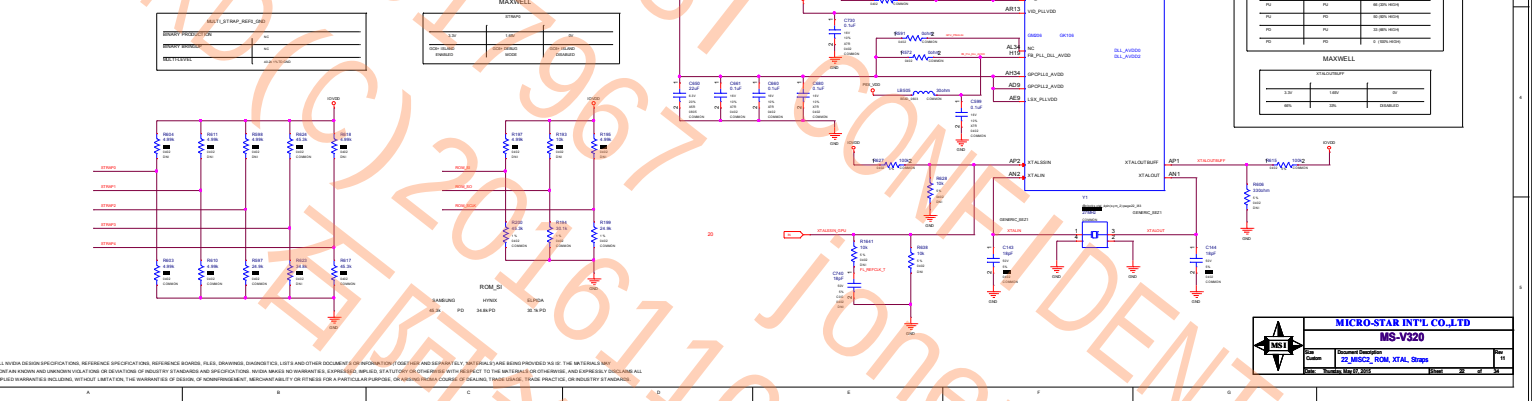
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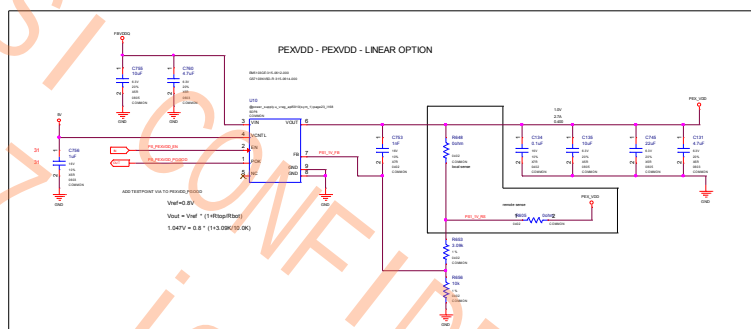
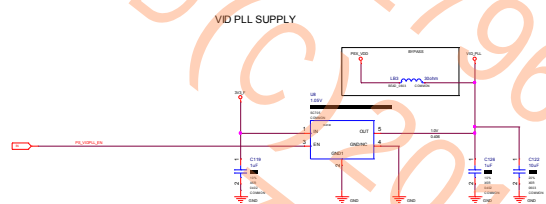
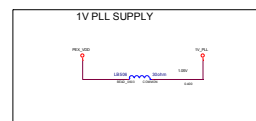
MICRO-STAR INT'L CO., LTD.	
MS-V320	
Rev	1.0
Date	2016/11/10
By	21_MISC1_Fan, Thermal, JTAG
Check	21_MISC1_Fan, Thermal, JTAG

MISC2: ROM, XTAL, Straps

	KEPLER	MAXWELL
STRAP0	USER_BIT [3:0]'	
STRAP1	3IGD_PRDCFG_LUT_ADR'	
STRAP2	PO_DEV0 [3:0]'	
STRAP3	SOR0_EXPOSED [3:0]'	
STRAP4	DP_PLL_VCO_DIV'	
	PEX_MAX_SPEED'	
	PEX_SPD_CHANCE_GEN'	
ROM_S1	RAMCFG[0]'	RAMCFG[0]'
	RAMCFG[1]'	RAMCFG[1]'
	RAMCFG[2]'	RAMCFG[2]'
	RAMCFG[3]'	RAMCFG[3]'
VGA_DEVICE	VGA_DEVICE'	
SMB_ALT_ADDR	SMB_ALT_ADDR'	
FB[0]_APERTURE_SIZE	PCE_CFG'	
FB[1]_APERTURE_SIZE	DEVID_SEL'	
PO_DEV0_TERM00'	SOR0_EXPOSED'	
PO_DEV0_EXT00'	SOR1_EXPOSED'	
SUB_VENDOR	SOR2_EXPOSED'	
PO_DEV0_EXT01'	SOR3_EXPOSED'	

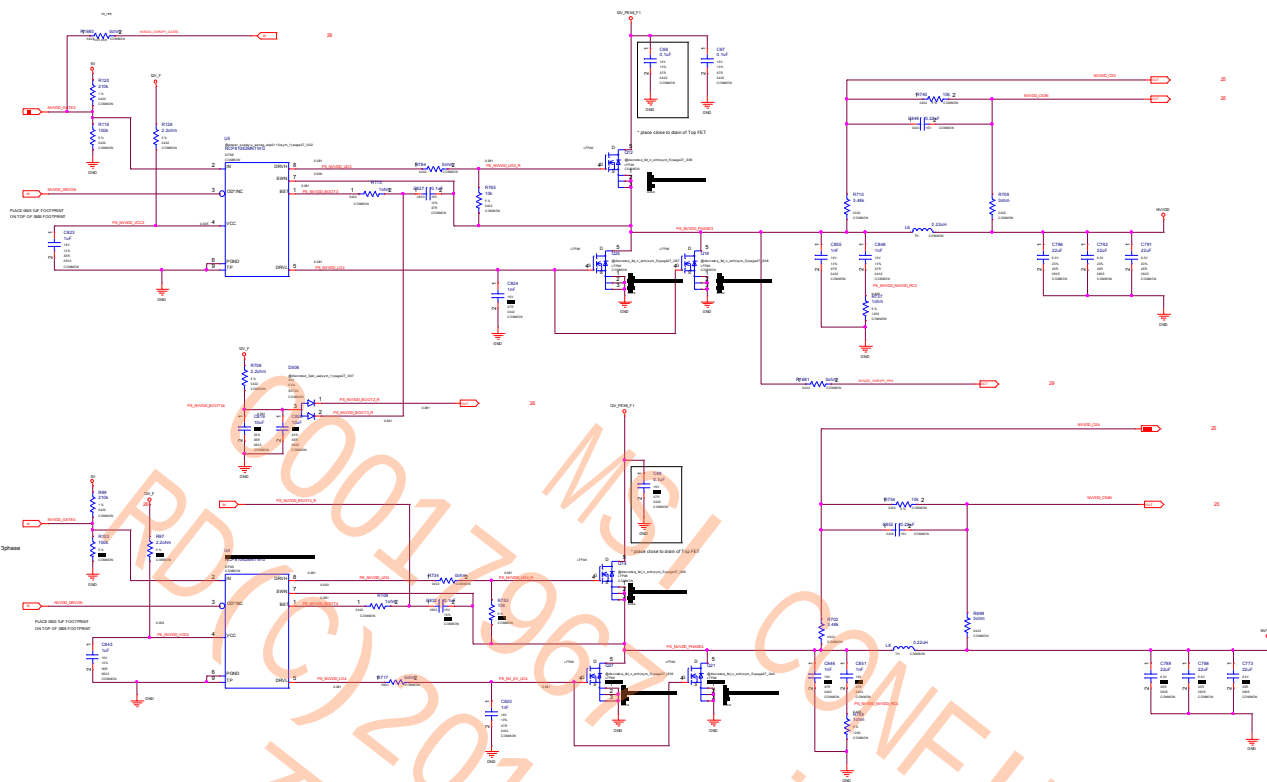
QW0	QW1
5A	0000
15A	0001
15B	0010
25A	0011
25B	0100
35A	0101
35B	0110
45A	0111





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Date Custom	Equipment Identification 24_P0_FBW0_Q	Date 11	





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Doc No.	27_PS_NVVDD Phase 3,4
Rev.	Rev. 1.0

[RESERVED]

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RD(C)2016110802 jonepei (裴亮樂)

RMA工程師 (00068760)

00017967

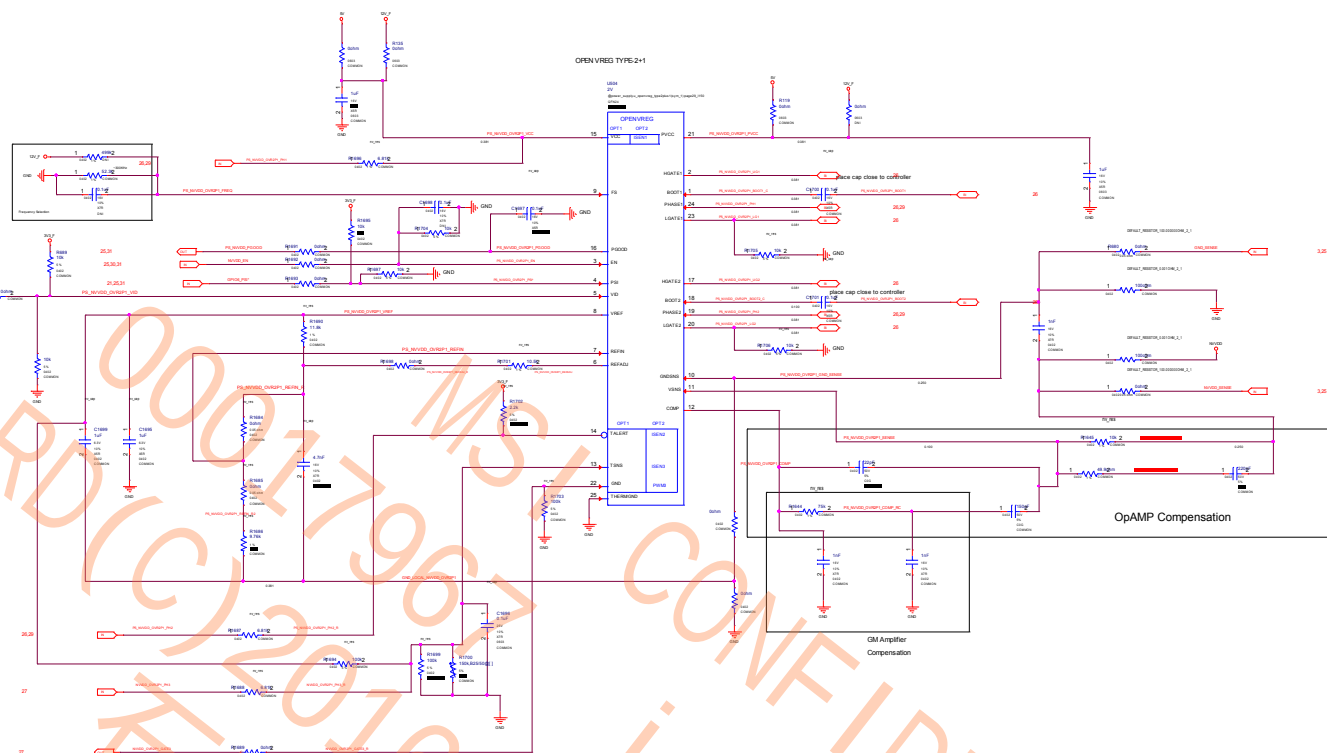
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in partnership

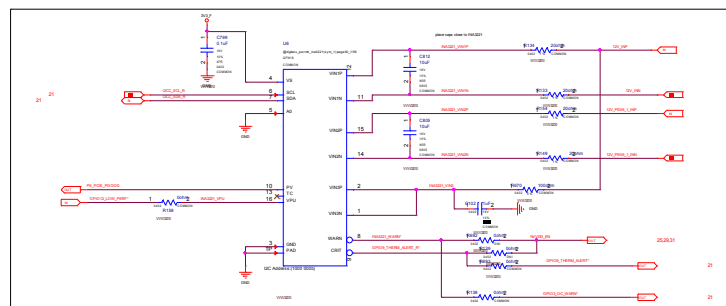
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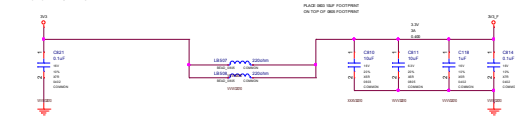
16ci203

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MS-V320	
Document Description	PS_PS_NVVDD OVR2+1 option
Version	1.0

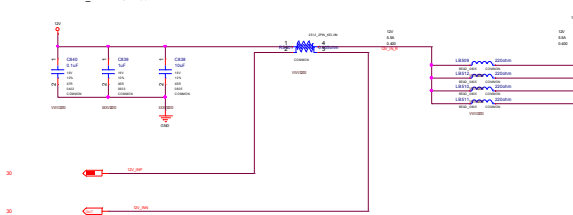
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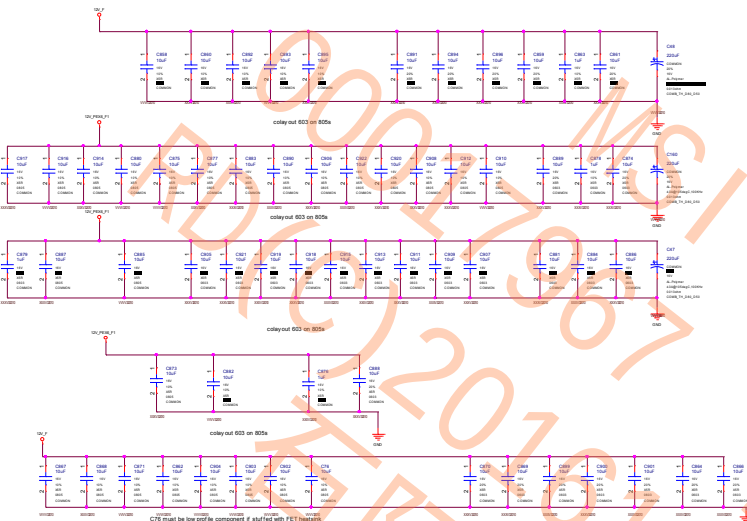
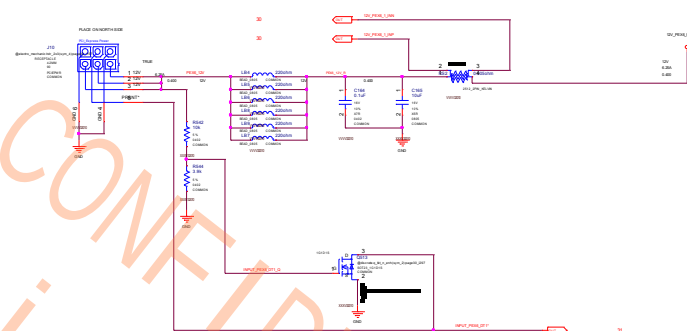
PEX_3V3 INPUT - 10W



PEX_12V INPUT - 6W



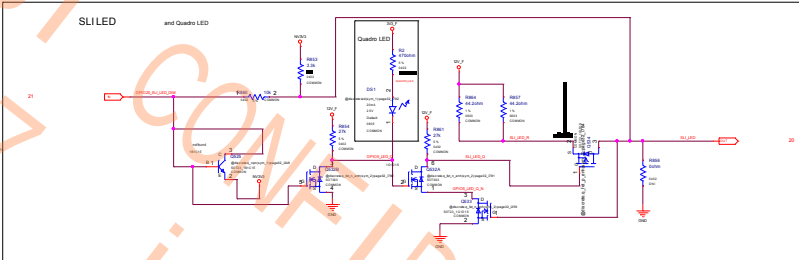
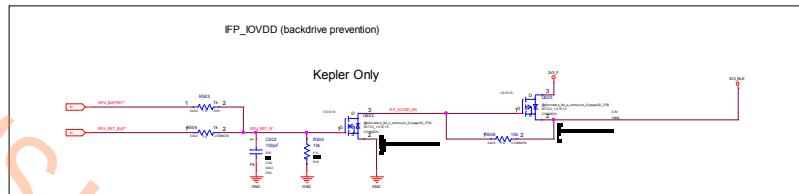
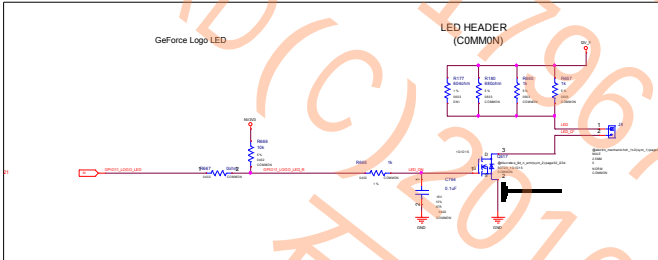
PEX_12V INPUT - 2x3 PCIe CON 75W



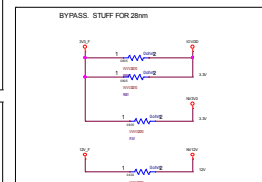
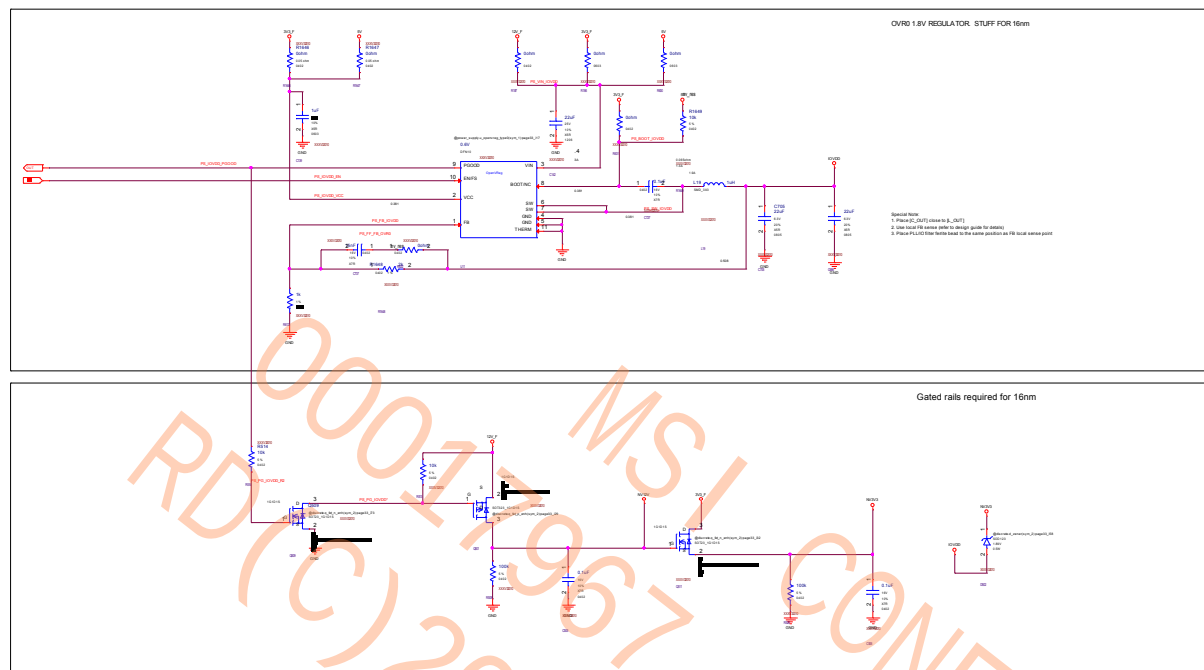
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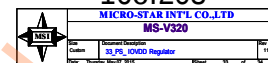




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