

PG301 A02

Comanche 192b GDDR5, <150W, 2-way SLI
Tall DVI-I + DP + DP + DP/HDMI + DP

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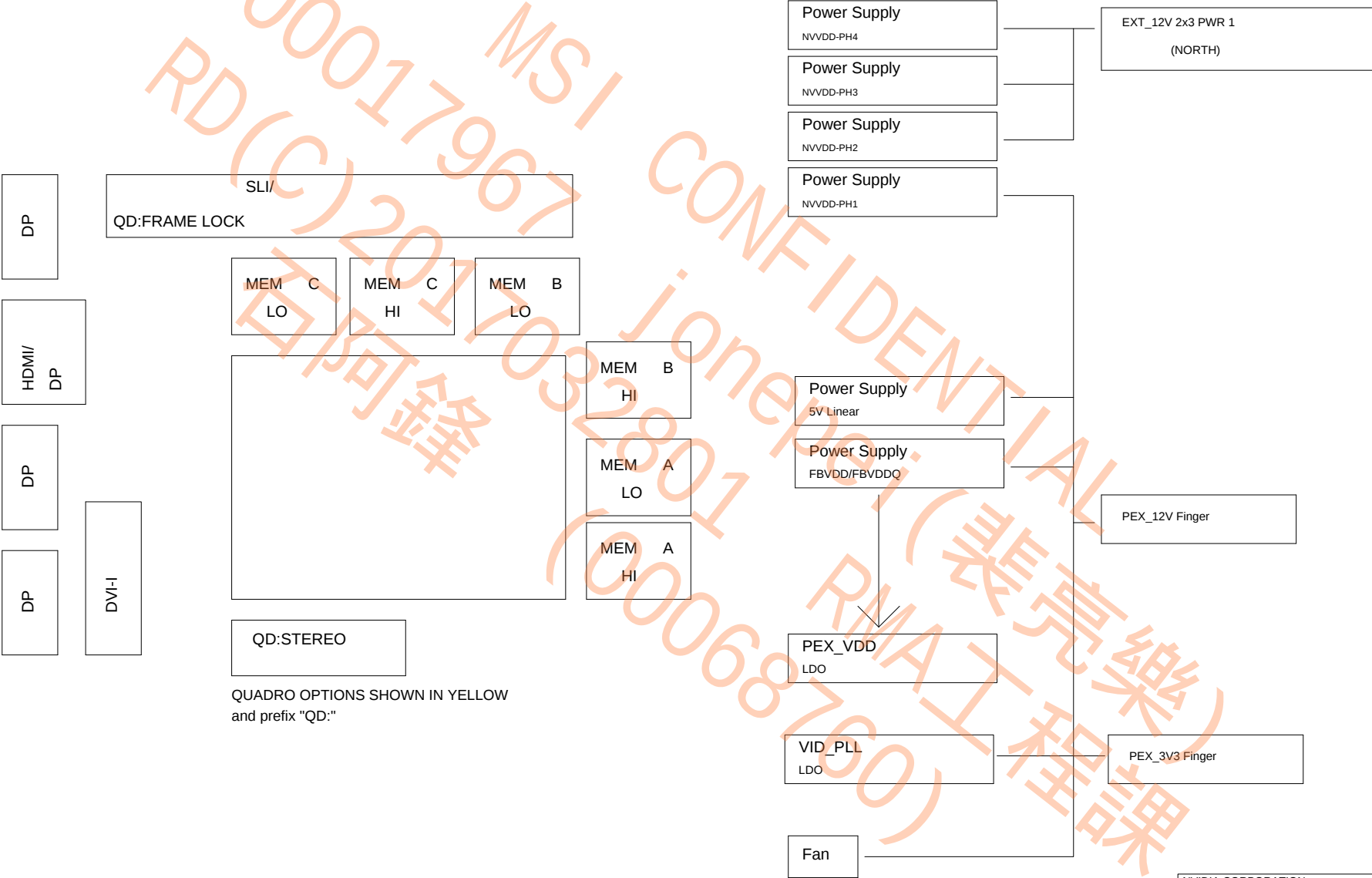
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Block Diagram



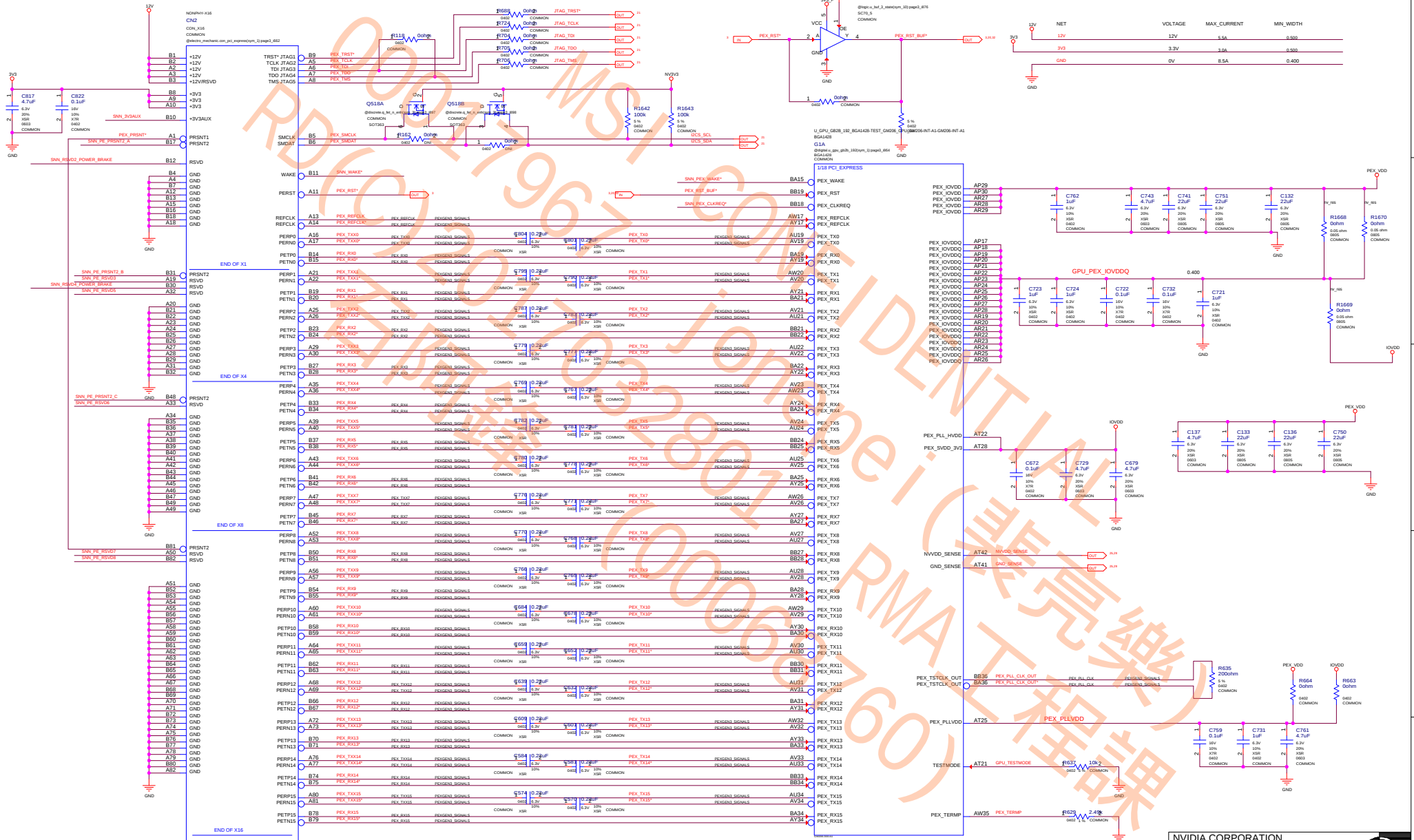
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PCI Express



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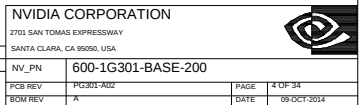
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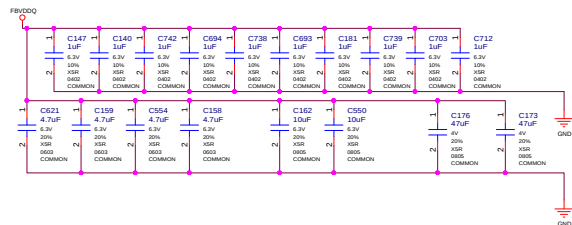
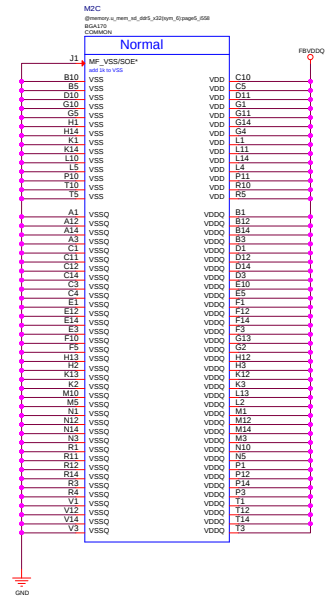
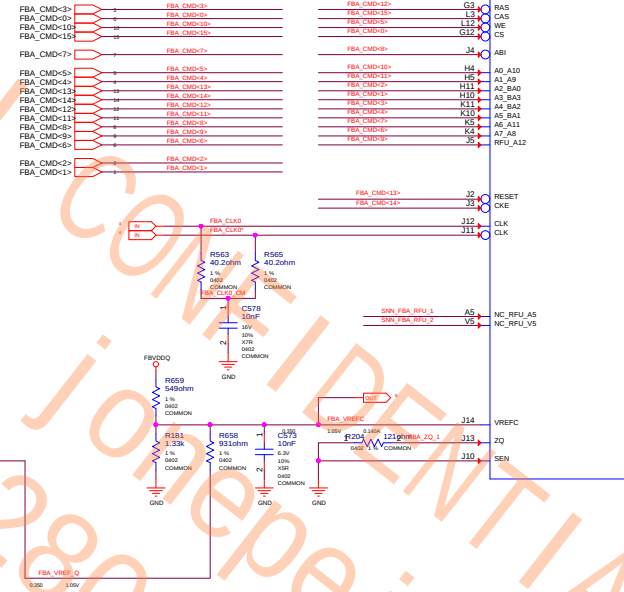
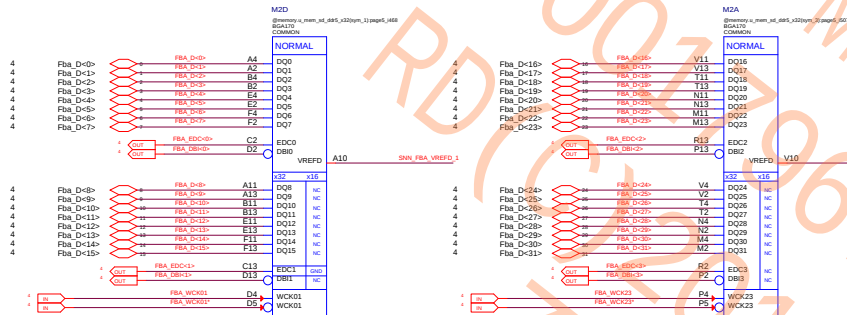


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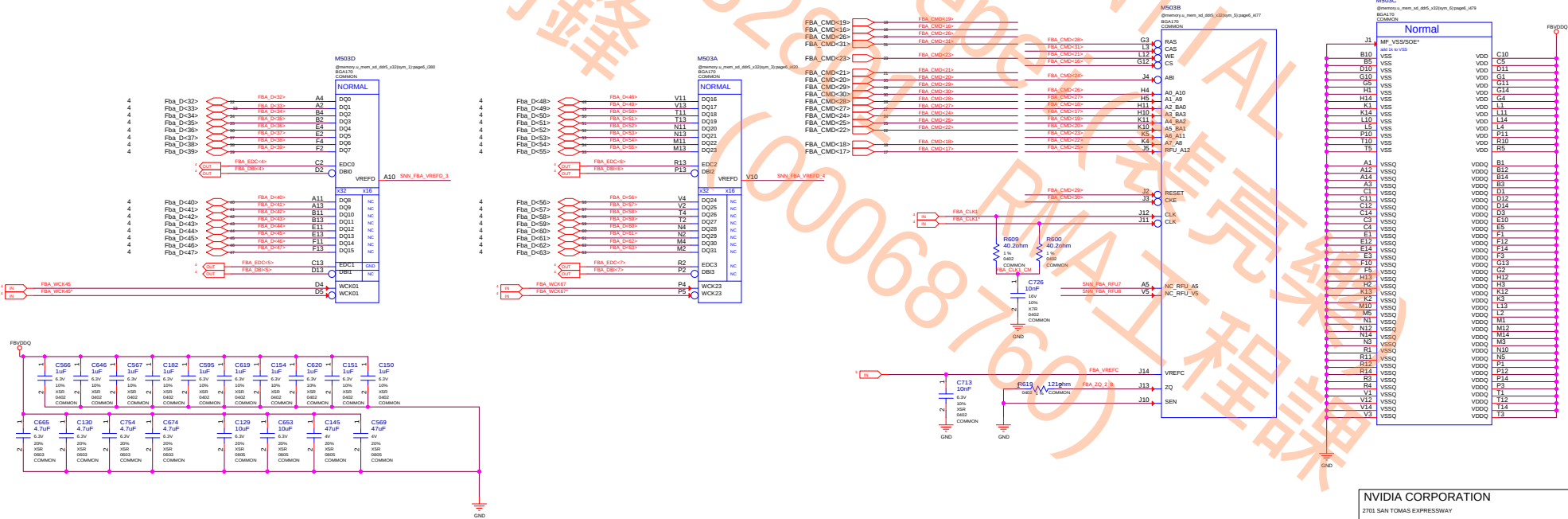
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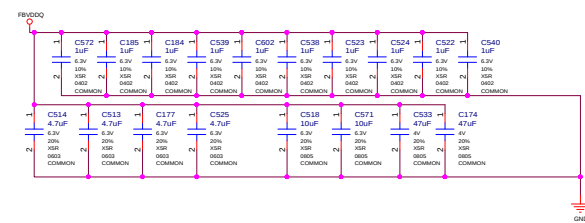
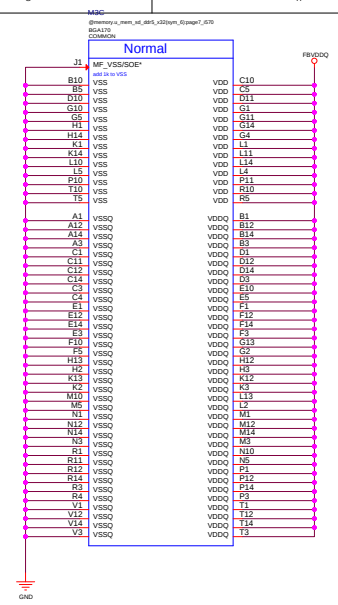
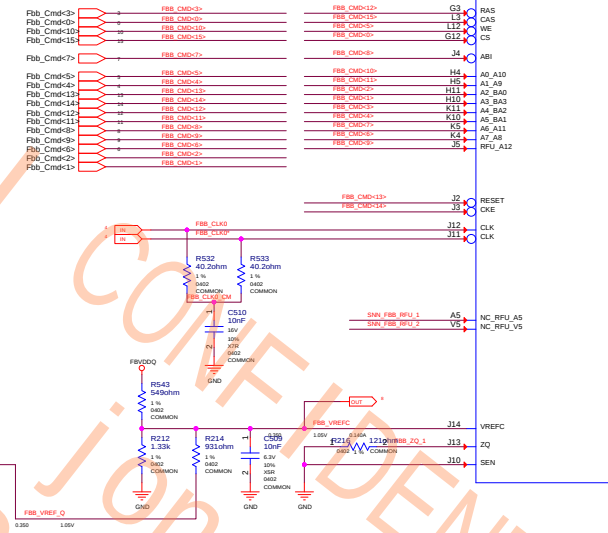
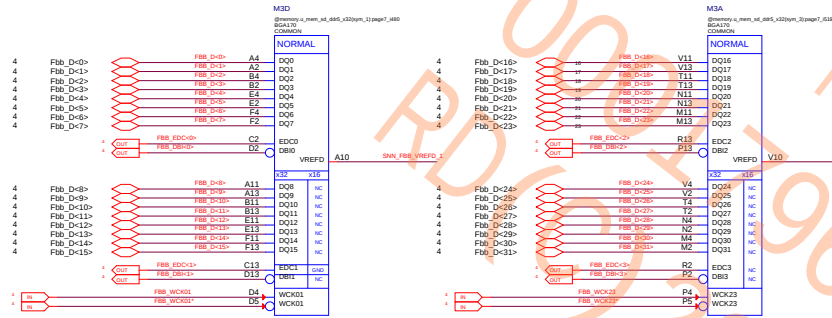
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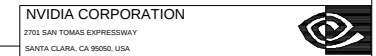
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MEMORY: FBB Partition 31..0



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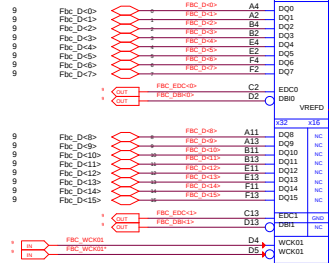
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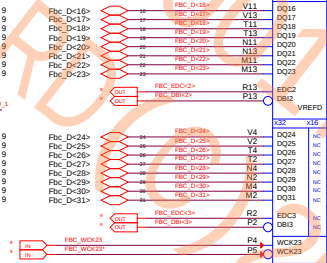
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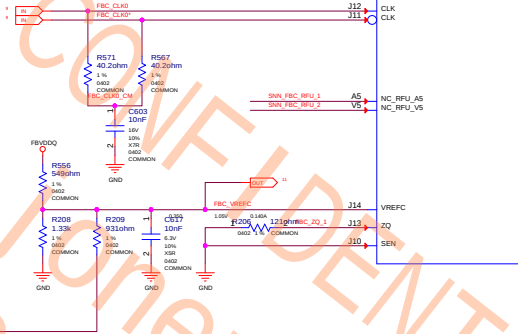
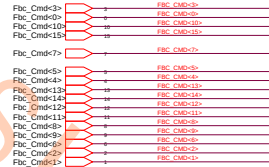


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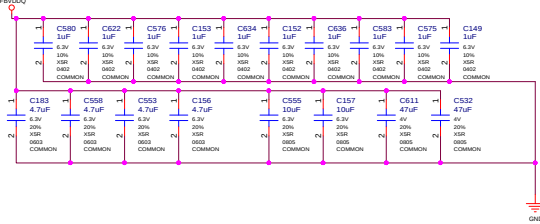
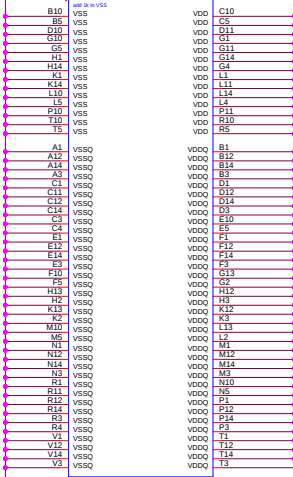


Use low VGSM part for P0404



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GPU PWR and GND



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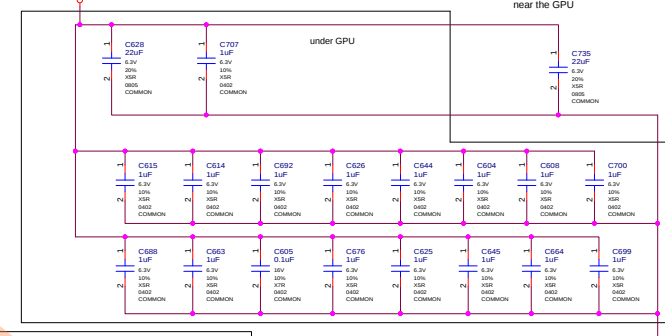
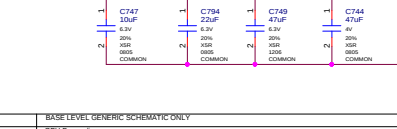
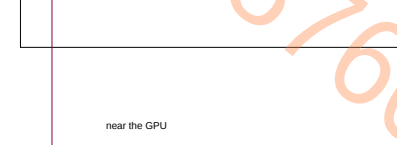
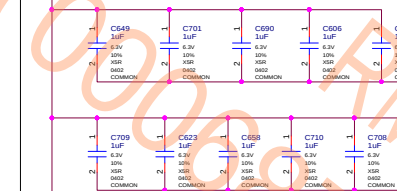
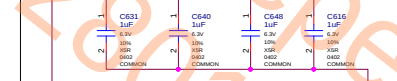
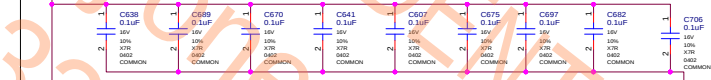
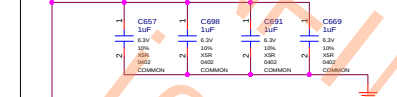
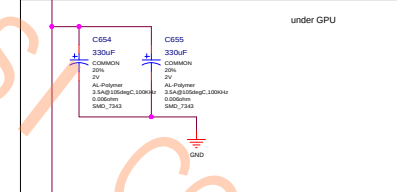
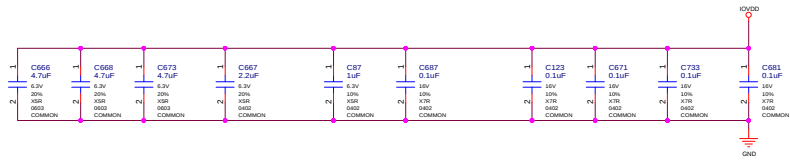
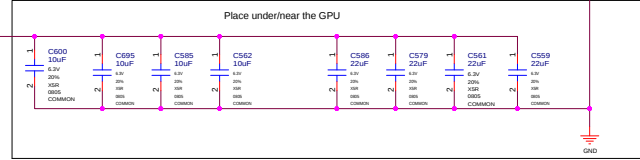
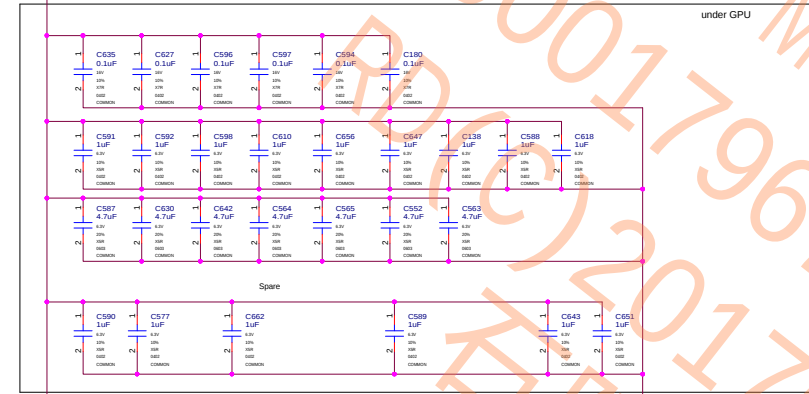
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GPU Decoupling

FBVDDQ

NVVD

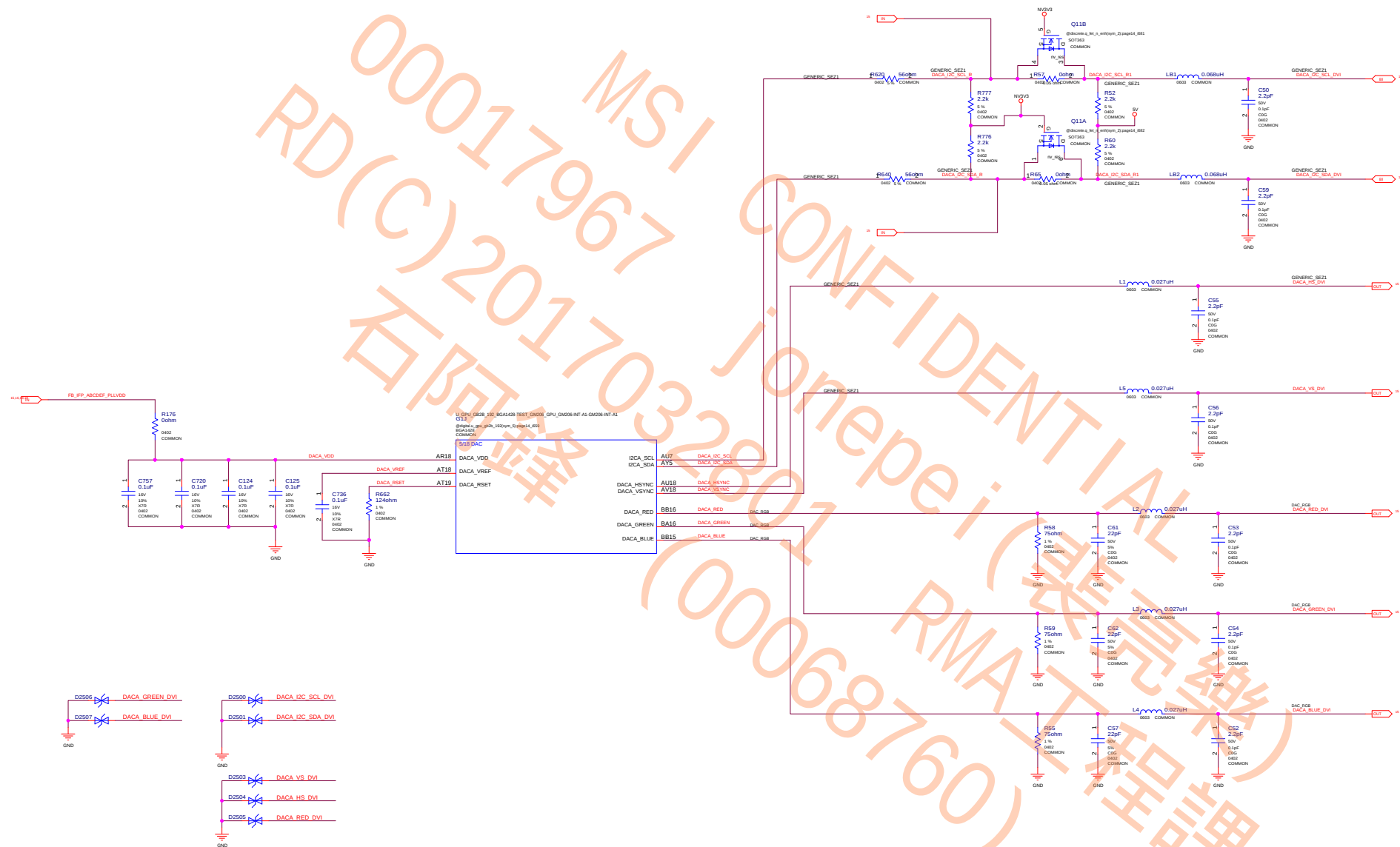


NVVD	Under GPU	90uF + 1x 330uF	Near GPU
SVVD		32uF	88uF
Combined (Maxwell)		122uF + 1x 330uF	110uF

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DACA Interface



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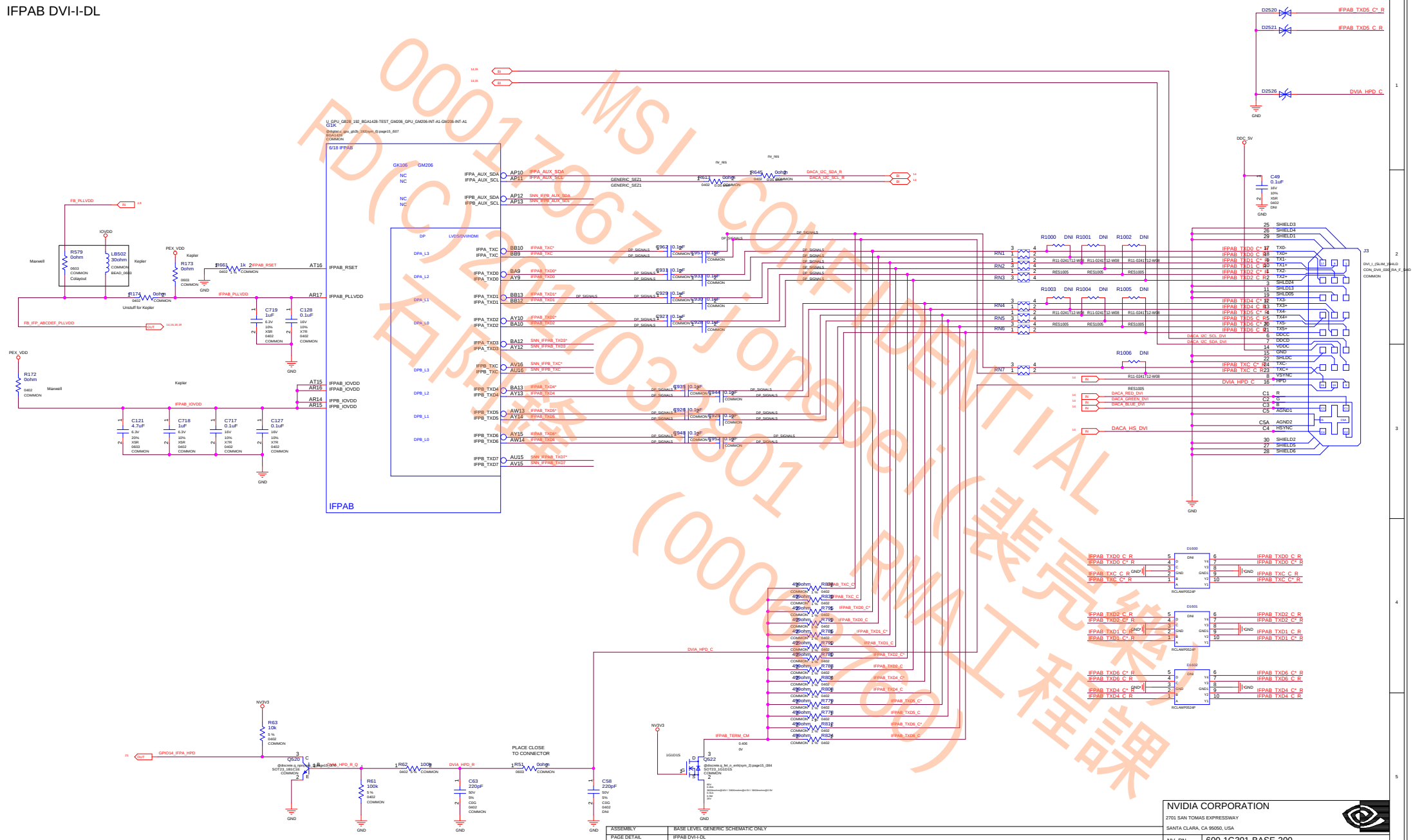
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IFPAB DVI-I-DL

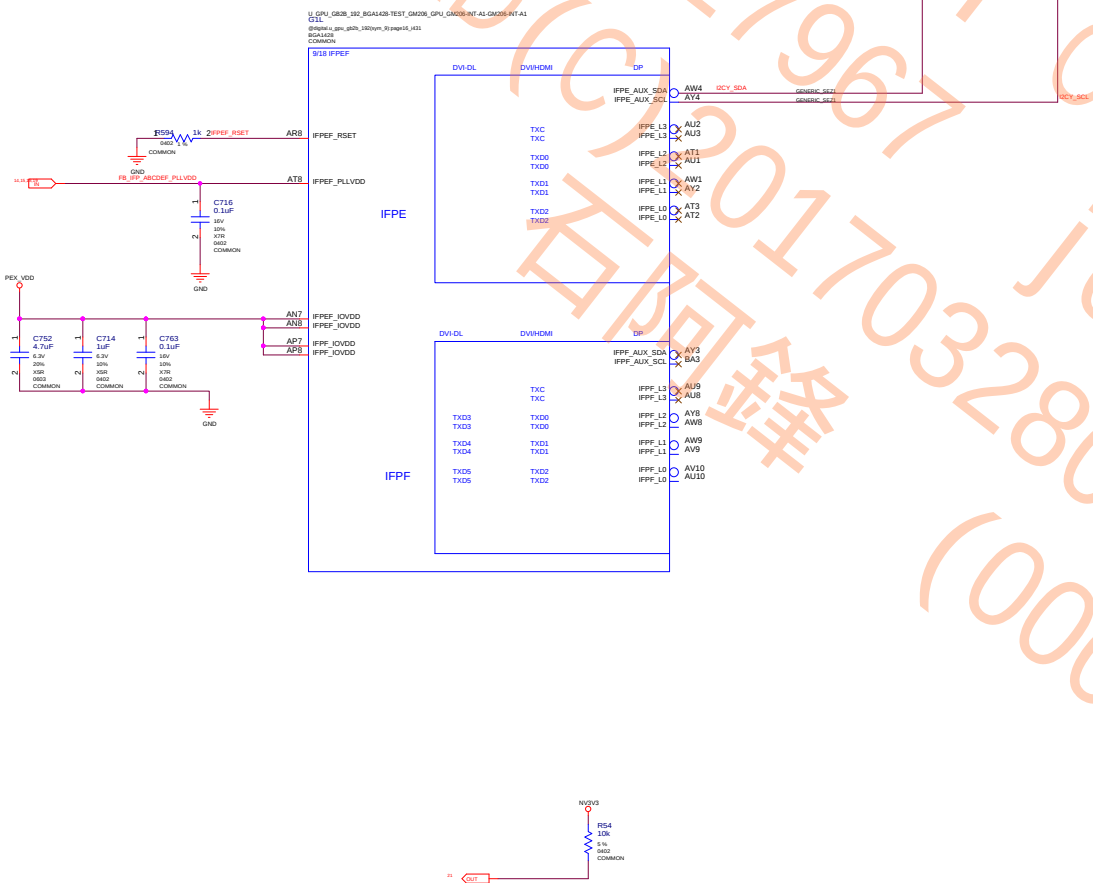


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1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



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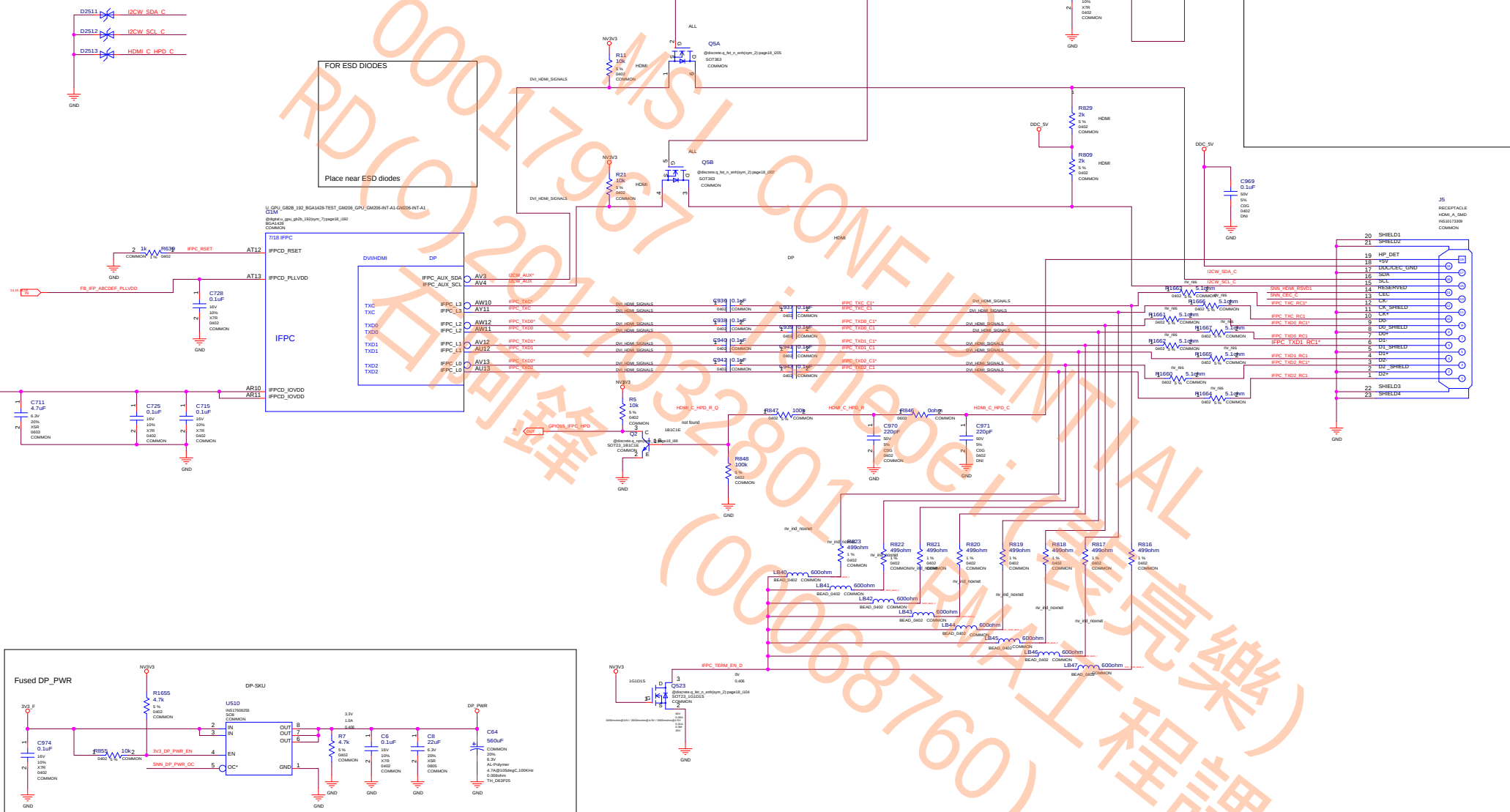
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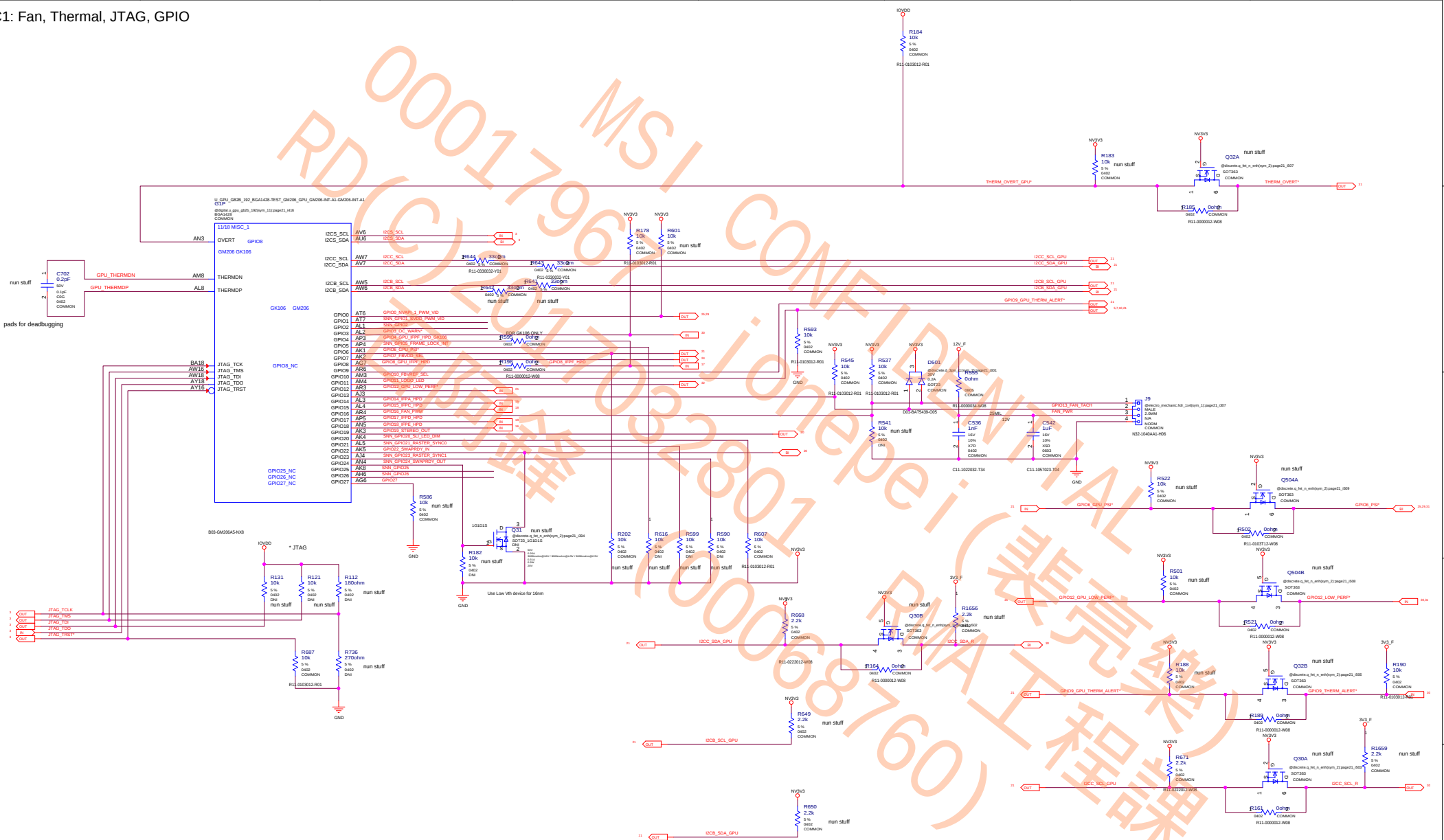
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MISC1: Fan, Thermal, JTAG, GPIO



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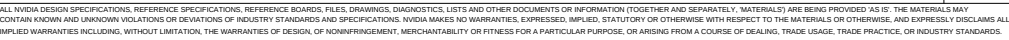
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MISC1: Fan, Thermal, JTAG, GPIO

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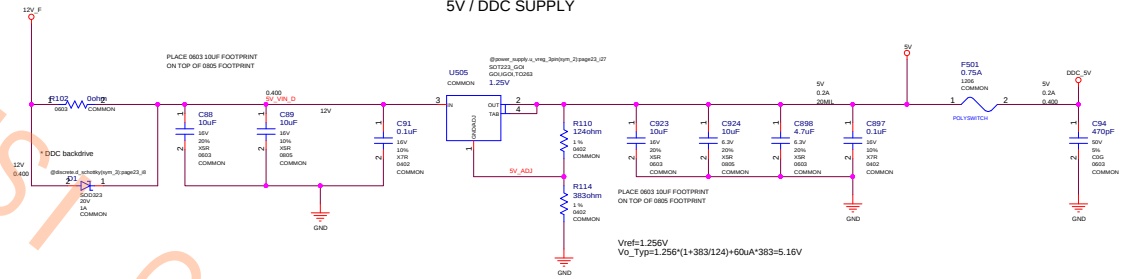
	KEPLER	MAXWELL
STRAP0	USER_BIT [3:0]*	
STRAP1	3GIO_PADCFG_LUT_ADR*	
STRAP2	PCI_DEVID [3:0]*	
STRAP3	SOR_EXPOSED [3:0]*	
STRAP4	DP_PLL_VDD_33V*	
	PEX_MAX_SPEED*	
	PEX_SPD_CHANGE_GEN3*	
	*	

ROM_SI	RAMCFG[0]*	RAMCFG[0]*
	RAMCFG[1]*	RAMCFG[1]*
	RAMCFG[2]*	RAMCFG[2]*
	RAMCFG[3]*	RAMCFG[3]*
ROM_SO	VGA_DEVICE*	VGA_DEVICE*
	SMB_ALT_ADDR*	SMB_ALT_ADDR*
	FB[0]_APERTURE_SIZE*	PCIE_CFG*
	FB[1]_APERTURE_SIZE*	DEVID_SEL*
ROM_SCLK	PEX_PLL_EN_TERM100*	SOR0_EXPOSED*
	PCI_DEVID_EXT[5]*	SOR1_EXPOSED*
	SUB_VENDOR*	SOR2_EXPOSED*
	PCI_DEVID_EXT[4]*	SOR3_EXPOSED*



PS: 5V, PEX_VDD

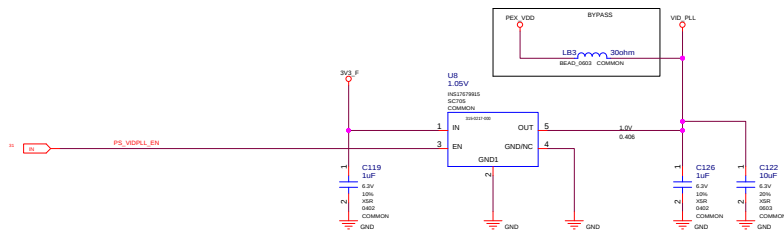
5V / DDC SUPPLY



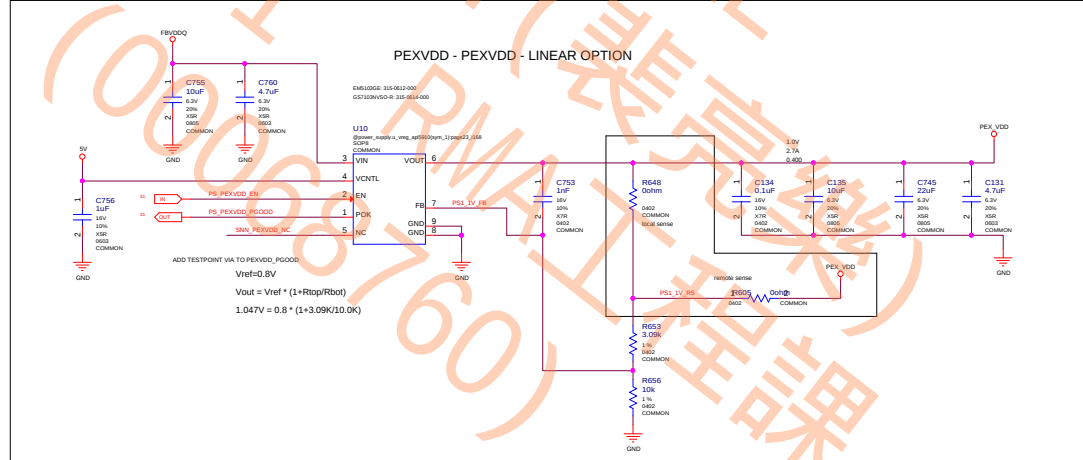
1V PLL SUPPLY



VID PLL SUPPLY



PEXVDD - PEXVDD - LINEAR OPTION



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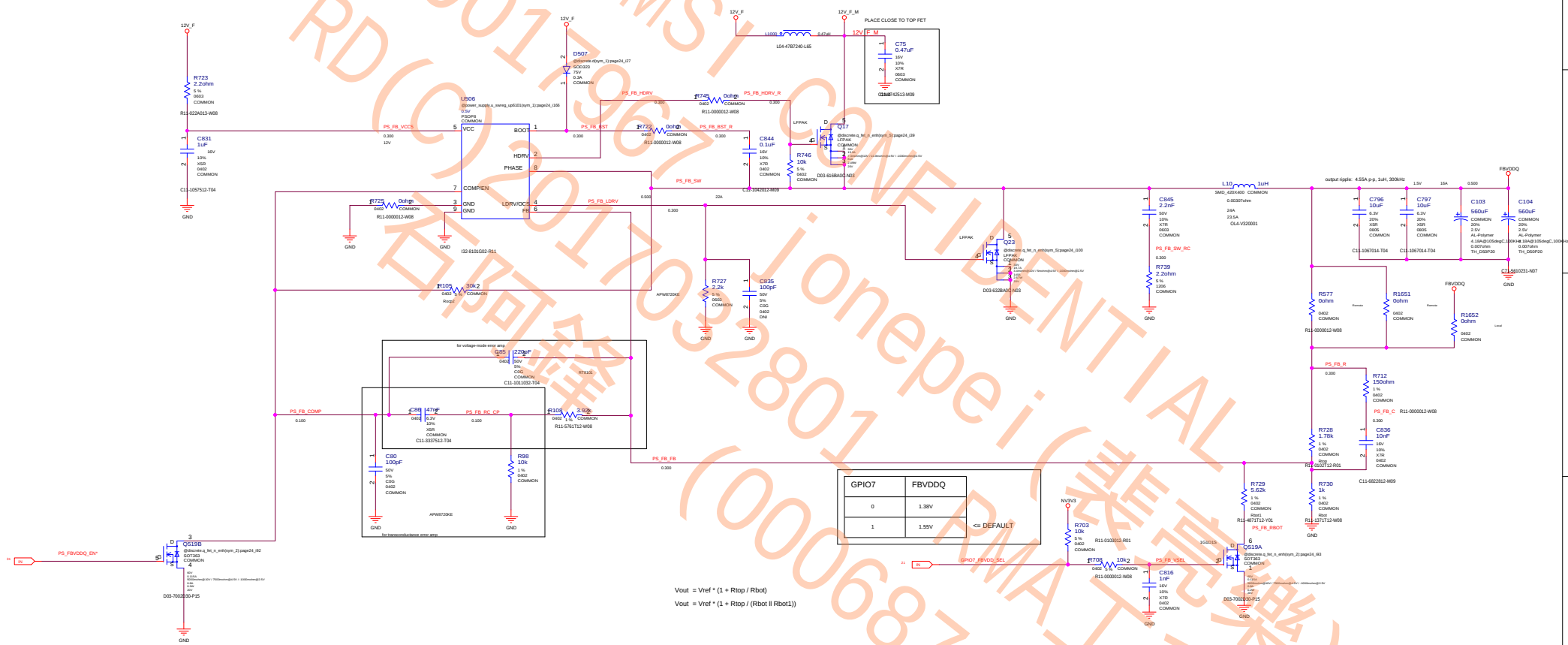
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PS: FBVDDQ



$$V_{out} = V_{ref} * (1 + R_{top} / R_{bot})$$
$$V_{out} = V_{ref} * (1 + R_{top} / (R_{bot} || R_{bot1}))$$

	Vref	Vref accuracy	Fosc	GPIO7	
APW720KE	0.5V	1%	300kHz	0	$V_{out} = 5V * (1 + 78m\Omega / 1.3V) = 1.39V$
				1	$V_{out} = 5V * (1 + 78m\Omega / (1.3V 1.54V)) = 1.54V$
RT801GSP	0.8V	1%	300kHz	0	$V_{out} = 8V * (1 + 141.37\Omega / 1.38V) = 1.38V$
				1	$V_{out} = 8V * (1 + 141.37\Omega / (1.38V 1.54V)) = 1.54V$

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ASSEMBLY

PAGE DETAIL

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PS: FBVDDQ

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DATE

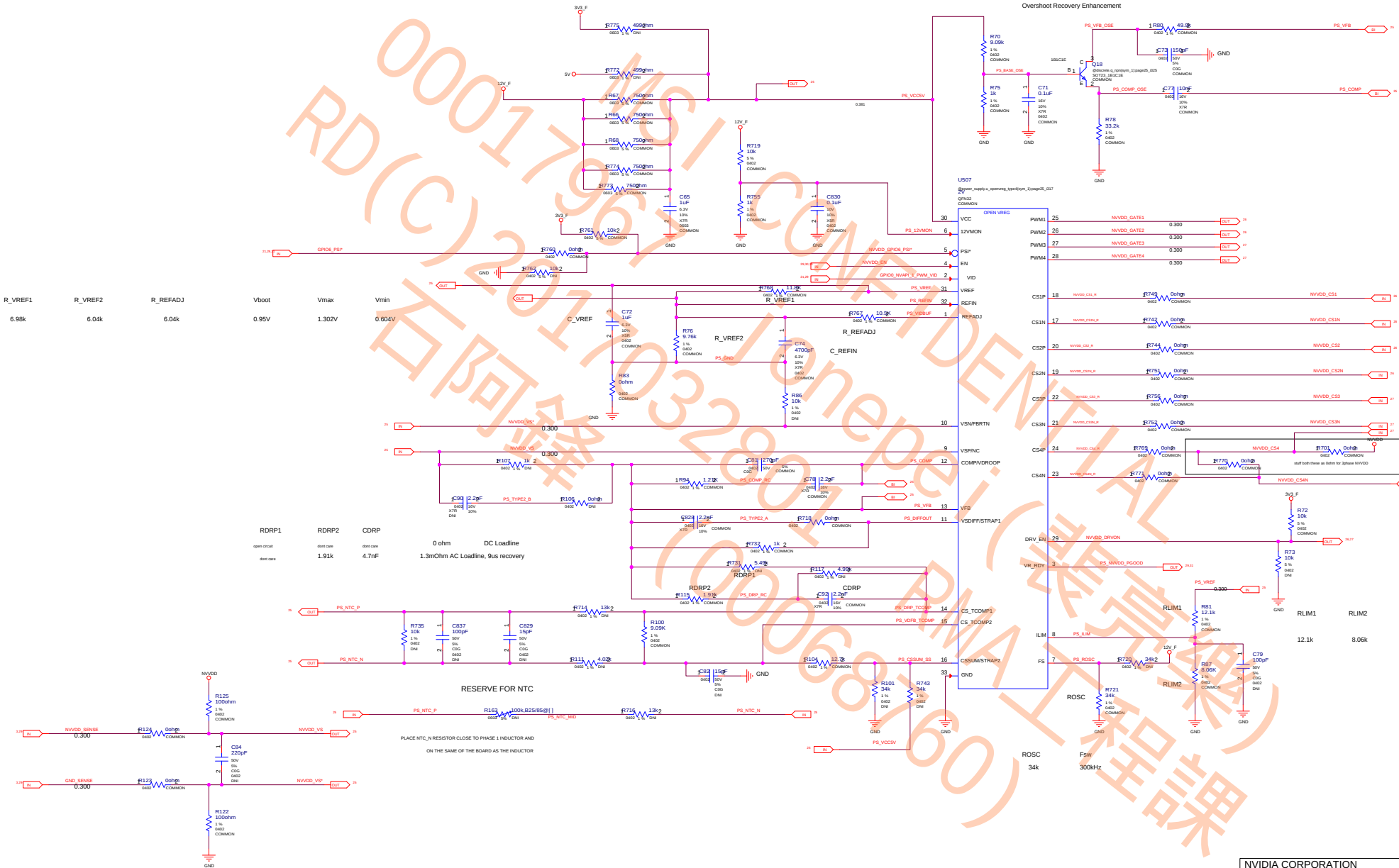
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PS: NVVDD Controller

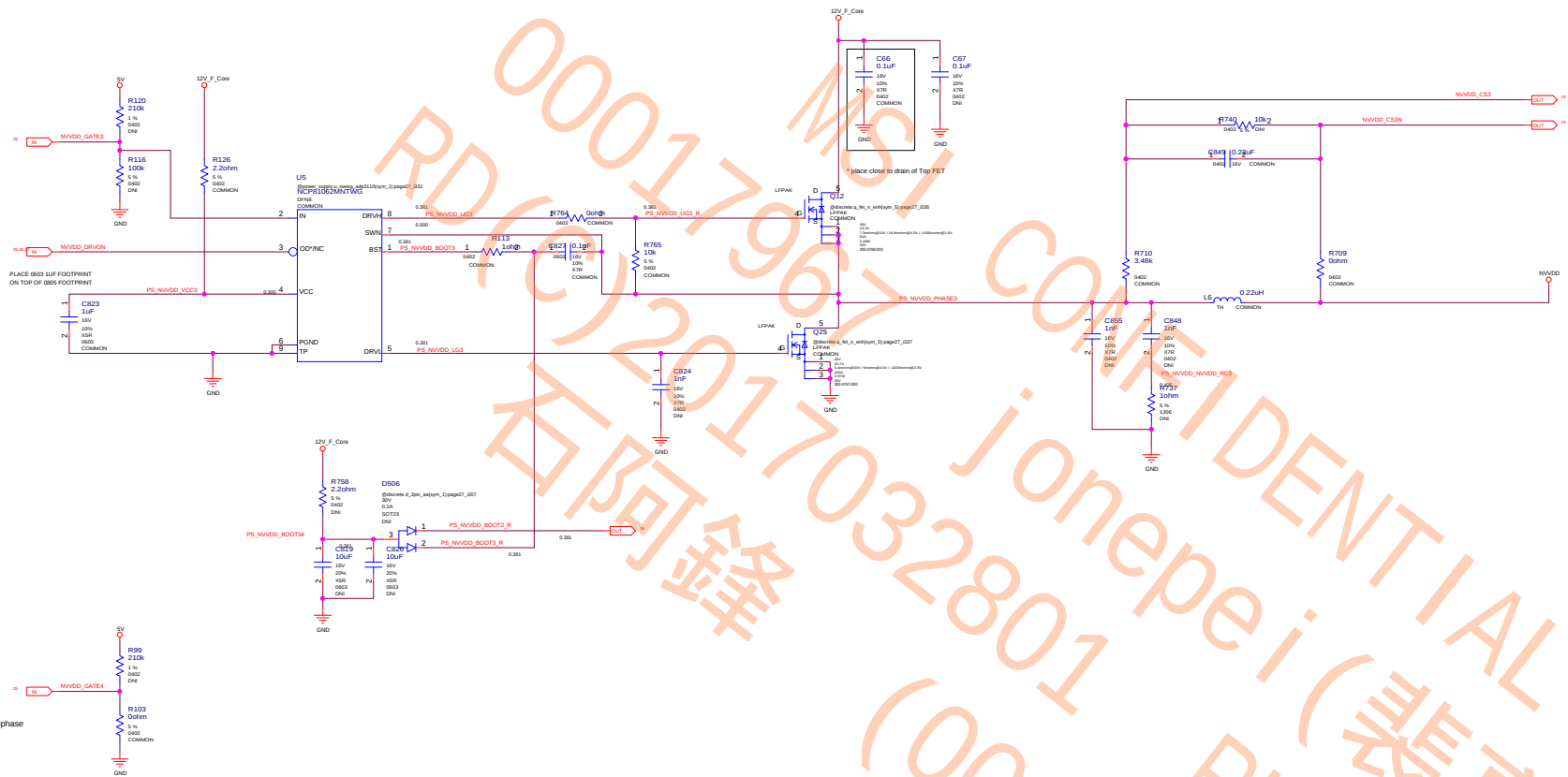




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PS: NVVDD Phase 3,4



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVDD Phase 3,4

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MSI CONFIDENTIAL
00017967 jonepei (裴亮樂)
RD(C)2017032801 RMA工程課
石阿鋒 (00068760)

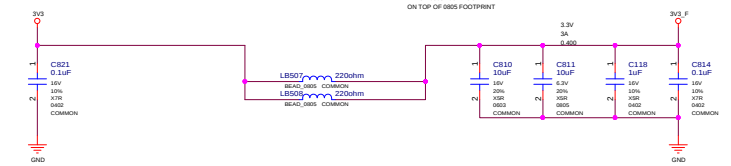
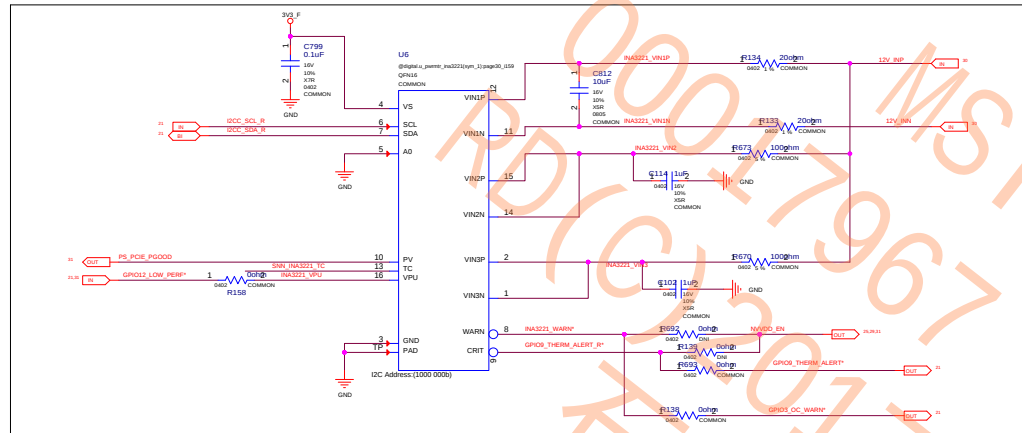
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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD OVR2+1.qxd

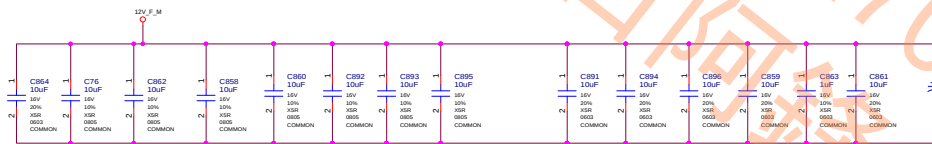
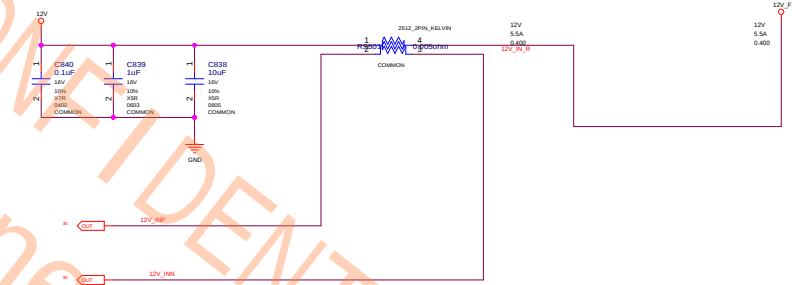
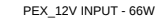
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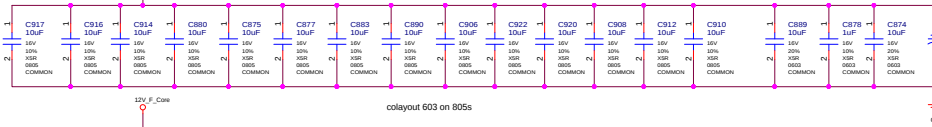
PS: Inputs, Filtering, and Monitoring



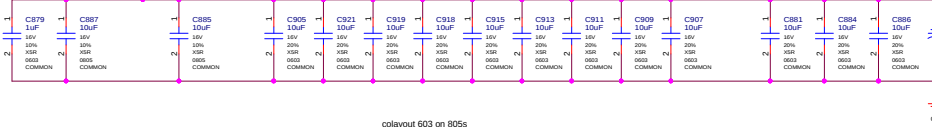
PLACE 0603 10UF FOOTPRINT
ON TOP OF C605 FOOTPRINT



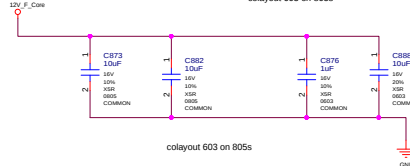
colayout 603 on 805s



colayout 603 on 805s



colayout 603 on 805s



colayout 603 on 805s

C76 must be low profile component if stuffed with FET heatsink

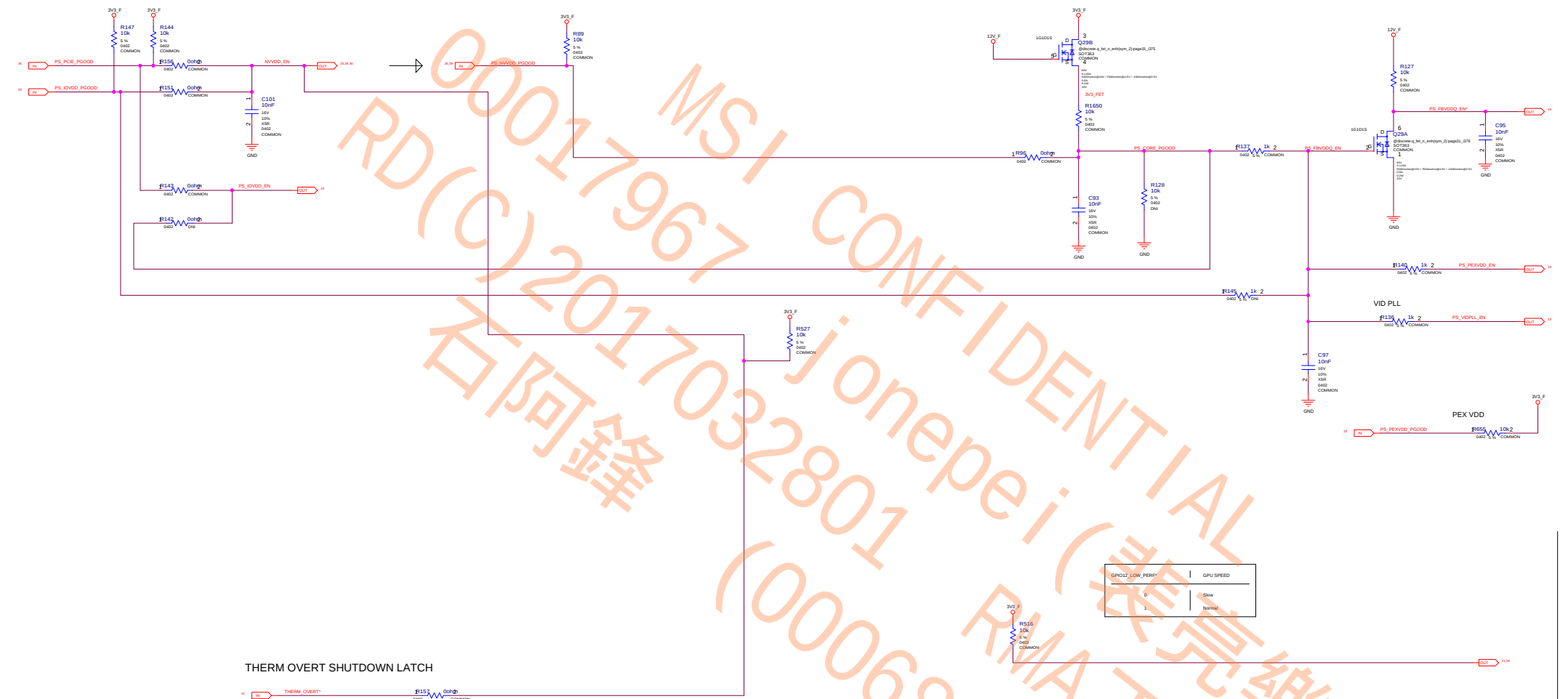
ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Inputs, Filtering, and Monitoring

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PS: Sequence and Shutdown



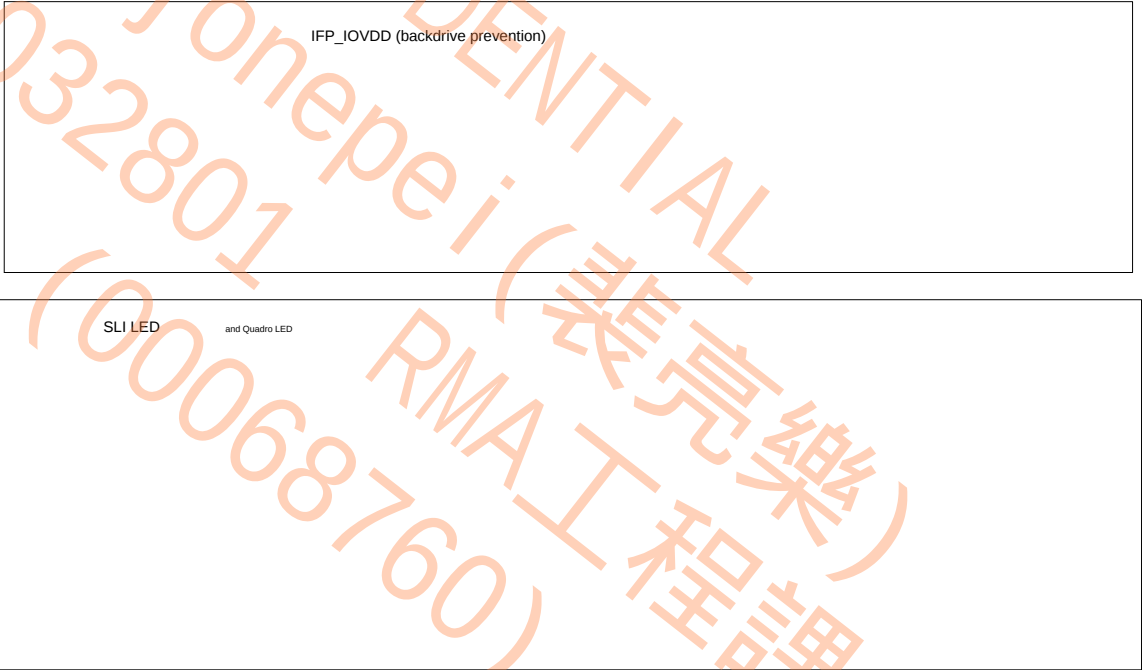
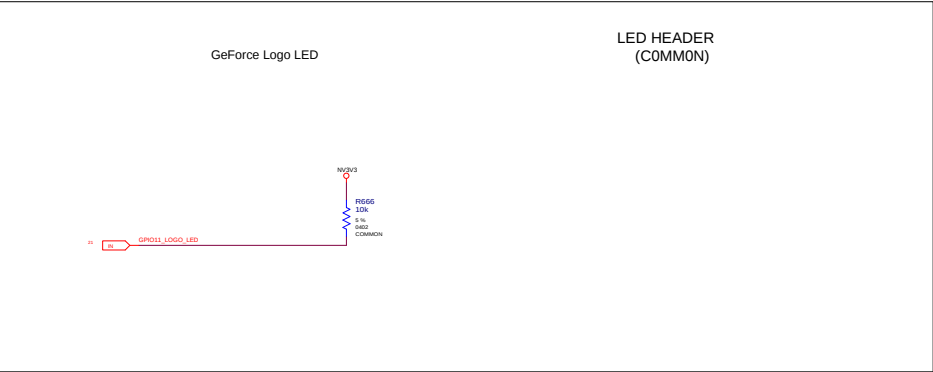
GPI012_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: Sequence and Shutdown

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LEDs



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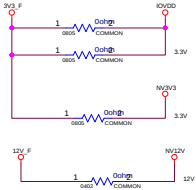
PS: IOVDD, NV3V3, NV12V

OVRO 1.8V REGULATOR. STUFF FOR 16nm

Special Note:
1. Place [C_OUT] close to [L_OUT]
2. Use local FB sense (refer to design guide for details)
3. Place PLL/JD filter ferrite bead to the same position as FB local sense point

Gated rails required for 16nm

BYPASS. STUFF FOR 28nm



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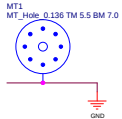


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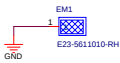
Mechanical: Bracket/Thermal Solution

FET HS

Brackets:



SCREW206
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>
E41-130408-P05



For DP Connector

DP SCREWS with top tab

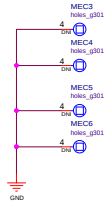
SCREW204
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>
E43-1204011-P05

For DVI Connector

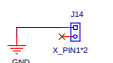
DVVDVI SCREWS with top tab

SCREW202
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>
E42-5047012-A43

SCREW203
SCREW
JACKPOST, HEX, 3/16 AF, 4-40 INT/EXT
<3rd part field>
E42-5047012-A43



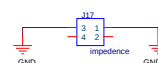
Reserve J3 - J20 for Impedance check



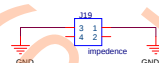
MEM Data
FBC_D<9>
Top
0.129MM / 47ohm +/- 10%
Reference L2 GND



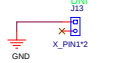
SLU Data
MOA_D7
L3
0.103MM / 52ohm +/- 10%
Reference L2 GND



MEM CLK
FBA_CLK1/FBA_CLK1*
L3 Inner
0.103MM / 52ohm +/- 10%
Reference L2 Inner GND



HDMI TMDS signals
IFPC_TXC/IFPC_TXC*
L4 Inner
0.104MM / 52ohm +/- 10%
Reference L5 Inner GND



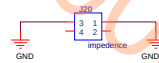
RGB signal
DACA_GREEN_DVI
Bottom
0.103MM / 52ohm +/- 10%
Reference L5 Inner GND



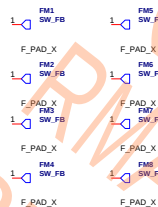
MEM Address
FBC_CMD<4>
L4
0.127MM / 47ohm +/- 10%
Reference L5 GND



PEX_PCEI / DVI IFPEF
PEX_RX13/PEX_RX13* IFPEF_TXC_C* RIIFPEF_TXC_C_R
TOP
0.101MM / 52ohm +/- 10%
Reference L2 Inner GND



PEX_PCEI / DVI IFPAB
PEX_TX6/PEX_TX6* IFPAB_TXD1_C* RIIFPAB_TXD1_C_R
Bottom
0.101MM / 52ohm +/- 10%
Reference L5 Inner GND



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