PG301 A02

Comanche 192b GDDR5, <150W, 2-way SLI

Tall DVI-I + DP + DP + DP/HDMI + DP

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Block Diagram

DP

HDMI/
DP

DP

DP

DVI-I

SLI/

QD:FRAME LOCK

MEM C
LO

MEM C
HI

MEM B
LO

MEM B
HI

MEM A
LO

MEM A
HI

QD:STEREO

QUADRO OPTIONS SHOWN IN YELLOW
and prefix "QD:"

Power Supply
NVVDD-PH4

Power Supply
NVVDD-PH3

Power Supply
NVVDD-PH2

Power Supply
NVVDD-PH1

EXT_12V 2x3 PWR 1
(NORTH)

Power Supply
5V Linear

Power Supply
FBVDD/FBVDDQ

PEX_12V Finger

PEX_VDD
LDO

VID_PLL
LDO

PEX_3V3 Finger

Fan

ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
Block Diagram

GIGABYTE

Title: Block of Diagram		
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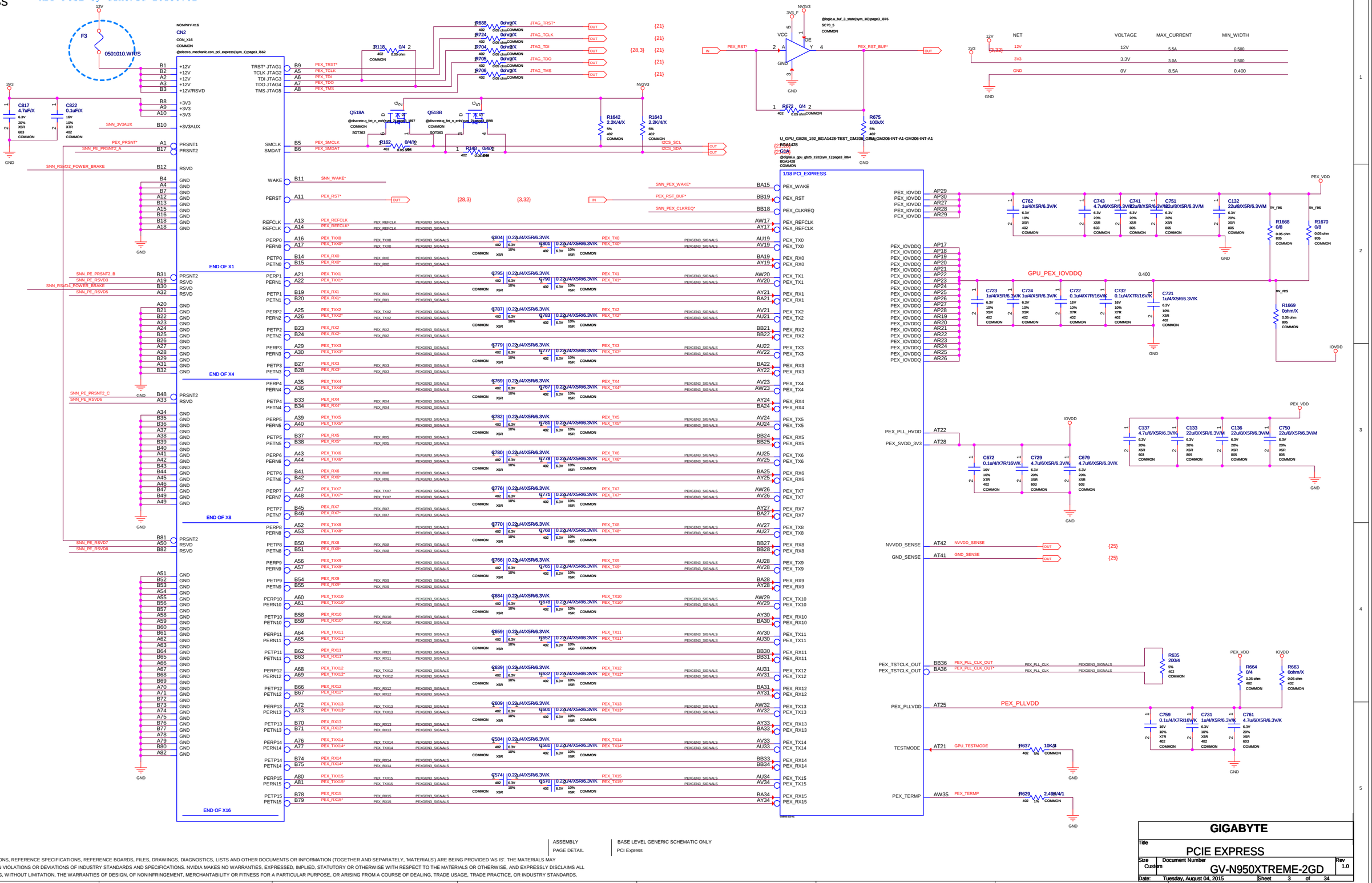
PCI Express

ADD FUSE by diho.su 20150702



ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
PCI Express

GIGABYTE

Title: PCIE EXPRESS

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MEMORY: GPU Partition A/B

U_GPU_GB2B_192_BGA1428-TEST_GM206_GPU_GM206-INT-A1-GM206-INT-A1
G1B
@digital:u_gpu_gb2b_192(sym_2):page4_U1905
BGA1428
COMMON

2/18 FBA

U_GPU_GB2B_192_BGA1428-TEST_GM206_GPU_GM206-INT-A1-GM206-INT-A1
G1C
@digital:u_gpu_gb2b_192(sym_3):page4_U906
BGA1428
COMMON

3/18 FBB

GDDR5_BGA170_MIRROR

	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD32		
CMD34	DBG0	DBG0
CMD16		CS*
CMD17		A3_BA3
CMD18		A2_BA0
CMD19		A4_BA2
CMD20		A5_BA1
CMD21		WE*
CMD22		A7_A8
CMD23		A6_A11
CMD24		ABI*
CMD25		A12_RFU
CMD26		A0_A10
CMD27		A1_A9
CMD28		RAS*
CMD29		RST*
CMD30		CKE*
CMD31		CAS*
CMD33		
CMD35	DBG1	DBG1

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: GPU Partition A/B

GIGABYTE

Title	DDR	
Size: Custom	Document Number: GV-N950XTREME-2GD	Rev: 1.0
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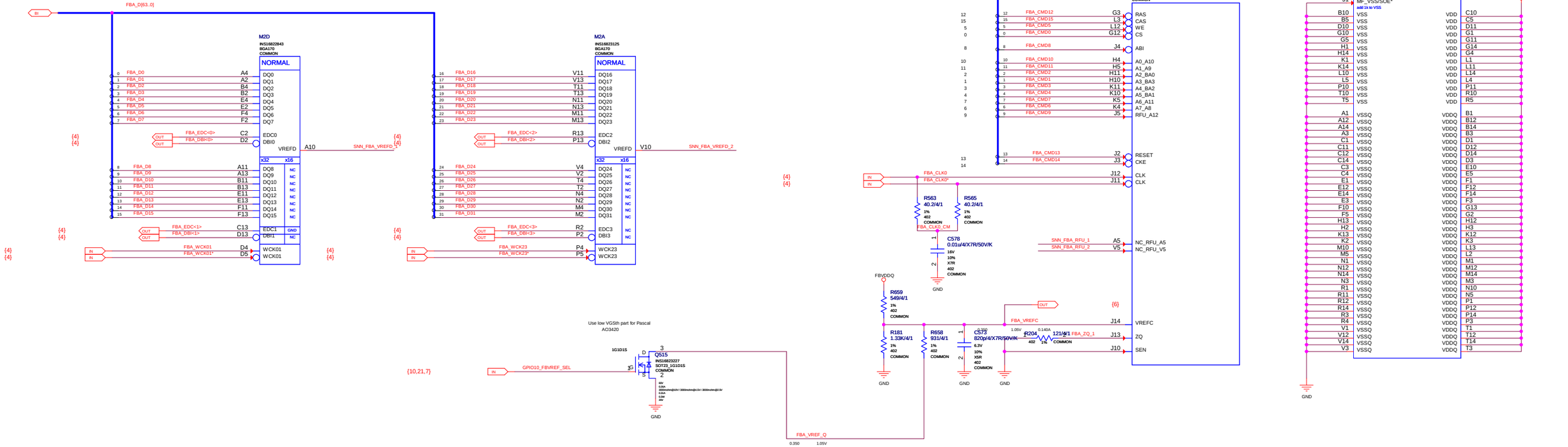
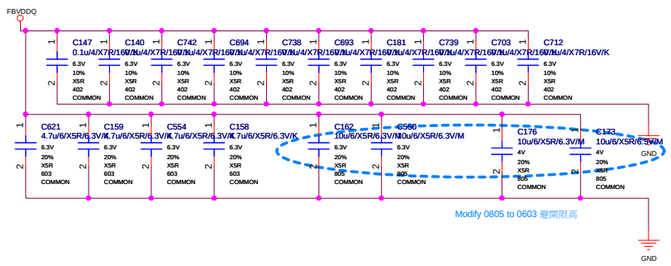
MEMORY: FBA Partition 31..0





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GIGABYTE

MEMORY: FBA Partition 63..32

{4,5}

BI FBA_D[63..0]

M503D
IN516825091
BGA170
COMMON
NORMAL

32	FBA_D32	A4	DQ0	
33	FBA_D33	A2	DQ1	
34	FBA_D34	B4	DQ2	
35	FBA_D35	B2	DQ3	
36	FBA_D36	E4	DQ4	
37	FBA_D37	E2	DQ5	
38	FBA_D38	F4	DQ6	
39	FBA_D39	F2	DQ7	
{4}	FBA_EDC<4>	C2	EDC0	
{4}	FBA_DBI<4>	D2	DBI0	
			VREFD	A10 SNN_FBA_VREFD_3
40	FBA_D40	A11	DQ8	NC
41	FBA_D41	A13	DQ9	NC
42	FBA_D42	B11	DQ10	NC
43	FBA_D43	B13	DQ11	NC
44	FBA_D44	E11	DQ12	NC
45	FBA_D45	E13	DQ13	NC
46	FBA_D46	F11	DQ14	NC
47	FBA_D47	F13	DQ15	NC
{4}	FBA_EDC<5>	C13	EDC1	GND
{4}	FBA_DBI<5>	D13	DBI1	NC
{4} FBA_WCK45		D4	WCK01	
{4} FBA_WCK45*		D5	WCK01	

M503A
IN516825233
BGA170
COMMON
NORMAL

48	FBA_D48	V11	DQ16	
49	FBA_D49	V13	DQ17	
50	FBA_D50	T11	DQ18	
51	FBA_D51	T13	DQ19	
52	FBA_D52	N11	DQ20	
53	FBA_D53	N13	DQ21	
54	FBA_D54	M11	DQ22	
55	FBA_D55	M13	DQ23	
{4}	FBA_EDC<6>	R13	EDC2	
{4}	FBA_DBI<6>	P13	DBI2	
			VREFD	V10 SNN_FBA_VREFD_4
56	FBA_D56	V4	DQ24	NC
57	FBA_D57	V2	DQ25	NC
58	FBA_D58	T4	DQ26	NC
59	FBA_D59	T2	DQ27	NC
60	FBA_D60	N4	DQ28	NC
61	FBA_D61	N2	DQ29	NC
62	FBA_D62	M4	DQ30	NC
63	FBA_D63	M2	DQ31	NC
{4}	FBA_EDC<7>	R2	EDC3	NC
{4}	FBA_DBI<7>	P2	DBI3	NC
{4} FBA_WCK67		P4	WCK23	
{4} FBA_WCK67*		P5	WCK23	

FBVDDQ

C566	0.1u/4/X7R/16V/K	1	2
C646	0.1u/4/X7R/16V/K	1	2
C567	0.1u/4/X7R/16V/K	1	2
C182	0.1u/4/X7R/16V/K	1	2
C595	0.1u/4/X7R/16V/K	1	2
C619	0.1u/4/X7R/16V/K	1	2
C154	0.1u/4/X7R/16V/K	1	2
C620	0.1u/4/X7R/16V/K	1	2
C151	0.1u/4/X7R/16V/K	1	2
C150	0.1u/4/X7R/16V/K	1	2

6.3V 10% X5R 402 COMMON

C665	4.7u/6/X5R/6.3V/M	1	2
C130	4.7u/6/X5R/6.3V/M	1	2
C754	4.7u/6/X5R/6.3V/M	1	2
C674	4.7u/6/X5R/6.3V/K	1	2
C125	10u/6/X5R/6.3V/M	1	2
C553	10u/6/X5R/6.3V/M	1	2
C145	10u/6/X5R/6.3V/M	1	2
C569	10u/6/5X5R/6.3V/M	1	2

6.3V 20% X5R 603 COMMON

4V 20% X5R 805 COMMON

Modify 0805 to 0603避開限高

GND

{4,5}

IN FBA_CMD[31..0]

M503B
IN516825403
BGA170
COMMON

28	FBA_CMD28	G3	RAS	
31	FBA_CMD31	L3	CAS	
21	FBA_CMD21	L12	WE	
16	FBA_CMD16	G12	CS	
24	FBA_CMD24	J4	ABI	
26	FBA_CMD26	H4	A0_A10	
27	FBA_CMD27	H5	A1_A9	
18	FBA_CMD18	H11	A2_BA0	
17	FBA_CMD17	H10	A3_BA3	
19	FBA_CMD19	K11	A4_BA2	
20	FBA_CMD20	K10	A5_BA1	
23	FBA_CMD23	K5	A6_A11	
22	FBA_CMD22	K4	A7_A8	
25	FBA_CMD25	J5	RFU_A12	
29	FBA_CMD29	J2	RESET	
30	FBA_CMD30	J3	CKE	
IN FBA_CLK1		J12	CLK	
IN FBA_CLK1*		J11	CLK	
	SNN_FBA_RFU7	A5	NC_RFU_A5	
	SNN_FBA_RFU8	V5	NC_RFU_V5	
	FBA_VREFC	J14	VREFC	
	FBA_ZQ_2_B	J13	ZQ	
		J10	SEN	

{4} {4}

R609 40.2/4/1 1% 402 COMMON FBA_CLK1_CM

R600 40.2/4/1 1% 402 COMMON

C726 0.01u/4/X7R/50V/K 16V 10% X7R 402 COMMON

GND

{5}

C713 820p/4/X7R/50V/K 6.3V 10% X5R 402 COMMON

R619 121/1/F 1% 402 COMMON

GND GND

M503C
IN516825505
BGA170
COMMON
Normal

J1	MF_VSS/SOE*		
	add 1k to VSS		
B10	VSS	VDD	C10
B5	VSS	VDD	C5
D10	VSS	VDD	D11
G10	VSS	VDD	G1
G5	VSS	VDD	G11
H1	VSS	VDD	G14
H14	VSS	VDD	G4
K1	VSS	VDD	L1
K14	VSS	VDD	L11
L10	VSS	VDD	L14
L5	VSS	VDD	L4
P10	VSS	VDD	P11
T10	VSS	VDD	R10
T5	VSS	VDD	R5
A1	VSSQ	VDDQ	B1
A12	VSSQ	VDDQ	B12
A14	VSSQ	VDDQ	B14
A3	VSSQ	VDDQ	B3
C1	VSSQ	VDDQ	D1
C11	VSSQ	VDDQ	D12
C12	VSSQ	VDDQ	D14
C14	VSSQ	VDDQ	D3
C3	VSSQ	VDDQ	E10
C4	VSSQ	VDDQ	E5
E1	VSSQ	VDDQ	F1
E12	VSSQ	VDDQ	F12
E14	VSSQ	VDDQ	F14
E3	VSSQ	VDDQ	F3
F10	VSSQ	VDDQ	G13
F5	VSSQ	VDDQ	G2
H13	VSSQ	VDDQ	H12
H2	VSSQ	VDDQ	H3
K13	VSSQ	VDDQ	K12
K2	VSSQ	VDDQ	K3
M10	VSSQ	VDDQ	L13
M5	VSSQ	VDDQ	L2
N1	VSSQ	VDDQ	M1
N12	VSSQ	VDDQ	M12
N14	VSSQ	VDDQ	M14
N3	VSSQ	VDDQ	M3
R1	VSSQ	VDDQ	N10
R11	VSSQ	VDDQ	N5
R12	VSSQ	VDDQ	P1
R14	VSSQ	VDDQ	P12
R3	VSSQ	VDDQ	P14
R4	VSSQ	VDDQ	P3
V1	VSSQ	VDDQ	T1
V12	VSSQ	VDDQ	T12
V14	VSSQ	VDDQ	T14
V3	VSSQ	VDDQ	T3

FBVDDQ

GND

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBA[63:32]

GIGABYTE

Title: DDR

Size	Document Number	Rev
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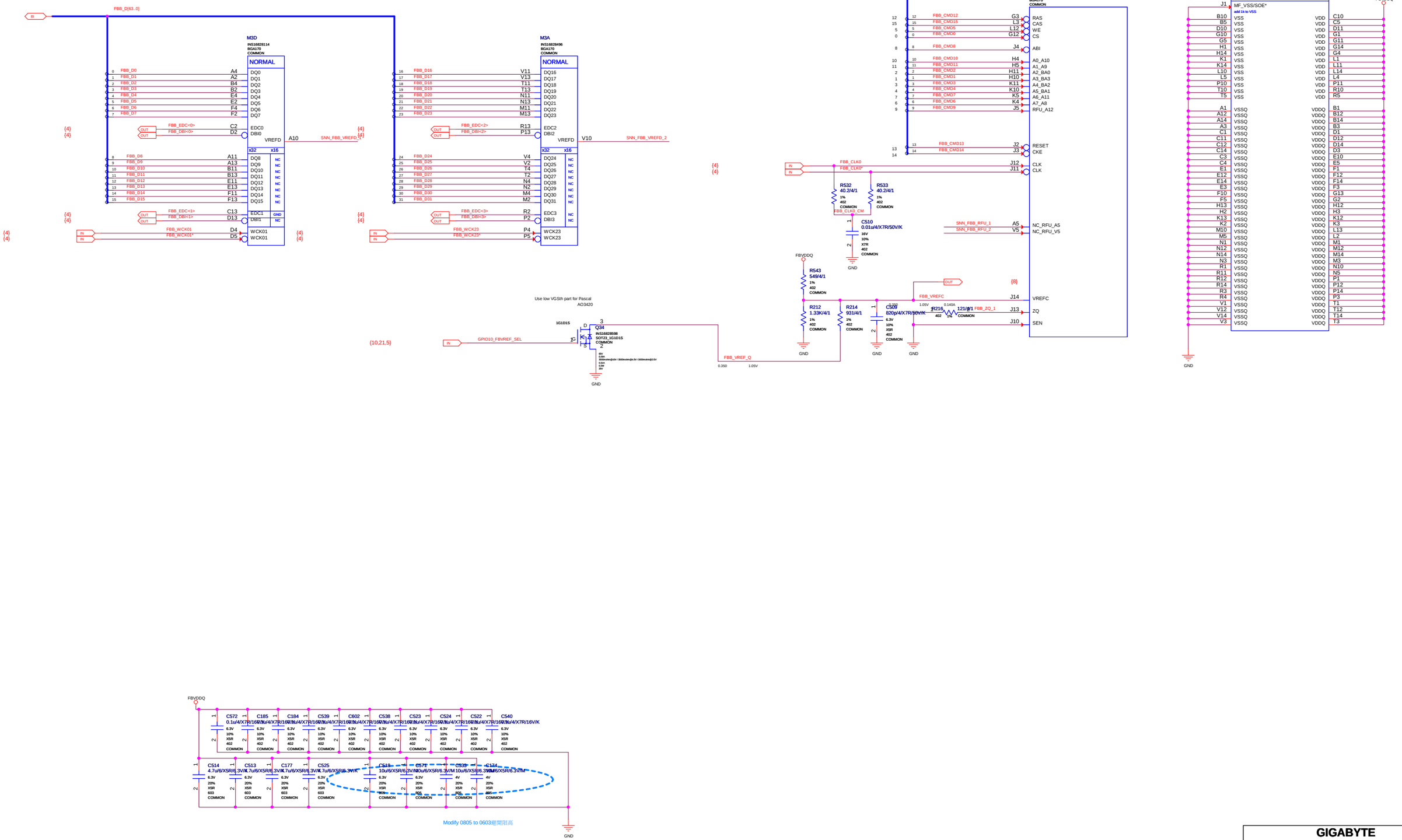
MEMORY: FBB Partition 31..0



ASSEMBLY | BASE LEVEL GENERIC SCHEMATIC ONLY

PAGE DETAIL | MEMORY: FBB[31:0]

GIGABYTE

Title: DDR

Size: Custom | Document Number: GV-N950XTREME-2GD | Rev: 1.0

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MEMORY: FBB Partition 63..32

{4,7}
BI
FBB_D[63..0]

M502D
INS16830039
BGA170
COMMON
NORMAL

32	FBB_D32	A4	DQ0
33	FBB_D33	A2	DQ1
34	FBB_D34	B4	DQ2
35	FBB_D35	B2	DQ3
36	FBB_D36	E4	DQ4
37	FBB_D37	E2	DQ5
38	FBB_D38	F4	DQ6
39	FBB_D39	F2	DQ7
	FBB_EDC<4>	C2	EDC0
	FBB_DBI<4>	D2	DBI0
			VREFD
		A10	SNN_FBB_VREFD_3
40	FBB_D40	A11	DQ8
41	FBB_D41	A13	DQ9
42	FBB_D42	B11	DQ10
43	FBB_D43	B13	DQ11
44	FBB_D44	E11	DQ12
45	FBB_D45	E13	DQ13
46	FBB_D46	F11	DQ14
47	FBB_D47	F13	DQ15
	FBB_EDC<5>	C13	EDC1
	FBB_DBI<5>	D13	DBI1
	FBB_WCK45	D4	WCK01
	FBB_WCK45*	D5	WCK01

x32 x16 NC GND NC NC NC NC NC NC NC NC NC NC NC NC NC NC

{4}
{4}

M502A
INS16830181
BGA170
COMMON
NORMAL

48	FBB_D48	V11	DQ16
49	FBB_D49	V13	DQ17
50	FBB_D50	T11	DQ18
51	FBB_D51	T13	DQ19
52	FBB_D52	N11	DQ20
53	FBB_D53	N13	DQ21
54	FBB_D54	M11	DQ22
55	FBB_D55	M13	DQ23
	FBB_EDC<6>	R13	EDC2
	FBB_DBI<6>	P13	DBI2
			VREFD
		V10	SNN_FBB_VREFD_4
56	FBB_D56	V4	DQ24
57	FBB_D57	V2	DQ25
58	FBB_D58	T4	DQ26
59	FBB_D59	T2	DQ27
60	FBB_D60	N4	DQ28
61	FBB_D61	N2	DQ29
62	FBB_D62	M4	DQ30
63	FBB_D63	M2	DQ31
	FBB_EDC<7>	R2	EDC3
	FBB_DBI<7>	P2	DBI3
	FBB_WCK67	P4	WCK23
	FBB_WCK67*	P5	WCK23

x32 x16 NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC NC

{4}
{4}

{4,7}
IN
FBB_CMD[31..0]

M502B
INS16830351
BGA170
COMMON

28	FBB_CMD28	G3	RAS
31	FBB_CMD31	L3	CAS
21	FBB_CMD21	L12	WE
16	FBB_CMD16	G12	CS
24	FBB_CMD24	J4	ABI
26	FBB_CMD26	H4	A0_A10
27	FBB_CMD27	H5	A1_A9
18	FBB_CMD18	H11	A2_BA0
17	FBB_CMD17	H10	A3_BA3
19	FBB_CMD19	K11	A4_BA2
20	FBB_CMD20	K10	A5_BA1
23	FBB_CMD23	K5	A6_A11
22	FBB_CMD22	K4	A7_A8
25	FBB_CMD25	J5	RFU_A12
29	FBB_CMD29	J2	RESET
30	FBB_CMD30	J3	CKE
	FBB_CLK1	J12	CLK
	FBB_CLK1*	J11	CLK
		A5	NC_RFU_A5
	SNN_FBB_RFU7	V5	NC_RFU_V5
	SNN_FBB_RFU8		
	FBB_VREFC	J14	VREFC
	FBB_ZQ_2_B	J13	ZQ
		J10	SEN

{4}
{4}

R534 40.2/4/1 1% 402 COMMON — FBB_CLK1_CM
R535 40.2/4/1 1% 402 COMMON
C512 0.01u/4/X7R/50V/K 16V 10% X7R 402 COMMON
GND

{7}
C511 820p/4/X7R/50V/K 6.3V 10% X5R 402 COMMON
R536 121/1/1 402 1% COMMON — FBB_ZQ_2_B
GND GND

M502C
INS16830453
BGA170
COMMON
Normal

J1	MF_VSS/SOE*		
	add 1k to VSS		
B10	VSS	VDD	C10
B5	VSS	VDD	C5
D10	VSS	VDD	D11
G10	VSS	VDD	G1
G5	VSS	VDD	G11
H1	VSS	VDD	G14
H14	VSS	VDD	G4
K1	VSS	VDD	L1
K14	VSS	VDD	L11
L10	VSS	VDD	L14
L5	VSS	VDD	L4
P10	VSS	VDD	P11
T10	VSS	VDD	R10
T5	VSS	VDD	R5
A1	VSSQ	VDDQ	B1
A12	VSSQ	VDDQ	B12
A14	VSSQ	VDDQ	B14
A3	VSSQ	VDDQ	B3
C1	VSSQ	VDDQ	D1
C11	VSSQ	VDDQ	D12
C12	VSSQ	VDDQ	D14
C14	VSSQ	VDDQ	D3
C3	VSSQ	VDDQ	E10
C4	VSSQ	VDDQ	E5
E1	VSSQ	VDDQ	F1
E12	VSSQ	VDDQ	F12
E14	VSSQ	VDDQ	F14
E3	VSSQ	VDDQ	F3
F10	VSSQ	VDDQ	G13
F5	VSSQ	VDDQ	G2
H13	VSSQ	VDDQ	H12
H2	VSSQ	VDDQ	H3
K13	VSSQ	VDDQ	K12
K2	VSSQ	VDDQ	K3
M10	VSSQ	VDDQ	L13
M5	VSSQ	VDDQ	L2
N1	VSSQ	VDDQ	M1
N12	VSSQ	VDDQ	M12
N14	VSSQ	VDDQ	M14
N3	VSSQ	VDDQ	M3
R1	VSSQ	VDDQ	N10
R11	VSSQ	VDDQ	N5
R12	VSSQ	VDDQ	P1
R14	VSSQ	VDDQ	P12
R3	VSSQ	VDDQ	P14
R4	VSSQ	VDDQ	P3
V1	VSSQ	VDDQ	T1
V12	VSSQ	VDDQ	T12
V14	VSSQ	VDDQ	T14
V3	VSSQ	VDDQ	T3

FBVDDQ
GND

FBVDDQ

C548 0.1u/4/X7R/16V/K
C547 1u/4/X7R/16V/K
C166 1u/4/X7R/16V/K
C169 1u/4/X7R/16V/K
C541 1u/4/X7R/16V/K
C521 1u/4/X7R/16V/K
C519 1u/4/X7R/16V/K
C155 1u/4/X7R/16V/K
C179 1u/4/X7R/16V/K
C520 1u/4/X7R/16V/K
6.3V 10% X5R 402 COMMON

C171 4.7u/6/X5R/6.3V/K
C172 4.7u/6/X5R/6.3V/K
C534 4.7u/6/X5R/6.3V/K
C535 4.7u/6/X5R/6.3V/K
C537 10u/6/X5R/6.3V/M
C170 10u/6/X5R/6.3V/M
C175 10u/6/X5R/6.3V/M
C141 10u/6/X5R/6.3V/M
6.3V 20% X5R 603 COMMON

Modify 0805 to 0603避開限高

GND

ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
MEMORY: FBB[63:32]

GIGABYTE

Title: DDR

Size	Document Number	Rev
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MEMORY: GPU Partition C/D

U_GPU_GB2B_192_BGA1428-TEST_GM206_GPU_GM206-INT-A1-GM206-INT-A1
G1D
INS1683Z012
BGA1428
COMMON

4/18 FBC

FBCNOTAVAILABLEWITHGM206

FB_DATA
FBC_D[63..0]

{10,11}	FBC_D0	AB5	FBC_D0
	FBC_D1	AB6	FBC_D1
	FBC_D2	AC7	FBC_D2
	FBC_D3	AB4	FBC_D3
	FBC_D4	AA5	FBC_D4
	FBC_D5	AA4	FBC_D5
	FBC_D6	W4	FBC_D6
	FBC_D7	W5	FBC_D7
	FBC_D8	W1	FBC_D8
	FBC_D9	Y3	FBC_D9
	FBC_D10	W2	FBC_D10
	FBC_D11	W3	FBC_D11
	FBC_D12	AB1	FBC_D12
	FBC_D13	AB2	FBC_D13
	FBC_D14	AC3	FBC_D14
	FBC_D15	AB3	FBC_D15
	FBC_D16	V5	FBC_D16
	FBC_D17	V6	FBC_D17
	FBC_D18	V4	FBC_D18
	FBC_D19	T4	FBC_D19
	FBC_D20	P7	FBC_D20
	FBC_D21	R5	FBC_D21
	FBC_D22	R6	FBC_D22
	FBC_D23	R4	FBC_D23
	FBC_D24	P3	FBC_D24
	FBC_D25	R1	FBC_D25
	FBC_D26	R2	FBC_D26
	FBC_D27	R3	FBC_D27
	FBC_D28	U3	FBC_D28
	FBC_D29	V2	FBC_D29
	FBC_D30	V3	FBC_D30
	FBC_D31	V1	FBC_D31
	FBC_D32	D13	FBC_D32
	FBC_D33	G14	FBC_D33
	FBC_D34	E13	FBC_D34
	FBC_D35	F13	FBC_D35
	FBC_D36	D12	FBC_D36
	FBC_D37	E12	FBC_D37
	FBC_D38	E10	FBC_D38
	FBC_D39	D10	FBC_D39
	FBC_D40	B10	FBC_D40
	FBC_D41	C10	FBC_D41
	FBC_D42	A10	FBC_D42
	FBC_D43	C11	FBC_D43
	FBC_D44	C13	FBC_D44
	FBC_D45	A13	FBC_D45
	FBC_D46	D14	FBC_D46
	FBC_D47	B13	FBC_D47
	FBC_D48	D9	FBC_D48
	FBC_D49	D7	FBC_D49
	FBC_D50	G8	FBC_D50
	FBC_D51	E7	FBC_D51
	FBC_D52	G5	FBC_D52
	FBC_D53	F6	FBC_D53
	FBC_D54	E6	FBC_D54
	FBC_D55	D6	FBC_D55
	FBC_D56	C5	FBC_D56
	FBC_D57	B6	FBC_D57
	FBC_D58	C6	FBC_D58
	FBC_D59	A6	FBC_D59
	FBC_D60	C8	FBC_D60
	FBC_D61	C9	FBC_D61
	FBC_D62	A9	FBC_D62
	FBC_D63	B9	FBC_D63

{10}	FBC_DBI<0>	AA6	FBC_DQM0
{10}	FBC_DBI<1>	AA1	FBC_DQM1
{10}	FBC_DBI<2>	U7	FBC_DQM2
{10}	FBC_DBI<3>	T1	FBC_DQM3
{11}	FBC_DBI<4>	F12	FBC_DQM4
{11}	FBC_DBI<5>	A12	FBC_DQM5
{11}	FBC_DBI<6>	H6	FBC_DQM6
{11}	FBC_DBI<7>	A7	FBC_DQM7

{10}	FBC_EDC<0>	AB8	FBC_DQS_WP0
{10}	FBC_EDC<1>	AA2	FBC_DQS_WP1
{10}	FBC_EDC<2>	T5	FBC_DQS_WP2
{10}	FBC_EDC<3>	T2	FBC_DQS_WP3
{11}	FBC_EDC<4>	H13	FBC_DQS_WP4
{11}	FBC_EDC<5>	B12	FBC_DQS_WP5
{11}	FBC_EDC<6>	G7	FBC_DQS_WP6
{11}	FBC_EDC<7>	B7	FBC_DQS_WP7

SNN_FBC_DQS_RN<0>	AA7	FBC_DQS_RN0
SNN_FBC_DQS_RN<1>	AA3	FBC_DQS_RN1
SNN_FBC_DQS_RN<2>	T6	FBC_DQS_RN2
SNN_FBC_DQS_RN<3>	T3	FBC_DQS_RN3
SNN_FBC_DQS_RN<4>	G12	FBC_DQS_RN4
SNN_FBC_DQS_RN<5>	C12	FBC_DQS_RN5
SNN_FBC_DQS_RN<6>	F7	FBC_DQS_RN6
SNN_FBC_DQS_RN<7>	C7	FBC_DQS_RN7

FB_CMD
FBC_CMD[31..0]

	FBC_CMD0	N6	{10,11}
	FBC_CMD1	N5	
	FBC_CMD2	N4	
	FBC_CMD3	N7	
	FBC_CMD4	N8	
	FBC_CMD5	M4	
	FBC_CMD6	M5	
	FBC_CMD7	M6	
	FBC_CMD8	L5	
	FBC_CMD9	L7	
	FBC_CMD10	M8	
	FBC_CMD11	G3	
	FBC_CMD12	F3	
	FBC_CMD13	F1	
	FBC_CMD14	F2	
	FBC_CMD15	G2	
	FBC_CMD16	D4	
	FBC_CMD17	E4	
	FBC_CMD18	F4	
	FBC_CMD19	G4	
	FBC_CMD20	H4	
	FBC_CMD21	D3	
	FBC_CMD22	D1	
	FBC_CMD23	B3	
	FBC_CMD24	C2	
	FBC_CMD25	L3	
	FBC_CMD26	N3	
	FBC_CMD27	M3	
	FBC_CMD28	M1	
	FBC_CMD29	E3	
	FBC_CMD30	D2	
	FBC_CMD31	M2	
	SNN_FBC_CMD<32>	K8	
	SNN_FBC_CMD<33>	K9	
	FBC_DEBUG0	K7	
	FBC_DEBUG1	L8	

FBVDDQ
R568 402 60.4ohm/X 1% DNI
R570 402 60.4ohm/X 1% DNI

{10}	FBC_CLK0	N2	
{10}	FBC_CLK0*	N1	
{11}	FBC_CLK1	A4	
{11}	FBC_CLK1*	B4	

FB_CLK

{10}	FBC_WCK01	V7	
{10}	FBC_WCK01*	U8	
	SNN_FBC_WCKB01	Y8	
	SNN_FBC_WCKB01*	W7	
{10}	FBC_WCK23	Y7	
{10}	FBC_WCK23*	W6	
	SNN_FBC_WCKB23	R8	
	SNN_FBC_WCKB23*	T7	
{11}	FBC_WCK45	E9	
{11}	FBC_WCK45*	F9	
	SNN_FBC_WCKB45	H8	
	SNN_FBC_WCKB45*	H9	
{11}	FBC_WCK67	G11	
{11}	FBC_WCK67*	F10	
	SNN_FBC_WCKB67	H11	
	SNN_FBC_WCKB67*	G10	

FB_WCK

	FBC_PLL_AVDD	P8	{15,4}

FB_PLLVDD

C612 0.1uF/X 16V 10% X7R 402 COMMON

GND

FBVDDQ

R546 10k/X 5% 402 COMMON
R573 10k/X 5% 402 COMMON
CKE*
FBC_CMD30
FBC_CMD14
FBC_CMD29
FBC_CMD13
R569 10k/X 5% 402 COMMON
R547 10k/X 5% 402 COMMON
RST*

GND

GDDR5_BGA170_MIRROR

	0..31	32..63
CMD0	CS*	
CMD1	A3_BA3	
CMD2	A2_BA0	
CMD3	A4_BA2	
CMD4	A5_BA1	
CMD5	WE*	
CMD6	A7_A8	
CMD7	A6_A11	
CMD8	ABI*	
CMD9	A12_RFU	
CMD10	A0_A10	
CMD11	A1_A9	
CMD12	RAS*	
CMD13	RST*	
CMD14	CKE*	
CMD15	CAS*	
CMD32		
CMD34	DBG0	DBG0
CMD16	CS*	
CMD17	A3_BA3	
CMD18	A2_BA0	
CMD19	A4_BA2	
CMD20	A5_BA1	
CMD21	WE*	
CMD22	A7_A8	
CMD23	A6_A11	
CMD24	ABI*	
CMD25	A12_RFU	
CMD26	A0_A10	
CMD27	A1_A9	
CMD28	RAS*	
CMD29	RST*	
CMD30	CKE*	
CMD31	CAS*	
CMD33		
CMD35	DBG1	DBG1

ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
MEMORY: GPU Partition C

GIGABYTE

Title: DDR

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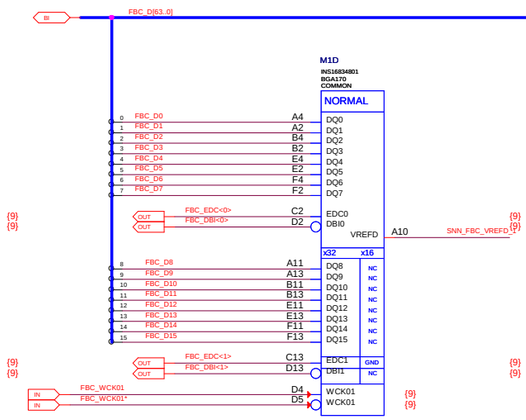
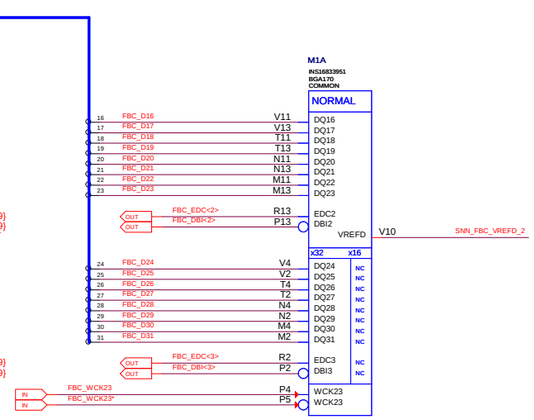
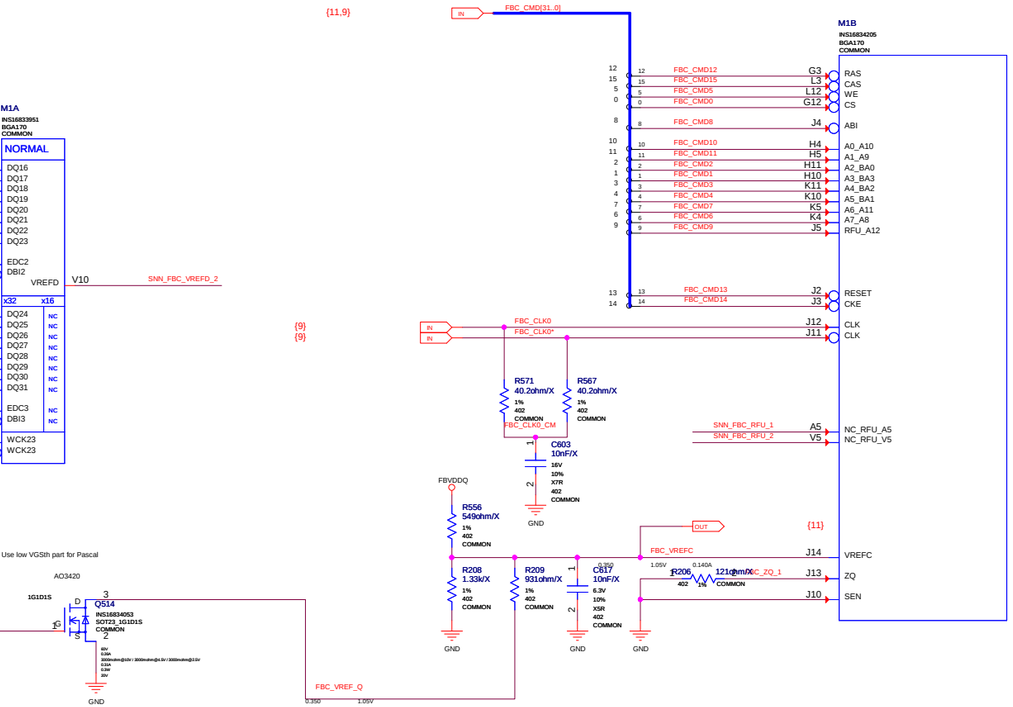
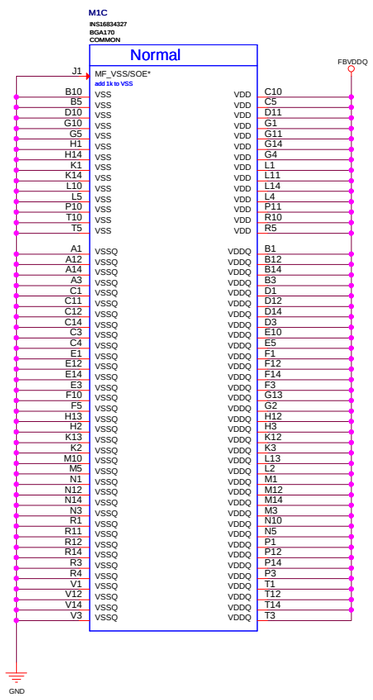
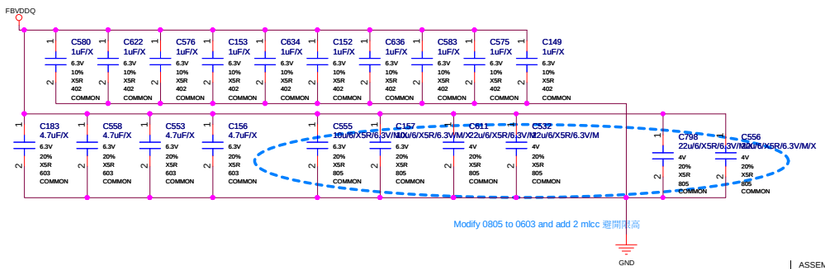
MEMORY: FBC Partition 31..0











ASSEMBLY | BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL | MEMORY: FBC[31:0]

GIGABYTE

Title: DDR

Size: Custom | Document Number: GV-N950XTREME-2GD | Rev: 1.0

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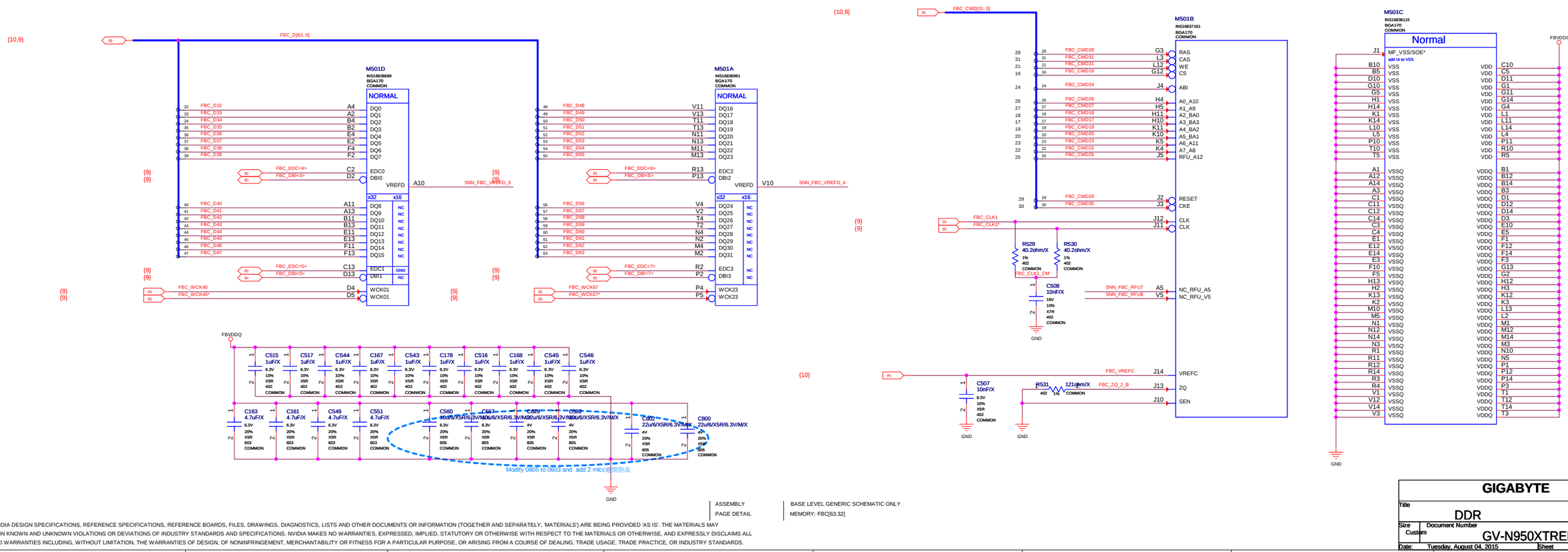
MEMORY: FBC Partition 63..32



ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
MEMORY: FBC[63:32]

GIGABYTE

Title: DDR

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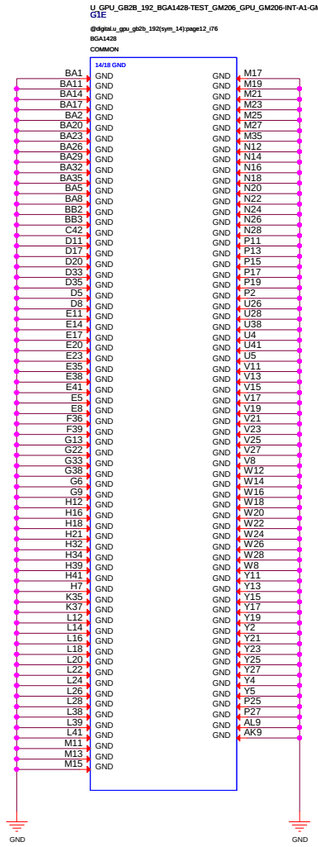
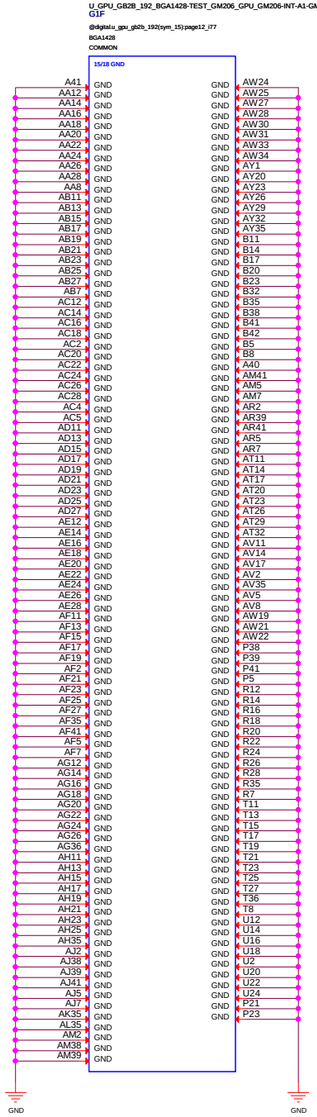
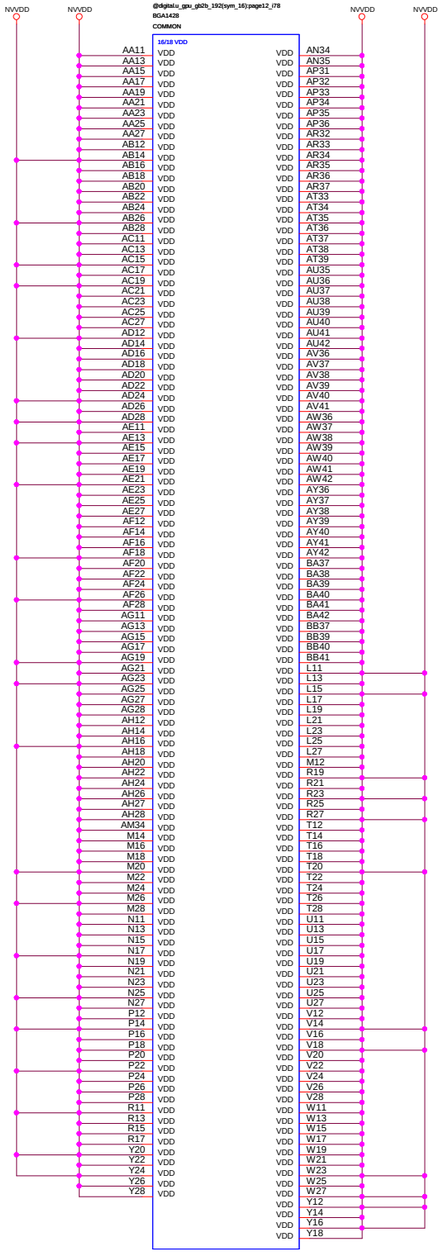
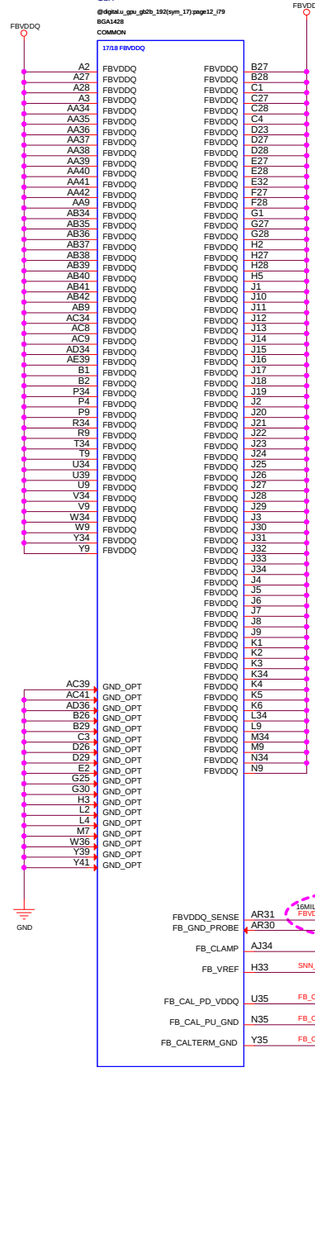
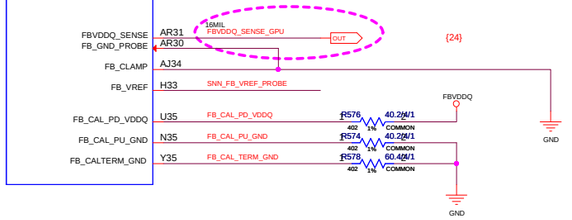
GPU PWR and GND

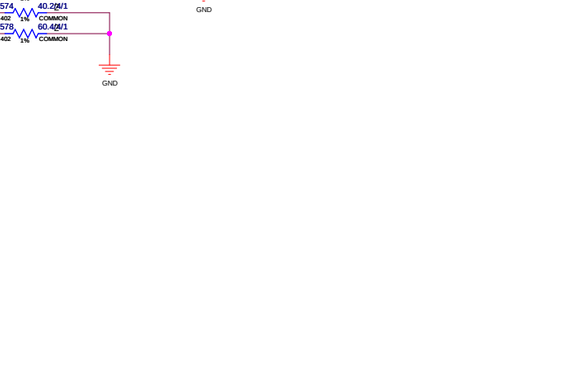












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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	GPU PWR and GND

GIGABYTE

Title: DDR

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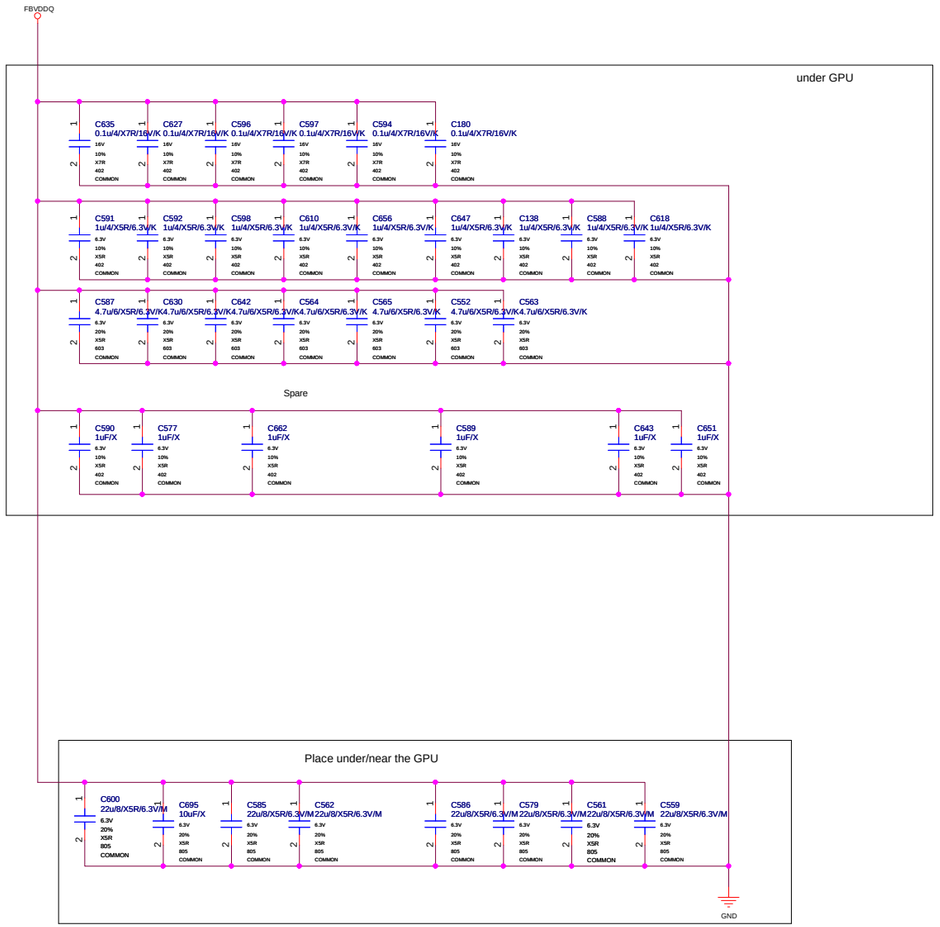
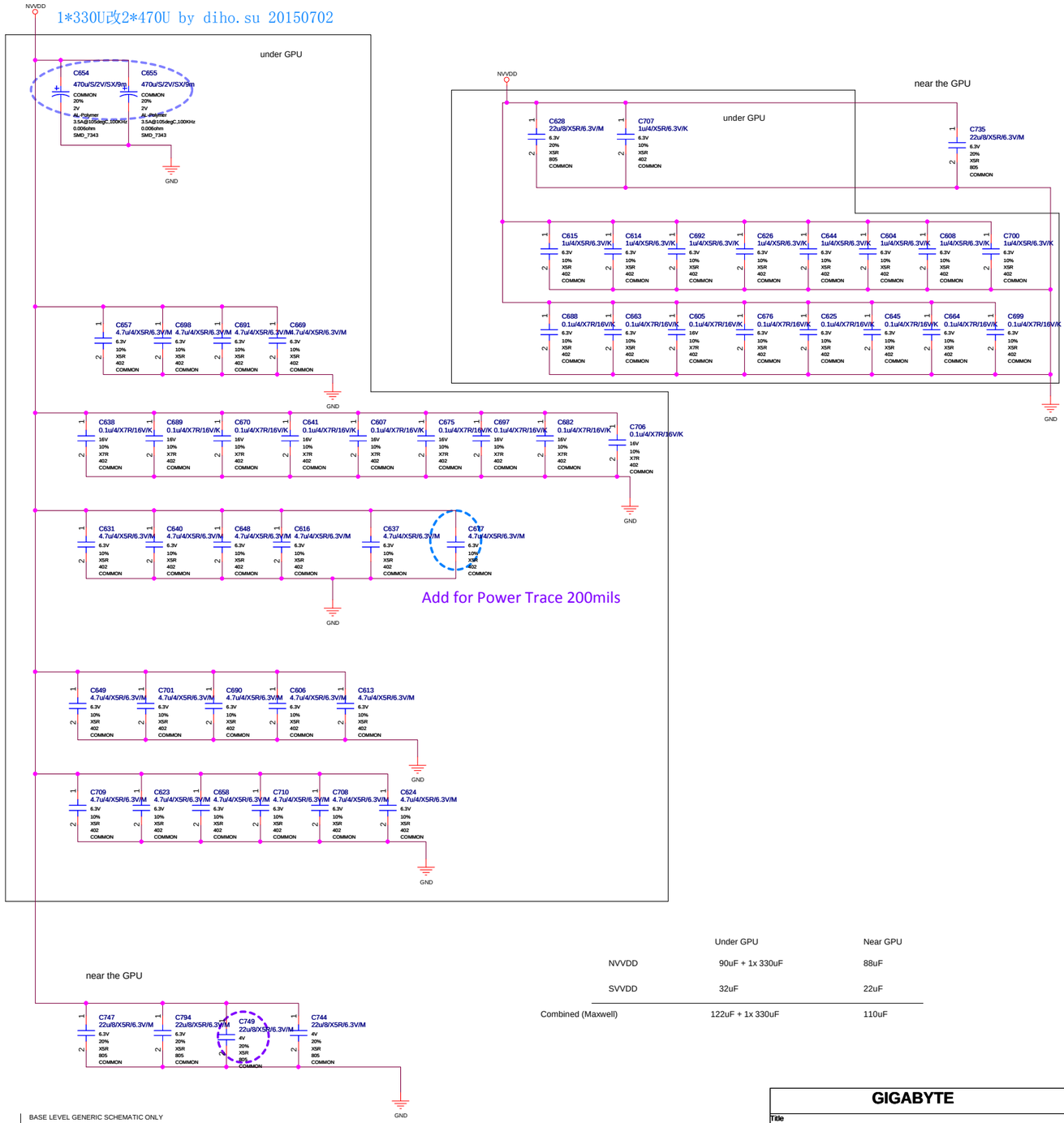
GPU Decoupling

FBVDDQ



NVVDD



	Under GPU	Near GPU
NVVDD	90uF + 1x 330uF	88uF
SVVDD	32uF	22uF
Combined (Maxwell)	122uF + 1x 330uF	110uF

ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
GPU Decoupling

GIGABYTE

Title: DDR

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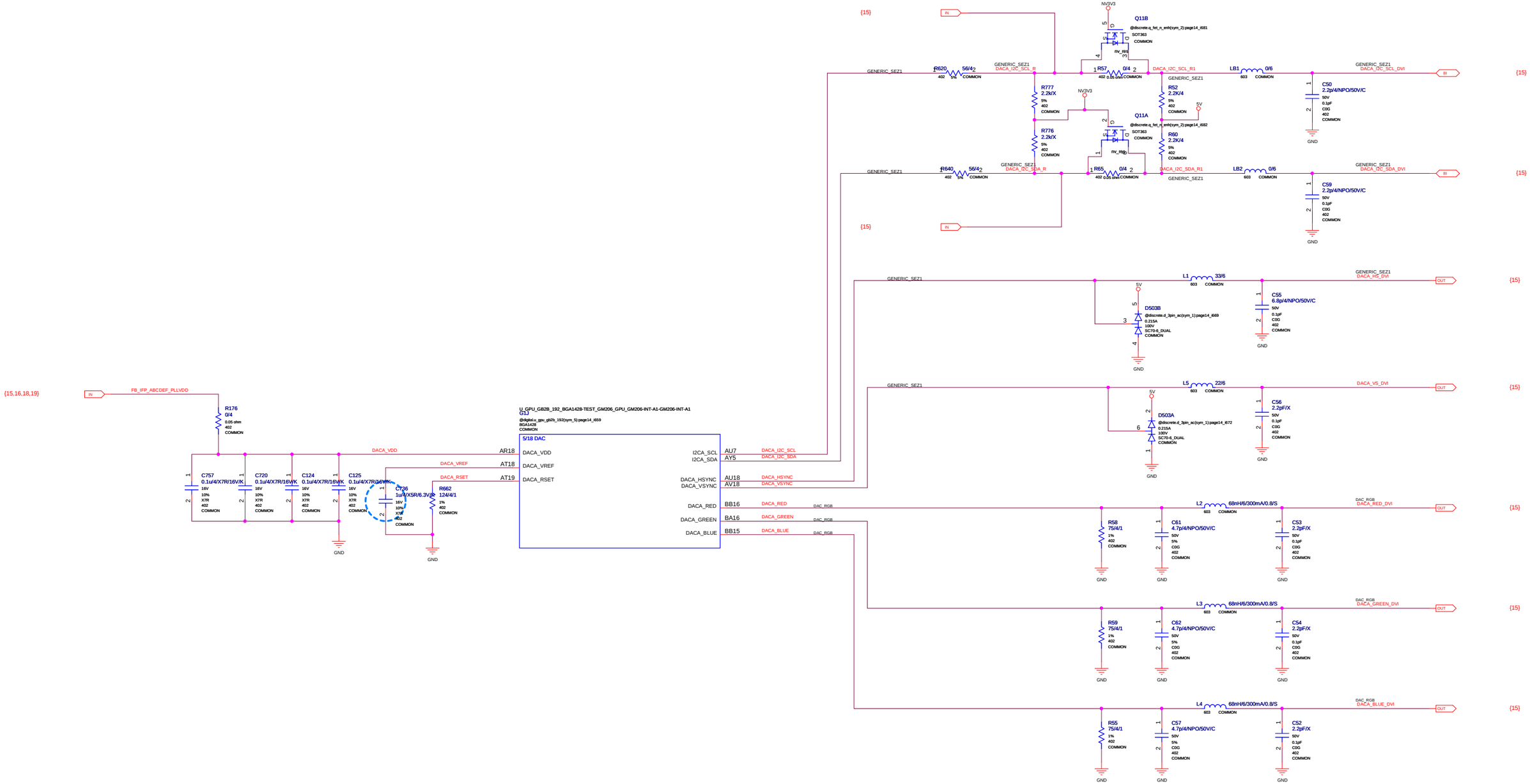
DACA Interface



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	DACA Interface

GIGABYTE

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IFPAB DVI-I-DL

U_GPU_GB2B_192_BGA142B-TEST_GM206_GPU_GM206-INT-A1-GM206-INT-A1
G1K
@sdgdal.u_gpu_gb2b_192(sym_6):page15_i507
BGA142B
COMMON

6/18 IFPAB

GK106 GM206
NC NC
NC NC

DP LVDS/DVI/HDMI

IFPA_AUX_SDA	AP10	IFPA_AUX_SDA		
IFPA_AUX_SCL	AP11	IFPA_AUX_SCL		
IFPB_AUX_SDA	AP12	SNN_IFPB_AUX_SDA		
IFPB_AUX_SCL	AP13	SNN_IFPB_AUX_SCL		
IFPA_TXC	BB10	IFPAB_TXC*	DPA_L3	
IFPA_TXC	BB9	IFPAB_TXC		
IFPA_TXD0	BA9	IFPAB_TXD0*	DPA_L2	
IFPA_TXD0	AY9	IFPAB_TXD0		
IFPA_TXD1	BB13	IFPAB_TXD1*	DPA_L1	
IFPA_TXD1	BB12	IFPAB_TXD1		
IFPA_TXD2	AY10	IFPAB_TXD2*	DPA_L0	
IFPA_TXD2	BA10	IFPAB_TXD2		
IFPA_TXD3	BA12	SNN_IFPAB_TXD3*		
IFPA_TXD3	AY12	SNN_IFPAB_TXD3		
IFPB_TXC	AV16	SNN_IFPB_TXC*	DPB_L3	
IFPB_TXC	AU16	SNN_IFPB_TXC		
IFPB_TXD4	BA13	IFPAB_TXD4*	DPB_L2	
IFPB_TXD4	AY13	IFPAB_TXD4		
IFPB_TXD5	AW13	IFPAB_TXD5*	DPB_L1	
IFPB_TXD5	AY14	IFPAB_TXD5		
IFPB_TXD6	AY15	IFPAB_TXD6*	DPB_L0	
IFPB_TXD6	AW14	IFPAB_TXD6		
IFPB_TXD7	AU15	SNN_IFPAB_TXD7*		
IFPB_TXD7	AV15	SNN_IFPAB_TXD7		

IFPAB

{14} BI DACA_I2C_SDA_DVI
{14} BI

nv_res
GENERIC_SEZ1 — R613 0ohm/X — R645 0ohm/X — nv_res
DACA_I2C_SDA_R
DACA_I2C_SCL_R
{14} BI
{14} BI

DDC_5V
C49 4.7nF/X 16V 10% X5R 402 DNI
GND

J6
DVI-I_(SLIM_)SHLD
DVI_I_SHLD
COMMON

G1	SHIELD1	17	TX0-
G3	SHIELD3	18	TX0+
G4	SHIELD4	9	TX1-
G7	SHIELD7	10	TX1+
17	TX0-	1	TX2-
18	TX0+	2	TX2+
9	TX1-	3	SHLD23
10	TX1+	11	SHLD11
1	TX2-	19	SHLD19
2	TX2+	12	TX3-
3	SHLD23	13	TX3+
11	SHLD11	4	TX4-
19	SHLD19	5	TX4+
12	TX3-	20	TX5-
13	TX3+	21	TX5+
4	TX4-	6	DDCC
5	TX4+	7	DDCD
20	TX5-	14	VDDC
21	TX5+	15	GND
6	DDCC	22	SHLD15
7	DDCD	24	TXC-
14	VDDC	23	TXC+
15	GND	8	VSYNC
22	SHLD15	16	HPD
24	TXC-	C1	R
23	TXC+	C2	G
8	VSYNC	C3	B
16	HPD	C5	AGND1
C1	R	C6	AGND2
C2	G	C4	HSYNC
C3	B	G2	SHIELD2
C5	AGND1	G5	SHIELD5
C6	AGND2	G6	SHIELD6
C4	HSYNC	G8	SHIELD8
G2	SHIELD2		
G5	SHIELD5		
G6	SHIELD6		
G8	SHIELD8		

DACA_I2C_SCL_DVI
DACA_V5_DVI
DVIA_HPD_C
DACA_RED_DVI
DACA_GREEN_DVI
DACA_BLUE_DVI
DACA_HS_DVI
{14}

FB_PLLVDD IN {4,9}
IOVDD
Maxwell — R579 0/6 0.05 ohm 603 COMMON Colayout — LB502 30ohm/X COMMON BEAD_0603 — Kepler
PEX_VDD — Kepler — R173 0ohm/X 0.05 ohm 603 COMMON
R661 1K/4 402 1% COMMON — IFPAB_RSET — AT16 IFPAB_RSET
GND
R174 0/4 2 402 0.05 ohm COMMON — Unstuff for Kepler
IFPAB_PLLVDD — AR17 IFPAB_PLLVDD
C719 1u/4/X5R/6.3V/K 6.3V 10% X5R 402 COMMON
C128 0.1u/4/X7R/16V/K 16V 10% X7R 402 COMMON
FB_IFP_ABCDEF_PLLVDD OUT {14,16,18,19}
GND

PEX_VDD — R172 0/4 0.05 ohm 402 COMMON — Maxwell
3V3_BLK — R171 0ohm/X 0.05 ohm 402 COMMON — Kepler
AT15 IFPAB_IOVDD
AR16 IFPAB_IOVDD
AR14 IFPB_IOVDD
AR15 IFPB_IOVDD
IFPAB_IOVDD
C121 4.7u/6/X5R/6.3V/K 6.3V 20% X5R 603 COMMON
C718 1u/4/X5R/6.3V/K 6.3V 10% X5R 402 COMMON
C717 0.1u/4/X7R/16V/K 16V 10% X7R 402 COMMON
C127 0.1u/4/X7R/16V/K 16V 10% X7R 402 COMMON
GND

DP_SIGNALS
C962 C957 C931 C933 C929 C930 C927 C928 C935 C944 C926 C925 C948 C952
0.1u/4/X7R/16V/K 16V 10% X7R 402 COMMON

NV3V3
R63 10K/4 5% 402 COMMON
{21} OUT GPIO14_IFPA_HPD
Q520 @discrete.q_npn(sch_1):page15_i384 SOT23_18LC1E COMMON
DVIA_HPD_R_Q
R62 100K/4 402 5% COMMON
DVIA_HPD_R
R61 100K/4 5% 402 COMMON
C63 220pf/4/NPO/50V/J 50V 5% C0G 402 COMMON
PLACE CLOSE TO CONNECTOR
R51 0/6 603 0.05 ohm COMMON
C58 220pF/X 50V 5% C0G 402 DNI
GND

IFPAB_TERM_CM 0.406 0V
1G1D1S
Q522 @discrete.q_fet_n_enh(sym_2):page15_i384 SOT23_1G1D1S COMMON
60v 0.80A 2000mohm@10V/ 1600mohm@4.5V/ 3000mohm@2.5V 0.01A 0.5W 40pF
GND

R833 IFPAB_TXC_C+
R832 IFPAB_TXC_C
R795 IFPAB_TXD0_C+
R796 IFPAB_TXD0_C
R784 IFPAB_TXD1_C+
R790 IFPAB_TXD1_C
R780 IFPAB_TXD2_C+
R783 IFPAB_TXD2_C
R804 IFPAB_TXD4_C+
R803 IFPAB_TXD4_C
R778 IFPAB_TXD5_C+
R779 IFPAB_TXD5_C
R812 IFPAB_TXD6_C+
R824 IFPAB_TXD6_C
100/4/1 1% 402 COMMON

ASSEMBLY
PAGE DETAIL
BASE LEVEL GENERIC SCHEMATIC ONLY
IFPAB DVI-I-DL

GIGABYTE

Title: DDR

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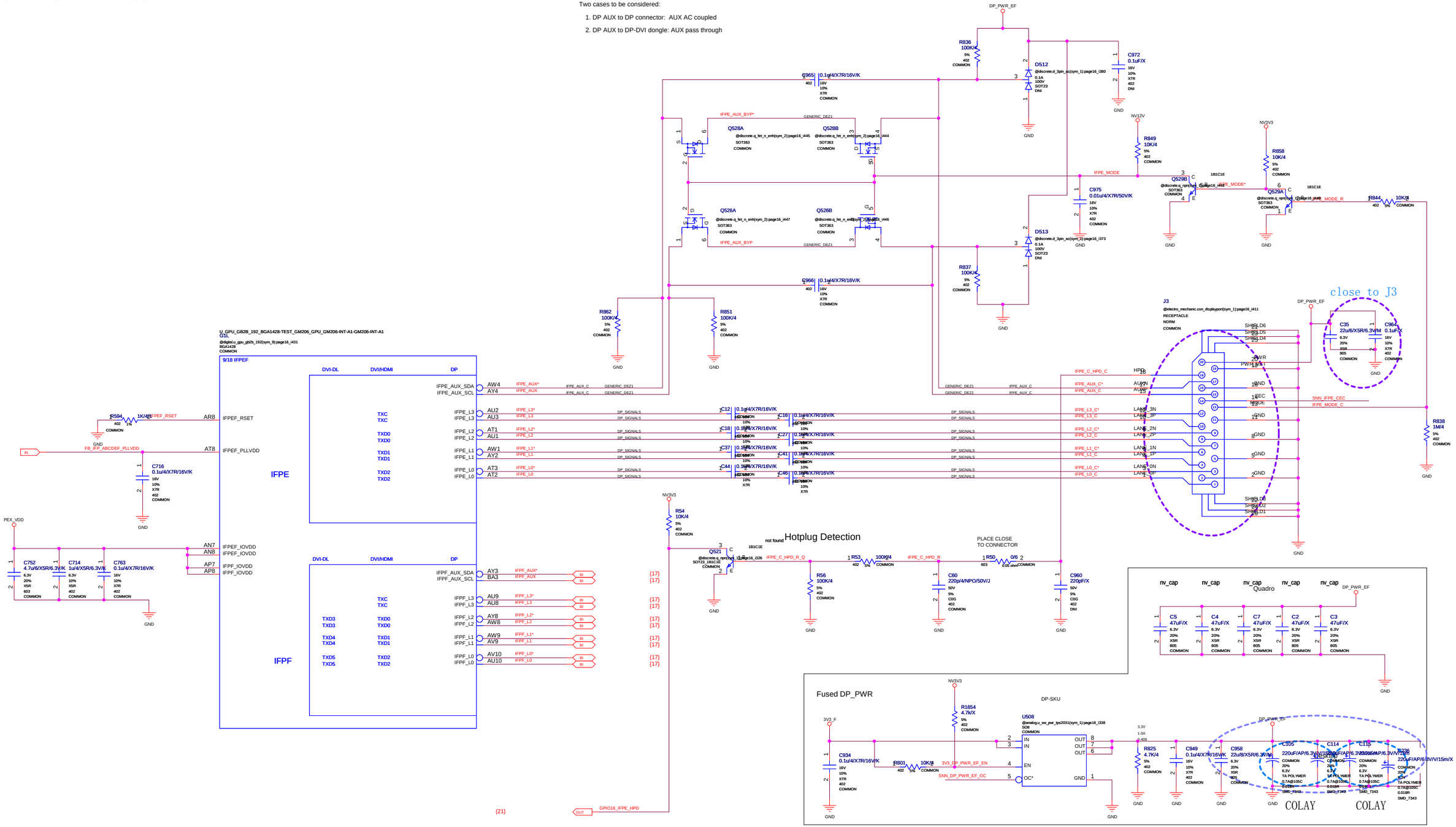
Page18: IFPEF with IFPE DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	IFPEF with IFPE DP

GIGABYTE

Title: DDR

Size	Document Number	Rev
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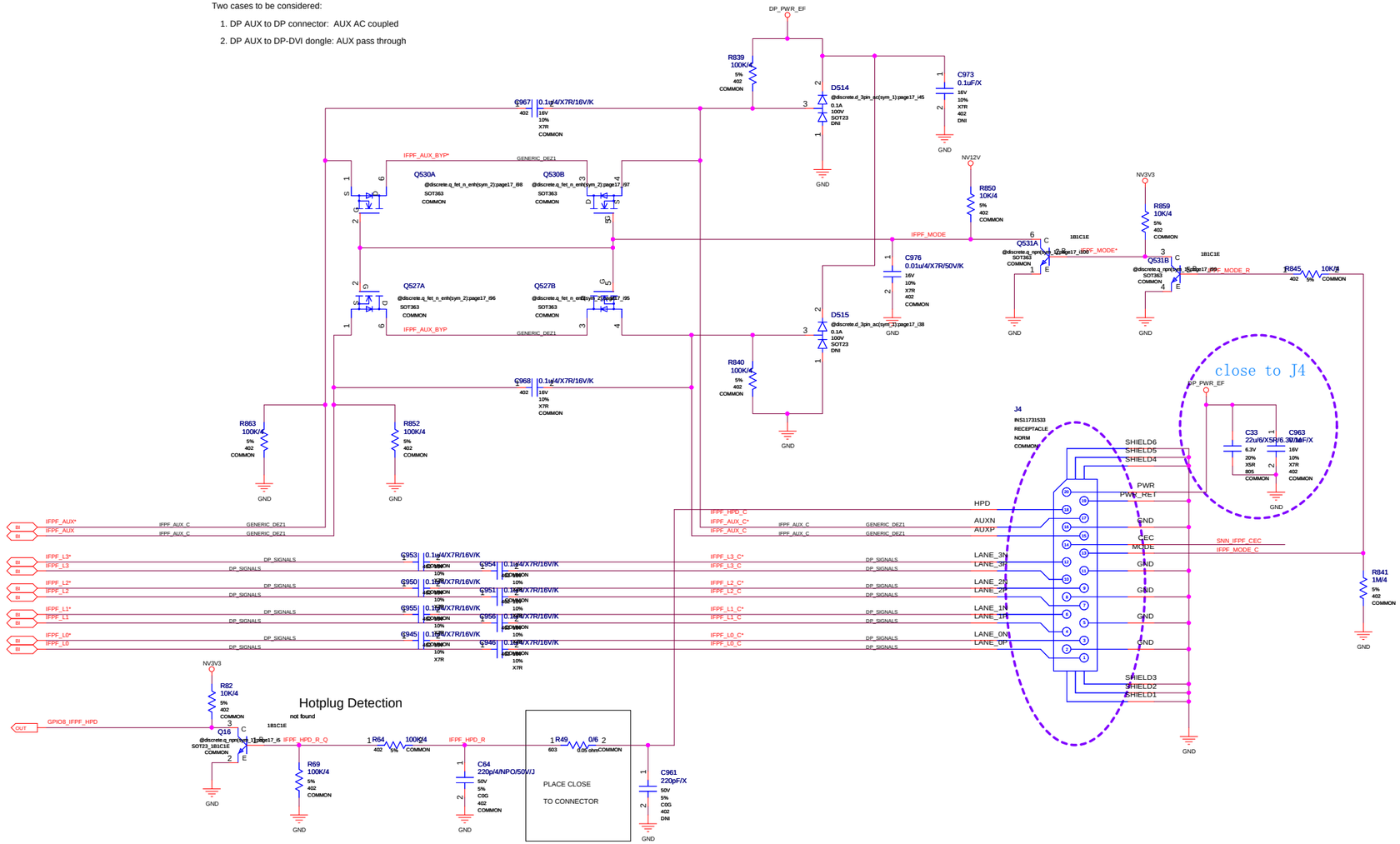
IFPF DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



ASSEMBLY | BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL | IFPF DP

GIGABYTE

Title: DDR

Size: Custom | Document Number: GV-N950XTREME-2GD | Rev: 1.0

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Page20: IFPC HDMI/DP

* I2C to DDC level switching

FOR ESD DIODES

IFPC_ESD

C947 0.1uF/X 16V 10% X7R 402 DNI

GND

Place near ESD diodes

DP-SKU ONLY

U_GPU_GB2B_192_BGA1428-TEST_GM206_GPU_GM206-INT-A1-GM206-INT-A1 G1M
@digital:u_gpu_gb2b_192(sym_7):page18_I192
BGA1428
COMMON

7/18 IFPC

IFPC

DVI/HDMI

DP

AT12 IFPCD_RSET — R639 1K/4/1 1% 402 COMMON — IFPC_RSET

AT13 IFPCD_PLLVDD — C728 0.1u/4/X7R/16V/K 16V 10% X7R 402 COMMON — FB_IFP_ABCDEF_PLLVDD — IN — {14,15,16,19}

AR10 IFPCD_IOVDD
AR11 IFPCD_IOVDD

PEX_VDD

C711 4.7u/6/X5R/6.3V/K 6.3V 20% X5R 603 COMMON
C725 0.1u/4/X7R/16V/K 16V 10% X7R 402 COMMON
C715 0.1u/4/X7R/16V/K 16V 10% X7R 402 COMMON

TXC / TXC
TXD0 / TXD0
TXD1 / TXD1
TXD2 / TXD2

IFPC_L3	AW10	IFPC_TXC*	DVI_HDMI_SIGNALS
IFPC_L3	AY11	IFPC_TXC	DVI_HDMI_SIGNALS
IFPC_L2	AW12	IFPC_TXD0*	DVI_HDMI_SIGNALS
IFPC_L2	AW11	IFPC_TXD0	DVI_HDMI_SIGNALS
IFPC_L1	AV12	IFPC_TXD1*	DVI_HDMI_SIGNALS
IFPC_L1	AU12	IFPC_TXD1	DVI_HDMI_SIGNALS
IFPC_L0	AV13	IFPC_TXD2*	DVI_HDMI_SIGNALS
IFPC_L0	AU13	IFPC_TXD2	DVI_HDMI_SIGNALS

IFPC_AUX_SDA — AV3 — I2CW_AUX*
IFPC_AUX_SCL — AV4 — I2CW_AUX

{21}

IFPC_MODE_O*

ALL

Q5A / Q6B — @discrete:q_fet_n_enh(sym_2):page18_I208 — SOT363 COMMON

Q5B / Q6A — @discrete:q_fet_n_enh(sym_2):page18_I208 — SOT363 COMMON

NV3V3

R11 10K/4 5% 402 COMMON — HDMI — DVI_HDMI_SIGNALS — I2CW_SDA_Q — R826 0/4 0.05 ohm 402 COMMON — HDMI — C14 0.1uF/X 16V 10% X7R 402 COMMON — DP
R13 100k/X 5% 402 COMMON — DP

R21 10K/4 5% 402 COMMON — HDMI — DVI_HDMI_SIGNALS — I2CW_SCL_Q — R813 0/4 0.05 ohm 402 COMMON — HDMI — C28 0.1uF/X 16V 10% X7R 402 COMMON — DP
R29 100k/X 5% 402 COMMON — DP

GND

DDC_5V — DP_PWR

R843 0ohm/X 0.05 ohm 402 COMMON — HDMI
R842 0ohm/X 0.05 ohm 402 COMMON — DP

C13 0.01u/4/X7R/50V/K 16V 10% X7R 402 COMMON

R16 0/4 0.05 ohm 402 COMMON — HDMI

R831 100k/X 5% 402 COMMON — DP_PWR

IFPC_ESD

D508 @discrete:d_3pin_ac(sym_1):page18_I47 0.1A 100V SOT23 DNI
D511 @discrete:d_3pin_ac(sym_1):page18_I58 0.1A 100V SOT23 DNI

DDC_5V

R829 2K/4 5% 402 COMMON — HDMI
R809 2K/4 5% 402 COMMON — HDMI

R807 100k/X 5% 402 COMMON — DP

C969 100pF/X 50V 5% C0G 402 DNI

J5
RECEPTACLE HDMI_R_SMD
@electro_mechanic:con_hdmi(sym_1):page18_I75
COMMON

20	SHIELD1		
21	SHIELD2		
19	HP_DET		
18	+5V	19	
17	DDC/CEC_GND	18	
16	SDA	17	
15	SCL	16	
14	RESERVED	15	
13	CEC	14	
12	CK-	13	
11	CK_SHIELD	12	
10	CK+	11	
9	D0-	10	
8	D0_SHIELD	9	
7	D0+	8	
6	D1-	7	
5	D1_SHIELD	6	
4	D1+	5	
3	D2-	4	
2	D2_SHIELD	3	
1	D2+	2	
22	SHIELD3	1	
23	SHIELD4		

USE NVPN 080-0424-000

nv_res — I2CW_SDA_C — I2CW_SCL_C

R1663	5.1/4	SNN_HDMI_RSVD1	
R1666	5.1/4	SNN_CEC_C	
R1661	5.1/4	IFPC_TXC_RC1*	IFPC_TXC*
R1667	5.1/4	IFPC_TXC_RC1	IFPC_TXC
R1662	5.1/4	IFPC_TXD0_RC1*	IFPC_TXD0*
R1665	5.1/4	IFPC_TXD0_RC1	IFPC_TXD0
R1660	5.1/4	IFPC_TXD1_RC1*	IFPC_TXD1*
R1664	5.1/4	IFPC_TXD1_RC1	IFPC_TXD1
		IFPC_TXD2_RC1*	IFPC_TXD2*
		IFPC_TXD2_RC1	IFPC_TXD2

C936–C943 0.1u/4/X7R/16V/K 16V 10% X7R 402 COMMON — IFPC_TXC_C1* / IFPC_TXC_C1 / IFPC_TXD0_C1* / IFPC_TXD0_C1 / IFPC_TXD1_C1* / IFPC_TXD1_C1 / IFPC_TXD2_C1* / IFPC_TXD2_C1

NV3V3

R5 10K/4 5% 402 COMMON — HDMI_C_HPD_R_Q — not found

GPIO15_IFPC_HPD — OUT

Q2 @discrete:q_npn(sym_1):page18_I88 SOT23_1B1C1E COMMON — 1B1C1E

R847 100K/4 5% 402 COMMON — HDMI_C_HPD_R

R846 0/6 0.05 ohm 603 COMMON — HDMI_C_HPD_C

C970 220/4/NPO/50V/J 50V 5% C0G 402 COMMON

C971 220pF/X 50V 5% C0G 402 DNI

R848 100K/4 5% 402 COMMON

GND

nv_ind_noxnet

R823	499/4/1	
R822	499/4/1	
R821	499/4/1	
R820	499/4/1	
R819	499/4/1	
R818	499/4/1	
R817	499/4/1	
R816	499/4/1	

1% 402 COMMON

LB40 LB41 LB42 LB43 LB44 LB45 LB46 LB47 — 600/4/500mA/S — BEAD_0402 COMMON

DP FOR QUADRO

del DP colay by diho.su 20150702

Fused DP_PWR

DP-SKU

NV3V3

R1655 4.7k/X 5% 402 COMMON

3V3_F

C974 0.1u/4/X7R/16V/K 16V 10% X7R 402 COMMON

R855 10K/4 5% 402 COMMON — 3V3_DP_PWR_EN — SNN_DP_PWR_OC

U510 @analog:u_sw_pwr_tps2031(sym_1):page18_I164 SO8 COMMON
IN / IN — EN — OC* — OUT / OUT / OUT — GND

3.3V 1.0A 0.406

R7 4.7K/4 5% 402 COMMON

C6 0.1u/4/X7R/16V/K 16V 10% X7R 402 COMMON

C8 22u/6/X5R/6.3V/M 6.3V 20% X5R 603 COMMON

DP_PWR

C233 220uF/AP/6.3V/V/15m 6.3V 20% TA POLYMER 0.7A@105C 0.018R SMD_7343 COMMON
C120 220uF/AP/6.3V/V/15m 6.3V 20% TA POLYMER 0.7A@105C 0.018R SMD_7343 COMMON
C235 220uF/AP/6.3V/V/15m 6.3V 20% TA POLYMER 0.7A@105C 0.018R SMD_7343 COMMON
C116 220uF/AP/6.3V/V/15m 6.3V 20% TA POLYMER 0.7A@105C 0.018R SMD_7343 COMMON

COLAY

IFPC_TERM_EN_D — 0V 0.406

Q523 @discrete:q_fet_n_enh(sym_2):page18_I104 SOT723_1G1D1S COMMON — 1G1D1S

ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
IFPC HDMI/DP

GIGABYTE

Title: DDR

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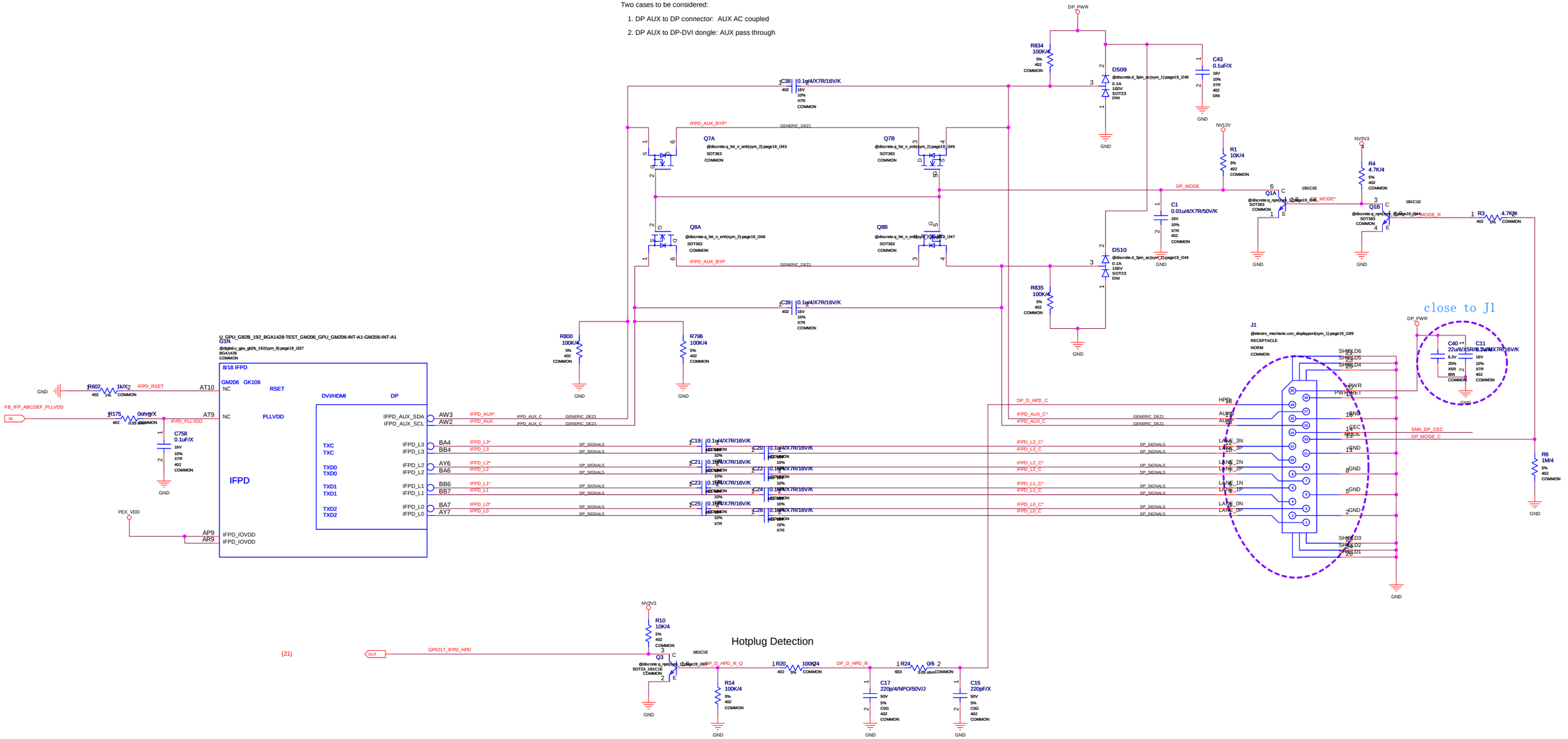
IFPD DP

Two cases to be considered:

1. DP AUX to DP connector: AUX AC coupled
2. DP AUX to DP-DVI dongle: AUX pass through



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY	
PAGE DETAIL	IFPD DP	

GIGABYTE

Title	DDR		
Size: Custom	Document Number: GV-N950XTREME-2GD		Rev: 1.0
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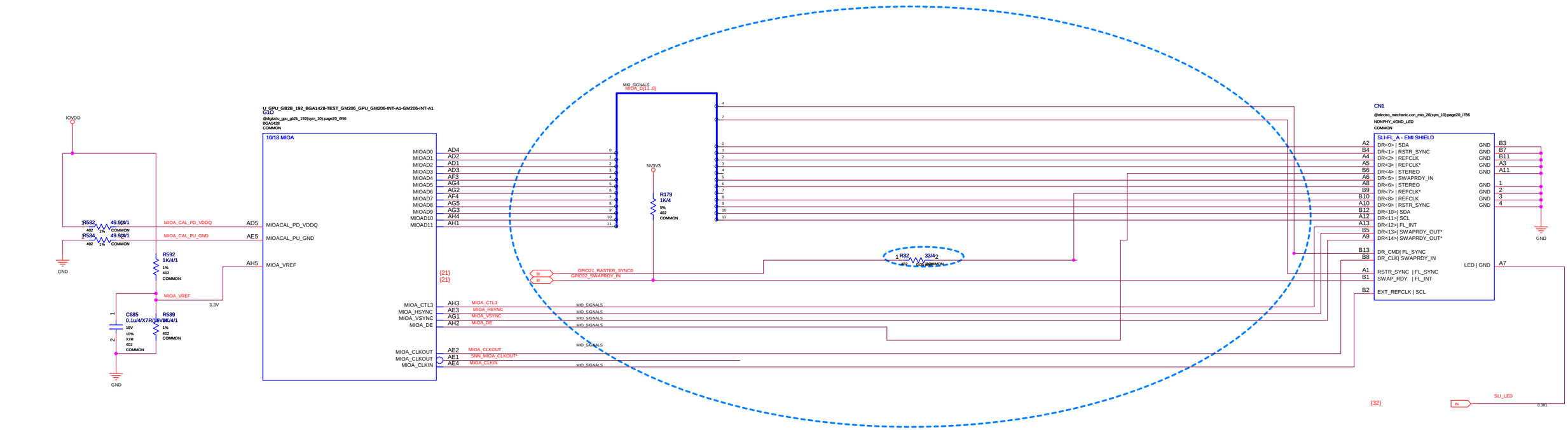
MIOA/SLI Interface

DEL MIO RESERVER CIRCUIT



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
IN MIOA_VREF	3.3V		0.305
IN MIOA_CAL_PD_VDDQ	2.5V		0.305
IN MIOA_CAL_PU_GND	0.0V		0.305

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MIOA

GIGABYTE

Title: DDR

Size: Custom | Document Number: GV-N950XTREME-2GD | Rev: 1.0

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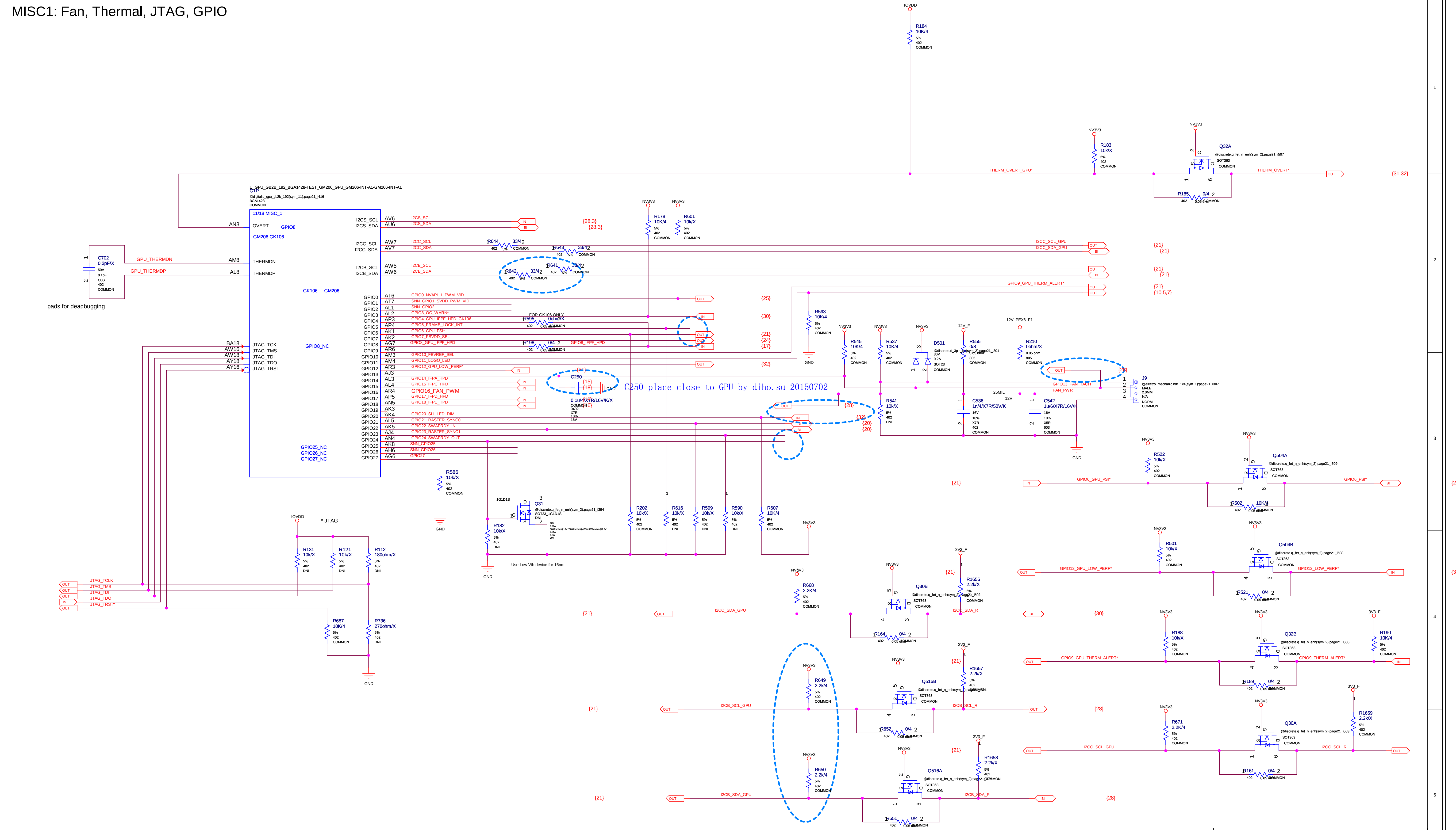
MISC1: Fan, Thermal, JTAG, GPIO



ASSEMBLY | BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL | MISC1: Fan, Thermal, JTAG, GPIO

GIGABYTE

Title: DDR

Size: Custom | Document Number: GV-N950XTREME-2GD | Rev: 1.0

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MISC2: ROM, XTAL, Straps

	KEPLER	MAXWELL
STRAP0	USER_BIT [3:0]*	
STRAP1	3GIO_PADCFG_LUT_ADR*	
STRAP2	PCI_DEVID [3:0]*	
STRAP3	SOR_EXPOSED [3:0]*	
STRAP4	DP_PLL_VDD_33V*	
	PEX_MAX_SPEED*	
	PEX_SPD_CHANGE_GEN3*	
	*	
ROM_SI	RAMCFG[0]*	RAMCFG[0]*
	RAMCFG[1]*	RAMCFG[1]*
	RAMCFG[2]*	RAMCFG[2]*
	RAMCFG[3]*	RAMCFG[3]*
ROM_SO	VGA_DEVICE*	VGA_DEVICE*
	SMB_ALT_ADDR*	SMB_ALT_ADDR*
	FB[0]_APERTURE_SIZE*	PCIE_CFG*
	FB[1]_APERTURE_SIZE*	DEVID_SEL*
ROM_SCLK	PEX_PLL_EN_TERM100*	SOR0_EXPOSED*
	PCI_DEVID_EXT[5]*	SOR1_EXPOSED*
	SUB_VENDOR*	SOR2_EXPOSED*
	PCI_DEVID_EXT[4]*	SOR3_EXPOSED*

	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

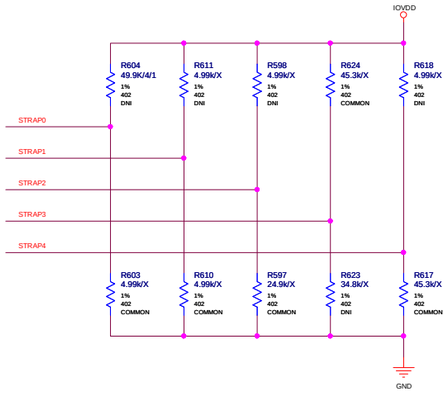
MULTI_STRAP_REF0_GND

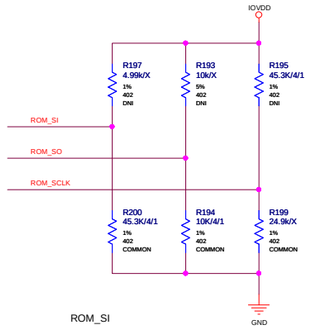
BINARY PRODUCTION	NC
BINARY BRINGUP	NC
MULTI-LEVEL	40.2k 1% TO GND

MAXWELL

STRAP0

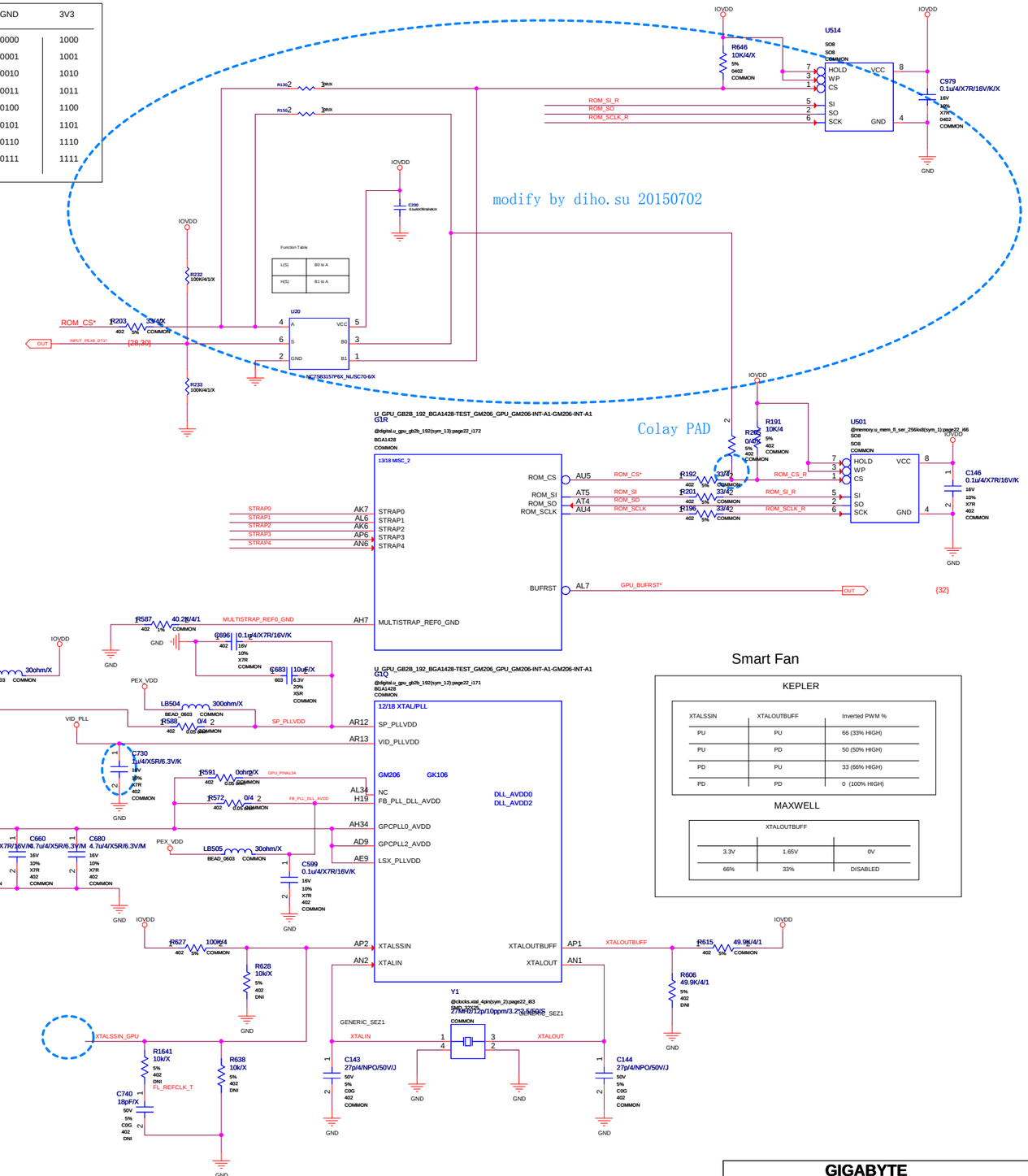
3.3V	1.65V	0V
GC6+ ISLAND ENABLED	GC6+ DEBUG MODE	GC6+ ISLAND DISABLED





ROM_SI

SAMSUNG	HYNIX	ELPIDA
45.3k PD	34.8k PD	30.1k PD



Smart Fan

KEPLER

XTALSSIN	XTALOUTBUFF	Inverted PWM %
PU	PU	66 (33% HIGH)
PU	PD	50 (50% HIGH)
PD	PU	33 (66% HIGH)
PD	PD	0 (100% HIGH)

MAXWELL

XTALOUTBUFF		
3.3V	1.65V	0V
66%	33%	DISABLED

ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MISC2: ROM, XTAL, Straps

GIGABYTE

Title: DDR

Size: Custom | Document Number: GV-N950XTREME-2GD | Rev: 1.0

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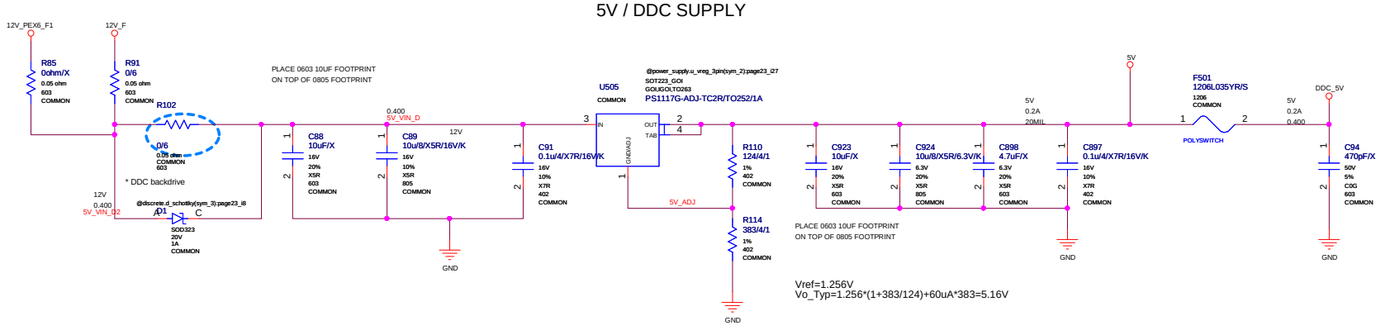
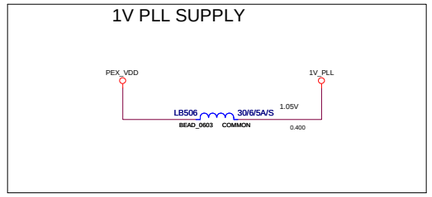
PS: 5V, PEX_VDD

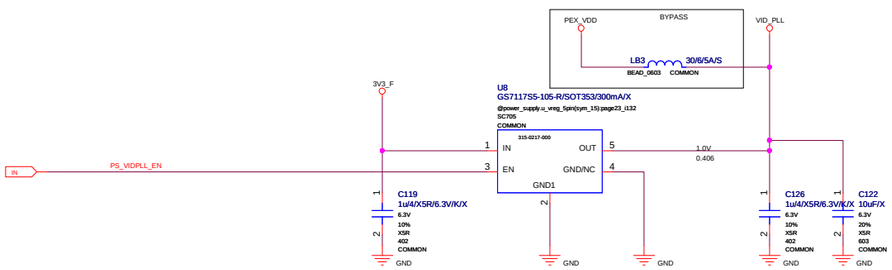
5V / DDC SUPPLY



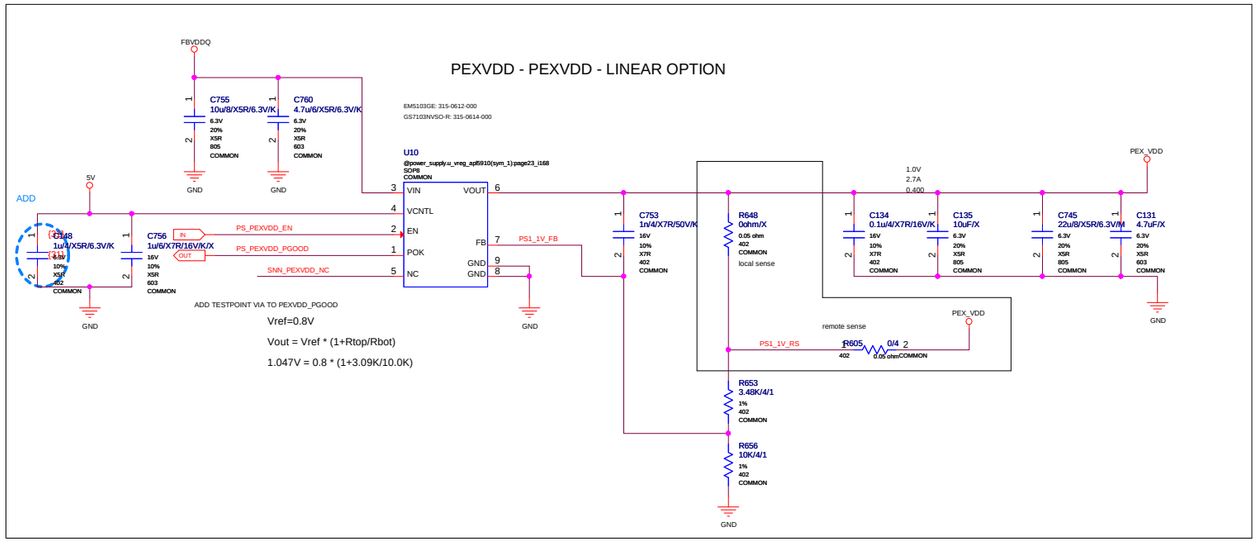
1V PLL SUPPLY



VID PLL SUPPLY



PEXVDD - PEXVDD - LINEAR OPTION



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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: 5V, PEX_VDD, VID_PLL

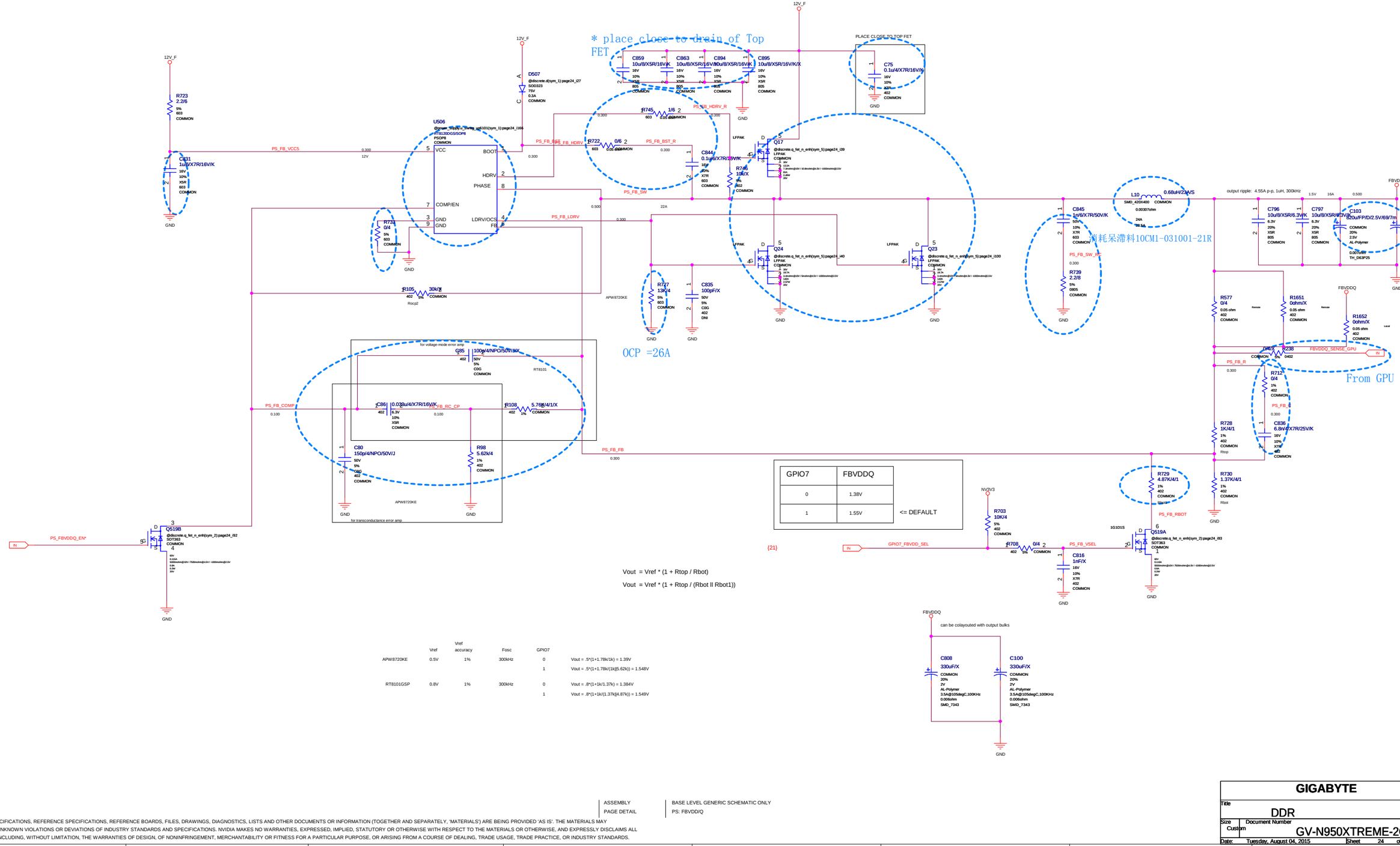
GIGABYTE

Title: DDR

Size: Custom | Document Number: GV-N950XTREME-2GD | Rev: 1.0

Date: Tuesday, August 04, 2015 | Sheet 23 of 34

PS: FBVDDQ



GPIO7	FBVDDQ
0	1.38V
1	1.55V

<= DEFAULT

Vout = Vref * (1 + Rtop / Rbot)

Vout = Vref * (1 + Rtop / (Rbot ll Rbot1))

	Vref	Vref accuracy	Fosc	GPIO7	
APW8720KE	0.5V	1%	300kHz	0	Vout = .5*(1+1.78k/1k) = 1.39V
				1	Vout = .5*(1+1.78k/(1k||5.62k)) = 1.548V
RT8101GSP	0.8V	1%	300kHz	0	Vout = .8*(1+1k/1.37k) = 1.384V
				1	Vout = .8*(1+1k/(1.37k||4.87k)) = 1.549V

FBVDDQ

can be colayouted with output bulks

C808 330uF/X

C100 330uF/X

ASSEMBLY

PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY

PS: FBVDD/Q

GIGABYTE

Title: DDR

Size: Custom | Document Number: GV-N950XTREME-2GD | Rev: 1.0

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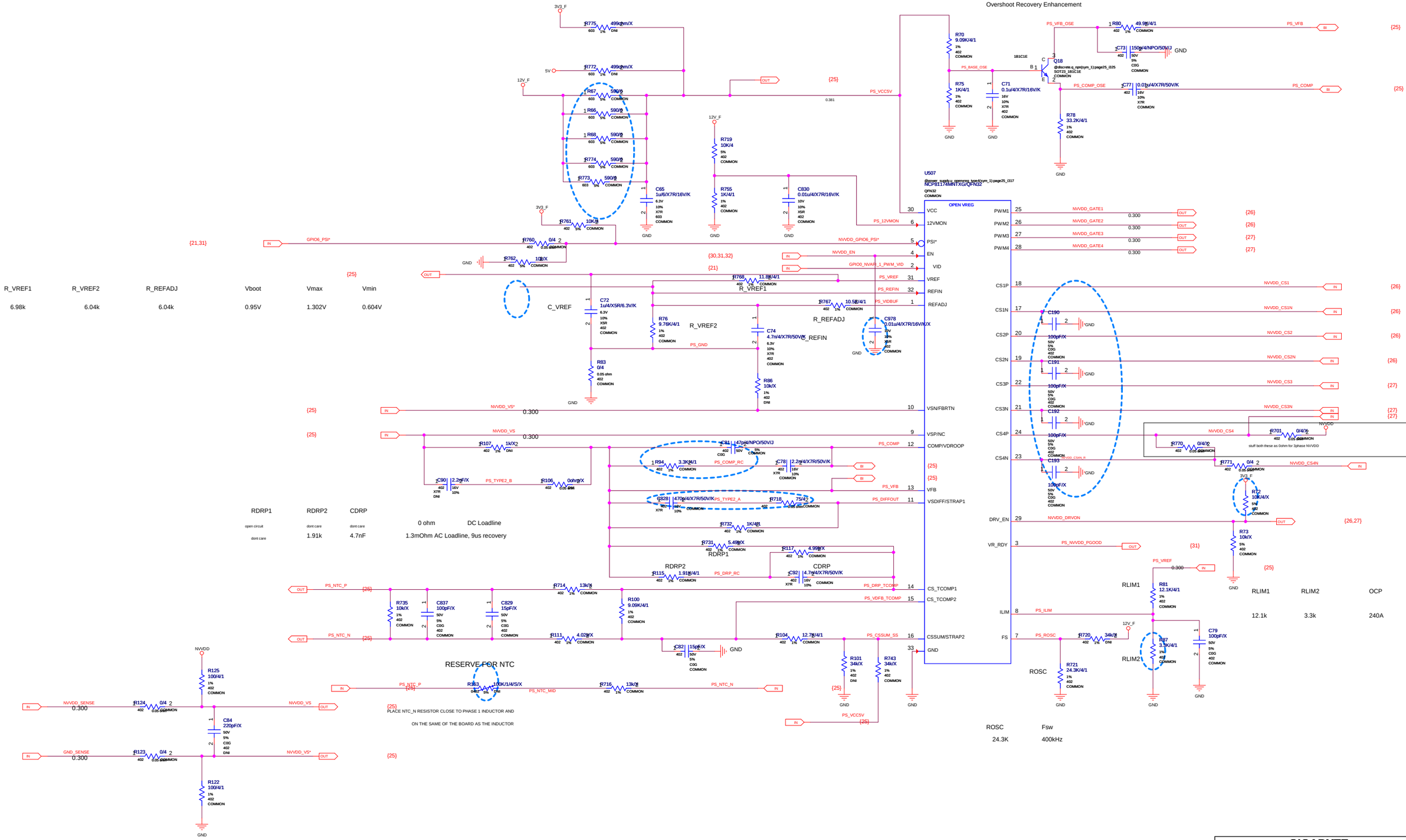
PS: NVVDD Controller



ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
PS: NVVDD Controller OVR4 option

GIGABYTE		
Title: DDR		
Size: Custom	Document Number: GV-N950XTREME-2GD	Rev: 1.0
Date: Tuesday, August 04, 2015	Sheet 25 of 34	

PS: NVVDD Phase 1,2

* place close to drain of Top FET

* place close to drain of Top FET

Place on PWM Side

Place on PWM Side

新增

colayout

colayout

colayout resistors

PLACE 0603 1UF FOOTPRINT ON TOP OF 0805 FOOTPRINT

PLACE 0603 1UF FOOTPRINT ON TOP OF 0805 FOOTPRINT

{25,26,27}

{27}

{25}

{25}

{25}

{25}

{27}

* place close to drain of Top FET

* place close to drain of Top FET

海耗呆滞料10CM1-031001-21R

海耗呆滞料10CM1-031001-21R

ASSEMBLY

PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY

PS: NVVDD Phase 1,2

GIGABYTE			
Title: DDR			
Size: Custom	Document Number: GV-N950XTREME-2GD		Rev: 1.0
Date: Tuesday, August 04, 2015	Sheet 26 of 34		

PS: NVVDD Phase 3,4

* place close to drain of Top FET

* place close to drain of Top FET

Place on PWM Side

Place on PWM Side

* place close to drain of Top FET

* place close to drain of Top FET

stuff 0ohm for 3phase

PLACE 0603 1UF FOOTPRINT ON TOP OF 0805 FOOTPRINT

PLACE 0603 1UF FOOTPRINT ON TOP OF 0805 FOOTPRINT

消耗呆滯料10CM1-031001-21R

消耗呆滯料10CM1-031001-21R

上件phase4 by diho.su 20150702

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ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	PS: NVVDD Phase 3,4

GIGABYTE

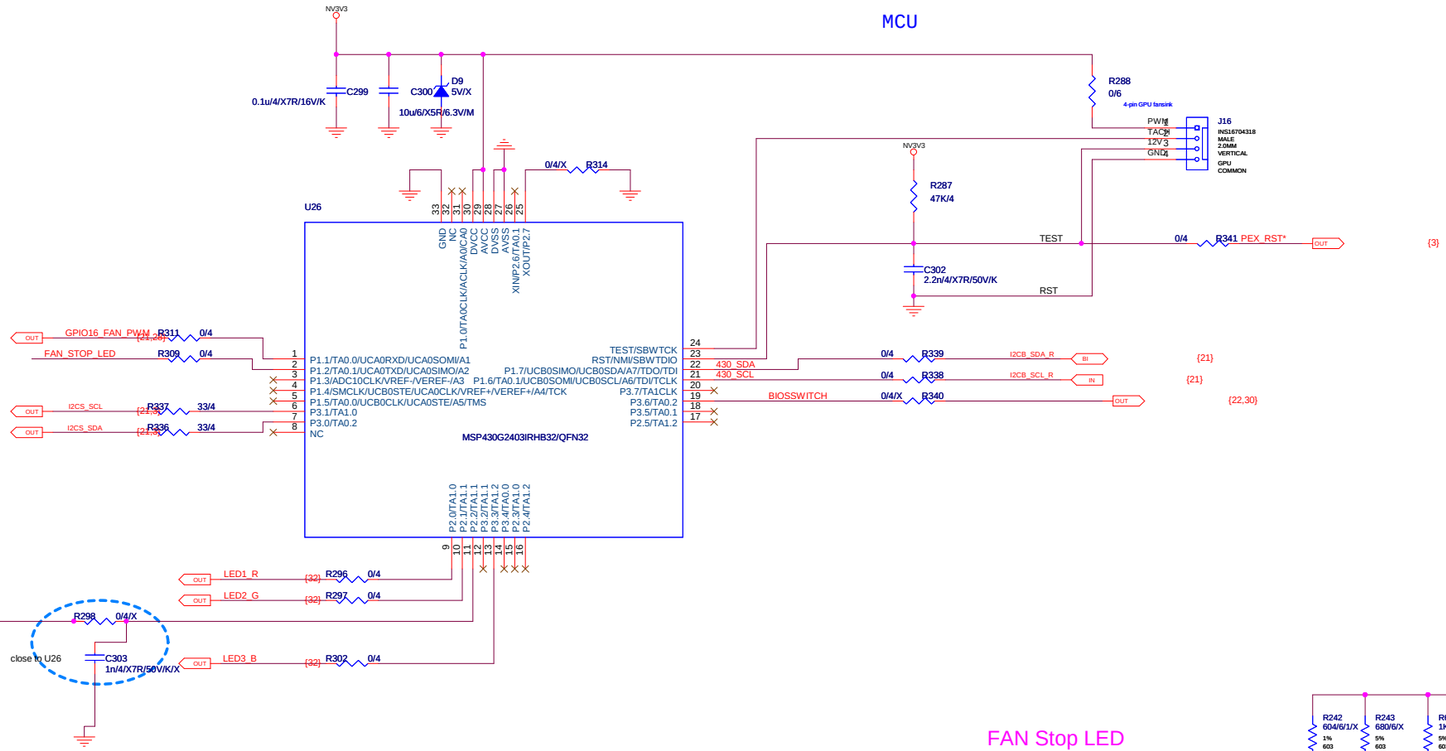
Title: DDR

Size: Custom | Document Number: GV-N950XTREME-2GD | Rev: 1.0

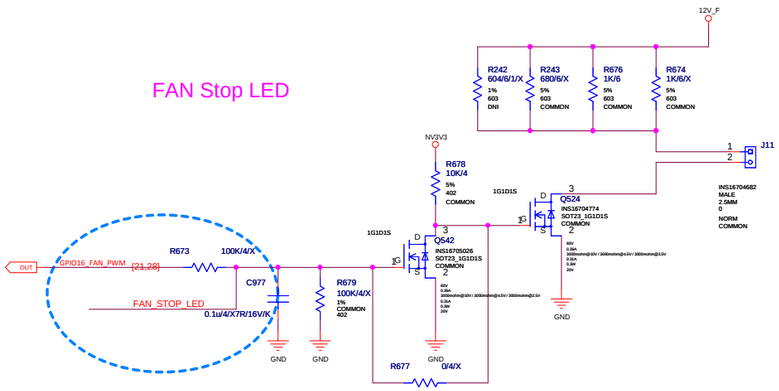
Date: Tuesday, August 04, 2015 | Sheet 27 of 34

Multi Colors LED Winforce Control by diho.su 20150702

MCU



FAN Stop LED



ASSEMBLY | BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL | [RESERVED]

GIGABYTE

Title: DDR

Size: Custom | Document Number: GV-N950XTREME-2GD | Rev: 1.0

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PS: NVVDD OVR2+1 POWER

DEL NVVDD COLAY PWM

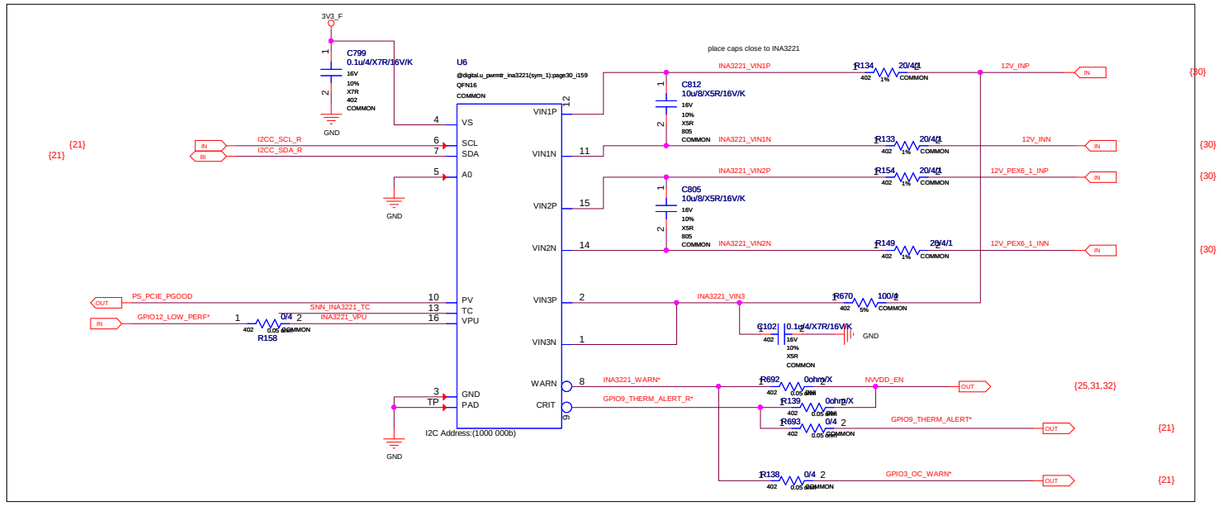
ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
PS: NVVDD OVR2+1 option

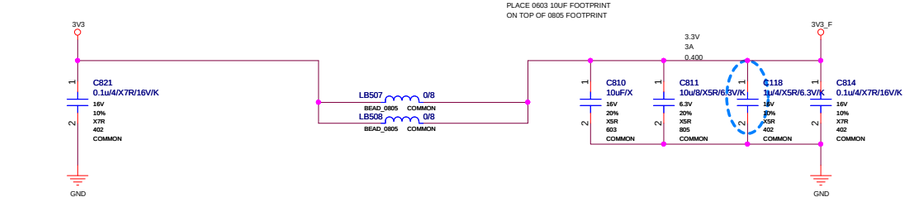
GIGABYTE

Title: DDR		
Size: Custom	Document Number: GV-N950XTREME-2GD	Rev: 1.0
Date: Tuesday, August 04, 2015	Sheet 29 of 34	

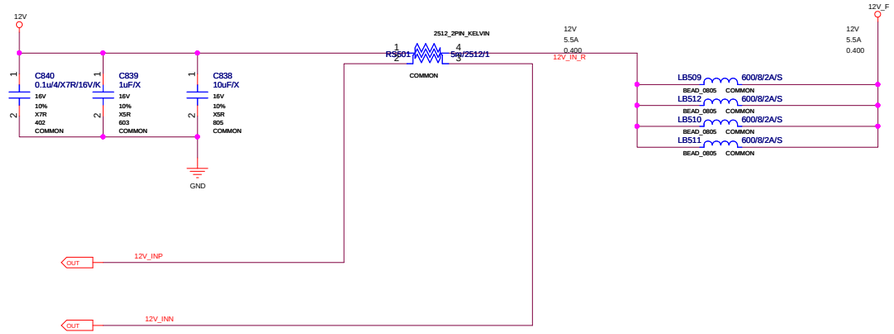
PS: Inputs, Filtering, and Monitoring



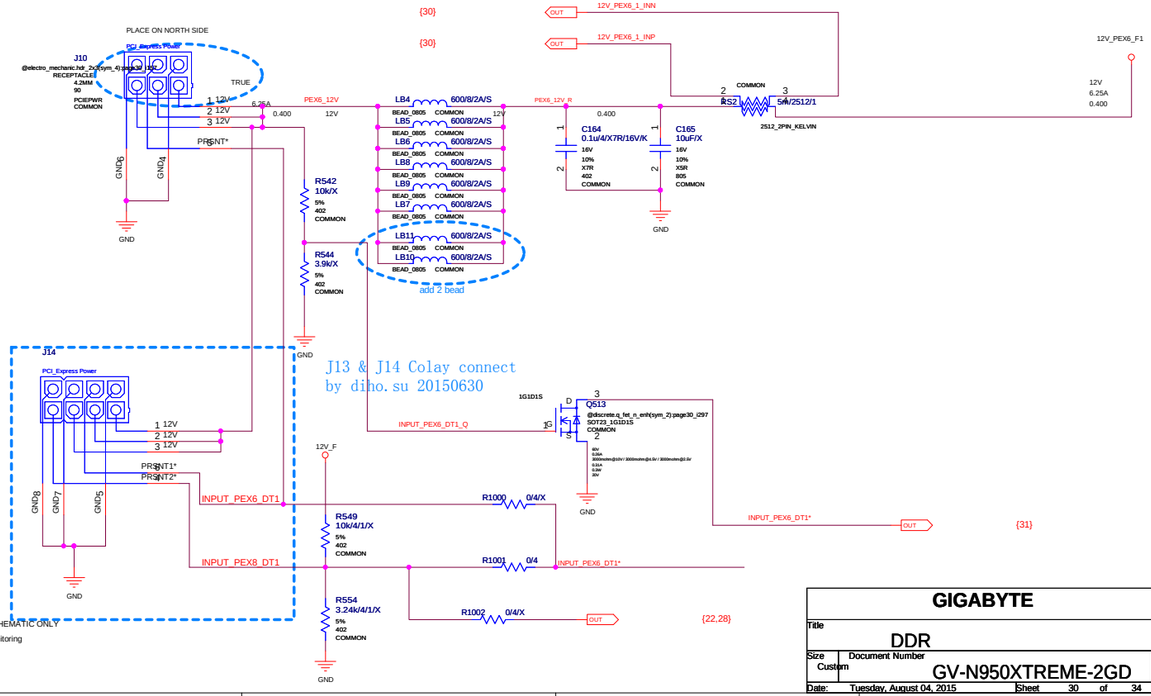
PEX 3V3 INPUT - 10W



PEX_12V INPUT - 66W



PEX6 INPUT - 2x3 PCIE CON 75W



ASSEMBLY | BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL | PS: Inputs, Filtering, and Monitoring

GIGABYTE

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PS: Sequence and Shutdown

POWER CONNECTOR HOT-UNPLUG DETECT

PEX Input Present

POWER OFF
ON HOTPLUG EVENT
STUFF TO LATCH

THERM OVERT SHUTDOWN LATCH

PEX Input - Power Level/PSI* Control

GPIO12_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

VID PLL

PEX VDD

ASSEMBLY
PAGE DETAIL

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PS: Sequence and Shutdown

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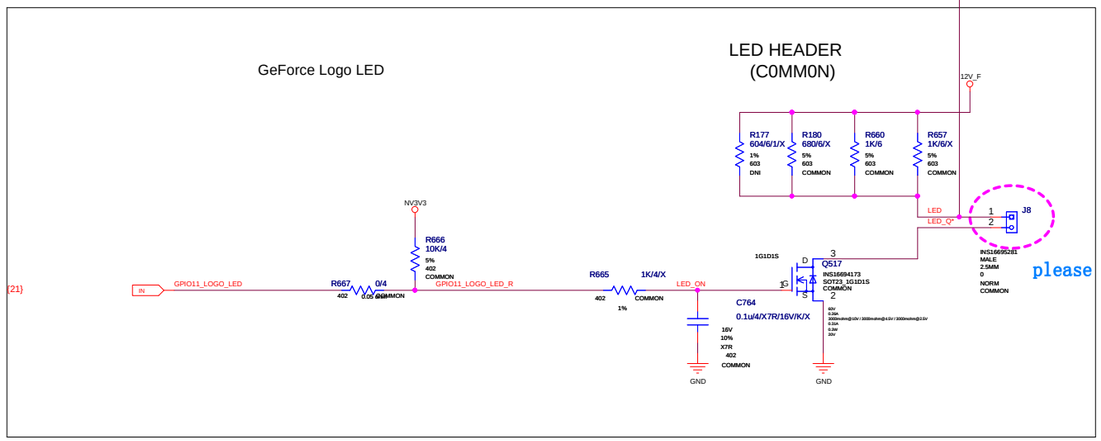
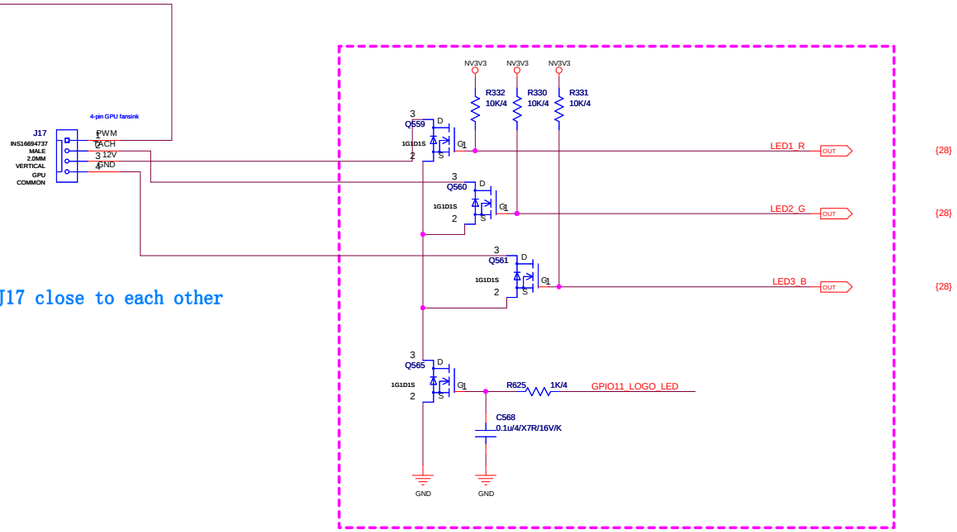
LEDs & 3 Pin FAN

GeForce Logo LED

LED HEADER
(C0MM0N)

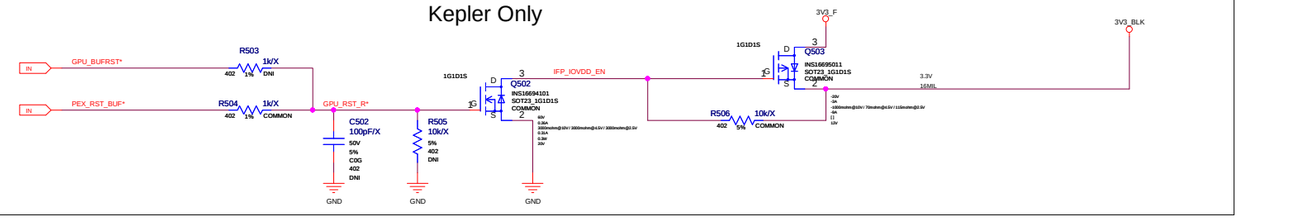


please place J8&J17 close to each other



IFP_IOVDD (backdrive prevention)

Kepler Only



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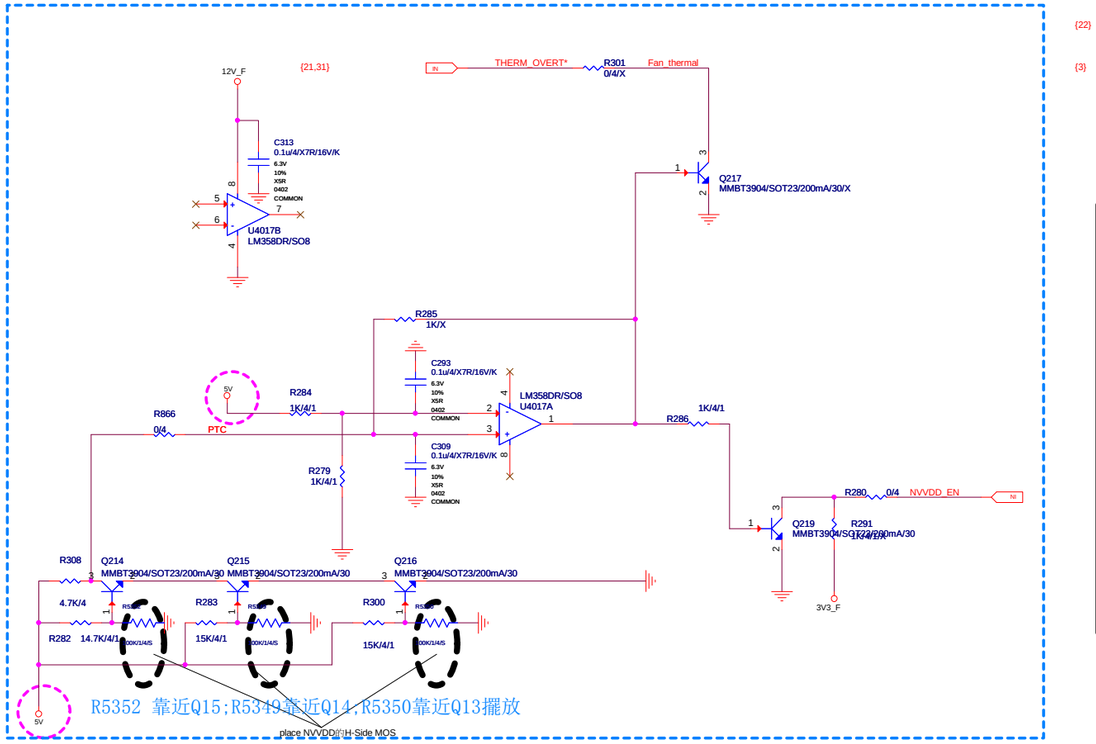
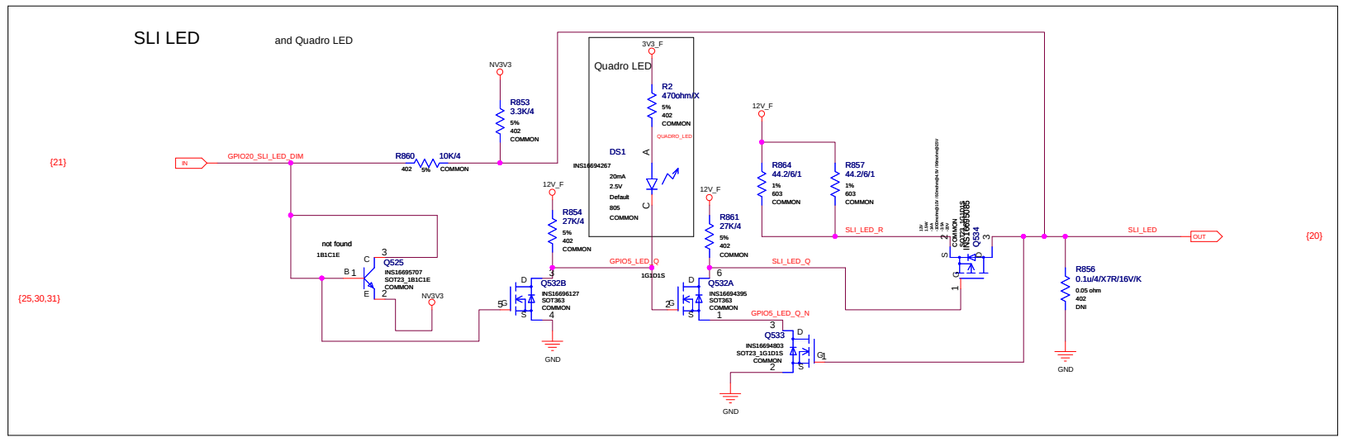
{3}



SLI LED and Quadro LED



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	LEDs

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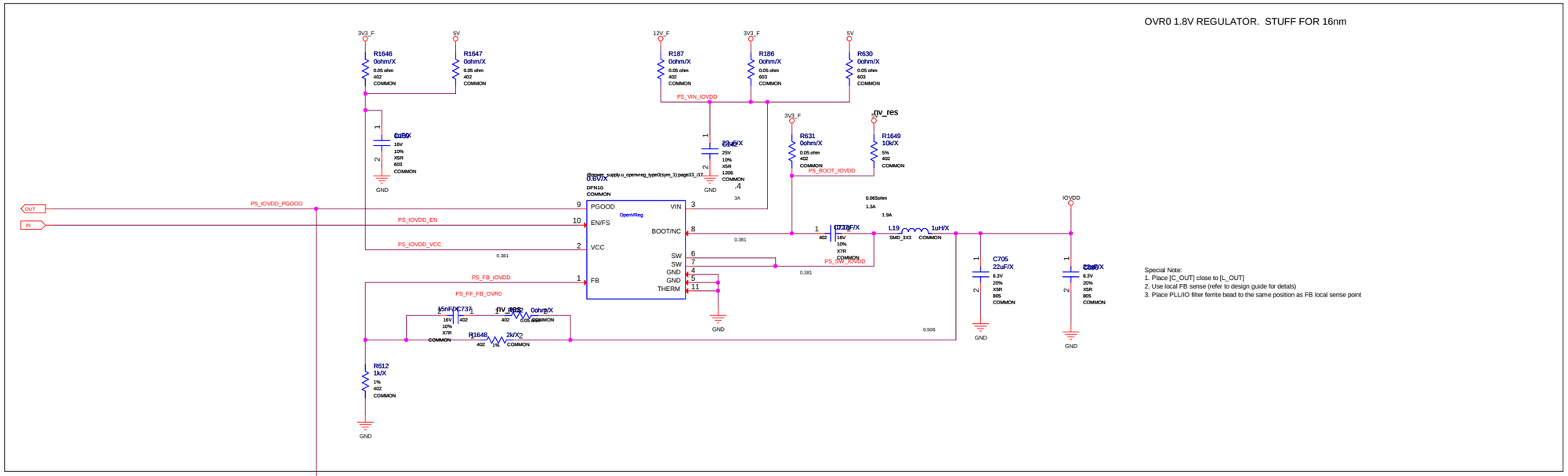
PS: IOVDD, NV3V3, NV12V



ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
PS: IOVDD Regulator

GIGABYTE

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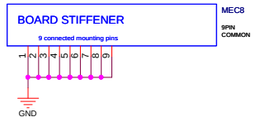
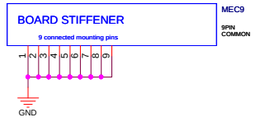
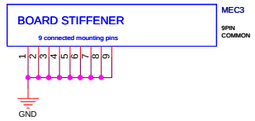
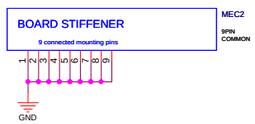
Mechanical: Bracket/Thermal Solution

GPU 螺絲孔

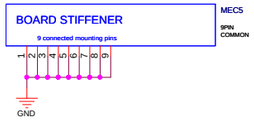


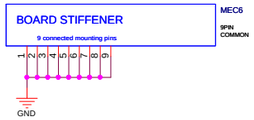


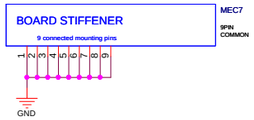


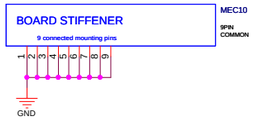


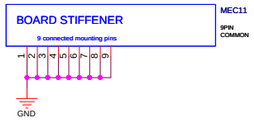
MOS 螺絲孔

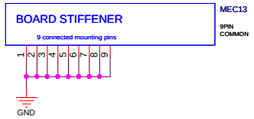




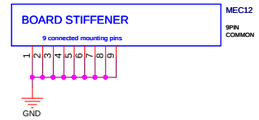








BK 螺絲孔



ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
MECH: Bracket/Thermal

GIGABYTE

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