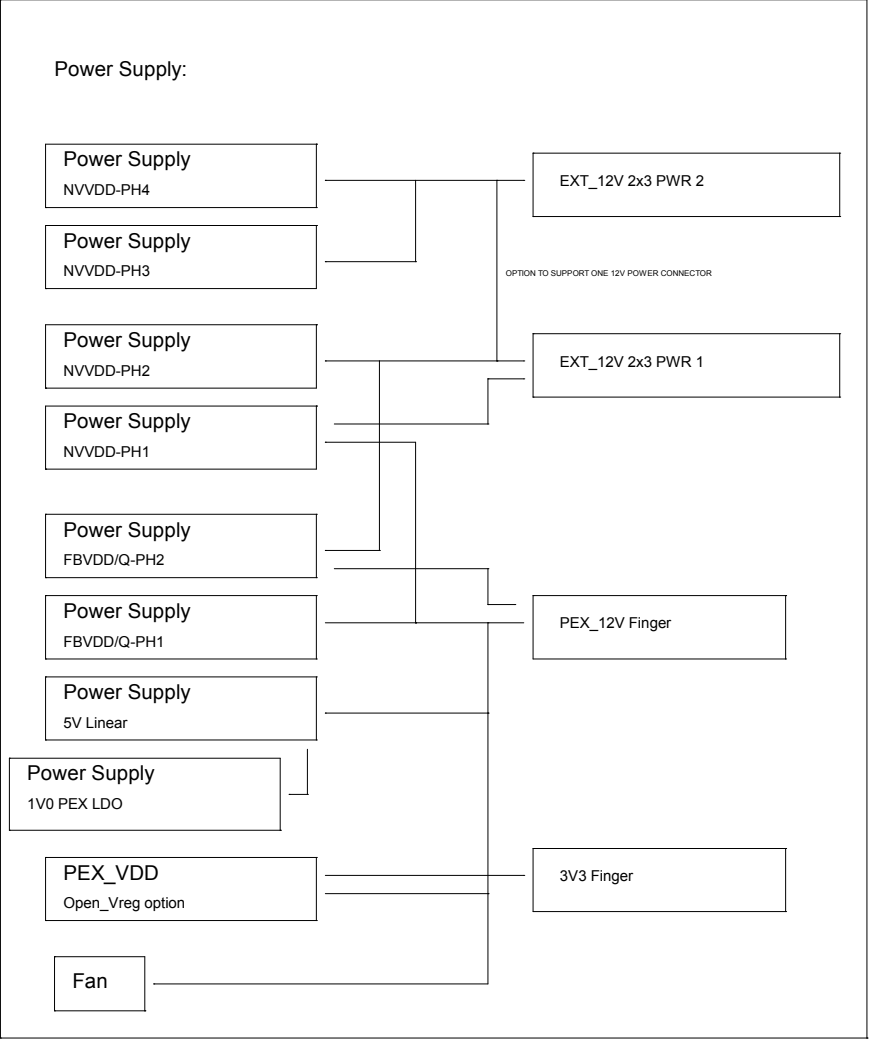
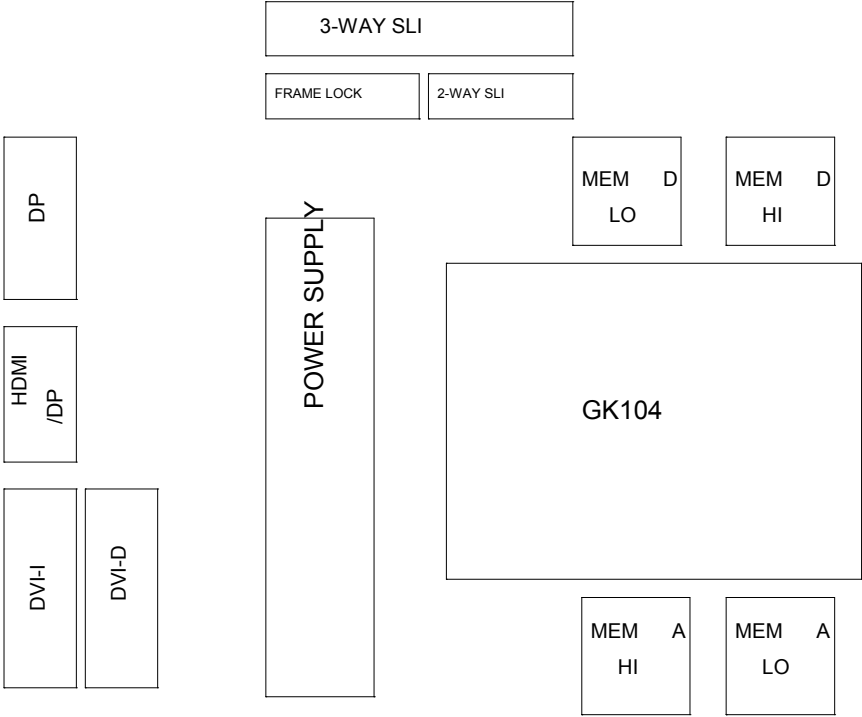
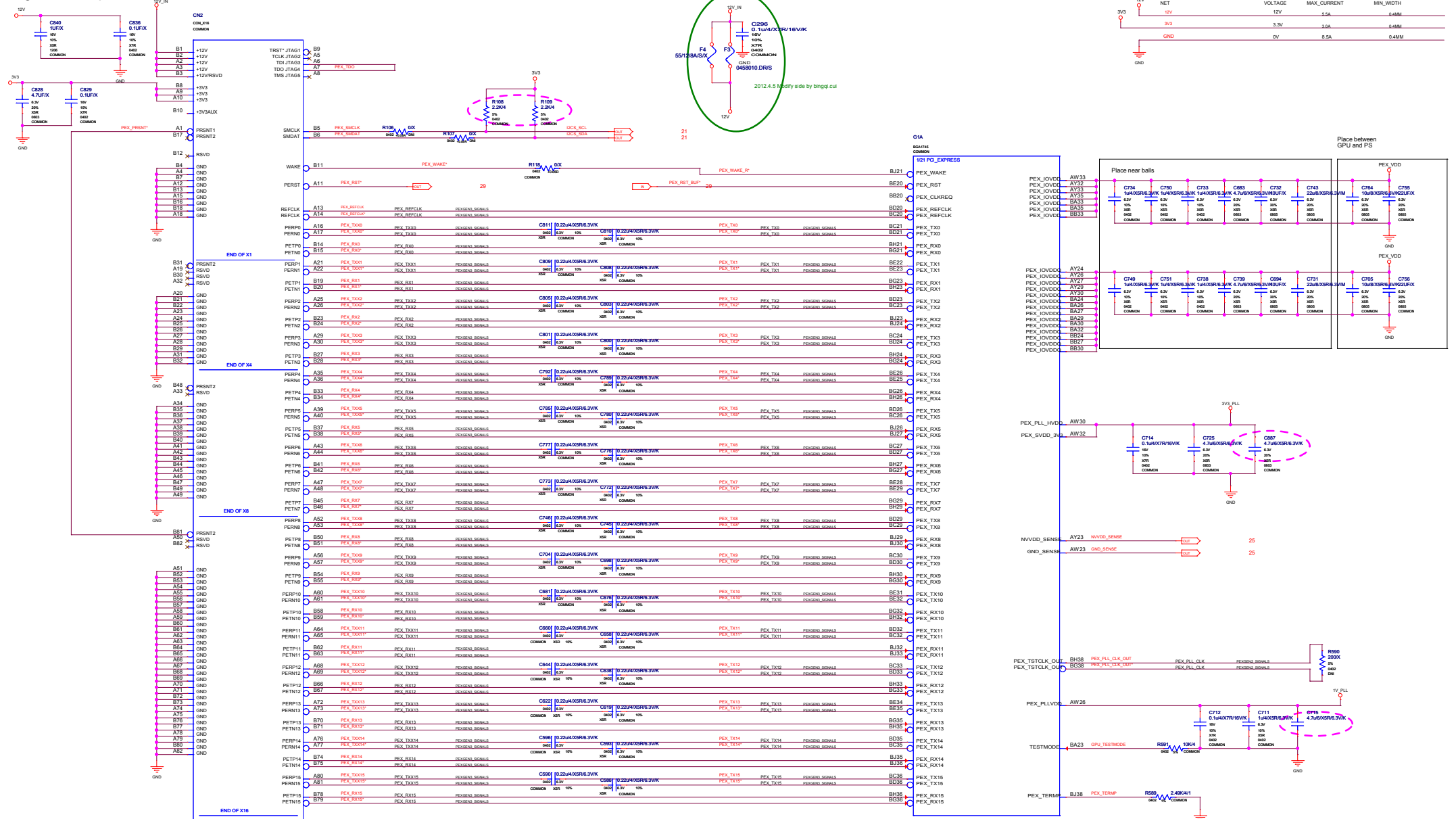
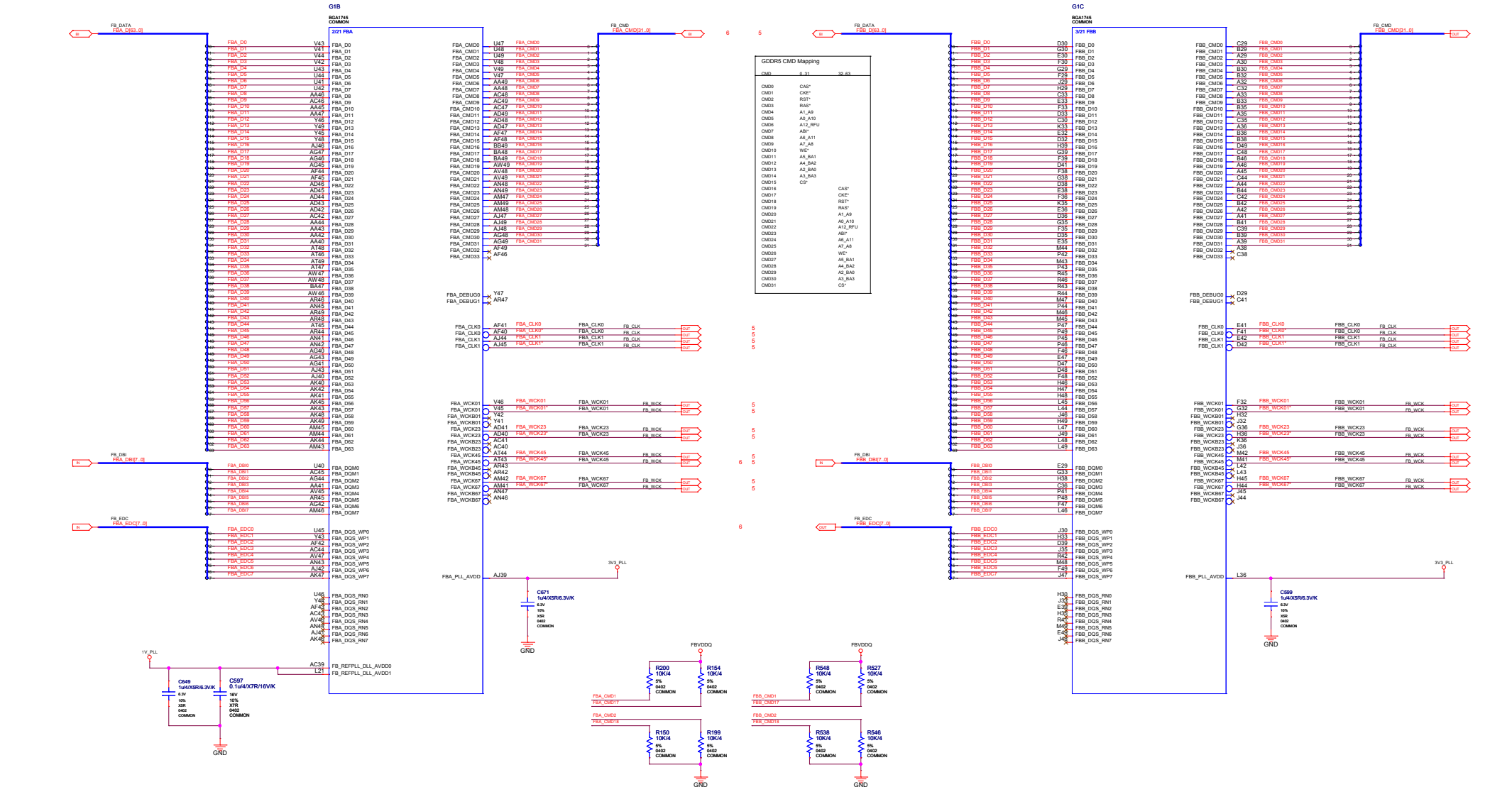








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Doc No.

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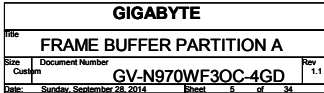
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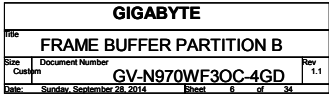
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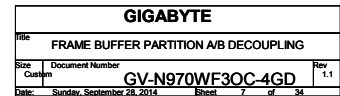
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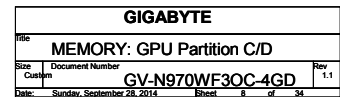
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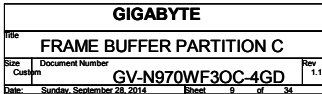
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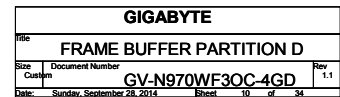


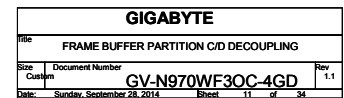


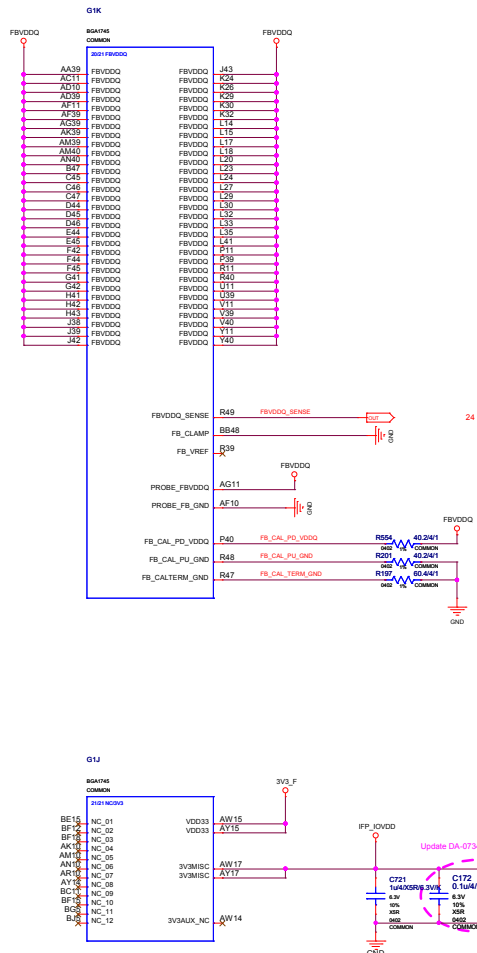




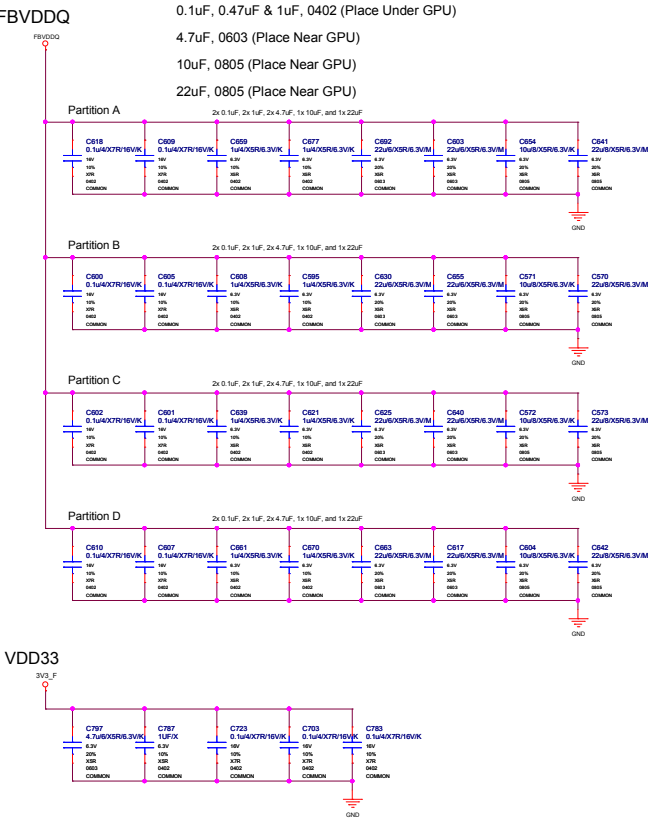






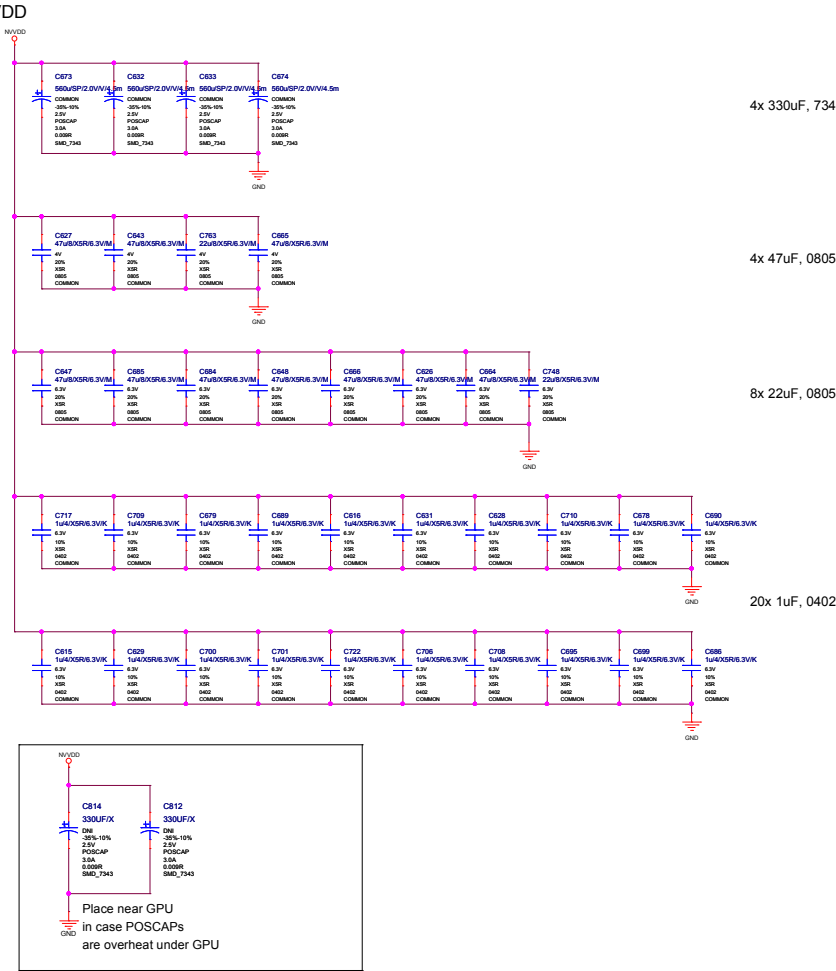


Based on GB2-X GDDR5 FBVDDQ Decap Guideline



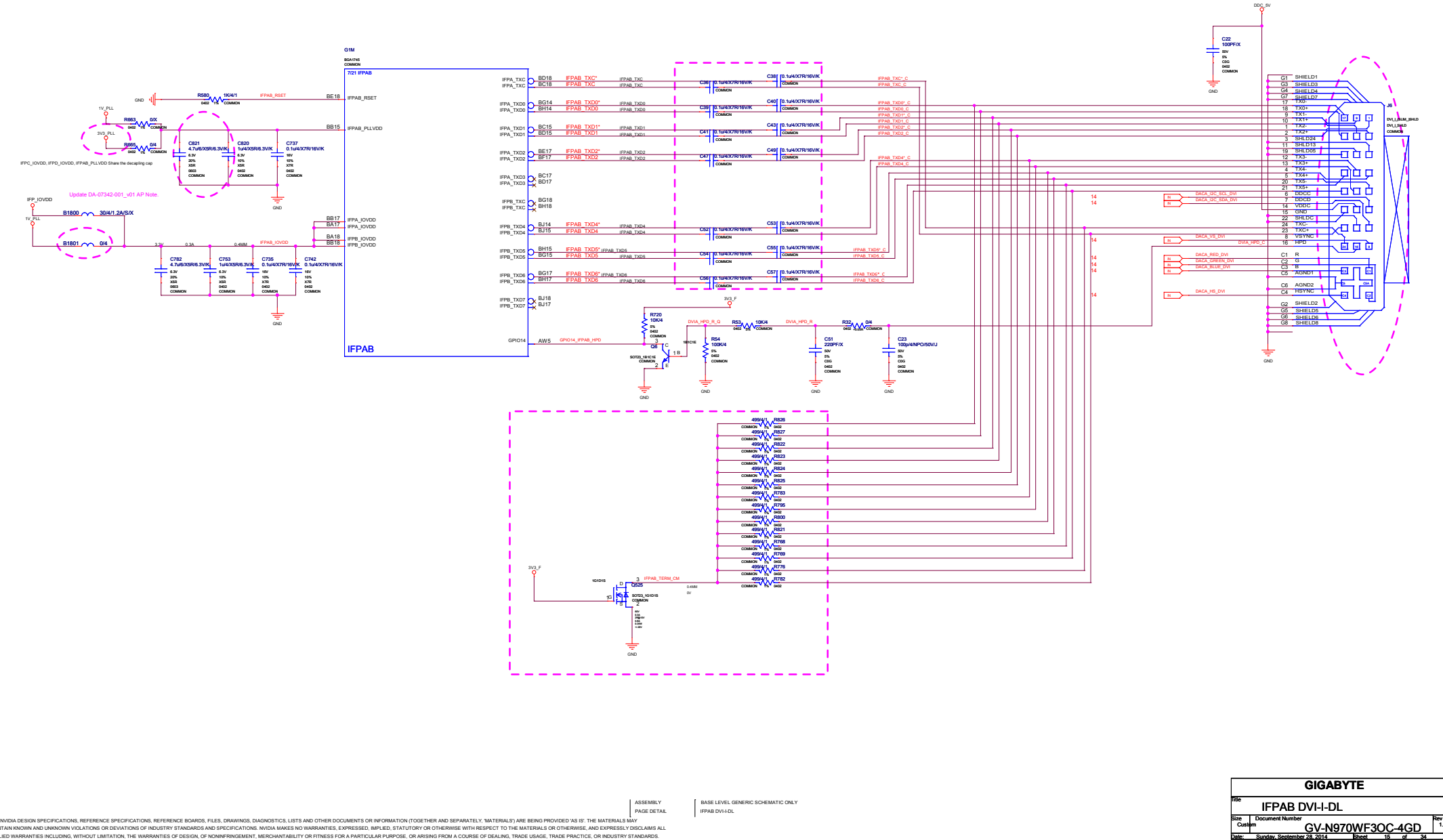
NVVD

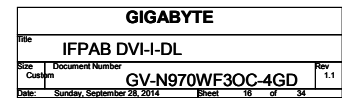
NVDD Decoupling caps. Place under GPU.

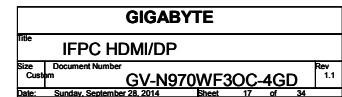




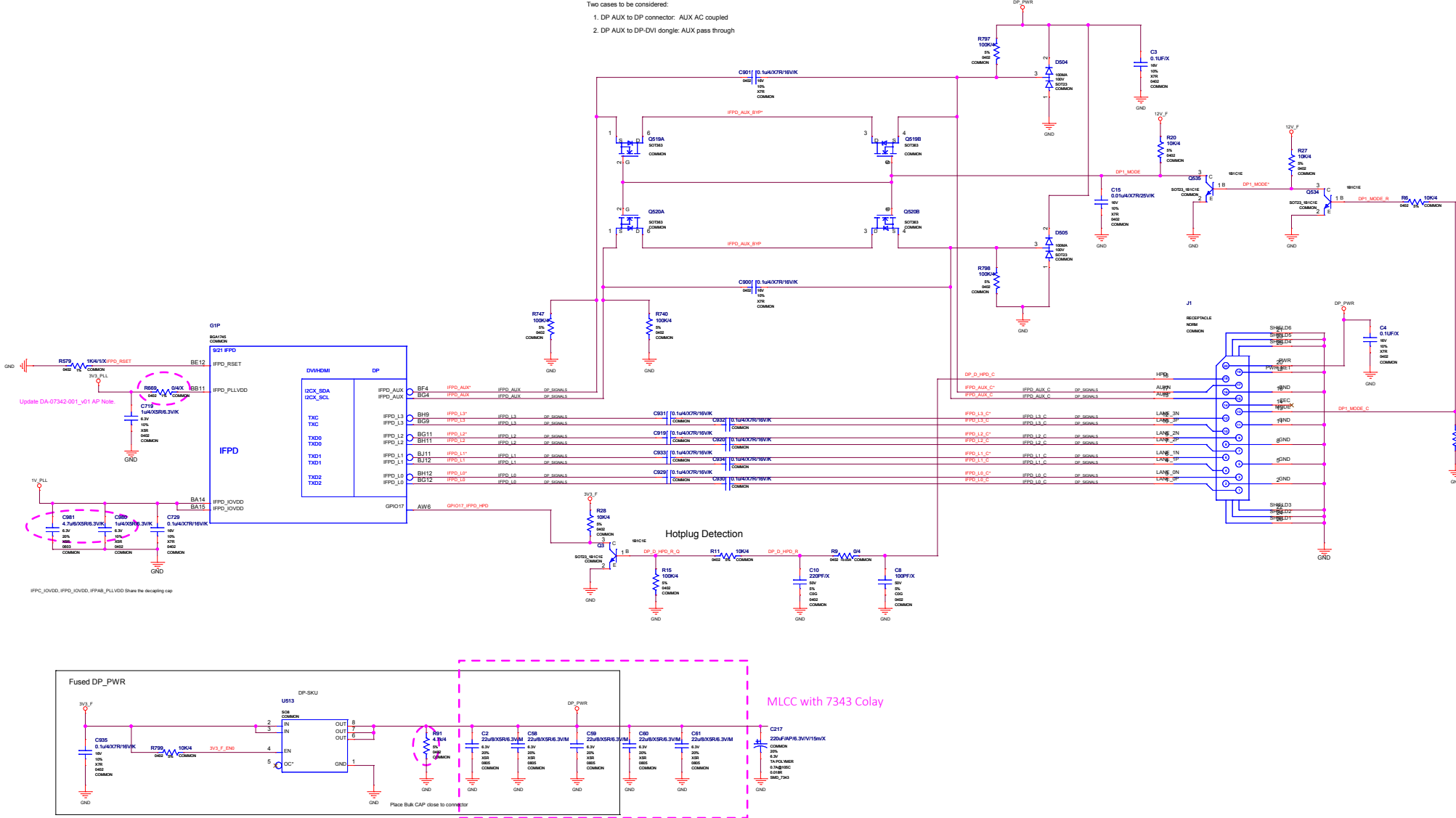
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DACA Interface			
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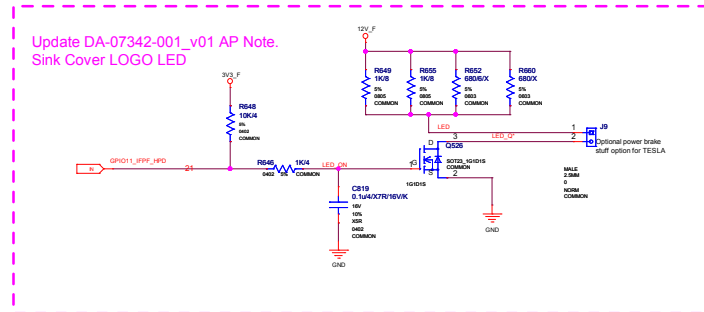


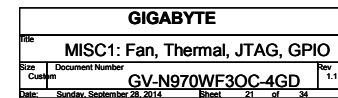


- Two cases to be considered:
- 1. DP AUX to DP connector: AUX AC coupled
 - 2. DP AUX to DP-DVI dongle: AUX pass through

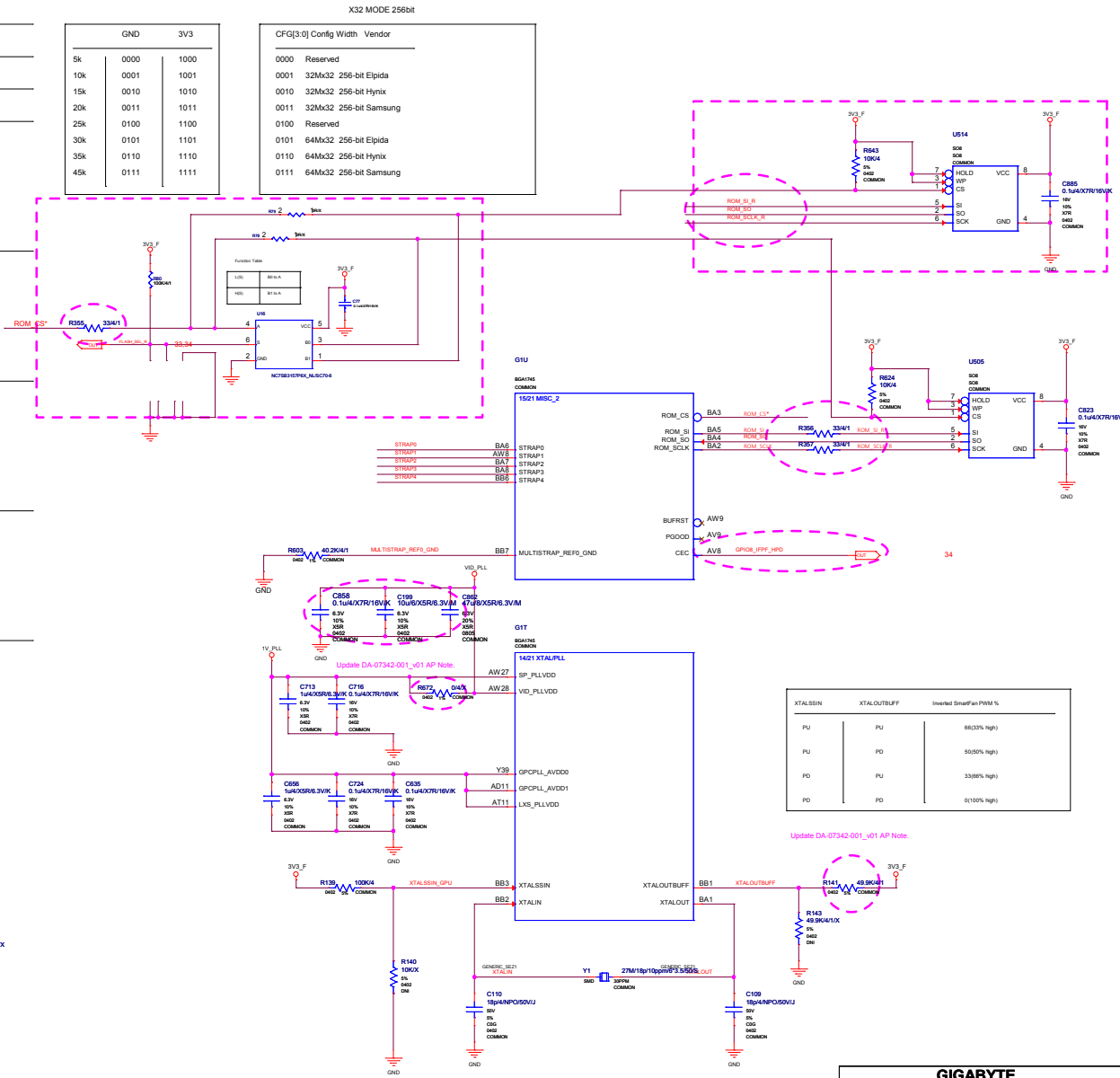


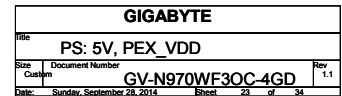
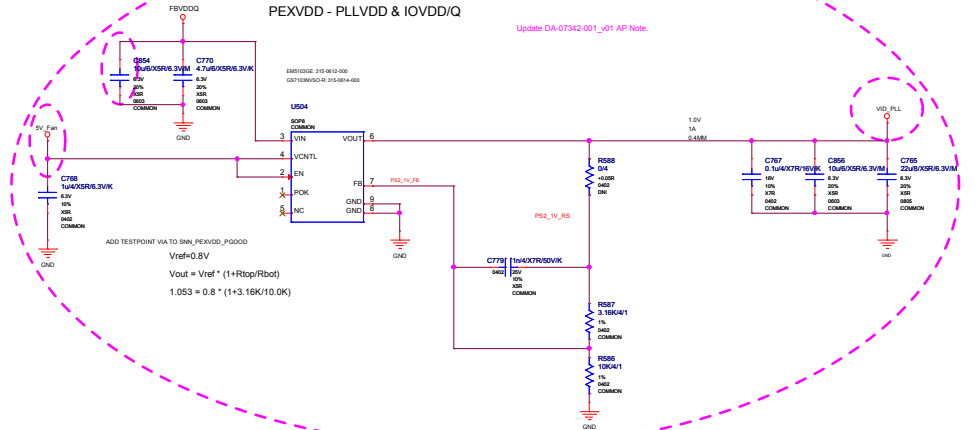


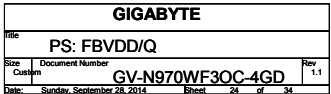


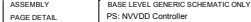
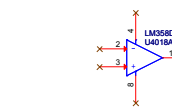


STRAP0	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	0111 - (0x1187)*	10K PU -325 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*
STRAP4	DP_PLL_VDD_33V*	1* FOR 3_3V*	
	PEX_MAX_SPEED*	1* FOR GEN2/3*	45K PD*
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	
	*		
ROM_Si	RAMCFG[0]*	0*	
	RAMCFG[1]*	1*	64Mx2 256 bit bytes for SGLT primary memory
	RAMCFG[2]*	1*	35K PD*
	RAMCFG[3]*	0*	
ROM_SO	VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	30k PD*
	FB[0]_APERTURE_SIZE*	1* For 128MB*	
	FB[1]_APERTURE_SIZE*	0* For 128MB*	
ROM_SCLK	PEX_PLL_EN_TERM100*	0* DISABLE*	
	PCI_DEVID_EXT[5]*	0* For 0x1189*	25K PD*
	SUB_VENDOR*	1* Dedicated BIOS*	
	PCI_DEVID_EXT[4]*	0* For 0x1189*	

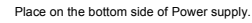






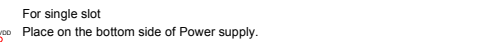
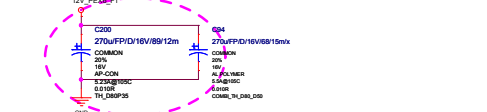


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PS: NVDD Phase 1 & 3			
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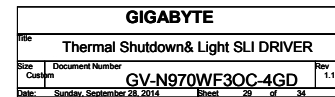
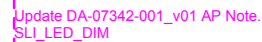
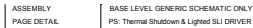
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PS: NVDD Phase 1 & 3			
Size	Document Number	Rev	
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[illegible]

The diagram shows a circuit with two inputs, SP21 and SP5, and one output, SHORT PADIX. A signal labeled CSP5 is connected to SP21. A signal labeled CSN6 is connected to SP5. A 25.27 MHz signal is shown entering from the right. The circuit is enclosed in a dashed purple box.

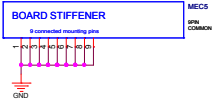


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Brackets:

MH-C236D118-8



GPU Stiffener:

For GPU

MOUNTING HOLES FOR HS:

