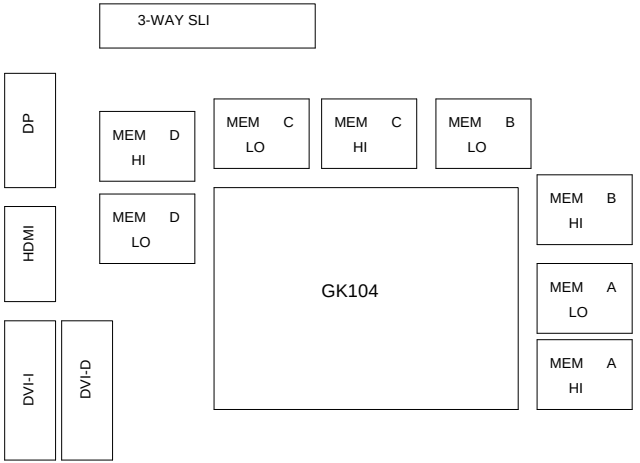
P2002

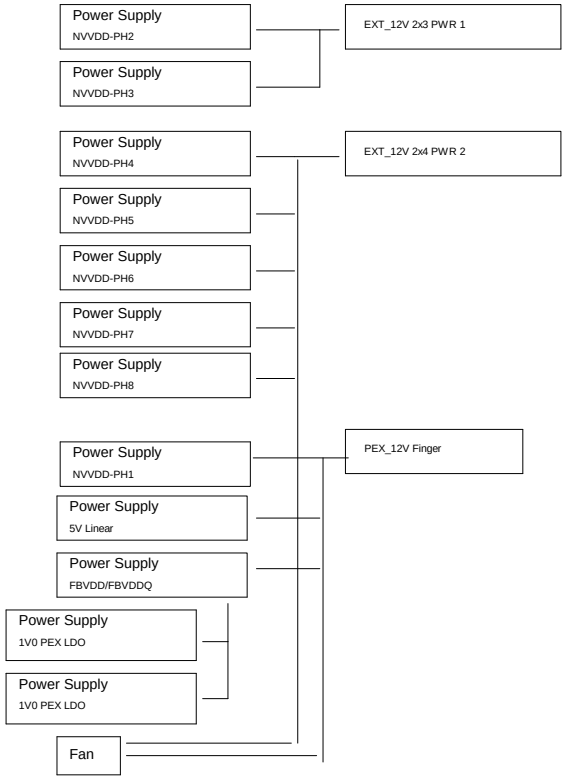
2GB GDDR5, 256b, 64Mx32

Stacked DVI-I/DVI-D + HDMI + DP

TABLE OF CONTENTS

GIGABYTE		
Title: Table of Contents		
Size: C	Document Number: GV-N980WF3OC-4GD	Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 1 of 37	

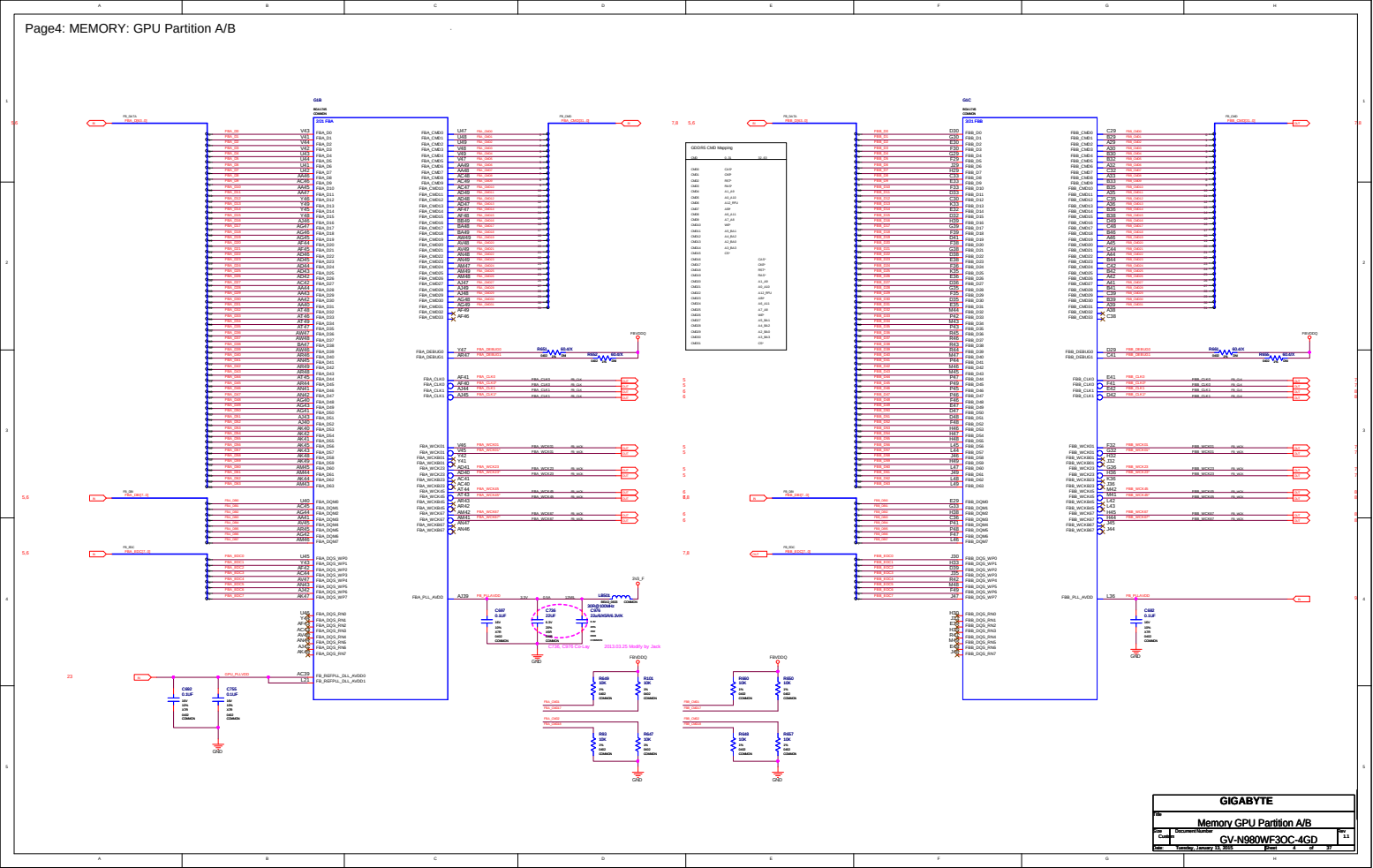




GIGABYTE		
File: Block of Diagram		
Size: C	Document Number: GV-N980WF3OC-4GD	Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 2 of 37	

Page3: PCI Express

Page4: MEMORY: GPU Partition A/B



GIGABYTE	
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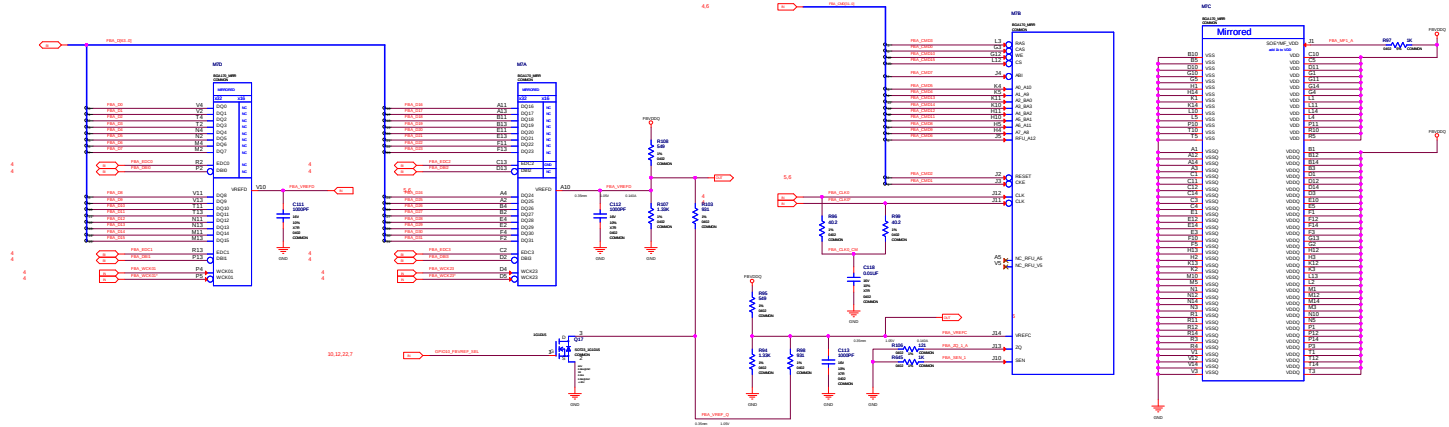
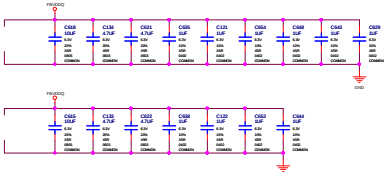
Size: Custom	Document Number: GV-N980WF3OC-4GD Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 4 of 37





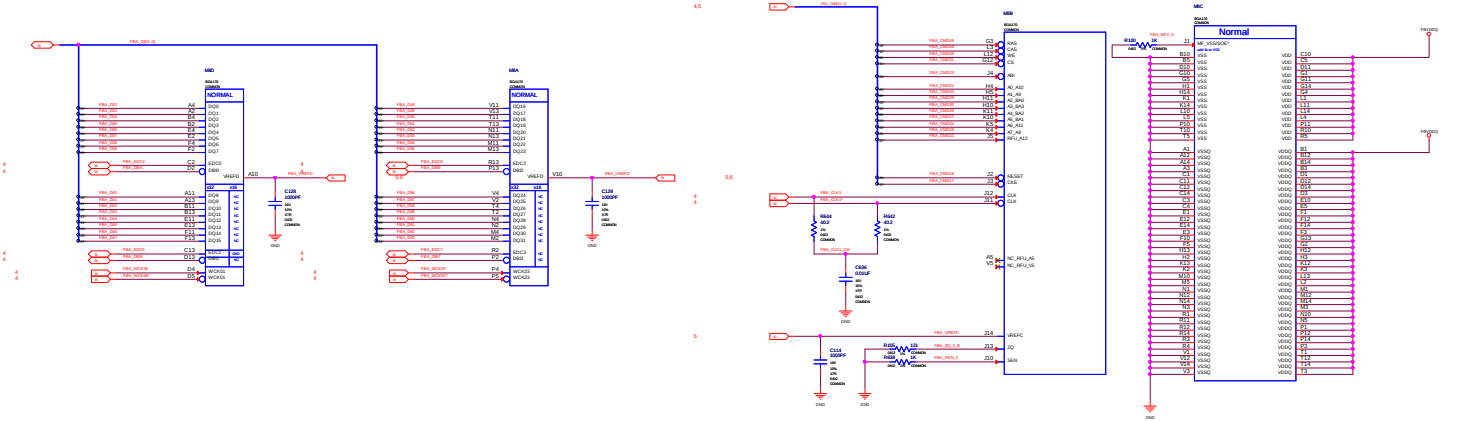
ASSEMBLY
PAGE DETAIL

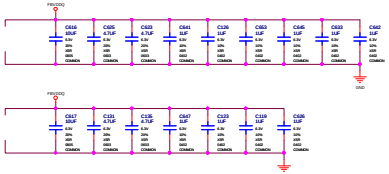
BASE LEVEL GENERIC SCHEMATIC ONLY
MEMORY: FBA[31:0]

GIGABYTE

File	Memory FBA{0..31}
Size: C	Document Number: GV-N980WF3OC-4GD
Custom	Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 5 of 37

Page6: MEMORY: FBA Partition 63..32





ASSEMBLY
PAGE DETAIL

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MEMORY FBA[63:32]

GIGABYTE		
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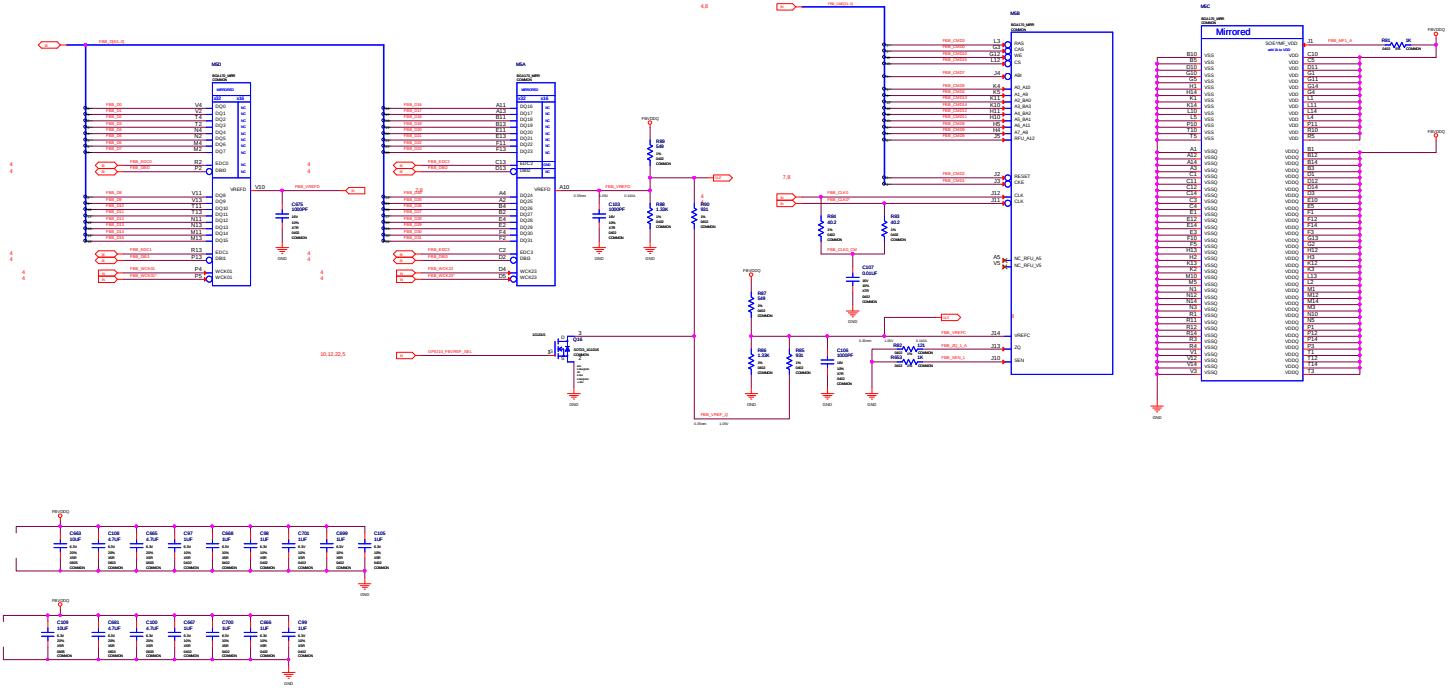
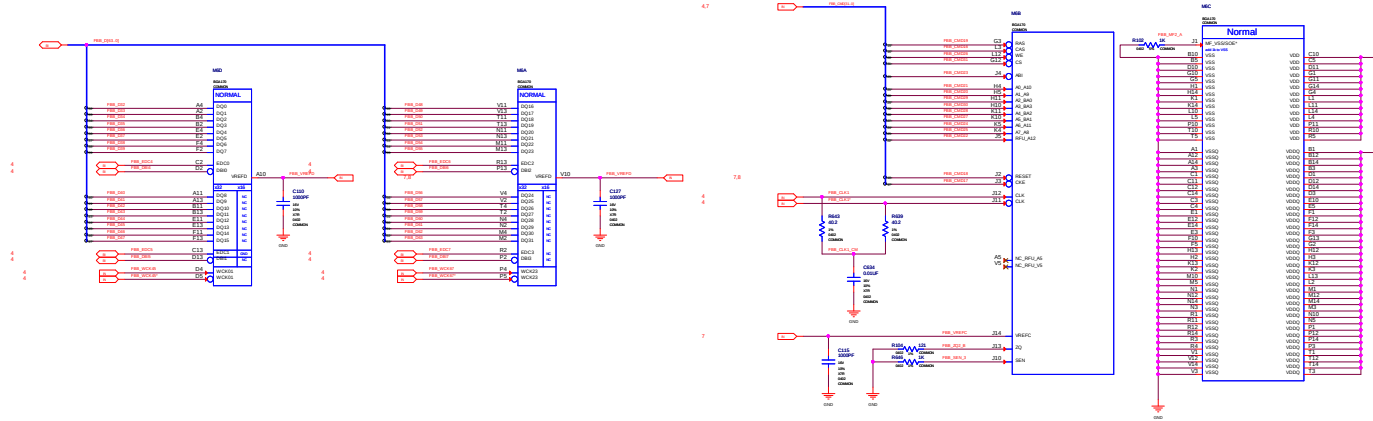
Size: C	Document Number: GV-N980WF3OC-4GD	Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 6 of 37	

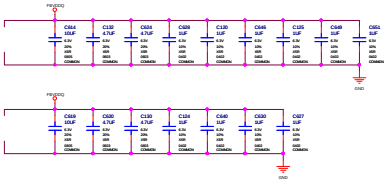


Title	Memory FBB{0..31}
Size	Document Number: GV-N980WF3OC-4GD
Custom	Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 7 of 37

GIGABYTE

Page8: MEMORY: FBB Partition 63..32



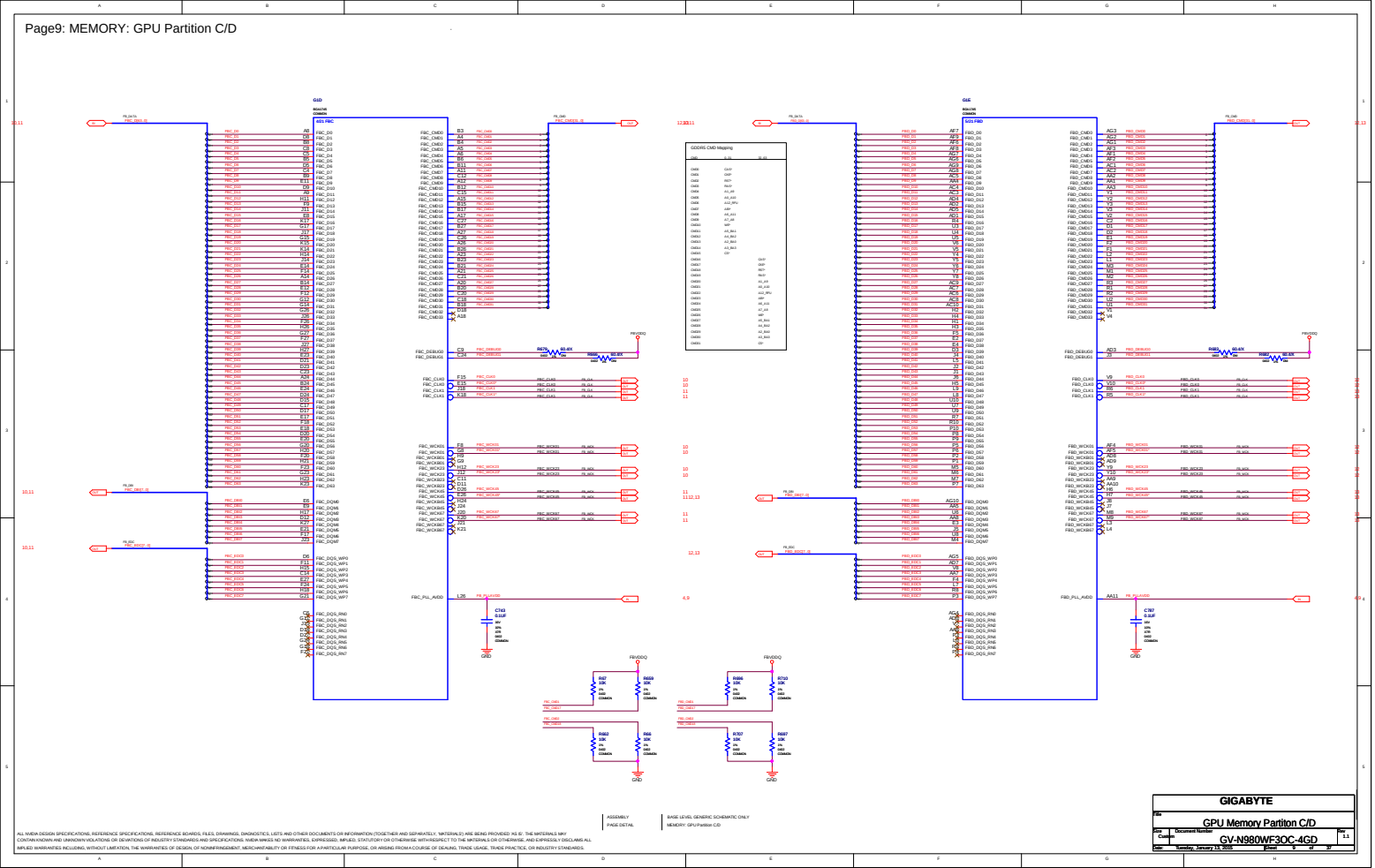


ASSEMBLY
PAGE DETAIL

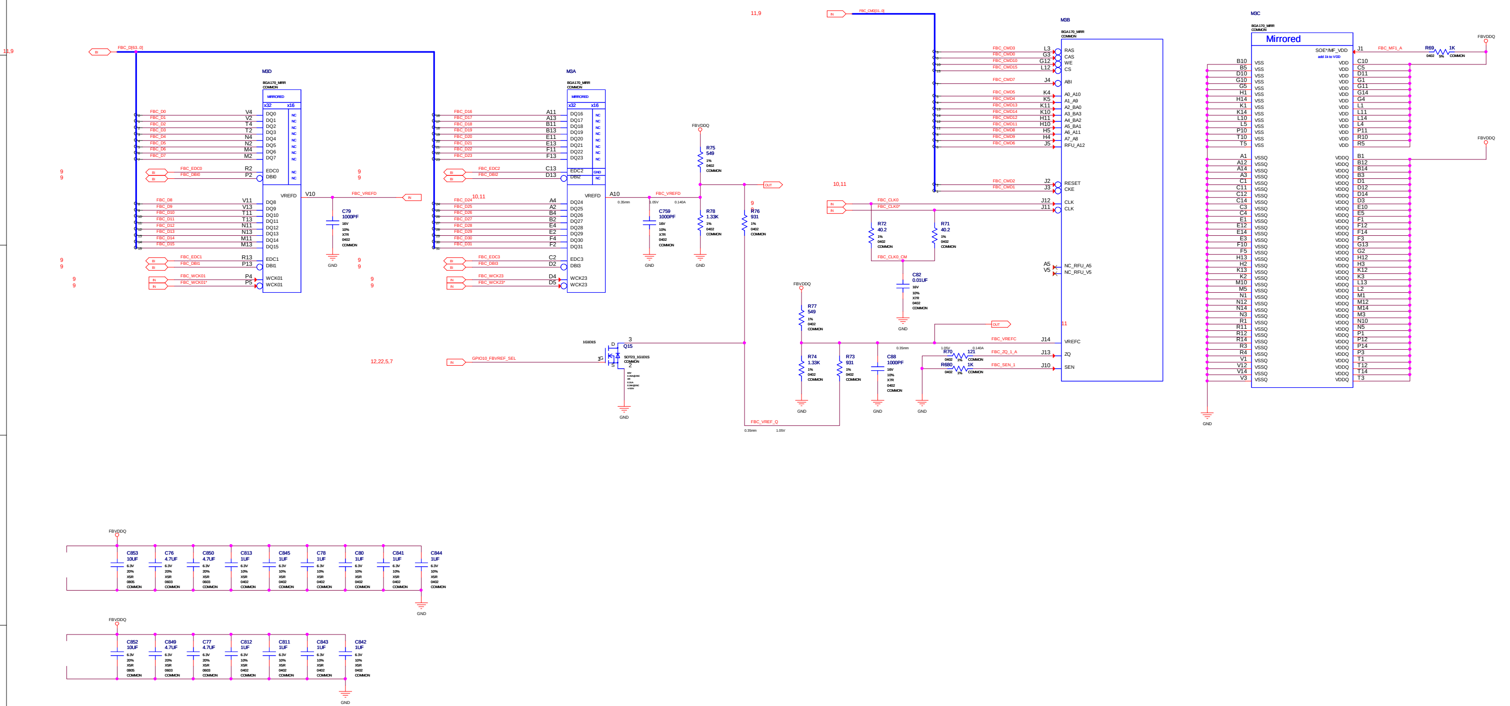
BASE LEVEL GENERIC SCHEMATIC ONLY
MEMORY: FBB[63:32]

	GIGABYTE
File	Memory FBB[32..63]
Size / Document Number	Rev: 1.1
Custom	GV-N980WF3OC-4GD
Date: Tuesday, January 13, 2015	Sheet 8 of 37

Page9: MEMORY: GPU Partition C/D



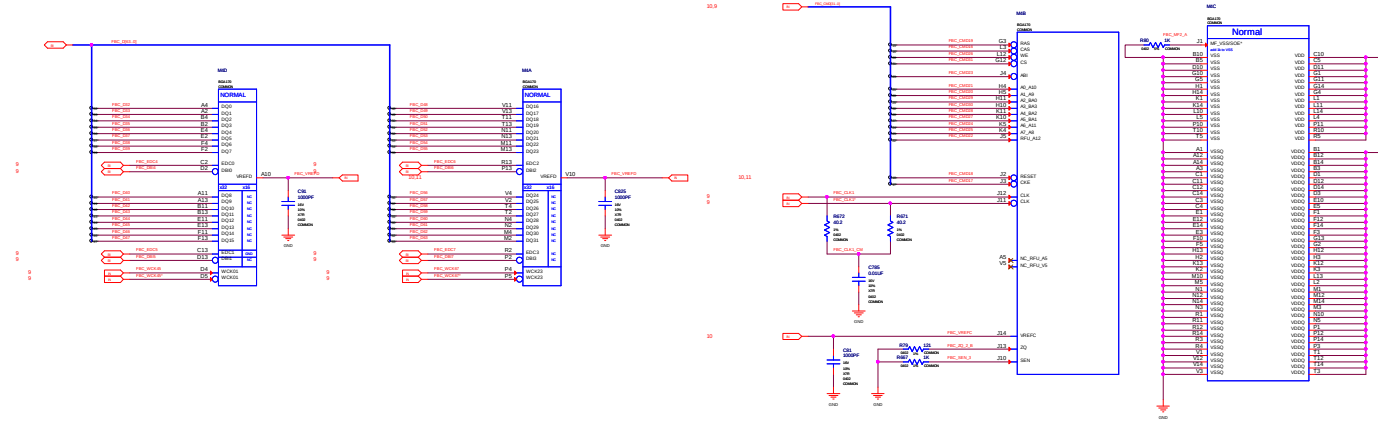
Page10: MEMORY: FBC Partition 31..0

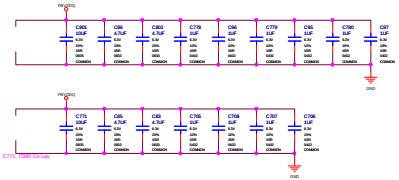


ASSEMBLY | BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL | MEMORY: FBC[31:0]

GIGABYTE

Title	Memory FBC{0..31}	
Size: Custom	Document Number: GV-N980WF3OC-4GD	Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 10 of 37	



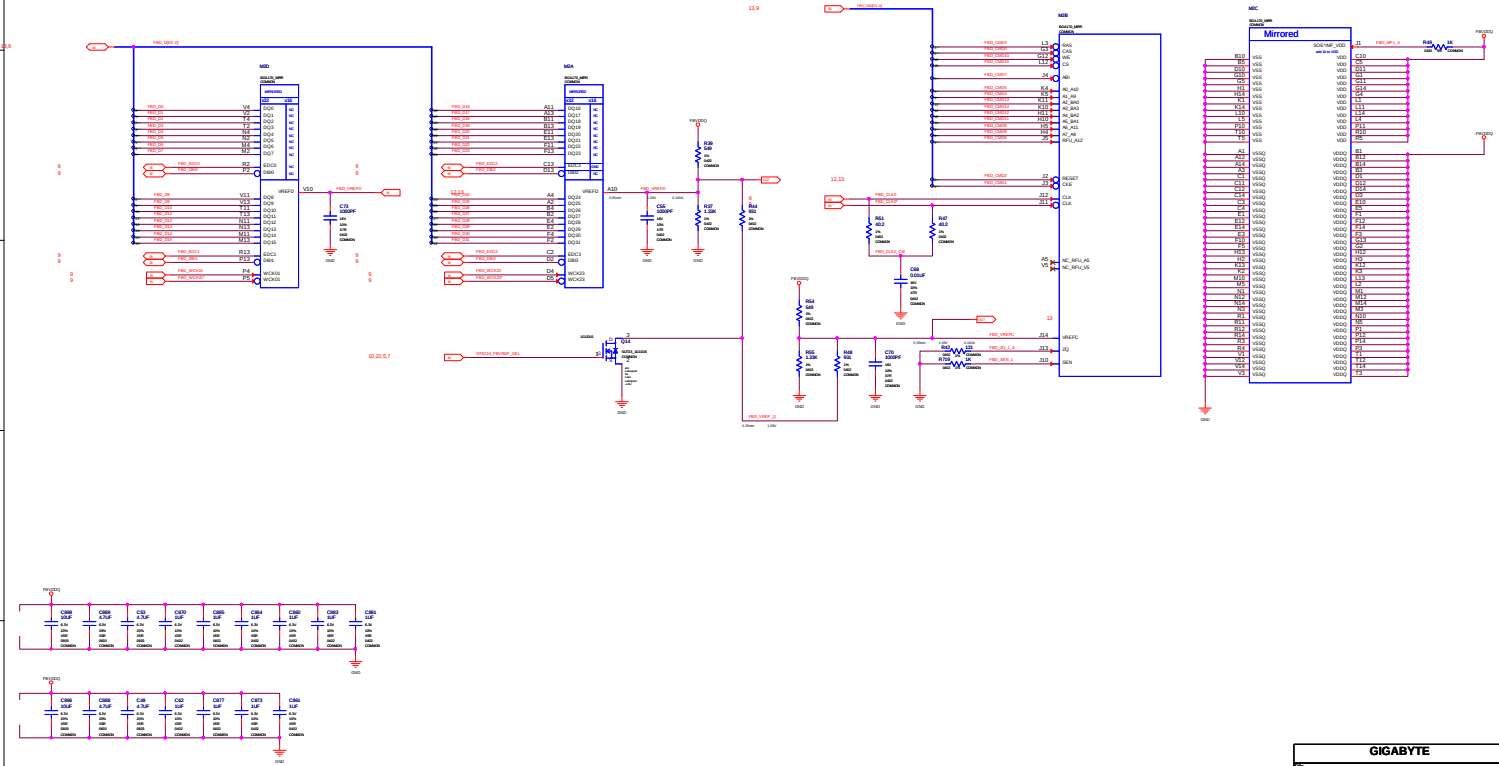


ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
MEMORY: FBC[63:32]

GIGABYTE

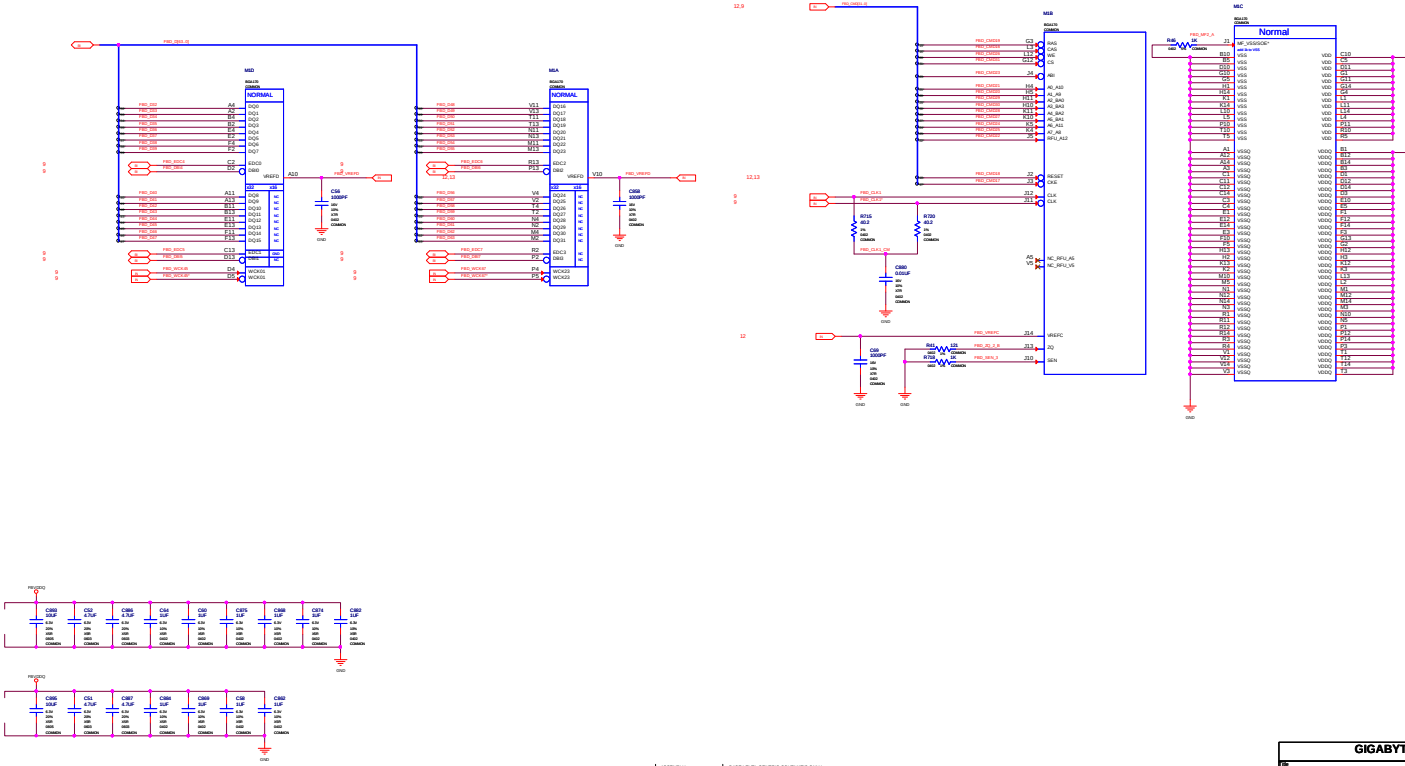
File	Memory FBC[32..63]	
Size: C	Document Number: GV-N980WF3OC-4GD	Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 31 of 37	



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBD[31:0]

GIGABYTE

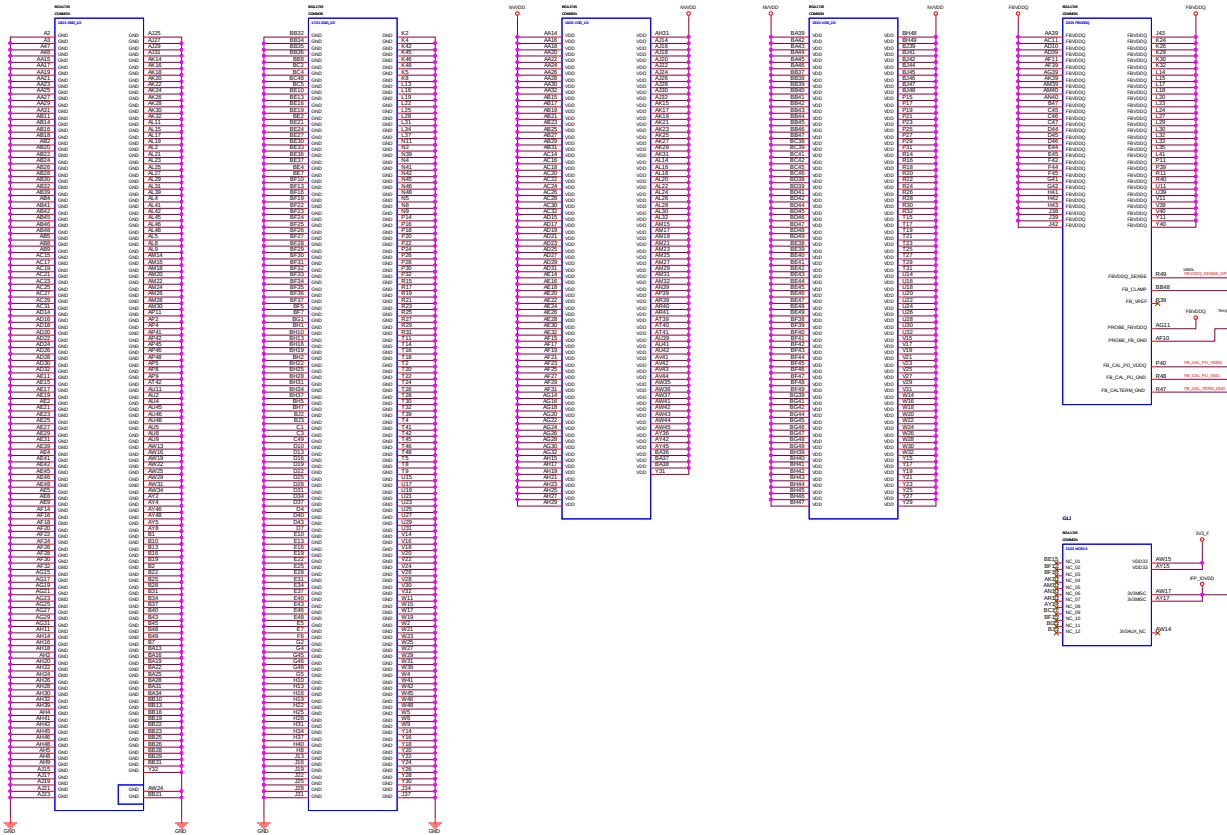
Title	Memory FBD[0..31]	
Size: C	Document Number: GV-N980WF3OC-4GD	Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 32 of 37	



ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY
PAGE DETAIL	MEMORY: FBD[63:32]

GIGABYTE	
File	Memory FBD[32..63]
Size: C	Document Number: GV-N980WF3OC-4GD
Rev: 1.1	
Date: Tuesday, January 13, 2015	Sheet 13 of 37

Page14: GPU PWR and GND



ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
GPU PWR and GND

Title	GPU PWR & GND
Size	Document Number
Custom	GV-N980WF3OC-4GD
Date:	Tuesday, January 13, 2015
Sheet	14 of 37

Based on GB2-X GDDR5 FBVDDQ Decap Guideline

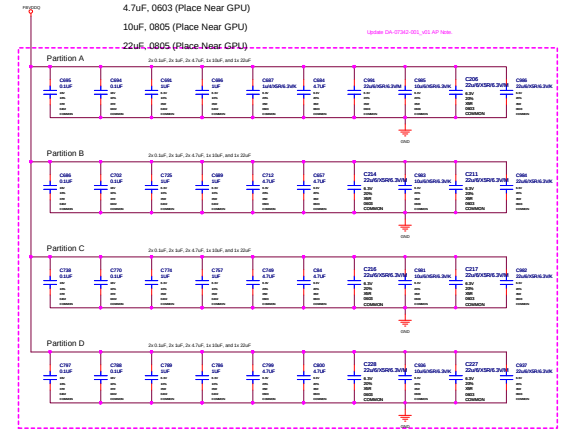
FBVDDQ

0.1uF, 0.47uF & 1uF, 0402 (Place Under GPU)

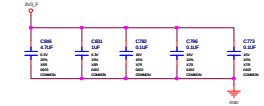
4.7uF, 0603 (Place Near GPU)

10uF, 0805 (Place Near GPU)

22uF, 0805 (Place Near GPU)

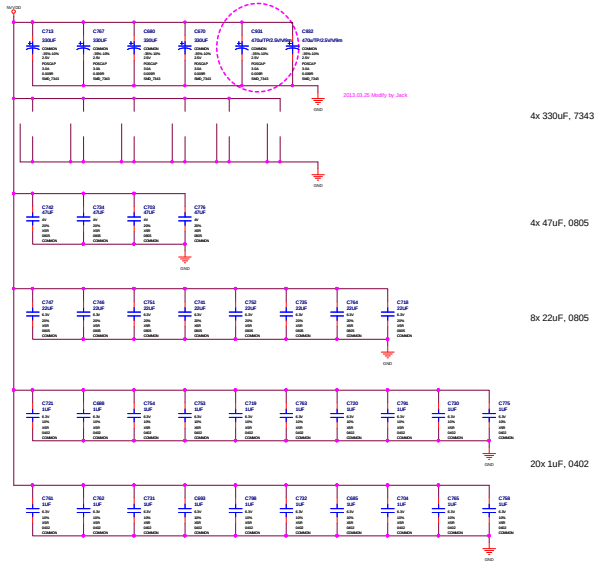


VDD33



NVVDD Decoupling caps. Place under GPU.

NVVDD

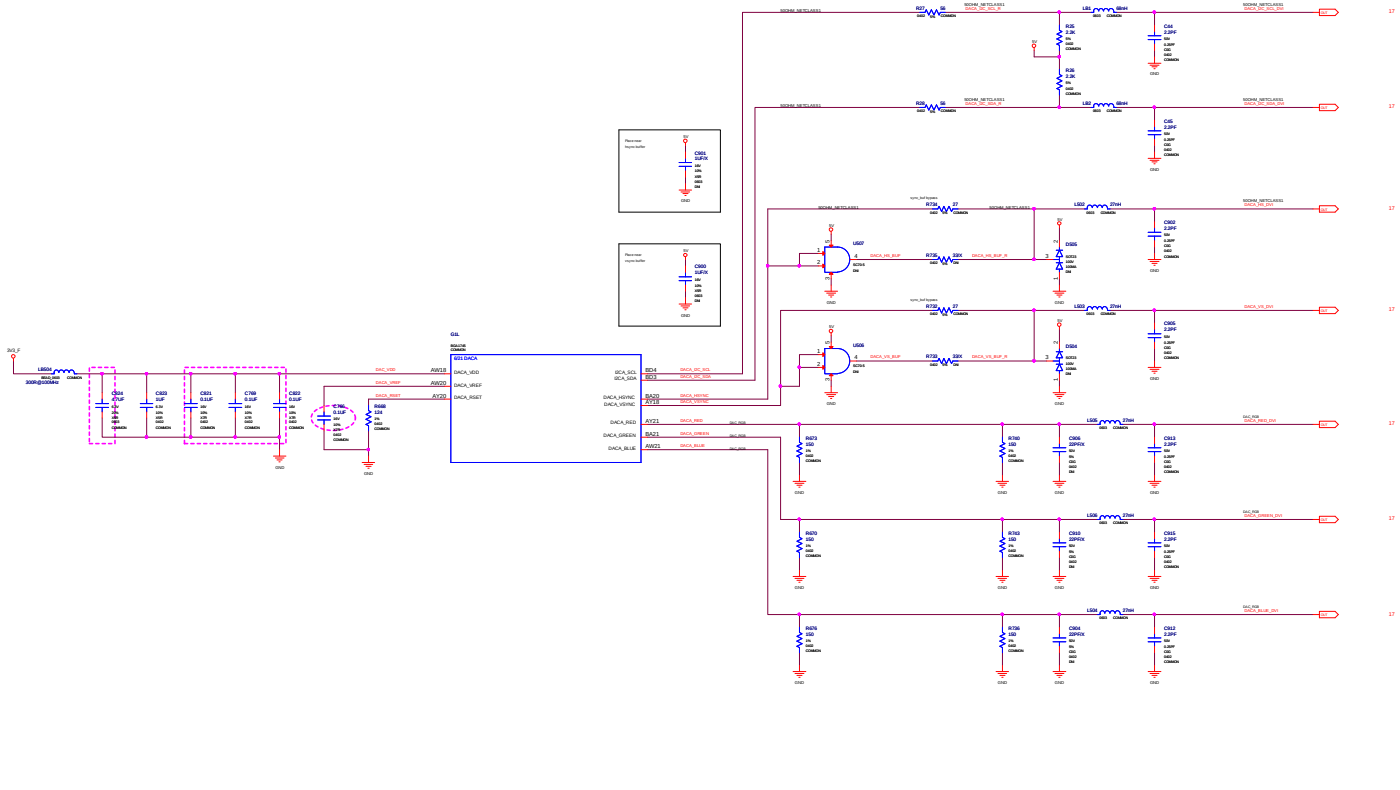


ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
GPU Decoupling

GIGABYTE		
Title: GPU Decoupling		
Size: C	Document Number: GV-N980WF3OC-4GD	Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 35 of 37	

Page16: DACA Interface



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
DAC_VDD	3.3V	0.25A	18MIL

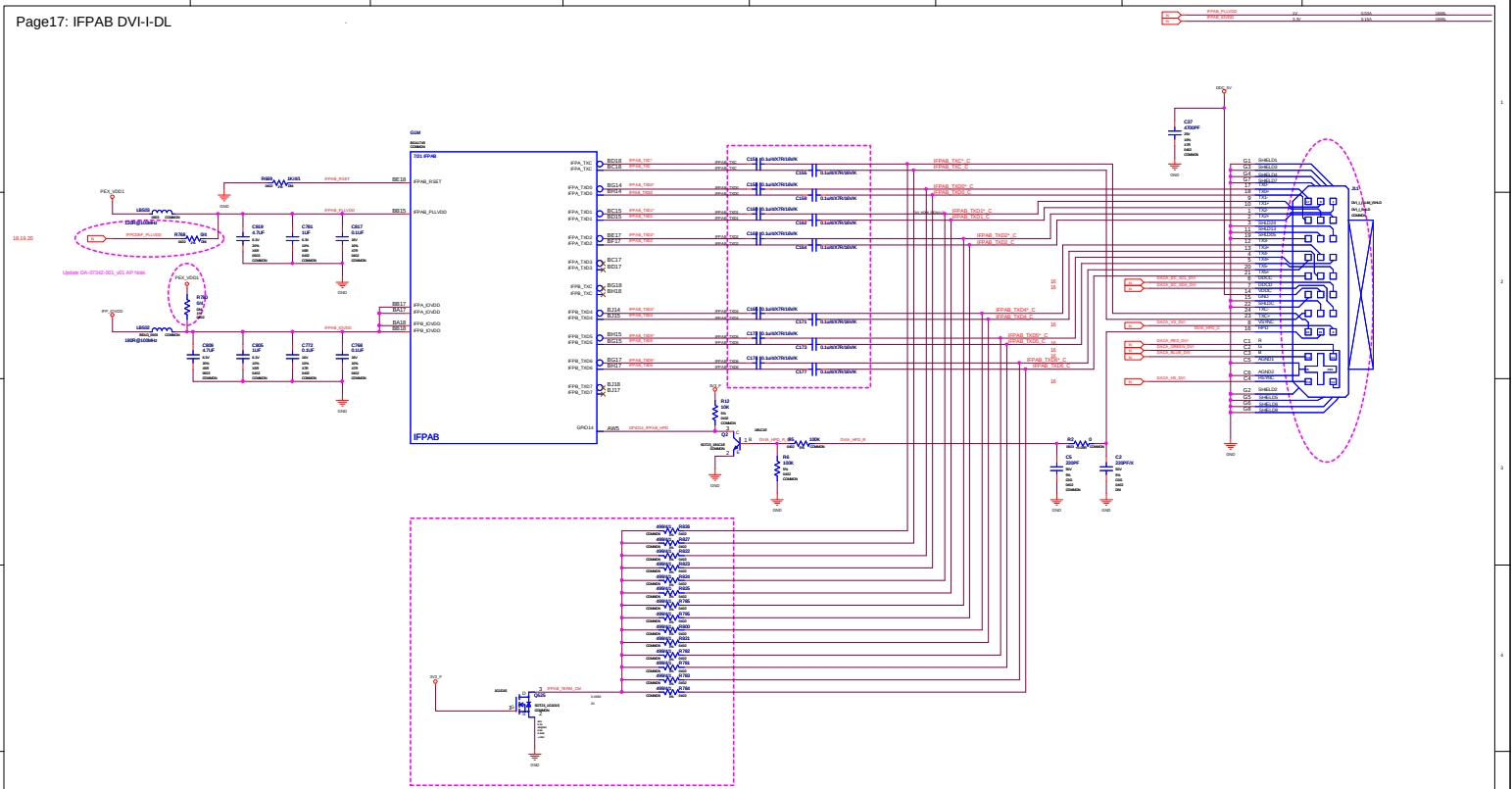
ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
DACA Interface

Title	DACA Interface
Size	Document Number
Custom	GV-N980WF3OC-4GD
Date	Tuesday, January 13, 2015
Sheet	16 of 37
Rev	1.1

GIGABYTE

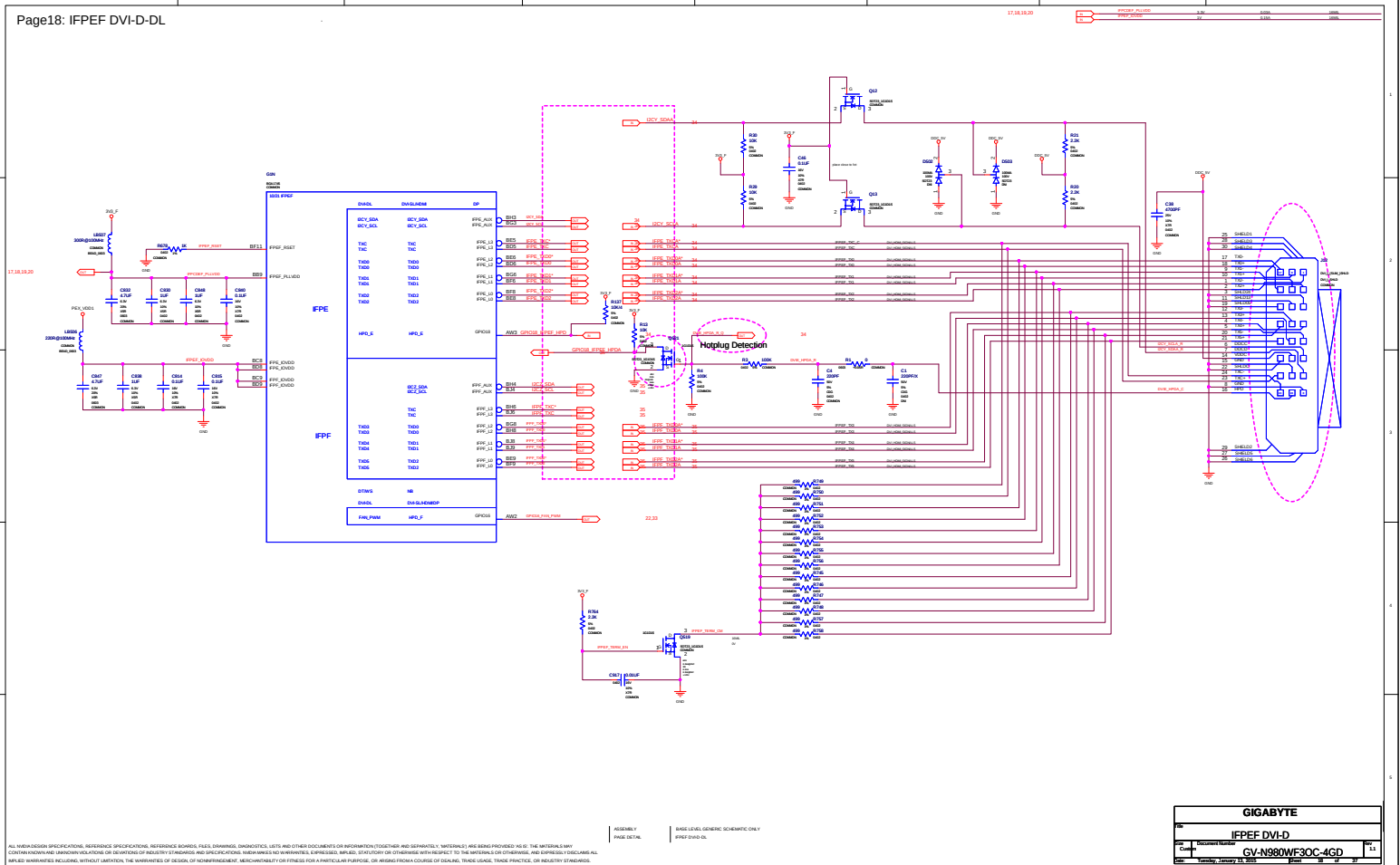
Page17: IFPAB DVI-I-DL

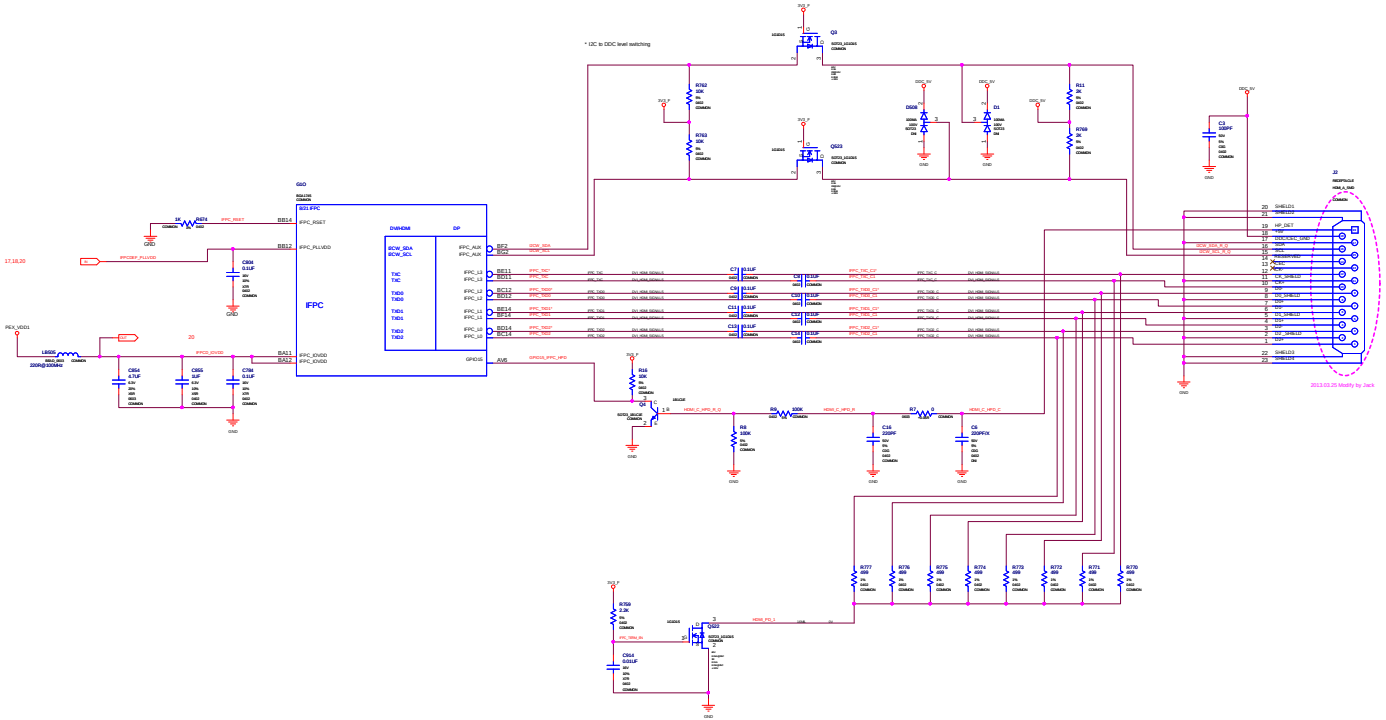


ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
IFPAB DVI-DL

Custom	Document Number		Rev 1.1
Date: Tuesday, January 13, 2015	Sheet 37 of 37		

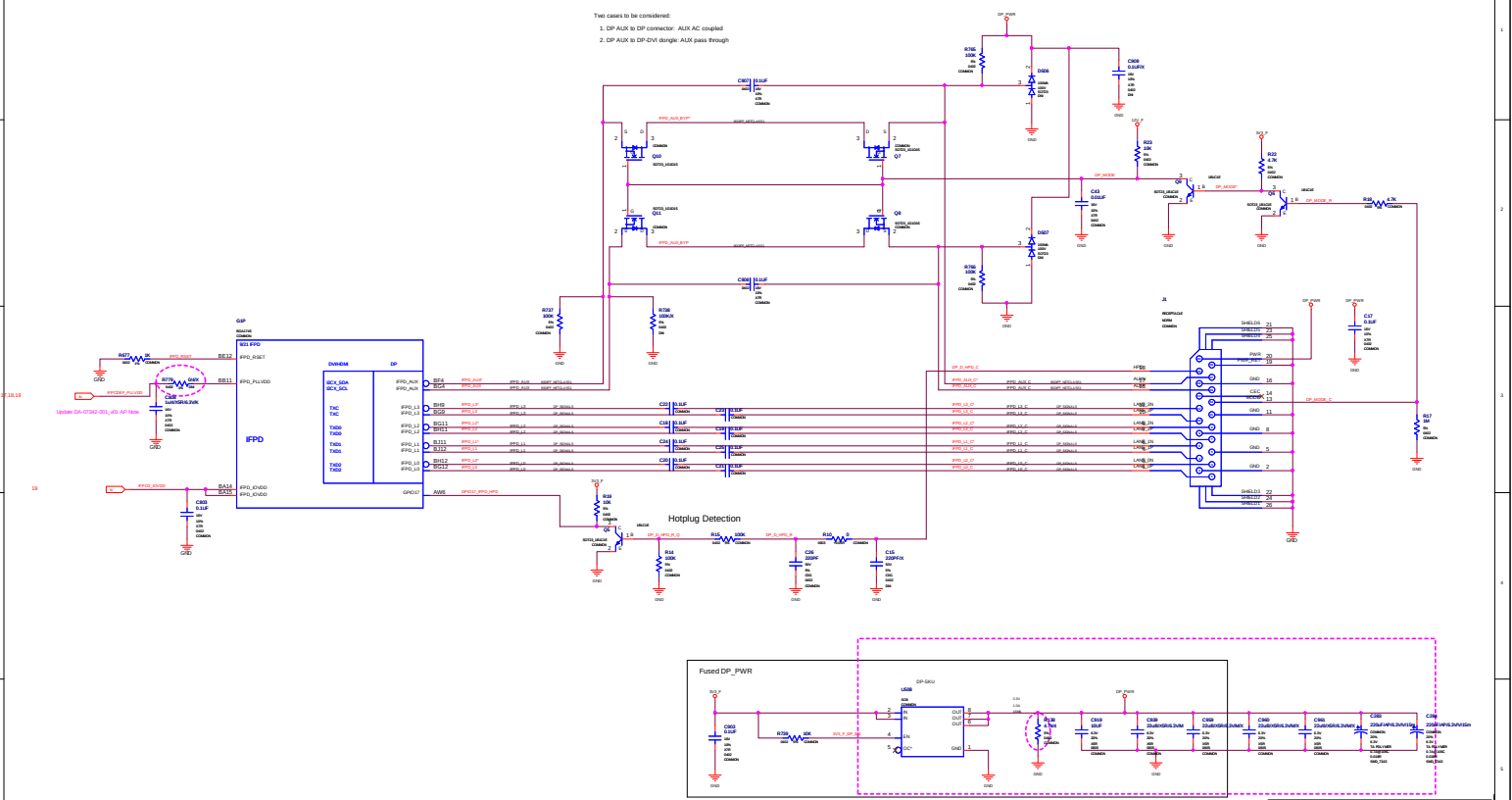




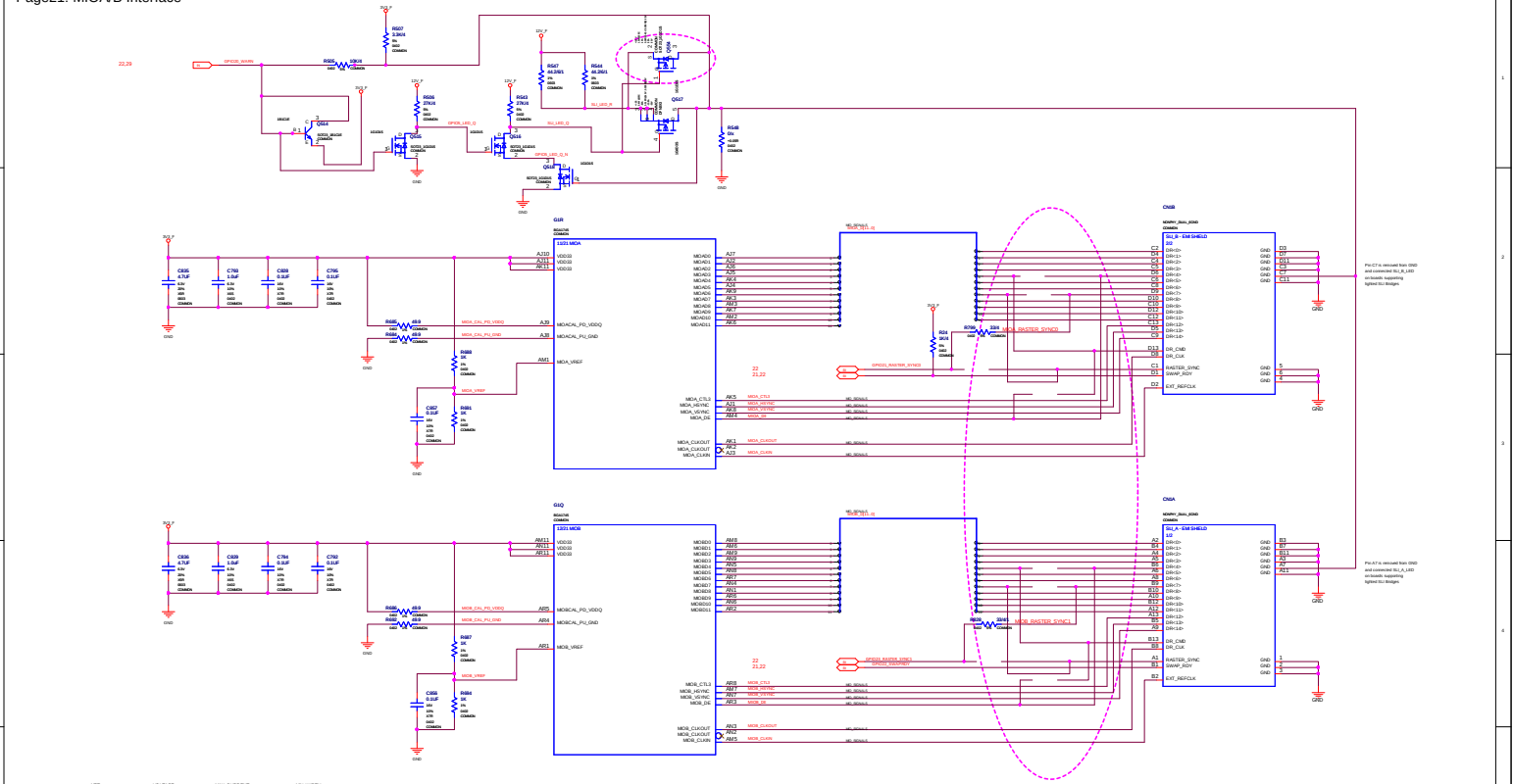
ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
IFPC HDMI

Page20: IFPD DP



Page21: MIOA/B Interface



NET	VOLTAGE	MAX_CURRENT	MIN_WIDTH
MIOA_VREF	1.65V		12MIL
MIOA_CAL_PU_VDDQ	1.35V		12MIL
MIOA_CAL_PU_GND	0V		12MIL
MIOB_VREF	1.65V		12MIL
MIOB_CAL_PU_VDDQ	1.35V		12MIL
MIOB_CAL_PU_GND	0V		12MIL

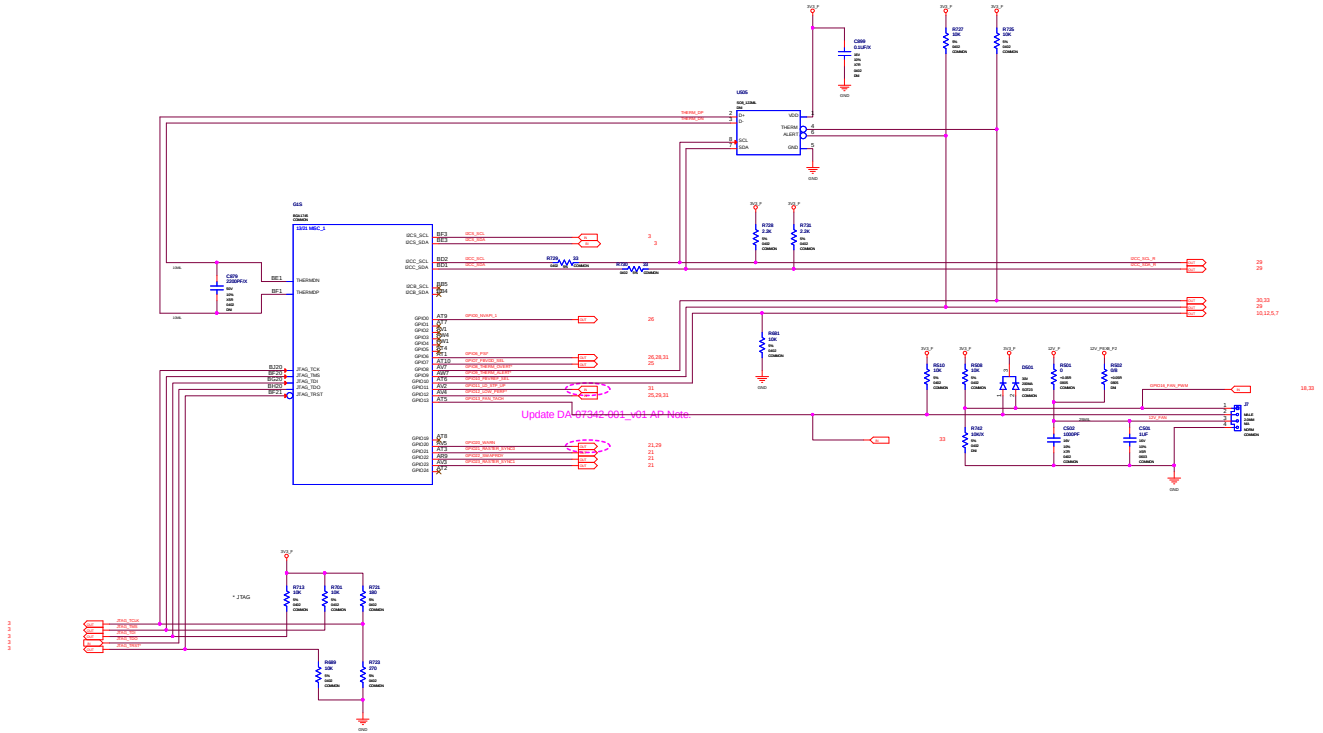
ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
MIOA/B Interface

Title	MIOA_B Interface
Size	Document Number: GV-N980WF3OC-4GD
Custom	Rev: 1.1
Date:	Tuesday, January 13, 2015 Sheet 21 of 37

GIGABYTE

Page22: MISC1: Fan, Thermal, JTAG, GPIO



ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
MISC1: Fan, Thermal, JTAG, GPIO

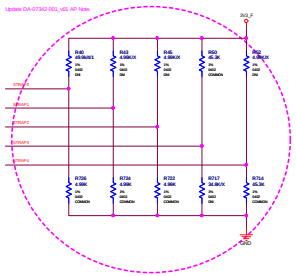
Page23: MISC2: ROM, XTAL, Straps

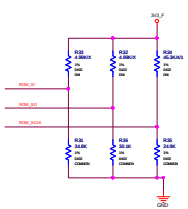
STRAP0	USER_BIT [3:0]*	0000*	5K PD*
STRAP1	3GIO_PADCFG_LUT_ADR*	0000*	5K PD Desktop*
STRAP2	PCI_DEVID [3:0]*	0000 - (0x1180)*	5K PD -600 GPU*
STRAP3	SOR_EXPOSED [3:0]*	1111*	45K PU*
STRAP4	DP_PLL_VDD_33V*	1* FOR 3_3V*	
	PEX_MAX_SPEED*	1* FOR GEN2/3*	45K PD*
	PEX_SPD_CHANGE_GEN3*	1* ENABLED*	
	*		
ROM_SI	RAMCFG[0]*	0*	
	RAMCFG[1]*	1*	35K PD*
	RAMCFG[2]*	1*	
	RAMCFG[3]*	0*	
ROM_SO	VGA_DEVICE*	1*	
	SMB_ALT_ADDR*	0*	10k PU*
	FB[0]_APERTURE_SIZE*	0* For 256MB*	
	FB[1]_APERTURE_SIZE*	1* For 256MB*	
ROM_SCLK	PEX_PLL_EN_TERM100*	0* DISABLED*	
	PCI_DEVID_EXT[5]*	0* For 0x1180*	25K PD*
	SUB_VENDOR*	1* Dedicated BIOS*	
	PCI_DEVID_EXT[4]*	0* For 0x1180*	

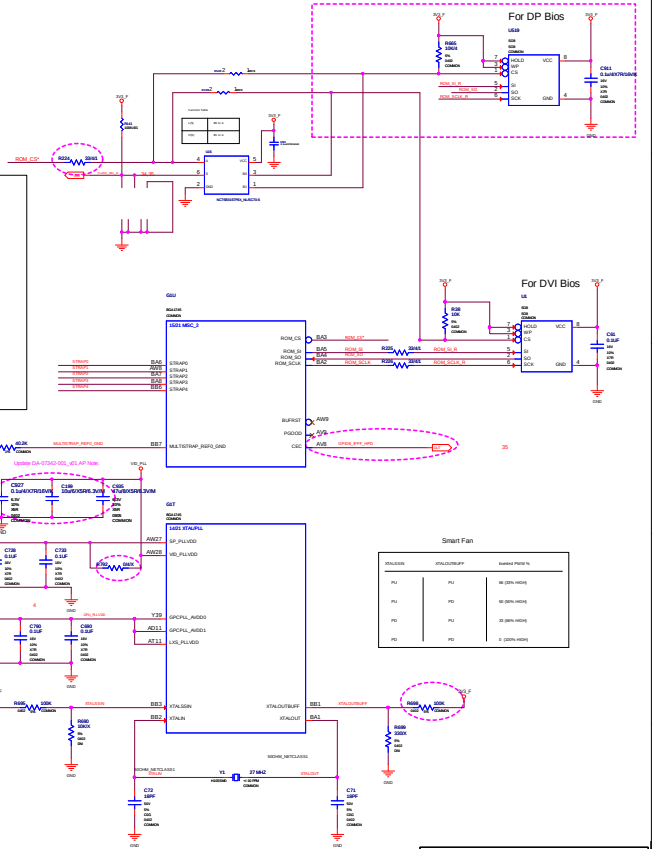
	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

CFG[3:0]	Config Width	Vendor
0000	Reserved	
0001	32Mx32 256-bit	Elpida
0010	32Mx32 256-bit	Hynix
0011	32Mx32 256-bit	Samsung
0100	Reserved	
0101	64Mx32 256-bit	Elpida
0110	64Mx32 256-bit	Hynix
0111	64Mx32 256-bit	Samsung
1000	Reserved	
1001	32Mx32 192-bit	Elpida
1010	32Mx32 192-bit	Hynix
1011	32Mx32 192-bit	Samsung
1100	Reserved	
1101	64Mx32 192-bit	Elpida
1110	64Mx32 192-bit	Hynix
1111	64Mx32 192-bit	Samsung

MULTI_STRAP_REF0_GND	
BRINNY PRODUCTION	NC
BRINNY BRINGUP	NC
MULTI-LEVEL	40.2K TO GND







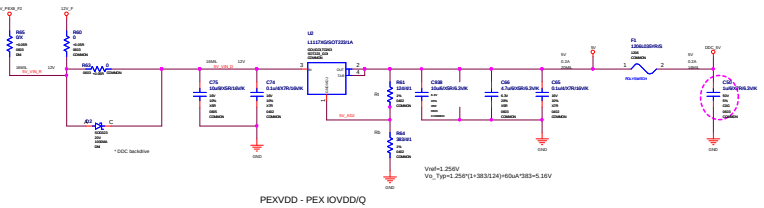
ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
MISC2: ROM, XTAL, Straps

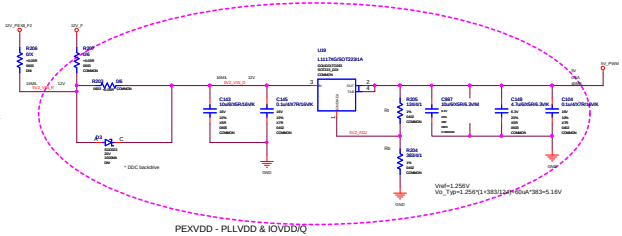
Title	ROM Xtal Straps
Size	Document Number: GV-N980WF3OC-4GD
Custom	Rev: 1.1
Date:	Tuesday, January 13, 2015 Sheet 23 of 37

GIGABYTE

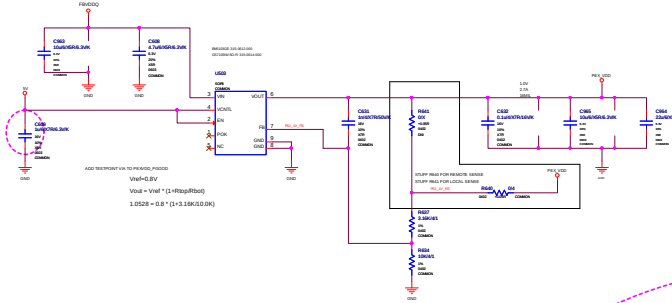
Page24: PS: 5V, PEX_VDD

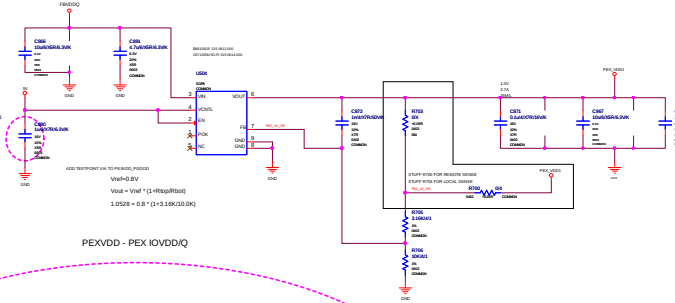


PEXVDD - PEX IOVDD/Q



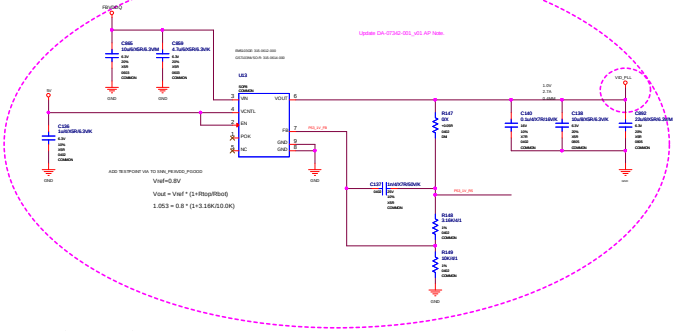
PEXVDD - PLLVDD & IOVDD/Q





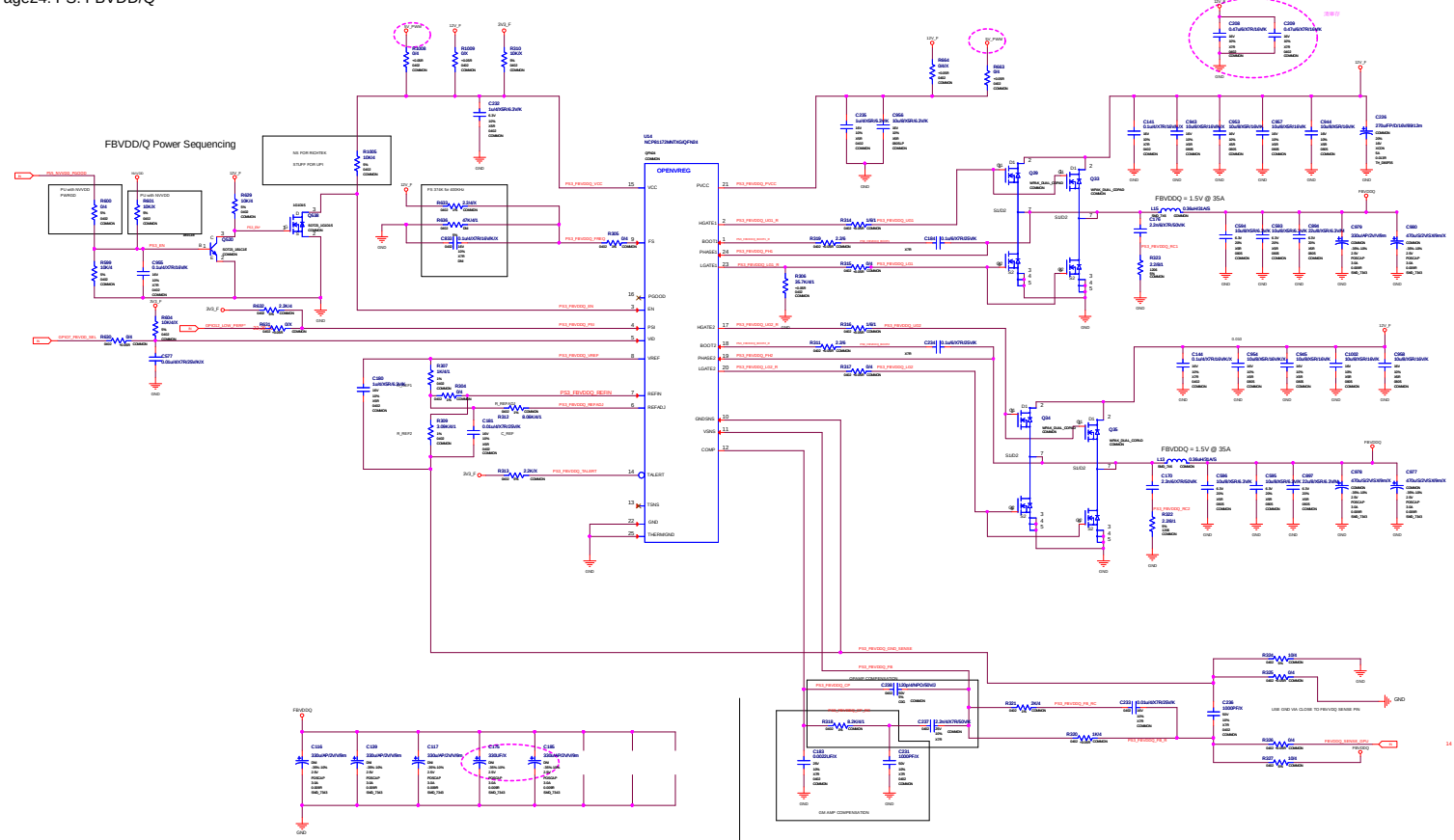
PEXVDD - PEX IOVDD/Q

Del PEXVDD Converter

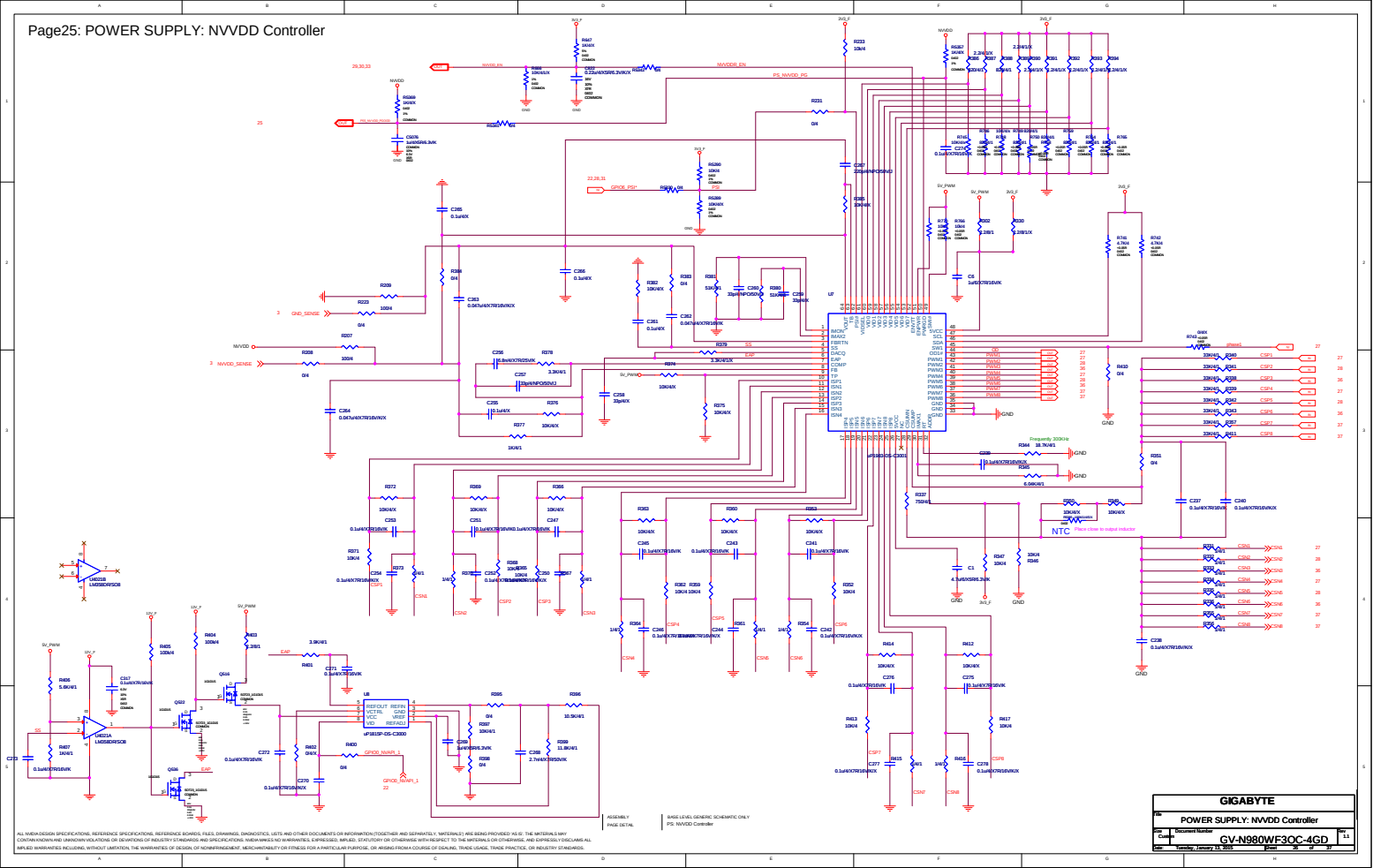


ASSEMBLY	BASE LEVEL GENERIC SCHEMATIC ONLY	
PAGE DETAIL	PS: 5V_PEX_VDD	

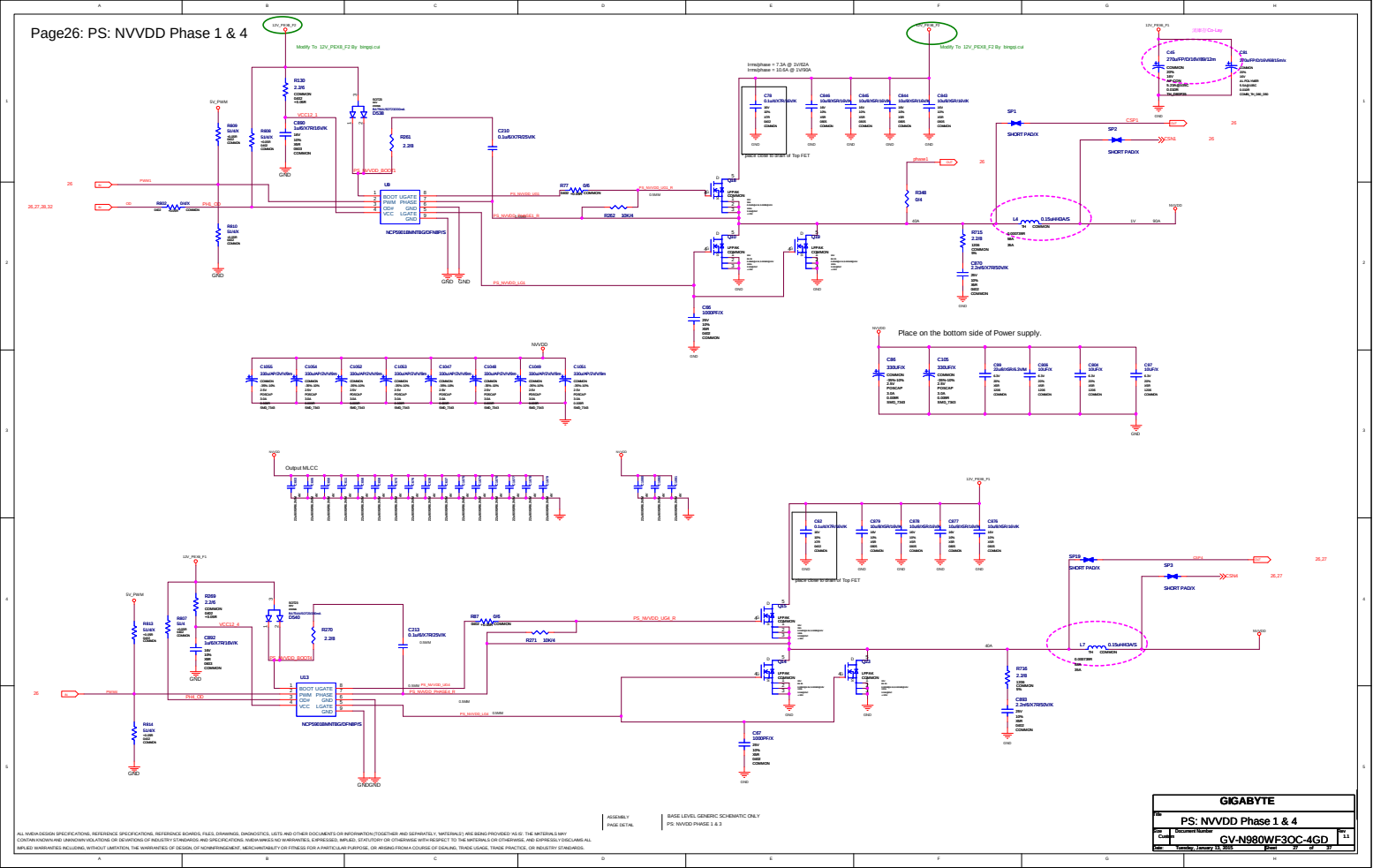
GIGABYTE			
File: 5V PEX_VDD			
Size: C	Document Number: GV-N980WF3OC-4GD		Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 36 of 37		



Page25: POWER SUPPLY: NVVDD Controller



Page26: PS: NVVDD Phase 1 & 4

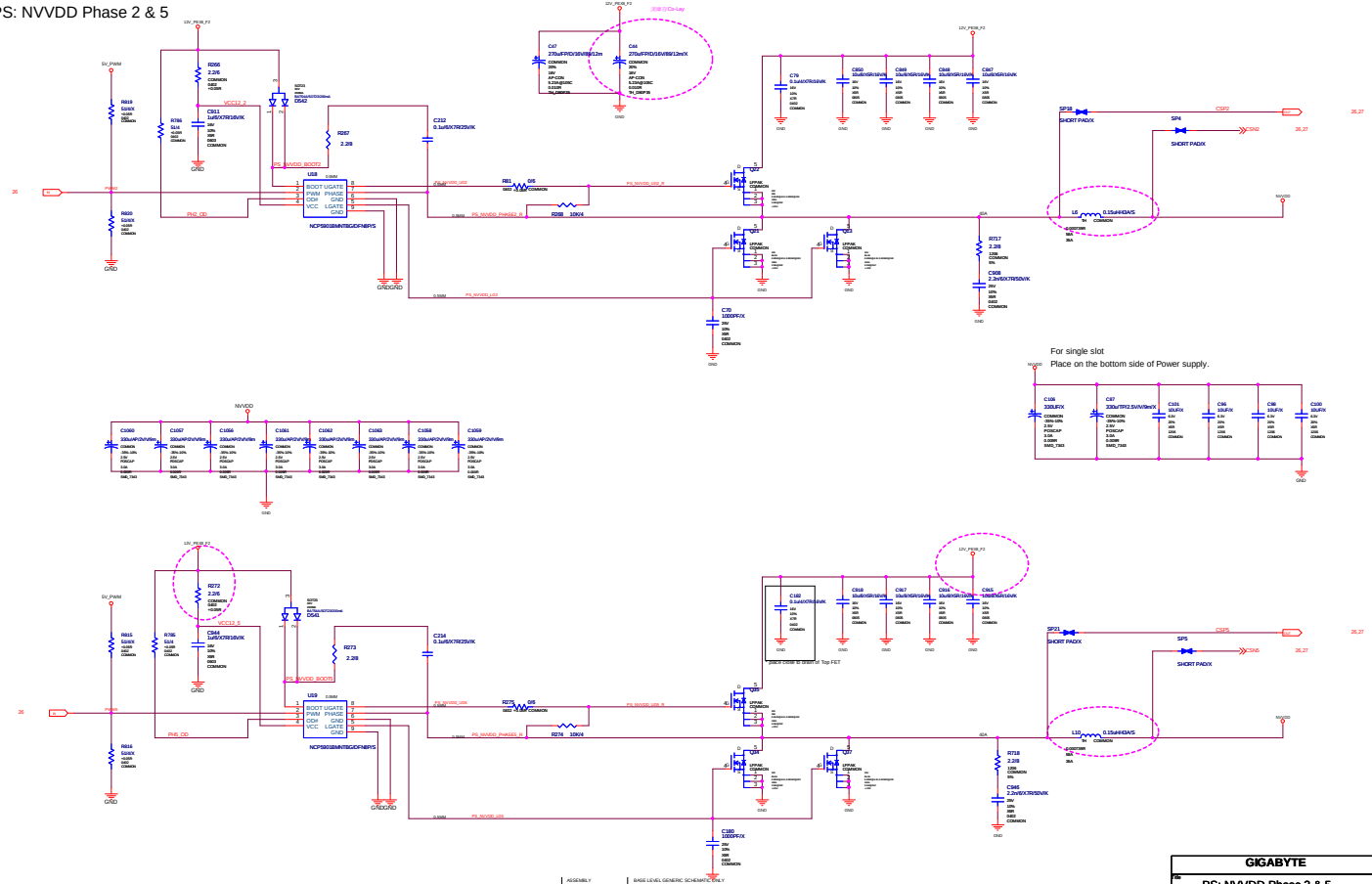


ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
PS: NVVDD Phase 1 & 3

GIGABYTE		
Title	PS: NVVDD Phase 1 & 4	
Size: C	Document Number: GV-N980WF3OC-4GD	Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 37 of 37	

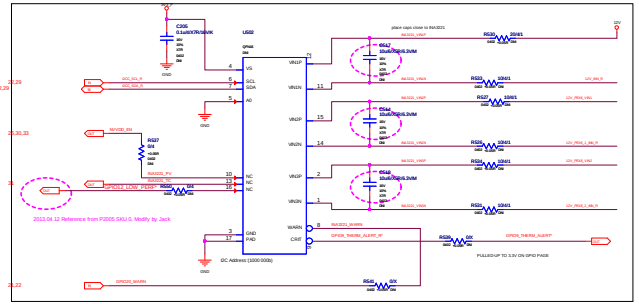
Page27: PS: NVVDD Phase 2 & 5

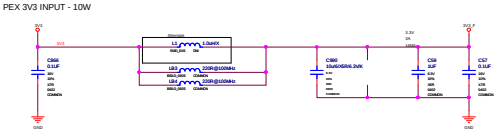


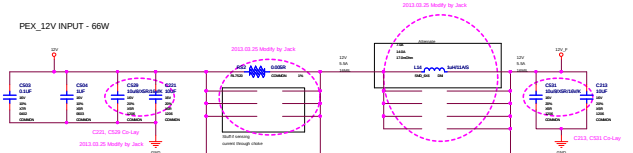
GIGABYTE

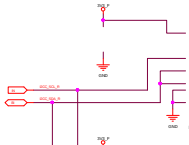
Title	PS: NVVDD Phase 2 & 5
Size: C	Document Number: GV-N980WF3OC-4GD
Rev: 1.1	
Date: Tuesday, January 13, 2015	Sheet 26 of 37

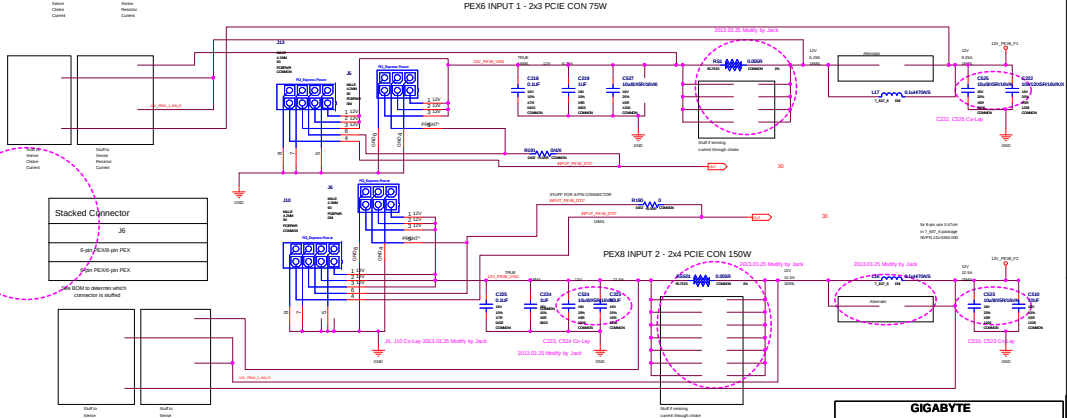
Page30: PS: Inputs, Filtering, and Monitoring











ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
PS: Inputs, Filtering, and Monitoring

Page31: PS: Shutdown

THERM OVERT SHUTDOWN LATCH

IFP_IOVDD (backdrive prevention)

PEX Input - NVVDD Power Sequence

PEX Input Present 1

PEX Input Present 2

Update DA-07342-001_v01 AP Note.

POWER CONNECTOR HPD

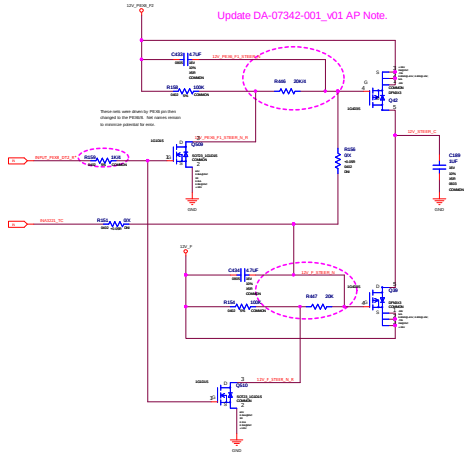
ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
PS: Shutdown

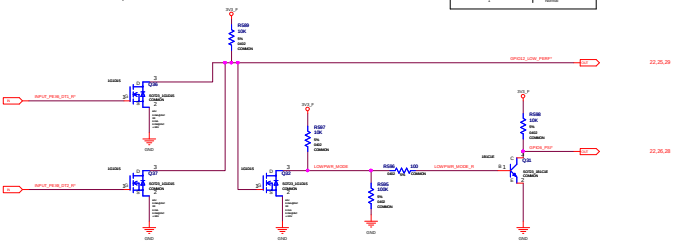
	GIGABYTE
File	Shutdown
Size: C	Document Number: GV-N980WF3OC-4GD
Custom	Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 30 of 37

Page32: PS: 12V Current Steering, PSI Control, and LED

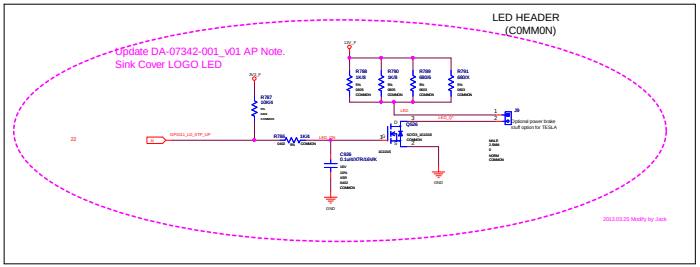
PEX Input - 12V Current Steering FETs



PEX Input - Power Level/PSI* Control



GeForce Logo LED



ASSEMBLY
PAGE DETAIL

BASE LEVEL GENERIC SCHEMATIC ONLY
PS: 12V Current Steering PSI Control and LED

GIGABYTE		
File: 12V Current Steering, PSI Control, and LED		
Size: C	Document Number: GV-N980WF3OC-4GD	Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 31 of 37	

Brackets:

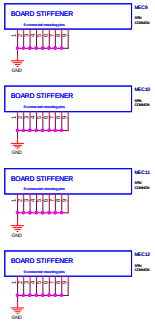
Bracket Screw

Hockey Stick

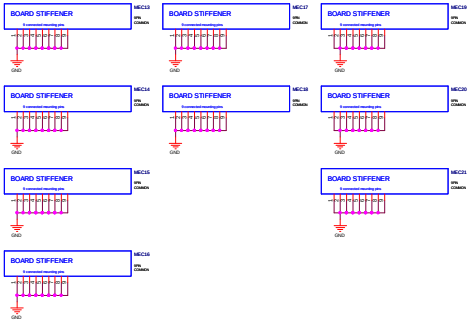
GPU Stiffner

Mechanical Holes Symbol

MH-TC236BC335D125-8



MH-C236D118-8



ASSEMBLY
PAGE DETAIL

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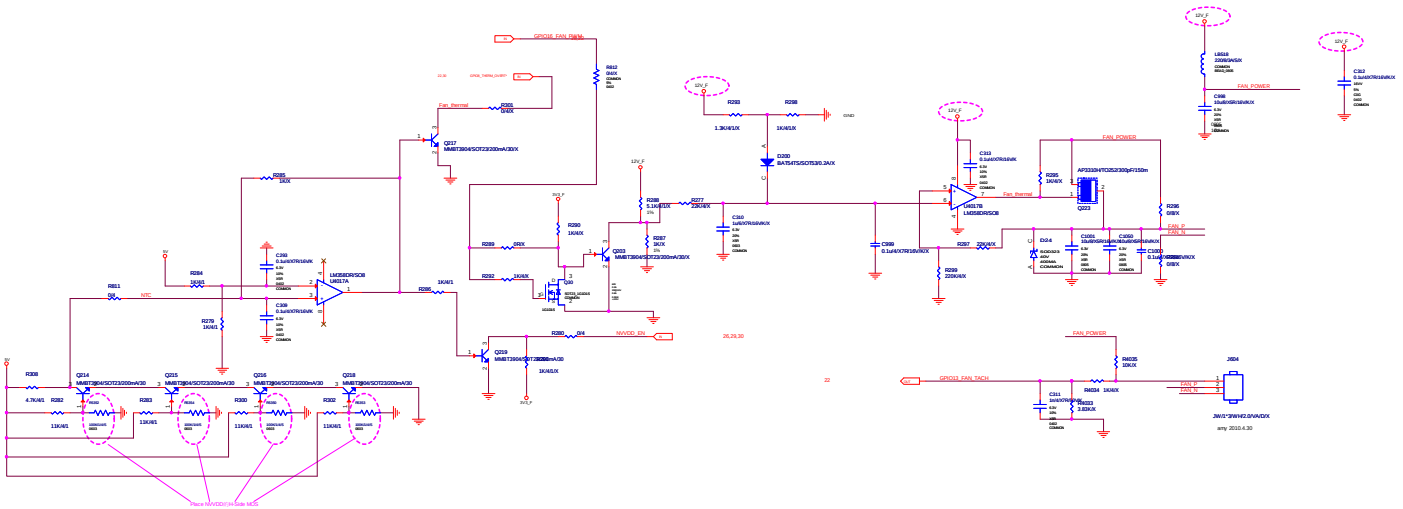
MECH: Bracket/Thermal

GIGABYTE		
File: Thermal Bk		
Size: C	Document Number: GV-N980WF3OC-4GD	Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 32 of 37	

Thermal_3 Pin Fan

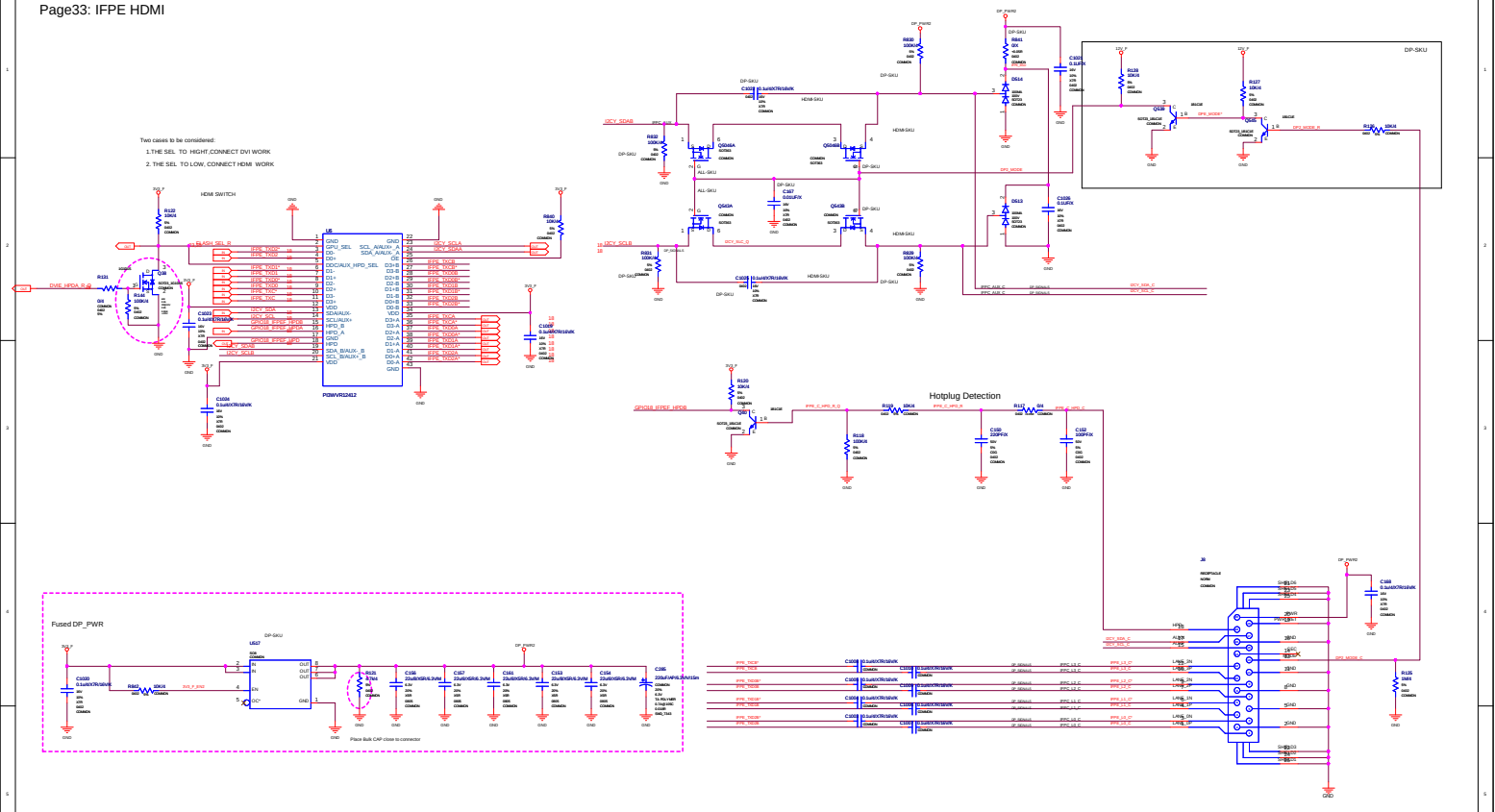


ASSEMBLY
PAGE DETAIL

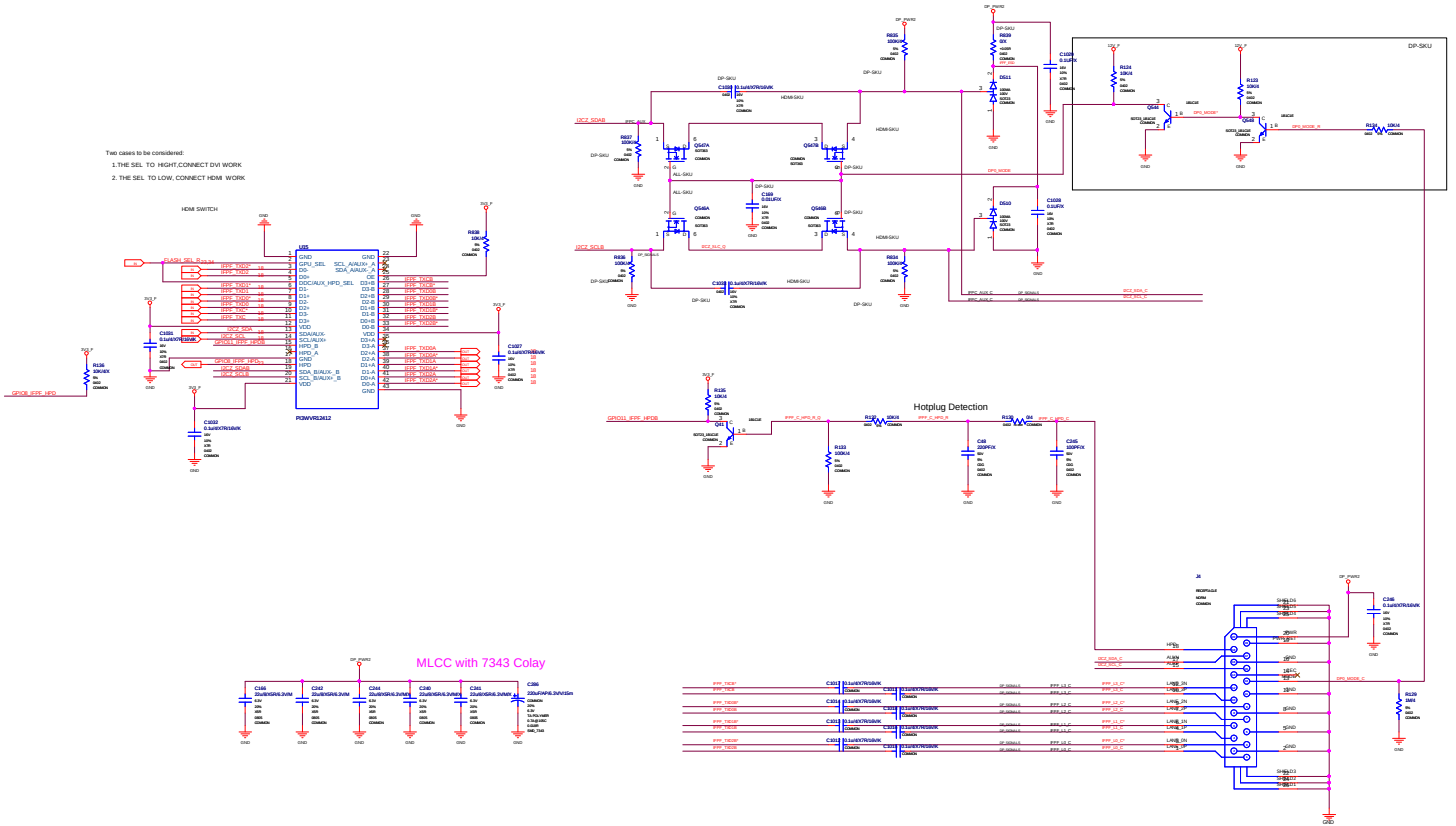
BASE LEVEL GENERIC SCHEMATIC ONLY
Sinaps, Thermal, Mechanical

GIGABYTE			
Title: 33_ Thermal_3 Pin Fan			
Size: C	Document Number: GV-N980WF3OC-4GD		Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 33 of 37		

Page33: IFPE HDMI



Page34: IFPF DP



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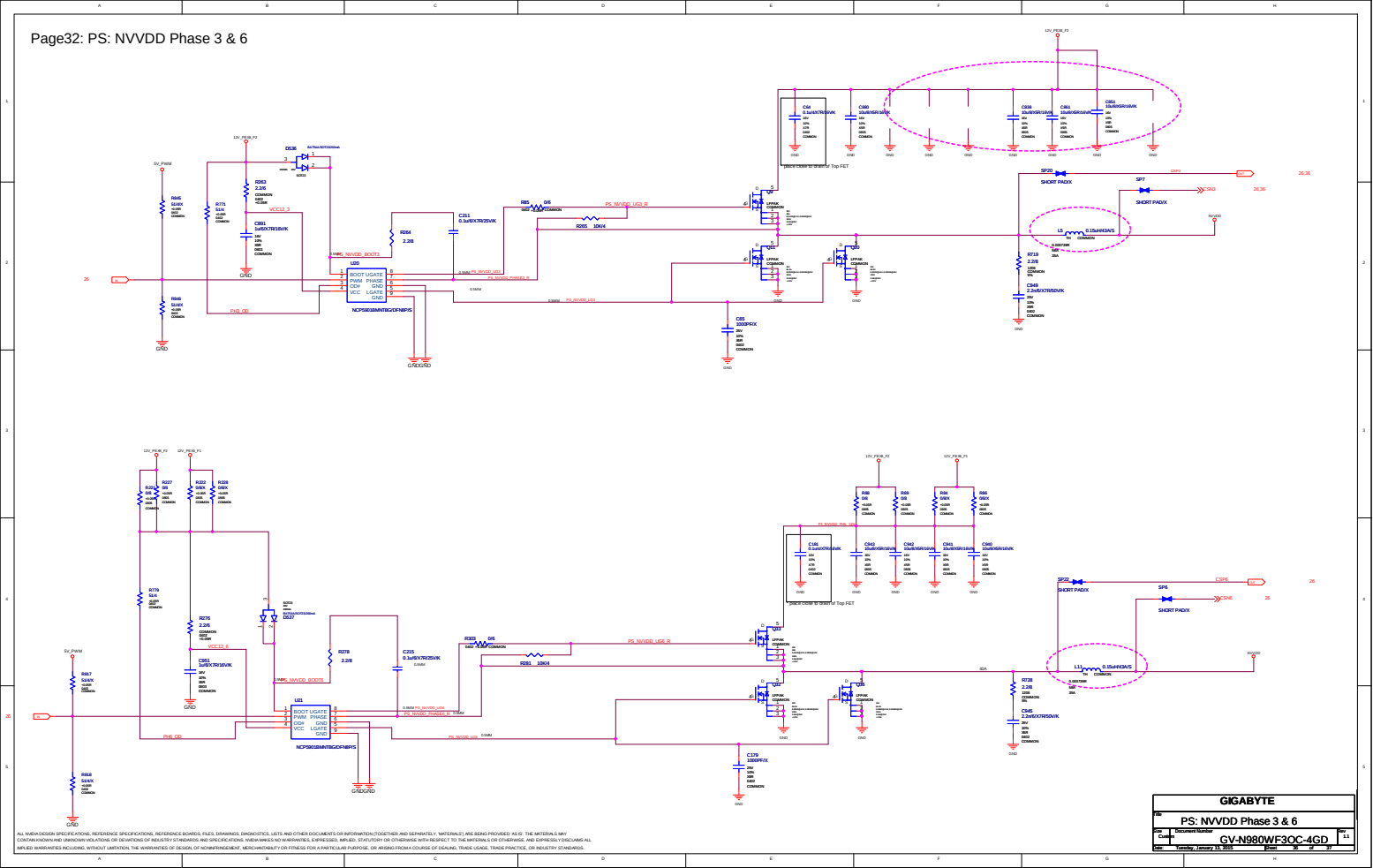
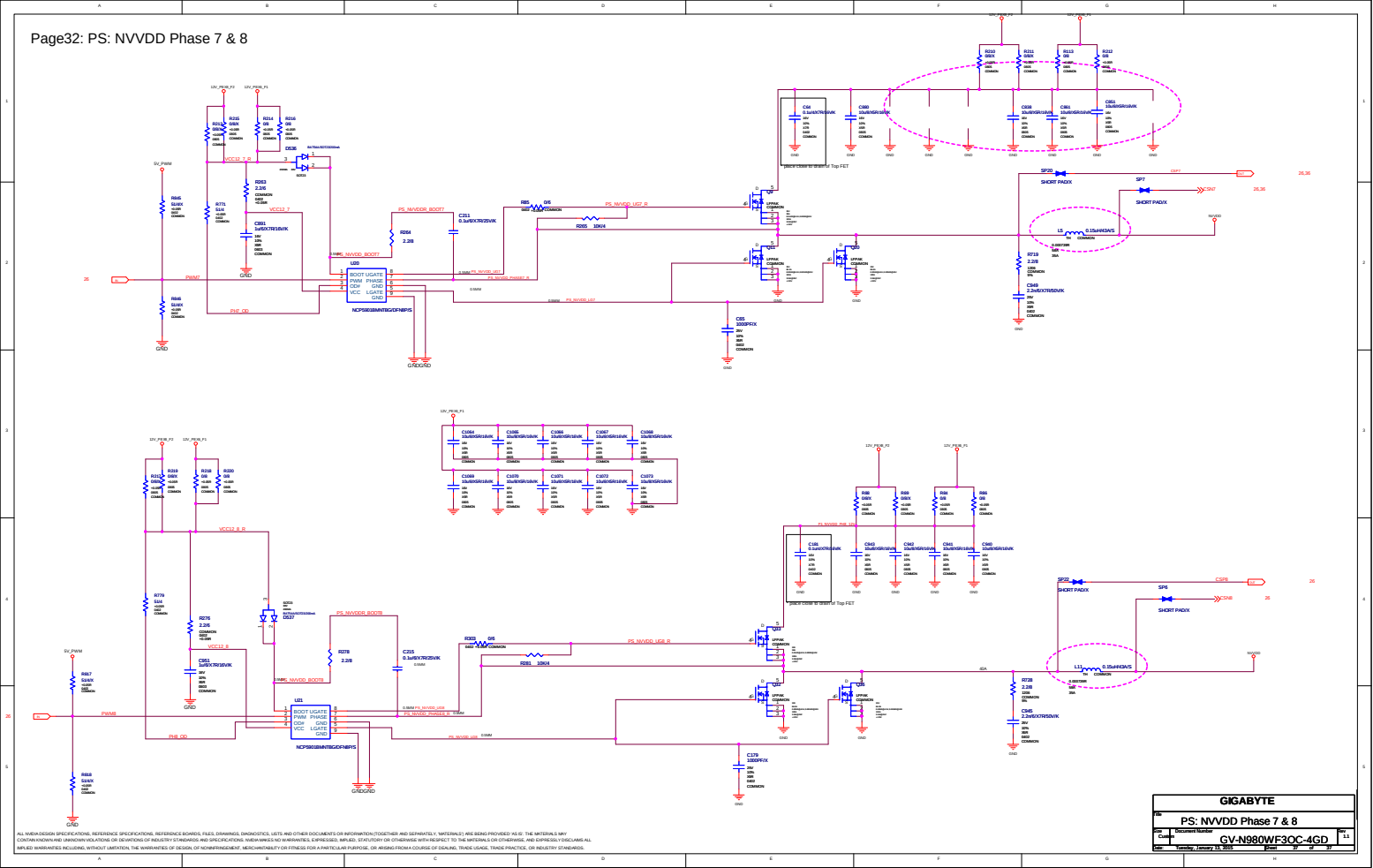
File	PS: NVVDD Phase 1 & 3
Size: A	Document Number: GV-N980WF3OC-4GD
Custom	Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 36 of 37

Page32: PS: NVVDD Phase 3 & 6



GIGABYTE			
File: PS: NVVDD Phase 3 & 6			
Size: Custom	Document Number: GV-N980WF3OC-4GD		Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 36 of 37		

Page32: PS: NVVDD Phase 7 & 8



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GIGABYTE			
Title: PS: NVVDD Phase 7 & 8			
Size: Custom	Document Number: GV-N980WF3OC-4GD		Rev: 1.1
Date: Tuesday, January 13, 2015	Sheet 32 of 37		