

PG600-B02 NIGHTHAWK

GB3B-384, 6GB GDDR5 128Mx32

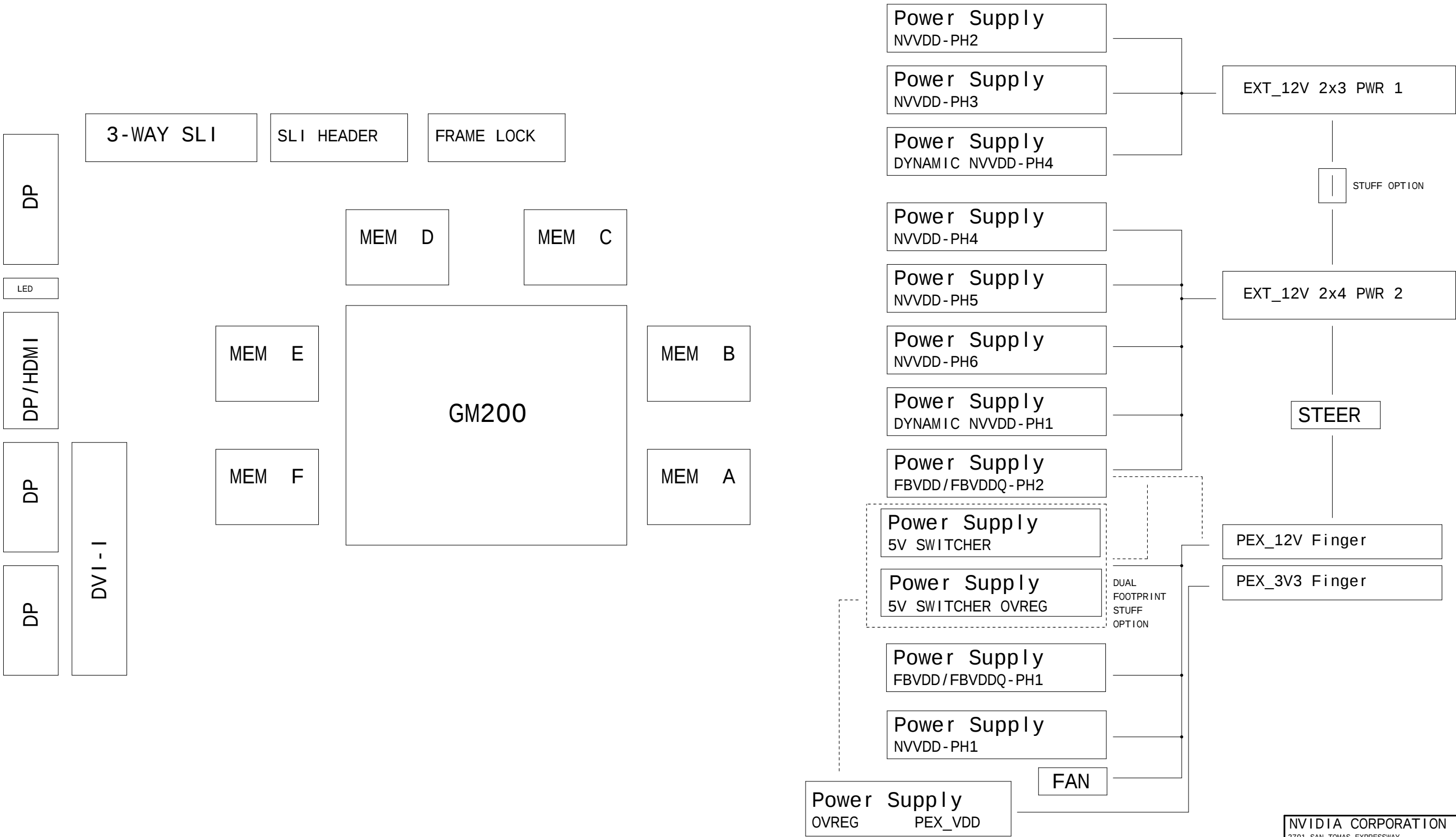
DP + HDMI / DP + DP + DP + DVI-I

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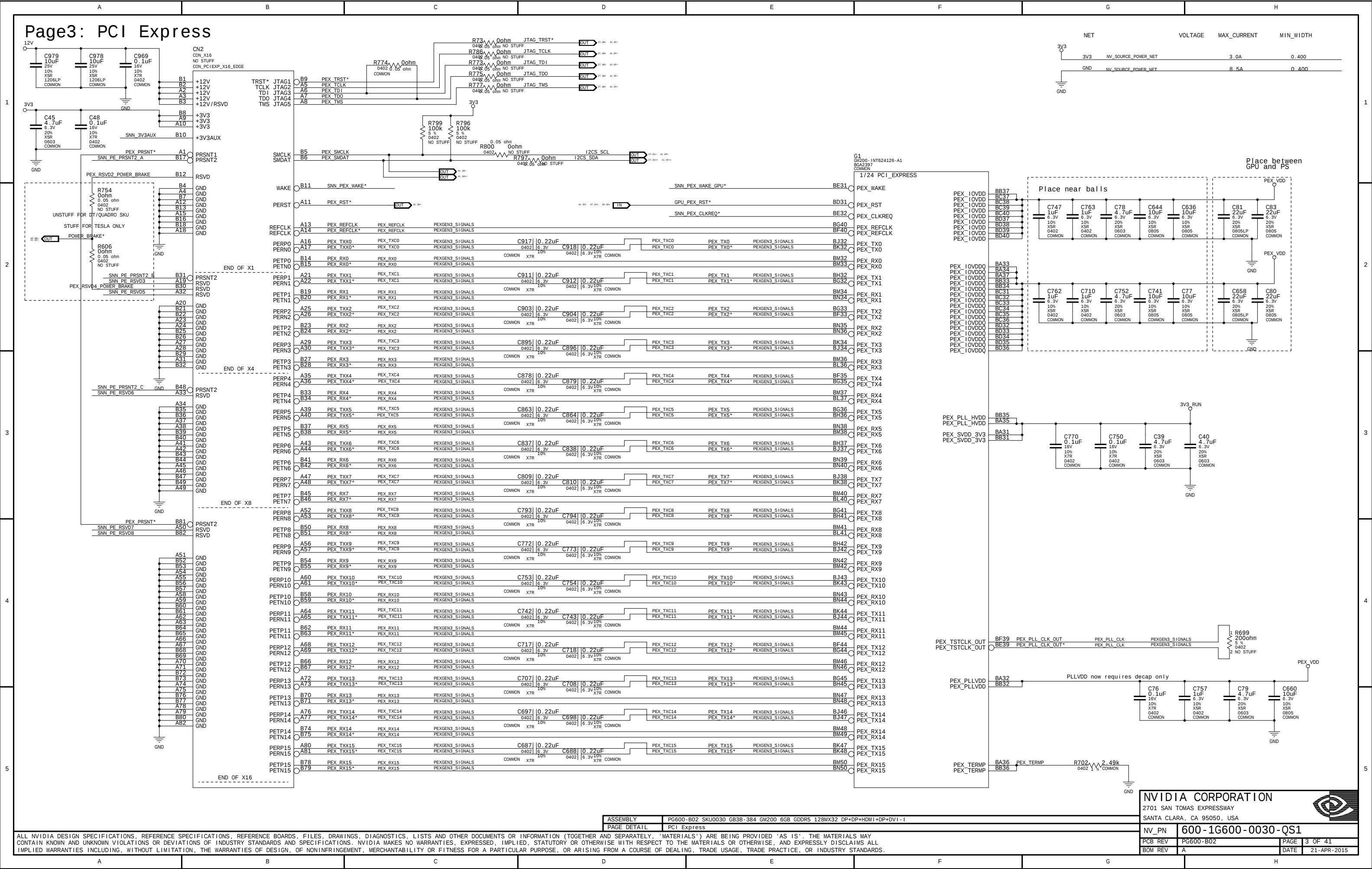
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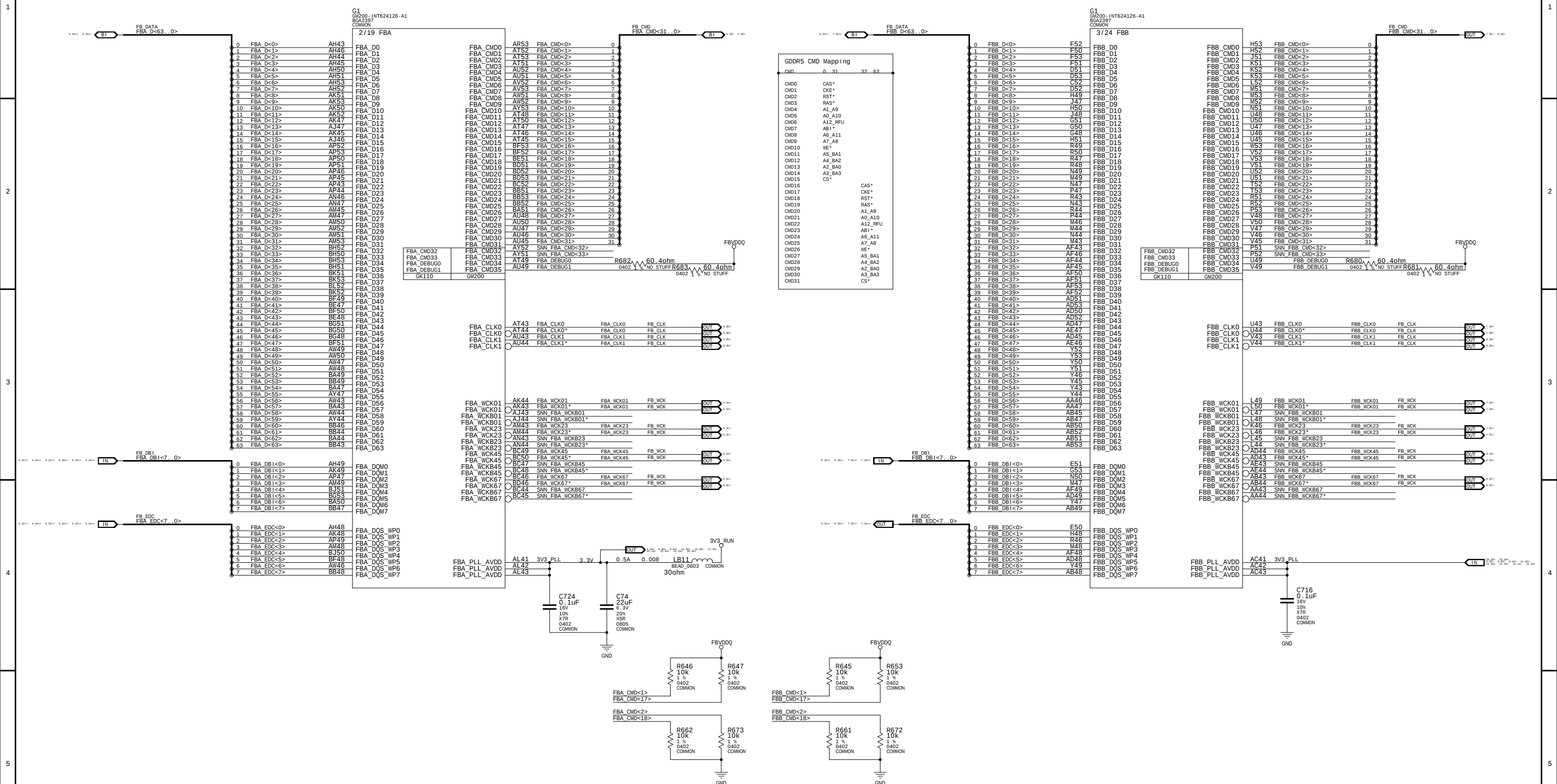
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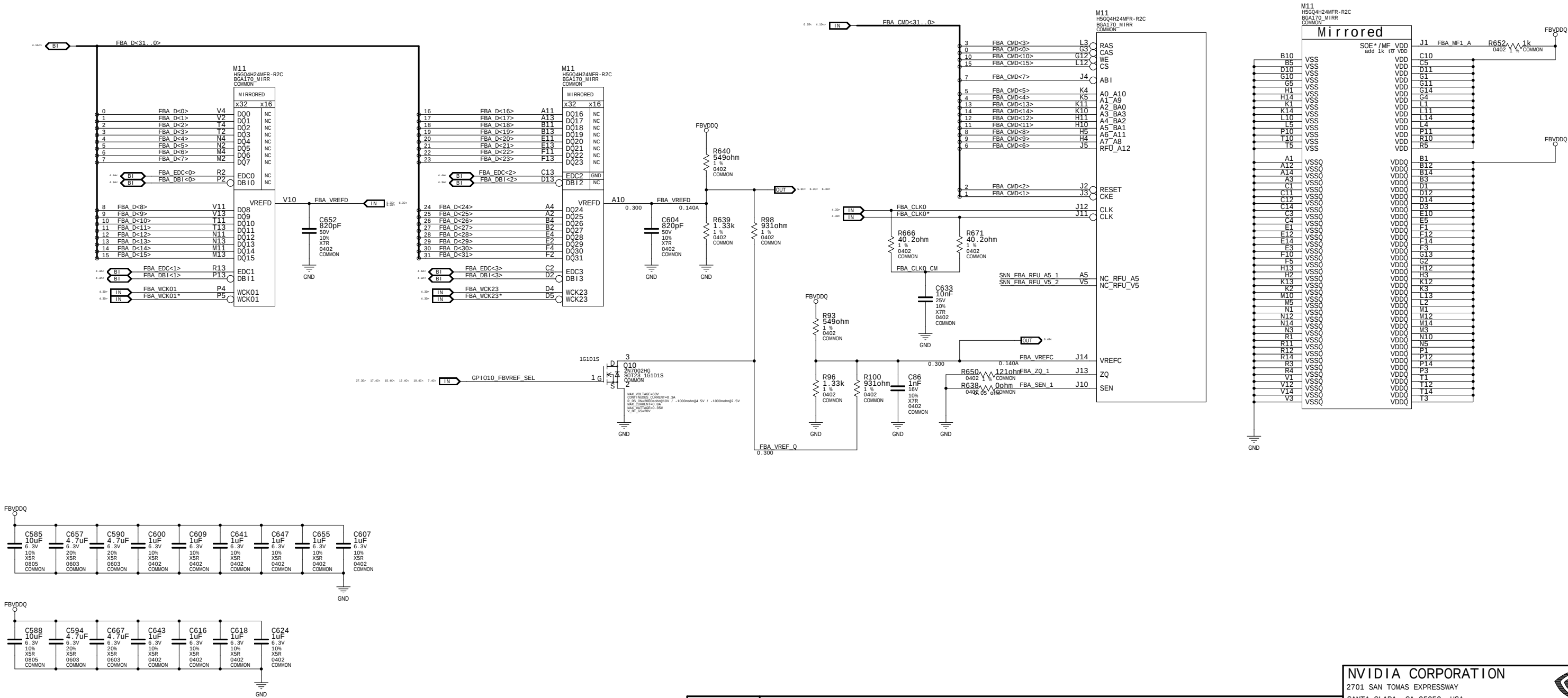
Page2: Block Diagram



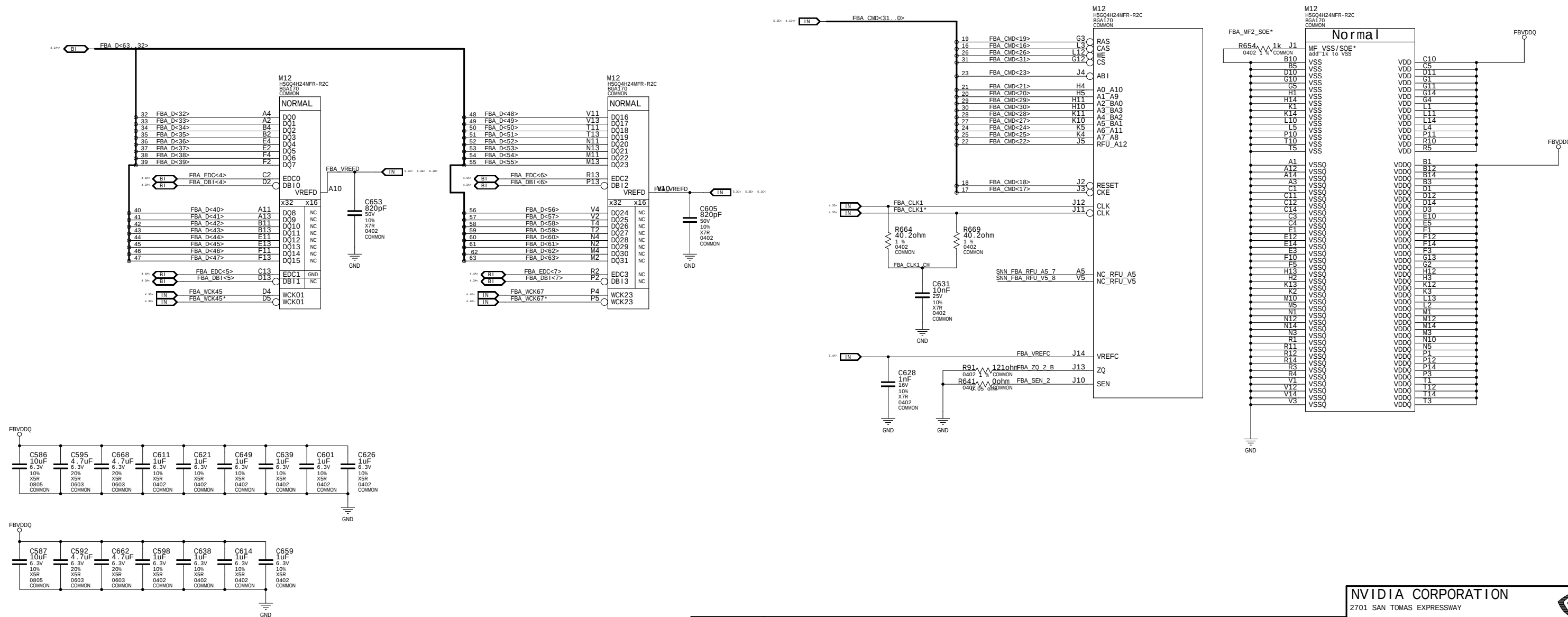
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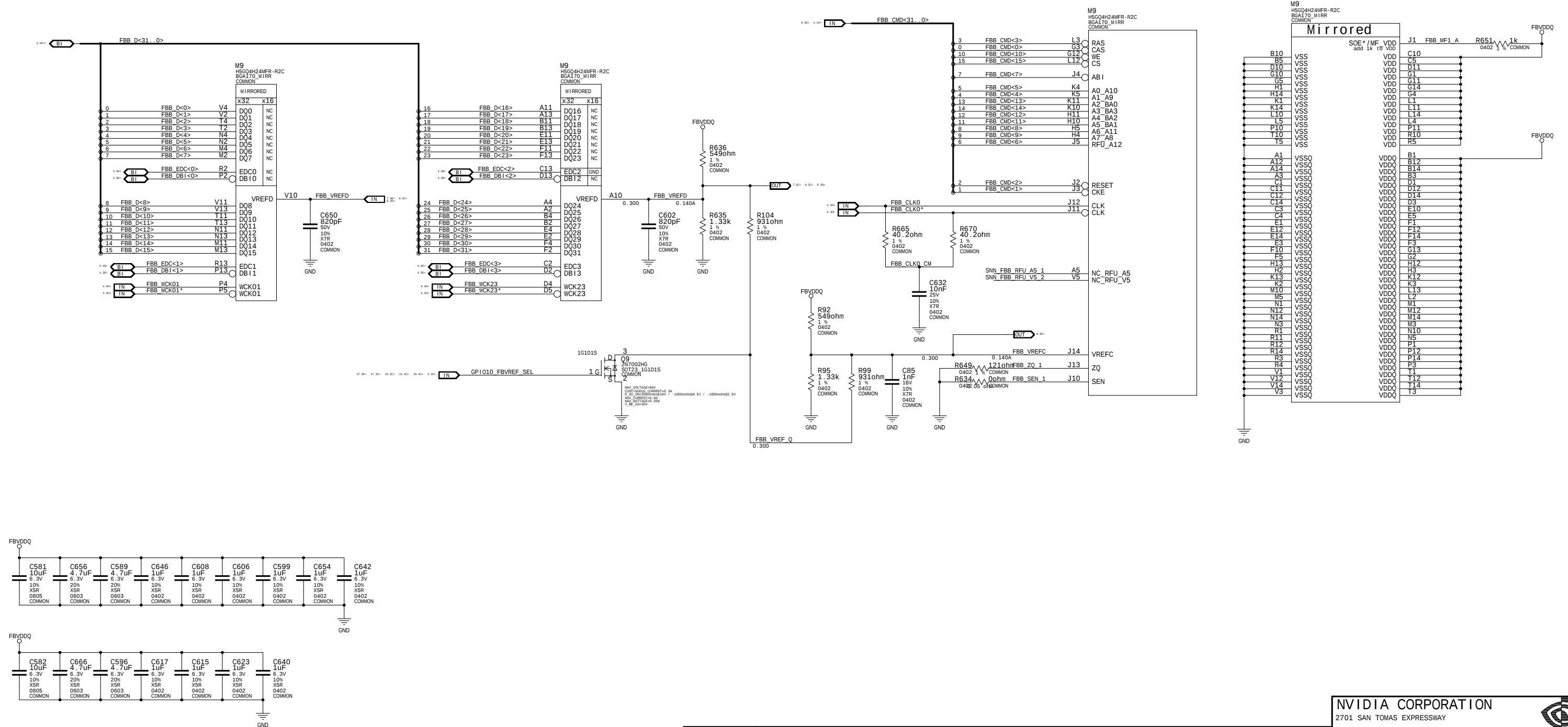


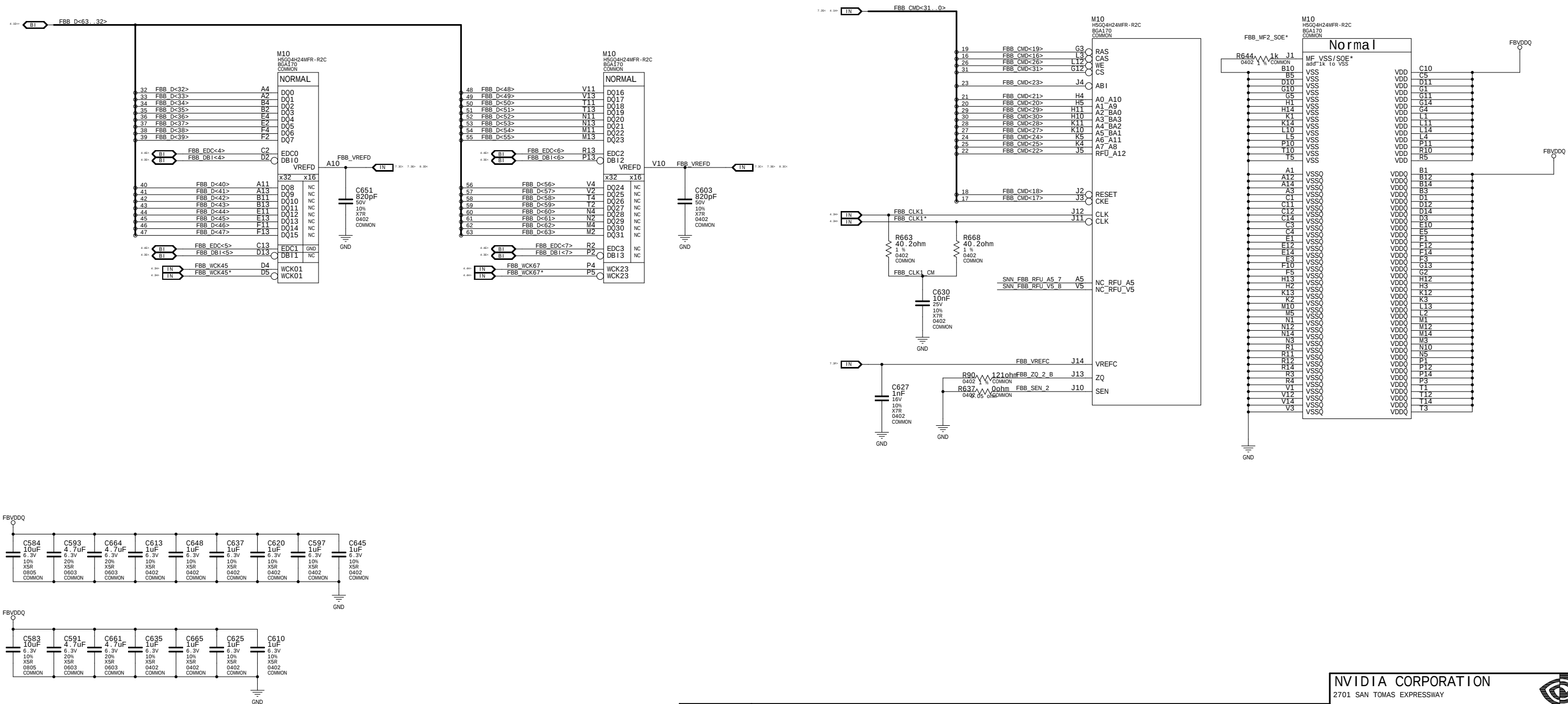




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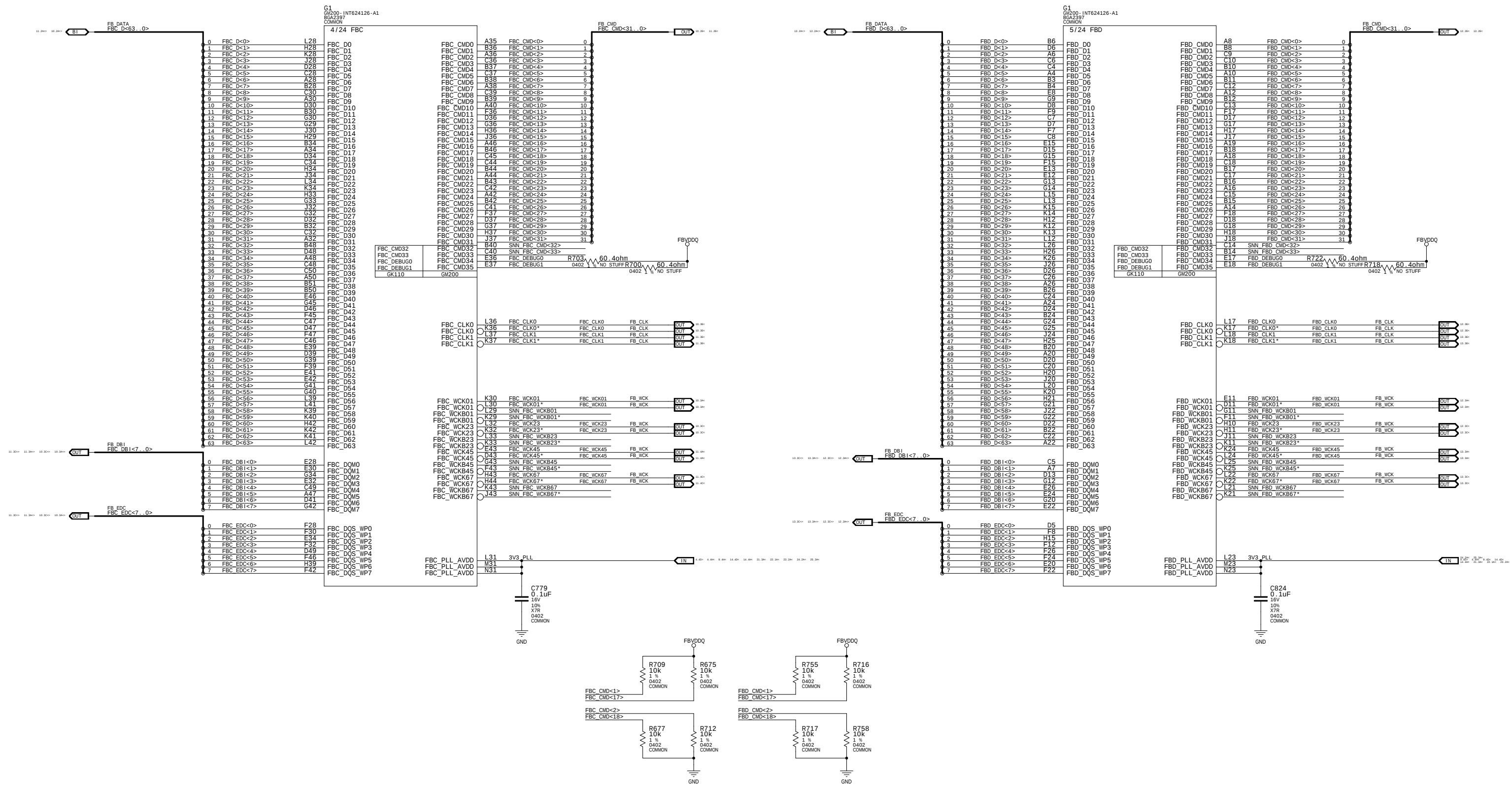




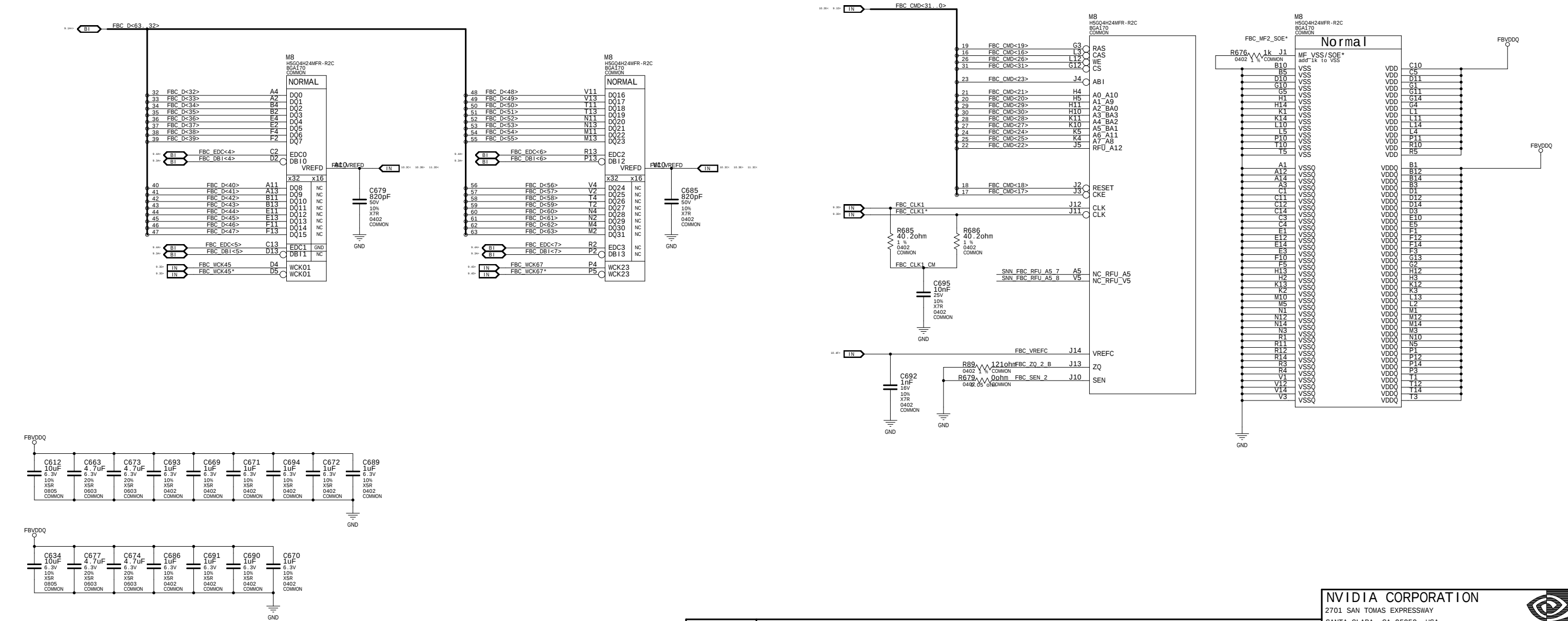
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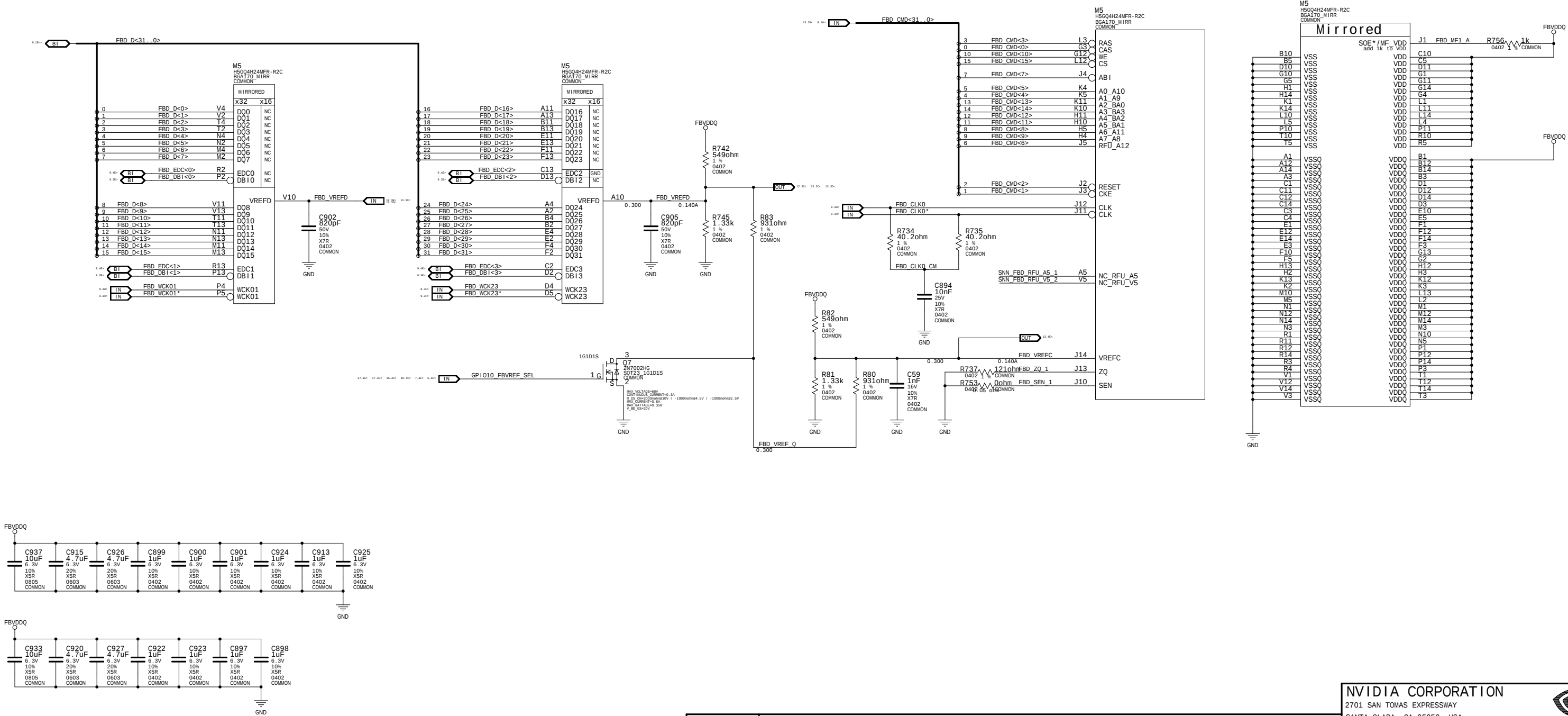
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ASSEMBLY

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PAGE DETAIL

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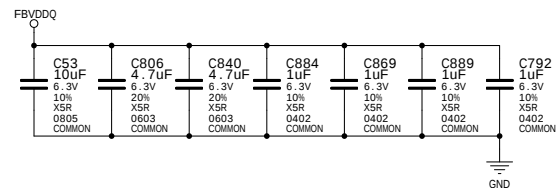
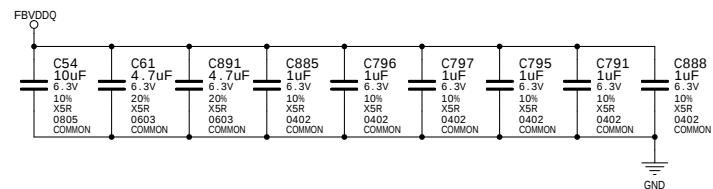
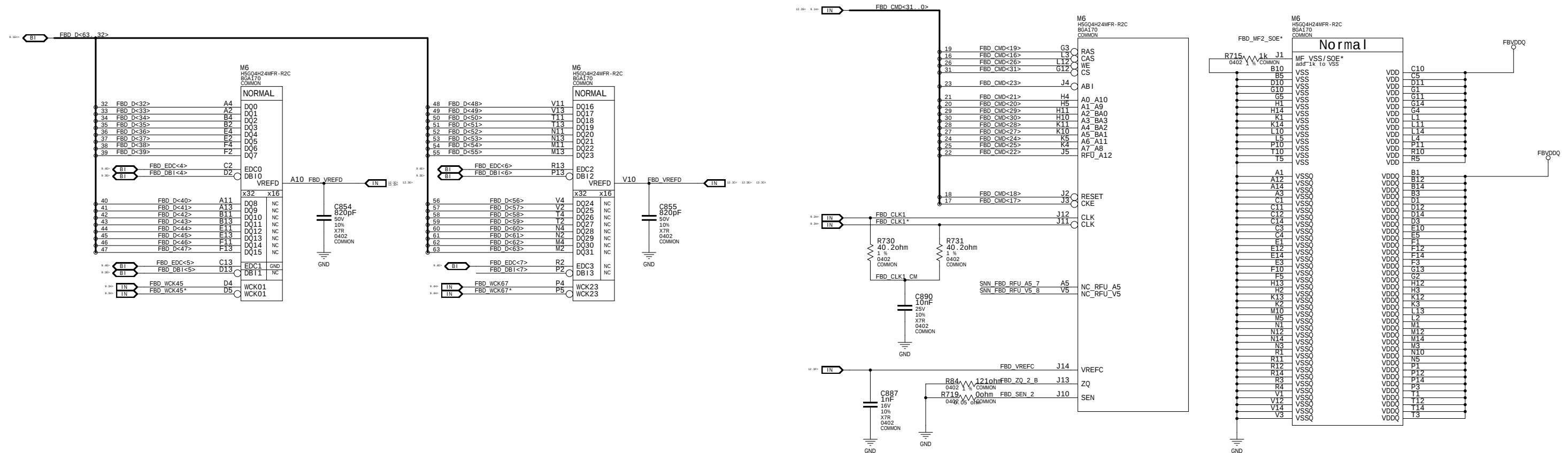
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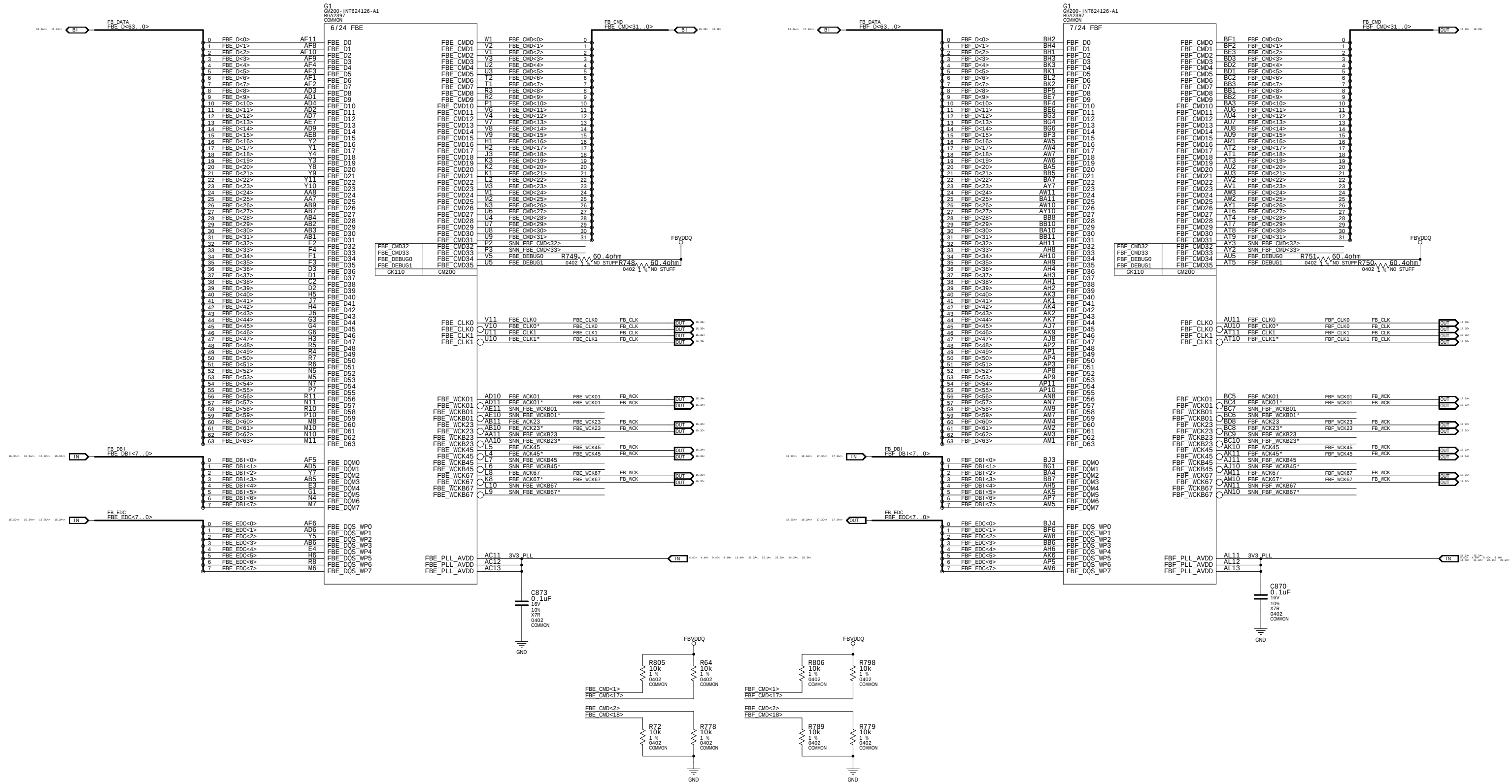
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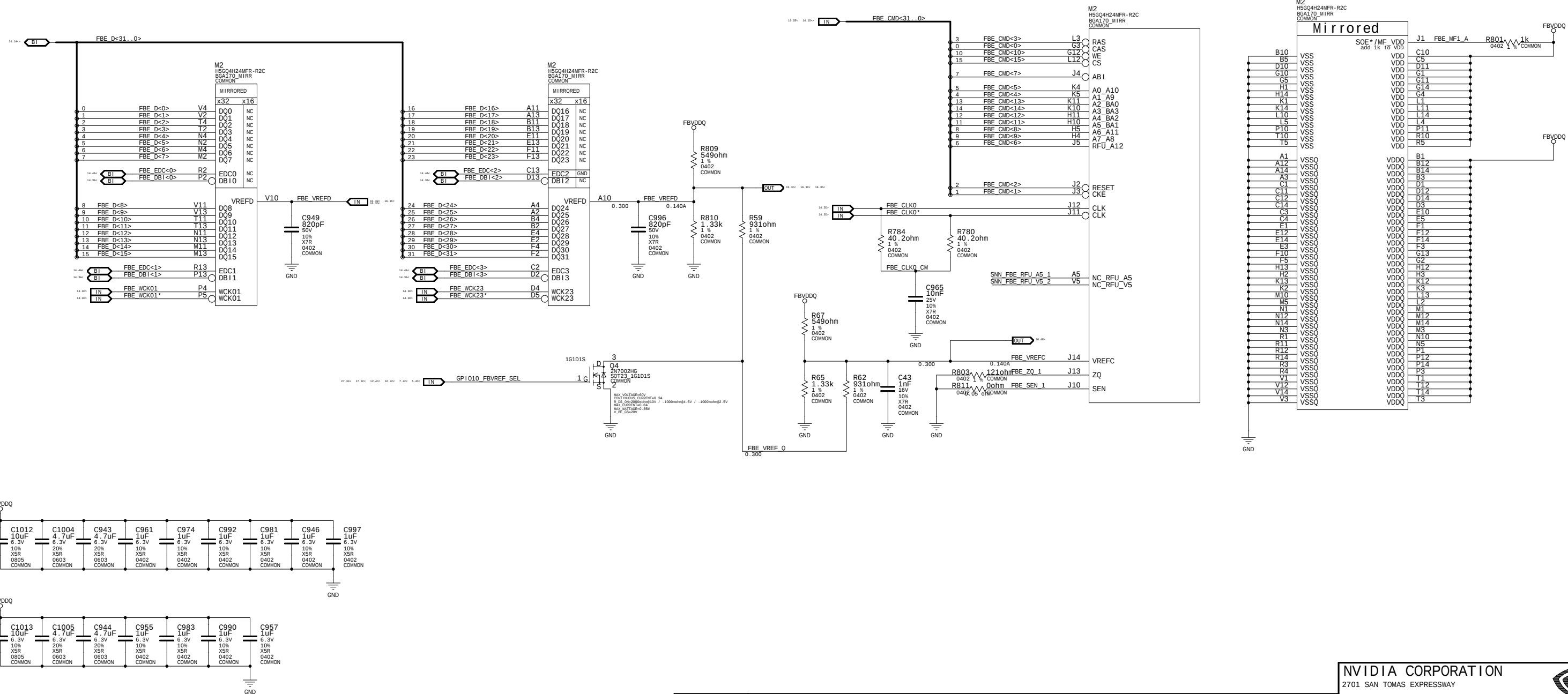


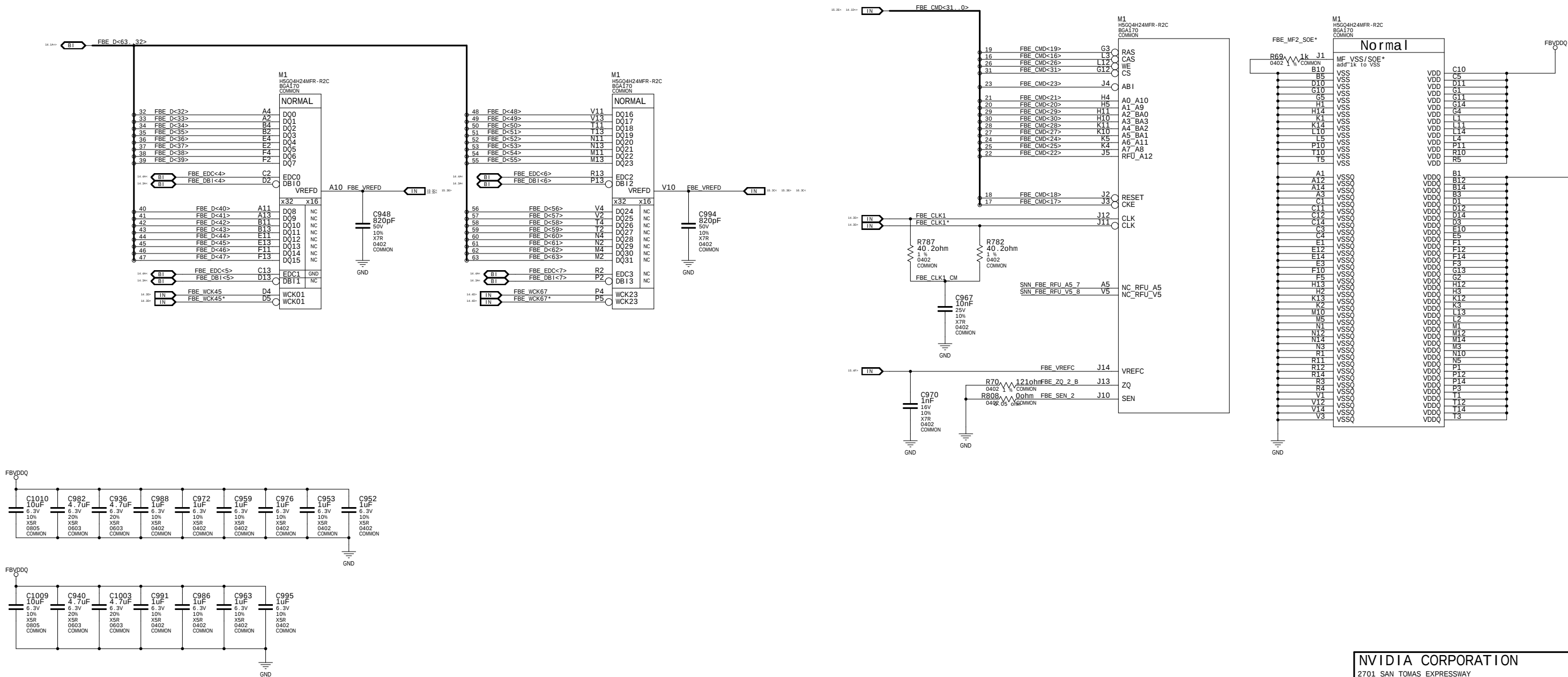
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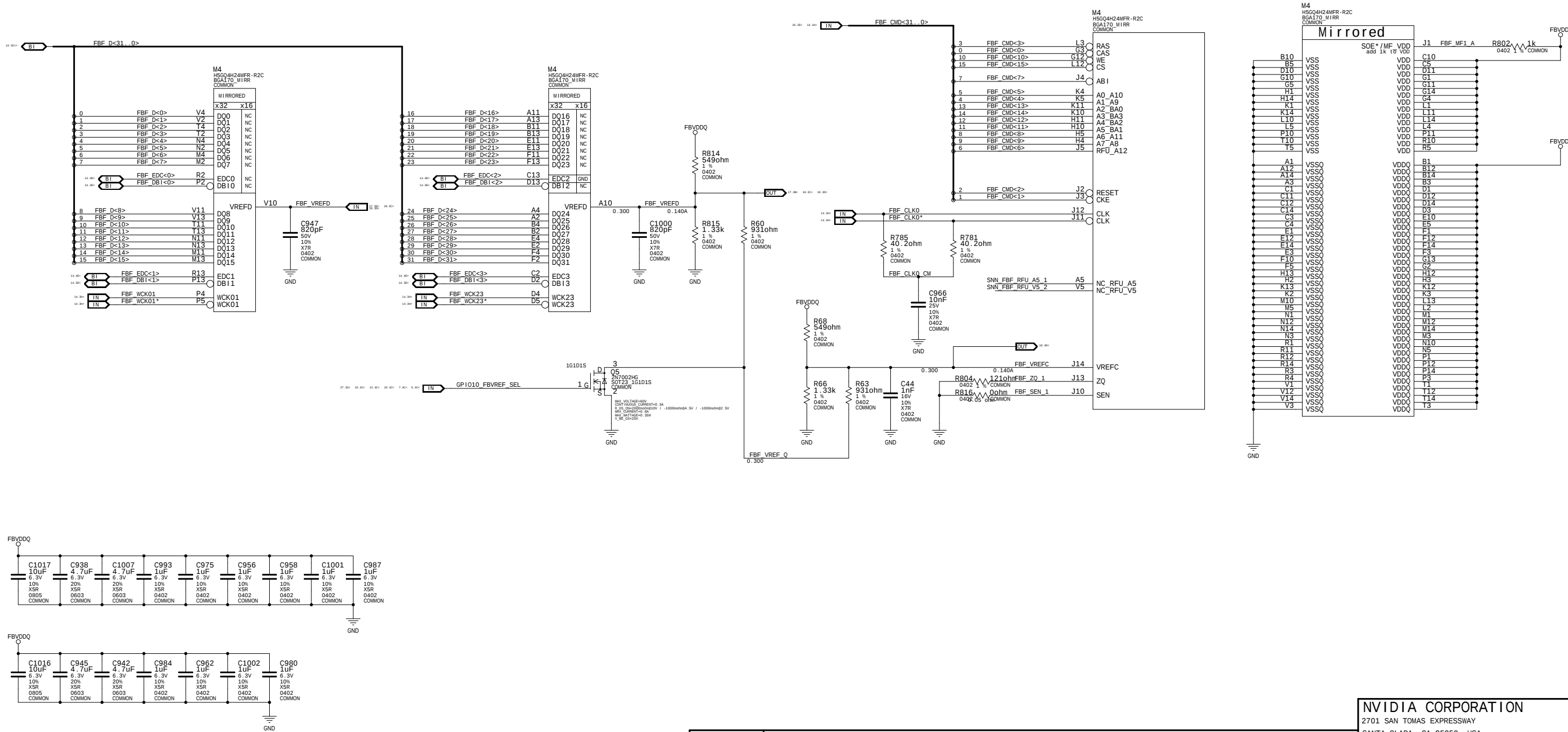
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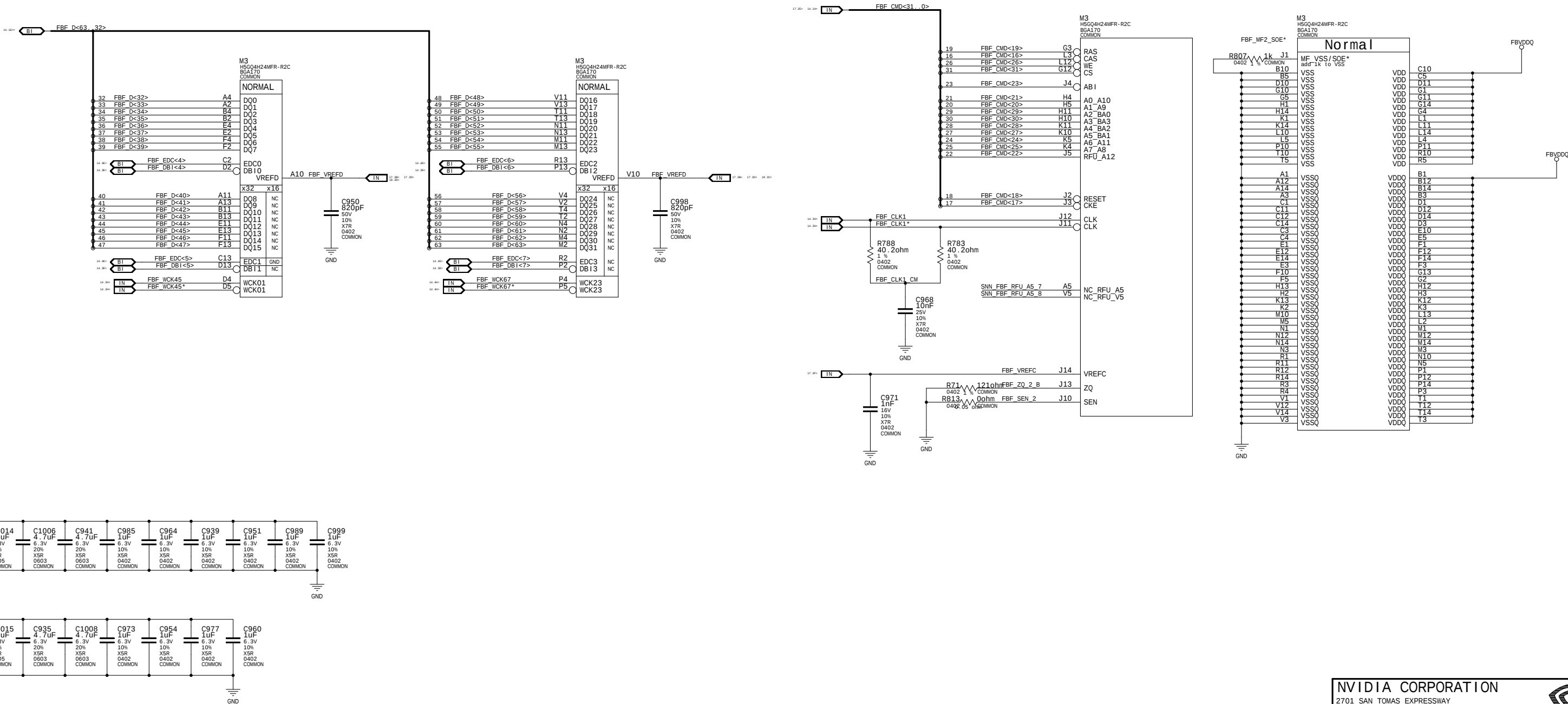
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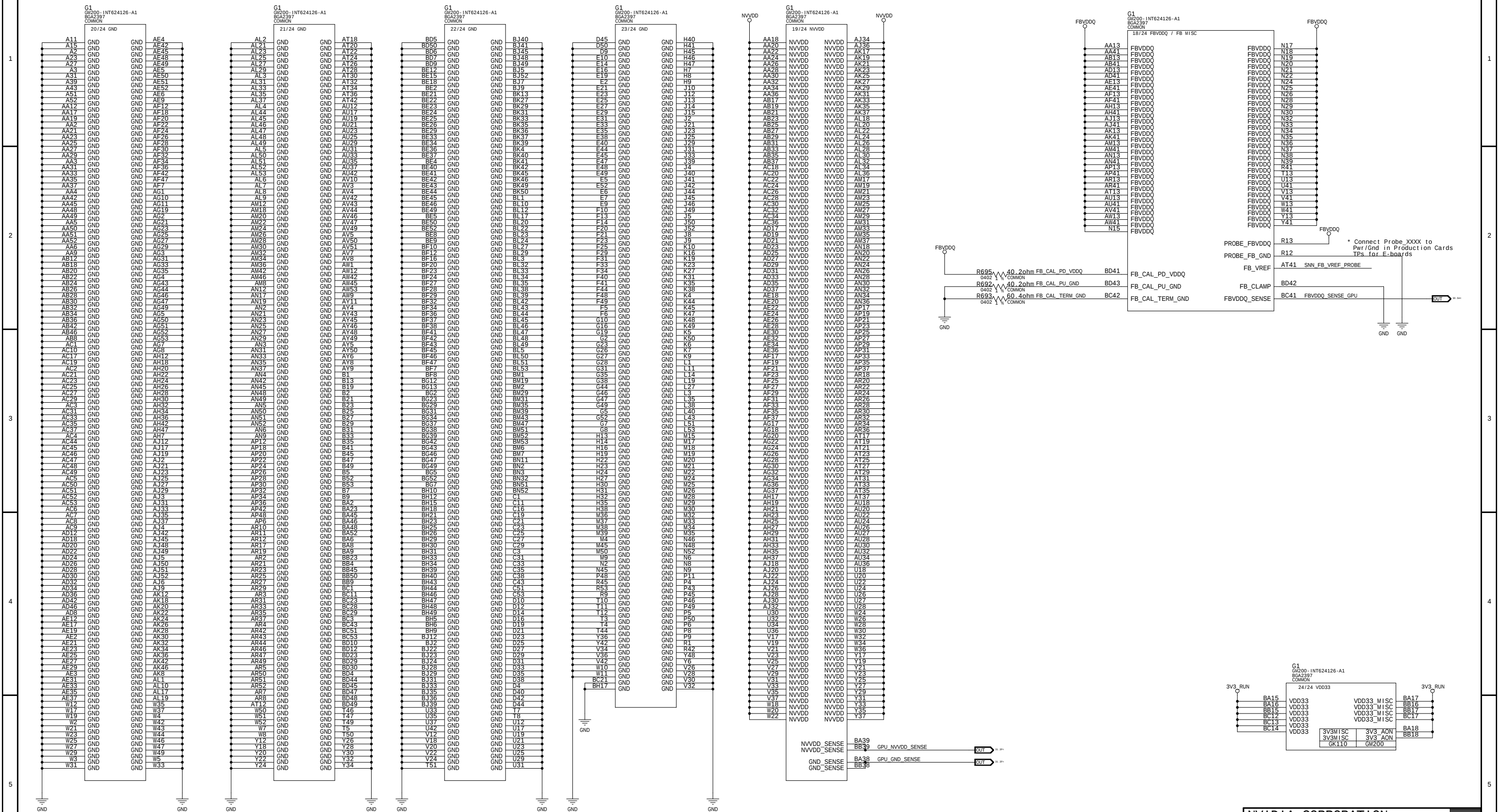
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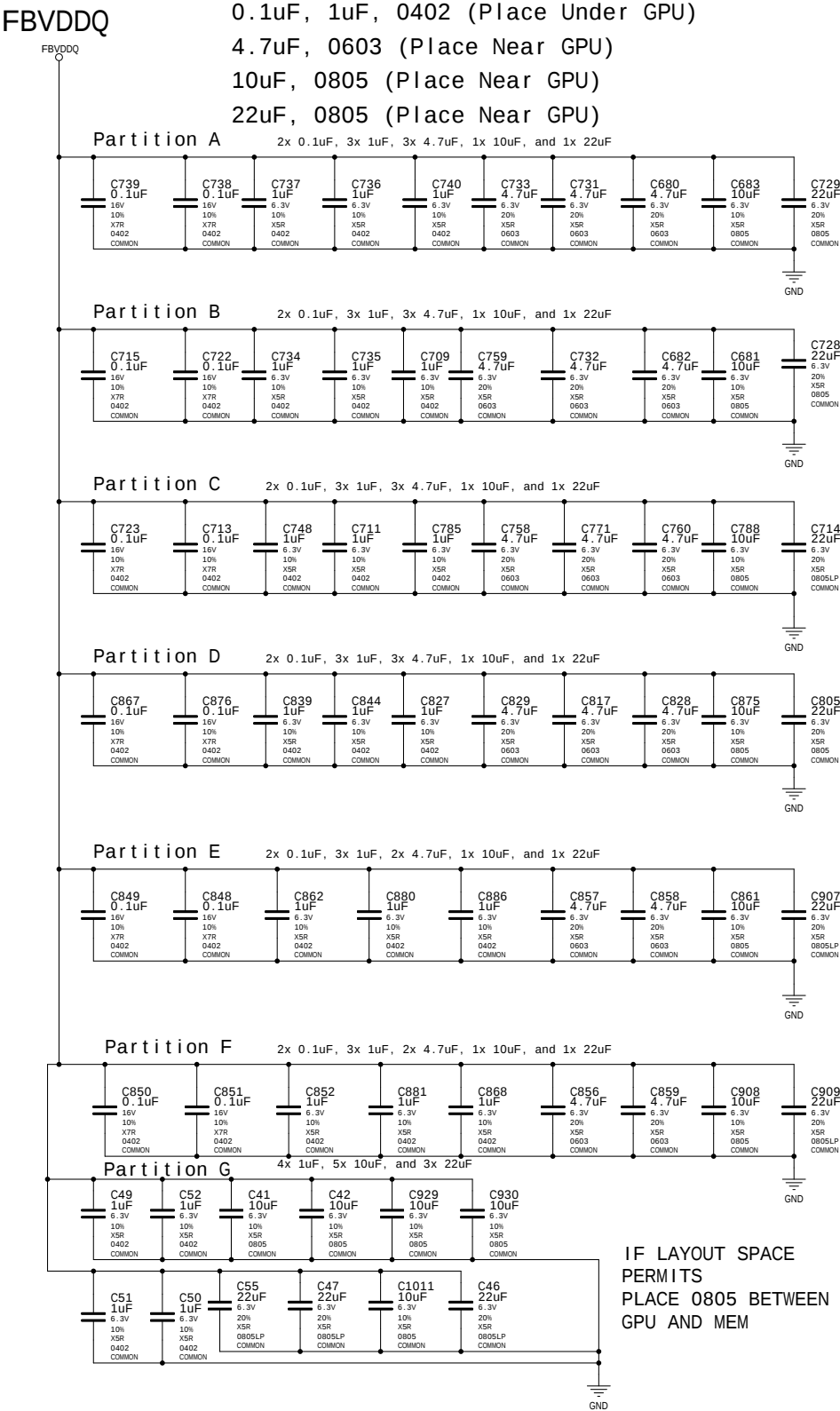
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Page19: GPU PWR and GND

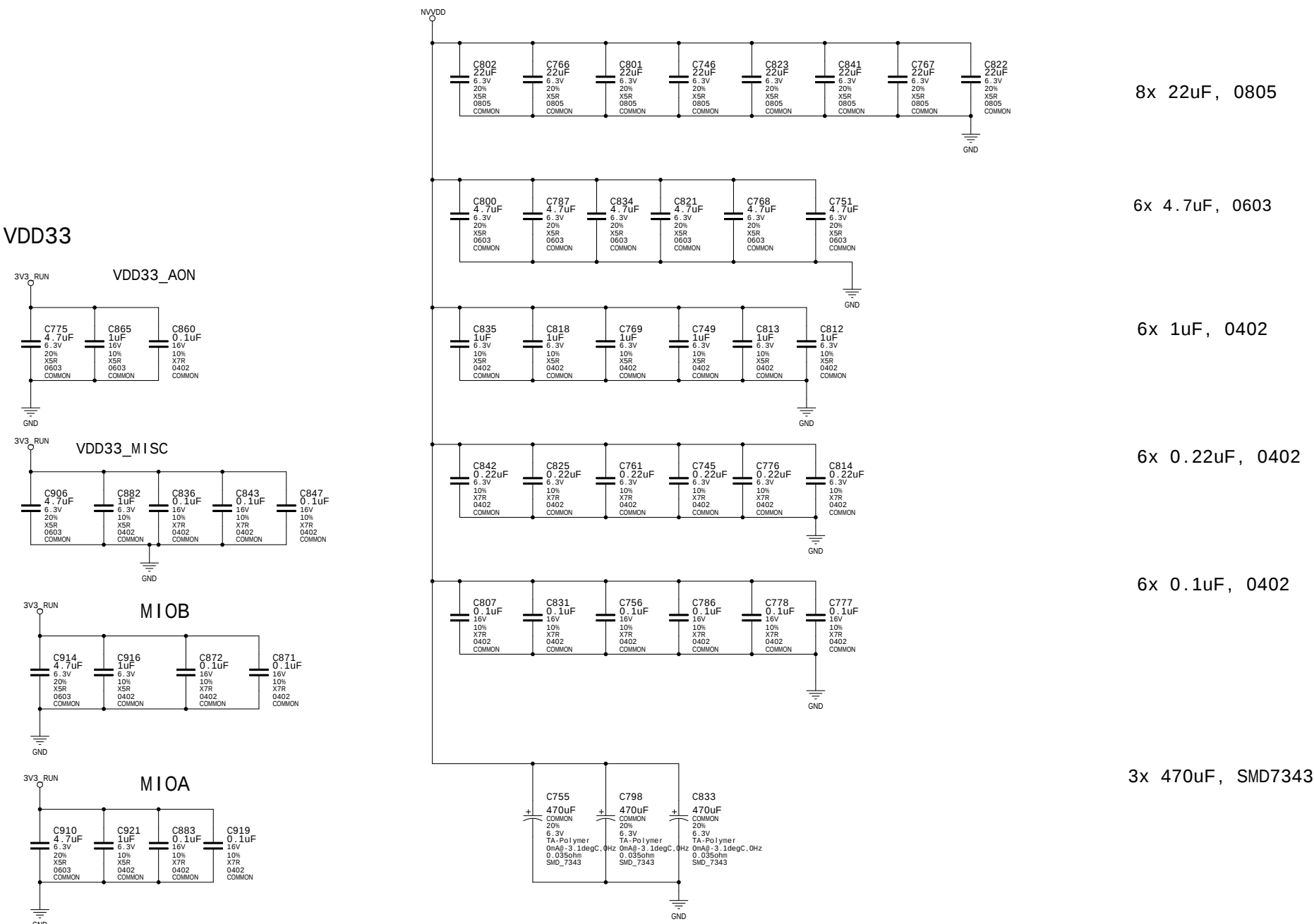


Based on GB3-X GDDR5 FBVDDQ Decap Guideline

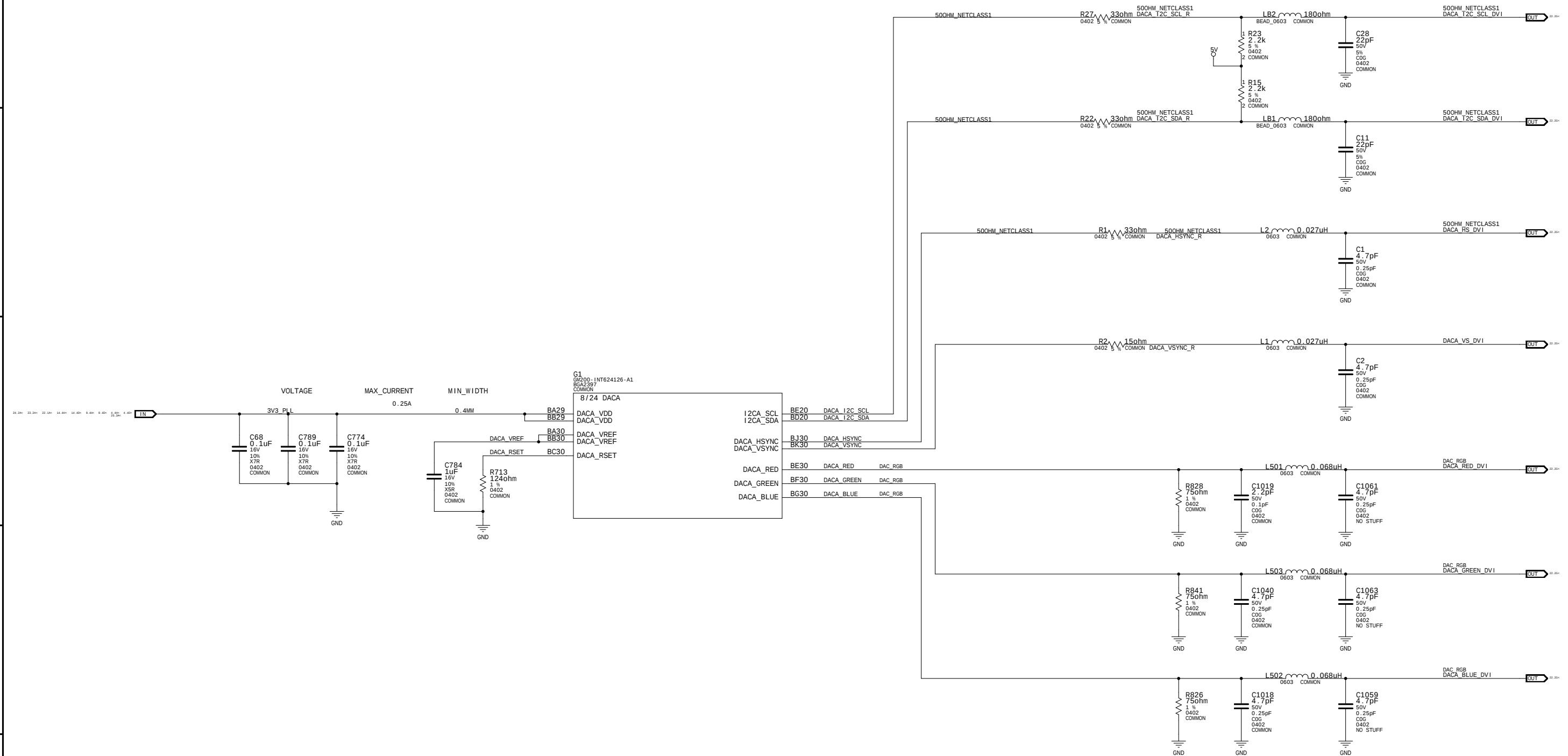


NVVDD Decoupling caps. Place under GPU.

NVVDD



Page21: DACA Interface



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PAGE DETAIL	DACA Interface

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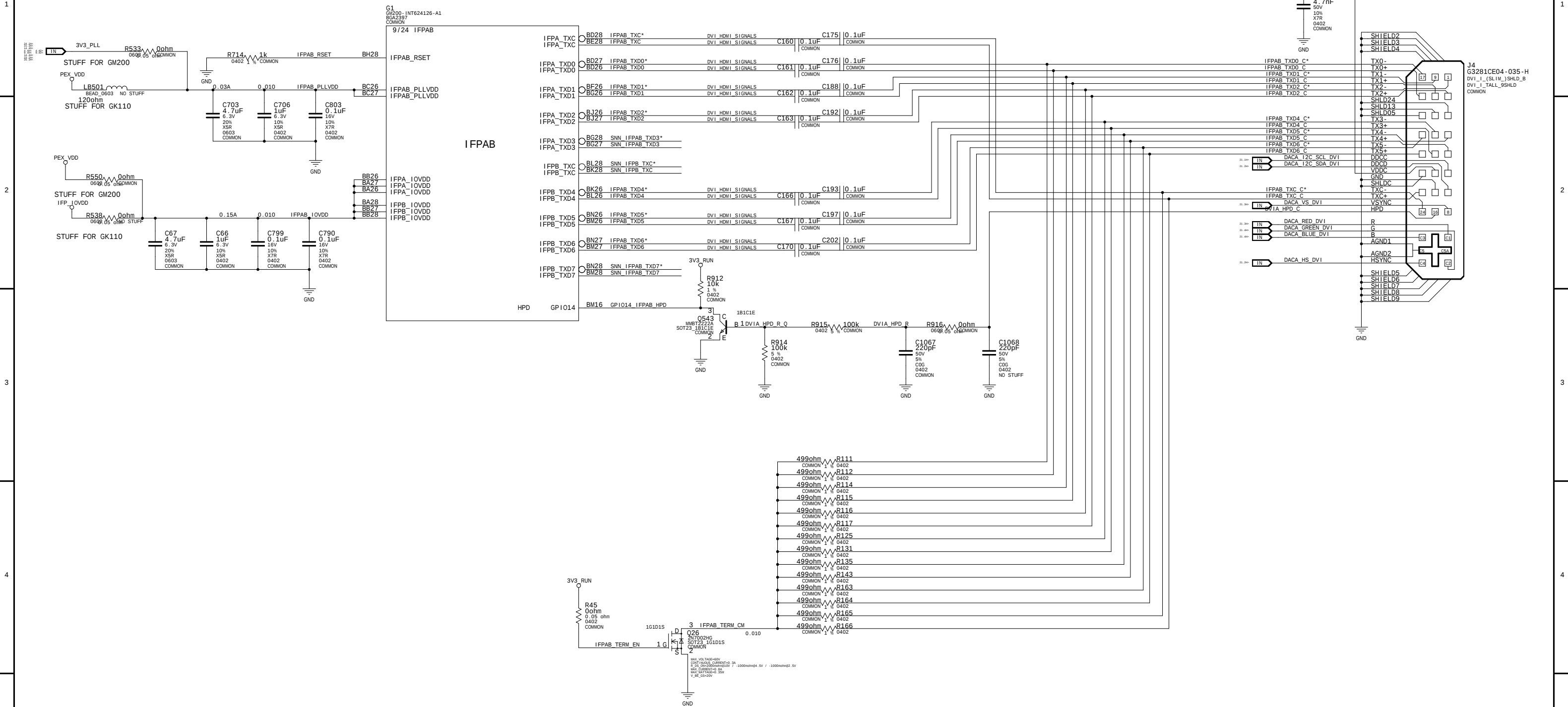
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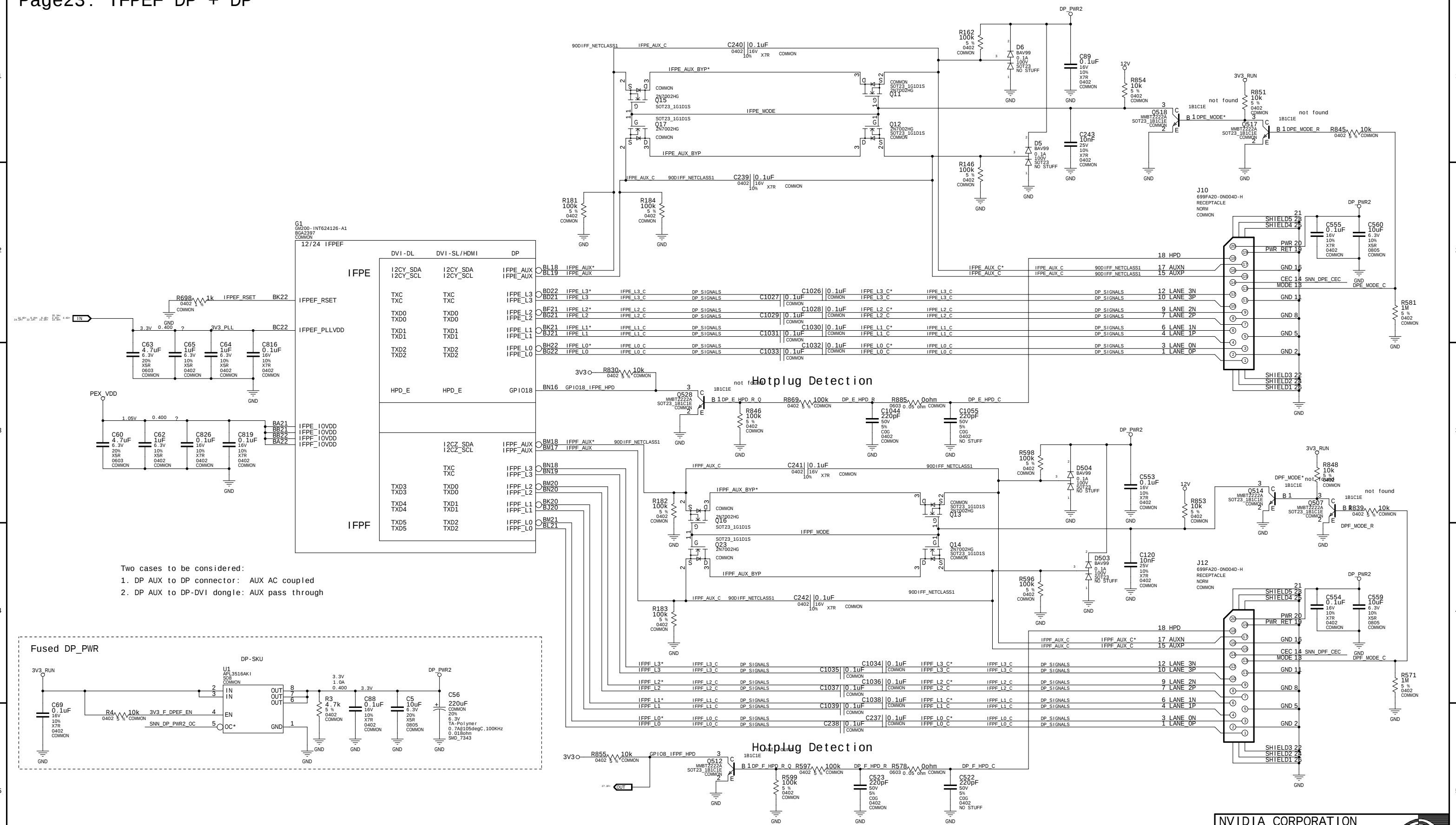
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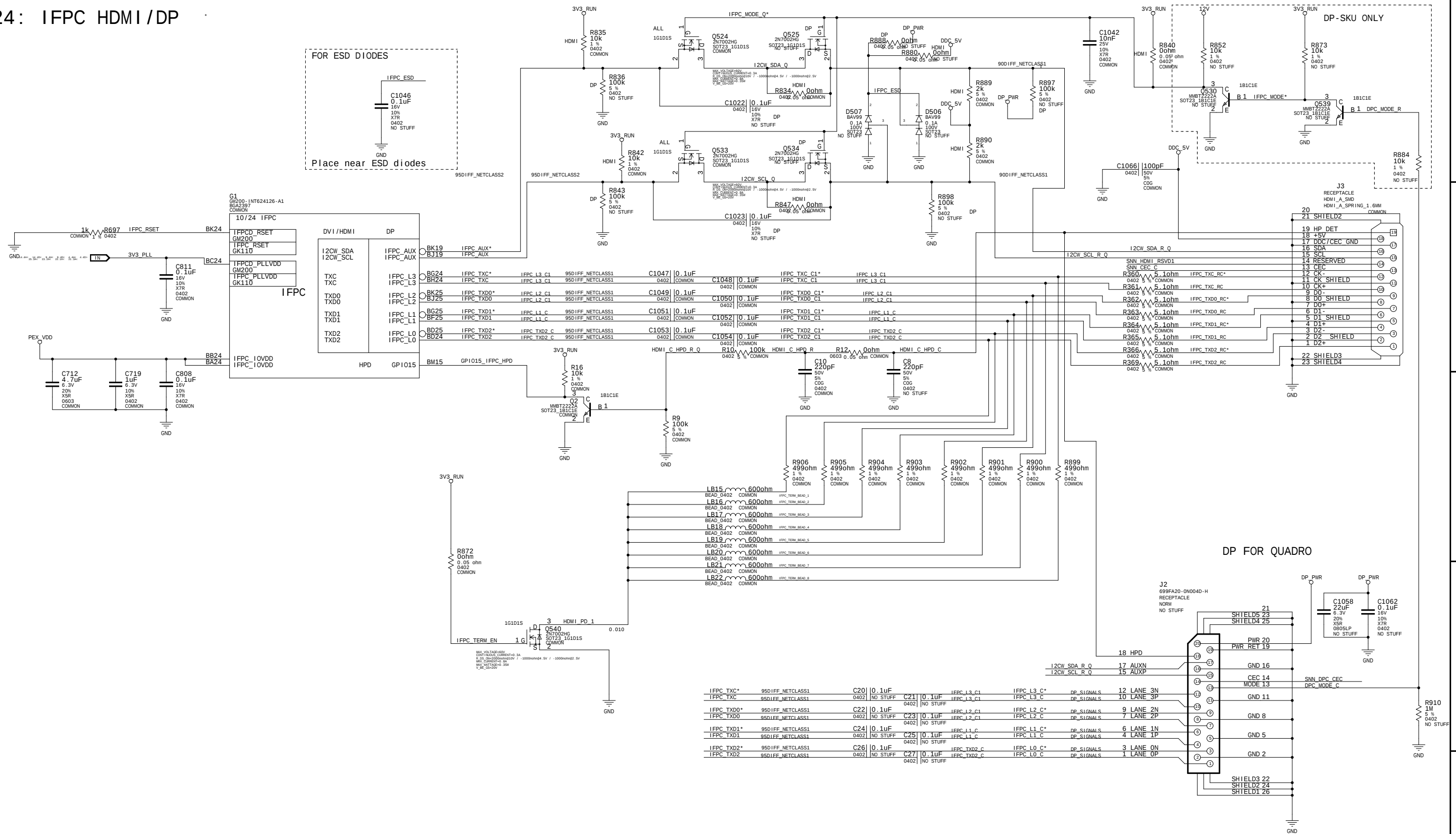
AC COUPLING NOT NEEDED for KEPLER
REPLACE WITH ZERO OHM RESISTORS FOR KEPLER SKUS





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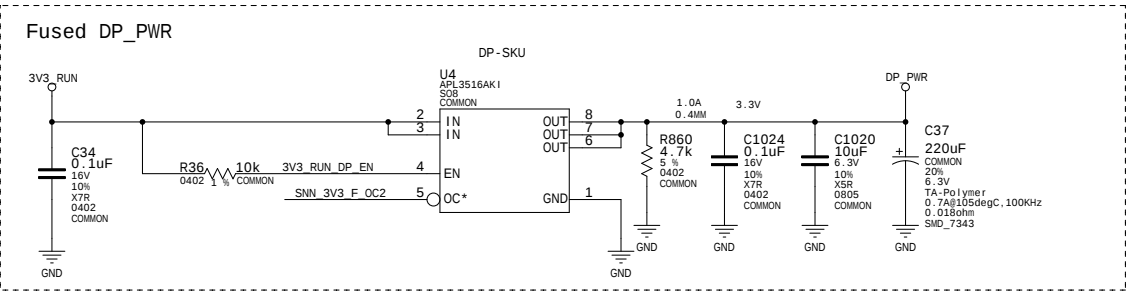
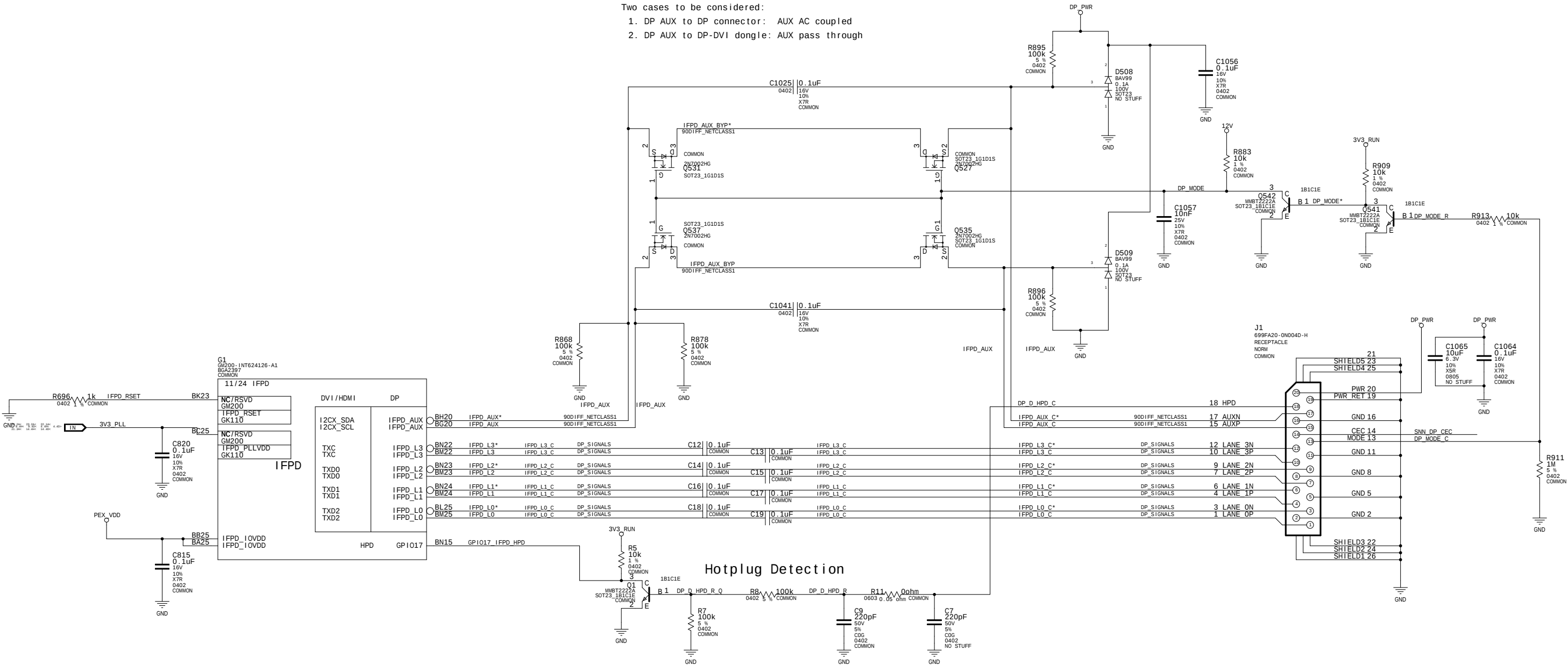
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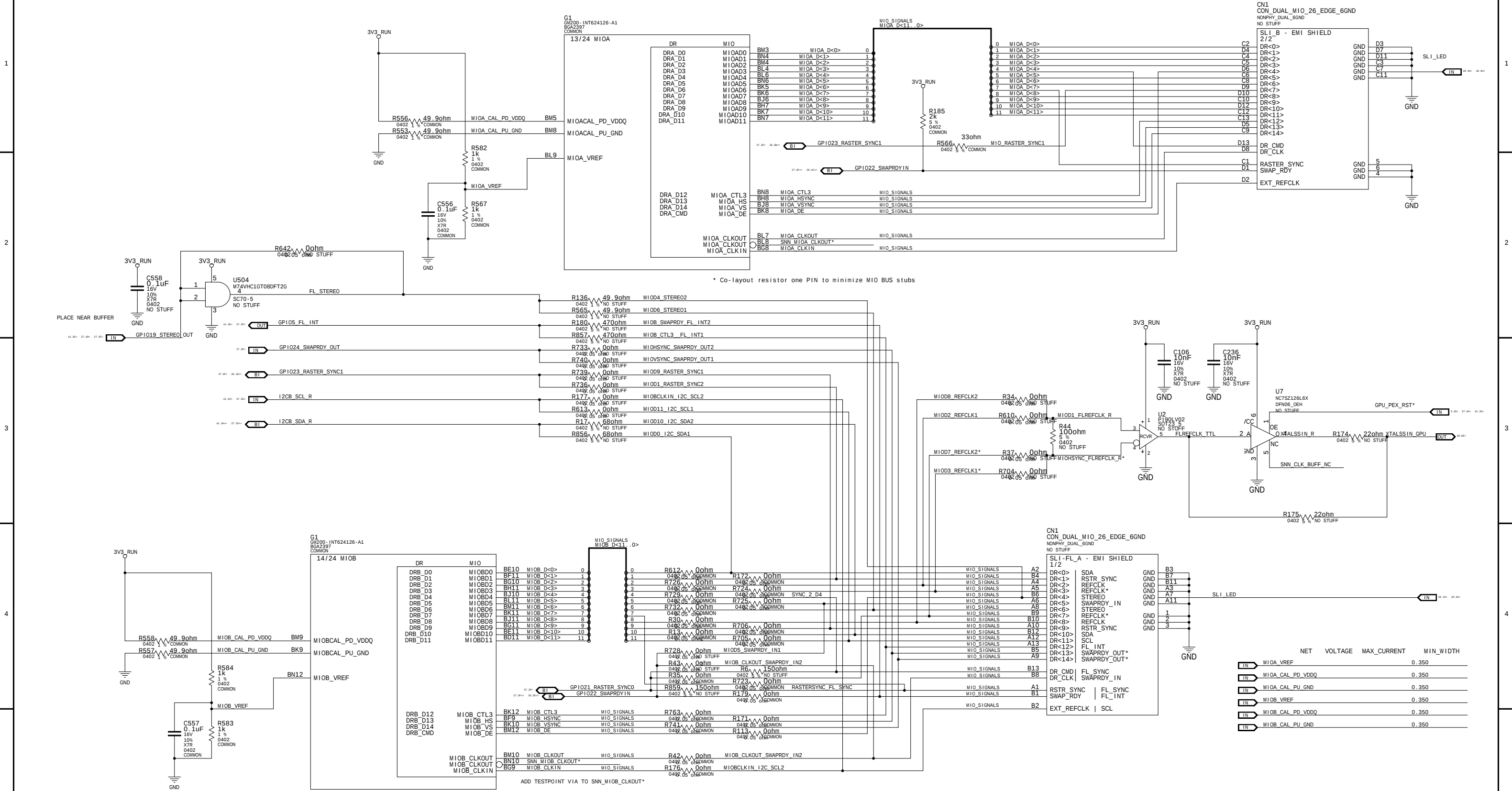
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1. DP AUX to DP connector: AUX AC coupled
 2. DP AUX to DP-DVI dongle: AUX pass through

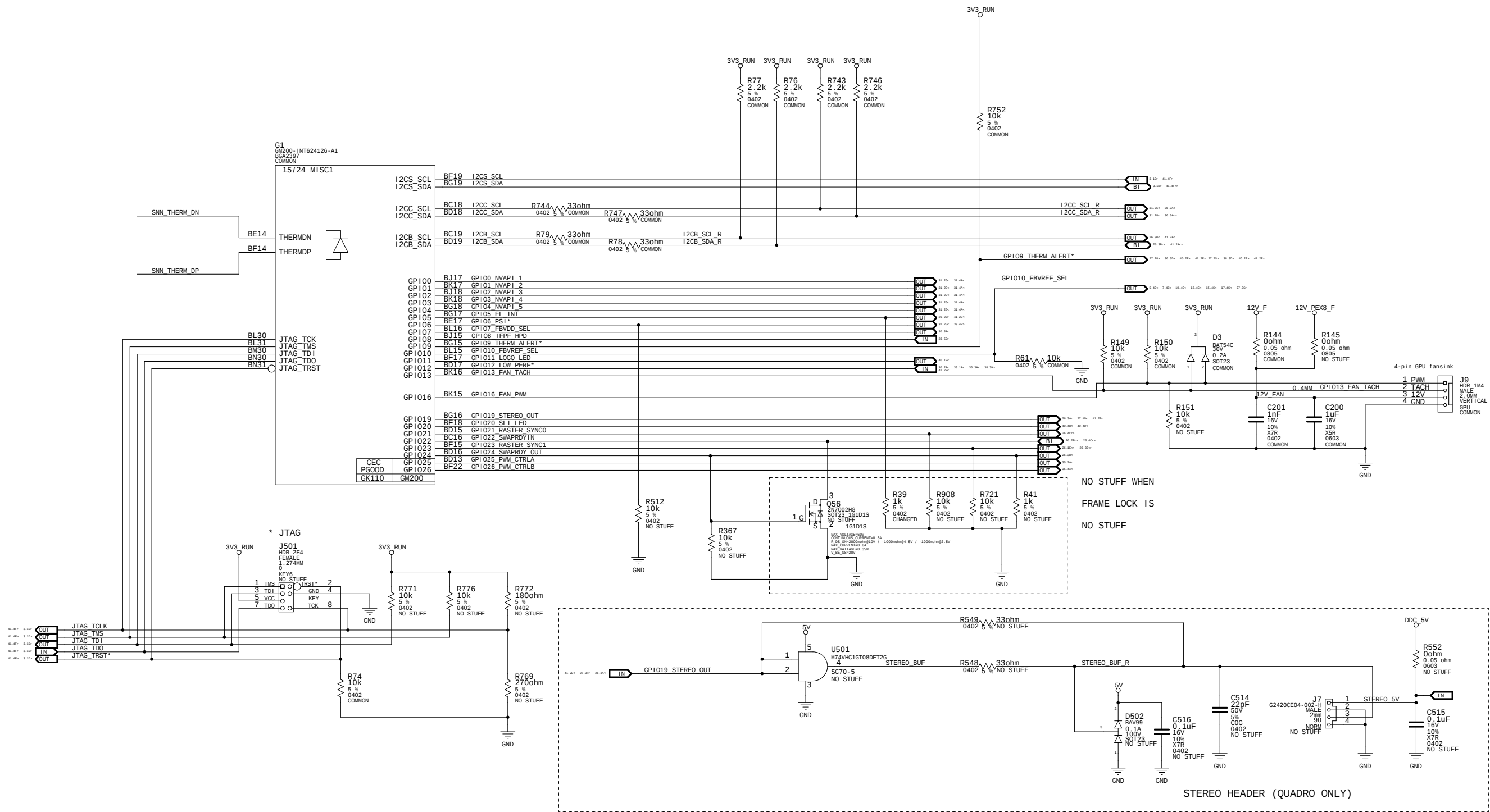


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Page26: MIOA/B and FRAMELOCK Interface

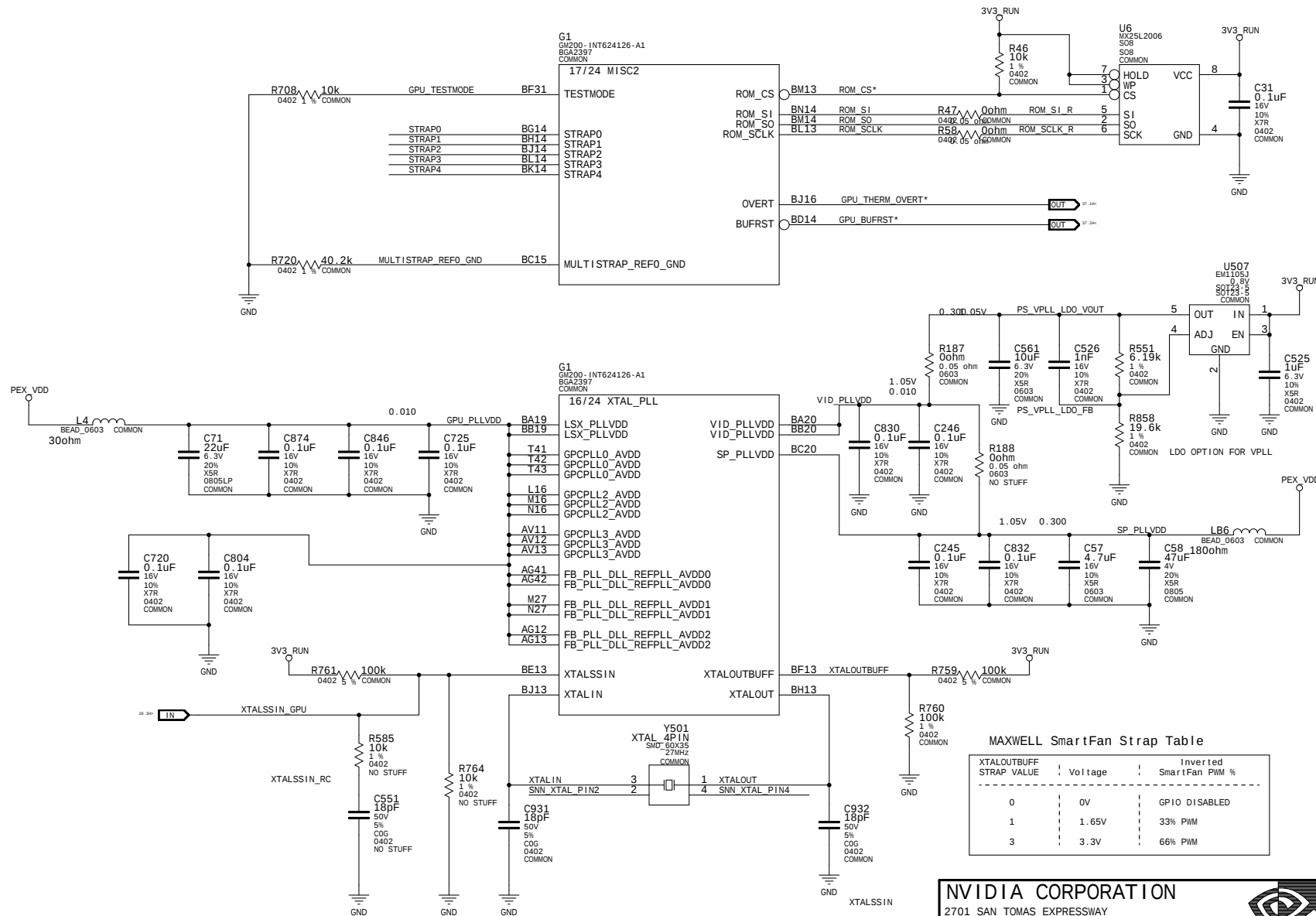
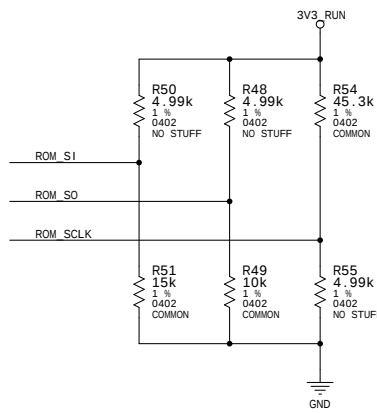
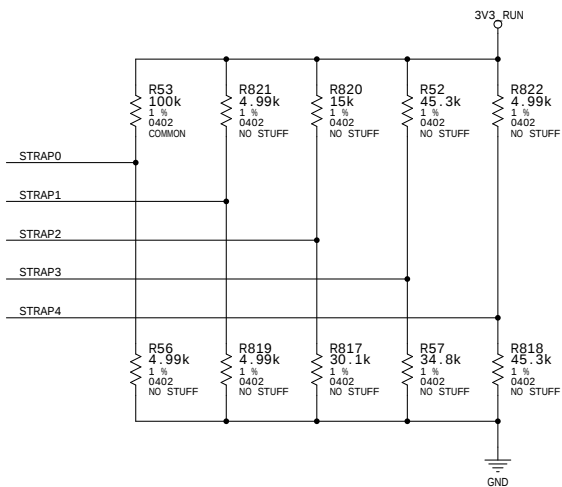




	GND	3V3
5k	0000	1000
10k	0001	1001
15k	0010	1010
20k	0011	1011
25k	0100	1100
30k	0101	1101
35k	0110	1110
45k	0111	1111

x32 DENSITY MODE STRAPS			
CFG[3:0]	Config	Width	Vendor
0000	Reserved		
0001	128Mx32	384-bit	Elpida
0010	128Mx32	384-bit	Hynix
0011	128Mx32	384-bit	Samsung
0100	64Mx32	384-bit	Hynix B
0101	64Mx32	384-bit	Elpida
0110	64Mx32	384-bit	Hynix
0111	64Mx32	384-bit	Samsung
1000	Reserved		
1001	128Mx32	320-bit	Elpida
1010	128Mx32	320-bit	Hynix
1011	128Mx32	320-bit	Samsung
1100	64Mx32	320-bit	Hynix B
1101	64Mx32	320-bit	Elpida
1110	64Mx32	320-bit	Hynix
1111	64Mx32	320-bit	Samsung

x16 DENSITY MODE STRAPS			
CFG[3:0]	Config	Width	Vendor
0000	Reserved		
0001	256Mx16	384-bit	Elpida
0010	256Mx16	384-bit	Hynix
0011	256Mx16	384-bit	Samsung
0100	128Mx16	384-bit	Hynix B
0101	128Mx16	384-bit	Elpida
0110	128Mx16	384-bit	Hynix
0111	128Mx16	384-bit	Samsung
1000	Reserved		
1001	256Mx16	320-bit	Elpida
1010	256Mx16	320-bit	Hynix
1011	256Mx16	320-bit	Samsung
1100	128Mx16	320-bit	Hynix B
1101	128Mx16	320-bit	Elpida
1110	128Mx16	320-bit	Hynix
1111	128Mx16	320-bit	Samsung



MAXWELL SmartFan Strap Table		
XTALOUTBUFF STRAP VALUE	Voltage	Inverted SmartFan PWM %
0	0V	GPIO DISABLED
1	1.65V	33% PWM
3	3.3V	66% PWM

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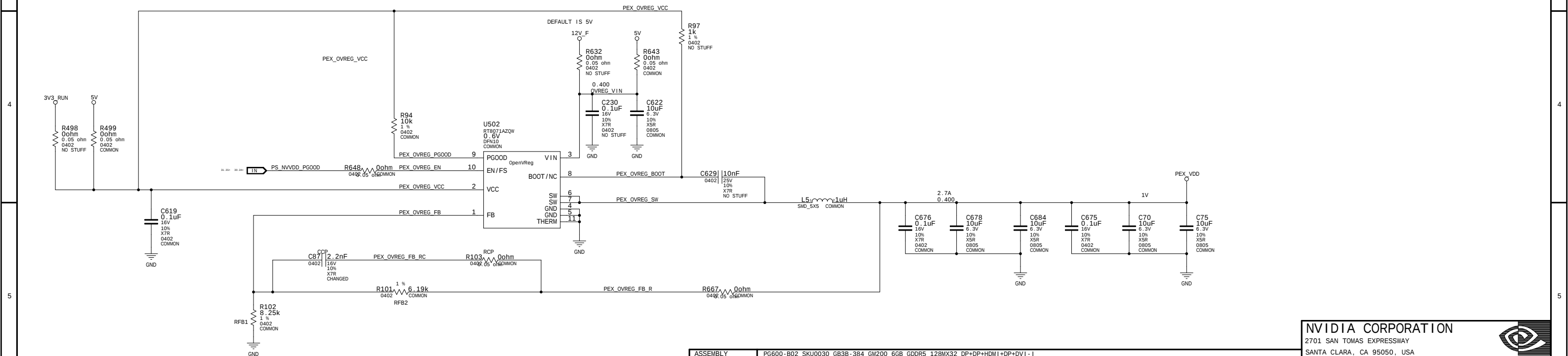
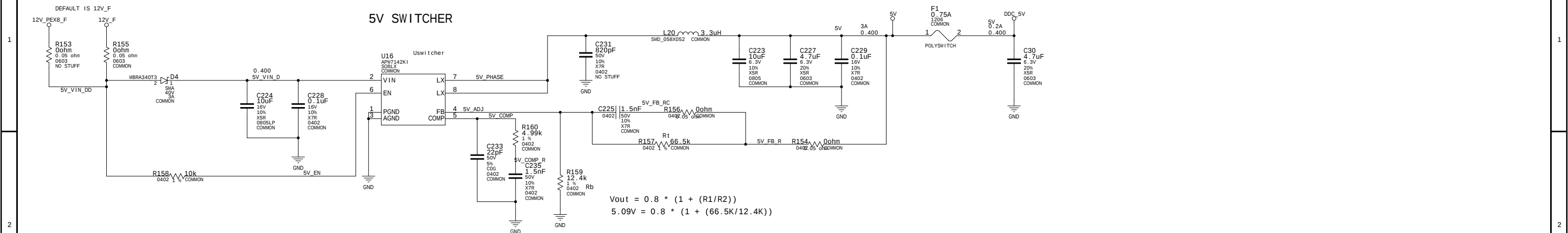
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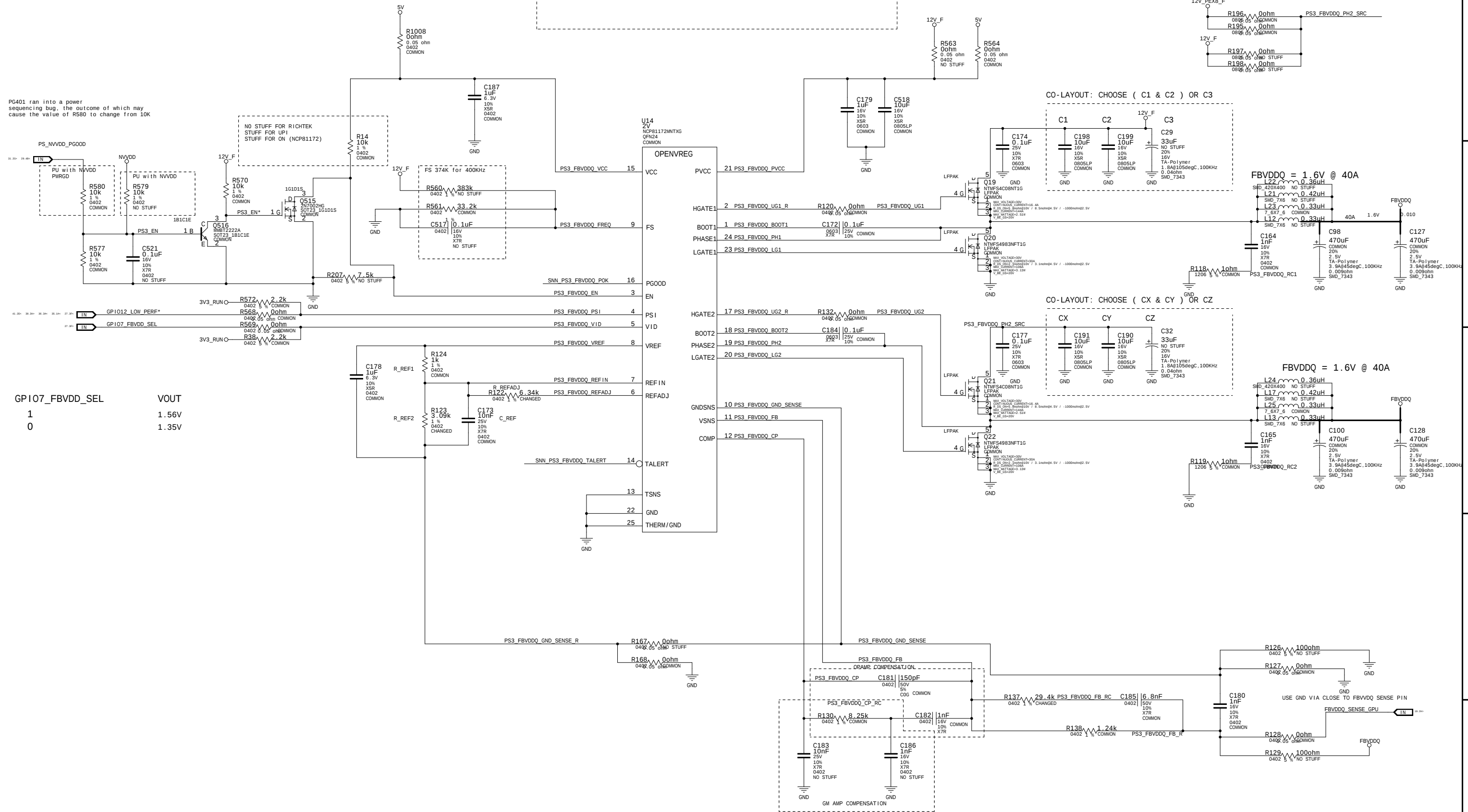
Page29: PS: 5V, PEX_VDD



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Page30: PS: FBVDDQ

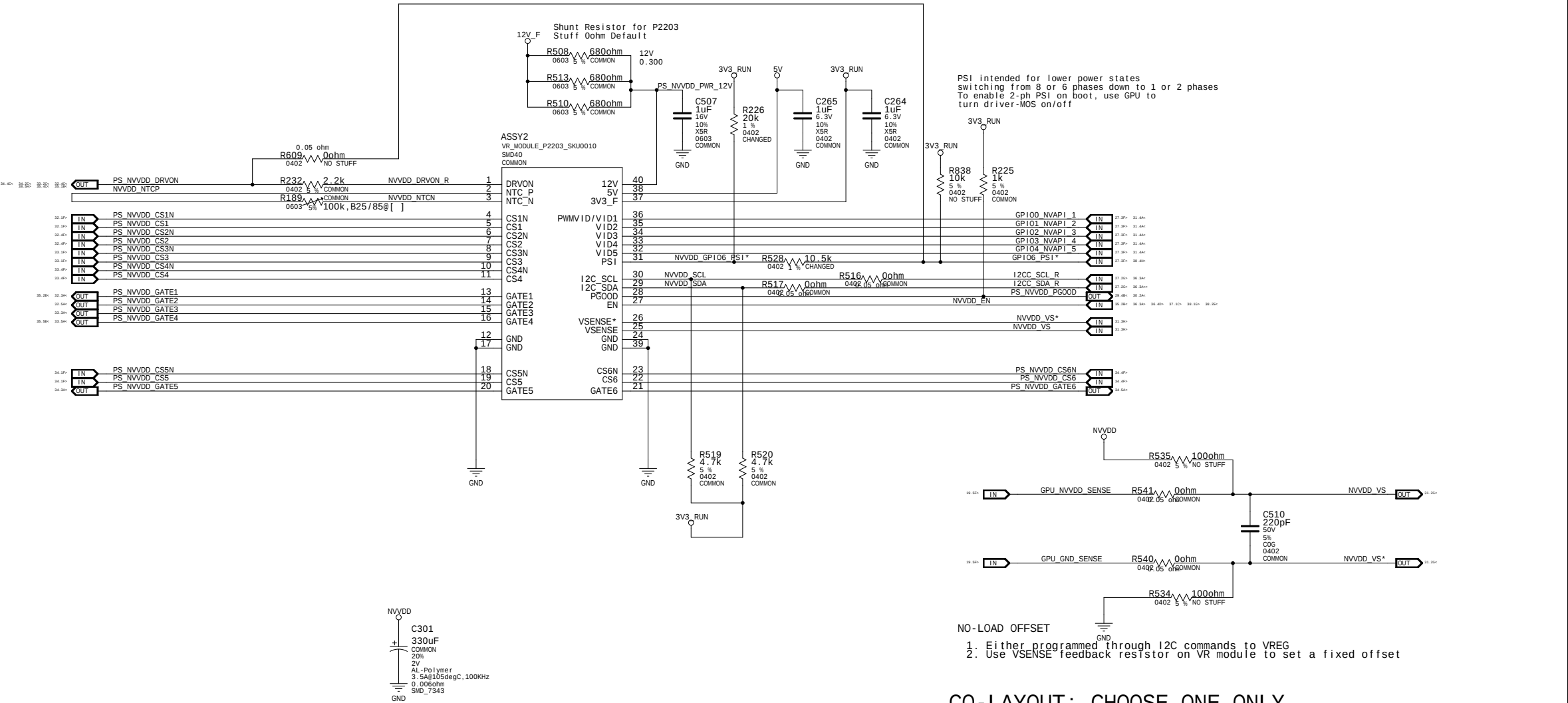


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PCB REV	PG600-B02	PAGE	30 OF 41
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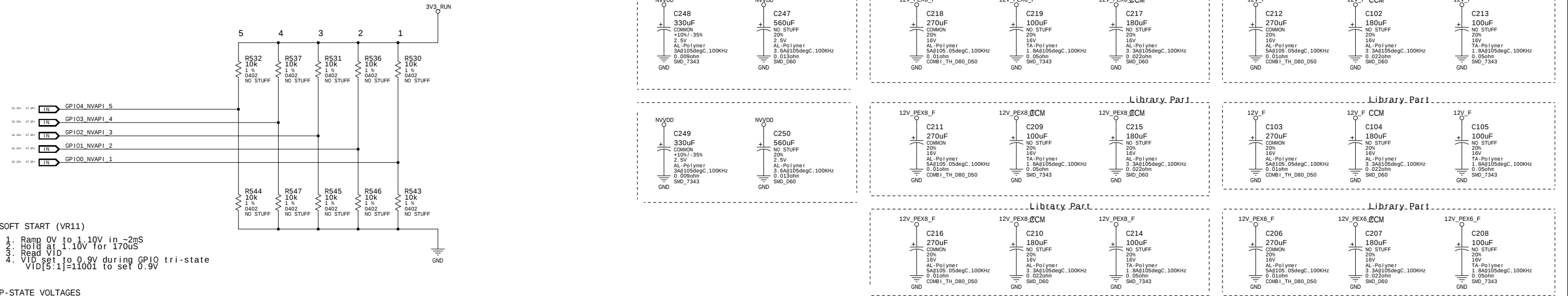
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VID Table

GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	VOUT
VID_5	VID_4	VID_3	VID_2	VID_1	
0	0	0	0	0	1.2125V
0	0	0	0	1	1.2000V
0	0	0	1	0	1.1875V
0	0	0	1	1	1.1750V
0	0	1	0	0	1.1625V
0	0	1	0	1	1.1500V
0	0	1	1	0	1.1375V
0	0	1	1	1	1.1250V
0	1	0	0	0	1.1125V
0	1	0	0	1	1.1000V
0	1	0	1	0	1.0875V
0	1	0	1	1	1.0750V
0	1	1	0	0	1.0625V
0	1	1	0	1	1.0500V
0	1	1	1	0	1.0375V
0	1	1	1	1	1.0250V
1	0	0	0	0	1.0125V
1	0	0	0	1	1.0000V
1	0	0	1	0	0.9875V
1	0	0	1	1	0.9750V
1	0	1	0	0	0.9625V
1	0	1	0	1	0.9500V
1	0	1	1	0	0.9375V
1	0	1	1	1	0.9250V
1	1	0	0	0	0.9125V
1	1	0	0	1	0.9000V
1	1	0	1	0	0.8875V
1	1	0	1	1	0.8750V
1	1	1	0	0	0.8625V
1	1	1	0	1	0.8500V
1	1	1	1	0	0.8375V
1	1	1	1	1	0.8250V



CO-LAYOUT: CHOOSE ONE ONLY



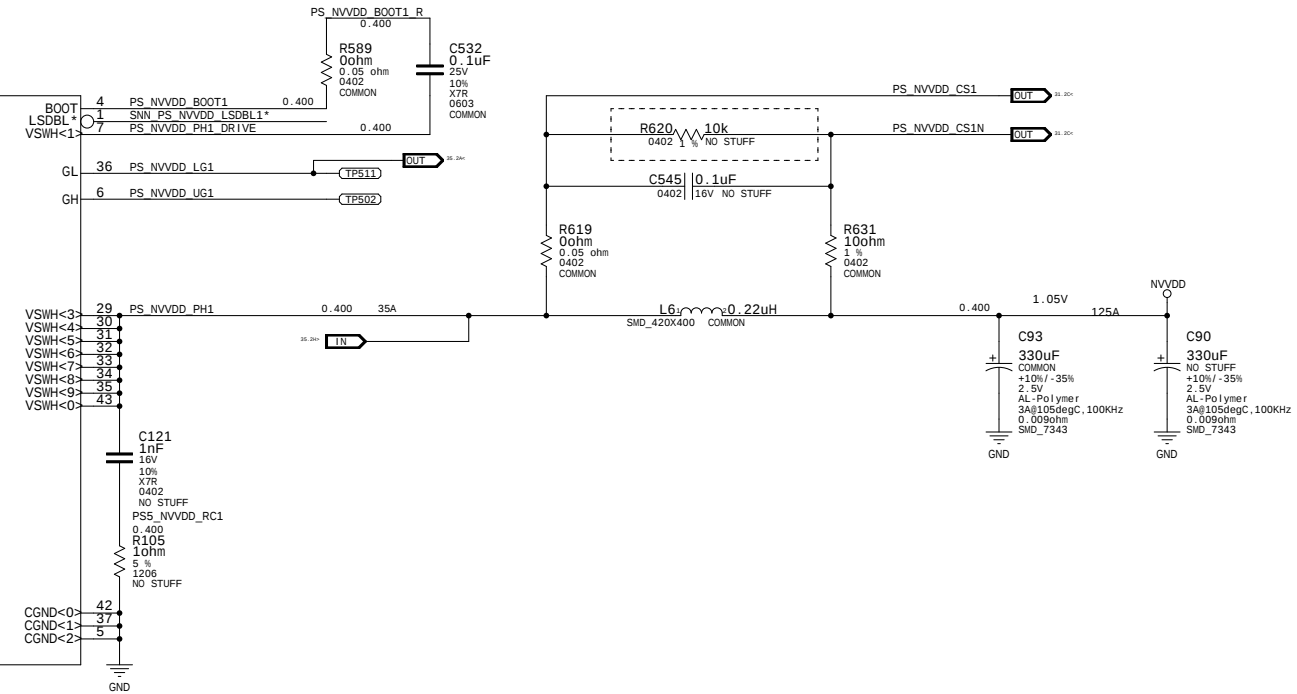
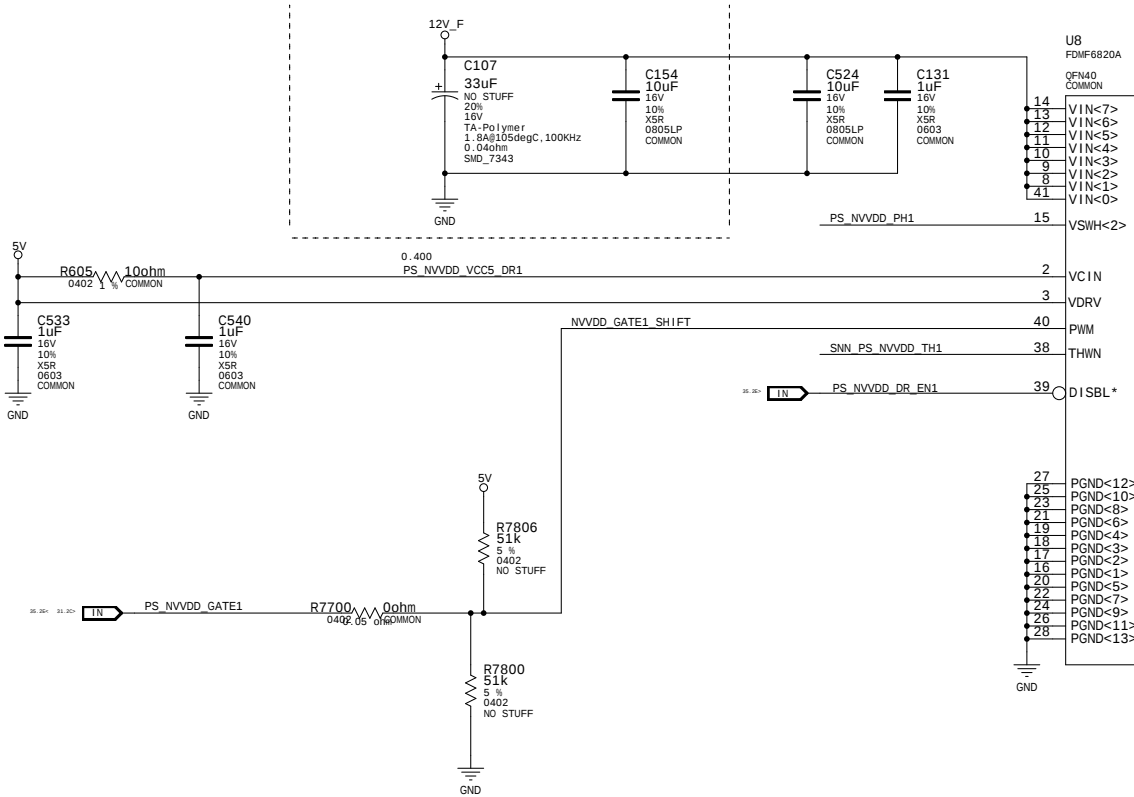
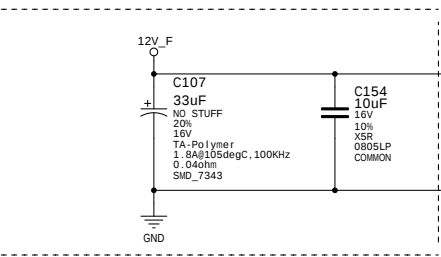
SOFT START (VR11)

1. Ramp 0V to 1.10V in ~2mS
2. Hold at 1.10V for 170uS
3. Read Vid
4. VID set to 0.9V during GPIO tri-state
VID[5:1]=11001 to set 0.9V

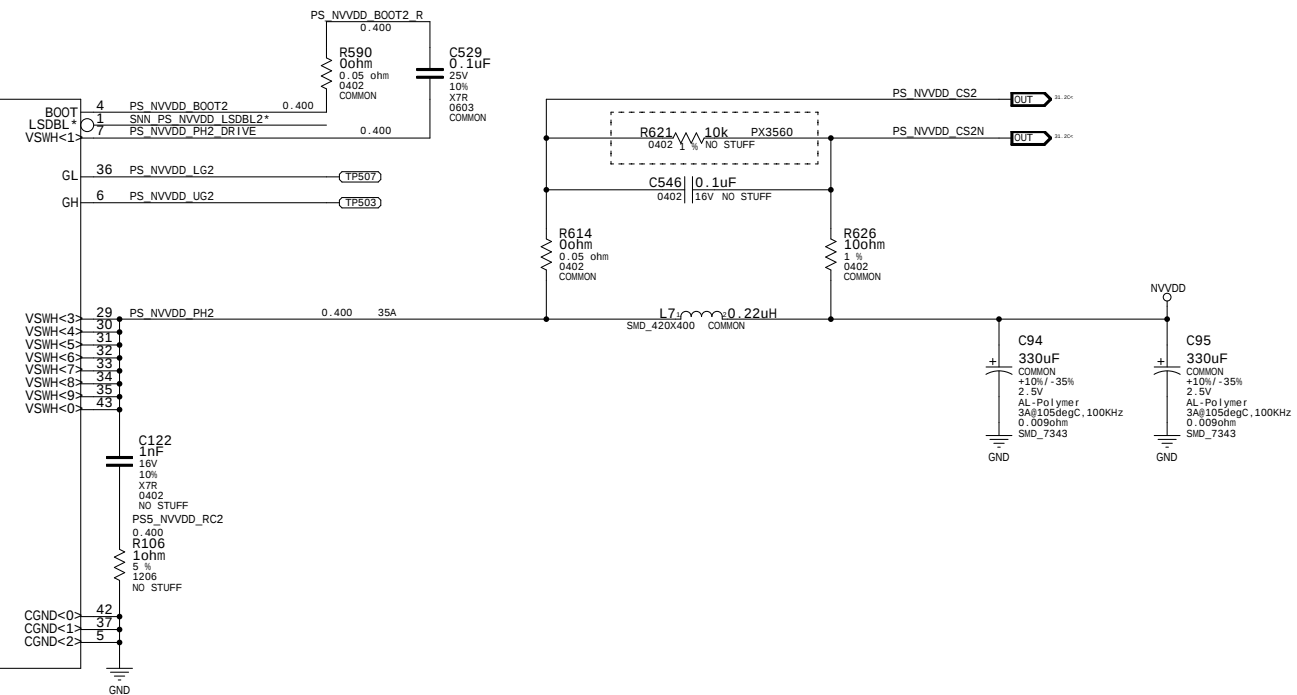
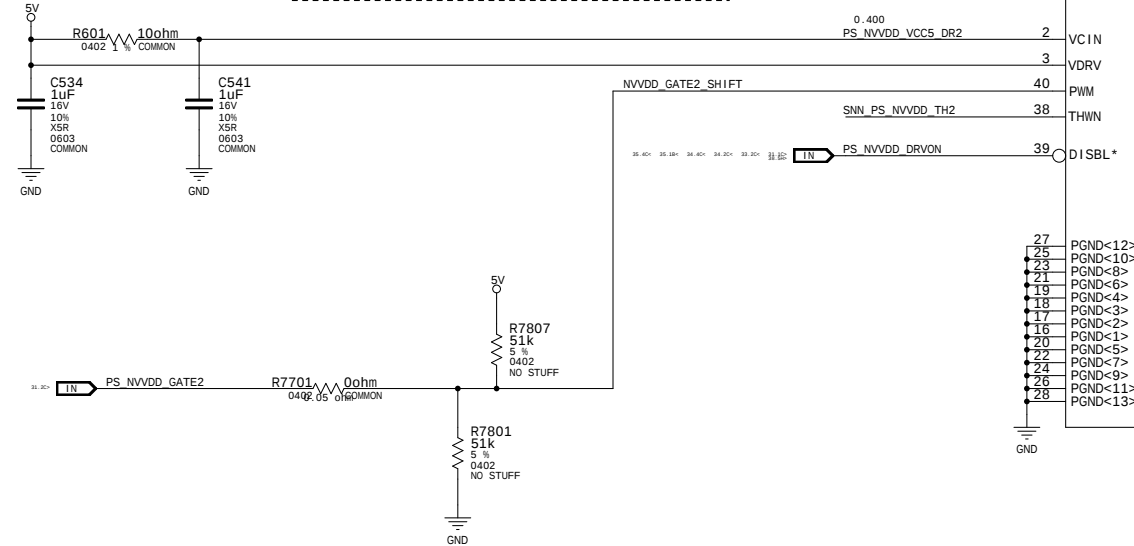
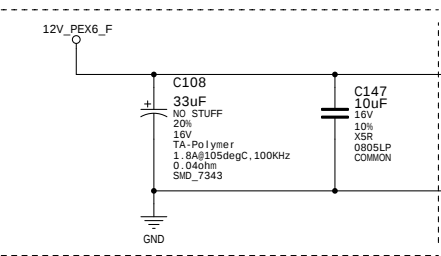
P-STATE VOLTAGES

1. P0 at 1.05V to 1.15V (depending on VB)
2. P8/P12 at 0.80V

CO-LAYOUT: STUFF ONLY ONE



CO-LAYOUT: STUFF ONLY ONE



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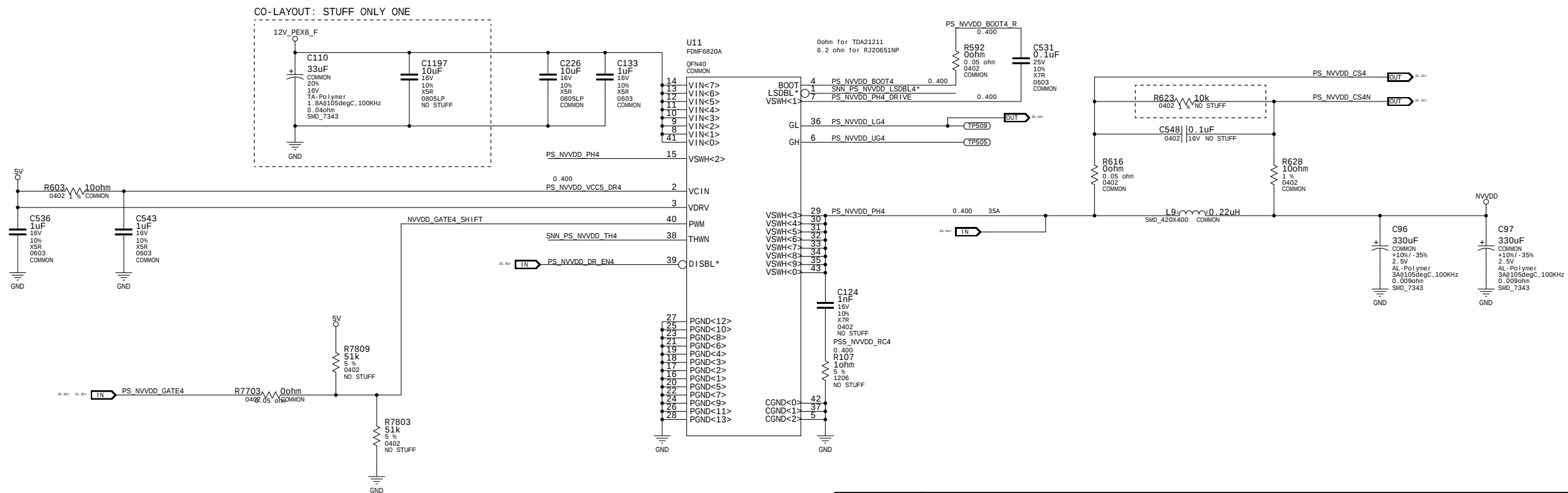
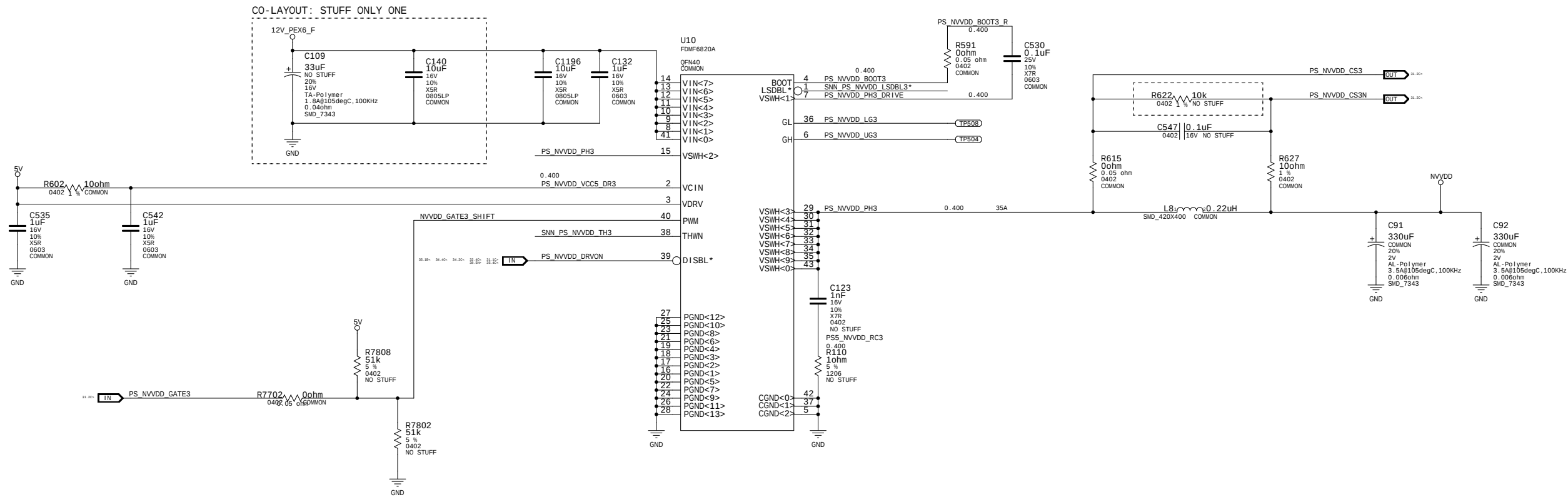
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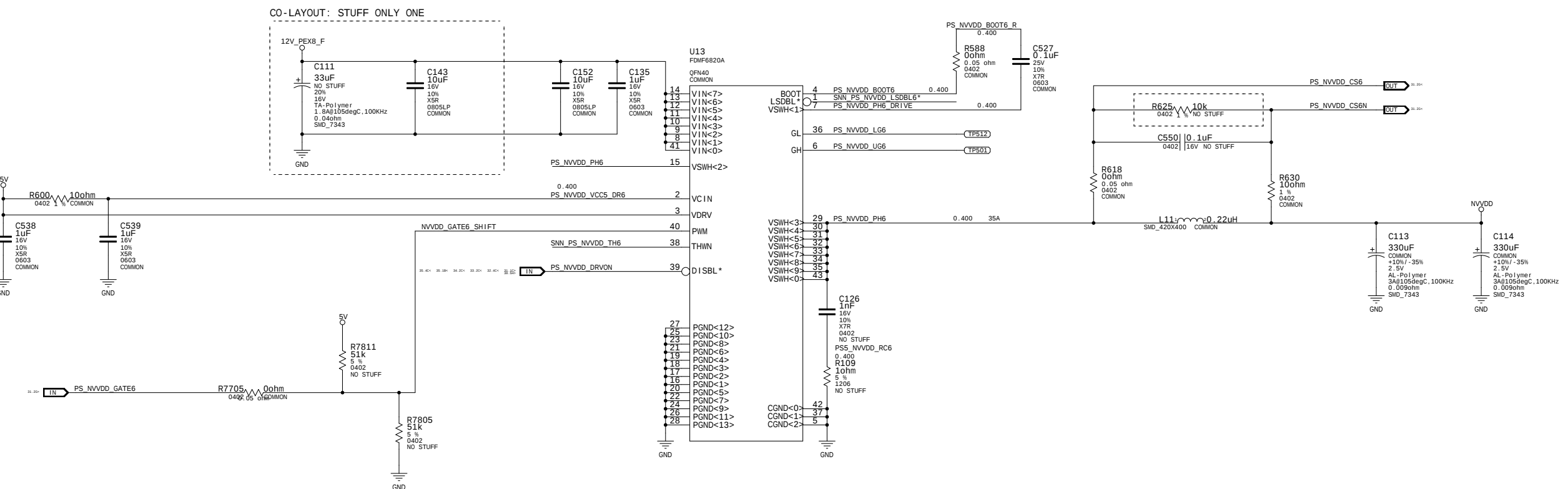
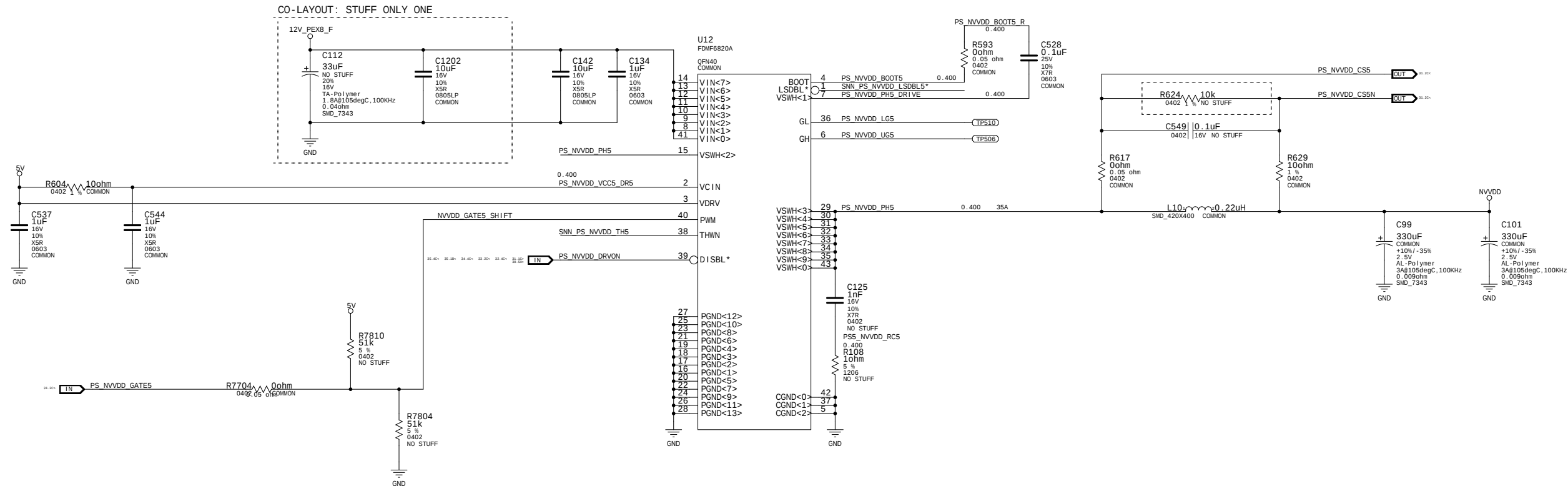


ASSEMBLY	PG600-B02 SKU0030 GB3B-384 GM200 6GB GDDR5 128MX32 DP+DP+HDMI+DP+DV1-I
PAGE DETAIL	PS: NVVDD Phase 1,2

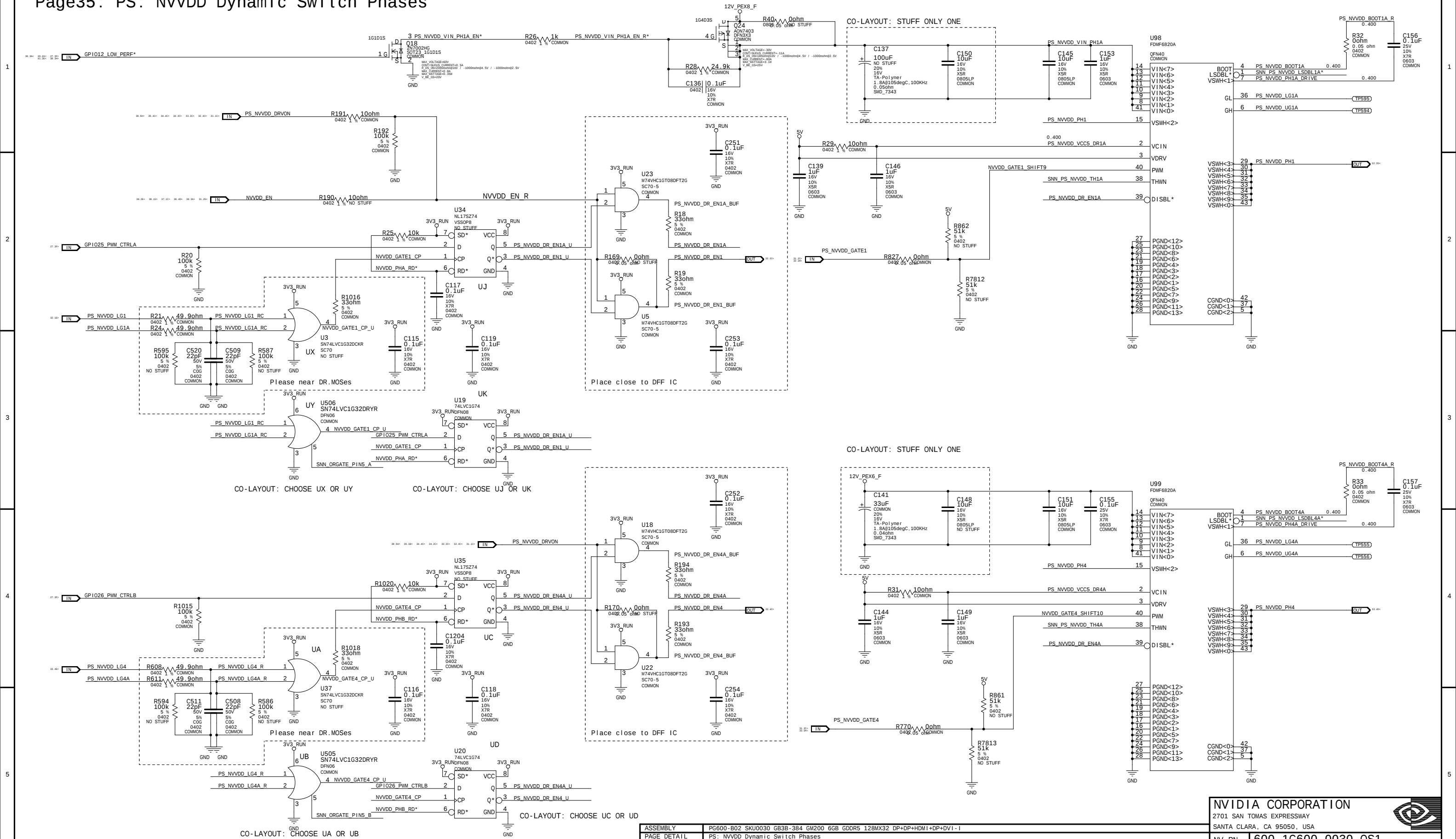
NV_PN	600-1G600-0030-QS1
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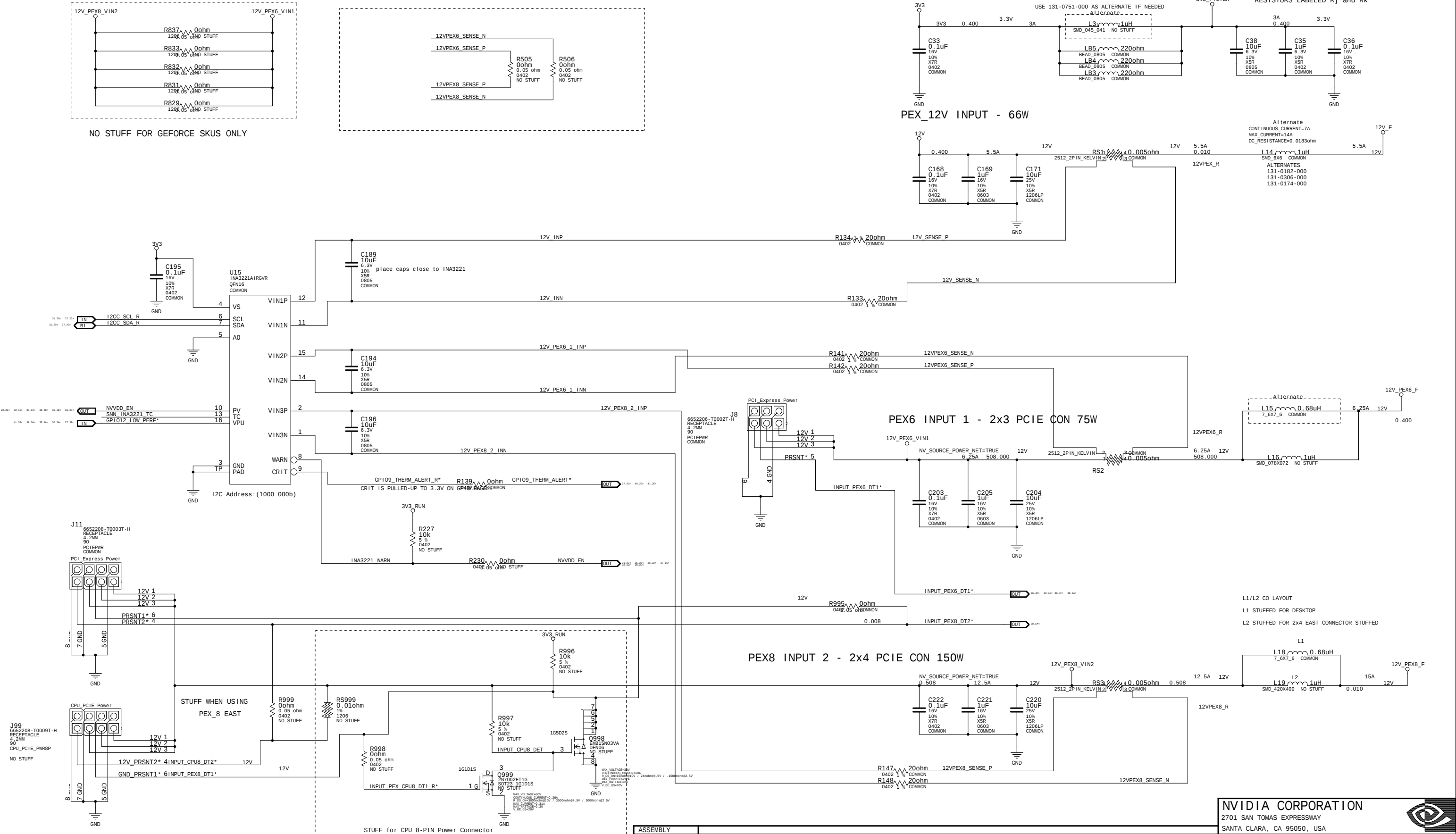
Page35: PS: NVVDD Dynamic Switch Phases



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Page36: PS: Inputs, Filtering, and Monitoring

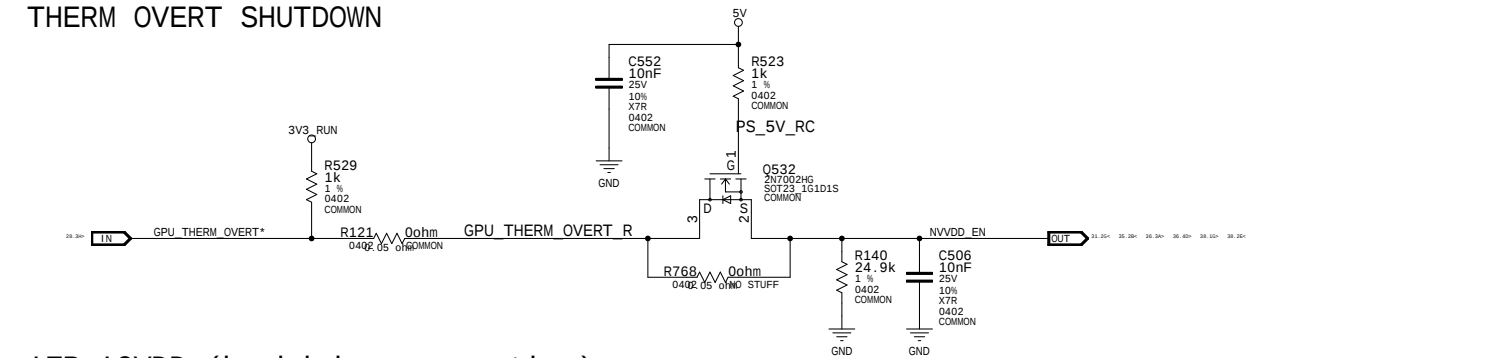


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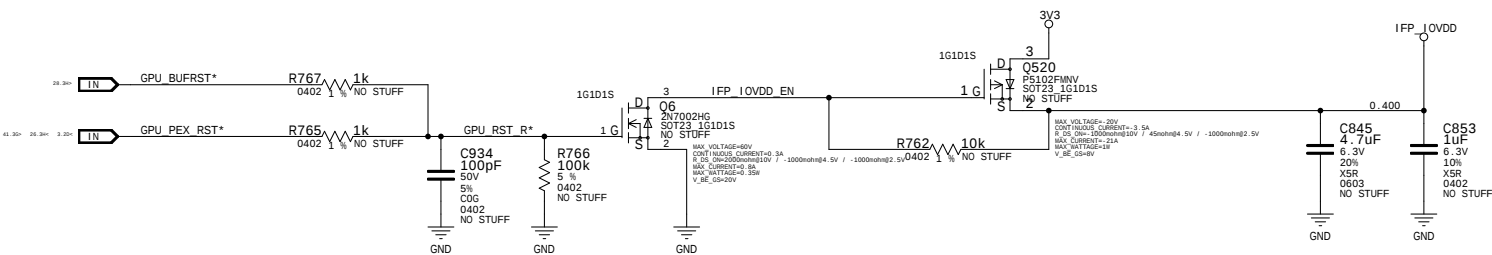
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NV_PN	600-1G600-0030-QS1		
PCB REV	PG600-B02	PAGE	36 OF 41
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Page37: PS: Shutdown & IFP_IOVDD & INPUT POWER CONNECTOR DETECTION

THERM OVERT SHUTDOWN



IFP_IOVDD (backdrive prevention)

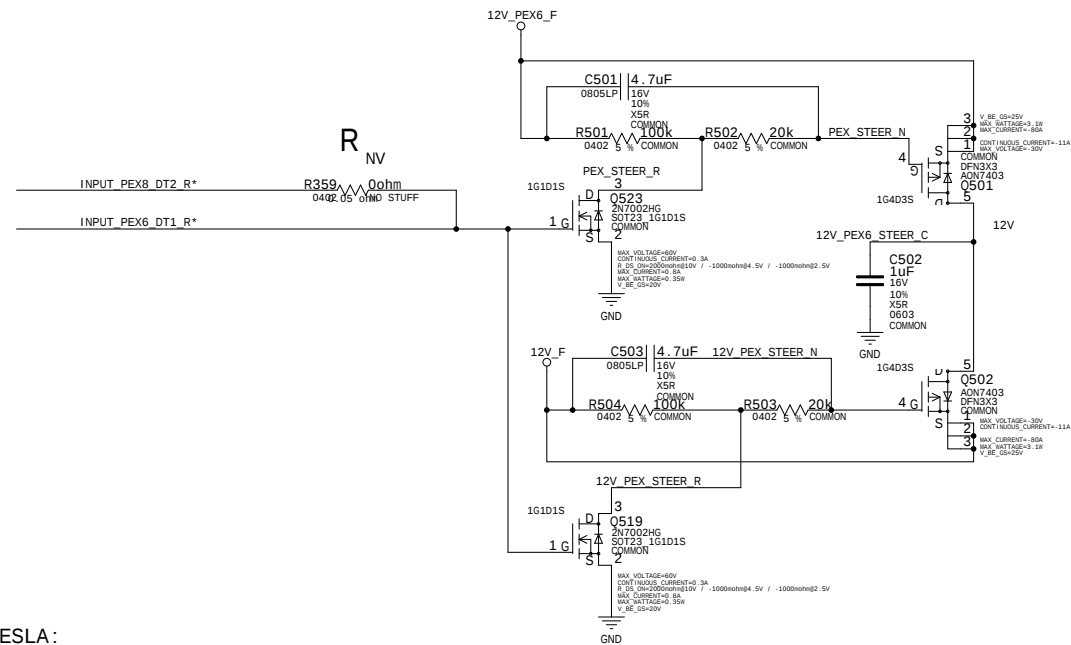


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Page38: PS: 12V Current Steering & Hot Unplug Detect

12V CURRENT STEERING (UNDER POWER BOOT):
GUIDES CURRENT FROM PEX EDGE TO PEX 6 PIN INPUT AREA

For OpenVreg Type4 + Phase Doubler, 2 phase PSI mode



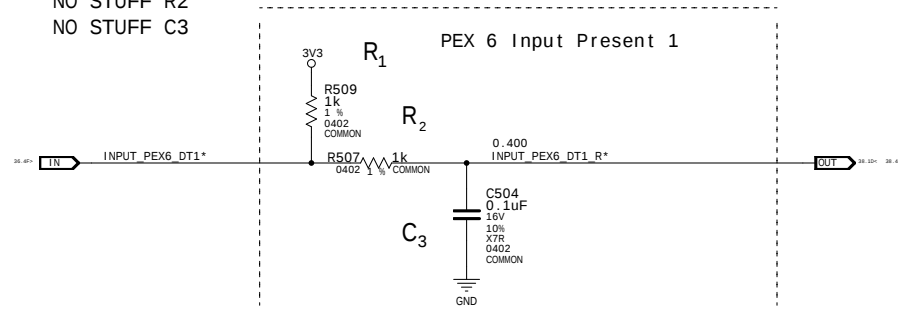
QUADRO / TESLA:

```

PEX 6 INPUT CONNECTOR IS NOT LOADED
PEX 6 INPUT DETECT MUST BE DISABLED
PEX 8 INPUT DETECT MUST BE USED TO CONTROL STEERING
STUFF Rnv IN STEERING CIRCUIT

NO STUFF R1
NO STUFF R2
NO STUFF C3

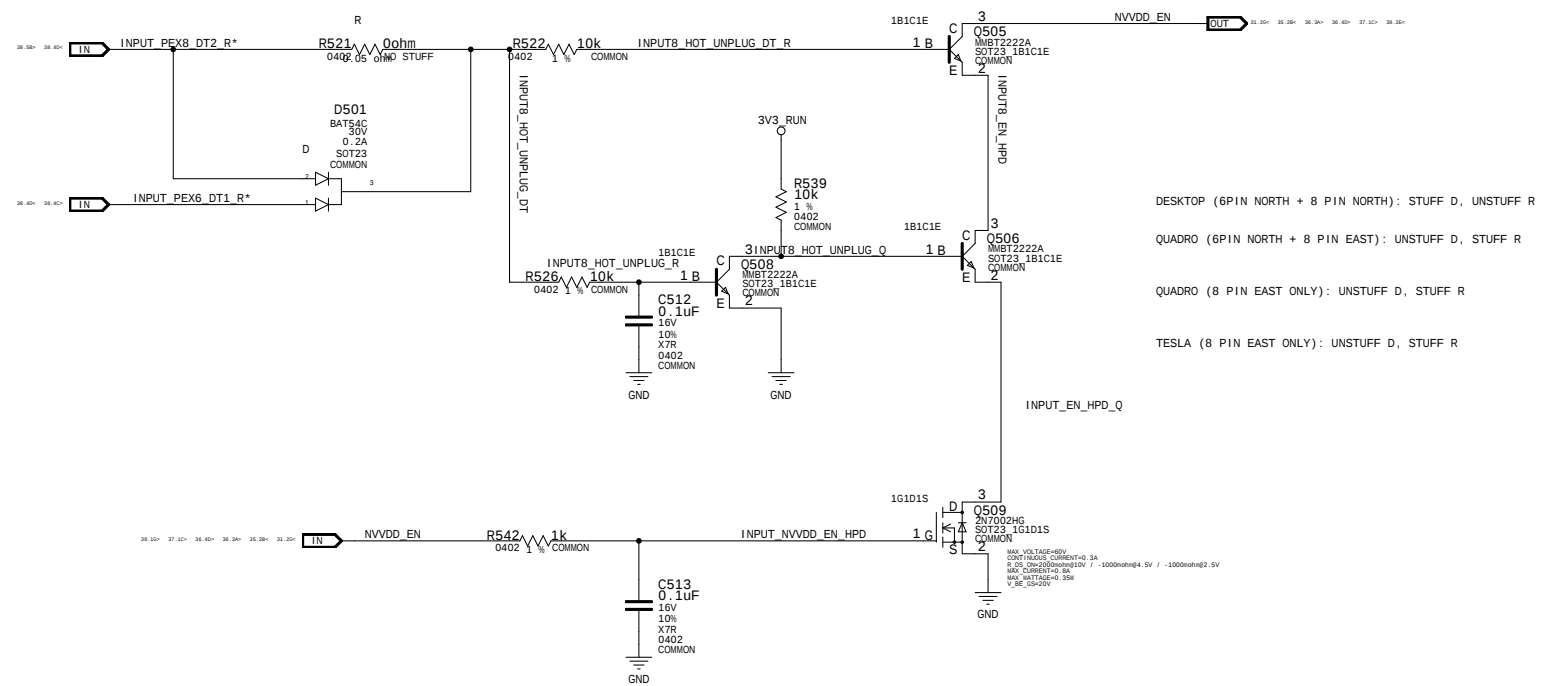
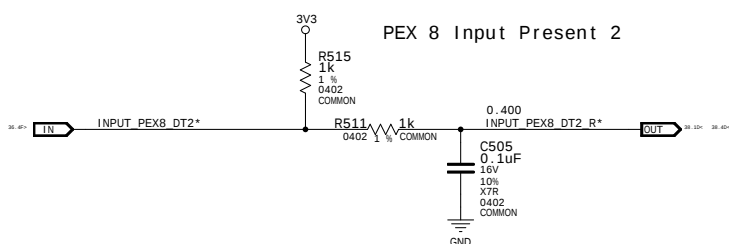
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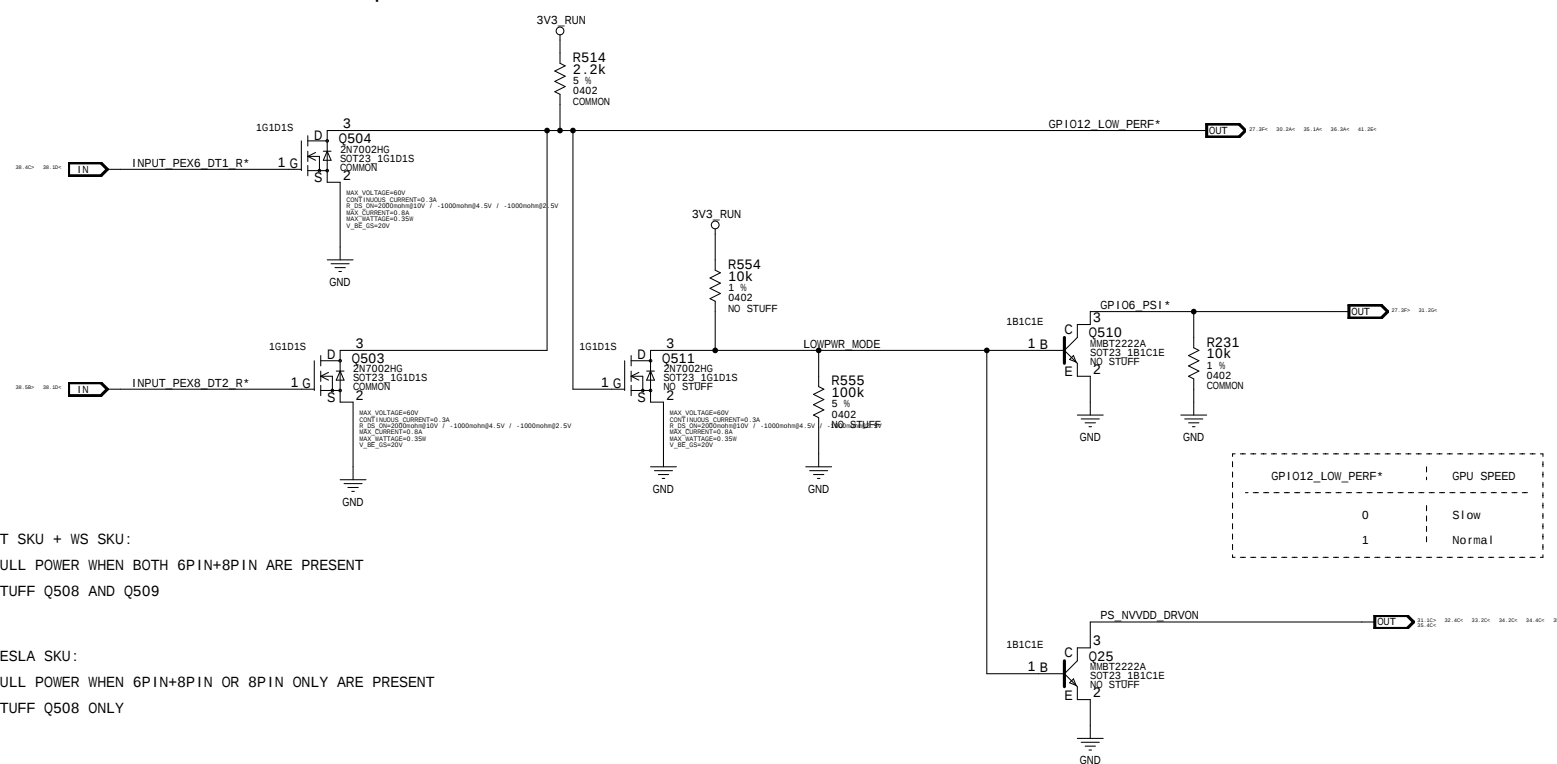
GeFORCE:

PEX 6 INPUT CONNECTOR IS LOADED
PEX 6 INPUT DETECT MUST BE USED TO CONTROL STEERING
NO STUFF Rnv IN STEERING CIRCUIT

STUFF R1
STUFF R2
STUFF C3



PEX Input - Under Power Boot Controls



DT SKU + WS SKU:

FULL POWER WHEN BOTH 6PIN+8PIN ARE PRESENT
STUFF Q508 AND Q509

TESLA SKU:

FULL POWER WHEN 6PIN+8PIN OR 8PIN ONLY ARE PRESENT
STUFF Q508 ONLY

GPI012_LOW_PERF*	GPU SPEED
0	Slow
1	Normal

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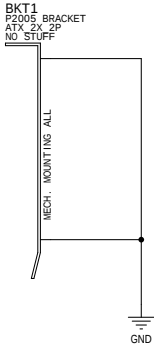
PCB_REV	PG600-B02	PAGE	38 OF 41
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PCB REV	PG0000-B02	PAGE	38 OF 41
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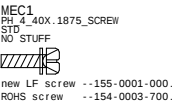
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Brackets:

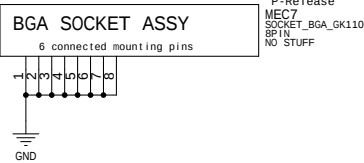
DVIDVI_HDMI_DP : 151-10001-0441-092



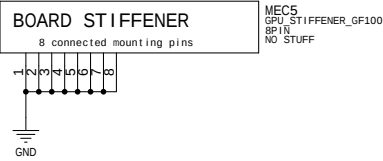
Bracket Screw



GPU SOCKET



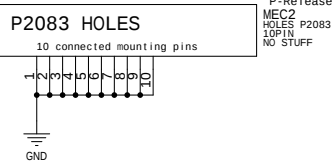
GPU Stiffener (BRING-UP COOLER)



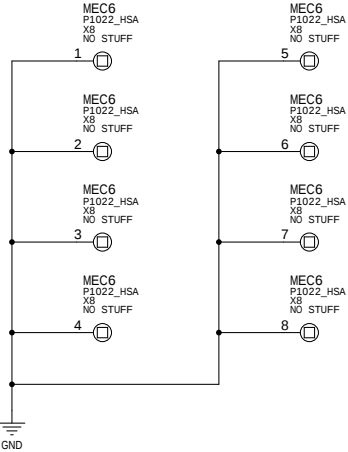
Stiffener

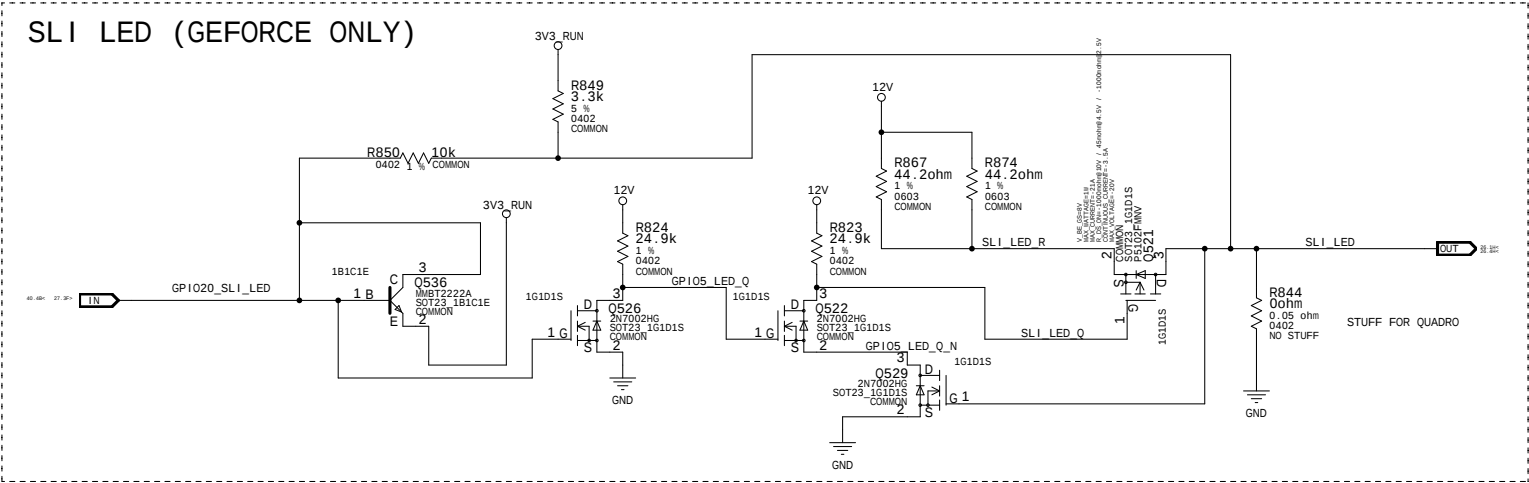
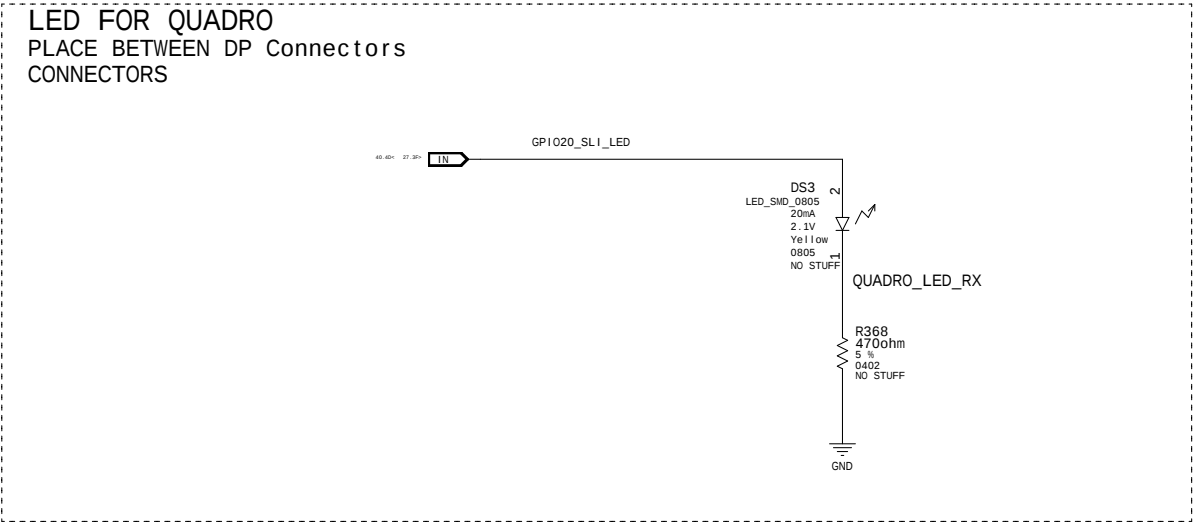
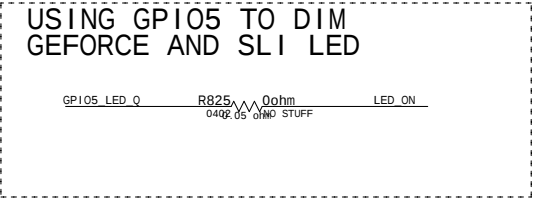
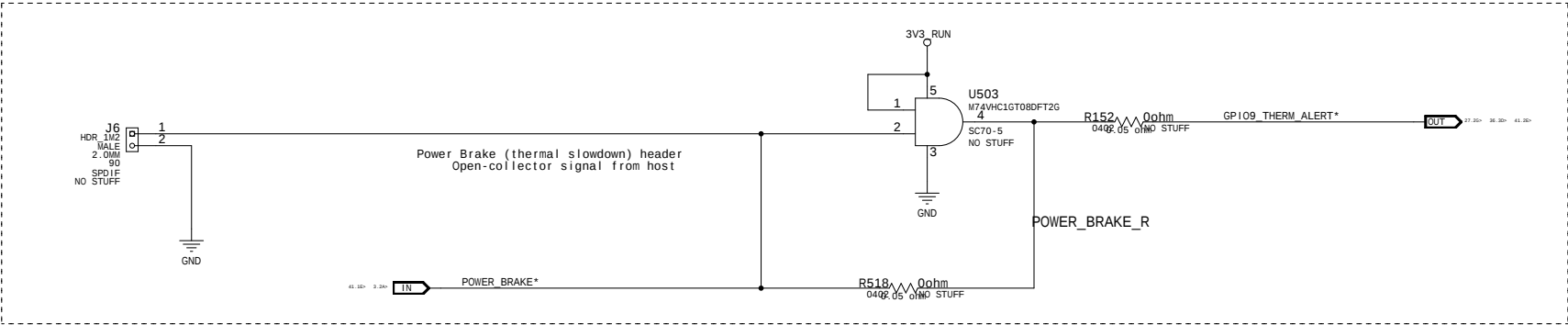
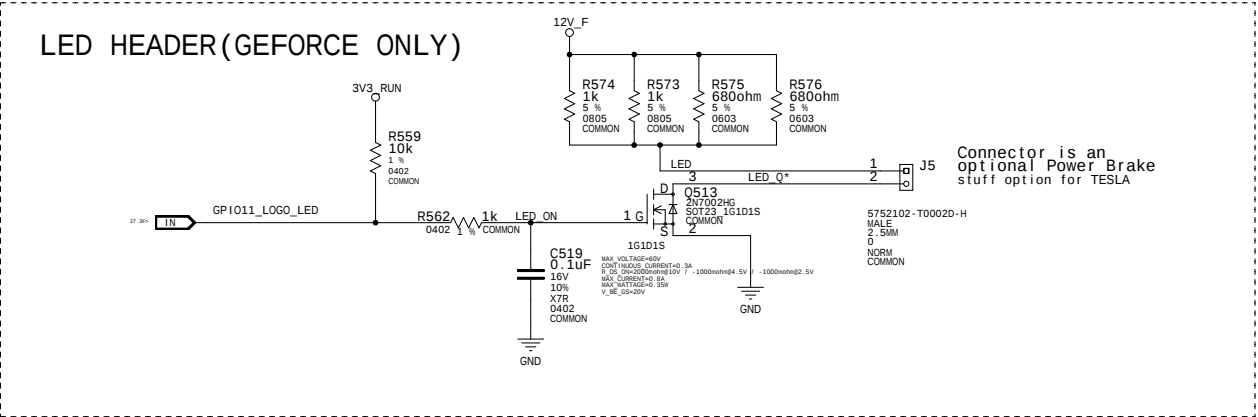


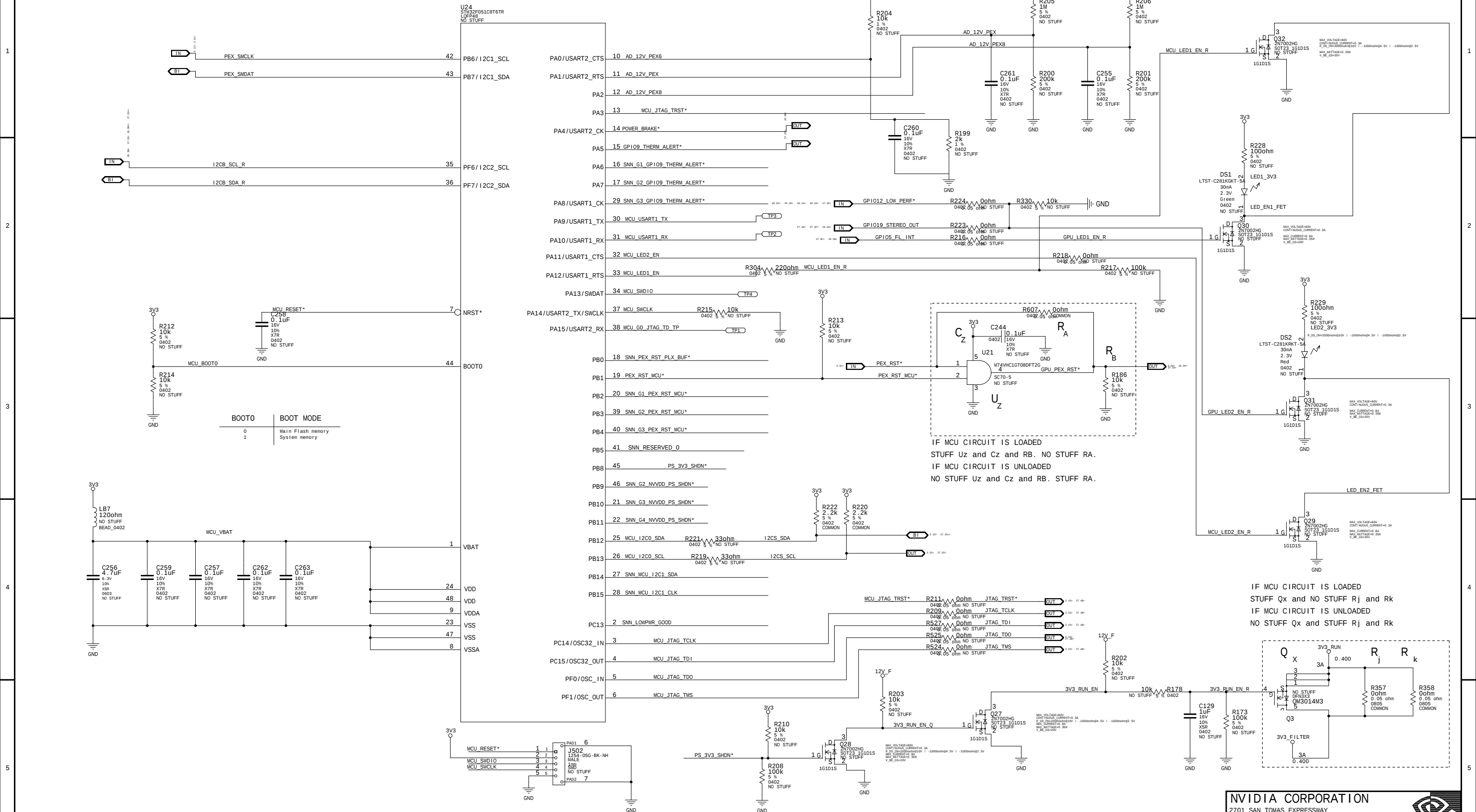
Mechanical Holes Symbol



Bring Up Cooler







ASSEMBLY	
PAGE DETAIL	MICROCONTROLLER

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